3-to-8 line decoder/demultiplexer 74HC/HCT238

FEATURES

- Demultiplexing capability
- Multiple input enable for easy expansion
- Ideal for memory chip select decoding
- Active HIGH mutually exclusive outputs
- Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT238 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT238 decoders accept three binary weighted address inputs (A_0, A_1, A_2) and when enabled, provide 8 mutually exclusive active HIGH outputs (Y_0 to Y_7).
The "238" features three enable inputs: two active LOW ($\overline{E}_1$ and $\overline{E}_2$) and one active HIGH (E_3). Every output will be LOW unless $\overline{E}_1$ and $\overline{E}_2$ are LOW and E_3 is HIGH.

This multiple enable function allows easy parallel expansion of the "238" to a 1-of-32 (5 lines to 32 lines) decoder with just four "238" ICs and one inverter.

The "238" can be used as an eight output demultiplexer by using one of the active LOW enable inputs as the data input and the remaining enable inputs as strobes. Unused enable inputs must be permanently tied to their appropriate active HIGH or LOW state.

The "238" is identical to the "138" but has non-inverting outputs.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/ t_{PLH}	propagation delay	C_L = 15 pF; V_{CC} = 5 V			
	A_n to Y_n		14	18	ns
	E_3 to Y_n		16	20	ns
	$\overline{E}_n$ to Y_n		17	21	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	72	76	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in ∝W):
   $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_i + \sum (C_L \cdot V_{CC}^2 \cdot f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\sum (C_L \cdot V_{CC}^2 \cdot f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

ORDERING INFORMATION

See *"74HC/HCT/HCU/HCMOS Logic Package Information"*.

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 2, 3	A_0 to A_2	address inputs
4, 5	$\overline{E}_1$, $\overline{E}_2$	enable inputs (active LOW)
6	E_3	enable input (active HIGH)
8	GND	ground (0 V)
15, 14, 13, 12, 11, 10, 9, 7	Y_0 to Y_7	outputs (active HIGH)
16	V_{CC}	positive supply voltage

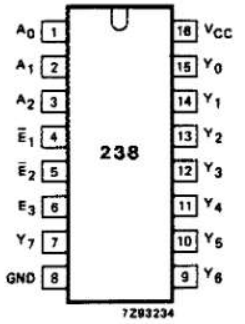


Fig.1 Pin configuration.

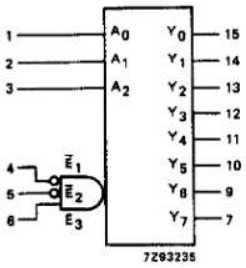
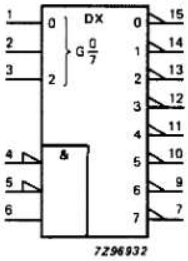
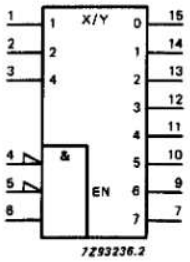


Fig.2 Logic symbol.



(a)



(b)

Fig.3 IEC logic symbol.

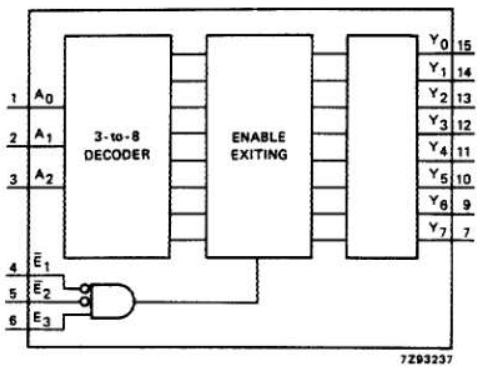


Fig.4 Functional diagram.

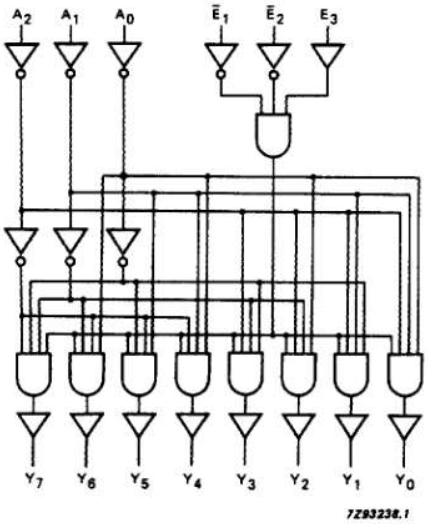


Fig.5 Logic diagram.

FUNCTION TABLE

INPUTS						OUTPUTS							
$\overline{E}_1$	$\overline{E}_2$	E_3	A_0	A_1	A_2	Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7
H	X	X	X	X	X	L	L	L	L	L	L	L	L
X	H	X	X	X	X	L	L	L	L	L	L	L	L
X	X	L	X	X	X	L	L	L	L	L	L	L	L
L	L	H	L	L	L	H	L	L	L	L	L	L	L
L	L	H	H	L	L	L	H	L	L	L	L	L	L
L	L	H	L	H	L	L	L	H	L	L	L	L	L
L	L	H	H	H	L	L	L	L	H	L	L	L	L
L	L	H	L	L	H	L	L	L	L	H	L	L	L
L	L	H	H	L	H	L	L	L	L	L	H	L	L
L	L	H	L	H	H	L	L	L	L	L	L	H	L
L	L	H	H	H	H	L	L	L	L	L	L	L	H

Note

1. H = HIGH voltage level
   L = LOW voltage level
   X = don't care