



August 1986
Revised March 2000

DM74LS283

4-Bit Binary Adder with Fast Carry

General Description

These full adders perform the addition of two 4-bit binary numbers. The sum (Σ) outputs are provided for each bit and the resultant carry (C4) is obtained from the fourth bit. These adders feature full internal look ahead across all four bits. This provides the system designer with partial look-ahead performance at the economy and reduced package count of a ripple-carry implementation.

The adder logic, including the carry, is implemented in its true form meaning that the end-around carry can be accomplished without the need for logic or level inversion.

Features

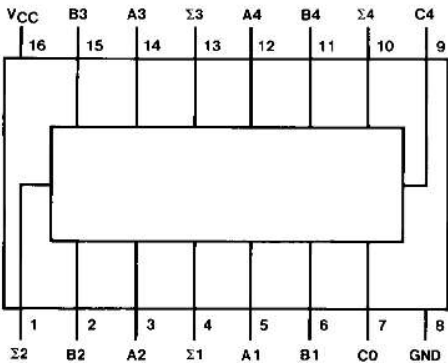
- Full-carry look-ahead across the four bits
- Systems achieve partial look-ahead performance with the economy of ripple carry
- Typical add times
 - Two 8-bit words 25 ns
 - Two 16-bit words 45 ns
- Typical power dissipation per 4-bit adder 95 mW

Ordering Code:

Order Number	Package Number	Package Description
DM74LS283M	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
DM74LS283N	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram



DM74LS283 4-Bit Binary Adder with Fast Carry

DM74LS283

Function Table

Input				Outputs					
				When C0 = L			When C0 = H		
				When C2 = L			When C2 = H		
A1	B1	A2	B2	Σ1	Σ2	C2	Σ1	Σ2	C2
A3	B3	A4	B4	Σ3	Σ4	C4	Σ3	Σ4	C4
L	L	L	L	L	L	L	H	L	L
H	L	L	L	H	L	L	L	H	L
L	H	L	L	L	H	L	L	H	L
H	H	L	L	L	H	L	L	H	L
L	L	H	L	L	L	L	H	L	L
H	L	H	L	L	L	L	H	L	L
L	H	H	L	L	L	L	H	L	L
H	H	H	L	L	L	L	H	L	L
L	L	L	H	L	H	H	L	L	H
H	L	L	H	L	H	H	L	L	H
L	H	L	H	L	H	H	L	L	H
H	H	L	H	L	H	H	L	L	H
L	L	H	H	L	L	H	H	L	H
H	L	H	H	L	L	H	H	L	H
L	H	H	H	L	L	H	H	L	H
H	H	H	H	L	L	H	H	L	H

H = HIGH Level, L = LOW Level
Input conditions at A1, B1, A2, B2, and C0 are used to determine outputs Σ1 and Σ2 and the value of the internal carry C2.
The values at C2, A3, B3, A4, and B4 are then used to determine outputs Σ3, Σ4, and C4.

Logic Diagram

