


### General Conventions:

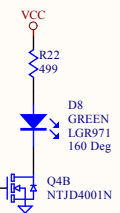
Signal names beginning with a '/' are active low

Unless Specified Otherwise:

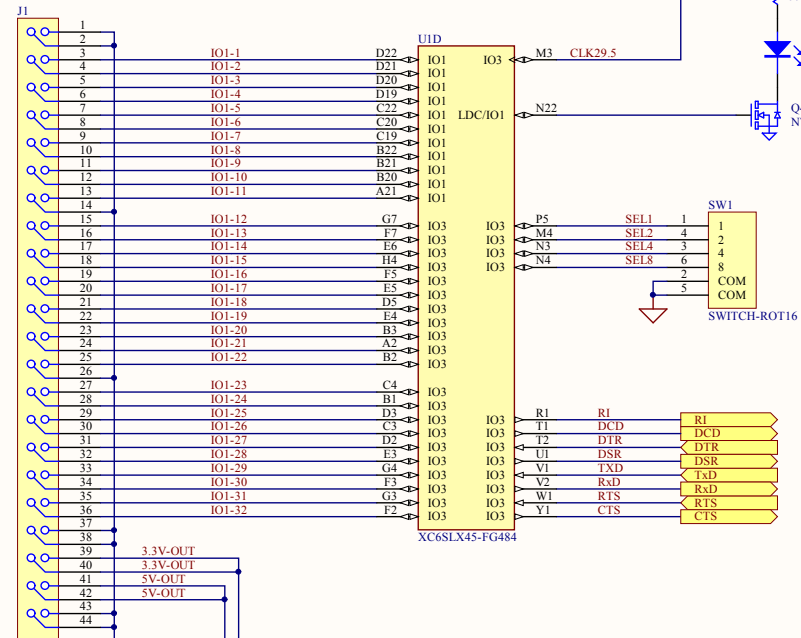
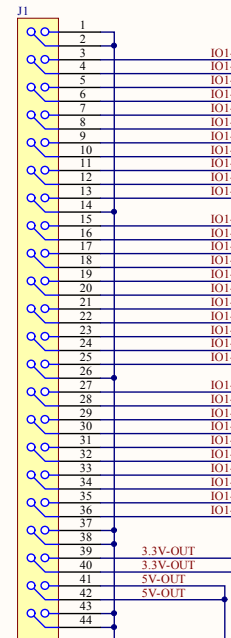
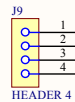
- All resistors are 1% metal film, 1/10W, in 0603 package
- All non-polarized capacitors are ceramic, in 0603 package
- All ceramic capacitors up to and including 1,000pF are NPO, 50V or higher, 5% or better
- All ceramic capacitors over 1,000pF up to and including 1.0uF are X7R, 16V or higher, 10% or better
- All ceramic capacitors over 1.0uF are of the specified type and voltage
- All polarized capacitors are of the specified type and voltage

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Part No:	Rev: 1.1	Print Date: 10/27/2010	
File Name: S01.SchDoc			
			Sheet 1 of 6

## F

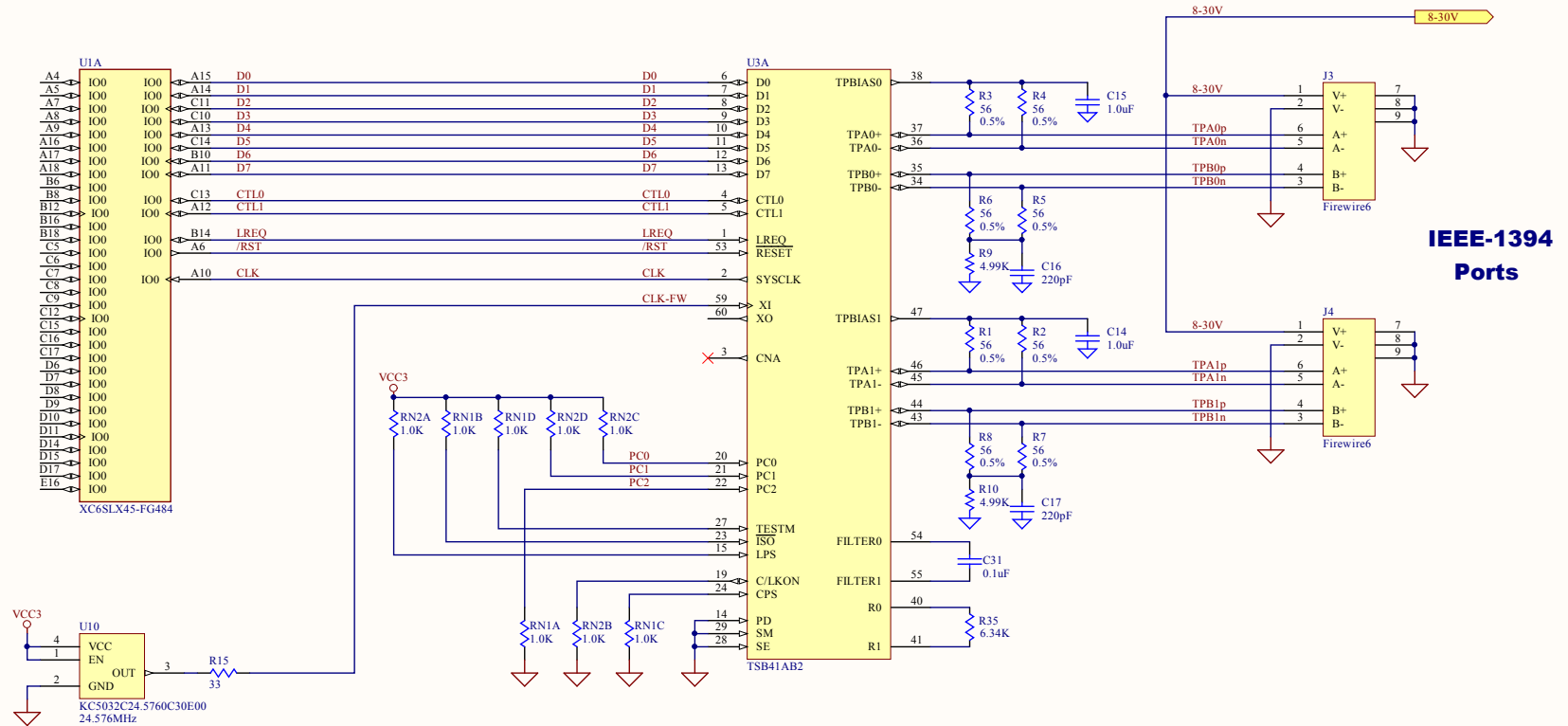


## Soft JTAG Port



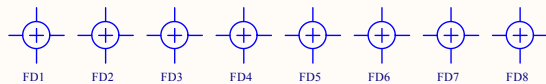
F

# FireWire Controller & Connectors

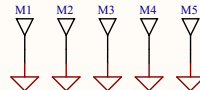



**IEEE-1394  
Ports**

**Fiducials**



**Mounting  
Holes**



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Part No:	Rev: 1.1	Print Date: 10/27/2010	
File Name: S03.SchDoc			

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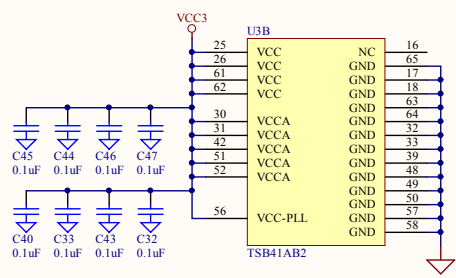
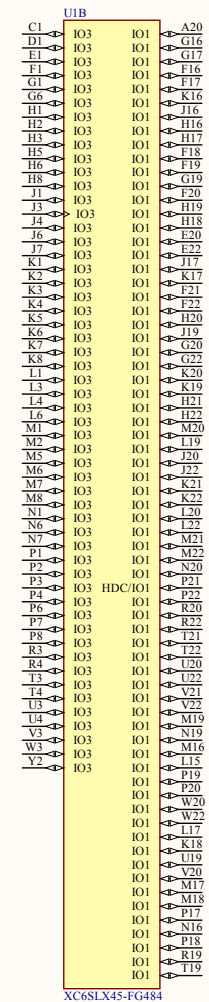
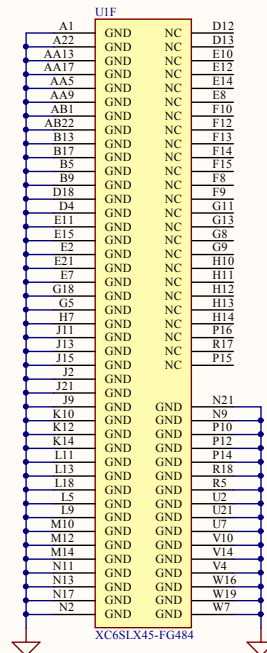
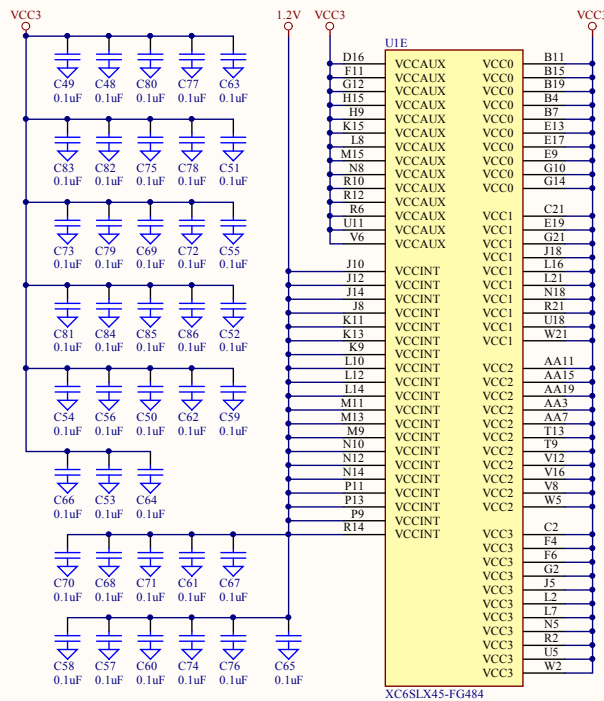
Drawing Title:  
IEEE-1394 FPGA Controller

Sheet:  
3

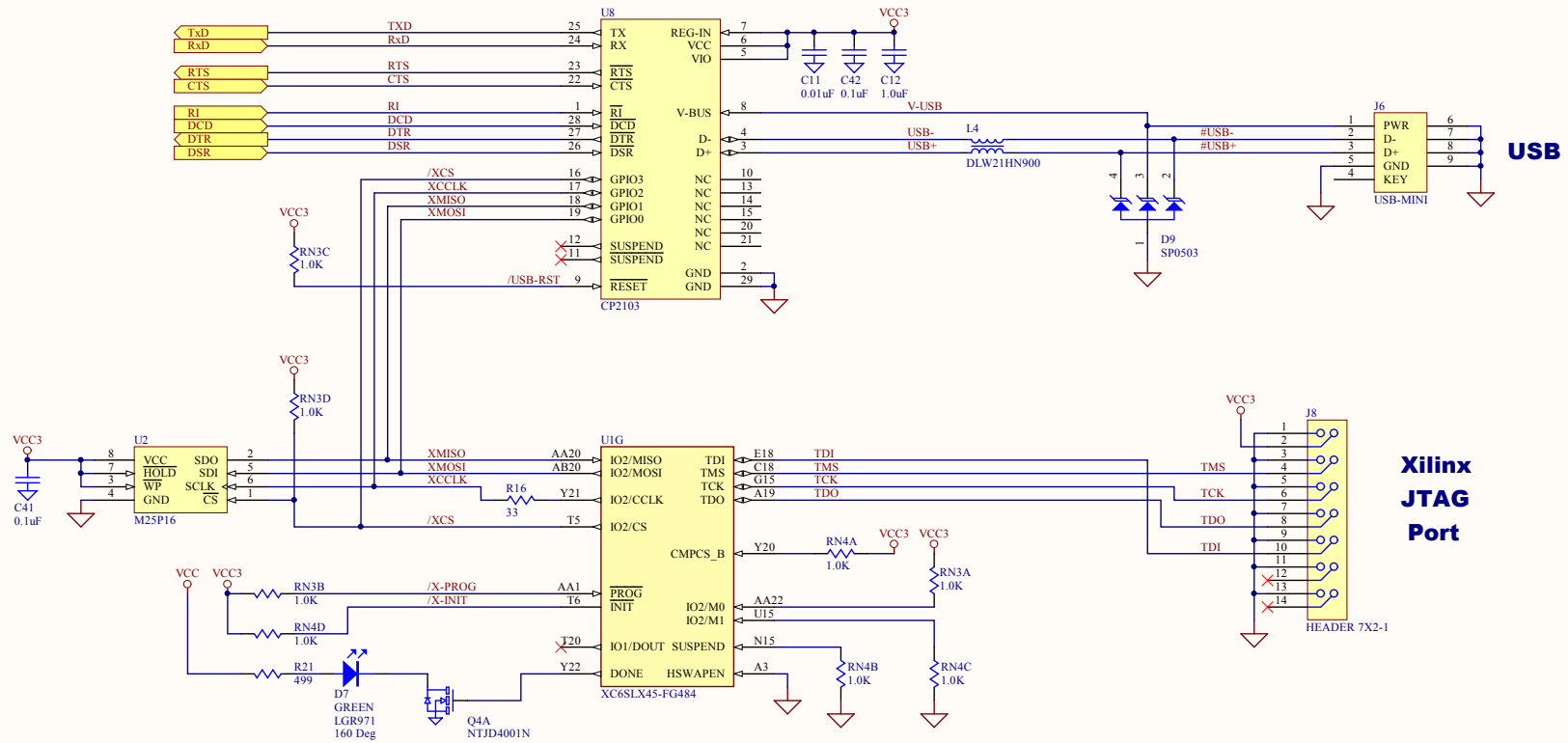
Rev:  
1.1

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# Power Pins & Unused



# JTAG Port



**Xilinx  
JTAG  
Port**

## Power Supplies

