Name:
Id:

Digital Logic Design Laboratory: CSE 1326
In Class Final Assignment
Total Marks: 10, Duration: 25 mins = 15 min writing + 10 min upload
[Maintain question sequence. Write answers only on one (1) page. All questions worth 1 point except Q 5.]

1. What connection we need to make a J-K flip flop output toggle (complement) in every clock pulse?

2. What is the main function of a MUX?

3. Here are the inputs to a 2 2-bit binary full adders:
   C_0=0,
   A_3=1, A_2=0, A_1=1, A_0=0
   B_3=1, B_2=1, B_1=1, B_0=0?

   What will be the outputs: (C_{out}, S_3, S_2, S_1, S_0)?

4. Draw clock pulse, and show the positive edge?

5. Draw the diagram of a 3-bit downward ripple counter using +ve edge J-K flip flop. [2]

True/False (Write T or F next to the question number):

6. Three flip-flops are required to detect the sequence '11010' from an input bit stream.
7. Registers can store only one bit.
8. Decoder takes n inputs and provides 2^n outputs?
9. Synchronous counters are called synchronous because all the flip-flops are connect from the same clock.