United International University
Department of CSE
CSE 313: Computer Architecture
Midterm Examination
Spring 2022

Time: 1 hour and 45 minutes **Full Marks: 30**

[Any examinee found adopting unfair means will be expelled from the trimester / program as per UIU disciplinary rules.]

[N.B.: Answer all the questions. Assume any data if it is not mentioned explicitly.]

1. a) For the same program, two different compilers are used. The table below shows the execution time of the two different compiled programs. [4]

	Compiler A		Compiler B	
	Number of instructions	Execution Time	Number of instructions	Execution Time
Program 1	$1x10^9$	1s.	$1.2x10^9$	1.4s
Program 2	$1x10^9$	0.8s	$1.2x10^9$	0.7s

i) Find the average CPI for each program given that the processor has a clock cycle time of 1ns.

ii) Use the average CPIs found in part (i), but that the compiled programs run on two different processors. If the execution times on the two processors are the same (5s), how much faster is the clock of the processor running compiler A's code versus the clock of the processor running compiler B's code?

b) Suppose, there are three classes of instructions A, B, C in a particular instruction set architecture with CPIs 1.2, 2 and 2.5 respectively. The number of instructions from each class in two separate programs are as follows: [4]

Programs	Instruction classes		
	A	B	C
P1	40	10	16
P2	12	13	40

CPU time = num. of instruction * cycle Period

num of instruction = IC * CPI

If the clock frequency is 2GHz, then what is the total execution time for P1? If the total time for P1 is 100 ns, then find out the improvement factor to make it two times faster.

c) What is the power wall? Explain how the introduction of multi core processors has overcome power limitation. [2]

2. Consider the following C function that calculates the sum of an array, *arr*, from index *low* to index *high*. Given that the base address of *arr* is contained in register *$s0*, the variable i and sum is contained in register *$s1* and *$s2* respectively. The starting MIPS assembly instruction address is 1000.

```
int func(int low , int high)
{
    int sum = 0,i;
    for(i = low ; i < high ; i++)
    {
        sum = sum + arr[i];
    }
    return sum;
}
```

a) Convert the code to the corresponding MIPS assembly instructions [6]

b) Convert the first 15 lines of your assembly instructions to corresponding machine code. No need to convert it to binary. [5]

c) A processor architect makes the following claim "The maximum array size that MIPS can handle is 32, as there are only 32 possible registers in MIPS to hold data." Briefly describe how arrays are stored in MIPS. In your answer, include the instructions that are used to access arrays. Based on this, explain if the architect's claim is correct. And find out what is the maximum array index size we can access in MIPS architecture? [4]

3. a) Assuming 4 bit architecture and using the division algorithm show each step of the division of 13 by 6. [3]

b) Optimized multiplication is better than the normal multiplication algorithm. Why? Explain. [2]

13 = 1101
6 = 110
A, Q: 0000, 1101
13/6
M = 110