United International University (UIU)
Department of CSE
CSE 313: Computer Architecture
(Summer 2020) Section B
CT-4

Full Marks: 20 Time: 35 min (+10 min for submission)

Answer all the questions. Your answer script must contain your name and ID.

If any portion of answer is found to be copied from other scripts, both will be marked as zero regardless of other answers.

1. Explain the difference between State elements and Combinational elements. 5
   State element= Output depends on input + state (Register Module)
   Combinational element = Output depends on input only (ALU)
2. For the instruction addi, what will be the control bit values of RegDst, Branch, MemRead, MemtoReg, ALUOp, MemWrite, ALUSrc, and RegWrite? 5
   RegDst(0), Branch(0), MemRead(0), MemtoReg(0), ALUOp(00), MemWrite(0), ALUSrc(1), and RegWrite(1) 5
3. Write the steps of executing the instruction: addi 5
   - rs and rt loaded, rt contains the destination address
   - Constant is provided as ALU operand after sign extension
   - ALU performs add
   - ALU result is put in write data of register
4. Suppose the data path of a process is divided into the following five stages-

Stage	Time (ps)
Instruction Fetch	250
Instruction Decode	200
ALU Operation	300
Memory Write	350
Write Back	250

   a. Calculate the clock cycle time for-
      i. Single cycle Data path. = 1350
      ii. Pipelined Data Path. = 350
   b. If five stages of pipeline is applied in the data-path, calculated the-
      i. expected speedup = 1350/350 = 3.85
      ii. actual speedup (Worst Case) = 1350/(1750) = 0.77