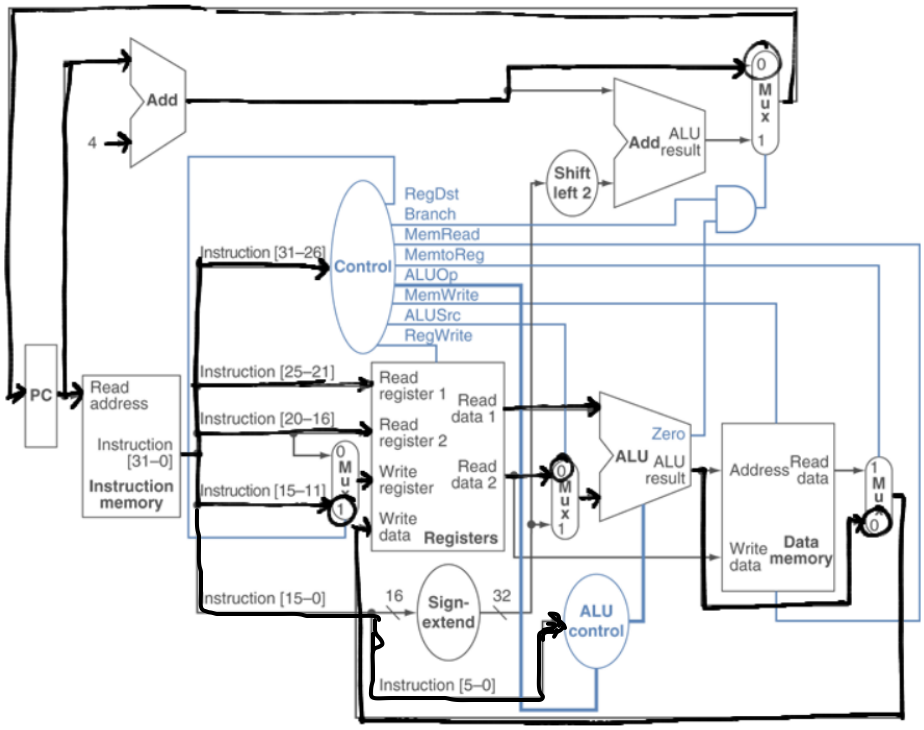
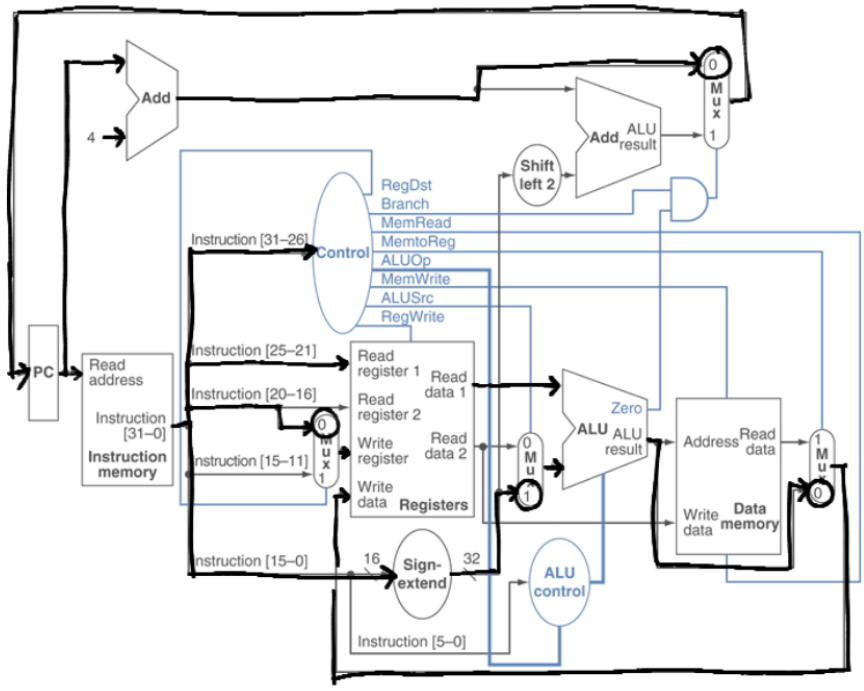
Taimur Rahman - 011221427
Wasimul Karim - 011211105

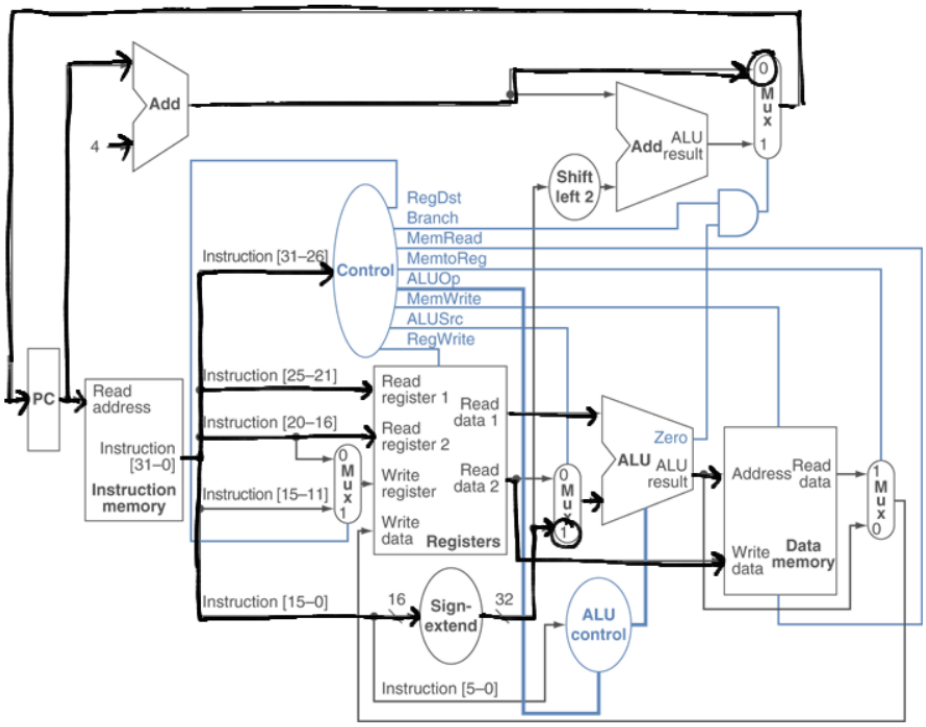
add	**ALUsrc = 0** **ALUOp = add/sub/etc** **RegDst = 1** **MemtoReg = 0** **RegWrite = 1** **Branch = 0**
sub	
and	
or	
nor	



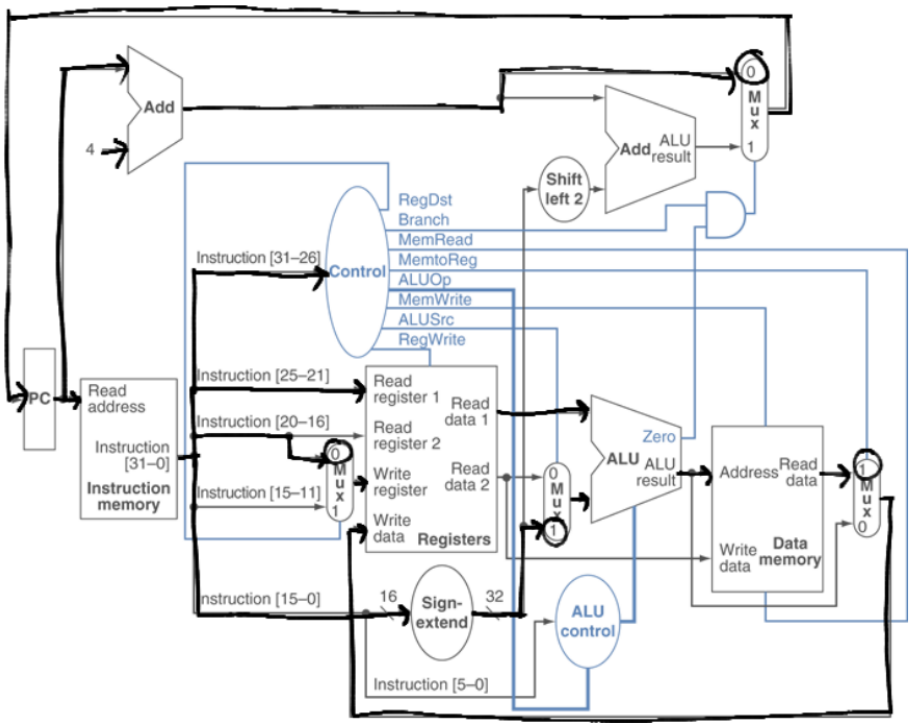
addi andi ori	ALUsrc = 1 ALUOp = add/and/or RegDst = 0 MemtoReg = 0 RegWrite = 1 Branch = 0



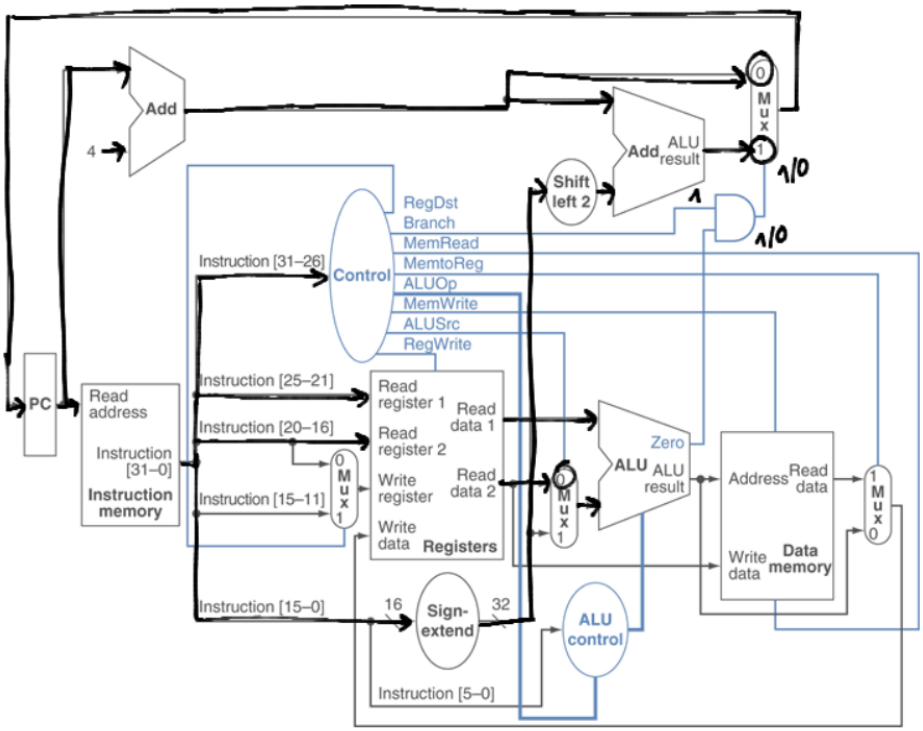
sw	**ALUsrc = 1** **ALUOp = add** **MemWrite = 1** **Branch = 0**



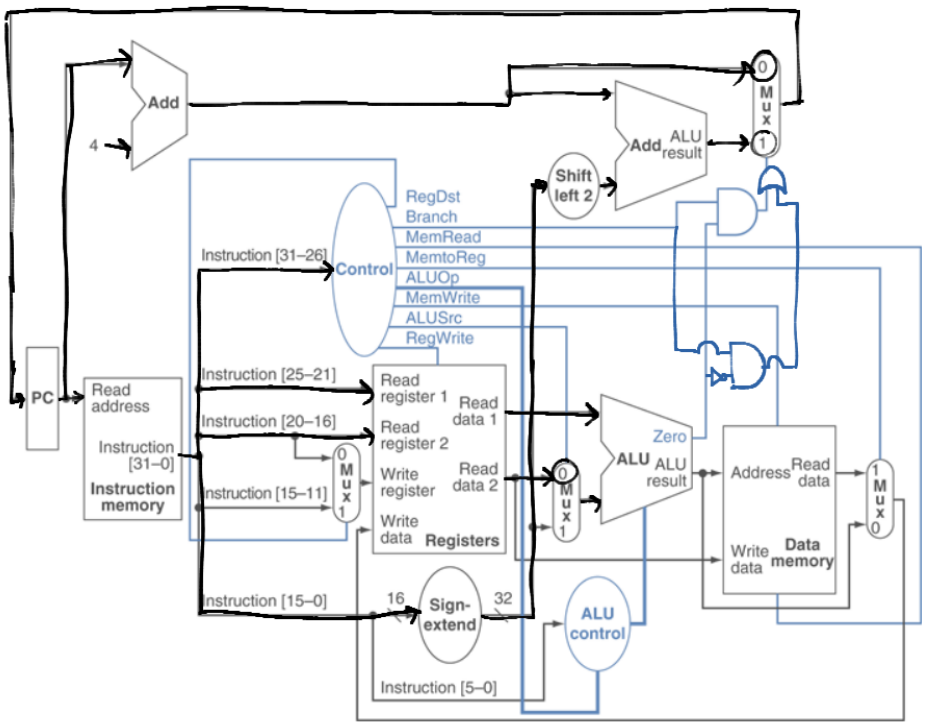
lw	**ALUsrc = 1** **ALUOp = add** **MemRead = 1** **MemToReg = 1** **RegDst = 0** **RegWrite = 1** **Branch = 0**



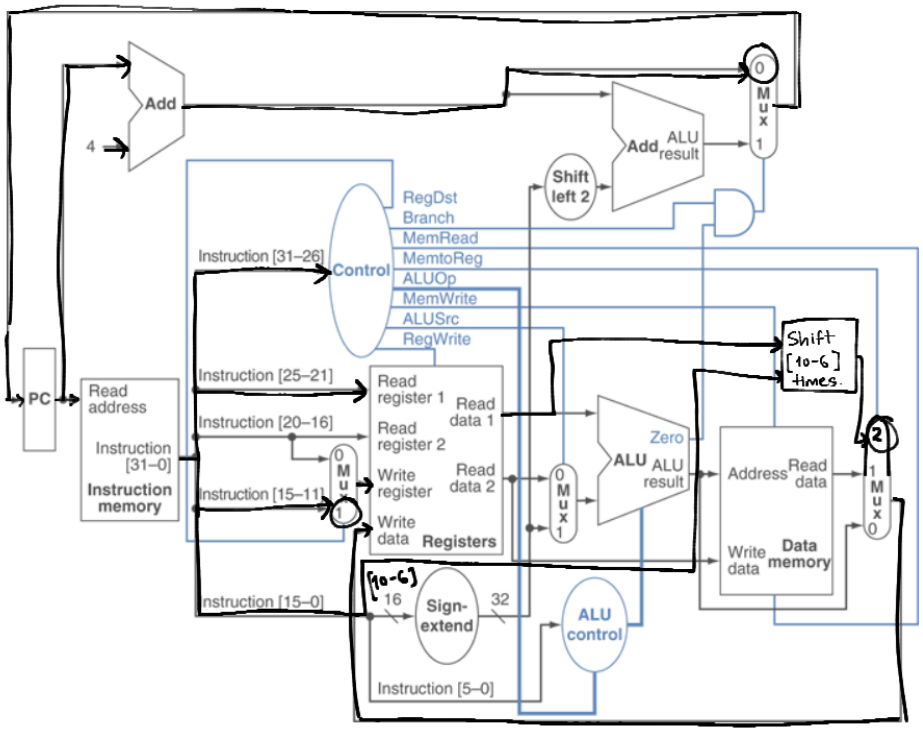
beq	**ALUsrc = 0** **ALUOp = sub** **Branch = 1**



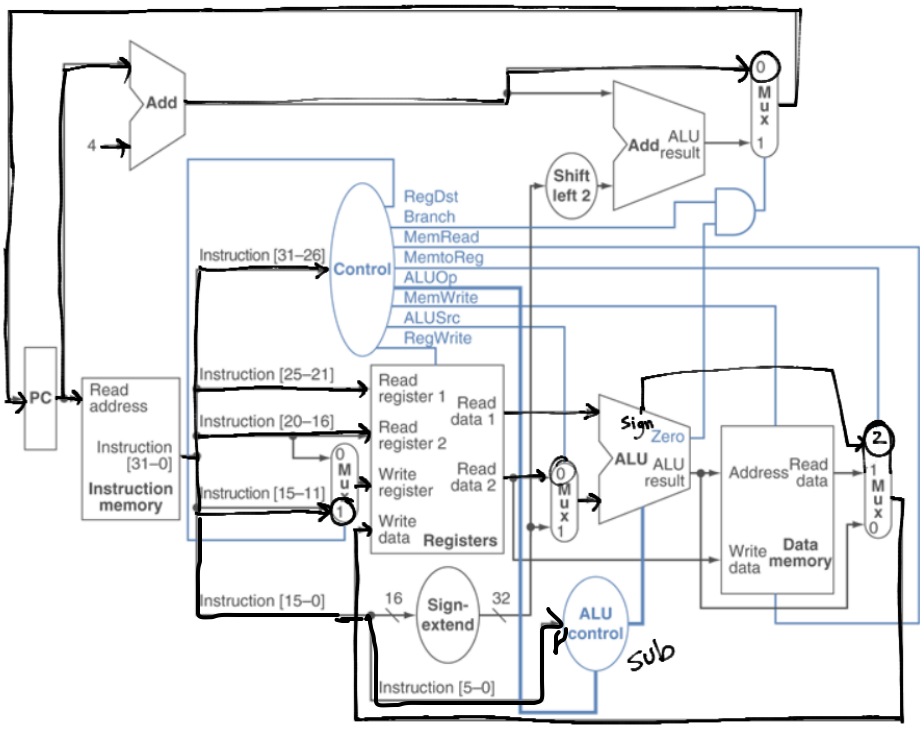
bne	**ALUsrc = 0** **ALUOp = sub** **Branch = 1**



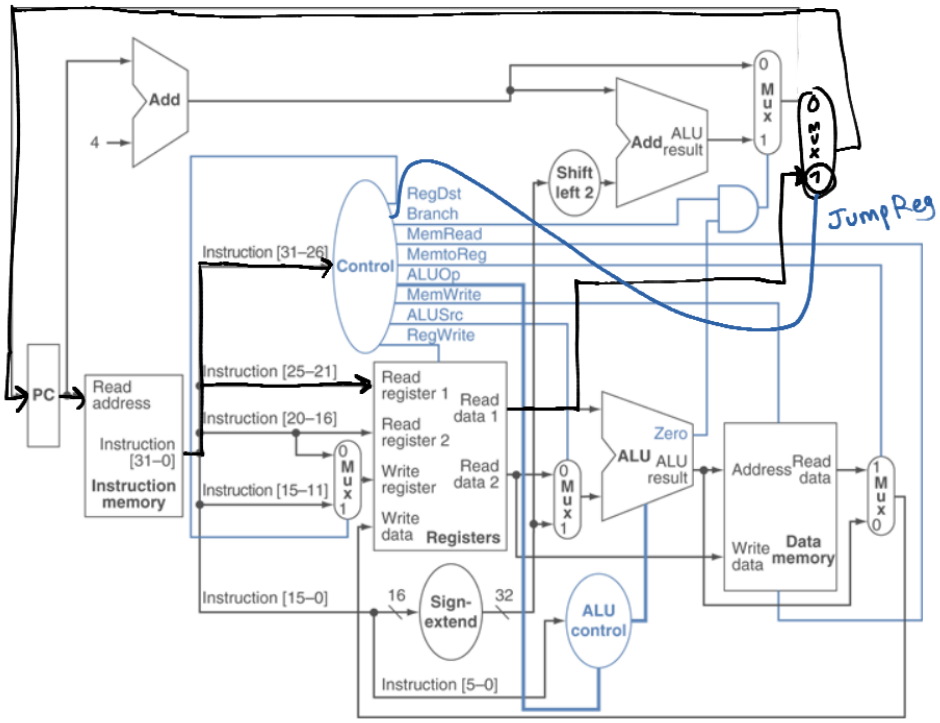
sll **srl**	**MemToReg = 2** **RegDst = 1** **RegWrite = 1** **Branch = 0**



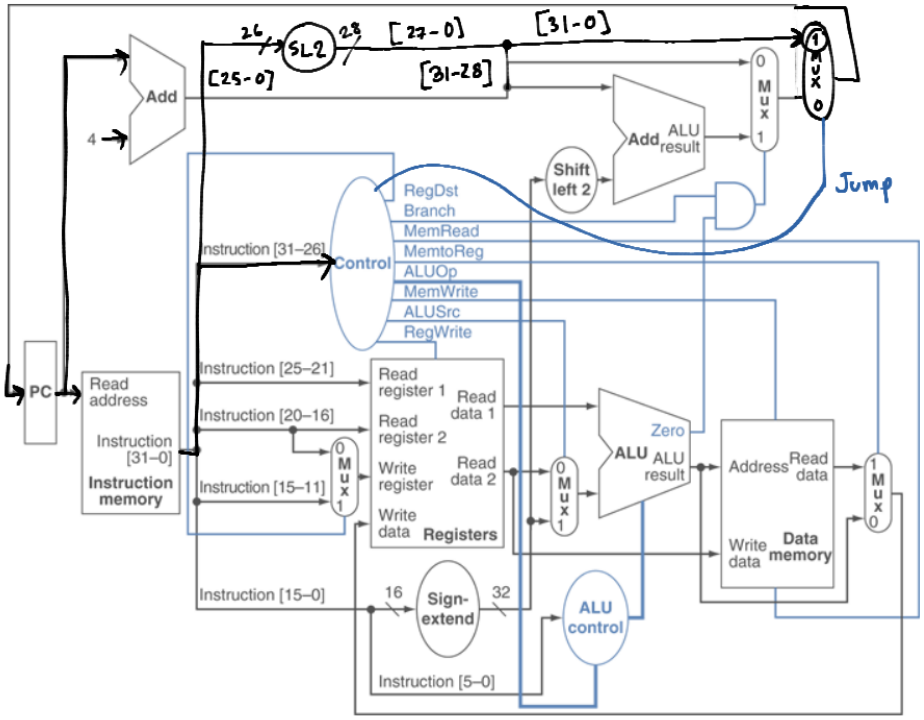
slt	**RegDst = 1** **ALUsrc = 0** **ALUOp = sub** **MemToReg = 2** **RegWrite = 1** **Branch = 0**



jr	JumpReg = 1


Add
4
Add
ALU result
0
M
u
x
1
Shift left 2
JumpReg
RegDst
Branch
MemRead
MemtoReg
ALUOp
MemWrite
ALUSrc
RegWrite
Instruction [31–26]
Control
PC
Read address
Instruction [31–0]
Instruction memory
Instruction [25–21]
Instruction [20–16]
Instruction [15–11]
Instruction [15–0]
Instruction [5–0]
Read register 1
Read register 2
Write register
Write data
Read data 1
Read data 2
Registers
16
Sign-extend
32
ALU control
Zero
ALU
ALU result
Address
Read data
Write data
Data memory

j	**Jump = 1**


26
SL2
28
[27-0]
[31-0]
[25-0]
[31-28]
Add
4
Add
ALU result
Shift left 2
Jump
RegDst
Branch
MemRead
MemtoReg
ALUOp
MemWrite
ALUSrc
RegWrite
Instruction [31–26]
Control
PC
Read address
Instruction [31–0]
Instruction memory
Instruction [25–21]
Instruction [20–16]
Instruction [15–11]
Instruction [15–0]
Instruction [5–0]
Read register 1
Read register 2
Write register
Write data
Read data 1
Read data 2
Registers
16
Sign-extend
32
ALU control
Zero
ALU
ALU result
Address
Read data
Write data
Data memory
M u x

jal	**Jump = 1** **MemToReg = 2** **RegDst = 2** **RegWrite = 1**