United International University

Department of CSE
CSE 313: Computer Architecture
Final Examination
Summer 2020

Time: 1 Hour 15 minutes **Full Marks: 25**

Any examinee found adopting unfair means will be expelled from the trimester / program as per UIU disciplinary rules.

[N.B.: Answer all the questions. Assume any data if it is not mentioned explicitly.]

1. **Modify** the block diagram for a single-cycle data path so that it can execute the following instruction. Note that, the job of the given instruction is to store '1' or '0' in a destination register after comparing two source registers. If **both source registers are equal** it will store '0' in the destination register otherwise it will store 1. **[5]**

2. a) Find out the required time to execute the following instruction based on the given table of different stages of pipeline. However, you have **not implemented forwarding** this time. Now draw the timing diagram assuming that you have **implemented pipelining**. **[5]**

Stage	IF	ID	EX	MEM	WB
Time(ps)	200	150	200	300	150

lw $s0, $t0, $s1

add $s2, $s0, $t1

or $s3, $s3, $t2

and $t2, $s1, $s3

addi $t0,$s1,$s3

b) For instructions given in question no 2(a), find out the total time required in number of cycles, where you will **have to implement forwarding**. **[5]**
[**Note** : There is no need to draw the timing diagram]

3. a) Consider a cache memory of size 4KB and block size having 4 words (1 word = 4 bytes). Determine the **miss rate** if the following bytes are addressed sequentially. **[5]**

10, 15, 20, 4090, 5000

b) If we **change the block size** in Q3(a) to **8 words**, what effect does it have on the **miss rate**? Does the miss rate increase or decrease? For which **principle of locality** does it occur? Explain. **[3+2]**