United International University
Department of Computer Science and Engineering

CSE 313: Computer Architecture

Final Examination Set: A Time: 2 Hours

1. (a) Write down the purpose of using **Multiplexer Unit** or `MUX` in a processor? Give one example from **MIPS processor** given in Figure 1. [2]

   (b) Write down the value of the **Branch** and **Zero** control signals for executing a successful `BEQ` instruction - [2]

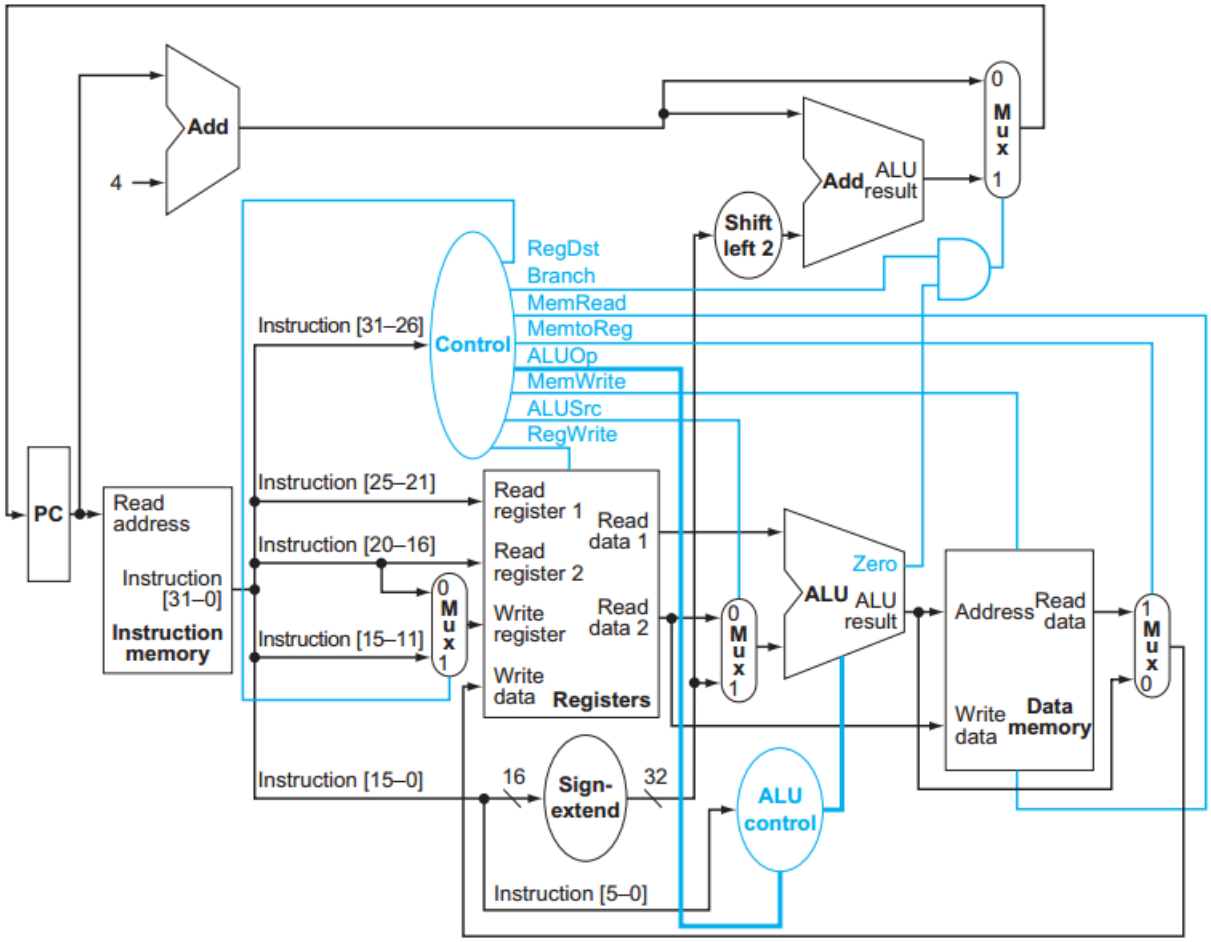

Figure 1: Basic MIPS Processor

(c) Suppose, You have designed a pipelined processor with the following **six stages**- Fetch, Register Read, Memory Read, Execution, Memory Write, Register Write. The following table Table 1: Processor Pipeline Stages contains the time required for each stage for different type of instructions. [4]
Assume there are **no pipeline hazards**. Calculate the time required for executing the following set of instructions of Table 2 using the **pipelined processor you have designed**.

(d) Calculate how much time it would require for the same set of instructions of Table 2 to be executed in a **non-pipelined processor**? [2]

Instruction	Fetch	Reg Read	Mem Read	Execution	Mem Write	Reg Write
add	100 ps	150 ps		150 ps		100 ps
addi	100 ps	150 ps	200 ps	150 ps		100 ps
lw	100 ps	150 ps	200 ps	150 ps	250 ps	
bne	100 ps	150 ps		150 ps		

Table 1: Processor Pipeline Stages

```
addi $5, $0, 10
L1:
    add  $1, $2, $3
    lw   $3, 100($2)
    addi $5, $5, -1
    bne  $5, $0, L1
```

Table 2: Instructions

2. (a) Your friend who is a fan of non-pipelined processor has warned you about some inherent problems about pipelining scheme. He also warned you about some problems which can not be solved by either simple hardware level changes or software level changes. What is the **type of Hazard** your friend was talking about? Write down an example scenario where pipelined processor can fail in such way. [2]

   (b) Give one example of **Double Data Hazard** [2]

   (c) The conditions for forwarding units are given for your convenience. [3+3]

```
EX hazard::
if (EX/MEM.RegWrite and (EX/MEM.RegisterRd != 0)
and (EX/MEM.RegisterRd = ID/EX.RegisterRs)){
    ForwardA = 10;
    EX = 1;
}
if (EX/MEM.RegWrite and (EX/MEM.RegisterRd != 0)
and (EX/MEM.RegisterRd = ID/EX.RegisterRt)){
    ForwardB = 10;
    EX = 1;
}
MEM hazard::
if (MEM/WB.RegWrite and (MEM/WB.RegisterRd != 0)
and (MEM/WB.RegisterRd = ID/EX.RegisterRs))
and (EX != 1)
    ForwardA = 01
if (MEM/WB.RegWrite and (MEM/WB.RegisterRd != 0)
and (MEM/WB.RegisterRd = ID/EX.RegisterRt))
and (EX != 1)
    ForwardB = 01
```

Complete the following tables with the value of **Forwarding Unit**for detecting data hazards in the following instructions.

i.

Instruction	ForwardA	ForwardB
`sw $5, 50($4)`		
`add $5, $3, $1`		
`sub $2, $5, $1`		

ii.

Instruction	ForwardA	ForwardB
`lw $3, 100($10)`		
`and $4, $1, $2`		
`or $5, $4, $3`		

3. (a) Write down the representation of -111.101011 in **single precision IEEE 754** standard floating point variable. Clearly mention all the parts of the IEEE 754 standard and also **mention how many bits** are in segment . [3]

   (b) Calculate the sum of 11.1010112^{-3} and 0.10012^{4} using the binary addition formula with result **upto 6 significant binary bits**. Mention the value at each step of the operation. [4]

   (c) What is **De-Normalized** Number? How do we represent De-Normalized number in IEEE 754 format? [2+1]

4. (a) An ideal memory requires to be as **fast** as a Cache Memory and as **cheap** as an Hard Disk. But this type of device is not possible in reality. How can one use existing devices and yet create cost efficient and speedy memory system? Write down the **principles** which are exploited for such systems to function. [1+1]

   (b) A Hard Disk has average seek time of 100μs. The rotational speed of the disk is 7200 rpm. It can transfer data at a rate of 100 mbps. The controller overhead takes 15ms per read. For a sector size of 5 mb, **calculate** the time for reading a file of size 100 mb from the disk, if the disk starts from idle scenario. [2]

   (c) Write down the key difference between **Write Back** and **Write Through** policy with proper examples. [2]

   (d) Suppose a PC uses three caches. The properties of the caches and the main memory are given on the following Table 3. **Calculate** the **Performance Gain** of using **all** L1, L2 and L3 cache with main memory over using **only** the L1 cache memory with main memory. [4]

	L1 Cache	**L2 Cache**	**L3 Cache**	**Main Memory**
Access Time	2 Cycles	10 Cycles	160 Cycles	400 Cycles
Miss Ratio	55%	20%	5%	-

Table 3: Cache Performance