United International University
Department of Computer Science and Engineering

CSE-3313: Computer Architecture

Midterm Examination: Summer 2023

Total Marks: 30 Time: 1 hour and 45 minutes

Any examinee found adopting unfair means will be expelled from the trimester / program as per UIU disciplinary rules.

Answer all questions. Numbers to the right of the questions denote their marks.

1. You are the most renowned computer architect in the world. Your friend asks you to find the answer to the following question for the given scenario: Consider computer A with a CPU speed of 2 GHz. The program P which has number of instruction(IC) and Cycle Per Instruction(CPI) as shown in Table 1.

Instruction	IC	CPI
addi	3	2
add	2	1
beq	1	4
bne	0	8
slt	1	4
sll	1	4
and	1	4
j	1	8

Table 1: Program P's number of instructions(IC) and CPI in Computer A architecture

(a) Find the execution time of program P in Computer A. [4]

(b) Computer B with a CPU speed of 10 GHz has the execution time of the program P, 2 times faster than computer A and same instruction set architecture(ISA), calculate the average CPI of computer B. [3]

(c) As we get the total execution time of the given program for Computer A from question (a). The Arithmetic unit takes 62.5%, the logical unit takes 25%, and the branch operation takes 12.5% time of total execution. Find the improvement factor of the given program if we replace the arithmetic unit with a better Arithmetic unit, which improves total completion time by 2x. [3]

2. Consider the following C function. Assume necessary registers.

```
1   2000:int find_series_sum(int n,int x){
2       int res=0;
3       if(n==0){
4           res = x;
5       }
6       else{
7           for(int i=1;i<=n;i++){
8               res = res + (x*5);
9           }
10      }
11      return res;
12  }
13  int main(){
14      1000: int s=10,x=2,r=0;
15      r = find_serise_sum(s,x);
16  }
```

(a) Convert the code to the corresponding MIPS assembly instructions. [8]

(b) Convert the first 8 lines of your assembly instructions to the corresponding machine code. No need to convert it to binary. [4]

(c) Assume we have a new instruction type available in MIPS architecture which is S-type. Only load/store instructions can be executed using the S-type MIPS field. The structure of the S-type is given in Table 2. Please find the maximum number of indexes that can be possible in an array. Explain your answer. [3]

op	rs	rt	C/A
8 bits	8 bits	8 bits	40 bits

Table 2: S-type format for MIPS

3. (a) Assuming 4-bit architecture and using the division algorithm show each step of the division of 13 by 5. [4]

   (b) If we want to multiply 32 by 32 using the multiplication algorithm then what will be the minimum size of the product register? [1]

Instruction	Opcode	Function Code
add	0	32
sub	0	34
lw	35	-
sw	43	-
and	0	36
or	0	37
nor	0	39
andi	12	-
ori	13	-
sll	0	0
srl	0	2
beq	4	-
bne	5	-
slt	0	42
j	2	-
jr	0	8
jal	3	-
addi	8	-

Table 3: MIPS Machine Codes

Name	Register Number
$zero	0
$at	1
$v0-$v1	2-3
$a0-$a3	4-7
$t0-$t7	8-15
$s0-$s7	16-23
$t8-$t9	24-25
$k0-$k1	26-27
$gp	28
$sp	29
$fp	30
$ra	31

Table 4: MIPS Registers