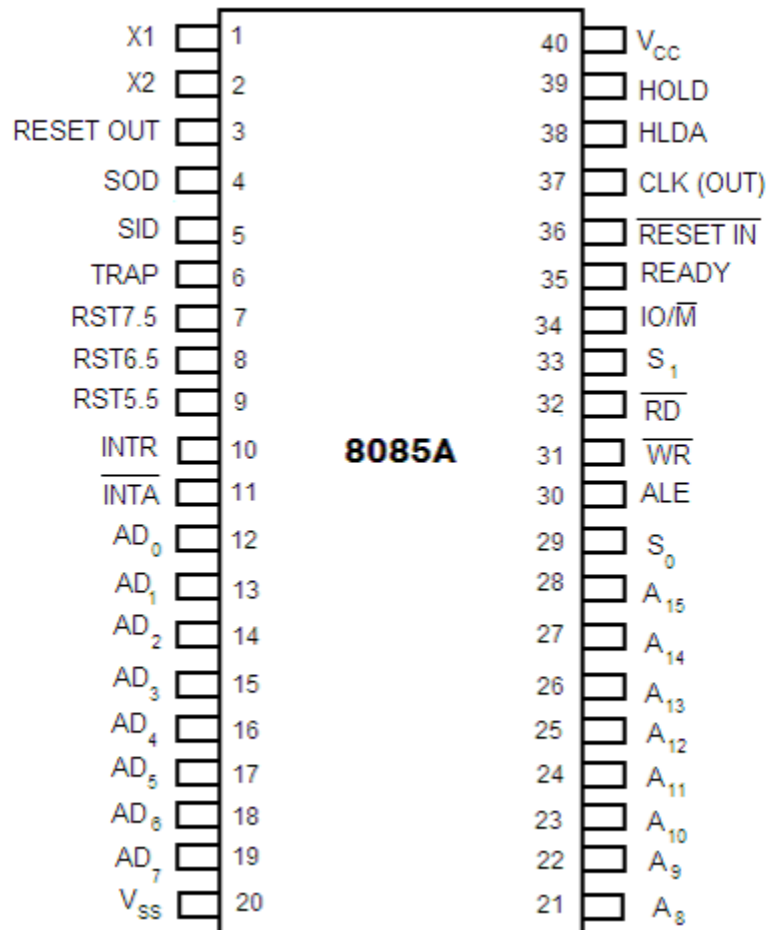


## 8085 Pin Configuration



The descriptions of various pins are as follows:

### Address Bus and Data Bus

#### A<sub>8</sub> -A<sub>15</sub> (Output):

These are **address bus** and are used for the most significant bits of the memory address or 8-bits of I/O address.

#### AD<sub>0</sub> -AD<sub>7</sub> (Input/output):

These are time multiplexed **address/data bus** i.e. they serve dual purpose. They are used for the least significant 8 bits of the memory address or I/O address during the first cycle. Again they are used for data during 2nd and 3rd clock cycles.

## Control and Status Signals

### ALE (Output):

ALE stands for **Address Latch Enable** signal. ALE goes high during first clock cycle of a machine cycle and enables the lower 8-bits of the address to be latched either into the memory or external latch.

### IO/M (Output):

It is a **status signal** which distinguishes whether the address is for memory or I/O device.

### S<sub>0</sub>, S<sub>1</sub> (Output):

These are **status signals** sent by the microprocessors to distinguish the various types of operation given in table below:

### Status codes for Intel 8085

S <sub>1</sub>	S <sub>0</sub>	Operations
0	0	HALT
0	1	WRITE
1	0	READ
1	1	FETCH

### RD (Output):

RD is a signal to control READ operation. When it goes low, the selected I/O device or memory is read.

### WR (Output):

WR is a signal to control WRITE operation. When it goes low, the data bus' data is written into the selected memory or I/O location.

### READY (Input):

It is used by the microprocessor to sense whether a peripheral is ready to transfer a data or not. If READY is high, the peripheral is ready. If it is low the micro processor waits till it goes high.

## Interrupts and Externally Initiated Signals

**HOLD (INPUT):** HOLD indicates that another device is requesting for the use of the address and data bus.

**HLDA (OUTPUT):** HLDA is a signal for HOLD acknowledgement which indicates that the HOLD request has been received. After the removal of this request the HLDA goes low.

**INTR (Input):** INTR is an Interrupt Request Signal. Among interrupts it has the lowest priority. The INTR is enabled or disabled by software.

**INTA (Output):** INTA is an interrupt acknowledgement sent by the microprocessor after INTR is received.

**RST 5.5, 6.5, 7.5 and TRAP (Inputs):** These all are interrupts. When any interrupt is recognized the next instruction is executed from a fixed location in the memory as given below:

Line	Location from which next instruction is picked up
TRAP	0024
RST 5.5	002C
RST 6.5	0034
RST 7.5	003C

## Reset Signals

### RESET IN (Input):

It resets the program counter (PC) to 0. It also resets interrupt enable and HLDA flip-flops. The CPU is held in reset condition till RESET is not applied.

### RESET OUT (Output):

RESET OUT indicates that the CPU is being reset.

## Clock Signals

**X1, X2 (Input):** X1 and X2 are terminals to be connected to an external crystal oscillator which drives an internal circuitry of the microprocessor. It is used to produce a suitable clock for the operation of microprocessor.

**CLK (Output):** CLK is a clock output for user, which can be used for other digital ICs. Its frequency is same at which processor operates.

## **Serial I/O Signals**

**SID (Input):** SID is data line for serial input. The data on this line is loaded into the seventh bit of the accumulator when RIM instruction is executed.

**SOD (Output):** SOD is a data line for serial output. The seventh bit of the accumulator is output on SOD line when SIM instruction is executed.

## **Power Supply**

Vcc : +5 V supply

Vss : ground reference