3.8 DIRECT MEMORY ACCESS (DMA) CONTROLLER (8257):

It is designed by Intel to transfer data at the fastest rate. It allows the device to transfer the data directly to/from memory without any interference of the CPU. Using a DMA controller, the device requests the CPU to hold its data, address and control bus, so the device is free to transfer data directly to/from the memory. The DMA data transfer is initiated only after receiving HLDA signal from the CPU.

The sequences of operations performed by a DMA are

- Initially, when any device has to send data to the memory, the device has to send DMA request (DRQ) to DMA controller.
- The DMA controller sends Hold request (HRQ) to the CPU and waits for the CPU to assert the HLDA signal.
- Then the microprocessor tri-states all the data bus, address bus, and control bus. The CPU will relinquish the bus and acknowledges the HOLD request through HLDA signal.
- Now the CPU is in HOLD state and the DMA controller has to manage the operations over buses between the memory interfaced with Microprocessor and I/O devices.

FEATURES OF 8257

- It has four channels that can be used over four I/O devices.
- Each channel has 16-bit address and 14-bit counter.
- Each channel can transfer data up to 64kb.
- Each channel can be programmed independently.
- Each channel can perform read transfer, write transfer and verify transfer operations.
- It operates in 2 modes, i.e., **Master mode** and **Slave mode**.

8257 PIN DESCRIPTION

The pin configuration of DMA Controller (8257) is shown in Figure 3.8.1 and the descriptions are as follows:
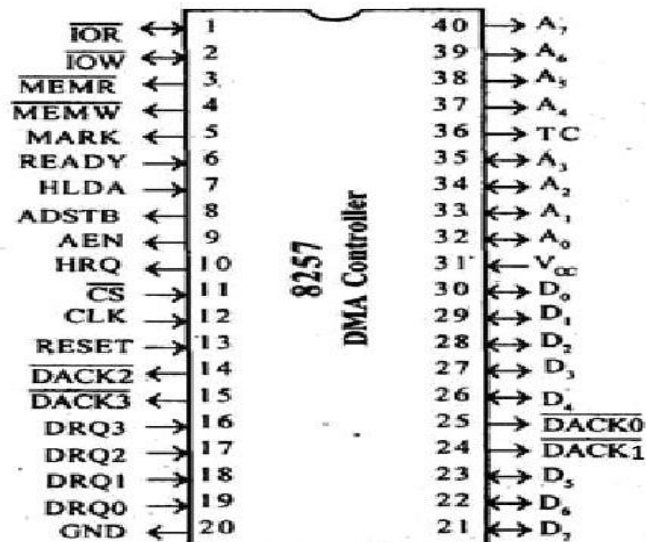

Figure 3.8.1 Pin Configuration of 8257

[Source: Advanced Microprocessors and Microcontrollers by A.K Ray & K.M.Bhurchandi]

DRQ0−DRQ3

    These are the four individual channel DMA request inputs, which are used by the peripheral devices for using DMA services. When the fixed priority mode is selected, then DRQ0 has the highest priority and DRQ3 has the lowest priority.

DACKo − DACK3

    These are the active-low DMA acknowledge lines, which updates the requesting peripheral about the status of their request by the CPU. These lines can also act as strobe lines for the requesting devices.

Do − D7

    These are bidirectional, data lines which are used to interface the system bus

with the internal data bus of DMA controller. In the Slave mode, it carries command words to 8257 and status word from 8257. In the master mode, these lines are used to send higher byte of the generated address to the latch. This address is further latched using ADSTB signal.

IOR

It is an active-low bidirectional tri-state input line, which is used by the CPU to read internal registers of 8257 in the Slave mode. In the master mode, it is used to read data from the peripheral devices during a memory write cycle.

IOW

It is an active low bi-direction tri-state line, which is used to load the contents of the data bus to the 8-bit mode register or upper/lower byte of a 16-bit DMA address register or terminal count register. In the master mode, it is used to load the data to the peripheral devices during DMA memory read cycle.

CLK

It is a clock frequency signal which is required for the internal operation of 8257.

RESET

This signal is used to RESET the DMA controller by disabling all the DMA channels.

Ao - A3

These are the four least significant address lines. In the slave mode, they act as an input, which selects one of the registers to be read or written. In the master mode, they are the four least significant memory address output lines generated by 8257.

CS

It is an active-low chip select line. In the Slave mode, it enables the read/write

operations to/from 8257. In the master mode, it disables the read/write operations to/from 8257.

READY

It is an active-high asynchronous input signal, which makes DMA ready by inserting wait states.

HRQ

This signal is used to receive the hold request signal from the output device. In the slave mode, it is connected with a DRQ input line 8257. In Master mode, it is connected with HOLD input of the CPU.

HLDA

It is the hold acknowledgement signal which indicates the DMA controller that the bus has been granted to the requesting peripheral by the CPU when it is set to 1.

MEMR

It is the low memory read signal, which is used to read the data from the addressed memory locations during DMA read cycles.

MEMW

It is the active-low three state signal which is used to write the data to the addressed memory location during DMA write operation.

ADSTB

It is a control output line used to split data and address line through Latches.

AEN

This signal is used to disable the address bus/data bus.

TC

It stands for 'Terminal Count', which indicates the present DMA cycle to the present peripheral devices.

MARK

The mark will be activated after each 128 cycles or integral multiples of it from the beginning. It indicates the current DMA cycle is the 128th cycle since the previous MARK output to the selected peripheral device.

Vcc

It is the power signal which is required for the operation of the circuit.

INTERNAL ARCHITECTURE OF 8257:

The functional Block Diagram of DMA controller(8257) is shown in Figure 3.8.2 and the description are as follows: It consists of five functional blocks:

a) Data bus buffer

b) Control logic

c) Read/write logic

d) Priority Resolver
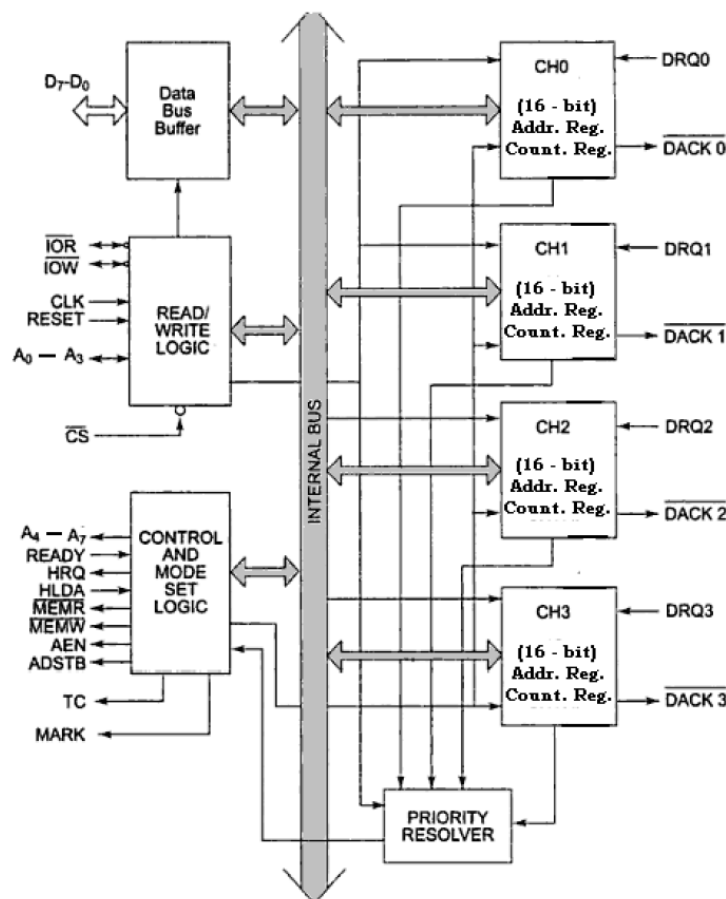
e) DMA channels

Figure 3.8.2 Functional Block Diagram of 8257

[Source: Advanced Microprocessors and Microcontrollers by A.K Ray & K.M.Bhurchandi]

Data Bus Buffer:

8-bit Tristate, bidirectional buffer interfaces the internal bus of 8257 with the external system bus under the control of various control signals.

Read/Write Logic:

In the slave mode, the read/write logic accepts the I/O Read or I/O Write signals, decodes the Ao-A3 lines and either writes the contents of the data bus to the addressed internal register or reads the selected register depending upon whether IOW or IOR signal is activated.In master mode, the read/write logic generates the IOR and IOW signals to control the dataflow to or from the selected peripheral.

Control Logic:

The control logic controls the sequences of operations and generates the required control signals like AEN, ADSTB, MEMR,MEMW, TC and MARK along with the address lines A4-A7, in master mode.

Priority Resolver:

The priority resolver resolves the priority of the four DMA channels depending upon whether normal priority or rotating priority is programmed.

Register Organisation of 8257:

The 8257 performs DMA operation over four independent DMA channels with the following Registers.

1. **DMA Address Register**

Each DMA channel has one DMA address register. The function of this register is to store the address of the starting memory location, which will be accessed by the DMA channel. The device that wants to transfer data over a DMA channel, will access the block of the memory with the starting address stored in the DMA Address

Register.

2. Terminal Count Registers

Each of the four DMA channels of 8257 has one terminal count register (TC). This 16-bit register is used for ascertaining that the data transfer through a DMA channel ceases or stops after the required number of DMA cycles.

After each DMA cycle, the terminal count register content will be decremented by one and finally it becomes zero after the required number of DMA cycles are over. The bits 14 and 15 of this register indicate the type of the DMA operation (transfer).

3. Mode Set Register

The mode set register is used for programming the 8257 as per the requirements of the system. The function of the mode set register is to enable the DMA channels individually and also to set the various modes of operation as shown in Figure 3.8.3.
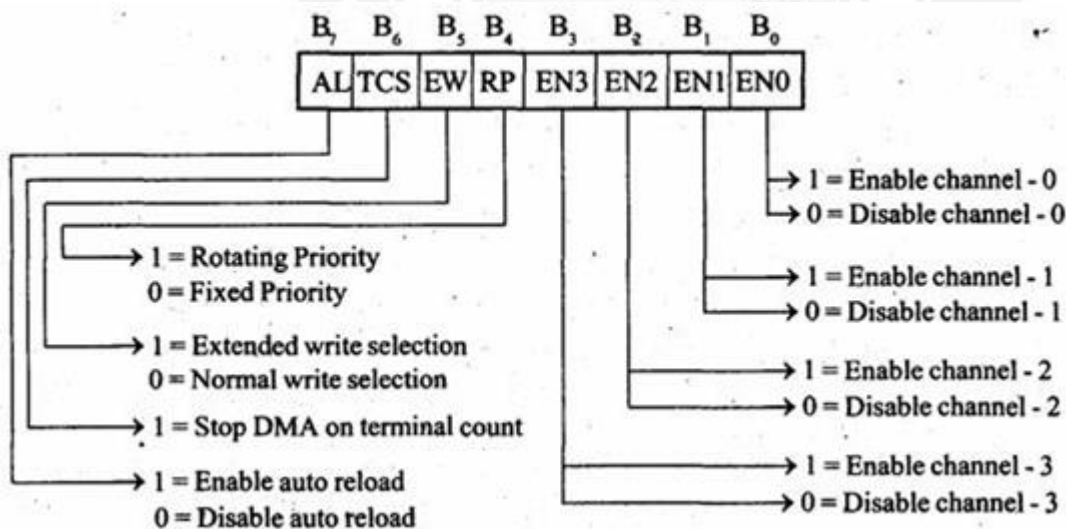

Figure 3.8.3 Mode Set Register

[Source: Advanced Microprocessors and Microcontrollers by A.K Ray & K.M.Bhurchandi]

The bits Do-D3 enable one of the four DMA channels of 8257. If the TC STOP bit is set, the selected channel is disabled after the terminal count condition is reached, and it further prevents any DMA cycle on the channel. If the TC STOP bit is programmed to be

zero, the channel is not disabled, even after the count reaches zero and further request are allowed on the same channel. The auto load bit, if set, enables channel 2 for the repeat block chaining operations, without immediate software intervention between the two successive blocks. The extended write bit, if set to '1', extends the duration of MEMW and IOW signals by activating them earlier, which is useful in interfacing the peripherals with different access times.

4. Status register

The lower order 4-bits of this register contain the terminal count status for the four individual channels. If any of these bits is set, it indicates that the specific channel has reached the terminal count condition. The update flag is not affected by the read operation. This flag can only be cleared by resetting 8257. The update flag is set every time, the channel 2 registers are loaded with contents of the channel 3 registers. It is cleared by the completion of the first DMA cycle of the new block. This register can only read.

DMA TRANSFER & OPERATIONS

The 8257 is able to accomplish three types of operations such as

1. DMA operation
2. Write Operation
3. Read Operation

Operational sequence of 8257 is as follows

o The 8257 request any one of the 8257 DRQ inputs to transfer single byte.

o In response to the request, the 8257 sends HRQ signal to CPU at its HLD input and waits for acknowledgement at the HLDA input.

o If the DMA controller receives the HLDA signal it indicates that the bus is available for the transfer.

o The DMA controller generate the read and write commands to transfer the

byte from/to the I/O Device.

o The DACK line of the used channel is pulled down by the DMA controller to I/O device that requested for DMA transfers.

o The HRQ line is lowered by the DMA controller to indicate the CPU that it may regain the control of the bus.

o The DRQ must be high until acknowledged.

o In each s4 state ,the DRQ lines are sampled and highest priority request is recognized during next transfer. The HRQ line is maintained active till all the DRQ line go low.