**A**

**Mini Project Report**

**On**

**ALU USING DSCH2**

**Submitted in partial fulfilment of the**

**Requirements for the award of the Degree of**

**Bachelor of Technology**

**in**

**Electronics & Communication Engineering**

**VLSI (17EC3301)**

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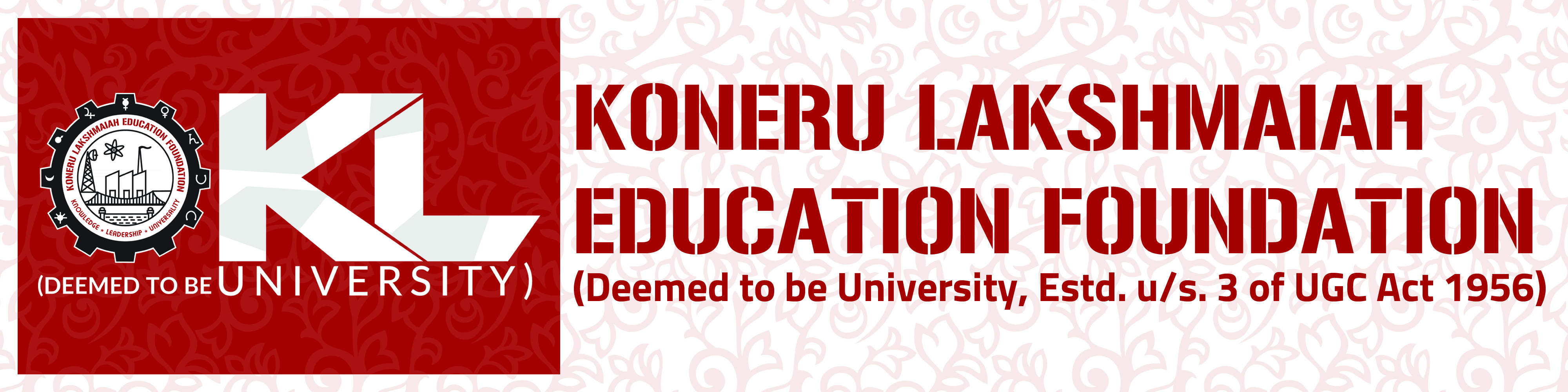
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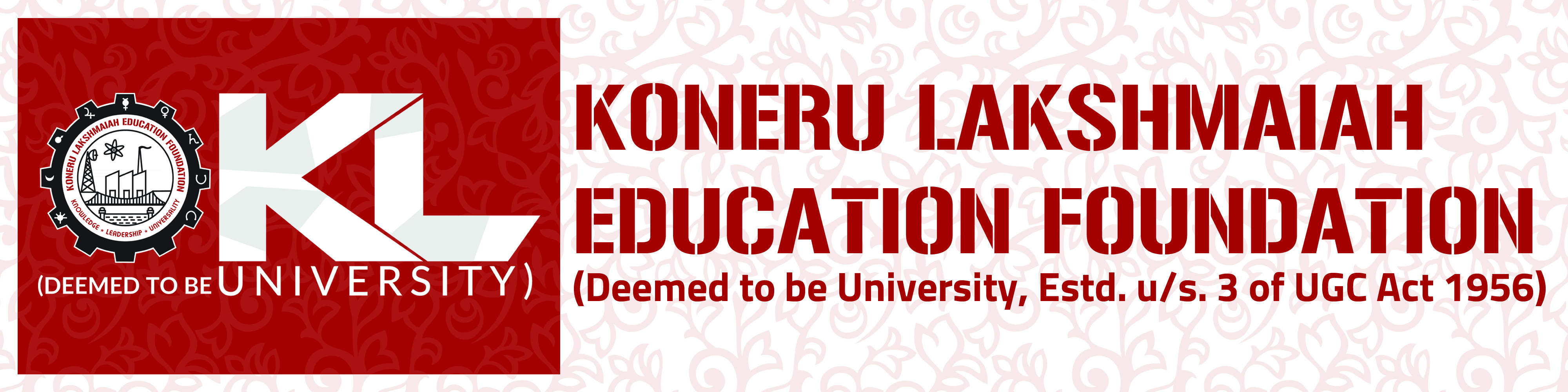
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**CERTIFICATE**

**This is to certify that this project based lab report entitled “ALU USING DSCH2” is a Bonafede work done by M.VINAY KUMAR (Id. No.170040555),SK. MUSHTAQ HUSSAIN (170040582),M.AVINASH(170040538) in partial fulfilment of the requirement for the award of degree in Bachelor of Technology in Electronics and Communication Engineering during the academic year 2019-2020. We also declare that this project based lab report is of our own effort and it has not been submitted to any other university for the award of any degree.**

Project Supervisor  Head of Department

**ACKNOWLEDGMENT**

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ABSTRACT

An arithmetic logic unit (ALU) is a combinational digital electronic circuit that performs arithmetic and bitwise operations on integer binary numbers. This is in contrast to a floating-point unit (FPU), which operates on floating point numbers. An ALU is a fundamental building block of many types of computing circuits, including the central processing unit (CPU) of computers, FPUs, and graphics processing units (GPUs). A single CPU, FPU or GPU may contain multiple ALUs.The inputs to an ALU are the data to be operated on, called operands, and a code indicating the operation to be performed; the ALU's output is the result of the performed operation. In many designs, the ALU also has status inputs or outputs, or both, which convey information about a previous operation or the current operation, respectively, between the ALU and external status registers.

CHAPTER 1

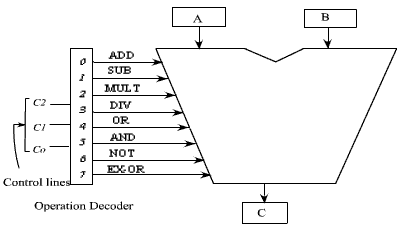
INTRODUCTION:

ALU is getting smaller and more complex nowadays to enable the development of a more powerful but smaller computer. However there are a few limiting factors that slow down the development of smaller and more complex IC chip and they are IC fabrication technology, designer productivity and design cost. The increasing demand for high speed very large scale integration (VLSI) can be addressed at different design levels, such as the architectural, circuit, layout, and the process technology level. At the circuit design level, considerable potential for speed enhancement exists by means of proper choice of a logic style for implementing combinational circuits. This is because all the important parameters governing speed switching capacitance, transition activity, and short-circuit currents are strongly influenced by the chosen logic style. Depending on the application, the kind of circuit to be implemented, and the design technique used, different performance aspects become important. In the past, the parameters like low power dissipation, small area and low cost were the major areas of concern, whereas speed considerations are now gaining the attention of the scientific community associated with VLSI design.

CHAPTER 2

BLOCK DIAGRAM

**BLOCK DIAGRAM**:



**BLOCK DIAGRAM DESCRIPTION:**

In CMOS technology, Power dissipation is the most critical parameter for portability & mobility and it is classified into dynamic and static power dissipation. Dynamic power dissipation occurs when the circuit is operational, while static power dissipation becomes an issue when the circuit is inactive or is in a power-down mode. There are three major sources of power dissipation in digital CMOS circuits, which are summarized as the first term represents the switching component of power, where C1 is the load capacitance, Fclk is the clock frequency and **α** is the probability that a power consuming transition occurs (the activity factor). The second term is due to the direct-path short circuit current, ISC, which arises when both the NMOS and PMOS transistors are simultaneously active, conducting current directly from supply to ground. Finally, leakage current, Ileakage, which can arise from substrate injection and sub-threshold effects, is primarily determined by fabrication technology considerations. The switching power in CMOS digital integrated circuits is a strong function of the power supply voltage. Therefore, reduction of Vdd emerges as a very effective means of limiting the power consumption. However, the saving in power consumption comes at a significant cost in terms increased circuit delay. Since the exact analysis of propagation delay .

**MAJOR PARTS OF THE PROJECT**

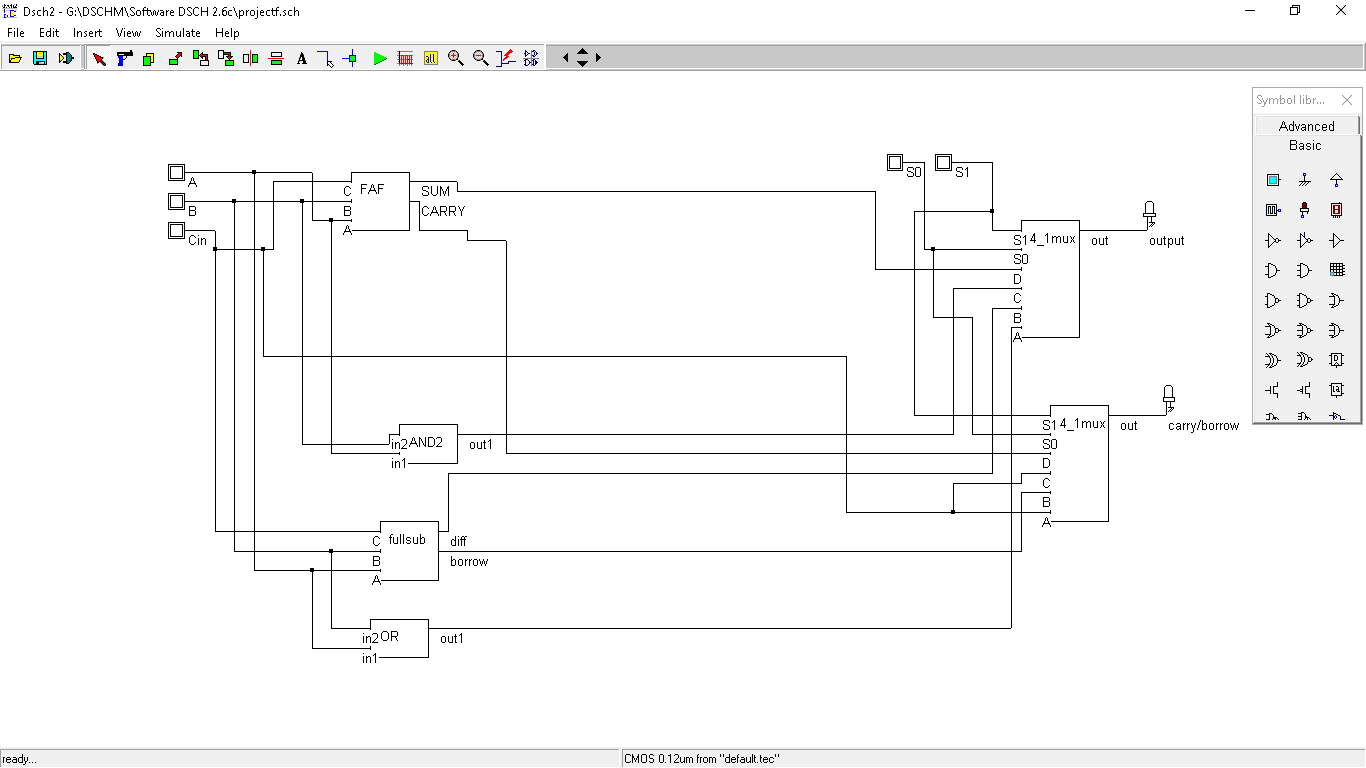
**Multiplexers:** These blocks are used to select the appropriate inputs for the arithmetic and logic blocks. Usually more than two buses arrive at the inputs of the ALU. Sometimes these multiplexers are used to perform some simple logic operations. The 2:1 MUX can be programmed to invert one of the operands (this can be used to execute a subtraction using just an adder).

**Arithmetic block:** This block is used to perform arithmetic operations such as addition, subtraction and comparison. The core of the arithmetic block is an adder. In the architecture presented in Figure 4.1, the adder uses carry look-ahead and sum-select techniques.

**Logic block:** This block is used to perform simple bitwise logic operations such as AND (masking), OR and XOR, XNOR, NAND, NOT and etc.

CHAPTER 3

CIRCUIT DIAGRAM:



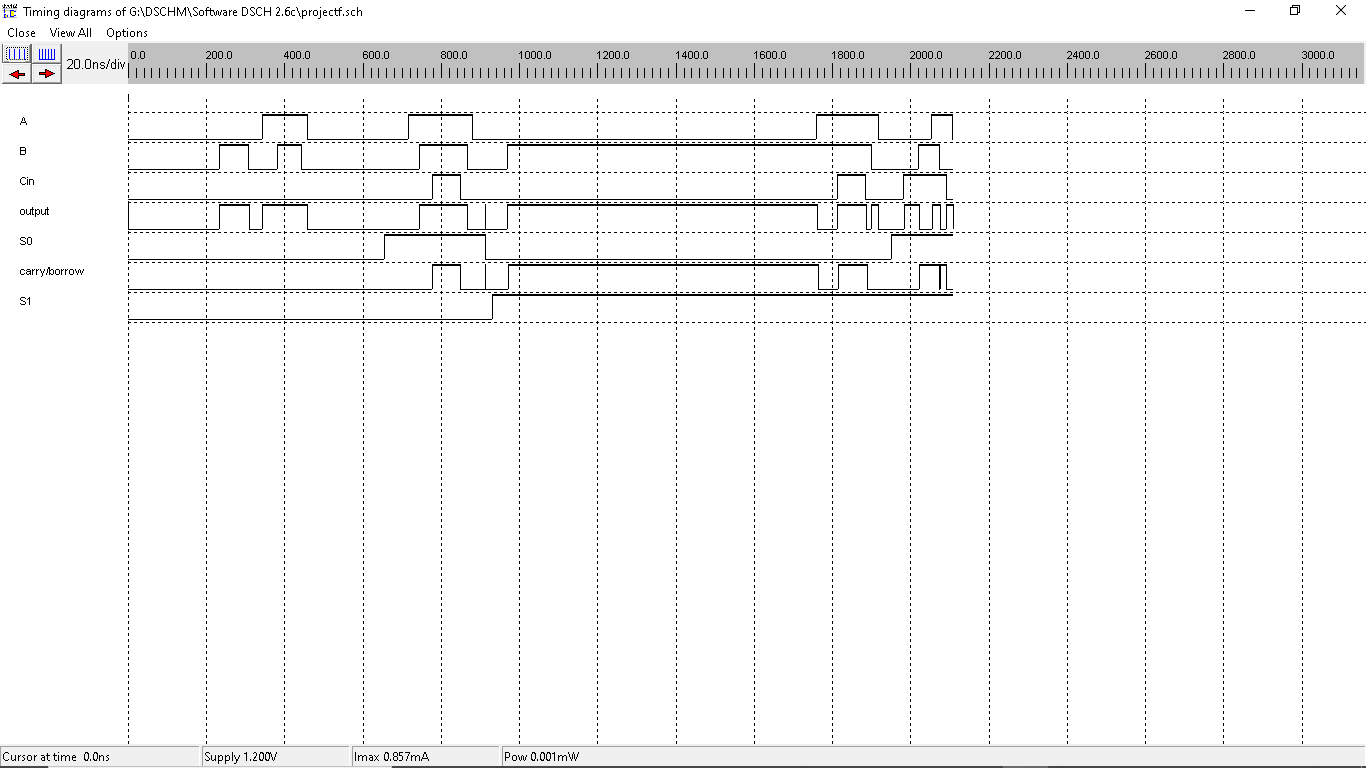
**Circuit Design:**

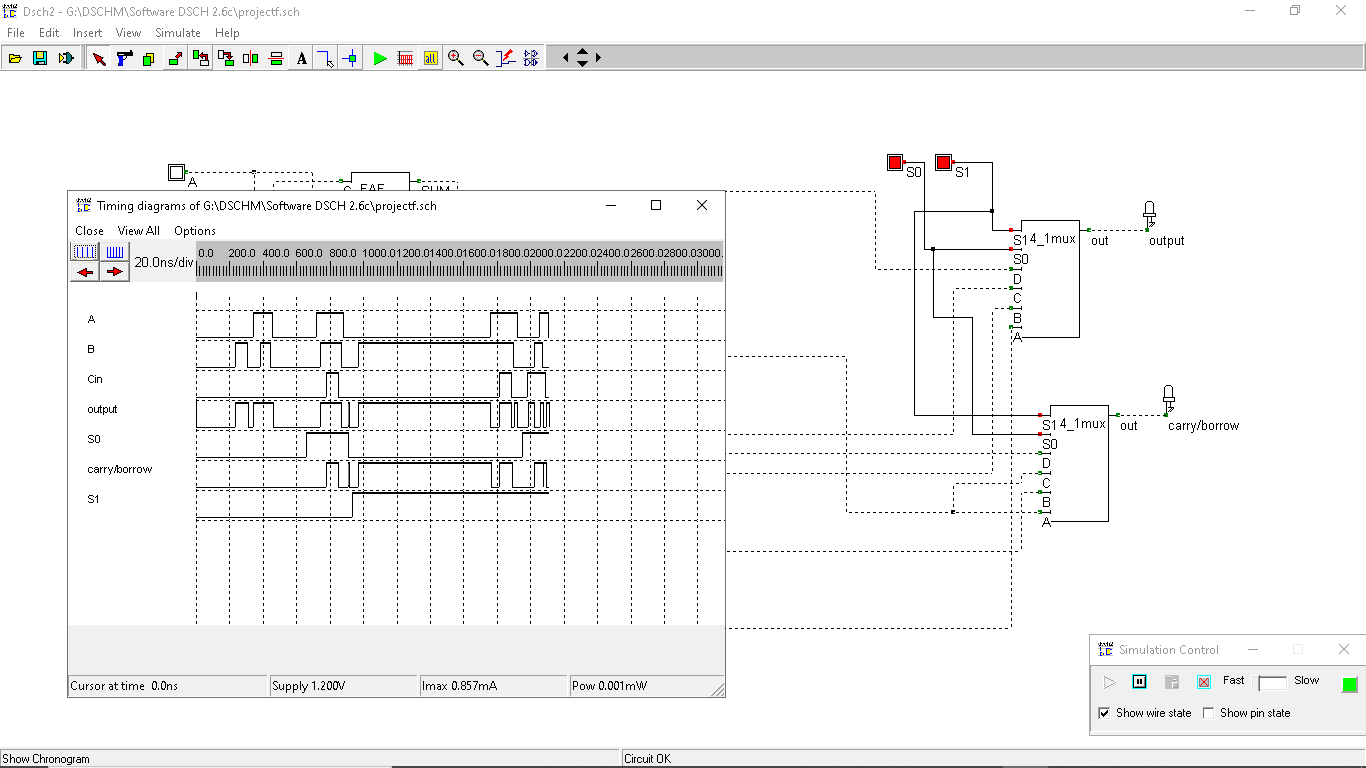
A 4-bit high-speed parallel Arithmetic Logic Unit (ALU). Controlled by the four Function Select inputs (S0–S3) and the Mode Control input (M), it can perform all the 16 possible logic operations or 16 different arithmetic operations on active-HIGH or active-LOW operands. The Function Table lists these operations. When the Mode Control input (M) is HIGH, all internal carries are inhibited and the device performs logic operations on the individual bits as listed. When the Mode Control input is LOW, the carries are enabled and the device performs arithmetic operations on the two 4-bit words. The device incorporates full internal carry lookahead and provides for either ripple carry between devices using the Cn+4 output, or for carry look-ahead between packages using the signals P (Carry Propagate) and G (Carry Generate). In the Add mode, P indicates that F is 15 or more, while G indicates that F is 16 or more. In the Subtract mode, P indicates that F is zeroorless, while G indicates that F is less than zero. P and G are not affected by carry in. When speed requirements are not stringent, it can be used in a simple Ripple Carry mode by connecting the Carry output (Cn+4) signal to the Carry input (Cn) of the next unit. For high-speed operation the device is used in conjunction with a carry lookahead circuit. One carry lookahead package is required for each group of four F181 devices. Carry lookahead can be provided at various levels and offers high-speed capability over extremely long word lengths

TRUTH TABLE

|  |  |  |
| --- | --- | --- |
| S1 | S0 | OPERATION |
| 0 | 0 | OR |
| 0 | 1 | SUBTRACTOR |
| 1 | 0 | AND |
| 1 | 1 | ADDER |

OUTPUT WAVE FORMS:





CONCLUSION:

To stay competitive in today’s market, engineers must take a design from engineering through manufacturing with shorter design cycles and faster time to market. To be successful, we need a set of powerful, intuitive, and integrated tools that work seamlessly across the entire design flow. We have studied well about arithmetic & logic unit. Here we have implemented 4-bit arithmetic logic unit successfully. The full integrated circuit is designed and simulated in standard 350 nm CMOS technology. Here the RTL coding is done first using a Verilog HDL and simulation is done by using Model Sim 6.2. Schematic layout simulation as well as the schematic versus layout comparison is done by using Mentor Graphics’ EDA Tools are used for. The experimental waveforms, power measurements have also been presented.

**The power consumption of ALU with** CMOS technology is about 120mW. There is power reduction 34.34% in comparison with Schottky TTL.

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