# Design of Noise and Process Variation Tolerant, Low-Power, High-Speed, and Low-Energy Full Adders in CNFET Technology

A Term paper Based Report

Submitted in partial fulfilment of the requirements for the award of degree

of Bachelor of Technology

in

ELECTRONICS AND COMMUNICATION ENGINEERING

by

Sk.Mushtaq Hussain 170040582
Y. Sundeep 170040970

Under the supervision of

**Dr. KAKARLA HARI KISHORE PROFESSOR**
**Dr. D SREE PHANI KISHORE PROFESSOR**


**DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING**

**KONERU LAKSHMAIAH EDUCATIONAL FOUNDATION**
Green Fields,Vaddeswaram,Guntur(Dist)-522502
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The Term Paper Report entitled "**Design of Noise and Process Variation Tolerant, Low-Power, High-Speed, and Low-Energy Full Adders in CNFET Technology**" is a record of bonafide work of Sk. Mushtaq Hussain-170040582 and Y. Sundeep 170040970 submitted in partial fulfillment for the award of B.Tech in **ELECTRONICS AND COMMUNICATION** in K L University. The results embodied in this report have not been copied from any other departments/University/Institute.

**Signature of Student**

**Sk. Mushtaq Hussian**
**170040582**

**Signature of Student**

**Y. Sundeep**
**170040970**

# CERTIFICATE

This is to certify that the Term Paper Report entitled "**Design of Noise and Process Variation Tolerant, Low-Power, High-Speed, and Low-Energy Full Adders in CNFET Technology**" is being submitted by Sk. Mushtaq Hussain-170040582 and Y. Sundeep 170040970 submitted in partial fulfillment for the award of B.Tech in **ELECTRONICS AND COMMUNICATION** to K L University is a record of bonafide work carried out under efficient guidance and supervision. The results embodied in this report have not been copied from any other departments/University/Institute.

**Signature of the Supervisor**
DR. HARI KISHORE
PROFESSOR

**Signature of the HOD**
Dr. Suman Maloji
HOD

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BY
SK. MUSHTAQ HUSSAIN (170040582)
Y. SUNDEEP (170040970)

# ABSTRACT

In this paper, a number of novel 1-bit full adder cells using carbon nanotube field-effect transistor devices are presented.

First of all, some two-input XOR/XNOR circuits are proposed, and then, they are employed to form 1-bit full adders.

Totally, five full adders with driving power and one without driving power are proposed in this paper, each of which has its own merits.

In this project main focus is on reducing the power consumption of the circuit and increasing its performance.

Different full adder circuits are being compared based on their power delay and energy delay products.

Simulations with regard to supply power scaling and different load conditions confirm the superiority of the proposed cells compared with the previously reported ones in terms of power, delay, power-delay product (PDP), and Energy delay product (EDP).

Also embedding the proposed full adders in the large circuits, such as ripple carry adder (RCA), with a wide word length shows that they have better power, speed, and PDP with regard to their counterparts.

Furthermore, the susceptibility of the full adders against both input noise and process variations (diameter deviations of carbon nanotubes) is studied.

# INDEX

# INTRODUCTION

Explosive usage of battery-based portable electronic systems, such as laptops, notebooks, tablets, personal communication systems, personal digital assistants, and so many others, demands high performance circuits with respect to power consumption and operation speed to save energy and process the input data with high performance.

Power consumption plays a pervasive role in VLSI systems. More power dissipation results in more heat that is taken out of a system.

Thus, it not only decreases the battery life but also needs a stronger fan to cool the system.

Therefore, power consumption directly affects on cost, weight, size, and battery life of a system.

On the other hand, operation speed is a vital task in today's high-speed electronic applications. Power consumption is a limiting factor to increase clock rate and density of circuits.

There is a quantitative metric that compromises between power dissipation and speed of circuit. In fact, a power-delay product (PDP) is widely used as a figure of merit to evaluate the overall performance of a designed circuit

There are many VLSI applications, such as digital signal processing, image and video processing, microprocessors, and microcontrollers that extensively use arithmetic operations.

Among various arithmetic operations, addition, subtraction, multiplication, and multiply and accumulate are mostly used. All aforementioned operations could be realized using the addition function.

Therefore, a 1-bit full adder cell still plays an important role in determining the performance metrics of an entire system.

Furthermore, a 1-bit full adder cell is used in arithmetic logic unit of a processor, in floating-point unit, and address generation for cache or memory access.

Until now many full adder cells with different logic styles are reported in the literature using the metal–oxide–semiconductor FET (MOSFET) technology, each having its own merits and demerits.

In 1965, Moore [12] predicted that the number of transistors per square inch of an integrated circuit doubles nearly every 18 months.

This law implies to scale silicon bulk transistors (i.e., MOSFETs) down continuously. Historically, the dimensions of transistors have been scaled down, such that nowadays, they have entered to a nanometer region.

There are some issues that limit the shrinking of MOSFETs further. For instance, nanometer silicon bulk transistors experience new problems, such as short channel effects, drain-induced barrier lowering (DIBL), decreased gate controllability, hot electron effect, and so on [13].

As a result, there has been enormous motive to develop new devices, such as carbon nanotube field effect transistor (CNFET), single electron transistor, FinFET, and so forth.

It is worthwhile to note that CNFET is one of the promising successors to the conventional MOSFETs due to its unique electrical characteristics, such as ballistic transport and low OFF-current, which enables high-speed and low-power circuit designs [14]–[16].

Carbon nanotubes (CNTs) are sheets of one-atom-thick layer of graphite, called graphene, which are rolled into tubes. They are classified into two groups called single-wall CNT (SWCNT) and multiwall CNT (MWCNT).

SWCNTs consist of one cylinder, whereas MWCNTs consist of more than one cylinder. An SWCNT can behave as semiconductor or conductor with respect to its chirality vector.

Chirality vector determines the angle of the arrangement of carbon atoms along the CNT, shown by integer pair (n1, n2) [16].

# THEROTICAL ANALYSIS

In this paper, we use MOSFET-like CNFETs to develop novel 1-bit full adder cells. First, some novel two-input XOR/XNOR circuits are presented, and their performances are compared with other classical and state-of-the-art circuits.

Then, using them, different novel structures are presented to construct 1-bit full adder cells, each having its own figure of merit. Comprehensive computer simulations are conducted to scrutinize the performance of the proposed full adders in various situations.

Simulation results confirm the superiority of the proposed cells against other designs. To have fair comparisons, all MOSFET oriented full adder cells have simulated in the CNFET technology.

We provide a detailed performance analysis for full adders with different logic styles. There are antithesis performance results for CNFET technology compared with MOSFET technology due to dissimilarities between them.

For instance, we consider two full adders namely FA1 and FA2. Simulations provide different results for MOSFET technology and CNFET technology.

In MOSFET technology, FA1 has better performance, while in CNFET technology, FA2 has better performance. Therefore, we aim at revise a set of full adders with different logic styles in CNFET technology.

# 1.ADDER DESIGN

Our proposed full adder cell is based on the following logic equations. In fact, we first need to generate two-input XOR/XNOR circuits, and then using a 2-to-1 multiplexer produce the Sum and Cout outputs. Fig. 1 shows the block diagram of the proposed 1-bit full adder cell, based on

Sum = $(B \oplus C)\cdot A + (B \oplus C)\cdot \overline{A}$ ——————————— (3)

Cout = $(B \oplus C)\cdot B + (B \oplus C)\cdot A$. (4)

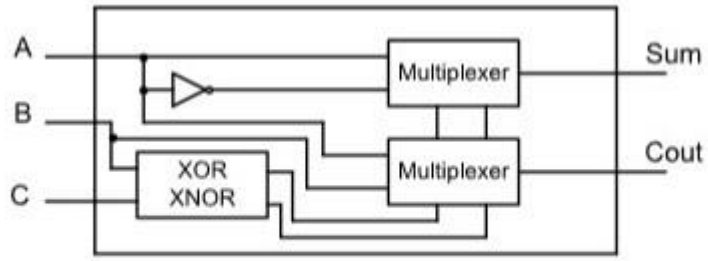



Fig. 1. Block diagram of the proposed full adder cell without driving capability.

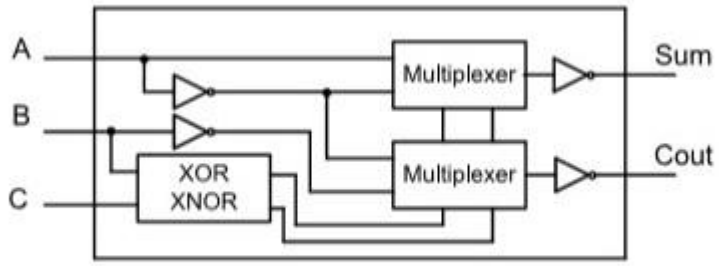



Fig. 2. Block diagram of the proposed full adder cell with driving capability.

Using multiplexers at the output nodes results in a low driving power for the design shown in Fig. 1. To enhance the driving capability, first, we complement (3) and (4) to obtain logic relations (5) and (6), respectively. Then, using NOT gates at the output nodes, the desired signals are produced

Sum = $(B \oplus C)\cdot \overline{A}$ ——————————— $+(B \oplus C)\cdot A$ (5)

Cout = $(B \oplus C)\cdot B$ ——————————— $+(B \oplus C)\cdot \overline{A}$ ——————————— . (6)

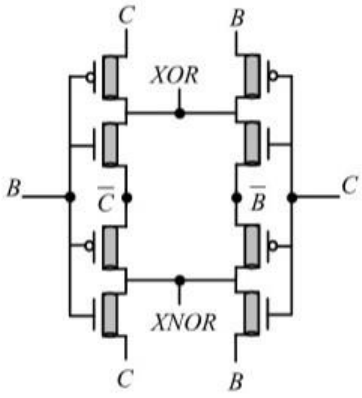



Fig. 3. Proposed structure of the XOR/XNOR circuit (X-Design1).

The block diagram of the proposed full adder cell, which is based on relations (5) and (6), is shown in Fig. 2. The presence of inverters at the output nodes decouples inputs and outputs and provides a sufficient driving power. Therefore, this structure can be efficiently used in any circuit configuration.

As the method proposed in [9], considering Figs. 1 and 2, we separately present and analyze corresponding circuits for XOR/XNOR and multiplexer modules to form the novel full adder cell. In Section III-A, we present the transistor level implementation of the novel XOR/XNOR functions. In Section III-B, the schematic of a 2-to-1 multiplexer is presented. Finally, in Section III-C, the transistor level implementations of the proposed full adder cells are presented.

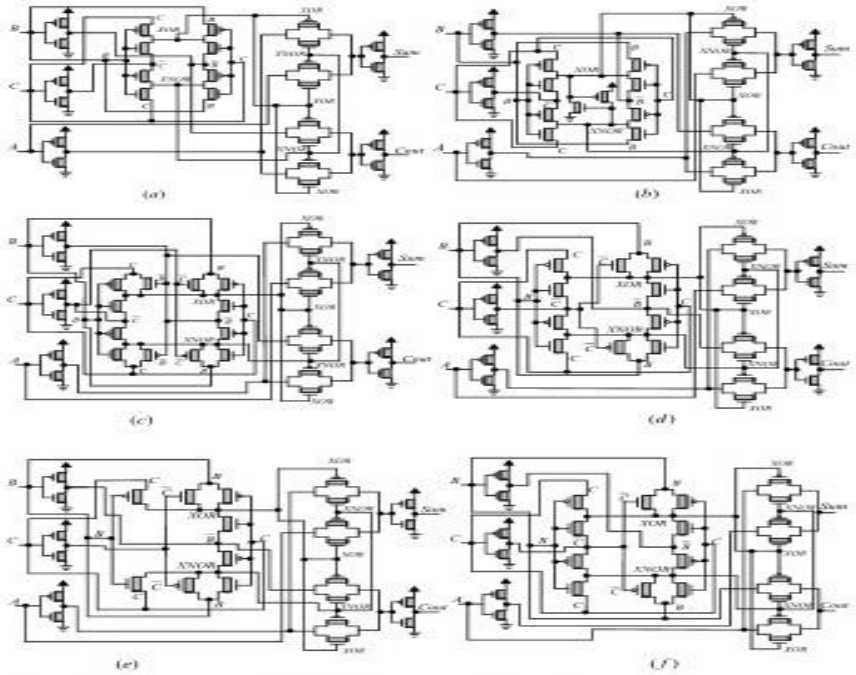


Fig. 6. Proposed hybrid-CNFET full adders. (a) NEW-PT-FA. (b) NEW-FL-FA. (c) NEW-DD-FA. (d) NEW-SD-FA. (e) NEW-RSD-FA. (f) NEW-ND-FA.

The last design for the XOR/XNOR circuit, called X-Design5, is shown in Fig. 4(d). By removing two transistors from the structure of the X-Design4, the X-Design5 is achieved. The X-Design5 consists of 12 transistors, two transistors less than the transistor count of X-Design4. The presence of TGs in both XOR and XNOR circuits guarantees the full-swing voltages at the output nodes. It is expected that X-Design5 has lower power consumption compared with the X-Design4 due to the smaller number of transistors.

## 1.1 PARAMETRIC STUDY AND ANALYSIS

The schematic of the Ours1 full adder cell is reported in [10]. The Ours1 cell uses double pass-transistor logic (DPL) to realize a full adder cell. It contains 28 transistors and is placed among high-gate-count full adders.

Although the Ours1 has the large number of transistors, due to using DPL logic style, its power dissipation is very low.

Furthermore, its maximum propagation path consists of three transistors, which cause high-speed operation.

To produce output signals of Sum and Cout, it employs TGs at the last stage of the circuit. TGs result in full voltage swing outputs but they have not driving capability.

In conclusion, the Ours1 will perform well against small fan-outs. Its performance will be drastically decreased when it is used in the cascaded mode of operation because of lacking driving power.

The structure of hybrid CMOS logic with a TG logic (HCTG) full adder cell is reported in [11]. In [11], a modified design for an XNOR circuit is presented.

This XNOR circuit consists of six transistors and offers low-power consumption and high-speed operation. Level restoring transistors MP3 and MN3 guarantee full voltage swing XNOR signal.

Then, using an inverter gate, the XOR signal is generated. To generate Cout and Sum outputs, TGL and CMOS logic style are employed, respectively.

The HCTG has 16 transistors, which result in the reduction of power consumption. One essential drawback of the HCTG is that it suffers driving power by coupling inputs to outputs.

Therefore, its performance will degrade in the presence of large fan-outs or when it is embedded in wide cascaded configuration without inserting buffers between cascaded stages. Table I summarizes the characteristics of these full adder cells. Among different cells, only CPL-TG is dual rail and the others are single rail. Driving capability does not exist when either inputs are coupled to the output signals or TGs are used at the output nodes. Considering Table I, only C-CMOS, Mirror, CPL-TG, HPSC, and NEW-HPSC have driving capability. A threshold-loss problem means that at least one output signal of Sum or Cout is not full voltage swing. Table I shows that all 10T cells have the threshold-voltage drop problem.

## 1.2 DESIGN

The design of a transmission gate full adder (TGA), which is formed using TGs, is reported in [1]. The TGA comprises 20 transistors, and its critical path has four transistors.

The same as the TFA, since the inputs of the TGA cell are coupled to the outputs, it suffers from lacking driving power.

Lacking driving capability drastically degrades the performance of the TGA, where it is employed in a cascaded structure or where there are large fan-outs. One solution to alleviate the performance degradation is to put buffers at the output nodes between consecutive cascaded stages.

However, this approach results in transistor count overhead and removes the advantage of small transistor count in large cascaded circuits.

The TGA cell performs better than the TFA due to employing TGs at the output nodes instead of pass transistors. In fact, its delay and power dissipation are less than that of TFA, especially in larger circuits.

The structure of a complementary pass-transistor logic TG (CPL-TG) is reported in [4]. The CPL-TG not only is dual rail but also provides driving capability at the expense of large transistor count. Then, it is advantageous in the cascaded circuits.

To generate the XOR/XNOR functions, it uses CPL. Thus, the input capacitance reduces because of small number of transistors. On the other hand, it uses TGs to drive the static inverter existence at the output nodes.

Then, the leakage power of inverters is removed due to full voltage swing signals are applied to drive them. When the CPL-TG is solely used, it contains 36 transistors; but when it is used in a cascaded structure, the transistor count will be decreased due to the elimination of static inverters to provide complementary signals.

The critical path of the CPL-TG as a standalone unit consists of four transistors, while in a cascaded configuration consists of three transistors. Therefore, the CPL-TG is expected to show good performance in larger structures.

The structure of static energy recovery full adder (SERF) is reported in. The SERF full adder contains only ten transistors (10T) in which three of them are along the critical path from the input to the output. To produce Sum signal, it employs two cascaded XNOR circuits.

It is worth to note that there is a threshold-loss problem for an XNOR circuit. In fact, the logic value high is equal to Vdd−Vtn (Vtn denotes the threshold voltage of the n-type transistor).

Therefore, both internal signals and output signals (i.e., Sum and Cout) are nonfull swing. As a result, the SERF design is not good at all for using in cascaded configuration.

Due to the presence of non full-voltage-swing signals of SERF, both the power dissipation and the delay are increased. The advantage of SERF is that it has the least number of transistors. The structure of a 13A full adder cell is reported in [6]. Like the SERF, 13A also uses 10T in its structure.

Both SERF and 13A cells use two cascaded two-input XNORs' to provide Sum output. The circuit for the first XNOR is the same in both SERF and 13A full adder cells. They use two different designs for an XNOR circuit at the second stage.

The SERF uses CMOS style to realize a two-input XNOR circuit, while the 13A uses a combination of CMOS (to realize a NOT gate) and pass-transistor logic (PTL) (to realize a 2-to-1 multiplexer) styles. It is apparent that the PTL-based XNOR circuit embedded in a 13A full adder has not enough driving power.

The presence of an inverter circuit in the structure of 13A will result in short-circuit power dissipation.

Therefore, the power consumption of 13A is expected to be more than the SERF. The structure of a complementary and level restoring carry logic (CLRCL) full adder cell is reported in .

The CLRCL is another 10T cell, which is based on PTL. Theoretical dc analysis demonstrates that the minimum power supply (Vdd) for the both SERF and 13A cells is equal to 2Vtn +| Vtp|(note that Vtn and Vtp stand for the threshold voltage of n- and p-type transistors, respectively).

This is because of connecting incomplete signals to the control select signal of PTL-based multiplexers. The CLRCL design eliminates this problem by applying full voltage swing signals to the select control of multiplexers.

The minimum Vdd that the CLRCL can function is equal to Vtn +|Vtp|. In conclusion, the delay of the CLRCL is less than that of SERF and 13A full adders. With regard to power consumption, SERF consumes the least power compared with 13A and CLRCL 10T full adders, since it does not use any inverter, and consequently, short-circuit power is removed.

On the other hand, the CLRCL design due to using more inverters consumes more power consumption compared with 13A and SERF 10T cells.

The structure of hybrid pass-transistor logic with static CMOS output drive full adder (HPSC) is reported in [8]. This design with 26 transistors is placed among high gate-count full adders. It exploits different logic styles, such as TG logic (TGL), PTL, and static CMOS to obtain the best performance.

It uses four transistors to generate two-input XOR/XNOR functions. Furthermore, to overcome the threshold-loss problem existence at the outputs of XOR/XNOR circuits, it uses feedback loop transistors and pass transistors to strengthen the outputs of the XOR and XNOR circuits.

The HPSC design has driving power due to employing inverters at the output nodes. Then, it functions properly in cascaded configurations. The maximum critical path of HPSC belongs to Cout with four transistors, which make a long propagation delay.

The structure of new hybrid pass-transistor logic with a static CMOS output drive full adder (NEW-HPSC) is reported in [9]. It consists of 24 transistors, and its maximum critical path contains four transistors.

Regardless of smaller transistor count of the NEW-HPSC compared with HPSC, its power consumption is higher than HPSC. This is due to it applies one inverter more than HPSC, which results in larger short-circuit current.

Furthermore, from the delay point of view, the delay of NEW-HPSC is expected to be higher than the HPSC. However, the critical path of both the NEW-HPSC and HPSC circuits is equal to four transistors. If we take a look at the XOR/XNOR circuits of both

cells, it is clear that HPSC benefits more strength outputs at the expense of two more transistors.

Employing feedback transistors along with pass transistors restores full-swing output signals of XOR/XNOR circuits with the less delay compared with NEW-HPSC. The NEW-HPSC employs only cross coupled p CNFETs to restore outputs of XOR/XNOR circuits.

Note that Goel et al. [9] reported that employing n MOS transistors at the first stage of an XOR/XNOR circuit leads to an increase in speed compared with that of existing in HPSC. They state that n MOS transistors have higher mobility than p MOS transistors. Thus, the speed of XOR/XNOR circuit existence in an HPSC full adder is less than that of existence in the NEW-HPSC, because the p MOS transistors have low mobility than n MOS transistors.

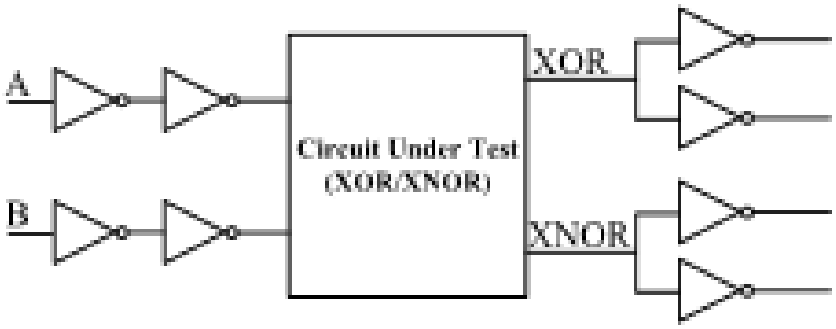
It is worth to notice that this statement is false in CNFET technology. In fact, in CNFET technology, both the p- and n-type transistors have equal mobility. In conclusion, the HPSC and the NEW-HPSC are two full adders that in MOSFET technology, the NEW-HPSC is dominant, while in CNFET technology, the HPSC has better results.

# 2. PRACTICAL SIMULATION

In this section, first, the simulation environments are proposed. Then, comprehensive simulations are performed to scrutinize the performance of each full adder cell. We simulate different cells with various loads, and power supplies. Then, their efficiency is studied in a large test bed. Furthermore, their susceptibility to noise and manufacturing process variations is also considered.

Simulation Setup In order to perform computer simulations, we use a well-known compact SPICE CNFET model proposed in [22] and [23]. This model is developed for MOSFET-like single-wall CNFETs. It considers nonidealities, such as the screening effect by the parallel CNTs for CNFET with multiple CNTs, Schottky-barrier resistance, parasitic gate capacitances, the elastic scattering in the channel region, the resistive source/drain (S/D), and so on. Table III shows some important parameters of the SPICE model with their values and brief descriptions. We have used the chirality vector of (19, 0) [22] and also three tubes as the channel of each transistor [23].By this selection, the diameter and the absolute value of threshold voltage of transistors are

reached 1.487 nm and 0.28 V, respectively. Simulations are performed using Synopsys HSPICE tool for transistors with 32-nm channel length.




## 2.1 RESULT'S AND DISCUSSIONS OF PARAMETER

Table IV shows the simulation results of the XOR/XNOR circuit with regard to varying output loads. We have reported power, delay, PDP, number of transistors (No. Tr.), and energy delay product (EDP) metrics for different circuits.

It is worth to note that the fan-out of FO2 is enough for studying the performance metrics of XOR/XNOR that is used in a full adder cell. However, we have extended our simulations to the fan-out of FO16. Shaded boxes show the best results in Table IV.

TABLE IV
AVERAGE POWER CONSUMPTION (E-6 W), DELAY (E-11 S), PDP (E-17 J), NUMBER OF TRANSISTORS, AND EDP (E-28 J.S) RESULTS FOR DIFFERENT LOADS

| Load | | FO2 | | | | | FO16 | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Design | Reference | Power | Delay | PDP | No. Tr. | EDP | Power | Delay | PDP | No. Tr. | EDP |
| X-Design1 | [Proposed] | 0.57673 | 1.4380 | 0.82933 | 12 | 1.19257 | 17.533 | 11.096 | 194.54 | 12 | 2158.61 |
| X-Design2 | [Proposed] | 0.11960 | 1.2398 | 0.14828 | 14 | 0.18383 | 1.4075 | 6.4962 | 9.1431 | 14 | 59.3954 |
| X-Design3 | [Proposed] | 0.09096 | 0.4269 | 0.03884 | 16 | 0.01658 | 0.8686 | 1.9247 | 1.6718 | 16 | 3.21771 |
| X-Design4 | [Proposed] | 0.08608 | 0.4091 | 0.03522 | 14 | 0.01440 | 0.9817 | 2.0972 | 2.0588 | 14 | 4.31771 |
| X-Design5 | [Proposed] | 0.07624 | 0.4703 | 0.03585 | 12 | 0.01686 | 1.0269 | 2.4801 | 2.5469 | 12 | 6.31656 |
| CPL-TG | [4] | 0.12580 | 0.9059 | 0.11397 | 10 | 0.10324 | 1.7706 | 4.9764 | 8.8114 | 10 | 43.8490 |
| HPSC | [8] | 0.11573 | 1.7726 | 0.20514 | 10 | 0.36363 | 1.6474 | 8.8313 | 14.549 | 10 | 128.486 |
| NEW-HPSC | [9] | 0.12933 | 2.1758 | 0.28139 | 8 | 0.61224 | 2.0043 | 11.020 | 22.088 | 8 | 243.409 |
| Ours1 | [10] | 0.07227 | 0.4500 | 0.03252 | 12 | 0.01463 | 0.95026 | 2.0005 | 1.9010 | 12 | 3.80295 |
| HCTG | [11] | 0.07114 | 0.8194 | 0.05829 | 8 | 0.04776 | 0.88218 | 4.9910 | 4.4029 | 8 | 21.9748 |
| TFA | [3] | 0.06900 | 0.8318 | 0.05739 | 8 | 0.04773 | 0.88958 | 4.7267 | 4.2048 | 8 | 19.8748 |
| TGA | [1] | 0.70007 | 6.4656 | 4.5264 | 10 | 29.2658 | 12.837 | 42.006 | 539.23 | 10 | 22650.8 |
| 13A | [6] | 1.6346 | 2.7016 | 4.4160 | 8 | 11.9302 | 48.783 | 22.546 | 1099.8 | 8 | 24796.0 |
| CLRCL | [7] | 1.3623 | 6.5932 | 8.9819 | 6 | 59.2194 | 27.310 | 45.276 | 1236.5 | 6 | 55983.7 |
| Wang | [24] | 0.13676 | 1.6974 | 0.23213 | 12 | 0.39401 | 0.90266 | 5.3881 | 4.8636 | 12 | 26.2055 |

## 2.2 APPLICATIONS

There are many VLSI applications, such as digital signal processing, image and video processing, microprocessors, and microcontrollers that extensively use arithmetic operations.

Among various arithmetic operations, addition, subtraction, multiplication, and multiply and accumulate are mostly used.

All aforementioned operations could be realized using the addition function. Therefore, a 1-bit full adder cell still plays an important role in determining the performance metrics of an entire system.

Furthermore, a 1-bit full adder cell is used in arithmetic logic unit of a processor, in floating-point unit, and address generation for cache or memory access. Until now many full adder cells with different logic styles are reported in the literature using the metal–oxide–semiconductor FET (MOSFET) technology, each having its own merits and demerits [1]–[11].

### 2.2.1 ADVANTAGES

- In MOSFET technology, the ratio of size of pMOS to nMOS should be almost three to have equal switching speed between them and good noise margin for the circuit.
- This causes the existence of large input capacitance in MOSFET technology and consequently more delay and power dissipation.
- On the other hand, since in CNFET technology, the both p-type (pCNFET) and n-type (nCNFET) transistors have equal current driving capability with the same transistor dimension.
- However, this approach results in transistor count overhead and removes the advantage of small transistor count in large cascaded circuits.
- The TGA cell performs better than the TFA due to employing TGs at the output nodes instead of pass transistors. In fact, its delay and power dissipation are less than that of TFA, especially in larger circuits.
- The structure of a complementary pass-transistor logic TG (CPL-TG) is reported in [4]. The CPL-TG not only is dual rail but also provides driving

capability at the expense of large transistor count. Then, it is advantageous in the cascaded circuits

# 3.CONCLUSION

The proposed cells perform well with supply voltage scaling and even under different output loads. When they are used in large adders, such as RCA, they outperform their counterparts and make them to be fitting to the large circuits.

In addition, the susceptibility of full adders against both noise and process variations was considered. In noise point of view, we observed that the proposed designs had a close competition with other full adders, and in some cases, they outperformed them.

Finally, to study the robustness of the full adders against the diameter variations of CNTs embedded in the channel of CNFET devices, we performed the MC transient analysis. Simulation results confirmed that the proposed cells are more robust than other cells with regard to process variation, making them suitable for implementing in the CNFET technology.

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