

RK818

Power Management System

Specifications

PRELIMINARY CONFIDENTIAL

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Fuzhou Rockchip Electronics Co.Ltd

Power Management System

Revision History

| Date | Version | Remarks |
|------------|---------|---|
| 2013-11-19 | 0.1 | Initial Specifications |
| 2014-03-15 | 0.2 | Register map added |
| 2014-7-18 | 0.3 | <ol style="list-style-type: none">1. Added ordering information2. Added Operational Description |
| 2015-05-05 | 0.5 | <ol style="list-style-type: none">1. Added RK818-1/RK818-2 ordering information and package mark information2. Added RK818-1/RK818-2 start up sequence and voltage information |
| 2015-10-23 | 0.6 | <ol style="list-style-type: none">1. Adding I2C slave address and changing timing spec2. changing charger register3. adding description of gas gauge register |
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1 DESCRIPTION

The RK818 is a complex power-management integrated circuit (PMIC) for multi-core system applications powered by a Li-ion or a Li-ion polymer battery cell, or by a 5V input either from an USB port or from an adaptor. The RK818 can provide a complete power management solution with very few external components.

The RK818 provides four configurable synchronous step-down converters and one synchronous step-up converter with current capability up to 4A and 2.5A, respectively. The device also contains 9 LDO regulators, one linear switch, one switch-mode charger, a battery fuel gauge, and the power path management function. Power-up/power-down controller is configurable and can support any customized power-up/power-down sequences (OTP based). A real-time clock (RTC) is also integrated to provide a 32-kHz output buffer, and real time function. The RK818 supports 32-kHz clock generation based on a crystal oscillator.

The switch-mode charger, together with the power path controller integrated in the RK818, allows supplying power to the loads while it is charging the battery. The charger provides functions such as input current limiting, trickle current charging, constant current (CC)/constant voltage (CV) charging, charging termination, charging over time protection, etc. All these functions can be conveniently configured through the I²C digital interface. The input current limit can be set to maximum 3A to accommodate a power adaptor as the input supply. When an input current limiting is triggered, the power path controller will distribute the input power in a way that the loads have the higher priority than the battery to take the input power. The difference between the input and output power will be used to charge the battery. In a case that the output power required by the loads exceeds the input power, the power path controller will automatically turn on the battery switch so that the battery can supply extra power to the loads together with the input supply. A “battery fuel gauge” is also integrated in the RK818. Using the proprietary algorithms and the sensed battery current and voltage, the gauge can accurately calculate the battery capacity based on the charging/discharging characteristics of the battery preloaded in the system. The gauge then sends the battery capacity information to the processor through the I²C interface. Other functions that the charger provides includes tiny current charging for an over discharged battery, or so called “dead battery”, battery temperature monitoring, safe charging timer and over temperature shut down.

The RK818 can dynamically adjust the output voltage of each DC-DC converter, as required by the processor based on the processor's operation status so as to maximize the system efficiency. The output voltages of most channels can be configured through the I²C interface. The inputs of all channels have soft start function, which greatly reduces the inrush current at the startup. The frequency compensations of all the control loops are implemented internally to eliminate external compensation components.

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The 2MHz switching frequency allows small size inductors to be used for both buck and boost converters. Also, as all the power switches are integrated on chip, no external power switches and Schottky diodes are needed, which reduces the system cost significantly.

The RK818 is available in a QFN68 7.0 mm x 7.0 mm package, with a 0.35-mm pin pitch.

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2 FEATURES

- Input range: 3.8V - 6V for USB input; 2.7V - 4.5V for BAT input
- Switch mode Li-ion battery charger providing charging current up to 3A ($R_s=20m\Omega$).
- Power path controller with 5A ($R_s=20m\Omega$) current path.
- Accurate battery fuel gauge.
- Real time clock (RTC)
- Low standby current of less than 40uA (at 32KHz clock frequency)
- 2MHz switching frequency for the buck converters
- 1MHz switching frequency for the boost converter
- Fast transient response due to the current mode architecture
- Internal frequency compensation and soft start
- Programmable output voltage and power up/down sequence through I2C interface
- Proprietary circuit architecture achieving high efficiency
- Internal discharge path in off state for BUCs and LDOs
- Power channels:
 - Ch1: Synchronous buck converter, 4A max
 - Ch 2: Synchronous buck converter, 4A max
 - Ch 3: Synchronous buck converter, 2.5A max
 - Ch 4: Synchronous buck converter, 2.5A max
 - Ch5: Synchronous boost converter, 2.5A max
 - Ch6—7, Ch9 and Ch11: LDOs, 150mA max
 - Ch8: Low noise, high PSRR LDO ,100mA max
 - Ch10, 12,14: LDOs, 300mA max
 - Ch13: LDO, 400mA max
 - Ch15: Low $R_{ds(on)}$ switch,0.15ohm ($V_{gs}=3V$)
 - Ch16: HDMI5V switch, 80mA max
 - Ch17: OTG switch, 800mA max
- Fixed and programmable power up/down sequences
- Package: 7mmx7mm QFN68

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3 BLOCK DIAGRAM

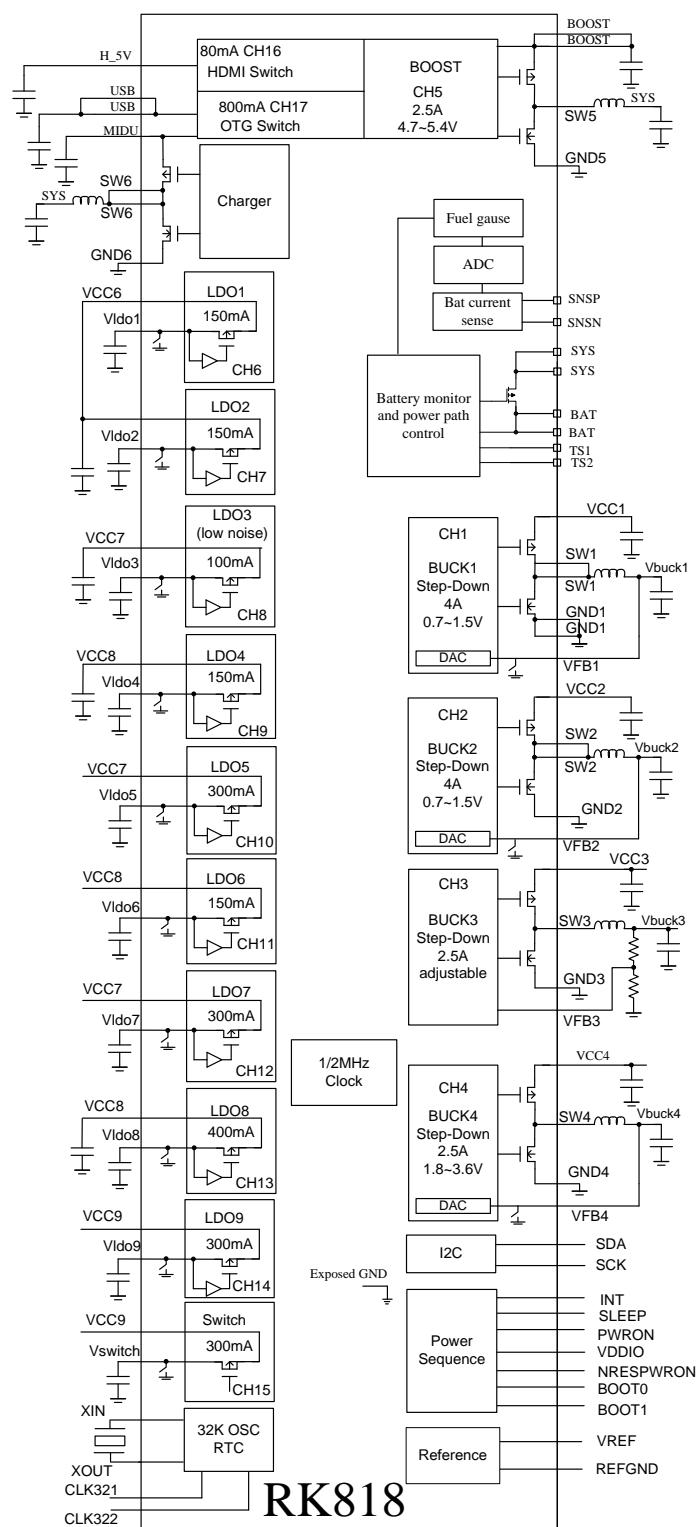


Figure 3-1 System Block Diagram

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4 TYPICAL APPLICATION

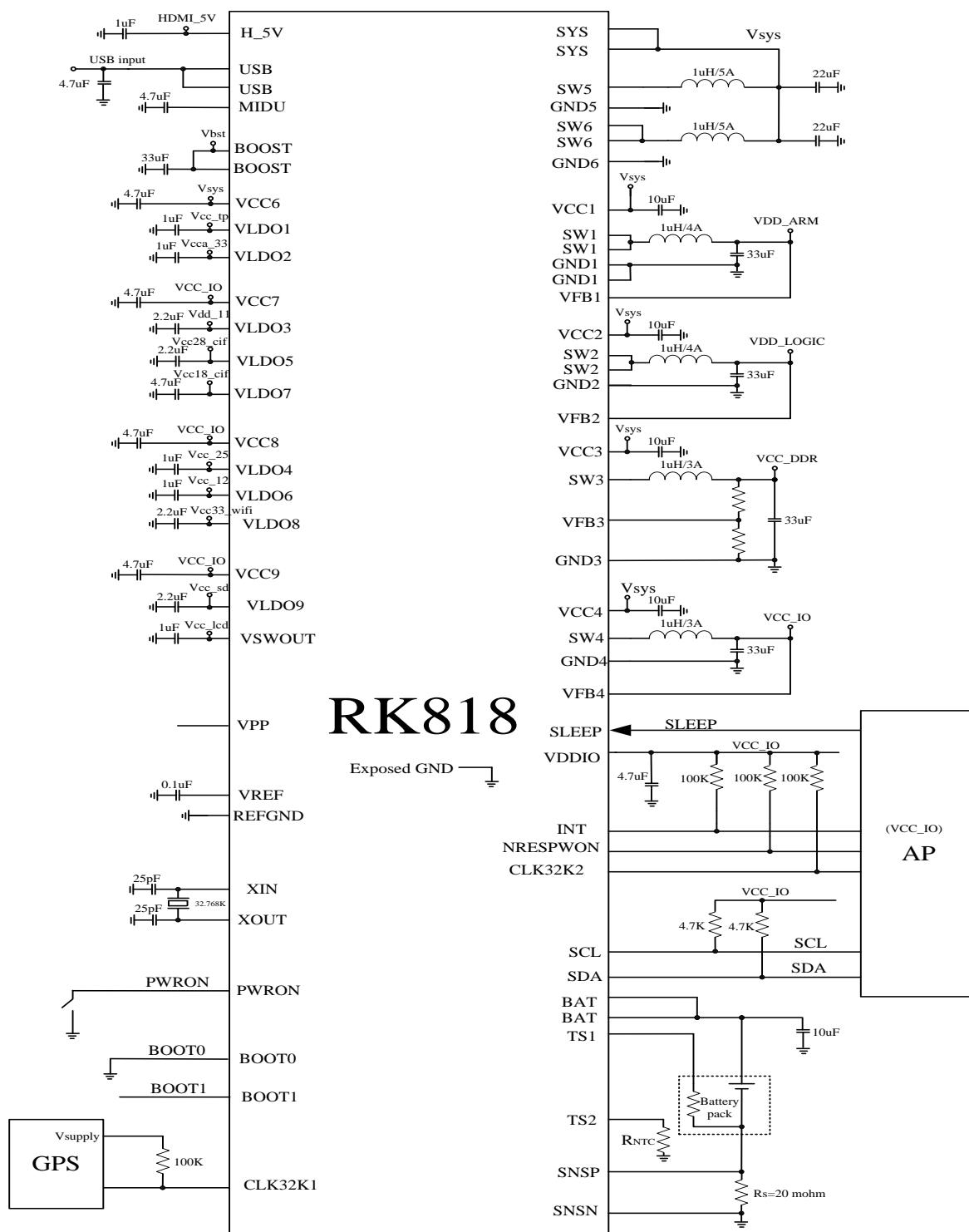


Figure 4-1 RK818 Typical Application Diagram

5 PIN DESCRIPTION

QFN68 7mm x 7mm, pitch0.35mm

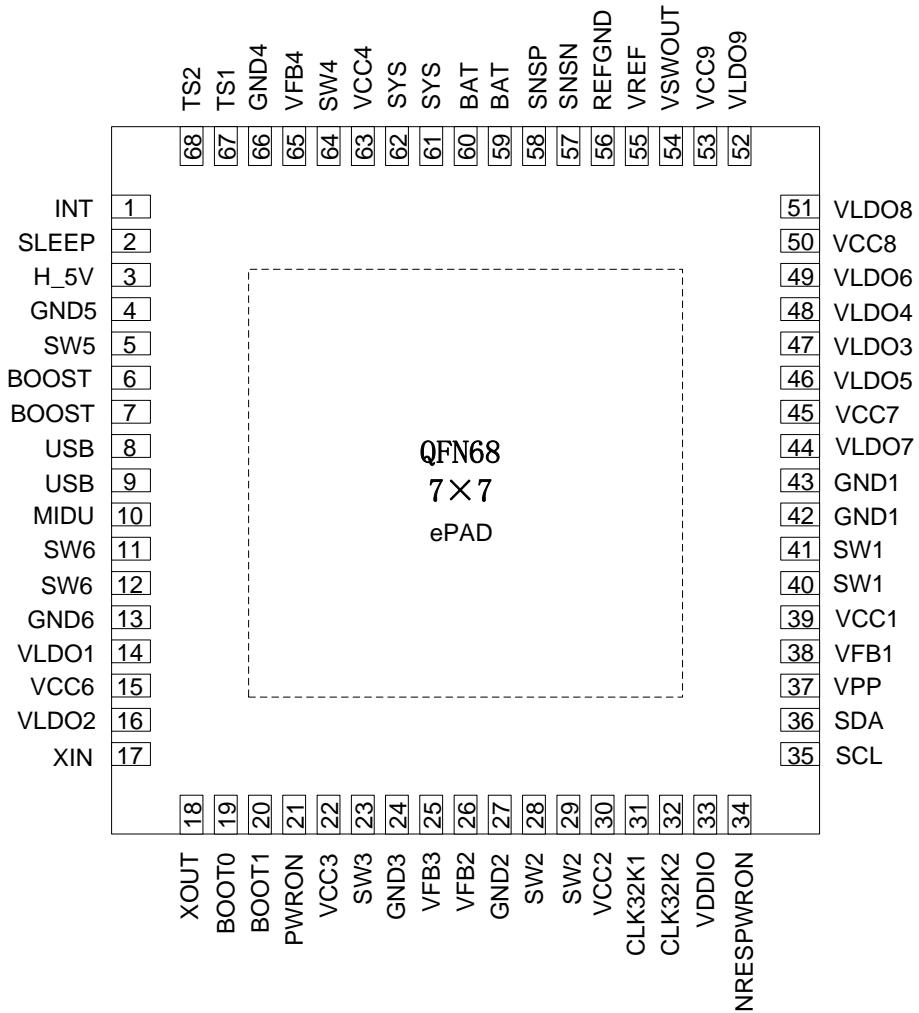


Figure 5-1 Package Pinout

6 PINOUT DEFINITION

| Pin No | Pin Name | Pin Description |
|--------|----------|--|
| 1 | INT | Interrupt request pin. Active low. |
| 2 | SLEEP | Input pin for switching state between sleep and non-sleep state. |
| 3 | H_5V | 5v supply output for HDMI |

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| 4 | GND5 | Power ground |
| 5 | SW5 | Switch output |
| 6,7 | BOOST | BOOST output |
| 8,9 | USB | Power input from USB |
| 10 | MIDU | Middle point of USB power supply |
| 11,12 | SW6 | Switch output |
| 13 | GND6 | Power ground |
| 14 | VLDO1 | LDO1 output |
| 15 | VCC6 | Power supply for LDO |
| 16 | VLDO2 | LDO2 output |
| 17 | XIN | 32.768KHz crystal oscillator input |
| 18 | XOUT | 32.768KHz crystal oscillator output |
| 19 | BOOT0 | Boot sequence selection, low bit |
| 20 | BOOT1 | Boot sequence selection, high bit |
| 21 | PWRON | Power on or power off enable pin, active low, internal 100K pull high to power supply |
| 22 | VCC3 | Power supply for DCDC3 |
| 23 | SW3 | Switch output of DCDC3 |
| 24 | GND3 | Power ground for DCDC3 |
| 25 | VFB3 | feedback voltage for DCDC3 |
| 26 | VFB2 | DCDC2 output voltage feedback input |
| 27 | GND2 | Power ground for DCDC2 |
| 28,29 | SW2 | Switch output of DCDC2 |
| 30 | VCC2 | Power supply for DCDC2 |
| 31 | CLK32K1 | 32.768K clock1 output, open drain, |
| 32 | CLK32K2 | 32.768K clock2 output, open drain, |
| 33 | VDDIO | Power supply for IO |
| 34 | NRESPWON | Reset pin after power on, active low |
| 35 | SCL | Clock input of I2C |
| 36 | SDA | Data input/output of I2C |
| 37 | VPP | Power supply for testing, floating in the application |
| 38 | VFB1 | DCDC1 output voltage feedback input |
| 39 | VCC1 | Power supply for DCDC1 |
| 40,41 | SW1 | Switch output of DCDC1 |
| 42,43 | GND1 | Power ground for DCDC1 |
| 44 | VLDO7 | LDO7 output |
| 45 | VCC7 | Power supply for LDO |

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| 46 | VLDO5 | LDO5 output |
| 47 | VLDO3 | LDO3 output |
| 48 | VLDO4 | LDO4 output |
| 49 | VLDO6 | LDO6 output |
| 50 | VCC8 | Power supply for switch |
| 51 | VLDO8 | LDO8 output |
| 52 | VLDO9 | LDO9 output |
| 53 | VCC9 | Power supply for LDO |
| 54 | VSWOUT | Switch output |
| 55 | VREF | Internal reference voltage |
| 56 | REFGND | Reference ground |
| 57 | SNSN | Bat charging and discharging sense current negative pin |
| 58 | SNSP | Bat charging and discharging sense current positive pin |
| 59,60 | BAT | Positive battery terminal |
| 61,62 | SYS | DC-DC regulator output to power the system load and charge the battery |
| 63 | VCC4 | Power supply for DCDC4 |
| 64 | SW4 | Switch output of DCDC4 |
| 65 | VFB4 | DCDC4 output voltage feedback input |
| 66 | GND4 | Power ground for DCDC4 |
| 67 | TS1 | Thermistor1 input. Connect a thermistor from this pin to ground. The thermistor is usually inside the battery pack. |
| 68 | TS2 | Thermistor2 input. Connect a thermistor from this pin to ground. Or it can be used as analog input pin of internal ADC if the control bit is set to ADC function. |
| Exposed pad | Exposed ground | It must be connected to ground for thermal and electrical enhancement. |

Table 1 Pin Descriptions

Power Management System

7 ORDERING INFORMATION

| Orderable Device | RoHS status | Package | Package Qty | Device special feature |
|------------------|-------------|------------|---|------------------------|
| RK818-1 | RoHS pass | QFN68(7X7) | 2600ea/inner box* 6 inner boxes/outer box | For RK3288/RK3368 |
| RK818-2 | RoHS pass | QFN68(7X7) | 2600ea/inner box* 6 inner boxes/outer box | For S-product |
| RK818-3 | RoHS pass | QFN68(7X7) | 2600ea/inner box* 6 inner boxes/outer box | For RK3399 |



Rockchip: Brand Name

RK818-X: Chip Name(X is 1 or 2 or 3)

ABC: Subcontractor Code

XXXXXX: Die Lot No #

DEFG: Date Code Year&Week

8 ABSOLUTE MAXIMUM RATINGS

| Parameter | Min | Max | Units |
|---|------|--------------------------|-------|
| Voltage range on pins USB , MIDU , BOOST , SWx/H_5V | -0.3 | 6.5 | V |
| Voltage range on pins VCCx, VFBx, VLDOx, VSWOUT, VREF | -0.3 | 6.5 | V |
| Voltage range on pin CLK32K1,CLK32K2, SLEEP | -0.3 | 6.5 | V |
| Voltage range on pins XIN,XOUT, BOOT0,BOOT1, PWRON | -0.3 | VSYS _{MAX} +0.3 | |
| Voltage range on pins NRESPWRON, INT, SDA, SCL | -0.3 | 4 | V |
| Storage temperature range, T _S | -40 | 150 | °C |
| Operating temperature range, T _J | -40 | 125 | °C |
| Maximum Soldering Temperature,T _{SOLDER} | | 300 | °C |

Table 2 Absolute Maximum Ratings

Note 1. Exposure to the conditions exceeded absolute maximum ratings may cause the permanent damages and affect the reliability and safety of both device and systems using the device. The functional operations cannot be guaranteed beyond specified values in the recommended

Power Management System

conditions.

9 RECOMMENDED OPERATING CONDITIONS

| Parameter | Min | TYP | Max | Units |
|-----------------------------|-----|-----|-----|-------|
| Voltage range on pins USB | 4 | 5 | 5.5 | V |
| Voltage range on other pins | | | 5.5 | V |
| Power Dissipation | | | 2.7 | W |

Table 3 Recommended Operating Conditions

10 ELECTRICAL CHARACTERISTICS

Test conditions: $V_{USB} = 5.0V$, $T_A = 25^\circ C$ for typical values, unless otherwise noted.

| PARAMETERS | SYMBOL | CONDITION | MIN | TYP | MAX | UNIT |
|---|---------------------|-------------------------|------|-----|------|------|
| USBIN | | | | | | |
| USB Operating Range | V_{USB} | | 4 | 5 | 6 | V |
| USB Under Voltage Lockout Threshold | | Rising | 3.65 | 3.8 | 3.95 | V |
| | | Falling | | 3.6 | | V |
| USB vs BATT Threshold | | Rising | | 70 | | mV |
| | | Falling | | 30 | | mV |
| USB Input Current Limit | I_{USB} | Min Current | 60 | 80 | 100 | mA |
| | | Default | 400 | 450 | 500 | mA |
| | | Max current | 2.7 | 3 | 3.3 | A |
| | | step (from 1A to 3A) | | 200 | | mA |
| Maximum USB and BATT Power on Reset Threshold (Rising) | V_{PORH} | | | | 2.2 | V |
| Maximum USB and BATT Power on Reset Threshold (Falling) | V_{PORL} | | 1.2 | | | V |
| Over Voltage Lock Out Threshold (USB Rising) | $V_{TH(OVLO)}$ | | 5.7 | 6.0 | 6.3 | V |
| Over Voltage Lock Out Hysteresis | V_{HYS} (OVLO) | | | 0.2 | | V |
| High-Side PMOS Peak Current Limit | | 0.5A step, Default=4.5A | 4 | | 5.5 | A |
| USB Input Quiescent Current | $I_{USBquie}$ | Charger Enable mode | | | 10 | mA |

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| PARAMETERS | SYMBOL | CONDITION | MIN | TYP | MAX | UNIT |
|--|----------------------|---|------|---------------------------|------|-----------------|
| | t | | | | | |
| CHARGING CONTROLLER | | | | | | |
| Terminal Battery Voltage | V _{BAT} | VBAT>VRECH, I _{CHG} ≤ I _{BF} | | 4.05 | | V |
| | | | | 4.1 | | V |
| | | | | 4.15 | | V |
| | | | | 4.2 | | V |
| | | | | 4.25 | | V |
| | | | | 4.3 | | V |
| | | | | 4.35 | | V |
| | | | -1 | | 1 | % |
| Recharge Threshold at V _{BATT} | V _{RECH} | | | V _{BAT} -0.15 | | V |
| Recharge Hysteresis | | | | 75 | | mV |
| Trickle Charge Threshold | V _{TRICKLE} | | 2.85 | 3.0 | 3.15 | V |
| Trickle Charge Hysteresis | | | | 200 | | mV |
| Trickle Charge Current | I _{TRICKLE} | | | 10% | | I _{CC} |
| Dead bat Charge Threshold | V _{DEAD} | | 1.8 | 2 | 2.2 | V |
| Dead bat Charge Hysteresis | | | | 200 | | mV |
| Dead bat Charge Current | I _{DEAD} | | | 70 | | mA |
| Termination Charger Current | I _{BF} | Rs=20mΩ, 50mA Step, default=150mA | 100 | | 250 | mA |
| | | Rs=10mΩ, 100mA Step, default=300mA | 200 | | 500 | mA |
| BAT Leakage Current | I _{BATT} | V _{BAT} =4.2V, SYS float, USB float | | 20 | 30 | uA |
| Charge current | I _{CC} | Rs=20mΩ, 0.2A step, default=2A | 1 | | 3 | A |
| | | Rs=10mΩ, 0.4A step, default=4A | 2 | | 6 | A |
| Trickle Charge Time | | 30 minutes step, default=60 minutes | 30 | | 210 | Min |
| Total Charge Time | | 2 hours step, default=6 | 4 | | 16 | Hour |
| Conversion Efficiency, Constant voltage stage (Vin=5V,Vbat=4.2V) | | | | 84 | | |
| Ibat=3A | | | | 87 | | |
| Ibat=2.5A | | | | 89 | | |
| Ibat=2A | | | | | | % |

Power Management System

| PARAMETERS | SYMBOL | CONDITION | MIN | TYP | MAX | UNIT |
|---|-------------------|--|------|------|------|------|
| Ibat=1.5A | | | | 91 | | |
| Ibat=1A | | | | 94 | | |
| Ibat=500mA | | | | 93 | | |
| Ibat=200mA | | | | 95 | | |
| Conversion Efficiency, Constant voltage stage (Vin=5V,Ibat=2A) | | | | 86 | | |
| Vbat=3.6V | | | | 87 | | |
| Vbat=3.8V | | | | 88 | | % |
| Vbat=4.0V | | | | 89 | | |
| Vbat=4.2V | | | | | | |
| A/D CONVERTER | | | | | | |
| Resolution | | | | 12 | | bits |
| Input voltage range | | Battery voltage | 0 | | 4.4 | V |
| | | Current channel | -64 | | 64 | mV |
| | | TS1/TS2 | 0 | | 2.2 | V |
| Supply current | Active | | | 0.6 | | mA |
| SYS INPUT | | | | | | |
| SYS Regulation Voltage | VSYS | Auto setting | | 3.6 | | V |
| | | | | 4.4 | | V |
| BAT to SYS Resistance | | I _{SYS} =200mA , V _{BAT} =4.2V | | 0.05 | 0.08 | Ω |
| BAT to SYS Current Limit | IBATLIM | Rs=20mΩ , 0.5A step,default=5A | 3 | | 5 | A |
| | | Rs=10mΩ , 1A step,default=10A | 6 | | 10 | A |
| | | SYS short, Rs=20mΩ | | 200 | | mA |
| | | SYS short, Rs=10mΩ | | 400 | | mA |
| BAT to SYS Current Limit accuracy | | | -10 | | 10 | % |
| SYS voltage range | VSYSINPUT | | 2.7 | | 5.45 | V |
| SYS low alarm voltage, if 3.3V (2.8V~3.5V programmable, step=100mV) | V _{BLO} | | 3.25 | 3.3 | 3.35 | V |
| SYS under voltage threshold (vin falling) | V _{BUVL} | | | 2.7 | | V |
| SYS under voltage threshold (vin rising) | V _{BUVH} | | 2.8 | 2.9 | 3.0 | V |

Power Management System

| PARAMETERS | SYMBOL | CONDITION | MIN | TYP | MAX | UNIT |
|---|------------------------|-------------------------------|------------------------|---------------|-----------------------|-------|
| SYS OK voltage threshold (3.3V~3.6V OTP programmable, step=100mV) | V _{BOK} | | | 3.4 | | V |
| Stand-by current, V _{DD} =3.6V, device OFF state 32KHz clock running | I _{Q(STNBY)} | | | 40 | | uA |
| THERMAL PROTECTION | | | | | | |
| Thermal Limit Temperature | | 10 °C step, default=85 °C | 85 | | 115 | °C |
| Thermal Shutdown | | 20 °C step, default=140 °C | 140 | | 160 | °C |
| OSCILLATOR | | | | | | |
| Switching Frequency CH1,2,3,4(T _j =25°C) | f _{sw} | | 1.8 | 2 | 2.2 | MHz |
| Switching Frequency, CH5(T _j =25°C) | f _{sw} | | 0.9 | 1 | 1.1 | MHz |
| LOGIC INPUT | | | | | | |
| Input LOW-Level Voltage (V _{DDIO}) | V _{IL} | | | | 0.3xV _{DDIO} | V |
| Input HIGH-Level Voltage (V _{DDIO}) | V _{IH} | | 0.7xV _{DDIO} | | | V |
| LOGIC OUTPUT | | | | | | |
| LOW-Level Output Voltage, 3.0 mA sink current | V _{OL} | | | | 0.4 | V |
| HIGH-Level Output Voltage, 3.0 mA source current | V _{OH} | | V _{DDIO} -0.4 | | | V |
| NRESPWON pin LOW-Level Output Voltage, 3.0mA sink current | V _{OL(NRES)} | | | | 0.4 | V |
| CLK32KOUT1 pin LOW-Level Output Voltage, 3.0mA sink current | V _{OL(CLKO1)} | | | | 0.4 | V |
| CLK32KOUT2 pin LOW-Level Output Voltage, 3.0mA sink current | V _{OL(CLKO2)} | | | | 0.4 | V |
| CLK32KOUT2 pin HIGH-Level Output Voltage, 3.0mA source current | V _{OH(CLKO2)} | | V _{DDIO} -0.4 | | | V |
| CH1 : BUCK DC-DC CONVERTER(BUCK1) | | | | | | |
| Input supply voltage range | V _{INPUT1} | | 2.7 | | 5.5 | V |
| Voltage Adjustable Range, 6bit | V _{FB1} | Step=12.5mV | 0.7125 | | 1.500 | V |
| Output voltage transition rate BUCK1_RATE=00 BUCK1_RATE=01 BUCK1_RATE=10 | | | | 2 3 4.5 | | mV/us |

Power Management System

| PARAMETERS | SYMBOL | CONDITION | MIN | TYP | MAX | UNIT |
|---|---------------------------|---------------------------|-------|-------|-------|------|
| BUCK1_RATE=11 | | | | 6 | | |
| Power Good threshold (Vout rising) | V _{PG1} | | | 93 | | % |
| Output under voltage lockout(Vout falling) | V _{UV1} | | | 85 | | % |
| Output over voltage lockout (Vout rising) | V _{Ov1} | | | 117 | | % |
| Preset Voltage, Default(T _j =25°C) | V _{FB1(Default)} | | 1.078 | 1.100 | 1.122 | V |
| Preset Voltage, Default(-10°C≤T _j ≤+85°C) | V _{FB1(Default)} | | 1.067 | 1.100 | 1.133 | V |
| Load Regulation, I _{OUT1} = 200mA to 4A | | | | 0.1 | | %/A |
| Line Regulation, VCC1 = 3 to 5.5V, I _{OUT1} = 2A | | | | 0.1 | | %/V |
| Rated output current | I _{MAX1} | Reg90H<1:0>=<11> | | 4 | | A |
| Switch Current Limit | I _{CL1} | 0.4A step, default=3.6A | 3.2 | | 4.4 | A |
| Operating Quiescent Current, No load, V _{DD} =3.8V | I _{Q1} | | | 70 | | uA |
| Minimun Switch Current Limit | I _{CLMIN1} | 50mA step, default=150mA | 50 | | 400 | mA |
| Minimum ON Time | T _{on1(min)} | | | 45 | | ns |
| Soft-start Time | t _{ss1} | Step=400us, default=400us | 400 | | 800 | us |
| C _{OUT} Discharge Switch ON Resistance | R _{DIS2} | | | 250 | | ohm |
| Conversion Efficiency (Vin=3.8V,Vout=1.1V) | | | | | | |
| Iout=4A | | | | 65 | | |
| Iout=3.5A | | | | 68 | | |
| Iout=3A | | | | 71 | | |
| Iout=2.5A | | | | 75 | | % |
| Iout=2A | | | | 79 | | |
| Iout=1.5A | | | | 83 | | |
| Iout=1 A | | | | 86 | | |
| Iout=500mA | | | | 89 | | |

Power Management System

| PARAMETERS | SYMBOL | CONDITION | MIN | TYP | MAX | UNIT |
|--|---------------------------|---------------------------|--------|--------------------|-------|-------|
| Iout=100 mA | | | | 80 | | |
| Iout=10 mA | | | | 81 | | |
| CH2: BUCK DC-DC CONVERTER (BUCK2) | | | | | | |
| Input supply voltage range | V _{INPUT2} | | 2.7 | | 5.5 | V |
| Voltage Adjustable Range, 6bit | V _{FB2} | Step=12.5mV | 0.7125 | | 1.500 | V |
| Output voltage transition rate BUCK2_RATE=00 BUCK2_RATE=01 BUCK2_RATE=10 BUCK2_RATE=11 | | | | 2 3 4.5 6 | | mV/us |
| Power Good threshold (Vout rising) | V _{PG2} | | | 93 | | % |
| Output under voltage lockout (Vout falling) | V _{UV2} | | | 85 | | % |
| Output over voltage lockout (Vout rising) | V _{OV2} | | | 117 | | % |
| Preset Voltage, Default(T _j =25°C) | V _{FB2(Default)} | | 1.078 | 1.100 | 1.122 | V |
| Preset Voltage, Default(-10°C ≤ T _j ≤ +85°C) | V _{FB2(Default)} | | 1.067 | 1.100 | 1.133 | V |
| Load Regulation, I _{OUT2} = 200 mA to 4A | | | | 0.1 | | %/A |
| Line Regulation, VCC2 = 3 to 5.5V, I _{OUT2} = 2A | | | | 0.1 | | %/V |
| Rated output current | I _{MAX2} | Reg90H<3:2>=<11> | | 4 | | A |
| Switch Current Limit | I _{CL2} | 0.4A step, default=3.6A | 3.2 | | 4.4 | A |
| Operating Quiescent Current, No load, V _{DD} =3.8V | I _{Q2} | | | 70 | | uA |
| Minimun Switch Current Limit | I _{CLMIN2} | 50mA step, default=150mA | 50 | | 400 | mA |
| Minimum ON Time | T _{on2(min)} | | | 45 | | ns |
| Soft-start Time | t _{ss2} | Step=400us, default=400us | 400 | | 800 | us |
| C _{OUT} Discharge Switch ON Resistance | R _{DIS2} | | | 250 | | ohm |
| Conversion Efficiency (Vin=3.8V,Vout=1.1V) Iout=4A Iout=3.5A | | | | 62 65 | | % |

Power Management System

| PARAMETERS | SYMBOL | CONDITION | MIN | TYP | MAX | UNIT |
|---|---------------------------|---------------------------|------|------|------|------|
| Iout=3A | | | | 69 | | |
| Iout=2.5A | | | | 73 | | |
| Iout=2A | | | | 76 | | |
| Iout=1.5A | | | | 81 | | |
| Iout=1 A | | | | 85 | | |
| Iout=500mA | | | | 89 | | |
| Iout=100 mA | | | | 85 | | |
| Iout=10 mA | | | | 83 | | |
| CH3: BUCK DC-DC CONVERTER (BUCK3) | | | | | | |
| Input supply voltage range | V _{INPUT3} | | 2.7 | | 5.5 | V |
| Feedback Voltage, Default(T _j =25°C) | V _{FB3(Default)} |) | 0.98 | 1.00 | 1.02 | V |
| Feedback Voltage, Default(-10°C ≤ T _j ≤+85°C) | V _{FB3(Default)} |) | 0.97 | 1.00 | 1.03 | V |
| Power Good threshold (Vout rising) | V _{PG3} | | | 93 | | % |
| Output under voltage lockout (Vout falling) | V _{UV3} | | | 85 | | % |
| Output over voltage lockout (Vout rising) | V _{OV3} | | | 117 | | % |
| Load Regulation, I _{OUT3} = 100mA to 2.5A | | | | 0.1 | | %/A |
| Line Regulation, VCC3 = 3 to 5.5V, I _{OUT3} = 2A | | | | 0.1 | | %/V |
| Rated output current | I _{MAX3} | Reg90H<5:4>=<11> | | 2.5 | | A |
| Switch Current Limit | I _{CL3} | 0.5A step, default=2.5A | 2 | | 3.5 | A |
| Operating Quiescent Current, No load, V _{DD} =3.8V | I _{Q3} | | | 70 | | uA |
| Minimum Switch Current Limit | I _{CLMIN3} | 50mA step, default=150mA | 50 | | 400 | mA |
| Minimum ON Time | T _{on3(min)} | | | 45 | | ns |
| Soft-start Time | t _{ss3} | Step=400us, default=400us | 400 | | 800 | us |
| C _{OUT} Discharge Switch ON Resistance | R _{DIS3} | | | 250 | | ohm |
| Conversion Efficiency | | | | | | % |

Power Management System

| PARAMETERS | SYMBOL | CONDITION | MIN | TYP | MAX | UNIT |
|--|---------------------------|---------------------------|-------|------|------|------|
| (Vin=3.8V,Vout=1.5V) | | | | 70 | | |
| Iout=2.5A | | | | 75 | | |
| Iout=2A | | | | 80 | | |
| Iout=1.5A | | | | 84 | | |
| Iout=1 A | | | | 88 | | |
| Iout=500mA | | | | 84 | | |
| Iout=100 mA | | | | 83 | | |
| Iout=10 mA | | | | | | |
| CH4: BUCK DC-DC CONVERTER (BUCK4) | | | | | | |
| Input supply voltage range | V _{INPUT4} | | 2.7 | | 5.5 | V |
| Voltage Adjustable Range, 4bit | V _{FB4} | Step=100mV | 1.8 | | 3.6 | V |
| Feedback Voltage, Default(T _j =25°C) | V _{FB4(Default)} | | 2.94 | 3.00 | 3.06 | V |
| Feedback Voltage, Default(-10°C ≤ T _j ≤ +85°C) | V _{FB4(Default)} | | -2.91 | 3.00 | 3.09 | V |
| Power Good threshold (Vout rising) | V _{PG4} | | | 93 | | % |
| Output under voltage lockout (Vout falling) | V _{UV4} | | | 85 | | % |
| Output over voltage lockout (Vout rising) | V _{OV4} | | | 117 | | % |
| Load Regulation, I _{OUT4} = 100mA to 2.5A | | | | 0.1 | | %/A |
| Line Regulation, VCC4 = 3 to 5.5V, I _{OUT4} = 2A | | | | 0.1 | | %/V |
| Rated output current | I _{MAX4} | Reg90H<7:6>=<11> | | 2.5 | | A |
| Switch Current Limit | I _{CL4} | 0.5A step, default=3A | 2.5 | | 4 | A |
| Operating Quiescent Current, No load, V _{DD} =3.8V | I _{Q4} | | | 70 | | uA |
| Minimun Switch Current Limit | I _{CLMIN4} | 50mA step, default=150mA | 50 | | 400 | mA |
| Minimum ON Time | T _{on4(min)} | | | 45 | | ns |
| Soft-start Time | t _{ss4} | Step=400us, default=400us | | 400 | | us |
| C _{OUT} Discharge Switch ON Resistance | R _{DIS4} | | | 250 | | Ohm |
| Conversion Efficiency, | | | | | | |

Power Management System

| PARAMETERS | SYMBOL | CONDITION | MIN | TYP | MAX | UNIT |
|---|---------------------------|-------------------------|------|--|------|------|
| (DCR<50mohm) Vin=3.8V,Vout=3V Iout=2.5A Iout=2A Iout=1.5A Iout=1 A Iout=500mA Iout=100mA Iout=10mA | | | | 81 84 87 91 94 88 75 | | % |
| CH5: BOOST DC-DC CONVERTER (BOOST) | | | | | | |
| Input supply voltage range | V _{INPUT5} | | 2.7 | | 4.4 | V |
| Output Voltage | V _{FB5} | Step=0.1v,default=5v | 4.7 | | 5.4 | V |
| Voltage, Default(T _j =25°C) | V _{FB5(Default)} | | 4.90 | 5.0 | 5.10 | V |
| Voltage, Default(-10°C≤ T _j ≤ +85°C) | V _{FB5(Default)} | | 4.75 | 5.0 | 5.25 | V |
| Power Good threshold (Vout rising) | V _{PG5} | | | 90 | | % |
| Output under voltage lockout (Vout falling) | V _{UV5} | | | 85 | | % |
| Load Regulation, I _{OUT5} = 100mA to 2.5A | | | | 0.2 | | %/A |
| Line Regulation, Vin = 3 to 4.2V, I _{OUT5} = 1.5A | | | | 0.1 | | %/V |
| Rated output current | I _{MAX5} | Reg3A<4:3>=11 | | 2.5 | | A |
| Switch Current Limit | I _{CL5} | 0.5A step, default=4.5A | 4 | | 5.5 | A |
| Minimum ON Time | T _{on5(min)} | | | 70 | | ns |
| Soft-start Time | t _{ss5} | | | 400 | | us |
| C _{OUT} Discharge Switch ON Resistance | R _{DIS5} | | | 250 | | ohm |
| Operating Quiescent Current, No load, V _{DD} =3.8V | I _{Q5} | | | 250 | | uA |
| Auto switch load current between PWM and PFM | I _{PWM/PFM5} | | | 50 | | mA |
| Conversion Efficiency, (DCR<50mohm) Vin=3.8V,Vout=5V Iout=2.5A Iout=2A Iout=1.5A | | | | 80 85 | | % |

Power Management System

| PARAMETERS | SYMBOL | CONDITION | MIN | TYP | MAX | UNIT |
|--|-----------------------------------|-----------|-------|-------|-------|-------|
| Iout=800mA | | | | 89 | | |
| Iout=500mA | | | | 93 | | |
| Iout=100mA | | | | 94 | | |
| Iout=10mA | | | | 90 | | |
| | | | | 71 | | |
| CH6 : LD01 | | | | | | |
| Input supply voltage range | V _{INPUT6} | | 2.7 | | 5.5 | V |
| V _{OUT} Output Voltage Adjustable Range, 4bit(step=100mv) | V _{OUT6} | | 1.8 | | 3.4 | V |
| V _{OUT} Output Voltage, Default(Tj=25°C) | V _{OUT6(Defa ult)} | | 3.234 | 3.300 | 3.366 | V |
| V _{OUT} Output Voltage, Default(Tj=-10~85°C) | V _{OUT6(Defa ult)} | | 3.201 | 3.300 | 3.399 | V |
| Power Good threshold (Vout rising) | V _{PG6} | | | 93 | | % |
| Output under voltage lockout (Vout falling) | V _{UV6} | | | 85 | | % |
| V _{OUT} Load Regulation, I _{OUT} = 1mA to 150mA | | | | 0.005 | | %/mA |
| V _{OUT} Line Regulation, V _{IN6} = 3 to 5V, I _{OUT6} = 0.1A | | | | 0.03 | | %/V |
| Power Supply Reject Ratio (f = 10kHz, V _{OUT6} =3.3V) | PSRR6 | | | 50 | | dB |
| Output noise (10Hz to 100kHz, V _{OUT6} =3.3V) | OUT _{NOISE} ₆ | | | 300 | | uVrms |
| Dropout voltage @ 150mA (V _{OUT6} =3.3V) | V _{DROP6} | | | 200 | | mV |
| Rated output current | I _{MAX6} | | | 150 | | mA |
| Operating Quiescent Current, No load, V _{DD} =3.8V | I _{Q6} | | | 28 | | uA |
| Current Limit, V _{OUT6} = V _{OUT6} x 0.95 | I _{CL6} | | 250 | 300 | | mA |
| Soft-start Time | t _{SS6} | | | 400 | | us |
| C _{OUT} Discharge Switch ON Resistance | R _{DIS6} | | | 400 | | ohm |
| CH7 : LD02 | | | | | | |

Power Management System

| PARAMETERS | SYMBOL | CONDITION | MIN | TYP | MAX | UNIT |
|--|----------------------------|-----------|-------|-------|-------|-------|
| Input supply voltage range | V _{INPUT7} | | 2.7 | | 5.5 | V |
| V _{OUT} Output Voltage Adjustable Range, 4bit(step=100mv) | V _{OUT7} | | 1.8 | | 3.4 | V |
| V _{OUT} Output Voltage, Default(T _j =25°C) | V _{OUT7(Default)} | | 3.234 | 3.300 | 3.366 | V |
| V _{OUT} Output Voltage, Default(T _j =-10~85°C) | V _{OUT7(Default)} | | 3.201 | 3.300 | 3.399 | V |
| Power Good threshold (Vout rising) | V _{PG7} | | | 93 | | % |
| Output under voltage lockout (Vout falling) | V _{UV7} | | | 85 | | % |
| Output over voltage lockout (Vout rising) | V _{OV7} | | | 125 | | % |
| V _{OUT} Load Regulation, I _{OUT} = 1mA to 150mA | | | | 0.005 | | %/mA |
| V _{OUT} Line Regulation, V _{IN7} = 3 to 5V, I _{OUT7} = 0.1A | | | | 0.03 | | %/V |
| Power Supply Reject Ratio (f = 10kHz, V _{OUT7} =3.3V) | PSRR7 | | | 50 | | dB |
| Output noise (10Hz to 100kHz, V _{OUT7} =3.3V) | OUT _{NOISE7} | | | 300 | | uVRms |
| Dropout voltage @ 150mA (V _{OUT7} =3.3V) | V _{DROP7} | | | 200 | | mV |
| Operating Quiescent Current, No load, V _{DD} =3.8V | I _{Q7} | | | 28 | | uA |
| Rated output current | I _{MAX7} | | | 150 | | mA |
| Current Limit, V _{OUT7} = V _{OUT7} x 0.95 | I _{CL7} | | 250 | 300 | | mA |
| Soft-start Time | t _{SS7} | | | 400 | | us |
| C _{OUT} Discharge Switch ON Resistance | R _{DIS7} | | | 400 | | Ohm |
| CH8 : LD03 | | | | | | |
| Input supply voltage range | V _{INPUT7} | | 2.7 | | 5.5 | V |
| V _{OUT} Output Voltage Adjustable Range, 4bit (0.8V~2V, step=100mV, 2V~2.5V step=500mV) | V _{OUT8} | | 0.8 | | 2.5 | V |
| V _{OUT} Output Voltage, Default(T _j =25°C) | V _{OUT8(Default)} | | 1.078 | 1.100 | 1.122 | V |

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| PARAMETERS | SYMBOL | CONDITION | MIN | TYP | MAX | UNIT |
|---|-----------------------------------|-----------|-------|-------|-------|-------|
| Vout Output Voltage, Default(Tj=-10~85°C) | V _{OUT8} | (Default) | 1.067 | 1.100 | 1.133 | V |
| Power Good threshold (Vout rising) | V _{PG8} | | | 93 | | % |
| Output under voltage lockout (Vout falling) | V _{UV8} | | | 85 | | % |
| Vout Load Regulation, I _{OUT} = 1mA to 150mA | | | | 0.006 | | %/mA |
| Vout Line Regulation, V _{IN8} = 3 to 5V, I _{OUT8} = 0.05A | | | | 0.015 | | %/V |
| Power Supply Reject Ratio (f = 10kHz, V _{OUT8} =1.1V) | PSRR8 | | | 70 | | dB |
| Output noise (10Hz to 100kHz, V _{OUT8} =1.1V) | OUT _{NOISE} ₈ | | | 30 | | uVRms |
| Dropout voltage @ 100mA (V _{OUT8} =2.5V) | V _{DROP8} | | | 200 | | mV |
| Rated output current | I _{MAX8} | | | 100 | | mA |
| Operating Quiescent Current, No load, V _{DD} =3.8V | I _{Q8} | | | 52 | | uA |
| Current Limit, VOUT8 = V _{OUT8} x 0.95 | I _{CL8} | | 150 | 200 | | mA |
| Soft-start Time | t _{SS8} | | | 400 | | us |
| C _{OUT} Discharge Switch ON Resistance | R _{DIS8} | | | 400 | | Ohm |
| CH9: LD04 | | | | | | |
| Input supply voltage range | V _{INPUT9} | | 2.7 | | 5.5 | V |
| Vout Output Voltage Adjustable Range, 4bit(step=100mv) | V _{OUT9} | | 1.8 | | 3.4 | V |
| Vout Output Voltage, Default(Tj=25°C) | V _{OUT9(Default)} | | 2.450 | 2.500 | 2.550 | V |
| Vout Output Voltage, Default(Tj=-10~85°C) | V _{OUT9(Default)} | | 2.425 | 2.500 | 2.575 | V |
| Power Good threshold (Vout rising) | V _{PG9} | | | 93 | | % |
| Output under voltage lockout (Vout falling) | V _{UV9} | | | 85 | | % |
| Vout Load Regulation, I _{OUT} = 1mA to 150mA | | | | 0.005 | | %/mA |
| Vout Line Regulation, V _{IN9} = 3 to 5V, I _{OUT9} = 0.15A | | | | 0.03 | | %/V |

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| PARAMETERS | SYMBOL | CONDITION | MIN | TYP | MAX | UNIT |
|---|------------------------------------|-----------|-------|-------|-------|-------|
| Power Supply Reject Ratio ($f = 10\text{kHz}$, $V_{OUT9}=3.3\text{V}$) | PSRR9 | | | 50 | | dB |
| Output noise (10Hz to 100kHz, $V_{OUT9}=3.3\text{V}$) | OUT _{NOISE} ₉ | | | 300 | | uVrms |
| Dropout voltage @ 150mA ($V_{OUT9}=3.3\text{V}$) | V _{DROP9} | | | 200 | | mV |
| Operating Quiescent Current, No load, $V_{DD}=3.8\text{V}$ | I _{Q9} | | | 28 | | uA |
| Rated output current | I _{MAX9} | | | 150 | | mA |
| Current Limit, $V_{OUT9} = V_{OUT9} \times 0.95$ | I _{CL9} | | 250 | 300 | | mA |
| Soft-start Time | t _{SS9} | | | 400 | | us |
| C _{OUT} Discharge Switch ON Resistance | R _{DIS9} | | | 400 | | Ohm |
| CH10 : LD05 | | | | | | |
| Input supply voltage range | V _{INPUT10} | | 2.7 | | 5.5 | V |
| V _{OUT} Output Voltage Adjustable Range, 4bit(step=100mv) | V _{OUT10} | | 1.8 | | 3.4 | V |
| V _{OUT} Output Voltage, Default($T_j=25^\circ\text{C}$) | V _{OUT10(Default)} | | 2.744 | 2.800 | 2.856 | V |
| V _{OUT} Output Voltage, Default($T_j=-10\text{~}85^\circ\text{C}$) | V _{OUT10(Default)} | | 2.716 | 2.800 | 2.884 | V |
| Power Good threshold (Vout rising) | V _{PG10} | | | 93 | | % |
| Output under voltage lockout (Vout falling) | V _{UV10} | | | 85 | | % |
| V _{OUT} Load Regulation, $I_{OUT} = 1\text{mA}$ to 300mA | | | | 0.003 | | %/mA |
| V _{OUT} Line Regulation, $V_{IN10} = 3$ to 5V, $I_{OUT10} = 0.3\text{A}$ | | | | 0.01 | | %/V |
| Power Supply Reject Ratio ($f = 10\text{kHz}$, $V_{OUT10}=3.3\text{V}$) | PSRR10 | | | 52 | | dB |
| Output noise (10Hz to 100kHz, $V_{OUT10}=3.3\text{V}$) | OUT _{NOISE} ₁₀ | | | 300 | | uVrms |
| Dropout voltage @ 300mA ($V_{OUT10}=2.8\text{V}$) | V _{DROP10} | | | 200 | | mV |
| Operating Quiescent Current, No load, $V_{DD}=3.8\text{V}$ | I _{Q10} | | | 28 | | uA |
| Rated output current | I _{MAX10} | | | 300 | | mA |

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| PARAMETERS | SYMBOL | CONDITION | MIN | TYP | MAX | UNIT |
|---|----------------------|-----------|-------|-------|-------|-------|
| Current Limit, $V_{OUT10} = V_{OUT10} \times 0.95$ | I_{CL10} | | 350 | 500 | | mA |
| Soft-start Time | t_{SS10} | | | 400 | | us |
| C _{OUT} Discharge Switch ON Resistance | R_{DIS10} | | | 400 | | Ohm |
| CH11: LD06 | | | | | | |
| Input supply voltage range | $V_{INPUT11}$ | | 2.7 | | 5.5 | V |
| V_{OUT} Output Voltage Adjustable Range, 5bit(step=100mv) | V_{OUT11} | | 0.8 | | 2.5 | V |
| V_{OUT} Output Voltage, Default($T_j=25^{\circ}C$) | $V_{OUT11(Default)}$ | | 1.176 | 1.200 | 1.224 | V |
| V_{OUT} Output Voltage, Default($T_j=-10\sim85^{\circ}C$) | $V_{OUT11(Default)}$ | | 1.164 | 1.200 | 1.236 | V |
| Power Good threshold (Vout rising) | V_{PG11} | | | 93 | | % |
| Output under voltage lockout (Vout falling) | V_{UV11} | | | 85 | | % |
| V_{OUT} Load Regulation, $I_{OUT} = 1mA$ to 150mA | | | | 0.005 | | %/mA |
| V_{OUT} Line Regulation, $V_{IN11} = 3$ to 5V, $I_{OUT11} = 0.1A$ | | | | 0.015 | | %/V |
| Power Supply Reject Ratio (f = 10kHz, $V_{OUT11}=3.3V$) | PSRR11 | | | 70 | | dB |
| Output noise (10Hz to 100kHz, $V_{OUT11}=3.3V$) | $OUT_{NOISE11}$ | | | 30 | | uVRms |
| Dropout voltage @ 150mA ($V_{OUT11}=2.5V$) | V_{DROP11} | | | 200 | | mV |
| Operating Quiescent Current, No load, $V_{DD}=3.8V$ | I_{Q11} | | | 52 | | uA |
| Rated output current | I_{MAX11} | | | 150 | | mA |
| Current Limit, $V_{OUT11} = V_{OUT11} \times 0.95$ | I_{CL11} | | 200 | 300 | | mA |
| Soft-start Time | t_{SS11} | | | 400 | | us |
| C _{OUT} Discharge Switch ON Resistance | R_{DIS11} | | | 400 | | Ohm |
| CH12: LD07 | | | | | | |
| Input supply voltage range | $V_{INPUT12}$ | | 2.7 | | 5.5 | V |
| V_{OUT} Output Voltage Adjustable Range, | V_{OUT12} | | 0.8 | | 2.5 | V |

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| PARAMETERS | SYMBOL | CONDITION | MIN | TYP | MAX | UNIT |
|--|------------------------------------|-----------|--------|-------|-------|-------|
| 5bit(step=100mv) | | | | | | |
| Vout Output Voltage, Default(Tj=25°C) | V _{OUT12(Default)} | | 1.764 | 1.800 | 1.836 | V |
| Vout Output Voltage, Default(Tj=-10~85°C) | V _{OUT12(Default)} | | -1.736 | 1.800 | 1.854 | V |
| Power Good threshold (Vout rising) | V _{PG12} | | | 93 | | % |
| Output under voltage lockout (Vout falling) | V _{UV12} | | | 85 | | % |
| Vout Load Regulation, I _{OUT} = 1mA to 300mA | | | | 0.005 | | %/mA |
| Vout Line Regulation, V _{IN12} = 3 to 5V, I _{OUT12} = 0.3A | | | | 0.015 | | %/V |
| Power Supply Reject Ratio (f = 10kHz, V _{OUT12} =3.3V) | PSRR12 | | | 65 | | dB |
| Output noise (10Hz to 100kHz, V _{OUT12} =3.3V) | OUT _{NOISE} ₁₂ | | | 50 | | uVrms |
| Dropout voltage @ 300mA (V _{OUT12} =2.5V) | V _{DROP12} | | | 200 | | mV |
| Operating Quiescent Current, No load, V _{DD} =3.8V | I _{Q12} | | | 48 | | uA |
| Rated output current | I _{MAX12} | | | 300 | | mA |
| Current Limit, V _{OUT12} = V _{OUT12} x 0.95 | I _{CL12} | | 400 | 400 | | mA |
| Soft-start Time | t _{SS12} | | | 400 | | us |
| C _{OUT} Discharge Switch ON Resistance | R _{DIS12} | | | 250 | | Ohm |
| CH13 : LD08 | | | | | | |
| Input supply voltage range | V _{INPUT13} | | 2.7 | | 5.5 | V |
| Vout Output Voltage Adjustable Range, 4bit(step=100mv) | V _{OUT13} | | 1.8 | | 3.4 | V |
| Vout Output Voltage, Default(Tj=25°C) | V _{OUT13(Default)} | | 3.234 | 3.300 | 3.366 | V |
| Vout Output Voltage, Default(Tj=-10~85°C) | V _{OUT13(Default)} | | 3.201 | 3.300 | 3.399 | V |
| Power Good threshold (Vout rising) | V _{PG13} | | | 93 | | % |
| Output under voltage lockout (Vout falling) | V _{UV13} | | | 85 | | % |
| Vout Load Regulation, I _{OUT} = 1mA | | | | 0.003 | | %/mA |

Power Management System

| PARAMETERS | SYMBOL | CONDITION | MIN | TYP | MAX | UNIT |
|---|----------------------|-----------|-------|-------|-------|-------|
| to 150mA | | | | | | |
| Vout Line Regulation, $V_{IN13} = 3$ to 5V, $I_{OUT6} = 0.15A$ | | | | 0.01 | | %/V |
| Power Supply Reject Ratio ($f = 10\text{kHz}$, $V_{OUT13}=3.3V$) | PSRR13 | | | 50 | | dB |
| Output noise (10Hz to 100kHz, $V_{OUT13}=3.3V$) | OUT_{NOISE}_{13} | | | 300 | | uVrms |
| Dropout voltage @ 300mA ($V_{OUT13}=2.8V$) | V_{DROP13} | | | 200 | | mV |
| Operating Quiescent Current, No load, $V_{DD}=3.8V$ | I_{Q13} | | | 30 | | uA |
| Rated output current | I_{MAX13} | | | 400 | | mA |
| Current Limit, $V_{OUT13} = V_{OUT13} \times 0.95$ | I_{CL13} | | 500 | 600 | | mA |
| Soft-start Time | t_{SS13} | | | 400 | | us |
| COUT Discharge Switch ON Resistance | R_{DIS13} | | | 400 | | Ohm |
| CH14 : LD09 | | | | | | |
| Input supply voltage range | $V_{INPUT14}$ | | 2.7 | | 5.5 | V |
| Vout Output Voltage Adjustable Range, 4bit(step=100mv) | V_{OUT14} | | 1.8 | | 3.4 | V |
| Vout Output Voltage, Default ($T_j=25^\circ C$) | $V_{OUT14(Default)}$ | | 3.234 | 3.300 | 3.366 | V |
| Vout Output Voltage, Default ($T_j=-10\sim 85^\circ C$) | $V_{OUT14(Default)}$ | | 3.201 | 3.300 | 3.399 | V |
| Power Good threshold (Vout rising) | V_{PG14} | | | 93 | | % |
| Output under voltage lockout (Vout falling) | V_{UV14} | | | 85 | | % |
| Vout Load Regulation, $I_{OUT} = 1\text{mA}$ to 150mA | | | | 0.003 | | %/mA |
| Vout Line Regulation, $V_{IN14} = 3$ to 5V, $I_{OUT14} = 0.15A$ | | | | 0.01 | | %/V |
| Power Supply Reject Ratio ($f = 10\text{kHz}$, $V_{OUT14}=3.3V$) | PSRR14 | | | 50 | | dB |
| Output noise (10Hz to 100kHz, $V_{OUT13}=3.3V$) | OUT_{NOISE}_{14} | | | 300 | | uVrms |
| Dropout voltage @ 300mA ($V_{OUT13}=2.8V$) | V_{DROP14} | | | 200 | | mV |
| Operating Quiescent Current, No | I_{Q14} | | | 30 | | uA |

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| PARAMETERS | SYMBOL | CONDITION | MIN | TYP | MAX | UNIT |
|---|----------------------|-------------------------|-----|-----|-----|------|
| load, V _{DD} =3.8V | | | | | | |
| Rated output current | I _{MAX14} | | | 300 | | mA |
| Current Limit, V _{OUT14} = V _{OUT14} x 0.95 | I _{CL14} | | 400 | 500 | | mA |
| Soft-start Time | t _{SS14} | | | 400 | | us |
| C _{OUT} Discharge Switch ON Resistance | R _{DIS14} | | | 400 | | Ohm |
| CH15 :SWITCH | | | | | | |
| Input supply voltage range | V _{INPUT15} | | 2.7 | | 5.5 | V |
| Rated output current | I _{MAX15} | | | 300 | | mA |
| On resistance(V _{GS} =3V) | | | | 150 | | mohm |
| Current Limit | I _{CL15} | | 400 | 500 | | mA |
| C _{OUT} Discharge Switch ON Resistance | R _{DIS15} | | | 400 | | Ohm |
| CH16: H_5V (HDMI_5V) | | | | | | |
| Input supply voltage range | V _{INPUT16} | | 4.7 | | 5.4 | V |
| Rated output current | I _{MAX16} | | | 80 | | mA |
| | | | | | | |
| CH17: OTG Switch | | | | | | |
| Input supply voltage range | V _{INPUT17} | | 4.7 | | 5.4 | V |
| Rated output current | I _{MAX17} | | | 800 | | mA |
| output current limit | I _{CL17} | 0.1A step, default=0.8A | 0.7 | | 1 | A |
| | | | | | | |
| Real Time Clock (RTC) | | | | | | |
| RTC Operating Voltage Range | V _{IN} | | 2.5 | | 5.5 | V |
| RTC Supply Current | I _Q | | | 5 | 10 | uA |
| CLK32OUT1 jitter (open drain) (always on) | | | | 100 | | ns |
| CLK32OUT1 duty cycle | | | 40 | | 60 | % |
| CLK32OUT2 jitter (open drain) | | | | 100 | | ns |
| CLK32OUT2 duty cycle | | | 40 | | 60 | % |
| I2C Interface (The 7-bits slave address is: 0011100) | | | | | | |
| SCL clock frequency | f _{SCL} | | | | 400 | kHz |
| SCL high time | t _{HIGH} | | 0.6 | | | us |
| SCL low time | t _{LOW} | | 1.3 | | | us |
| Data setup time | t _{SU,DAT} | | 0.1 | | | us |
| Data hold time | t _{HD,DAT1} | | 0.3 | | | us |
| Setup time for repeated start | t _{SU,STA} | | 0.6 | | | us |

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| PARAMETERS | SYMBOL | CONDITION | MIN | TYP | MAX | UNIT |
|--|---------------------|-----------|---------------------------|-----|-----|------|
| HOLD time for start/repeated start | t _{HD,STA} | | 0.6 | | | us |
| Bus free time between a stop and condition | t _{BUF} | | 1.3 | | | us |
| Rise time of SCL/SDA | t _r | | 20 + 0.1C _B | | 300 | ns |
| Fall width of SCL/SDA | t _f | | 20 + 0.1C _B | | 300 | ns |
| Pulse width of suppressed spike | t _{SP} | | 0 | | 50 | ns |
| Capacitive load for each of bus line | C _{B2} | | | | 400 | pF |

11 FUNCTION DESCRIPTION

11.1 POWER UP/POWER DOWN

The RK818 can be powered by either a battery, or an external power supply through the USB port. When the PMIC is powered by a battery only, pressing the PWRON key powers up the PMIC. All the power channels start up at the default output voltages with a preset power up sequence, which has 2mS intervals between the channels. When the power up process is done, the NRESPWRON turns to high logic level to inform the processor that all the power rails are up and stable. And now the processor can communicate with the PMIC to re-configure the output voltage of each power channel if needed.

To power down the PMIC, the processor needs to issue a “power down” signal through the I²C interface. Upon receiving the power down signal, the PMIC first saves all the information on the existing states, and then switches the NRESPWRON to low logic level. At this point, the power channels start to be turned off one after another with the power down sequence. If for any reason the processor fails to issue the power down signal, the PMIC can be powered off by “pressing and holding” the PWRON key.

In a case where a battery is the sole power supply and the PMIC is in off state, when an external power supply is plugged into the USB, the PMIC will first check to see if this is a valid power supply. If the power supply from the USB is valid, then the power channels are turned on and the battery is charged.

11.2 SWITCHING CHARGER

The RK818 has integrated a switch mode charger, which provides the functions like trickle current

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charging, constant current charging, constant voltage charging, charging termination, automatic recharging, battery temperature monitoring, charging timer and thermal feedback protection. The values of constant current and constant voltage charging can be set through I²C interface.

The input average current limit function allows as large as possible a charging current to be used without having to worry about the input current exceeding the maximum current allowed by the USB port. The input current limits can be configured through I²C interface. For example, when an USB port is used as the input, the input current limit can be configured to either 450mA, or 820mA, to meet the requirements of USB2.0 and USB3.0 respectively.

The charger also has a timer function which sets the maximum charging time for trickle, constant current and constant voltage charging, respectively. If the charging does not complete when a preset maximum charging time is reached, the charging is terminated.

The battery temperature can be monitored through the TS1 pin. A battery typically has a thermistor inside. The RK818 sinks a constant current into the thermistor and senses the voltage across the thermistor through an internal ADC. A safe charging temperature range is preset in the PMIC. The charging can proceed normally if the battery temperature falls within the preset range. If, however, the battery temperature goes either above the upper limit or below the lower limit of the preset range, the charging will pause until the battery temperature goes back in the preset range. If the value of the available thermistor is either too large or too small, a normal resistor can be connected in series or in parallel with the thermistor so that the sensed voltage fits the ADC's input range.

During Charging, Vsyst will be set to 3.6V when the battery voltage is below 3.6V. This design is to guarantee that when an external power supply is plugged into the USB port to charge the battery while the battery voltage is low, the Vsyst is already at 3.6V, which allows the PMIC to start up quickly without having to wait for the Vsyst ramping up.

11.3 POWER PATH MANAGEMENT

A power path management function is integrated in the RK818, which, together with the accurate input current limit function, can provide intelligent power path control. In a power path control process, the PMIC gives the outputs, or the system loads, the highest priority of using the input power. The battery is getting charged only if the input power is greater than the output power required by the system loads. The intelligent power path control function automatically reduces the charging current when the output power required by the loads increases. In an extreme case where the required output power is greater than the input power, the charging current will be cut off and the battery will join the input power supply to provide power to the load. This is how the intelligent power path control works: As the system power loading increases, the PMIC will draw more input current from the power supply to meet the output power requirement while keep the charging current unchanged. If the system power loading continues to increase to the point where the input current limit is reached, then

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the PMIC will lower the charging current so that enough power still goes to the load. If the system power loading further increases and due to the input current limit, the input power can not meet the output power requirement, then the battery will start to discharge to supply power to the load together with the USB power supply. If for some reason the USB is unplugged, the battery will automatically switched in to take over the USB power supply and provide full power to the load. The wide power path loop bandwidth allows all the above mentioned power path switching transient to be quick and seamless and therefore no overshoot and notch occur at the system and output voltages.

To minimize the loss from the voltage drop along the current path when the battery is charged or discharged, a 50mΩ MOSFET is integrated in the RK818 to serve as a control switch as well as the power switch of the switching mode battery charger.

11.4 THERMAL FOLDBACK

Generally speaking, the higher the operating junction temperature is, the shorter the chip's life time. Therefore, keeping the operating junction temperature as low as possible is one of the keys in reliability design. The RK818 provides a thermal feedback protection function for charging process. When the die temperature reaches a preset value, the PMIC will lower the charging current so as to keep the die temperature within an appropriate range. The life time of the PMIC equipped with this function can be reliably prolonged and no over-heat damage will occur.

11.5 BATTERY FUEL GAUGE

The RK818 provides an accurate battery fuel gauge. A 12-bit ADC is integrated in the RK818 to collect the information on the battery, such as battery voltage, charging/discharging status, battery temperature, etc. Using the proprietary algorithms and the information collected by the ADC, the battery fuel gauge can accurately calculate the battery capacity based on the charging/discharging characteristics of the battery preloaded in the system. The gauge then sends the battery capacity information to the processor through the I²C interface.

11.6 BUCK CONVERTERS

The RK818 provides four high current synchronous buck converters, which deliver up to 4A, 4A, 2.5A and 2.5A, respectively. An enhanced current mode architecture is used, which improves the transient response significantly. All output voltages can be adjusted dynamically during operation through DVS (Dynamic Voltage Scaling), which guarantees a linear and gradual voltage ramping up and down. A

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complete set of protection functions, such as short circuit protection, is implemented in the buck converters too.

The key parameters such as operating mode, output voltage, DVS change rate, and output current limit can be configured through the I²C interface.

11.7 BOOST CONVERTER

The synchronous boost converter has 2.5A current capability and is used to power the OTG and the HDMI5V. The OTG has a built-in current limiting switch, which can effectively protect the boost converter from being damaged if a short circuit occurs at the OTG port.

As the USB input port and the OTG output port share a same pin, when the USB port is being used as a power supply and charging the battery, the OTG switch is forbidden to be turned on. Only when there is no external power supply plugged into the USB port, can the OTG be turned on and serve as a power supply.

The key parameters such as operating mode, output voltage, and output current limit can be configured through the I²C interface.

11.8 LOW DROPOUT REGULATORS (LDOS)

The RK818 also integrates nine LDOs and one low R_{dson} switch, with four LDOs (Ch6, Ch7, Ch9 and Ch11) capable of providing up to 150mA and three LDOs (CH10, CH12 and CH14) providing maximum 300mA. The LDO on Ch8 is a low noise, high PSRR LDO which delivers up to 100mA current and the LDO on Ch14 has 400mA current capability. The parameters such as output voltage in the different operating modes can be adjusted through the I²C interface.

11.9 REAL TIME CLOCK (RTC)

The RK818 integrates a crystal oscillator buffer and a real time clock (RTC). The buffer works with an external 32.768kHz crystal oscillator. With the RTC function, the PMIC provides second/minute/hour/day/month/year information, alarm wake up as well as time calibration. The RK818 provides two channels of 32.768kHz clocks with open drain outputs, where one channel is constantly on and the other is enabled through I²C interface.

12 STATE MACHINE DESCRIPTION

12.1 STATE DIAGRAM

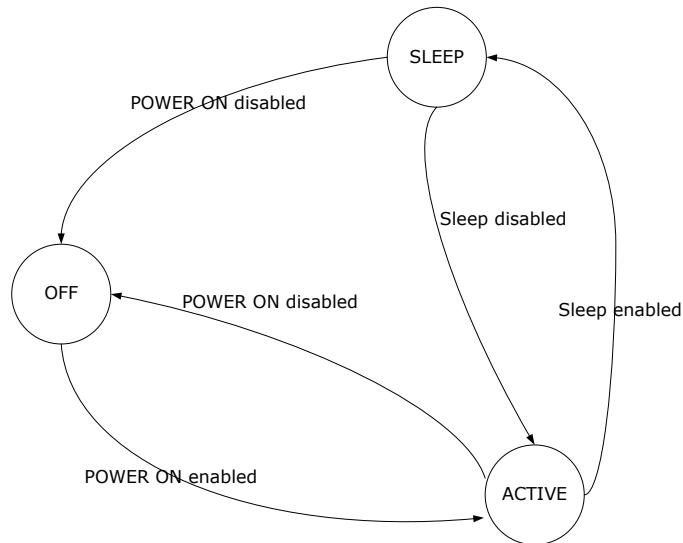


Figure 12-1 PMU State Diagram

OFF state: the PMIC is off. All channels are shut down.

ACTIVE state: the PMIC is on. All channels are on and operates as required by the system.

SLEEP state: the PMIC is in low power standby.

12.2 POWER ON ENABLE CONDITIONS

If none of the device power-on disable conditions is met, the following conditions are available to turn on and/or maintain the ON state of the device:

- PWRON signal is low for a period of time
- USB is plugged in. (PLUG_IN_INT goes to high level)
- RTC set time power on

12.3 POWER-ON DISABLE CONDITIONS

The PMIC will be powered off, or can not be powered on under the following conditions:

- PWRON signal keeps at low lever longer than the long-press delay $T_{DPWRONLP}$ and **PWRON_LP_ACT** is set to “0” (If it is set to “1”, the PMIC will restart automatically after the it is shut down) The interrupt corresponding to this condition is **PWRON_LP_INT** in the **INT_STS_REG** register.

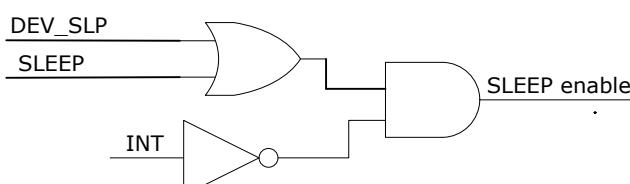
Power Management System

- The die temperature reaches the TSD threshold, in which case the TSD_STS bit in the register THERMAL_REG is set to “1”.
- Vsys is lower than UVLO threshold, in which case the VB_UV_STS bit in the register VB_MON_REG is set to “1”.
- Vsys is lower than the low voltage warning threshold which can be set with the VB_LO_SEL bit in the register VB_MON_REG, and the VB_LO_ACT bit is set to “0”.
- Vsys is higher than the over voltage protection threshold.
- The DEV_OFF control bit is set to “1”. (DEV_OFF is reset when the system is powered off).
- The temperature sensed at TS2 is either too high or too low. (To use TS2, a thermistor on a device to be monitored should be connected between TS2 and GND, and the ADC_TS2_EN bit in the register ADC_CTRL_REG must be set to “enable”. When the sensed voltage at TS2, which is saved in the register TS2_ADC_REG, is greater than the value in BAT_LTS_TS2_REG or smaller than the value in BAT_HTS_TS2_REG, the PMIC will be powered off.

12.4 SLEEP ENABLE CONDITIONS

- SLEEP signal is at high level
- Or DEV_SLP control bit is set to “1”.
- And interrupt flag inactive (INT high): No non-masked interrupt pending

The SLEEP state can be controlled by programming DEV_SLP and keeping the SLEEP state.



INT=1的条件：下面16种发生任意一种情况都会令INT=1
 1. VOUT_INT=1(if VOUT_INT_IM=0)
 2. VB_LO_INT=1(if VB_LO_INT_IM=0)
 3. PWRON_INT=1(if PWRON_INT_IM=0)
 4. PWRON_LP_INT=1(if PWRON_LP_INT_IM=0)
 5. HOTDIE_INT=1(if HOTDIE_INT_IM=0)
 6. RTC_ALARM_INT=1(if RTC_ALARM_INT_IM=0)
 7. RTC_PERIOD_INT=1(if RTC_PERIOD_INT_IM=0)
 8. USB_OV_INT=1(if USB_OV_INT_IM=0)
 9. PLUG_IN_INT=1(if PLUG_IN_INT_IM=0)
 10. PLUG_OUT_INT=1(if PLUG_OUT_INT_IM=0)
 11. CHGOK_INT=1(if CHGOK_INT_IM=0)
 12. CHGTE_INT=1(if CHGTE_INT_IM=0)
 13. CHGTS1_INT=1(if CHGTS1_INT_IM=0)
 14. TS2_INT=1(if TS2_INT_IM=0)
 15. CHG_CVTLIM_INT(if CHG_CVTLIM_INT_IM=0)
 16. DISCHG_ILIM_INT=1(if DISCHG_ILIM_INT_IM=0)

Figure 12-2 SLEEP enable control

13 POWER SEQUENCE

| AP | RK3188/RK3168/ RK3188M/RK3168M /RK3028A/RK3028 /RK2928 | | Partial Customized otp/ BUCK1~4, LD03/LD04/ LD05/LD07 | | RK3066 | | RK3288/RK3368 | | S-Product | | RK3399 | | |
|-------|---|-------------------|---|-------------------|--------------|-------------------|---------------|-------------------|--------------|-------------------|--------------|-------------------|---------|
| | 11 | | 10 | | 01 | | 00 | | RK818-1 | | RK818-2 | | RK818-3 |
| BOOT | Typical Vout | Power up Sequence | Typical Vout | Power up Sequence | Typical Vout | Power up Sequence | Typical Vout | Power up Sequence | Typical Vout | Power up Sequence | Typical Vout | Power up Sequence | |
| BUCK1 | 1.1V | 3 | OTP | OTP | 1.2V | 3 | 1.1V | 3 | 1.0V | 12 | 0.9V | 6 | |
| BUCK2 | 1.1V | 1 | OTP | OTP | 1.2V | 1 | 1.1V | 1 | 1.0V | 12 | 0.9V | 4 | |
| BUCK3 | x | 4 | x | OTP | x | 4 | x | 3 | x | 13 | x | 5 | |
| BUCK4 | 3.0V | 1 | OTP | OTP | 3.0V | 1 | 3.3V | 4 | 3.3V | 14 | 1.8V | 3 | |
| LDO1 | 3.3V | x | 3.3V | x | 3.3V | x | 3.3V | x | 1.8V | 11 | x | x | |

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| | | | | | | | | | | | | | |
|---------|------|---|------|-----|------|---|------|----|------|----|------|----|--|
| LDO2 | 3.0V | x | 3V | x | 3.0V | x | 3.0V | x | x | x | x | x | |
| LDO3 | 1.1V | 1 | OTP | OTP | 1.1V | 1 | 1.0V | 2 | 1.8V | 15 | x | x | |
| LDO4 | 2.5V | 2 | OTP | OTP | 2.5V | 2 | 2.5V | x | 1.8V | 1 | 3.3V | 1 | |
| LDO5 | 3V | 1 | OTP | OTP | 3.0V | 2 | 1.8V | 4 | 1.8V | 11 | 3.0V | 7 | |
| LDO6 | 1.2V | x | 1.2V | x | 1.1V | x | 1.1V | x | X | X | 1.5V | 2 | |
| LDO7 | 1.8V | 2 | OTP | OTP | 1.8V | 2 | 1.8V | 3 | 1.1V | 15 | x | x | |
| LDO8 | 1.8V | x | 1.8V | x | 1.8V | x | 1.8V | x | 3.0V | 14 | 3.3V | 8 | |
| LDO9 | 3.0V | 4 | 3.0V | 5 | 3.0V | 4 | 3.3V | 10 | 1.8V | 15 | 3.0V | 9 | |
| SWITCH | x | x | x | x | x | x | x | 10 | x | x | x | 10 | |
| OTG | 5V | x | 5V | x | 5V | x | 5V | x | 5V | x | x | x | |
| HDMI_5V | 5V | x | 5V | x | 5V | x | 5V | x | 5V | x | x | x | |

Table 4 Power up/down Sequence

13.1 BOOT1=1, BOOT0 = 1

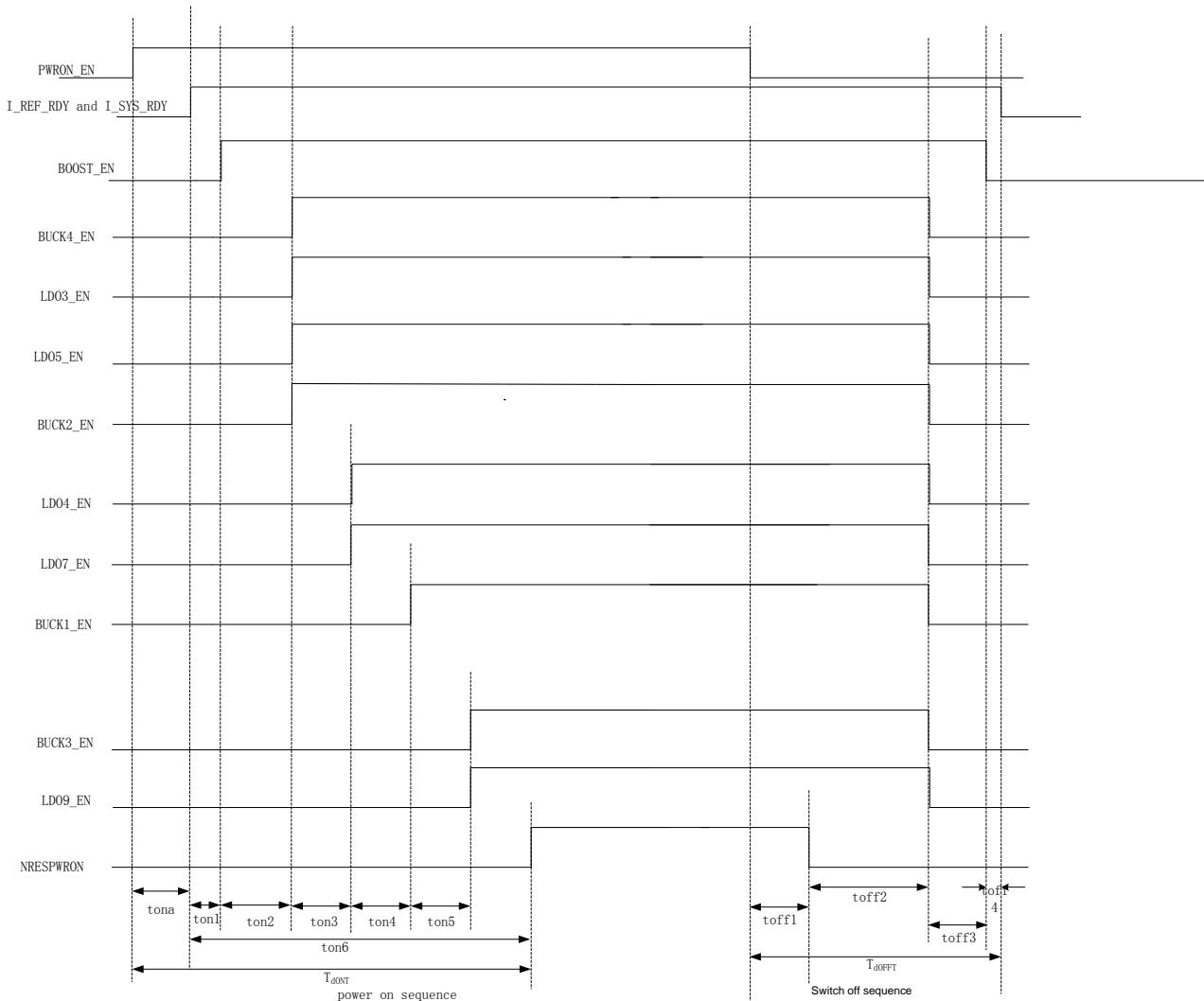


Figure 13-1 Power up/down sequence: BOOT1=1, BOOT0=1

Power Management System

13.2 BOOT1=0, BOOT0 = 1

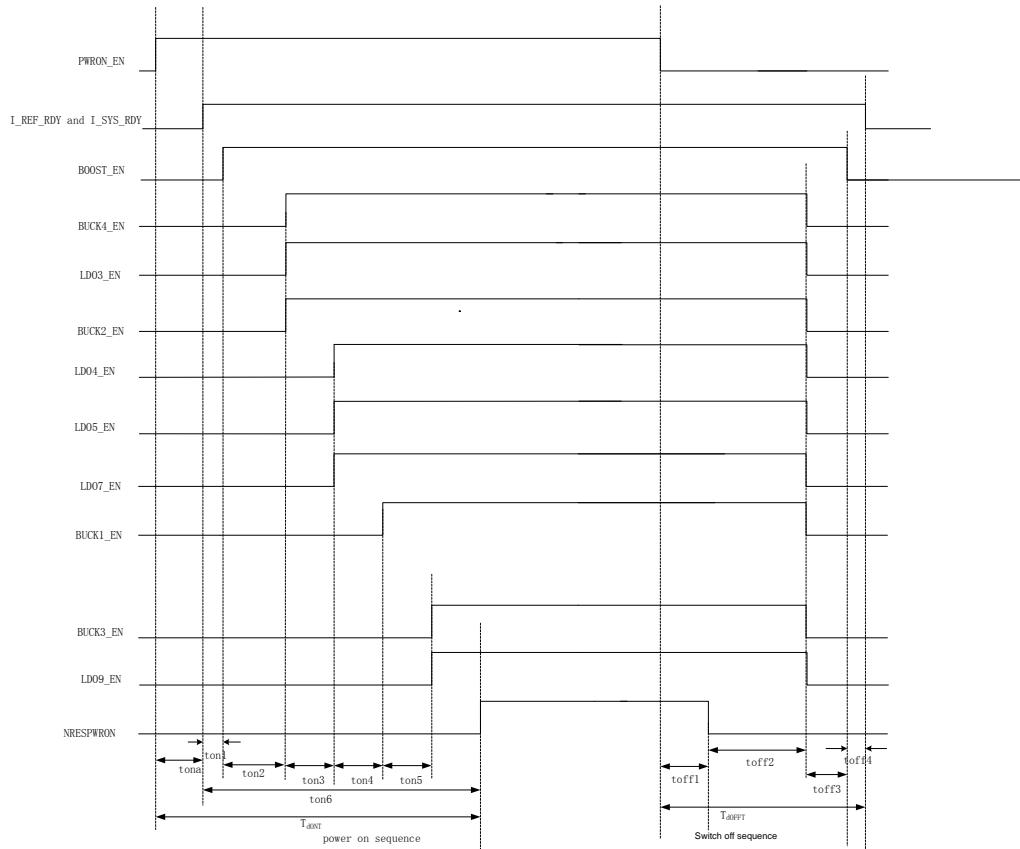


Figure 13-2 Power up/down sequence: BOOT1=0, BOOT0=1

13.3 BOOT1=1, BOOT0 = 0

In the “10” mode, 9 power channels are powered up, which are BUCK1- BUCK4, LDO3-LDO5 and LDO7. The power up sequence and the default output voltage of these 9 channels can be configured through OTP. The default output voltage of the BUCK3 can also be set by the external resistors. The default output voltage of the LDO9 is 3V, and the startup sequence of the LDO9 is 9th.

13.4 BOOT1=0, BOOT0 = 0

In the mode of “00”, 14 power channels are powered up, among which, the power up sequence and the default voltage of the BUCK1-4, LDO1-9 and the SWITCH can be configured through OTP. Again, The default output voltage of the BUCK3 can also be set by the external resistors. The voltage of the SWITCH is the same as the input supply.

13.5 BOOT TIMING CHARACTERISTIC

| PARAMETERS | DESCRIPTION | MIN | TYP | MAX | UNIT |
|------------|---|-----|-----------------------|-----|------|
| T_{ona} | power on enable to system ready and reference ready delay | | | | us |
| T_{on1} | Reference and system ready to boost enable delay | | $66 \times t_{CK32K}$ | | us |
| T_{on2} | Boost enable delay to 1st channel enable delay | | $66 \times t_{CK32K}$ | | us |
| T_{on3} | 1st channel enable to 2st channel enable delay | | $66 \times t_{CK32K}$ | | us |
| T_{on4} | 2nd channel enable to 3rd channel enable delay | | $66 \times t_{CK32K}$ | | us |
| T_{on5} | 3rd channel enable to 4th channel enable delay | | $66 \times t_{CK32K}$ | | us |
| T_{on6} | 1st channel enable to NRESPWRON rising edge delay | | 82 | | ms |
| t_{off1} | PWRON disable to NRESPWRON falling delay | | $1 \times t_{CK32K}$ | | us |
| T_{off2} | NRESPWRON falling delay to supplies disable delay | | 2 | | ms |
| T_{off3} | Other supplies disable to boost disable | | 2 | | ms |
| T_{off4} | Supplies disable to house-keeping disable delay | | $1 \times t_{CK32K}$ | | us |

Table 5 BOOT Timing Characteristics

14 POWER CONTROL TIMING

14.1 DEVICE TURN-ON WITH USB PLUG_IN

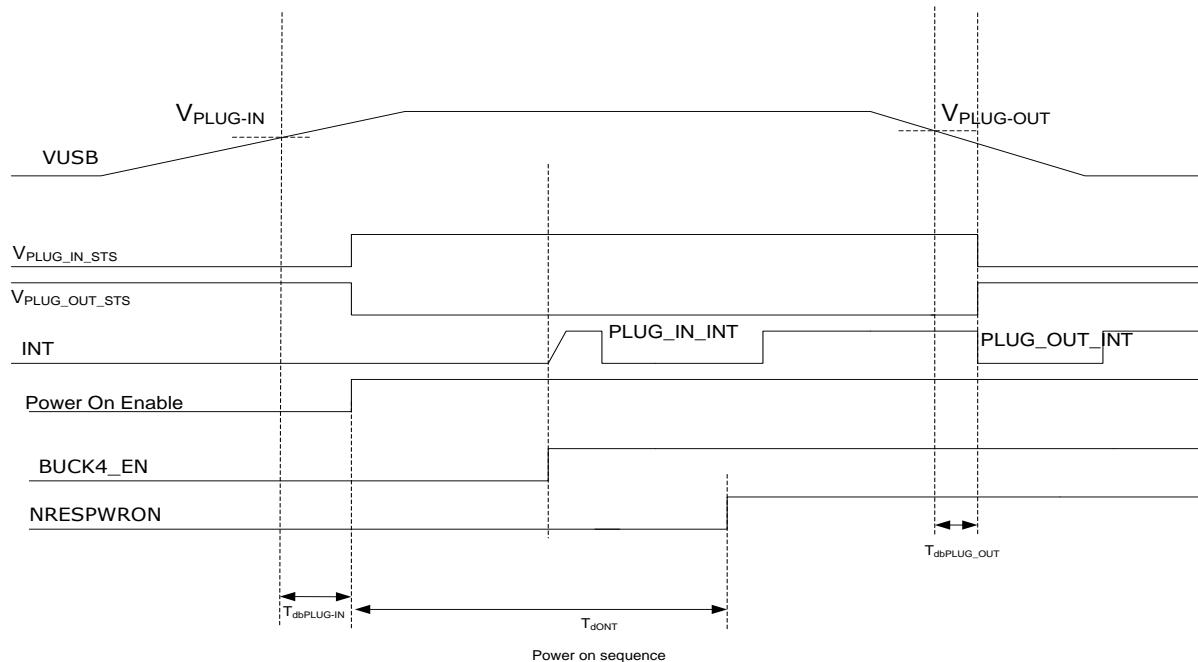


Figure 14-1 Turn on sequence when USB is plugged in (PLUP_IN_INT triggered power on enable)

14.2 POWER CONTROL TIMING WHEN POWERED BY BAT

$V_{bat} = V_{sys}$, as shown in the Figure 14-2

Power Management System

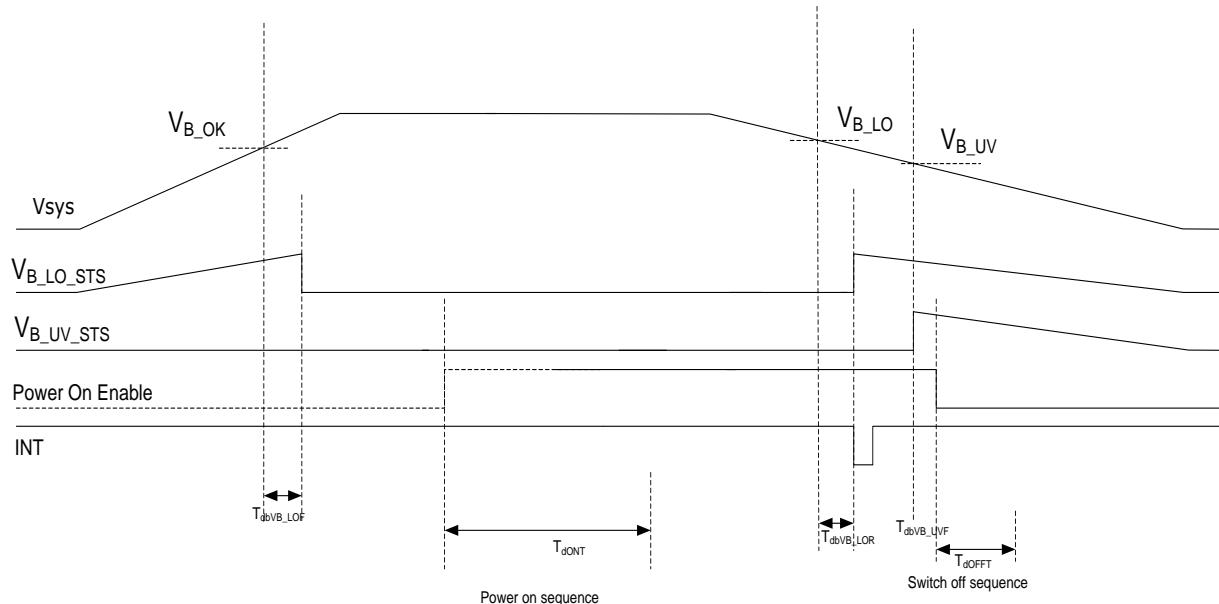


图 14-2 Power Control Timing with VIN Falling

14.3 TIMING CHARACTERISTICS (USB or Vsyst rising, falling and plug-in)

| Parameter | Description | Min | Typ | Max | Unit |
|-------------------|--------------------------------------|-----|-----|-----|------|
| T_{dbVB_LOF} | VB_LO falling-edge debouncing delay | | 2 | | ms |
| T_{dONT} | Total power on delay time(ton1~ton6) | | 62 | | ms |
| T_{dbVB_LOR} | VB_LO rising-edge debouncing delay | | 2 | | ms |
| T_{dVB_UVF} | VB_UV falling-edge debouncing delay | | 2 | | ms |
| T_{dOFFT} | Total power off delay time | | 2 | | ms |
| T_{dbPLUG_IN} | USB plug-in debouncing delay | | 100 | | ms |
| T_{dbPLUG_OUT} | USB plug-out debouncing delay | | 100 | | ms |

Table 6 Timing characteristics of USB and VSYS voltages

Power Management System

14.4 DEVICE STATE CONTROL THROUGH PWRON SIGNAL

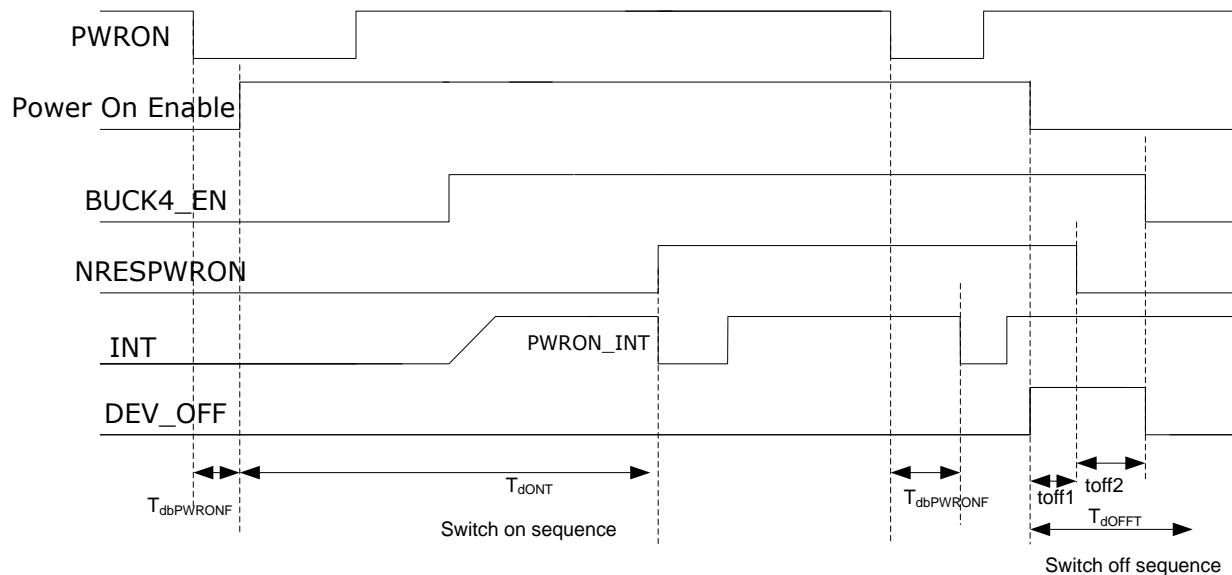


Figure 14-3 PWRON turn on/DEV_OFF turn off (DEV_OFF software power off signal comes before t_{off1})

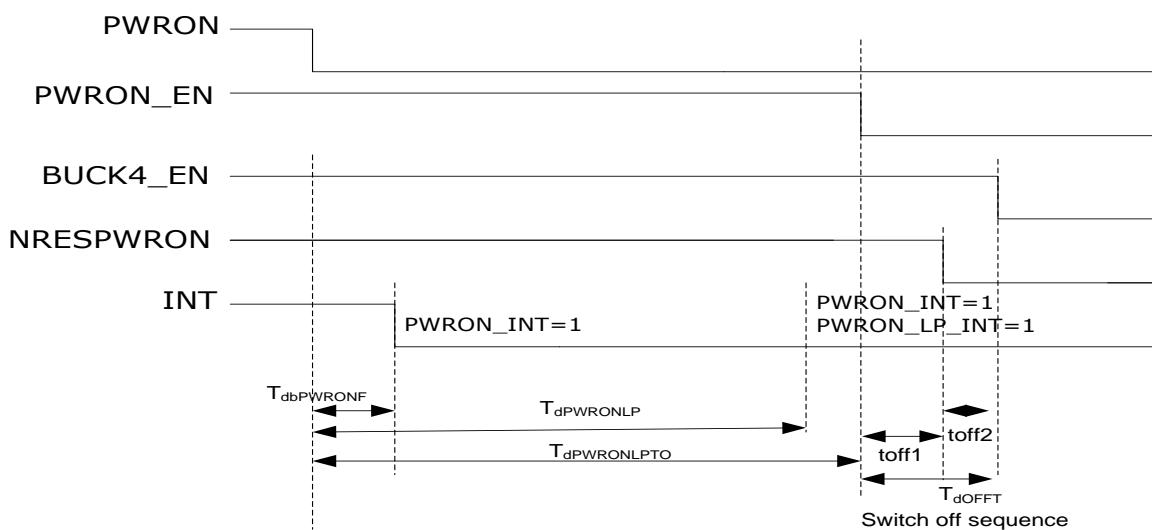


Figure 14-4 PWRON long press turn off (Register setting Reg4B<6>=0: Long press turning off
Reg4B<5:4>=0: Long press time set to 6S)

14.5 TIMING CHARACTERISTICS (PWRON, DEV_OFF)

| 参数 | 描述 | 最小 | 典型 | 最大 | 单位 |
|------------------|---|----|----------------------|----|----|
| $T_{dbPWRONF}$ | PWRON falling-edge debouncing delay | | 500 | | ms |
| T_{dONT} | Total power on delay time(ton1~ton6) | | 62 | | ms |
| $T_{dPWRONLP}$ | PWRON long press delay to interrupt (PWRON falling edge to PWRON_LP_INT=1) | | 4 | | s |
| $T_{dPWRONLPTO}$ | PWRON long press delay to turn off (PWRON falling edge to NRESPWRON falling edge) | | 6 | | s |
| toff1 | POWER ON disable to NRESPWRON falling delay | | $1 \times t_{CK32K}$ | | us |
| Toff2 | NRESPWRON falling delay to supplies disable delay | | 2 | | ms |
| T_{dOFFT} | total power off delay time | | 2 | | ms |

Table 7 PWRON/DEV_OFF timing characteristics

14.6 SLEEP STATE CONTROL

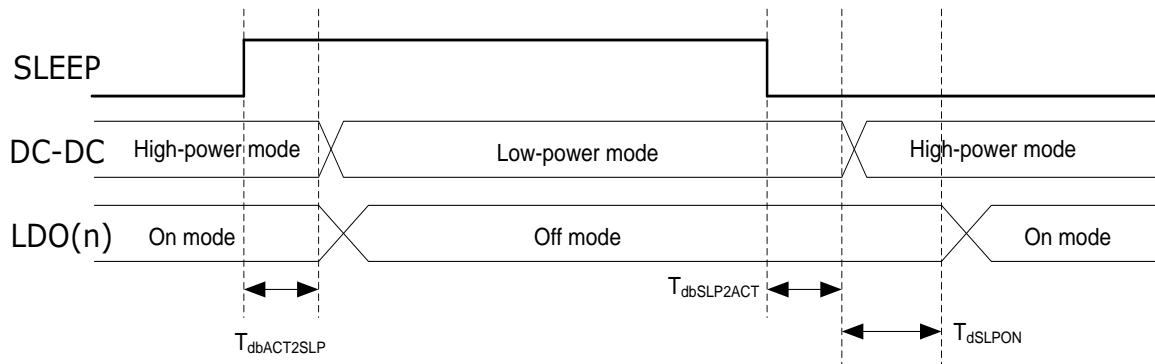


图 14-5 SLEEP/ACTIVE Transition Timing

14.7 TIMING CHARACTERISTICS (SLEEP)

| Parameter | Description | Min | Typ | Max | Unit |
|------------------------|--|-----|----------------------|-----|------|
| T _{dbACT2SLP} | SLEEP falling-edge debouncing delay | | 3xt _{ck32k} | | us |
| T _{dbSLP2ACT} | SLEEP rising-edge debouncing delay | | 3xt _{ck32k} | | us |
| T _{dSLPON} | Delay to turn on enable after SLEEP rising-edge debouncing | | 1xt _{ck32k} | | us |

Table 8 SLEEP Timing Characteristics

15 REGISTER DEFINITION

15.1 REGISTER MAP

| HEX ADDRESS | FUNCTION DESCRIPTION | R/W | DEFAULT/RESET |
|--------------------|----------------------|-----|---------------|
| RTC REGISTERS | | | |
| 00 | SECONDS REG | RW | 00 |
| 01 | MINUTES REG | RW | 50 |
| 02 | HOURS REG | RW | 08 |
| 03 | DAYS_REG | RW | 21 |
| 04 | MONTHS_REG | RW | 01 |
| 05 | YEARS_REG | RW | 13 |
| 06 | WEEKS_REG | RW | 01 |
| 08 | ALARM_SECONDS_REG | RW | 00 |
| 09 | ALARM_MINUTES_REG | RW | 00 |
| 0A | ALARM_HOURS_REG | RW | 00 |
| 0B | ALARM_DAYS_REG | RW | 01 |
| 0C | ALARM_MONTHS_REG | RW | 01 |
| 0D | ALARM_YEARS_REG | RW | 00 |
| 10 | RTC_CTRL_REG | RW | 00 |
| 11 | RTC_STATUS_REG | RW | 82 |
| 12 | RTC_INT_REG | RW | 00 |
| 13 | RTC_COMP_LSB_REG | RW | 00 |
| 14 | RTC_COMP_MSB_REG | RW | 00 |
| RESERVED REGISTERS | | | |
| 0E | RESERVED | RW | 00 |

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| | | | |
|---|--------------------|----|------|
| 0F | RESERVED | RW | 00 |
| 15 | RESERVED | RW | 00 |
| 16 | RESERVED | RW | 00 |
| 17 | RESERVED | RW | 00 |
| 18 | RESERVED | RW | 00 |
| MISC REGISTERS | | | |
| 20 | CLK32KOUT_REG | RW | 00 |
| 21 | VB_MON_REG | RW | 06 |
| 22 | THERMAL_REG | RW | 00 |
| POWER CHANNEL CONTROL/MONITOR REGISTERS | | | |
| 23 | DCDC_EN_REG | RW | boot |
| 24 | LDO_EN_REG | RW | boot |
| 25 | SLEEP_SET_OFF_REG1 | RW | 00 |
| 26 | SLEEP_SET_OFF_REG2 | RW | 00 |
| 27 | DCDC_UV_STS_REG | RO | 00 |
| 28 | DCDC_UV_ACT_REG | RW | 1F |
| 29 | LDO_UV_STS_REG | RO | 00 |
| 2A | LDO_UV_ACT_REG | RW | FF |
| 2B | DCDC_PG_REG | RO | 00 |
| 2C | LDO_PG_REG | RO | 00 |
| 2D | VOUT_MON_TDB_REG | RW | 02 |
| POWER CHANNEL CONFIGURATION REGISTERS | | | |
| 2E | BUCK1_CONFIG_REG | RW | 01 |
| 2F | BUCK1_ON_VSEL | RW | boot |
| 30 | BUCK1_SLP_VSEL | RW | 00 |
| 31 | BUCK1_DVS_VSEL | RW | 00 |
| 32 | BUCK2_CONFIG_REG | RW | 01 |
| 33 | BUCK2_ON_VSEL | RW | boot |
| 34 | BUCK2_SLP_VSEL | RW | 00 |
| 35 | BUCK2_DVS_VSEL | RW | 00 |
| 36 | BUCK3_CONFIG_REG | RW | 01 |
| 37 | BUCK4_CONFIG_REG | RW | 00 |
| 38 | BUCK4_ON_VSEL | RW | boot |
| 39 | BUCK4_SLP_VSEL_REG | RW | 00 |
| 3A | BOOST_CONFIG_REG | RW | 09 |
| 3B | LDO1_ON_VSEL_REG | RW | boot |
| 3C | LDO1_SLP_VSEL_REG | RW | 00 |
| 3D | LDO2_ON_VSEL_REG | RW | boot |
| 3E | LDO2_SLP_VSEL_REG | RW | 00 |

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| | | | |
|--|------------------------------|----|------|
| 3F | LDO3_ON_VSEL_REG | RW | boot |
| 40 | LDO3_SLP_VSEL_REG | RW | 00 |
| 41 | LDO4_ON_VSEL_REG | RW | boot |
| 42 | LDO4_SLP_VSEL_REG | RW | 00 |
| 43 | LDO5_ON_VSEL_REG | RW | boot |
| 44 | LDO5_SLP_VSEL_REG | RW | 00 |
| 45 | LDO6_ON_VSEL_REG | RW | boot |
| 46 | LDO6_SLP_VSEL_REG | RW | 00 |
| 47 | LDO7_ON_VSEL_REG | RW | boot |
| 48 | LDO7_SLP_VSEL_REG | RW | 00 |
| 49 | LDO8_ON_VSEL_REG | RW | boot |
| 4A | LDO8_SLP_VSEL_REG | RW | 00 |
| 4B | DEVCTRL_REG | RW | 00 |
| INTERRUPT REGISTERS | | | |
| 4C | INT_STS_REG1 | RW | 00 |
| 4D | INT_STS_MSK_REG1 | RW | 00 |
| 4E | INT_STS_REG2 | RW | 00 |
| 4F | INT_STS_MSK_REG2 | RW | 00 |
| 50 | IO_POL_REG | RW | 06 |
| BOOST/OTG/DCDC CURRENT LIMIT REGISTERS | | | |
| 52 | H5V_EN_REG | RW | 00 |
| 53 | SLEEP_SET_OFF_REG3 | RW | 00 |
| 54 | BOOST_LDO9_ON_VSEL_REG | RW | |
| 55 | BOOST_LDO9_SLP_VSEL_REG | RW | 60 |
| 56 | BOOST_CTRL_REG | RW | 00 |
| 90 | DCDC_ILMAX | RW | 55 |
| CHARGING CONTROL REGISTERS | | | |
| 9A | CHRG_COMP_REG | RW | 00 |
| A0 | SUP_STS_REG | RW | 0C |
| A1 | USB_CTRL_REG | RW | |
| A3 | CHRG_CTRL_REG1 | RW | B5 |
| A4 | CHRG_CTRL_REG2 | RW | 4A |
| A5 | CHRG_CTRL_REG3 | RW | 02 |
| A6 | OTG_ILIM_REG BAT_CTRL_REG | RW | 8C |
| A8 | BAT_HTS_TS1_REG | RW | 00 |
| A9 | BAT_LTS_TS1_REG | RW | FF |
| AA | BAT_HTS_TS2_REG | RW | 00 |

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| | | | |
|-----------------------------|------------------------|----|----|
| AB | BAT_LTS_TS2_REG | RW | FF |
| AC | TS_CTRL_REG | RW | 8F |
| AD | ADC_CTRL_REG | RW | 00 |
| AE | ON_SOURCE | RO | 00 |
| AF | OFF_SOURCE | RO | 00 |
| BATTERY FUEL GAUSE REGISTER | | | |
| B0 | GGCON | RW | 4A |
| B1 | GGSTS | RW | 40 |
| B2 | FRAME_SMP_INTERV_REG | RW | 01 |
| B3 | AUTO_SLP_CUR_THR_REG | RW | 40 |
| B4 | GASCNT_CAL_REG3 | RW | 00 |
| B5 | GASCNT_CAL_REG2 | RW | 00 |
| B6 | GASCNT_CAL_REG1 | RW | 00 |
| B7 | GASCNT_CAL_REG0 | RW | 00 |
| B8 | GASCNT3 | R | 00 |
| B9 | GASCNT2 | R | 00 |
| BA | GASCNT1 | R | 00 |
| BB | GASCNT0 | R | 00 |
| BC | BAT_CUR_AVG_REGH | R | 00 |
| BD | BAT_CUR_AVG_REGL | R | 00 |
| BE | TS1_ADC_REGH | R | 00 |
| BF | TS1_ADC_REGL | R | 00 |
| C0 | TS2_ADC_REGH | R | 00 |
| C1 | TS2_ADC_REGL | R | 00 |
| C2 | BAT_OCV_REGH | R | 00 |
| C3 | BAT_OCV_REGL | R | 00 |
| C4 | BAT_VOL_REGH | R | 00 |
| C5 | BAT_VOL_REGL | R | 00 |
| C6 | RELAX_ENTRY_THRES_REGH | RW | 00 |
| C7 | RELAX_ENTRY_THRES_REGL | RW | 60 |
| C8 | RELAX_EXIT_THRES_REGH | RW | 00 |
| C9 | RELAX_EXIT_THRES_REGL | RW | 60 |
| CA | RELAX_VOL1_REGH | R | 00 |
| CB | RELAX_VOL1_REGL | R | 00 |
| CC | RELAX_VOL2_REGH | R | 00 |
| CD | RELAX_VOL2_REGL | R | 00 |

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| | | | |
|-----------------------|------------------------|----|----|
| CE | BAT_CUR_R_CALC_REGH | R | 00 |
| CF | BAT_CUR_R_CALC_REGL | R | 00 |
| D0 | BAT_VOL_R_CALC_REGH | R | 00 |
| D1 | BAT_VOL_R_CALC_REGL | R | 00 |
| D2 | CAL_OFFSET_REGH | RW | 7F |
| D3 | CAL_OFFSET_REGL | RW | FF |
| D4 | NON_ACT_TIMER_CNT_REGL | R | 00 |
| D5 | VCALIB0_REGH | R | 00 |
| D6 | VCALIB0_REGL | R | 00 |
| D7 | VCALIB1_REGH | R | 00 |
| D8 | VCALIB1_REGL | R | 00 |
| DD | IOFFSET_REGH | R | 00 |
| DE | IOFFSET_REGL | R | 00 |
| DATA REGISTERS | | | |
| DF | DATA0 | RW | 00 |
| E0 | DATA1 | RW | 00 |
| E1 | DATA2 | RW | 00 |
| E2 | DATA3 | RW | 00 |
| E3 | DATA4 | RW | 00 |
| E4 | DATA5 | RW | 00 |
| E5 | DATA6 | RW | 00 |
| E6 | DATA7 | RW | 00 |
| E7 | DATA8 | RW | 00 |
| E8 | DATA9 | RW | 00 |
| E9 | DATA10 | RW | 00 |
| EA | DATA11 | RW | 00 |
| EB | DATA12 | RW | 00 |
| EC | DATA13 | RW | 00 |
| ED | DATA14 | RW | 00 |
| EE | DATA15 | RW | 00 |
| EF | DATA16 | RW | 00 |
| F0 | DATA17 | RW | 00 |
| F1 | DATA18 | RW | 00 |
| F2 | DATA19 | RW | 00 |

NOTE: Addresses of 60h through 9Fh (except for 9Ah) are for OTP. F3h through FFh are for OTP registers, read/write on these registers is forbidden.

Power Management System

15.2 REGISTER DESCRIPTION

15.2.1 RTC REGISTER

15.2.1.1 SECONDS_REG : RTC SECOND REGISTER

| ADDRESS: 00H | | | | TYPE: RW | | | | |
|--------------|------|------|------|----------|------|------|------|------|
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | RESV | SEC1 | | | SECO | | | |
| DEFAULT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

DESCRIPTION

- Bit 7 Reserved
 Bit 6-4 Set the second digit of the RTC seconds (0-5)
 Bit 3-0 Set the first digit of the RTC seconds (0-9)
 Note BCD coding from 00 to 59

15.2.1.2 MINUTES_REG : RTC MINUTE REGISTER

| ADDRESS: 01H | | | | TYPE: RW | | | | |
|--------------|------|------|------|----------|------|------|------|------|
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | RESV | MIN1 | | | MIN0 | | | |
| DEFAULT | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 |

DESCRIPTION

- Bit 7 Reserved
 Bit 6-4 Set the second digit of the RTC minutes (0-5)
 Bit 3-0 Set the first digit of the RTC minutes (0-9)
 Note BCD coding from 00 to 59

15.2.1.1 HOURS_REG : RTC HOUR REGISTER

| ADDRESS: 02H | | | | TYPE: RW | | | | | |
|--------------|-------|------|-------|----------|------|-------|------|------|--|
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | |
| SYMBOL | PM/AM | RESV | HOUR1 | | | HOUR0 | | | |
| DEFAULT | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | |

DESCRIPTION

- Bit 7 Set PM or AM: Only used in PM-AM mode, 1: PM. 0:AM.

Power Management System

- Bit 6 Reserved
 Bit 5-4 Set the second digit of the RTC hours
 Bit 3-0 Set the first digit of the RTC hours
 Note HOUR1/0 BCD coding from 0 to 11/23

15.2.1.2 **DAYS_REG : RTC DAY REGISTER**

| ADDRESS: 03H | | | | TYPE: RW | | | | |
|--------------|------|------|------|----------|------|------|------|------|
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | RESV | RESV | DAY1 | | DAY0 | | | |
| DEFAULT | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 |

DESCRIPTION

- Bit 7-6 Reserved
 Bit 5-4 Set the second digit of the RTC days
 Bit 3-0 Set the first digit of the RTC days
 Note BCD coding from 0 to 28/29/30/31

15.2.1.3 **MONTHS_REG : RTC MONTH REGISTER**

| ADDRESS: 04H | | | | TYPE: RW | | | | |
|--------------|------|------|------|----------|--------|------|------|------|
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | RESV | RESV | RESV | MONTH1 | MONTH0 | | | |
| DEFAULT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

DESCRIPTION

- Bit 7-5 Reserved
 Bit 4 Set the second digit of the RTC months
 Bit 3-0 Set the first digit of the RTC months
 Note BCD coding from 01 to 12

15.2.1.4 **YEARS_REG : RTC YEAR REGISTER**

| ADDRESS: 05H | | | | TYPE: RW | | | | |
|--------------|-------|------|------|----------|-------|------|------|------|
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | YEAR1 | | | | YEAR0 | | | |
| DEFAULT | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 |

DESCRIPTION

Power Management System

- Bit 7-5 Set the second digit of the RTC years
 Bit 3-0 Set the first digit of the RTC years
 Note BCD coding from 00 to 99

15.2.1.5 WEEKS_REG : RTC WEEK REGISTER

| ADDRESS: 06H | | | | | TYPE: RW | | | | | | | | |
|--------------|------|------|------|------|----------|------|------|------|--|--|--|--|--|
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | | | | | |
| SYMBOL | RESV | RESV | RESV | RESV | RESV | WEEK | | | | | | | |
| DEFAULT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | | | | | |

DESCRIPTION

- Bit 7-3 Reserved
 Bit 3-0 Set the second digit of the RTC weeks
 Note BCD coding from 1 to 7

ALARM_SECONDS_REG : RTC ALARM SECOND REGISTER

| ADDRESS: 08H | | | | | TYPE: RW | | | | |
|--------------|------|------------|------|------|------------|------|------|------|--|
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | |
| SYMBOL | RESV | ALARM_SEC1 | | | ALARM_SECO | | | | |
| DEFAULT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |

DESCRIPTION

- Bit 7 Reserved
 Bit 6-4 Set the second digit of the RTC alarm seconds
 Bit 3-0 Set the first digit of the RTC alarm seconds
 Note BCD coding from 00 to 59

15.2.1.6 ALARM_MINUTES_REG : RTC ALARM MINUTE REGISTER

| ADDRESS: 09H | | | | | TYPE: RW | | | | |
|--------------|------|------------|------|------|------------|------|------|------|--|
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | |
| SYMBOL | RESV | ALARM_MIN1 | | | ALARM_MIN0 | | | | |
| DEFAULT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |

DESCRIPTION

Power Management System

- | | |
|---------|---|
| Bit 7 | Reserved |
| Bit 6-4 | Set the second digit of the RTC alarm minutes |
| Bit 3-0 | Set the first digit of the RTC alarm minutes |
| Note | BCD coding from 00 to 59 |

15.2.1.7 **ALARM_HOURS_REG : RTC ALARM HOUR REGISTER**

| ADDRESS: 0AH | | | | TYPE: RW | | | | |
|--------------|-------------|------|-------------|----------|------|-------------|------|------|
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | ALARM_PM_AM | RESV | ALARM_HOUR1 | | | ALARM_HOUR0 | | |
| DEFAULT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

DESCRIPTION

- | | |
|---------|--|
| Bit 7 | Set PM) or AM: only used in PM-AM mode, 1: PM. 0:AM. |
| Bit 6 | Reserved |
| Bit 5-4 | Set the second digit of the RTC alarm hours |
| Bit 3-0 | Set the first digit of the RTC alarm hours |
| Note | HOUR1/0 BCD coding from 0 to 11/23 |

15.2.1.8 **ALARM_DAYS_REG : RTC ALAR DAY REGISTER**

| ADDRESS: 0BH | | | | TYPE: RW | | | | |
|--------------|------|------|------------|----------|------|------------|------|------|
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | RESV | RESV | ALARM_DAY1 | | | ALARM_DAY0 | | |
| DEFAULT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

DESCRIPTION

- | | |
|---------|--|
| Bit 7-6 | Reserved |
| Bit 5-4 | Set the second digit of the RTC alarm days |
| Bit 3-0 | Set the first digit of the RTC alarm days |
| Note | BCD coding from 0 to 28/29/30/31 |

15.2.1.9 **ALARM_MONTHS_REG : RTC ALARM MONTH REGISTER**

| ADDRESS: 0CH | | | | TYPE: RW | | | | |
|--------------|------|------|------|--------------|--------------|------|------|------|
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | RESV | RESV | RESV | ALARM_MONTH1 | ALARM_MONTH0 | | | |

Power Management System

| | | | | | | | | |
|---------|---|---|---|---|---|---|---|---|
| DEFAULT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
|---------|---|---|---|---|---|---|---|---|

DESCRIPTION

- Bit 7-5 Reserved
 Bit 4 Set the second digit of the RTC alarm months
 Bit 3-0 Set the first digit of the RTC alarm months
 Note BCD coding from 01 to 12

15.2.1.10 ALARM_YEARS_REG : RTC ALARM YEAR REGISTER

| ADDRESS: 0DH | | | | TYPE: RW | | | | |
|--------------|-------------|------|------|----------|------|-------------|------|------|
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | ALARM_YEAR1 | | | | | ALARM_YEAR0 | | |
| DEFAULT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

DESCRIPTION

- Bit 7-5 Set the second digit of the RTC alarm years
 Bit 3-0 Set the first digit of the RTC alarm years
 Note BCD coding from 00 to 99

15.2.1.11 RTC_CTRL_REG : RTC CONTROL REGISTER

| ADDRESS: 10H | | | | TYPE: RW | | | | |
|--------------|--------------|-------------|----------------|-----------|-----------|-----------|----------------------|----------|
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | RTC_READ_SEL | GET_TIME_ME | SET_32_COUNTER | TEST_MODE | AMPM_MODE | AUTO_COMP | ROUND_30S_(Auto Clr) | STOP_RTC |
| DEFAULT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

DESCRIPTION

- Bit 7 RTC_READ_SEL: 0: Read access directly to dynamic registers.
 1: Read access to static shadowed registers.
 Bit 6 GET_TIME: Rising transition of this register transfers dynamic registers into static shadowed registers..
 Bit 5 SET_32_COUNTER: 1: Set the 32Khz counter with COMP_REG value. It must only be used when the RTC is frozen.
 Bit 4 TEST_MODE: 1: Test mode (Auto compensation is enabled when the 32kHz counter reaches at its end)
 Bit 3 AMPM_MODE: 0: 24 hours mode.
 1: 12 hours mode (PM-AM mode)

Power Management System

- | | | |
|-------|------------|---|
| Bit 2 | AUTO_COMP: | 0: No auto compensation RW0. 1: Auto compensation enabled |
| Bit 1 | ROUND_30S: | 1: When "1" is written, the time is rounded to the closest minute in the next second, and is self-cleared after rounding. |
| Bit 0 | STOP_RTC: | 0: RTC is running. 1: RTC is frozen. RTC_time can only be changed during RTC frozen. |

15.2.1.12 RTC_STATUS_REG : RTC STATUS REGISTER

| ADDRESS: 11H | | | | TYPE: RW | | | | |
|--------------|---------------------------|---------------------------|---------------------------|---------------------------|---------------------------|---------------------------|-------------|------|
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | POWER_UP (Write 1 Clr) | ALARM (Write 1 Clr) | EVENT_1D (Write 1 Clr) | EVENT_1H (Write 1 Clr) | EVENT_1M (Write 1 Clr) | EVENT_1S (Write 1 Clr) | RUN (RO) | RESV |
| DEFAULT | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

DESCRIPTION

- | | |
|-------|---|
| Bit 7 | POWER_UP: POWER_UP is set by a reset, is cleared by writing one in this bit. |
| Bit 6 | ALARM: Indicates that an alarm interrupt has been generated (bit clear by writing 1) The alarm interrupt keeps its low level, until the micro-controller writes 1 in the ALARM bit of the RTC_STATUS register. The timer interrupt is a low-level pulse (15 µs duration). |
| Bit 5 | EVENT_1D: One day has occurred |
| Bit 4 | EVENT_1H: One hour has occurred |
| Bit 3 | EVENT_1M: One minute has occurred |
| Bit 2 | EVENT_1S :One secondr has occurred |
| Bit 1 | RUN: 0: RTC is frozen. 1: RTC is running. This bit shows the real state of the RTC |
| Bit 0 | RESEVERED |

15.2.1.13 RTC_INT_REG : RTC INTERRUPT REGISTER

| ADDRESS: 12H | | | | TYPE: RW | | | | |
|--------------|------|------|------|------------|-----------|-----------|-------|------|
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | RESV | RESV | RESV | INT_SLEEP_ | INT_ALARM | INT_TIMER | EVERY | |

Power Management System

| | | | | MASK_EN | _EN | _EN | | |
|---------|---|---|---|---------|-----|-----|---|---|
| DEFAULT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

DESCRIPTION

- Bit 7-5 RESEVERED
- Bit 4 INT_SLEEP_MASK_EN:
1: Mask periodic interrupt while the device is in SLEEP mode
0: Normal mode, no interrupt masked.
- Bit 3 INT_ALARM_EN: Enable one interrupt when the alarm value is reached
1: Enable
0: Disable
- Bit 2 INT_TIMER_EN: Enable periodic interrupt
- Bit 1-0 EVERY: 00: every second 01: every minute 10: every hour 11: every day

15.2.1.14 RTC_COMP_LSB_REG : RTC COMPENSATION LSB REGISTER

| ADDRESS: 13H | | | | TYPE: RW | | | | |
|--------------|--------------|------|------|----------|------|------|------|------|
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | RTC_COMP_LSB | | | | | | | |
| DEFAULT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

DESCRIPTION

- Bit7-0 This register contains the number of 32-kHz periods to be added into the 32KHz counter every hour [LSB]

15.2.1.15 RTC_COMP_MSB_REG : RTC COMPENSATION MSB REGISTER

| ADDRESS: 14H | | | | TYPE: RW | | | | |
|--------------|--------------|------|------|----------|------|------|------|------|
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | RTC_COMP_MSB | | | | | | | |
| DEFAULT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

DESCRIPTION

- Bit7-0 This register contains the number of 32-kHz periods to be added into the 32KHz counter every hour [MSB]

Power Management System

15.2.2 MISC REGISTERS

15.2.2.1 CLK32KOUT_REG : RTC 32KHz CLOCK OUTPUT REGISTER

| ADDRESS: 20H | | | | TYPE: RW | | | | |
|--------------|----------|------|------|----------|------|--------------------|-------------------|------|
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | RESERVED | | | | | CLK32KO UT2_FUN | CLK32KO UT2_EN | |
| DEFAULT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

DESCRIPTION

- Bit 7-2 RESERVED
- Bit 1 CLK32KOUT2_FUN: CLK32KOUT2 pin functional definition
0: 32.768K clock output
1: Recovery function
- Bit 0 CLK32KOUT2_EN: If CLK32KOUT2_FUN=0, then
1: CLK32KOUT2 is enabled
0: CLK32KOUT2 is disabled

15.2.2.2 VB_MON_REG : BATTERY VOLTAGE MONITOR REGISTER

| ADDRESS: 21H | | | | TYPE: RW | | | | |
|--------------|------|---------------------|-------------------|-----------|-------------------|-----------|------|------|
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | RESV | PLUG_IN_STS (RO) | VB_UV_STS (RO) | VB_LO_ACT | VB_LO_STS (RO) | VB_LO_SEL | | |
| DEFAULT | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 |

DESCRIPTION

- Bit 7 RESERVED
- Bit 6 PLUG_IN_STS: charger plug-in event occurs(DC PIN voltage >3.8V)
0: no charger plug in
1: charger plused in
This bit is read only
- Bit 5 VB_UV_STS: Battery under voltage lockout status(shut down system if the bit=1)
This bit is read only

Power Management System

| | |
|---------|--|
| Bit 4 | VB_LO_ACT: VBAT low action 0: shut down system 1: insert interrupt |
| Bit 3 | VB_LO_STS: Battery low voltage status 0: VBAT>VB_LO_SEL 1: VBAT<VB_LO_SEL This bit is read only |
| Bit 2-0 | VB_LO_SEL: Battery low voltage threshold 000~111: 2.8V~3.5V, step=100mV |

15.2.2.3 THERMAL_REG : THERMAL CONTROL REGISTER

| ADDRESS: 22H | | | | TYPE: RW | | | | |
|--------------|------|------|------|--------------|-------------|------|--------------------|-----------------|
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | RESV | RESV | RESV | TSD_T EMP | HOTDIE_TEMP | | HOTDIE_STS (RO) | TSD_STS (RO) |
| DEFAULT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

DESCRIPTION

| | |
|---------|---|
| Bit 7-5 | Reserved |
| Bit 4 | TSD_TEMP: Thermal shutdown temperature threshold 0: 140°C; 1: 160°C |
| Bit 3-2 | HOTDIE_TEMP: Hot-die temperature threshold 00: 85°C; 01: 95°C; 10: 105°C; 11: 115°C; |
| Bit 1 | HOTDIE_STS: Hot-die warning This bit is read only bit. |
| Bit 0 | TSD-STS: Thermal shut down |

15.2.3 POWER CHANNEL CONTROL/MONITOR REGISTERS

15.2.3.1 DCDC_EN_REG : DC-DC CONVERTER ENABLE REGISTER

| ADDRESS: 23H | | | | TYPE: RW | | | | |
|--------------|------------|---------------|-------------|--------------|--------------|--------------|--------------|--------------|
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | OTG_E N | SWITC H_EN | LDO9_ EN | BOOST _EN | BUCK4 _EN | BUCK3 _EN | BUCK2 _EN | BUCK1 _EN |

Power Management System

| | |
|---------|------|
| DEFAULT | Boot |
|---------|------|

| DESCRIPTION | |
|-------------|--|
| Bit 7 | OTG_EN, OTG enable 1: Enable 0: Disable DEFAULT value is set by boot. |
| Bit 6 | SWITCH_EN: SWITCH enable 1: Enable 0: Disable DEFAULT 由 bootSet. |
| Bit 5 | LDO9_EN: LDO9 enable 1: Enable 0: Disable DEFAULT value is set by boot. |
| Bit 4 | BOOST_EN: BOOST enable 1: Enable 0: Disable The default value is set by boot. |
| Bit 3-0 | BUCK(n)_EN: BUCKn enable 1: Enable 0: Disable The default value is set by boot. |

15.2.3.2 LDO_EN_REG : LDO ENABLE REGISTER

| ADDRESS: 24H | | | | TYPE: RW | | | | |
|--------------|---------|---------|---------|----------|---------|---------|---------|---------|
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | LDO8_EN | LDO7_EN | LDO6_EN | LDO5_EN | LDO4_EN | LDO3_EN | LDO2_EN | LDO1_EN |
| DEFAULT | Boot | | | | | | | |

| DESCRIPTION | |
|-------------|---|
| Bit 7-0 | LDOn: LDO(n) enable 1: Enable 0: Disable The default value is set by boot. |

Power Management System

15.2.3.3 SLEEP_SET_OFF_REG1 : SLEEP SET OFF REGISTER #1

| ADDRESS: 25H | | | | TYPE: RW | | | | |
|--------------|-------------------------|----------------------------|----------------------|---------------------------|---------------------------|---------------------------|---------------------------|---------------------------|
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | OTG_S LP_SE T_OFF | SWITCH_ SLP_SET_ OFF | LDO9_SLP _SET_OFF | BOOST_S LP_SET_O FF | BUCK4_S LP_SET_O FF | BUCK3_S LP_SET_O FF | BUCK2_S LP_SET_O FF | BUCK1_ SLP_SE T_OFF |
| DEFAULT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

DESCRIPTION

- | | |
|-------|--|
| Bit 7 | 1: OTG is set off in sleep mode 0: No effect. |
| Bit 6 | 1: Switch is set off in sleep mode 0: No effect. |
| Bit 5 | 1: LDO9 is set off in sleep mode 0: No effect. |
| Bit 4 | 1: The boost converter is set off in sleep mode 0: No effect. |
| Bit 3 | 1: Buck4 is set off in sleep mode 0: No effect. |
| Bit 2 | 1: Buck3 is set off in sleep mode 0: No effect. |
| Bit 1 | 1: Buck2 is set off in sleep mode 0: No effect. |
| Bit 0 | 1: Buck1 is set off in sleep mode 0: No effect. |

15.2.3.4 SLEEP_SET_OFF_REG2 : SLEEP SET OFF REGISTER #2

| ADDRESS: 26H | | | | TYPE: RW | | | | |
|--------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | LDO8_S LP_SET_ | LDO7_S LP_SET_ | LDO6_S LP_SET_ | LDO5_S LP_SET_ | LDO4_S LP_SET_ | LDO3_S LP_SET_ | LDO2_S LP_SET_ | LDO1_S LP_SET_ |

Power Management System

| | | | | | | | | |
|---------|-----|-----|-----|-----|-----|-----|-----|-----|
| | OFF |
| DEFAULT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

DESCRIPTION

- | | |
|-------|---|
| Bit 7 | 1: LDO8 is set off in sleep mode 0: No effect. |
| Bit 6 | 1: LDO7 is set off in sleep mode 0: No effect. |
| Bit 5 | 1: LDO6 is set off in sleep mode 0: No effect. |
| Bit 4 | 1: LDO5 is set off in sleep mode 0: No effect. |
| Bit 3 | 1: LDO4 is set off in sleep mode 0: No effect. |
| Bit 2 | 1: LDO3 is set off in sleep mode 0: No effect. |
| Bit 1 | 1: LDO2 is set off in sleep mode 0: No effect. |
| Bit 0 | 1: LDO1 is set off in sleep mode 0: No effect. |

15.2.3.5 DCDC_UV_STS_REG : DC-DC UNDER VOLTAGE STATUS REGISTER

| ADDRESS: 27H | | | | TYPE: RO | | | | |
|--------------|-------------|-------------|-------------|--------------|--------------|--------------|--------------|--------------|
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | OTG_U_V_STS | H5V_U_V_STS | LDO9_UV_STS | BOOST_UV_STS | BUCK4_UV_STS | BUCK3_UV_STS | BUCK2_UV_STS | BUCK1_UV_STS |
| DEFAULT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

DESCRIPTION

- | | |
|-------|---|
| Bit 7 | OTG_UV_STS: OTG under voltage flag. 1: Output voltage drop below 85% of nominal voltage 0: Normal |
| Bit 6 | H5V_UV_STS: H5V under voltage flag. 1: Output voltage drop below 85% of nominal voltage 0: Normal |
| Bit 5 | LDO9_UV_STS: LDO9 under voltage flag. 1: Output voltage drop below 85% of nominal voltage |

Power Management System

| | |
|-------|--|
| | 0: Normal |
| Bit 4 | BOOST_UV_STS: BOOST under voltage flag. 1: Output voltage drop below 85% of nominal voltage |
| | 0: Normal |
| Bit 3 | BUCK4_UV_STS: BUCK4 under voltage flag. 1: Output voltage drop below 85% of nominal voltage |
| | 0: Normal |
| Bit 2 | BUCK3_UV_STS: BUCK3 under voltage flag. 1: Output voltage drop below 85% of nominal voltage |
| | 0: Normal |
| Bit 1 | BUCK2_UV_STS: BUCK2 under voltage flag. 1: Output voltage drop below 85% of nominal voltage |
| | 0: Normal |
| Bit 0 | BUCK1_UV_STS: BUCK1 under voltage flag. 1: Output voltage drop below 85% of nominal voltage |
| | 0: Normal |

15.2.3.6 DCDC_UV_ACT_REG : DC-DC UNDER VOLTAGE ACTION REGISTER

| ADDRESS: 28H | | | | TYPE: RW | | | | |
|--------------|-------------|-------------|-------------|--------------|--------------|--------------|--------------|--------------|
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | OTG_U_V_ACT | H5V_U_V_ACT | LDO9_UV_ACT | BOOST_UV_ACT | BUCK4_UV_ACT | BUCK3_UV_ACT | BUCK2_UV_ACT | BUCK1_UV_ACT |
| DEFAULT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

DESCRIPTION

| | |
|-------|---|
| Bit 7 | OTG_UV_ACT: OTG under voltage action. 1: Restart OTG 0: No effect |
| Bit 6 | H5V_UV_ACT: H5V under voltage action. 1: Restart H5V 0: No effect |
| Bit 5 | LDO9_UV_ACT: LDO9 under voltage action. 1: Restart LDO9 0: No effect |
| Bit 4 | BOOST_UV_ACT: BOOST under voltage action. 1: shut down converter(this shut down action will also reset the BOOST_EN bit) |

Power Management System

- to 0)
0: No effect
- Bit 3 BUCK4_UV_ACT: BUCK4 under voltage action.
1: Restart BUCK4
0: No effect
- Bit 2 BUCK3_UV_ACT: BUCK3 under voltage action.
1: Restart BUCK3
0: No effect
- Bit 1 BUCK2_UV_ACT: BUCK2 under voltage action.
1: Restart BUCK2
0: No effect
- Bit 0 BUCK1_UV_ACT: BUCK1 under voltage action.
1: Restart BUCK1
0: No effect

15.2.3.7 LDO_UV_STS_REG : LDO UNDER VOLTAGE S TATUS REGISTER

| ADDRESS: 29H | | | | TYPE: RO | | | | |
|--------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | LDO8_UV _STS | LDO7_UV _STS | LDO6_UV _STS | LDO5_UV _STS | LDO4_UV _STS | LDO3_U V_STS | LDO2_U V_STS | LDO1_U V_STS |
| DEFAULT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

DESCRIPTION

- Bit 7 LDO8_UV_STS: LDO8 under voltage flag.
1: Output voltage drop below 85% of nominal voltage
0: Normal
- Bit 6 LDO7_UV_STS: LDO7 under voltage flag.
1: Output voltage drop below 85% of nominal voltage
0: Normal
- Bit 5 LDO6_UV_STS: LDO6 under voltage flag.
1: Output voltage drop below 85% of nominal voltage
0: Normal
- Bit 4 LDO5_UV_STS: LDO5 under voltage flag.
1: Output voltage drop below 85% of nominal voltage
0: Normal
- Bit 3 LDO4_UV_STS: LDO4 under voltage flag.
1: Output voltage drop below 85% of nominal voltage
0: Normal
- Bit 2 LDO3_UV_STS: LDO3 under voltage flag.

Power Management System

- 1: Output voltage drop below 85% of nominal voltage
 0: Normal
- Bit 1 LDO2_UV_STS: LDO2 under voltage flag.
 1: Output voltage drop below 85% of nominal voltage
 0: Normal
- Bit 0 LDO1_UV_STS: LDO1 under voltage flag.
 1: Output voltage drop below 85% of nominal voltage
 0: Normal

15.2.3.8 LDO_UV_ACT_REG : LDO UNVER VOLTAGE ACTION REGISTER

| ADDRESS: 2AH | | | | TYPE: RW | | | | |
|--------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | LDO8_U V_ACT | LDO7_U V_ACT | LDO6_U V_ACT | LDO5_U V_ACT | LDO4_U V_ACT | LDO3_U V_ACT | LDO2_U V_ACT | LDO1_U V_ACT |
| DEFAULT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

DESCRIPTION

- Bit 7 LDO8_UV_ACT: LDO8 under voltage action
 1: Restart LDO8
 0: No effect
- Bit 6 LDO7_UV_ACT: LDO7 under voltage action
 1: Restart LDO7
 0: No effect
- Bit 5 LDO6_UV_ACT: LDO6 under voltage action
 1: Restart LDO6
 0: No effect
- Bit 4 LDO5_UV_ACT: LDO5 under voltage action
 1: Restart LDO5
 0: No effect
- Bit 3 LDO4_UV_ACT: LDO4 under voltage action
 1: Restart LDO4
 0: No effect
- Bit 2 LDO3_UV_ACT: LDO3 under voltage action
 1: Restart LDO3
 0: No effect
- Bit 1 LDO2_UV_ACT: LDO2 under voltage action
 1: Restart LDO2
 0: No effect
- Bit 0 LDO1_UV_ACT: LDO1 under voltage action

Power Management System

- 1: Restart LDO1
 0: No effect

15.2.3.9 DCDC_PG_REG : DC-DC POWER GOOD STATUS REGISTER

| ADDRESS: 2BH | | | | TYPE: RO | | | | |
|--------------|-------------|-------------|--------------|--------------|---------------|---------------|---------------|---------------|
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | OTG_PG_S_TS | H5V_P_G_STS | LDO9_P_G_STS | BOOST_PG_STS | BUCK4_P_G_STS | BUCK3_P_G_STS | BUCK2_P_G_STS | BUCK1_P_G_STS |
| DEFAULT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

DESCRIPTION

- Bit 7 OTG_PG_STS: OTG power good flag.
 1: Power good, Vout>90% of setting voltage
 0: Power not good, Vout<90% of setting voltage
- Bit 6 H5V_PG_STS: H5V power good flag.
 1: Power good, Vout>90% of setting voltage
 0: Power not good, Vout<90% of setting voltage
- Bit 5 LDO9_PG_STS: LDO9 power good flag.
 1: Power good, Vout>90% of setting voltage
 0: Power not good, Vout<90% of setting voltage
- Bit 4 BOOST_PG_STS: BOOST power good flag.
 1: Power good, Vout>90% of setting voltage
 0: Power not good, Vout<90% of setting voltage
- Bit 3 BUCK4_PG_STS : BUCK4 power good flag.
 1: Power good, Vout>90% of setting voltage
 0: Power not good, Vout<90% of setting voltage
- Bit 2 BUCK3_PG_STS : BUCK3 power good flag.
 1: Power good, Vout>90% of setting voltage
 0: Power not good, Vout<90% of setting voltage
- Bit 1 BUCK2_PG_STS : BUCK2 power good flag.
 1: Power good, Vout>90% of setting voltage
 0: Power not good, Vout<90% of setting voltage
- Bit 0 BUCK1_PG_STS : BUCK1 power good flag.
 1: Power good, Vout>90% of setting voltage
 0: Power not good, Vout<90% of setting voltage

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15.2.3.10 LDO_PG_REG : LDO POWER GOOD STATUS REGISTER

| ADDRESS: 2CH | | | | TYPE: RO | | | | |
|--------------|-------------|-------------|-------------|-------------|-------------|--------------|--------------|--------------|
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | LDO8_PG_STS | LDO7_PG_STS | LDO6_PG_STS | LDO5_PG_STS | LDO4_PG_STS | LDO3_P_G_STS | LDO2_P_G_STS | LDO1_P_G_STS |
| DEFAULT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

DESCRIPTION

- Bit 7 LDO8_PG_STS : LDO8 power good flag.
1: Power good, Vout>90% of setting voltage
0: Power not good, Vout<90% of setting voltage
- Bit 6 LDO7_PG_STS : LDO7 power good flag.
1: Power good, Vout>90% of setting voltage
0: Power not good, Vout<90% of setting voltage
- Bit 5 LDO6_PG_STS : LDO6 power good flag.
1: Power good, Vout>90% of setting voltage
0: Power not good, Vout<90% of setting voltage
- Bit 4 LDO5_PG_STS : LDO5 power good flag.
1: Power good, Vout>90% of setting voltage
0: Power not good, Vout<90% of setting voltage
- Bit 3 LDO4_PG_STS : LDO4 power good flag.
1: Power good, Vout>90% of setting voltage
0: Power not good, Vout<90% of setting voltage
- Bit 2 LDO3_PG_STS : LDO3 power good flag.
1: Power good, Vout>90% of setting voltage
0: Power not good, Vout<90% of setting voltage
- Bit 1 LDO2_PG_STS : LDO2 power good flag.
1: Power good, Vout>90% of setting voltage
0: Power not good, Vout<90% of setting voltage
- Bit 0 LDO1_PG_STS : LDO1 power good flag.
1: Power good, Vout>90% of setting voltage
0: Power not good, Vout<90% of setting voltage

15.2.3.11 VOUT_MON_TDB_REG : VOUT DEBOUNCE MONITOR REGISTER

| ADDRESS: 2DH | | | | TYPE: RW | | | | |
|--------------|------|------|------|----------|------|------|--------------|------|
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | RESV | RESV | RESV | RESV | RESV | RESV | VOUT_MON_TDB | |
| DEFAULT | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

DESCRIPTION

Bit 7-2 Reserved

Bit 1-0 VOUT_MON_TDB: Vout monitor debouncing time(UV_STS rising edge and PG_STS rising edge debounce time)

00: 62us

01: 124us(default)

10: 186us

11: 248us

15.2.4 POWER CHANNEL CONFIGURATION REGISTER
15.2.4.1 BUCK1_CONFIG_REG : BUCK1 CONFIGURATION REGISTER

| ADDRESS: 2EH | | | | TYPE: RW | | | | |
|--------------|------|-------------|------|------------|------|-------------|------|------|
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | RESV | BUCK1_PHASE | RESV | BUCK1_RATE | | BUCK1_ILMIN | | |
| DEFAULT | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 |

DESCRIPTION

Bit 7 Reserved

Bit 6 BUCK1_PHASE,

0: Normal,

1: Inverted

Bit 5 Reserved

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- Bit 4-3 BUCK1_RATE: Voltage change rate after DVS
 00: 2mv/us
 01: 3mv/us
 10: 4.5mv/us
 11: 6mv/us
- Bit 2-0 BUCK1_ILMIN:
 000: 50mA, 001: 100mA, 010: 150mA, 011: 200mA
 100: 250mA, 101: 300mA, 110: 350mA, 111: 400mA

15.2.4.2 **BUCK1_ON_VSEL : BUCK1 ACTIVE MODE REGISTER**

| ADDRESS: 2FH | | | | TYPE: RW | | | | |
|--------------|----------------|------|---------------|----------|------|------|------|------|
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | BUCK1_O_N_FPWM | RESV | BUCK1_ON_VSEL | | | | | |
| DEFAULT | 0 | 0 | Boot | | | | | |

DESCRIPTION

- Bit 7 BUCK1_ON_FPWM:
 1: Forced PWM mode in active mode.
 0: PWM/PFM auto change mode.(default)
- Bit 6 Reserved
- Bit 5-0 BUCK1_ON_VSEL: BUCK1 active mode voltage selection,
 0.7125V~1.5V ,step=12.5mV
 000 000: 0.7125V
 000 001: 0.725V

 111 111: 1.5V
 The default value is set by boot.

15.2.4.3 **BUCK1_SLP_VSEL : BUCK1 SLEEP MODE REGISTER**

| ADDRESS: 30H | | | | TYPE: RW | | | | |
|--------------|----------------|------|----------------|----------|------|------|------|------|
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | BUCK1_SLP_FPWM | RESV | BUCK1_SLP_VSEL | | | | | |
| DEFAULT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

DESCRIPTION

Power Management System

| | |
|---------|--|
| Bit 7 | BUCK1_SLP_FPWM: |
| | 1: Forced PWM mode in sleep mode. |
| | 0: PWM/PFM auto change mode.(default) |
| Bit 6 | Reserved |
| Bit 5-0 | BUCK1_SLP_VSEL: BUCK1 sleep mode voltage selection, 0.7125V~1.5V , step=12.5mV |
| | 000 000: 0.7125V |
| | 000 001: 0.725V |
| | |
| | 111 111: 1.5V |

15.2.4.4 **BUCK2_CONFIG_REG : BUCK2 CONFIGURATION REGISTER**

| ADDRESS: 32H | | | | TYPE: RW | | | | |
|--------------|------|-------------|------|------------|------|-------------|------|------|
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | RESV | BUCK2_PHASE | RESV | BUCK2_RATE | | BUCK2_ILMIN | | |
| DEFAULT | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 |

DESCRIPTION

| | |
|---------|--|
| Bit 7 | Reserved |
| Bit 6 | BUCK2_PHASE, |
| | 0: Normal, |
| | 1: Inverted |
| Bit 5 | Reserved |
| Bit 4-3 | BUCK2_RATE: Voltage change rate after DVS. |
| | 00: 2mv/us |
| | 01: 3mv/us |
| | 10: 4.5mv/us |
| | 11: 6mv/us |
| Bit 2-0 | BUCK2_ILMIN: |
| | 000: 50mA, 001: 100mA, 010: 150mA, 011: 200mA |
| | 100: 250mA, 101: 300mA, 110: 350mA, 111: 400mA |

15.2.4.5 **BUCK2_ON_VSEL : BUCK2 ACTIVE MODE REGISTER**

| ADDRESS: 33H | | | | TYPE: RW | | | | |
|--------------|------|------|------|----------|------|------|------|------|
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |

Power Management System

| | | | |
|---------|----------------|------|---------------|
| SYMBOL | BUCK2_O_N_FPWM | RESV | BUCK2_ON_VSEL |
| DEFAULT | 0 | 0 | Boot |

DESCRIPTION

- Bit 7 BUCK2_ON_FPWM
 1: Forced PWM mode in active mode.
 0: PWM/PFM auto change mode.(default)
- Bit 6 Reserved
- Bit 5-0 BUCK2_ON_VSEL: BUCK2 active mode voltage selection, 0.7125V~1.5V , step=12.5mV
 000 000: 0.7125V
 000 001: 0.725V

 111 111: 1.5V
 The default value is set by boot.

15.2.4.6 BUCK2_SLP_VSEL : BUCK2 SLEEP MODE REGISTER

| ADDRESS: 34H | | | | TYPE: RW | | | | |
|--------------|-----------------|------|----------------|----------|------|------|------|------|
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | BUCK2_S_LP_FPWM | RESV | BUCK2_SLP_VSEL | | | | | |
| DEFAULT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

DESCRIPTION

- Bit 7 BUCK2_SLP_FPWM:
 1: Forced PWM mode in sleep mode.
 0: PWM/PFM auto change mode.(default)
- Bit 6 Reserved
- Bit 5-0 BUCK2_SLP_VSEL: BUCK1 sleep mode voltage selection, 0.7125V~1.5V , step=12.5mV
 000 000: 0.7125V
 000 001: 0.725V

 111 111: 1.5V

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15.2.4.7 **BUCK3_CONFIG_REG** : BUCK3 CONFIGURATION REGISTER

| ADDRESS: 36H | | | | TYPE: RW | | | | |
|--------------|----------------|-------------|------|----------|------|-------------|------|------|
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | BUCK3_O_N_FPWM | BUCK3_PHASE | RESV | RESV | RESV | BUCK3_ILMIN | | |
| DEFAULT | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

DESCRIPTION

- Bit 7 BUCK3_ON_FPWM:
 1: Forced PWM mode in active mode.
 0: PWM/PFM auto change mode.(default)
- Bit 6 BUCK3_PHASE,
 0: Normal,
 1: Inverted
- Bit 5-3 Reserved
- Bit 2-0 BUCK3_ILMIN:
 000: 50mA, 001: 100mA, 010: 150mA, 011: 200mA
 100: 250mA, 101: 300mA, 110: 350mA, 111: 400mA

15.2.4.8 **BUCK4_CONFIG_REG** : BUCK4 CONFIGURATION REGISTER

| ADDRESS: 37H | | | | TYPE: RW | | | | |
|--------------|------|-------------|------|----------|------|-------------|------|------|
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | RESV | BUCK4_PHASE | RESV | RESV | RESV | BUCK4_ILMIN | | |
| DEFAULT | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

DESCRIPTION

- Bit 7 RESERVED

Power Management System

| | |
|---------|---|
| Bit 6 | BUCK4_PHASE, 0: Normal, 1: Inverted |
| Bit 2-0 | BUCK4_ILMIN: 000: 50mA, 001: 100mA, 010: 150mA, 011: 200mA 100: 250mA, 101: 300mA, 110: 350mA, 111: 400mA |

15.2.4.9 BUCK4_ON_VSEL : BUCK4 ACTIVE MODE REGISTER

| ADDRESS: 38H | | | | TYPE: RW | | | | | | |
|--------------|----------------|------|------|---------------|------|------|------|------|--|--|
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | | |
| SYMBOL | BUCK4_O_N_FPWM | RESV | RESV | BUCK4_ON_VSEL | | | | | | |
| DEFAULT | 0 | 0 | 0 | Boot | | | | | | |

DESCRIPTION

| | |
|---------|---|
| Bit 7 | BUCK4_ON_FPWM: 1: Forced PWM mode in active mode. 0: PWM/PFM auto change mode.(default) |
| Bit 6-4 | RESERVED |
| Bit 3-0 | BUCK4_ON_VSEL: BUCK4 active mode voltage selection, 1.8V~3.3V , step=100Mv 00000: 1.8V 00001: 1.9V 01110: 3.2V 01111: 3.3V 10000: 3.4V 10001: 3.5V 10010: 3.6V The default value is set by boot. |

15.2.4.10 BUCK4_SLP_VSEL : BUCK4 SLEEP MODE REGISTER

| ADDRESS: 39H | | | | TYPE: RW | | | | |
|--------------|------|------|------|----------|------|------|------|------|
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |

Power Management System

| | | | | | | | | |
|---------|-----------------|------|------|----------------|---|---|---|---|
| SYMBOL | BUCK4_S_LP_FPWM | RESV | RESV | BUCK4_SLP_VSEL | | | | |
| DEFAULT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

DESCRIPTION

- Bit 7 BUCK4_SLP_FPWM:
 1: Forced PWM mode in sleep mode.
 0: PWM/PFM auto change mode.(default)
- Bit 6-5 Reserved
- Bit 4-0 BUCK4_SLP_VSEL: BUCK4 sleep mode voltage selection, 1.8V~3.3V , step=100Mv
- 00000: 1.8V
 00001: 1.9V

 01110: 3.2V
 01111: 3.3V
 10000: 3.4V
 10001: 3.5V
 10010: 3.6V

15.2.4.11 **BOOST_CONFIG_REG** : BOOST CONFIGURATION REGISTER

| ADDRESS: 3AH | | | | TYPE: RW | | | | |
|--------------|------|-----------------|-------------|-------------|------|------|-------------|------|
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | RESV | BOOST_ANTI_RING | BOOST_PHASE | BOOST_ILMAX | | | BOOST_ILMIN | |
| DEFAULT | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 |

DESCRIPTION

- Bit 7 RESERVED
- Bit 6 BOOST_ANTI_RING: BOOST anti-ring enable
 0: Disable
 1: Enable
- Bit 5 BOOST_PHASE,
 0: Normal
 1: Inverted
- Bit 4-3 BOOST_ILMAX:
 00: 4A,

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01: 4.5A,

10: 5A,

11: 5.5A

Bit 2-0 BOOST_ILMIN:

000: 75mA, 001: 100mA, 010: 125mA, 011: 150mA

100: 175mA, 101: 200mA, 110: 225mA, 111: 250mA

15.2.4.12 LDO1_ON_VSEL_REG : LDO1 ACTIVE MODE VOLTAGE REGISTER

| ADDRESS: 3BH | | | | TYPE: RW | | | | |
|--------------|------|------|------|--------------|------|------|------|------|
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | RESV | RESV | RESV | LDO1_ON_VSEL | | | | |
| DEFAULT | 0 | 0 | 0 | Boot | | | | |

DESCRIPTION

Bit 7-5 RESERVED

Bit 4-0 LDO1_ON_VSEL: LDO1 active mode voltage selection, 1.8V~3.4V, step=0.1V

00000: 1.8V

00001: 1.9V

....

01110: 3.2V

01111: 3.3V

10000: 3.4V

The default value is set by boot.

15.2.4.13 LDO1_SLP_VSEL_REG : LDO1 SLEEP MODE VOLTAGE SELECT REGISTER

| ADDRESS: 3CH | | | | TYPE: RW | | | | |
|--------------|------|------|------|---------------|------|------|------|------|
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | RESV | RESV | RESV | LDO1_SLP_VSEL | | | | |
| DEFAULT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

DESCRIPTION

Bit 7-5 Reserved

Power Management System

| | | | | | | | | | |
|---------|--|--|--|--|--|--|--|--|--|
| Bit 4-0 | LDO1_SLP_VSEL: LDO1 SLEEP mode voltage selection. 1.8V~3.4V, step=0.1V | | | | | | | | |
| | 00000: 1.8V | | | | | | | | |
| | 00001: 1.9V | | | | | | | | |
| | | | | | | | | | |
| | 01110: 3.2V | | | | | | | | |
| | 01111: 3.3V | | | | | | | | |
| | 10000: 3.4V | | | | | | | | |

15.2.4.14 LDO2_ON_VSEL_REG : LDO2 ACTIVE MODE VOLTAGE SELECT REGISTER

| ADDRESS: 3DH | | | | TYPE: RW | | | | | |
|--------------|------|------|------|--------------|------|------|------|------|--|
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | |
| SYMBOL | RESV | RESV | RESV | LDO2_ON_VSEL | | | | | |
| DEFAULT | 0 | 0 | 0 | Boot | | | | | |

DESCRIPTION

| | | | | | | | | | |
|---------|--|--|--|--|--|--|--|--|--|
| Bit 7-5 | RESERVED | | | | | | | | |
| Bit 4-0 | LDO2_ON_VSEL: LDO2 active mode voltage selection. 1.8V~3.4V, step=0.1V | | | | | | | | |
| | 00000: 1.8V | | | | | | | | |
| | 00001: 1.9V | | | | | | | | |
| | | | | | | | | | |
| | 01110: 3.2V | | | | | | | | |
| | 01111: 3.3V | | | | | | | | |
| | 10000: 3.4V | | | | | | | | |
| | DEFAULT value is set by boot. | | | | | | | | |

15.2.4.15 LDO2_SLP_VSEL_REG : LDO2 SLEEP MODE VOLTAGE SELECT REGISTER

| ADDRESS: 3EH | | | | TYPE: RW | | | | | |
|--------------|------|------|------|---------------|------|------|------|------|--|
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | |
| SYMBOL | RESV | RESV | RESV | LDO2_SLP_VSEL | | | | | |
| DEFAULT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |

DESCRIPTION

| | | | | | | | | | |
|---------|---|--|--|--|--|--|--|--|--|
| Bit 7-5 | RESERVED | | | | | | | | |
| Bit 4-0 | LDO2_SLP_VSEL: LDO2 sleep mode voltage selection. | | | | | | | | |

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1.8V~3.4V, step=0.1V

00000: 1.8V

00001: 1.9V

....

01110: 3.2V

01111: 3.3V

10000: 3.4V

15.2.4.16 LDO3_ON_VSEL_REG : LDO3 ACTIVE MODE VOLTAGE SELECT REGISTER

| ADDRESS: 3FH | | | | TYPE: RW | | | | |
|--------------|------|------|------|----------|--------------|------|------|------|
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | RESV | RESV | RESV | RESV | LDO3_ON_VSEL | | | |
| DEFAULT | 0 | 0 | 0 | 0 | Boot | | | |

DESCRIPTION

Bit 7-4 RESERVED

Bit 4-3 LDO3_ON_VSEL: LDO3 active mode voltage selection.

0.8V~2.5V, step=0.1V

0000: 0.8V

0001: 0.9V

....

1100: 2.0V

1101: 2.2V

1111: 2.5V

DEFAULT value is set by boot.

15.2.4.17 LDO3_SLP_VSEL_REG : LDO3 SLEEP MODE VOLTAGE SELECT REGISTER

| ADDRESS: 40H | | | | TYPE: RW | | | | |
|--------------|------|------|------|----------|---------------|------|------|------|
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | RESV | RESV | RESV | RESV | LDO3_SLP_VSEL | | | |
| DEFAULT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

DESCRIPTION

Bit 7-4 RESERVED

Bit 3-0 LDO3_SLP_VSEL: LDO3 sleep mode voltage selection.

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0.8V~2.5V, step=0.1V

0000: 0.8V

0001: 0.9V

....

1100: 2.0V

1101: 2.2V

1111: 2.5V

DEFAULT value is set by boot.

15.2.4.18 LDO4_ON_VSEL_REG : LDO4 ACTIVE MODE VOLTAGE SELECT

| ADDRESS: 41H | | | | TYPE: RW | | | | |
|--------------|------|------|------|--------------|------|------|------|------|
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | RESV | RESV | RESV | LDO4_ON_VSEL | | | | |
| DEFAULT | 0 | 0 | 0 | Boot | | | | |

DESCRIPTION

Bit 7-5 RESERVED

Bit 4-0 LDO4_ON_VSEL: LDO4 active mode voltage selection.

1.8V~3.4V, step=0.1V

00000: 1.8V

00001: 1.9V

....

01110: 3.2V

01111: 3.3V

10000: 3.4V

DEFAULT value is set by boot.

15.2.4.19 LDO4_SLP_VSEL_REG : LDO4 SLEEP MODE VOLTAGE SELECT REGISTER

| ADDRESS: 42H | | | | TYPE: RW | | | | |
|--------------|------|------|------|---------------|------|------|------|------|
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | RESV | RESV | RESV | LDO4_SLP_VSEL | | | | |
| DEFAULT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

DESCRIPTION

Power Management System

| | |
|---------|--|
| Bit 7-5 | RESERVED |
| Bit 4-0 | LDO2_SLP_VSEL: LDO2 sleep mode voltage selection. 1.8V~3.4V, step=0.1V 00000: 1.8V 00001: 1.9V 01110: 3.2V 01111: 3.3V 10000: 3.4V |

15.2.4.20 **LDO5_ON_VSEL_REG : LDO5 ACTIVE MODE VOLTAGE SELECT REGISTER**

| ADDRESS: 43H | | | | TYPE: RW | | | | |
|--------------|------|------|------|--------------|------|------|------|------|
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | RESV | RESV | RESV | LDO5_ON_VSEL | | | | |
| DEFAULT | 0 | 0 | 0 | Boot | | | | |

DESCRIPTION

| | |
|---------|--|
| Bit 7-5 | RESERVED |
| Bit 4-0 | LDO5_ON_VSEL: LDO5 active mode voltage selection. 1.8V~3.4V, step=0.1V 00000: 1.8V 00001: 1.9V 01110: 3.2V 01111: 3.3V 10000: 3.4V |
| | DEFAULT is set by boot. |

15.2.4.21 **LDO5_SLP_VSEL_REG : LDO5 SLEEP MODE VOLTAGE SELECT REGISTER**

| ADDRESS: 44H | | | | TYPE: RW | | | | |
|--------------|------|------|------|---------------|------|------|------|------|
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | RESV | RESV | RESV | LDO5_SLP_VSEL | | | | |
| DEFAULT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Power Management System

DESCRIPTION

| | |
|---------|--|
| Bit 7-5 | RESERVED |
| Bit 4-0 | LDO5_SLP_VSEL: LDO5 sleep mode voltage selection. 1.8V~3.4V, step=0.1V 00000: 1.8V 00001: 1.9V 01110: 3.2V 01111: 3.3V 10000: 3.4V |

15.2.4.22 LDO6_ON_VSEL_REG : LDO6 ACTIVE MODE VOLTAGE SELECT REGISTER

| ADDRESS: 45H | | | | TYPE: RW | | | | |
|--------------|------|------|------|--------------|------|------|------|------|
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | RESV | RESV | RESV | LDO6_ON_VSEL | | | | |
| DEFAULT | 0 | 0 | 0 | Boot | | | | |

DESCRIPTION

| | |
|---------|---|
| Bit 7-5 | RESERVED |
| Bit 4-0 | LDO6_ON_VSEL: LDO6 active mode voltage selection. 0.8V~2.5V, step=0.1V 00000: 0.8V 00001: 0.9V 10000: 2.4V 10001: 2.5V DEFAULT is set by boot. |

15.2.4.23 LDO6_SLP_VSEL_REG : LDO6 SLEEP MODE VOLTAGE SELECT REGISTER

| ADDRESS: 46H | | | | TYPE: RW | | | | |
|--------------|------|------|------|---------------|------|------|------|------|
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | RESV | RESV | RESV | LDO6_SLP_VSEL | | | | |
| DEFAULT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Power Management System

DESCRIPTION

- Bit 7-5 RESERVED
- Bit 4-0 LDO6_SLP_VSEL: LDO6 sleep mode voltage selection.
0.8V~2.5V, step=0.1V
00000: 0.8V
00001: 0.9V
.....
10000: 2.4V
10001: 2.5V

15.2.4.24 LDO7_ON_VSEL_REG : LDO7 ACTIVE MODE VOLTAGE SELECT REGISTER

| ADDRESS: 47H | | | | TYPE: RW | | | | |
|--------------|------|------|------|--------------|------|------|------|------|
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | RESV | RESV | RESV | LDO7_ON_VSEL | | | | |
| DEFAULT | 0 | 0 | 0 | Boot | | | | |

DESCRIPTION

- Bit 7-5 RESERVED
- Bit 4-0 LDO7_ON_VSEL: LDO7 active mode voltage selection.
0.8V~2.5V, step=0.1V
00000: 0.8V
00001: 0.9V
.....
10000: 2.4V
10001: 2.5V
DEFAULT is set by boot.

15.2.4.25 LDO7_SLP_VSEL_REG : LDO7 SLEEP MODE VOLTAGE SELECT REGISTER

| ADDRESS: 48H | | | | TYPE: RW | | | | |
|--------------|------|------|------|---------------|------|------|------|------|
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | RESV | RESV | RESV | LDO7_SLP_VSEL | | | | |
| DEFAULT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Power Management System

DESCRIPTION

| | | | | | | | | |
|---------|--|--|--|--|--|--|--|--|
| Bit 7-5 | RESERVED | | | | | | | |
| Bit 4-0 | LDO7_SLP_VSEL: LDO7 sleep mode voltage selection. 0.8V~2.5V, step=0.1V 00000: 0.8V 00001: 0.9V 10000: 2.4V 10001: 2.5V | | | | | | | |

15.2.4.26 LDO8_ON_VSEL_REG : LDO8 ACTIVE MODE VOLTAGE SELECT REGISTER

| ADDRESS: 49H | | | | TYPE: RW | | | | |
|--------------|------|------|------|--------------|------|------|------|------|
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | RESV | RESV | RESV | LDO8_ON_VSEL | | | | |
| DEFAULT | 0 | 0 | 0 | Boot | | | | |

DESCRIPTION

| | | | | | | | | |
|---------|---|--|--|--|--|--|--|--|
| Bit 7-5 | RESERVED | | | | | | | |
| Bit 4-0 | LDO8_ON_VSEL: LDO8 active mode voltage selection. 1.8V~3.4V, step=0.1V 00000: 1.8V 00001: 1.9V 01110: 3.2V 01111: 3.3V 10000: 3.4V DEFAULT is set by boot. | | | | | | | |

15.2.4.27 LDO8_SLP_VSEL_REG : LDO8 SLEEP MODE VOLTAGE SELECT REGISTER

| ADDRESS: 4AH | | | | TYPE: RW | | | | |
|--------------|------|------|------|---------------|------|------|------|------|
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | RESV | RESV | RESV | LDO8_SLP_VSEL | | | | |
| DEFAULT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Power Management System

DESCRIPTION

| | | | | | | | | |
|---------|---|--|--|--|--|--|--|--|
| Bit 7-5 | RESERVED | | | | | | | |
| Bit 4-0 | LDO8_SLP_VSEL: LDO8 sleep mode voltage selection. 1.8V~3.4V, step=0.1V | | | | | | | |
| | 00000: 1.8V | | | | | | | |
| | 00001: 1.9V | | | | | | | |
| | | | | | | | | |
| | 01110: 3.2V | | | | | | | |
| | 01111: 3.3V | | | | | | | |
| | 10000: 3.4V | | | | | | | |

15.2.4.28 DEV_CTRL_REG : DEVICE CONTROL REGISTER

| ADDRESS: 4BH | | | | TYPE: RW | | | | |
|--------------|------|----------------------|-----------------------|----------|-----------------|------|-------------|-------------|
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | RESV | PWRO N_LP_ ACT | PWRON_LP_OFF_TI ME | | DEV_OFF _RST | RESV | DEV_SL P | DEV_O FF |
| DEFAULT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

DESCRIPTION

| | |
|---------|--|
| Bit 7 | RESERVED |
| Bit 6 | Long Press Action Selection 0: Power off 1: Power off and restart |
| Bit 5-4 | PWRON_LP_OFF_TIME: PWRON long press turn off time: 00: 6s 01: 8s 10: 10s 11: 12s |
| Bit 3 | DEV_OFF_RST: Write 1 will start an ACTIVE to OFF or SLEEP to OFF device state transition (switch-off event) and activate reset of the digital core. |
| Bit 2 | Reserved |
| Bit 1 | DEV_SLP: Write 1 allows SLEEP device state (if DEV_OFF = 0 and DEV_OFF_RST = 0). Write '0' will start a SLEEP to ACTIVE device state transition (wake-up event) (if DEV_OFF = 0 and DEV_OFF_RST = 0). This bit is cleared in OFF state. |
| Bit 0 | DEV_OFF: Write 1 will start an ACTIVE to OFF or SLEEP to OFF device state transition (switch-off event). This bit is cleared in OFF state. |

Power Management System

15.2.5 INTERRUPT REGISTER

15.2.5.1 INT_STS_REG1 : INTERRUPT STATUS REGISTER #1

| ADDRESS: 4CH | | | | TYPE: RW | | | | |
|--------------|---|------------------------------------|-----------------------------------|--------------------------------|----------------------------------|---------------------------------|-------------------------------|---------------------------------|
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | USB_OV_INT(Write 1 clr or RegA3<7> =0 clr) | RTC_PERIOD_INT (Write 1 clr) | RTC_ALARM_INT (Write 1 clr) | HOTDIE_INT (Write 1 clr) | PWRON_LP_INT (Write 1 clr) | PWRON_N_INT (Write 1 clr) | VB_LO_INT (Write 1 clr) | VOUT_LO_INT (Write 1 clr) |
| DEFAULT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

DESCRIPTION

- Bit 7 USB_OV_INT: USB over voltage event interrupt.
 Bit 6 RTC_PERIOD_INT: RTC period event interrupt.
 Bit 5 RTC_ALARM_INT: RTC alarm event interrupt.
 Bit 4 HOTDIE_INT: Hot die event interrupt status.
 Bit 3 PWRON_LP_INT: PWRON PIN long press event interrupt status.
 Bit 2 PWRON_INT: PWRON event interrupt status.
 Bit 1 VB_LO_INT: Battery under voltage alarm event interrupt status.
 Bit 0 VOUT_LO_INT: VOUT under voltage alarm event interrupt status
 Note: 1: Interrupt asserted, write "1" to clear
 0: No interrupt

15.2.5.2 INT_MSK_REG1 : INTERRUPT MASK REGISTER #1

| ADDRESS: 4DH | | | | TYPE: RW | | | | |
|--------------|---------------|---------------|--------------|-----------|-------------|------------|----------|------------|
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | USB_OV_INT_IM | RTC_PERIOD_IM | RTC_ALARM_IM | HOTDIE_IM | PWRON_LP_IM | PWRON_N_IM | VB_LO_IM | VOUT_LO_IM |
| DEFAULT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Power Management System

DESCRIPTION

| | |
|-------|---|
| Bit 7 | USB_OV_INT_IM: USB over voltage event interrupt mask. |
| Bit 6 | RTC_PERIOD_INT: RTC period event interrupt mask. |
| Bit 5 | RTC_ALARM_INT: RTC alarm event interrupt mask. |
| Bit 4 | HOTDIE_INT: Hot die event interrupt status mask. |
| Bit 3 | PWRON_LP_INT: PWRON PIN long press event interrupt status mask. |
| Bit 2 | PWRON_INT: PWRON event interrupt status mask. |
| Bit 1 | VB_LO_INT: Battery under voltage alarm event interrupt status mask. |
| Bit 0 | VOUT_LO_IM: Vout under voltage alarm event interrupt status mask |
| Note: | 1: Mask the specified interrupt 0: Do not mask the specified interrupt |

15.2.5.3 INT_STS_REG2 : INTERRUPT STATUS REGISTER#2

| ADDRESS: 4EH | | | | TYPE: RW | | | | |
|--------------|----------------------------------|--|---------------------------------|---|--|--|-----------------------------------|-----------------------------------|
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | DISCHG_ILIM_INT (Write 1 clr) | CHG_CVTLIM_IN T (Write 1 clr or RegA3<7>=0 clr) | TS2_IN T (Write 1 clr) | CHGTS1_INT (Write 1 clr or RegA3<7>=0 clr) | CHGTE_INT (Write 1 clr or RegA3<7>=0 clr) | CHGOK_INT (Write 1 clr or RegA3<7>=0 clr) | PLUG_OUT_IN T (Write 1 clr) | PLUG_IN_IN NT (Write 1 clr) |
| DEFAULT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

DESCRIPTION

| | |
|-------|---|
| Bit 7 | DISCHG_ILIM_INT: Discharging triggering current limit event interrupt. |
| Bit 6 | CHG_CVTLIM_INT: Charging triggering input voltage limit, or current limit, or temperature protection event interrupt. |
| Bit 5 | TS2_INT: TS2 value exceeding upper or lower limits event interrupt. |
| Bit 4 | CHGTS1_INT: TS1 value exceeding upper or lower limits event interrupt. |
| Bit 3 | CHGTE_INT: Charging overtime event interrupt. |
| Bit 2 | CHGOK_INT: Charging termination event interrupt |
| Bit 1 | PLUG_OUT_INT: charger plug out event interrupt(PLUG_IN_STS falling edge interrupt) |
| Bit 0 | PLUG_IN_INT: charger plug in event interrupt(PLUG_IN_STS rising edge interrupt) |
| Note: | Write "1" to clear. |

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15.2.5.4 **INT_STS_MSK_REG2** : **INTERRUPT MASK REGISTER#2**

| ADDRESS: 4FH | | | | TYPE: RW | | | | |
|--------------|--------------------|-------------------|------------|---------------|--------------|--------------|-----------------|----------------|
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | DISCHG_ILIM_INT_IM | CHG_CVTLIM_INT_IM | TS2_INT_IM | CHGTS1_INT_IM | CHGTE_INT_IM | CHGOK_INT_IM | PLUG_OUT_INT_IM | PLUG_IN_INT_IM |
| DEFAUL | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

DESCRIPTION

- Bit 7 DISCHG_ILIM_INT_IM: Discharging triggering current limit event interrupt mask
 1: Mask the interrupt
 0: Do not mask the interrupt
- Bit 6 CHG_CVTLIM_INT_IM: Charging triggering input voltage limit, or current limit, or temperature protection event interrupt mask.
 1: Mask the interrupt
 0: Do not mask the interrupt
- Bit 5 TS2_INT_IM: TS2 value exceeding upper or lower limits event interrupt mask
 1: Mask the interrupt
 0: Do not mask the interrupt
- Bit 4 CHGTS1_INT_IM: TS1 value exceeding upper or lower limits event interrupt mask.
 1: Mask the interrupt
 0: Do not mask the interrupt
 CHGTE_INT_IM: Charging overtime event interrupt mask
- Bit 3 1: Mask the interrupt
 0: Do not mask the interrupt
 CHGOK_INT_IM: Charging termination event interrupt mask.
- Bit 2 1: Mask the interrupt
 0: Do not mask the interrupt
- Bit 1 PLUG_OUT_INT_IM: Charger plug out event interrupt mask.
 1: Mask the interrupt
 0: Do not mask the interrupt
- Bit 0 PLUG_IN_INT_IM: Charger plug in event interrupt mask
 1: Mask the interrupt
 0: Do not mask the interrupt

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15.2.5.5 IO_POL_REG : IO POLARITY REGISTER

| ADDRESS: 50H | | | | TYPE: RW | | | | |
|--------------|------|------|------|----------|------|------|------|---------|
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | RESV | RESV | RESV | RESV | RESV | RESV | RESV | INT_POL |
| DEFAULT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

DESCRIPTION

- Bit 7-1 RESERVED
 Bit 0 INT_POL: INT pin polarity
 0: active low
 1: active high

15.2.6 BOOST/OTG/DCDC REGISTER

15.2.6.1 H5V_EN_REG:

| ADDRESS: 52H | | | | TYPE: RW | | | | |
|--------------|------|------|------|----------|------|------------|--------------|--------|
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | RESV | RESV | RESV | RESV | RESV | BST_UHV_ST | REF_RDY_CTRL | H5V_EN |
| DEFAULT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

DESCRIPTION

- Bit 7-3 RESERVED
 Bit 2 BST_UHV_ST: Boost over load enable
 0: Enable
 1: Disable
 Bit 1 REF_RDY_CTRL: ref_rdy control
 0: After PMIC is powered up, if vref is lower than a preset value, then ref_rdy can be switched to logic low level.
 1: After PMIC is powered up, if vref is lower than a preset value, then RED_rdy must be kept at logic high level.
 Bit 0 H5V_EN: HDMI 5V enable control
 1: Enable
 0: Disable

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15.2.6.2 **SLEEP_SEL_OFF_REG3:**

| ADDRESS: 53H | | | | TYPE: RW | | | | |
|--------------|------|------|------|----------|------|------|------|-----------------|
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | RESV | RESV | RESV | RESV | RESV | RESV | RESV | H5V_SLP_SET_OFF |
| DEFAULT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

DESCRIPTION

- Bit 7-1 RESERVED
- Bit 0 1: HDMI 5V disabled in the SLEEP mode
0: HDMI 5V enabled in the SLEEP mode

15.2.6.3 **BOOST_LDO9_ON_VSEL_REG:**

| ADDRESS: 54H | | | | TYPE: RW | | | | |
|--------------|---------------|------|------|--------------|------|------|------|------|
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | BOOST_ON_VSEL | | | LDO9_ON_VSEL | | | | |
| DEFAULT | 由 BOOT 设定 | | | | | | | |

DESCRIPTION

- Bit 7-5 BOOST_ON_VSEL<2:0>: BOOST active mode voltage selection
- | | |
|-----------|-----------|
| 000: 4.7V | 001: 4.8V |
| 010: 4.9V | 011: 5V |
| 100: 5.1V | 101: 5.2V |
| 110: 5.3V | 111: 5.4V |
- Bit 4-0 LDO9_ON_VSEL: LDO9 active mode voltage selection
- | |
|----------------------|
| 1.8V~3.4V, step=0.1V |
| 00000: 1.8V |
| 00001: 1.9V |
| |
| 01110: 3.2V |
| 01111: 3.3V |
| 10000: 3.4V |
- Default value is set by boot.

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15.2.6.4 **BOOST_LDO9_SLP_VSEL_REG:**

| ADDRESS: 55H | | | | TYPE: RW | | | | |
|--------------|----------------|------|------|---------------|------|------|------|------|
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | BOOST_SLP_VSEL | | | LDO9_SLP_VSEL | | | | |
| DEFAULT | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |

DESCRIPTION

- Bit 7-5 BOOST_SLP_VSEL<2:0>: BOOST SLEEP mode voltage selection
 000: 4.7V 001: 4.8V
 010: 4.9V 011: 5V
 100: 5.1V 101: 5.2V
 110: 5.3V 111: 5.4V
- Bit 4-0 LDO9_SLP_VSEL: LDO9 SLEEP mode voltage selection
 1.8V~3.4V, step=0.1V
 00000: 1.8V
 00001: 1.9V

 01110: 3.2V
 01111: 3.3V
 10000: 3.4V

15.2.6.5 **BOOST_CTRL_REG: BOOST 控制 REGISTER**

| ADDRESS: 56H | | | | TYPE: RW | | | | |
|--------------|------|---------------|-------------------|-----------------------|-------------------|------|------|------|
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | RESV | BST_H V_ST | BST_SWI TCH_VT | BST_SWITC H_VT_HYS | BST_SWI TCH_EN | RESV | RESV | RESV |
| DEFAULT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

DESCRIPTION

- Bit 7 RESERVED
- Bit 6 BST_HV_ST: boost startup with heavy load
 0: disable
 1: enable
- Bit 5 BST_SWITCH_VT: Switching threshold from Boost mode to Switch mode.
 0: 3.8V
 1: 3.9V

Power Management System

| | | | | | | | | |
|---------|---|--|--|--|--|--|--|--|
| Bit 4 | BST_SWITCH_VT_HYS: Hysteresis of switching threshold from Boost mode to Switch mode. 0: 200mV 1: 300mV | | | | | | | |
| Bit 3 | BST_SWITCH_EN: Boost operating in the switch mode enable control. 0: Disable 1: Enable | | | | | | | |
| Bit 2:0 | RESERVED | | | | | | | |

15.2.6.6 DCDC_ILMAX: DCDC inductor peak current register

| ADDRESS: 56H | | | | TYPE: RW | | | | |
|--------------|-------------|------|-------------|----------|------|-------------|------|-------------|
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | BUCK4_ILMAX | | BUCK3_ILMAX | | | BUCK2_ILMAX | | BUCK1_ILMAX |
| DEFAULT | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |

DESCRIPTION

| | | | | | | | | |
|---------|--|--|--|--|--|--|--|--|
| Bit 7:6 | BUCK4_ILMAX: BUCK4 inductor peak current bit 00: 2.5A 01:3A 10:3.5A 11:4A | | | | | | | |
| Bit 5:4 | BUCK3_ILMAX: BUCK3 inductor peak current bit 00: 2A 01:2.5A 10:3A 11:3.5A | | | | | | | |
| Bit 3:2 | BUCK2_ILMAX: BUCK2 inductor peak current bit 00: 3.2A 01:3.6A 10:4A 11:5A | | | | | | | |
| Bit 1:0 | BUCK1_ILMAX: BUCK1 inductor peak current bit 00: 3.2A 01:3.6A 10:4A 11:5A | | | | | | | |

15.2.7 CHARGER SET REGISTER

15.2.7.1 CHRG_COMP_REG:

| ADDRESS: 9AH | | | | TYPE: RW | | | | |
|--------------|------|------|-----------------|----------|------|-----------|------|-----------------|
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | RESV | | BAT_SYS_CMP_DLY | | | CHRG_IRVS | | CHRG_OUTCV_COMP |

Power Management System

| | | | | | | | | |
|---------|---|---|---|---|---|---|---|---|
| DEFAULT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
|---------|---|---|---|---|---|---|---|---|

DESCRIPTION

- Bit 7-6 RESERVED
- Bit 5-4 BAT_SYS_CMP_DLY: Delay time for the voltage comparator between BAT and SYS.
 00: 20uS
 10: 10uS
 01: 40uS
 11: 20uS
- Bit 3-2 CHRG_IRVS: Setting the charger reverse current.
- Bit 1-0 CHRG_OUTCV_COMP: Setting the charger output voltage loop compensation

15.2.7.2 SUP_STS_REG:

| ADDRESS: A0H | | | | TYPE: RW | | | | |
|--------------|------------------------|------------------------|------|----------|------|-------------|------------------------|------------------------|
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | BAT_EXS (Read only) | CHG_STS (Read only) | | | RESV | USB_ILIM_EN | USB_EXS (Read only) | USB_EFF (Read only) |
| DEFAULT | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 |

DESCRIPTION

- Bit 7 BAT_EXS: Battery existence monitor
 0: No battery
 1: With battery
- Bit 6-4 CHG_STS: Charging status
 000: No Charging
 001: Wakeup current charging
 010: Trickle current charging
 011: Constant current or constant voltage charging
 100: Charging termination
 101: USB over voltage
 110: Battery temperature fault
 111: Charging time fault
- Bit 3 RESV: Reserved
- Bit 2 USB_ILIM_EN: USB input current limit enable control
 0: Disable
 1: Enable
- Bit 1 USB_EXS: USB plug-in monitor
 0: No USB plugged in
 1: USB plugged in

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Bit 0 USB_EFF: USB fault monitor
 0: USB fault
 1: USB okay

15.2.7.3 **USB_CTRL_REG:**

| ADDRESS: A1H | | | | TYPE: RW | | | | |
|--------------|------------|-----------------|------|----------|--------------|------|------|------|
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | CHRG_CT_EN | USB_CHG_SD_VSEL | | | USB_ILIM_SEL | | | |
| DEFAULT | OTP | | | | | | | |

DESCRIPTION

Bit 7 CHRG_CT_EN: Constant temperature charging enable
 0:disable
 1:enable

Bit 6-4 USB_CHG_SD_VSEL: the USB low voltage shutdown charger voltage selection
 000: 2.78V, 001:2.85V, 010: 2.92V, 011: 2.99V
 100: 3.06V, 101: 3.13V, 110: 3.19V, 111: 3.26V

Bit 3-0 USB_ILIM_SEL: USB input current selection
 0000: 0.45A, 0001: 0.08A, 0010: 0.85A, 0011: 1A,
 0100: 1.25A, 0101: 1.5A, 0110: 1.75A, 0111: 2A,
 1000: 2.25A, 1001: 2.5A, 1010: 2.75A, 1011: 3A,
 11xx:3A

DEFAULT value is set by BOOT

15.2.7.4 **CHRG_CTRL_REG1: CHARGE CONTROL REGISTER1**

| ADDRESS: A3H | | | | TYPE: RW | | | | |
|--------------|---------|--------------|------|----------|--------------|------|------|------|
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | CHRG_EN | CHRG_VOL_SEL | | | CHRG_CUR_SEL | | | |
| DEFAULT | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 1 |

DESCRIPTION

Bit 7 CHRG_EN: Charger enable
 0: Disable
 1: Enable

Power Management System

| | | | | | | | | |
|---------|--|--|--|--|--|--|--|--|
| Bit 6-4 | CHRG_VOL_SEL: Charging termination voltage selection 000: 4.05V, 001:4.1V, 010:4.15V, 011:4.2V 100: 4.25V, 101: 4.3V, 110/111: 4.35V | | | | | | | |
| Bit 3-0 | CHRG_CUR_SEL: Charging current selection, Rs=20mΩ 0000:1A, 0001:1.2A, 0010:1.4A, 0011:1.6A 0100:1.8A, 0101:2A, 0110:2.2A, 0111:2.4A 1000:2.6A, 1001:2.8A, 1010--1111:3A CHRG_CUR_SEL: Charging current selection, Rs=10mΩ 0000:2A, 0001:2.4A, 0010:2.8A, 0011:3.2A 0100:3.6A, 0101:4A, 0110:4.4A, 0111:4.8A 1000:5.2A, 1001:5.6A, 1010--1111:6A | | | | | | | |

15.2.7.5 CHRG_CTRL_REG2: CHARGER CONTROL REGISTER2

| ADDRESS: A4H | | | | TYPE: RW | | | | |
|--------------|---------------|------|------|------------------|------|------|-----------------|------|
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | CHRG_TERM_SEL | | | CHRG_TIMER_TRIKL | | | CHRG_TIMER_CCCV | |
| DEFAULT | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 |

DESCRIPTION

| | | | | | | | | |
|---------|--|--|--|--|--|--|--|--|
| Bit 7-6 | CHRG_TERM_SEL: Charging termination current selection, Rs=20mΩ 00:100mA, 01:150mA, 10:200mA, 11:250mA CHRG_TERM_SEL: Charging termination current selection, Rs=10mΩ 00:200mA, 01:300mA, 10:400mA, 11:500mA | | | | | | | |
| Bit 5-3 | CHRG_TIMER_TRIKL: Trickle current charging time selection 000:30min, 001:60min, 010:90min, 011:120min, 100:150min, 101:180min, 110, 111:210min | | | | | | | |
| Bit 2-0 | CHRG_TIMER_CCCV: Constant current/voltage charging timeout threshold selection 000:4h, 001:5h, 010:6h, 011:8h, 100:10h 101:12h, 110:14h, 111:16h | | | | | | | |

15.2.7.6 CHRG_CTRL_REG3: CHARGING CONTROL REGISTER3

| ADDRESS: A5H | | | | TYPE: RW | | | | |
|--------------|----------------|---------------|---------------------------|------------|-----------------------------|----------------------------|------|------|
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | SYS_C AN_SD | TS2_S D_EN | CHRG_TE RM_ANA_D IG | CHRG_PHASE | CHRG_TI MER_TRI KL_EN | CHRG_TIM ER_CCCV_ EN | RESV | |

Power Management System

| | | | | | | | | |
|---------|---|---|---|---|---|---|---|---|
| DEFAULT | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
|---------|---|---|---|---|---|---|---|---|

DESCRIPTION

| | |
|---------|--|
| Bit 7 | SYS_CAN_SD: Vsys shutdown control with battery as sole power supply 0: Disable 1: Enable |
| Bit 6 | TS2_SD_EN: PMIC EN bit control when TS2 is over either upper or lower limit 0: Disable the EN bit 1: Enable the EN bit |
| Bit 5 | CHRG_TERM_ANA_DIG: Charging termination flag bit source selection 0: Analog 1: Digital |
| Bit 4 | CHRG_PHASE: Charger timer reverse mode control 0: Normal 1: Reverse |
| Bit 3 | CHRG_TIMER_TRIKL_EN: Trickle current charging timer control 0: Enable 1: Disable |
| Bit 2 | CHRG_TIMER_CCCV_EN: Constant current/constant voltage timer control 0: Disable 1: Enable |
| Bit 1-0 | Reserved |

15.2.7.7 OTG_ILIM_REG/BAT_CTRL_REG: OTG/BATTERY CURRENT LIMIT REGISTER

| ADDRESS: A6H | | | | TYPE: RW | | | | |
|--------------|-----------------|----------------|----------------|--------------|------|------|------------------|------|
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | BAT_DIS_ILIM_EN | H5V_IPKLIM_SEL | OTG_IPKLIM_SEL | OTG_ILIM_SEL | | | BAT_DISCHRG_ILIM | |
| DEFAULT | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 |

DESCRIPTION

| | |
|-------|--|
| Bit 7 | BAT_DIS_ILIM_EN: Discharging current limit function control 0: Disable 1: Enable |
| Bit 6 | H5V_IPKLIM_SEL: HDMI 5V peak current limit selection 0: 100mA 1: 115mA |
| Bit 5 | OTG_IPKLIM_SEL: OTG peak current limit selection |

Power Management System

| | |
|---------|--|
| | 0:125%*OTG_ILIM_SEL |
| | 1:150%*OTG_ILIM_SEL |
| Bit 4-3 | OTG_ILIM_SEL:OTG current limit selection 00:700mA, 01:800mA, 10:900mA, 11:1A |
| Bit 2-0 | BAT_DISCHRG_ILIM: Discharging current limit selection, Rs=20mΩ 000:3A, 001:3.5A, 010:4A, 011 4.5A, 1xx:5A BAT_DISCHRG_ILIM: Discharging current limit selection, Rs=10mΩ 000:6A, 001:7A, 010:8A, 011 9A, 1xx:10A |

15.2.7.8 **BATHTS_TS1_REG: TS1 HT PROTECTION THRESHOLD REGISTER**

| ADDRESS: A8H | | | | TYPE: RW | | | | |
|--------------|------------|------|------|----------|------|------|------|------|
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | BATHTS_TS1 | | | | | | | |
| DEFAULT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

DESCRIPTION

Bit 7-0 BATHTS_TS1: Battery over temperature protection threshold sensed at TS1.

15.2.7.9 **BATLTS_TS1_REG: TS1 LT PROTECTION REGISTER**

| ADDRESS: A9H | | | | TYPE: RW | | | | |
|--------------|------------|------|------|----------|------|------|------|------|
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | BATLTS_TS1 | | | | | | | |
| DEFAULT | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

DESCRIPTION

Bit 7-0 BATLTS_TS1: Battery low temperature protection threshold sensed at TS1.

15.2.7.10 **BATHTS_TS2_REG: TS2 HT PROTECTION REGISTER**

| ADDRESS: AAH | | | | TYPE: RW | | | | |
|--------------|------------|------|------|----------|------|------|------|------|
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | BATHTS_TS2 | | | | | | | |
| DEFAULT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Power Management System

DESCRIPTION

Bit 7-0 BATHTS_TS2: Battery over temperature protection threshold sensed at TS2

15.2.7.11 BAT_LTS_TS2_REG: TS2 LT PROTECTION REGISTER

| ADDRESS: ABH | | | | TYPE: RW | | | | |
|--------------|-------------|------|------|----------|------|------|------|------|
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | BAT_LTS_TS2 | | | | | | | |
| DEFAULT | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

DESCRIPTION

Bit 7-0 BAT_LTS_TS2: Battery low temperature protection threshold sensed at TS2.

15.2.7.12 TS_CTRL_REG: TS PIN CONTROL REGISTER

| ADDRESS: ACH | | | | TYPE: RW | | | | |
|--------------|-------|-----------------------|---------|----------|---------|------|---------|------|
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | GG_EN | TS2_TE (Read only) | TS2_FUN | TS1_FUN | TS2_CUR | | TS1_CUR | |
| DEFAULT | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |

DESCRIPTION

- Bit 7 GG_EN: Battery fuel gauge enable control
0: Disable
1: Enable
- Bit 6 TS2_TE: Flag for TS2 value out of higher or lower limit
0: Out of limit
1: In the limit
- Bit 5 TS2_FUN: TS2 pin function selection
0: External temperature monitoring (NTC thermistor connected externally)
1: ADC input
- Bit 4 TS1_FUN: TS1pin function selection
0: External temperature monitoring (NTC thermistor connected externally)

Power Management System

1:ADC input

- Bit 3-2 TS2_CUR: TS2 pin output current selection in the temperature monitoring mode
00:20uA, 01:40uA, 10:60uA, 11:80uA
- Bit 1-0 TS1_CUR: TS1 pin output current selection in the temperature monitoring mode
00:20uA, 01:40uA, 10:60uA, 11:80uA

15.2.7.13 ADC_CTRL_REG: ADC CONTROL REGISTER

| ADDRESS: ADH | | | | TYPE: RW | | | | |
|--------------|----------------|----------------|----------------|----------------|---------------|-------------|------|------|
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | ADC_VO L_EN | ADC CU R_EN | ADC_TS1 _EN | ADC_TS 2_EN | ADC_PHA SE | ADC_CLK_SEL | | |
| DEFAULT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

DESCRIPTION

- Bit 7 ADC_VOL_EN: If GG_EN=0: Battery voltage ADC enable control
0: Disable
1: Enable
- Bit 6 ADC_CUR_EN: If GG_EN=0: Battery current ADC enable control
0: Disable
1: Enable
- Bit 5 ADC_TS1_EN: TS1 ADC enable control
0: Disable
1: Enable
- Bit 4 ADC_TS2_EN: TS2 ADC enable control
0: Disable
1: Enable
- Bit 3 ADC_PHASE: ADC's clock phase
0: Normal
1: Reverse
- Bit 2-0 ADC_CLK_SEL: ADC clock frequency selection
000: 2Meg, 001: 1Meg, 010: 500K, 011: 250K, 100: 125K
101: 64K, 110: 32K, 111: 16K

Power Management System

15.2.7.14 ON_SOURCE_REG: POWER UP SOURCE REGISTER

| ADDRESS: AEH | | | | TYPE: RW | | | | |
|--------------|----------|------------|--------|----------------|------------------|------------------|------|------|
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | ON_PWRON | ON_PLUG_IN | ON_RTC | RESTART_RESETB | RESTART_PWRON_LP | RESTART_RECOVERY | RESV | RESV |
| DEFAULT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

DESCRIPTION

- Bit 7 ON_PWRON: PMIC power up by pressing PWRON
 Bit 6 ON_PLUG_IN: PMIC power up by USB plugging in
 Bit 5 ON_RTC: PMIC power up by RTC timer
 Bit 4 RESTART_RESETB: PMIC restart by pulling down NRESPWRON pin
 Bit 3 RESTART_PWRON_LP: PMIC restart by long pressing PWRON
 Bit 2 RESTART_RECOVERY: PMIC restart by long pressing PWRON to trigger Recovery

 Bit 1-0 RESERVED

15.2.7.15 OFF_SOURCE_REG: POWER OFF SOURCE REGISTER

| ADDRESS: AFH | | | | TYPE: R | | | | |
|--------------|------------|------------|---------|------------|-------------|--------------|---------|------------|
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | OFF_REF_DN | OFF_SYS_OV | OFF_TSD | OFF_SYS_UV | OFF_DEV_OFF | OFF_PWRON_LP | OFF_TS2 | OFF_SYS_LO |
| DEFAULT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

DESCRIPTION

- Bit 7 OFF_REF_DN: PMIC power off due to Vref off the range during normal operation
 Bit 6 OFF_SYS_OV: PMIC power off by Vsys over voltage protection
 Bit 5 OFF_TSD: PMIC power off due to over temperature protection
 Bit 4 OFF_SYS_UV: PMIC power off due to Vsys under voltage protection
 Bit 3 OFF_DEV_OFF: PMIC power off due to DEV_OFF bit written
 Bit 2 OFF_PWRON_LP: PMIC power off due to long pressing PWRON
 Bit 1 OFF_TS2: PMIC power off due to TS2 value over the high or low limit
 Bit 0 OFF_SYS_LO: PMIC power off due to Vsys low voltage set by software (If Reg21<4> vb_lo_act=0)

15.2.8 BATTERY FUEL GAUGE CONFIGURATION REGISTER

15.2.8.1 GGCON_REG: FUEL GAUGE CONFIGURATION REGISTER

| ADDRESS: B0H | | | | TYPE: RW | | | | |
|--------------|---------------------|--------------------|------|------------------|------|------------------|--------------|------|
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | CUR_SAMPL_CON_TIMES | ADC_OFF_CAL_INTERV | | OCV_SAMPL_INTERV | | ADC_CUR_VOL_MODE | ADC_RES_MODE | |
| DEFAULT | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 |

DESCRIPTION

- Bit 7-6 CUR_SAMPL_CON_TIMES: The number of continuous sampling on the battery current ADC
00:8 01:16 10:32 11:64
- Bit 5-4 ADC_OFF_CAL_INTERV<1:0>: ADC's error calibration interval time
00:8min, 01:16min, 10:32min, 11:48min
- Bit 3-2 OCV_SAMPL_INTERV<1:0>: OCV sampling interval time
00:8min, 01:16min, 10:32min, 11:48min
- Bit 1 ADC_CUR_VOL_MODE: Fuel gauge operation mode selection
0: Voltage mode
1: Current mode
- Bit 0 ADC_RES_MODE: Battery internal resistance calculation control
0: Disable
1: Enable

15.2.8.2 GGSTS_REG: FUEL GAUGE STATUS REGISTER

| ADDRESS: B1H | | | | TYPE: RW | | | | |
|--------------|------|----------------------|------|----------|----------------------------|----------------------------|---------------------------|----------------------------|
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | RESV | RES_CUR_AVG_SEL<1:0> | | BAT_CON | RELAX_V _{OL1_UPD} | RELAX_V _{OL2_UPD} | RELAX_S _{TS(RO)} | IV_AVG_U _{PD_STS} |
| DEFAULT | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |

DESCRIPTION

- Bit 7 RESERVED
- Bit 6-5 RES_CUR_AVG_SEL<1:0>: The fraction of the current ripple for internal resistance calculation

Power Management System

| | |
|-------|--|
| | 00: 1/2, 01:1/4, 10:1/8, 11:1/16 |
| Bit 4 | BAT_CON: The rising edge detection when the battery is first connected 0: Not detected 1: Detected |
| Bit 3 | RELAX_VOL1_UPD:Flag bit for battery voltage1 update in the relaxation state. 0:NOT 1:YES |
| Bit 2 | RELAX_VOL2_UPD: Flag bit for battery voltage1 update in the relaxation state 0:NOT 1:YES |
| Bit 1 | RELAX_STS: Flag bit for battery turning to relaxation state 0: Not in relaxation 1: in relaxation |
| Bit 0 | IV_AVG_UPD_STS: Flag bit for the internal resistance successfully sensed 0: Not sensed 1: Sensed |

15.2.8.3 FRAME_SMP_INTERV_REG:

| ADDRESS: B2H | | | | TYPE: RW | | | | |
|--------------|------|------|-------------|---------------------------|------|------|------|------|
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | RESV | RESV | AUTO_SLP_EN | FRAME_SMP_INTERV_REG<4:0> | | | | |
| DEFAULT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

DESCRIPTION

| | |
|-----------|---|
| Bit 7-6 | RESERVED |
| Bit 5 | AUTO_SLP_EN: Automatically switching to SLEEP mode control 0: Disable 1: Enable |
| Bit4-Bit0 | FRAME_SMP_INTERV_REG<4:0>: The interval of DATA frame acquisition in the SLEEP mode |

15.2.8.4 AUTO_SLP_CUR_THR_REG: CURRENT THRESHOLD REGISTER

| ADDRESS: B3H | | | | TYPE: RW | | | | |
|--------------|------|------|------|----------|------|------|------|------|
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |

Power Management System

| | | | | | | | | |
|---------|---------------------------|---|---|---|---|---|---|---|
| SYMBOL | AUTO_SLP_CUR_THR_REG<7:0> | | | | | | | |
| DEFAULT | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |

DESCRIPTION

Bit 7-0 AUTO_SLP_CUR_THR_REG<7:0>: Current threshold for automatically switching to Sleep mode

15.2.8.5 GASCNT_CAL_REG3: BAT CAPACITY CALIBRATION REGISTER3

| | | | | | | | | |
|--------------|-------------------|------|------|----------|------|------|------|------|
| ADDRESS: B4H | | | | TYPE: RW | | | | |
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | GASCNT_CAL<31:24> | | | | | | | |
| DEFAULT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

DESCRIPTION

Bit 7-0 GASCNT_CAL<31:24>: Calibrated battery capacity value bits <31:24>

Note The register B4 must be written first, and then B5, B6...B7 must be written last.

15.2.8.6 GASCNT_CAL_REG2: BAT CAPACITY CALIBRATION REGISTER2

| | | | | | | | | |
|--------------|-------------------|------|------|----------|------|------|------|------|
| ADDRESS: B5H | | | | TYPE: RW | | | | |
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | GASCNT_CAL<23:16> | | | | | | | |
| DEFAULT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

DESCRIPTION

Bit 7-0 GASCNT_CAL<23:16>: Calibrated battery capacity value bits <23:16>

15.2.8.7 GASCNT_CAL_REG1: BAT CAPACITY CALIBRATION REGISTER1

| | | | | | | | | |
|--------------|------------------|------|------|----------|------|------|------|------|
| ADDRESS: B6H | | | | TYPE: RW | | | | |
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | GASCNT_CAL<15:8> | | | | | | | |

Power Management System

| | | | | | | | | | |
|---------|---|---|---|---|---|---|---|---|---|
| DEFAULT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
|---------|---|---|---|---|---|---|---|---|---|

DESCRIPTION

Bit 7-0 GASCNT_CAL<15:8>: Calibrated battery capacity value bits <15:8>

15.2.8.8 **GASCNT_CAL_REG0: BAT CAPACITY CALIBRATION REGISTER0**

| ADDRESS: B7H | | | | TYPE: RW | | | | | |
|--------------|-----------------|------|------|----------|------|------|------|------|---|
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | |
| SYMBOL | GASCNT_CAL<7:0> | | | | | | | | |
| DEFAULT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

DESCRIPTION

Bit 7-0 GASCNT_CAL<7:0>: Calibrated battery capacity value bits <7:0>

15.2.8.9 **GASCNT_REG3: BAT CAPACITY REGISTER3**

| ADDRESS: B8H | | | | TYPE: R | | | | | |
|--------------|----------------|------|------|---------|------|------|------|------|---|
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | |
| SYMBOL | GASCNT <31:24> | | | | | | | | |
| DEFAULT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

DESCRIPTION

Bit 7-0 GASCNT<31:24>: Battery capacity value bits<31:24>

15.2.8.10 **GASCNT_REG2: BAT CAPACITY REGISTER2**

| ADDRESS: B9H | | | | TYPE: R | | | | | |
|--------------|----------------|------|------|---------|------|------|------|------|---|
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | |
| SYMBOL | GASCNT <23:16> | | | | | | | | |
| DEFAULT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

DESCRIPTION

Bit 7-0 GASCNT<23:16>: Battery capacity value bits<23:16>

Power Management System

15.2.8.11 **GASCNT_REG1: BAT CAPACITY REGISTER1**

| ADDRESS: BAH | | | | TYPE: R | | | | |
|--------------|---------------|------|------|---------|------|------|------|------|
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | GASCNT <15:8> | | | | | | | |
| DEFAULT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

DESCRIPTION

Bit 7-0 GASCNT<15:8>: Battery capacity value bits<15:8>

15.2.8.12 **GASCNT_REG0: BAT CAPACITY REGISTER0**

| ADDRESS: BBH | | | | TYPE: R | | | | |
|--------------|--------------|------|------|---------|------|------|------|------|
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | GASCNT <7:0> | | | | | | | |
| DEFAULT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

DESCRIPTION

Bit 7-0 GASCNT<7:0>: Battery capacity value bits<7:0>

15.2.8.13 **BAT_CUR_REGH: BAT CURRENT HIGH BITS REGISTER**

| ADDRESS: BCH | | | | TYPE: R | | | | |
|--------------|------|------|------|---------|-------------------|------|------|------|
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | RESV | RESV | RESV | RESV | BAT_CUR_AVG<11:8> | | | |
| DEFAULT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

DESCRIPTION

Bit 7-4 RESERVED

Bit 3-0 BAT_CUR_AVG<11:8>: Battery average current value bits<11:8>

15.2.8.14 **BAT_CUR_AVG_REGL: BAT CURRENT LOW BITS REGISTER**

| | |
|--------------|---------|
| ADDRESS: BDH | TYPE: R |
|--------------|---------|

Power Management System

| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---------|------------------|------|------|------|------|------|------|------|
| SYMBOL | BAT_CUR_AVG<7:0> | | | | | | | |
| DEFAULT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

DESCRIPTION

Bit 7-0 BAT_CUR_AVG<7:0>: Battery average current value bits<7:0>

15.2.8.15 TS1_ADC_REGH: TS1 ADC HIGH BITS REGISTER

| ADDRESS: BEH | | | | TYPE: R | | | | | | | | |
|--------------|------|------|------|---------|---------------|------|------|------|--|--|--|--|
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | | | | |
| SYMBOL | RESV | RESV | RESV | RESV | TS1_ADC<11:8> | | | | | | | |
| DEFAULT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | | | |

DESCRIPTION

Bit 7-4 RESERVED

Bit 3-0 TS1_ADC<11:8>: TS1 ADC value bits<11:8>

15.2.8.16 TS1_ADC_REGL: TS1 ADC LOW BITS REGISTER

| ADDRESS: BFH | | | | TYPE: R | | | | |
|--------------|--------------|------|------|---------|------|------|------|------|
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | TS1_ADC<7:0> | | | | | | | |
| DEFAULT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

DESCRIPTION

Bit 7-0 TS1_ADC<7:0>: TS1 ADC value bits<7:0>

15.2.8.17 TS2_ADC_REGH: TS2 ADC HIGH BITS REGISTER

| ADDRESS: C0H | | | | TYPE: R | | | | | | | | |
|--------------|------|------|------|---------|---------------|------|------|------|--|--|--|--|
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | | | | |
| SYMBOL | RESV | RESV | RESV | RESV | TS2_ADC<11:8> | | | | | | | |

Power Management System

| | | | | | | | | |
|---------|---|---|---|---|---|---|---|---|
| DEFAULT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
|---------|---|---|---|---|---|---|---|---|

DESCRIPTION

- Bit 7-4 RESERVED
 Bit 3-0 TS2_ADC<11:8>; TS2 ADC value bits<15:8>.

15.2.8.18 TS2_ADC_REGHL: TS2 ADC LOW BITS REGISTER

| ADDRESS: C1H | | | | TYPE: R | | | | |
|--------------|--------------|------|------|---------|------|------|------|------|
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | TS2_ADC<7:0> | | | | | | | |
| DEFAULT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

DESCRIPTION

- Bit 7-0 TS2_ADC<7:0>; TS2 ADC value bits<7:0>

15.2.8.19 BAT_OCV_REGH: BAT OVER VOLTAGE HIGH BITS REGISTER

| ADDRESS: C2H | | | | TYPE: R | | | | |
|--------------|------|------|------|---------|---------------|------|------|------|
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | RESV | RESV | RESV | RESV | BAT_OCV<11:8> | | | |
| DEFAULT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

DESCRIPTION

- Bit 7-4 RESERVED
 Bit 3-0 BAT_OCV<11:8>; Battery OCV value bits<11:8>

15.2.8.20 BAT_OCV_REGL : BAT OVER TEMP LOW BITS REGISTER

| ADDRESS: C3H | | | | TYPE: R | | | | |
|--------------|------|------|------|---------|------|------|------|------|
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |

Power Management System

| | | | | | | | | |
|---------|--------------|---|---|---|---|---|---|---|
| SYMBOL | BAT_OCV<7:0> | | | | | | | |
| DEFAULT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

DESCRIPTION

Bit 7-0 BAT_OCV<7:0>: Battery OCV voltage value bits<7:0>.

15.2.8.21 **BAT_VOL_REGH : BAT VOLTAGE HIGH BITS REGISTER**

| | | | | | | | | | | | | |
|--------------|------|------|------|---------|---------------|------|------|------|--|--|--|--|
| ADDRESS: C4H | | | | TYPE: R | | | | | | | | |
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | | | | |
| SYMBOL | RESV | RESV | RESV | RESV | BAT_VOL<11:8> | | | | | | | |
| DEFAULT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | | | |

DESCRIPTION

Bit 7-4 RESERVED

Bit 3-0 BAT_VOL<11:8>: Real time battery voltage value bits<11:8>.

15.2.8.22 **BAT_VOL_REGL: BAT VOLTAGE LOW BITS REGISTER**

| | | | | | | | | |
|--------------|--------------|------|------|---------|------|------|------|------|
| ADDRESS: C5H | | | | TYPE: R | | | | |
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | BAT_VOL<7:0> | | | | | | | |
| DEFAULT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

DESCRIPTION

Bit 7-0 BAT_VOL<7:0>: Real time battery voltage value bits<7:0>.

15.2.8.23 **RELAX_ENTRY_THRES_REGH**

| | | | | | | | | |
|--------------|------|------|------|----------|------|------|------|------|
| ADDRESS: C6H | | | | TYPE: RW | | | | |
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |

Power Management System

| SYMBOL | RESV | RESV | RESV | RESV | RELAX_ENTRY_THRES<11:8> | | | |
|---------|------|------|------|------|-------------------------|---|---|---|
| DEFAULT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

DESCRIPTION

- Bit 7-4 RESERVED
 Bit 3-0 RELAX_ENTRY_THRES<11:8>: The threshold value bits<15:8> for the battery going into relaxation state

15.2.8.24 RELAX_ENTRY_THRES_REGL

| ADDRESS: C7H | | | | TYPE: RW | | | | |
|--------------|------------------------|------|------|----------|------|------|------|------|
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | RELAX_ENTRY_THRES<7:0> | | | | | | | |
| DEFAULT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

DESCRIPTION

- Bit 7-0 RELAX_ENTRY_THRES<7:0>: The threshold value bits<7:0> for the battery going into relaxation state

15.2.8.25 RELAX_EXIT_THRES_REGH

| ADDRESS: C8H | | | | TYPE: RW | | | | |
|--------------|------|------|------|----------|------------------------|------|------|------|
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | RESV | RESV | RESV | RESV | RELAX_EXIT_THRES<11:8> | | | |
| DEFAULT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

DESCRIPTION

- Bit 7-4 RESERVED
 Bit 3-0 RELAX_EXIT_THRES<11:8>: The threshold value bits<15:8> for the battery out of relaxation state

15.2.8.26 RELAX_EXIT_THRES_REGL

| ADDRESS: C9H | | | | TYPE: RW | | | | |
|--------------|------|------|------|----------|------|------|------|------|
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |

Power Management System

| | | | | | | | | |
|---------|-----------------------|---|---|---|---|---|---|---|
| SYMBOL | RELAX_EXIT_THRES<7:0> | | | | | | | |
| DEFAULT | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |

DESCRIPTION

Bit 7-0 RELAX_EXIT_THRES<7:0>: The threshold value bits<7:0> for the battery out of relaxation state

15.2.8.27 RELAX_VOL1_REGH

| | | | | | | | | |
|--------------|------|------|------|---------|------------------|------|------|------|
| ADDRESS: CAH | | | | TYPE: R | | | | |
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | RESV | RESV | RESV | RESV | RELAX_VOL1<11:8> | | | |
| DEFAULT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

DESCRIPTION

Bit 7-4 RESERVED

Bit 3-0 RELAX_VOL1<11:8>: Voltage1 value bits<11:8> in the relaxation state

15.2.8.28 RELAX_VOL1_REGL

| | | | | | | | | |
|--------------|-----------------|------|------|---------|------|------|------|------|
| ADDRESS: CBH | | | | TYPE: R | | | | |
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | RELAX_VOL1<7:0> | | | | | | | |
| DEFAULT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

DESCRIPTION

Bit 7-0 RELAX_VOL1<7:0>: Voltage1 value bits<7:0> in the relaxation state

15.2.8.29 RELAX_VOL2_REGH

| | | | | | | | | |
|--------------|------|------|------|---------|------------------|------|------|------|
| ADDRESS: CCH | | | | TYPE: R | | | | |
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | RESV | RESV | RESV | RESV | RELAX_VOL2<11:8> | | | |
| DEFAULT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Power Management System

DESCRIPTION

Bit 7-4 RESERVED

Bit 3-0 RELAX_VOL2<11:8>: Voltage2 value bits<11:8> in the relaxation state

15.2.8.30 **RELAX_VOL2_REGL**

| ADDRESS: CDH | | | | TYPE: R | | | | |
|--------------|-----------------|------|------|---------|------|------|------|------|
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | RELAX_VOL2<7:0> | | | | | | | |
| DEFAULT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

DESCRIPTION

Bit 7-0 RELAX_VOL2<7:0>: Voltage2 value bits<7:0> in the relaxation state

15.2.8.31 **BAT_CUR_R_CALC_REGH:BAT CURRENT HIGH BITS REGISTER**

| ADDRESS: CEH | | | | TYPE: R | | | | | | | | |
|--------------|------|------|------|---------|----------------------|------|------|------|--|--|--|--|
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | | | | |
| SYMBOL | RESV | RESV | RESV | RESV | BAT_CUR_R_CALC<11:8> | | | | | | | |
| DEFAULT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | | | |

DESCRIPTION

Bit 7-4 RESERVED

Bit 3-0 BAT_CUR_R_CALC<11:8>: Battery stable current value bits<11:8> for the internal resistance calculation.

15.2.8.32 **BAT_CUR_R_CALC_REGL: BAT CURRENT LOW BITS REGISTER**

| ADDRESS: CFH | | | | TYPE: R | | | | |
|--------------|---------------------|------|------|---------|------|------|------|------|
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | BAT_CUR_R_CALC<7:0> | | | | | | | |

Power Management System

| | | | | | | | | |
|---------|---|---|---|---|---|---|---|---|
| DEFAULT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
|---------|---|---|---|---|---|---|---|---|

DESCRIPTION

Bit 7-0 BAT_CUR_R_CALC<7:0>: Battery stable current value bits<7:0> for the internal resistance calculation.

15.2.8.33 BAT_VOL_R_CALC_REGH: BAT VOLTAGE HIGH BITS REGISTER

| ADDRESS: D0H | | | | TYPE: R | | | | | |
|--------------|------|------|------|---------|----------------------|------|------|------|--|
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | |
| SYMBOL | RESV | RESV | RESV | RESV | BAT_VOL_R_CALC<11:8> | | | | |
| DEFAULT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |

DESCRIPTION

Bit 7-4 RESERVED

Bit 3-0 BAT_VOL_R_CALC<11:8>: Battery stable voltage value bits<11:8> for the internal resistance calculation.

15.2.8.34 BAT_VOL_R_CALC_REGL: BAT VOLTAGE LOW BITS REGISTER

| ADDRESS: D1H | | | | TYPE: R | | | | |
|--------------|---------------------|------|------|---------|------|------|------|------|
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | BAT_VOL_R_CALC<7:0> | | | | | | | |
| DEFAULT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

DESCRIPTION

Bit 7-0 BAT_VOL_R_CALC<7:0>: Battery stable voltage value bits<7:0> for the internal resistance calculation.

15.2.8.35 CAL_OFFSET_REGH: OFFSET HIGH BITS REGISTER

| ADDRESS: D2H | | | | TYPE: RW | | | | | |
|--------------|------|------|------|----------|----------------------|------|------|------|--|
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | |
| SYMBOL | RESV | RESV | RESV | RESV | CAL_OFFSET_REG<11:8> | | | | |

Power Management System

| | | | | | | | | |
|---------|---|---|---|---|---|---|---|---|
| DEFAULT | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
|---------|---|---|---|---|---|---|---|---|

DESCRIPTION

- Bit 7-4 RESERVED
 Bit 3-0 CAL_OFFSET_REG<11:8>: PCB current offset value bits<11:8>.
 Note The register D2 must be written first, and D3 must be written last.

15.2.8.36 CAL_OFFSET_REGL: OFFSET LOW BITS REGISTER

| | | | | | | | | |
|--------------|---------------------|------|------|----------|------|------|------|------|
| ADDRESS: D3H | | | | TYPE: RW | | | | |
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | CAL_OFFSET_REG<7:0> | | | | | | | |
| DEFAULT | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

DESCRIPTION

- Bit 7-0 CAL_OFFSET_REG<7:0>: PCB current offset value bits<7:0>.

15.2.8.37 NON_ACT_TIMER_CNT_REGL:

| | | | | | | | | |
|--------------|------------------------|------|------|---------|------|------|------|------|
| ADDRESS: D4H | | | | TYPE: R | | | | |
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | NON_ACT_TIMER_CNT<7:0> | | | | | | | |
| DEFAULT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

DESCRIPTION

- Bit 7-0 NON_ACT_TIMER_CNT<7:0>: Timer for SLEEP or OFF state (Unit: minute)

15.2.8.38 VCALIB0_REGH: VOLTAGE0 CALIBRATION HIGH BITS REGISTER

| | | | | | | | | |
|--------------|------|------|------|---------|---------------|------|------|------|
| ADDRESS: D5H | | | | TYPE: R | | | | |
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | RESV | RESV | RESV | RESV | VCALIB0<11:8> | | | |
| DEFAULT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Power Management System

DESCRIPTION

- | | | | | | | | | |
|---------|--|--|--|--|--|--|--|--|
| Bit 7-4 | RESERVED | | | | | | | |
| Bit 3-0 | Voltage0 calibration value bits<11:8> for calculating offset error and gain error. | | | | | | | |

15.2.8.39 VCALIB0_REGL: VOLTAGE0 CALIBRATION LOW BITS REGISTER

| ADDRESS: D6H | | | | TYPE: R | | | | |
|--------------|--------------|------|------|---------|------|------|------|------|
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | VCALIB0<7:0> | | | | | | | |
| DEFAULT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

DESCRIPTION

- | | | | | | | | | |
|---------|---|--|--|--|--|--|--|--|
| Bit 7-0 | Voltage0 calibration value bits<7:0> for calculating offset error and gain error. | | | | | | | |
|---------|---|--|--|--|--|--|--|--|

15.2.8.40 VCALIB1_REGH: VOLTAGE1 CALIBRATION HIGH BITS REGISTER

| ADDRESS: D7H | | | | TYPE: R | | | | | |
|--------------|------|------|------|---------|---------------|------|------|------|--|
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | |
| SYMBOL | RESV | RESV | RESV | RESV | VCALIB1<11:8> | | | | |
| DEFAULT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |

DESCRIPTION

- | | | | | | | | | |
|---------|--|--|--|--|--|--|--|--|
| Bit 7-4 | RESERVED | | | | | | | |
| Bit 3-0 | Voltage1 calibration value bits<11:8> for calculating offset error and gain error. | | | | | | | |

15.2.8.41 VCALIB1_REGL: VOLTAGE1 CALIBRATION LOW BITS REGISTER

| ADDRESS: D8H | | | | TYPE: R | | | | |
|--------------|--------------|------|------|---------|------|------|------|------|
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | VCALIB1<7:0> | | | | | | | |
| DEFAULT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Power Management System

DESCRIPTION

Bit 7- Voltage1 calibration value bits<7:0> for calculating offset error and gain error.

15.2.8.42 IOFFSET_REGH: CURRENT OFFSET HIGH BITS REGISTER

| ADDRESS: DDH | | | | TYPE: R | | | | |
|--------------|------|------|------|---------|----------------|------|------|------|
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | RESV | RESV | RESV | RESV | IOOFFSET<11:8> | | | |
| DEFAULT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

DESCRIPTION

Bit 7-4 RESERVED

Bit 3-0 Calculated current offset value bits<11:8>

15.2.8.43 IOFFSET_REGL: CURRENT OFFSET LOW BITS REGISTER

| ADDRESS: DEH | | | | TYPE: R | | | | |
|--------------|---------------|------|------|---------|------|------|------|------|
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | IOOFFSET<7:0> | | | | | | | |
| DEFAULT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

DESCRIPTION

Bit 7-0 Calculated current offset value bits<7:0>

15.2.9 DATA REGISTER

15.2.9.1 DATA0_REG: DATA0 DATA REGISTER

| ADDRESS: DFH | | | | TYPE: RW | | | | |
|--------------|----------|----------|----------|----------|----------|----------|----------|----------|
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | DATA0(7) | DATA0(6) | DATA0(5) | DATA0(4) | DATA0(3) | DATA0(2) | DATA0(1) | DATA0(0) |
| DEFAULT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Power Management System

| | | | | | | | | |
|---|--|--|--|--|--|--|--|--|
| T | | | | | | | | |
|---|--|--|--|--|--|--|--|--|

DESCRIPTION

Bit 7-0 DATA0<7:0>

15.2.9.2 DATA1_REG: DATA1 DATA REGISTER

| ADDRESS: E0H | | | | TYPE: RW | | | | |
|--------------|----------|----------|----------|----------|----------|----------|----------|----------|
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | DATA1(7) | DATA1(6) | DATA1(5) | DATA1(4) | DATA1(3) | DATA1(2) | DATA1(1) | DATA1(0) |
| DEFAULT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

DESCRIPTION

Bit 7-0 DATA1<7:0>

15.2.9.3 DATA2_REG: DATA2 DATA REGISTER

| ADDRESS: E1H | | | | TYPE: RW | | | | |
|--------------|----------|----------|----------|----------|----------|----------|----------|----------|
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | DATA2(7) | DATA2(6) | DATA2(5) | DATA2(4) | DATA2(3) | DATA2(2) | DATA2(1) | DATA2(0) |
| DEFAULT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

DESCRIPTION

Bit 7-0 DATA2<7:0>

15.2.9.4 DATA3_REG: DATA3 DATA REGISTER

| ADDRESS: E2H | | | | TYPE: RW | | | | |
|--------------|----------|----------|----------|----------|----------|----------|----------|----------|
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | DATA3(7) | DATA3(6) | DATA3(5) | DATA3(4) | DATA3(3) | DATA3(2) | DATA3(1) | DATA3(0) |
| DEFAULT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

DESCRIPTION

Bit 7-0 DATA3<7:0>

Power Management System

15.2.9.5 DATA4_REG: DATA4 DATA REGISTER

| ADDRESS: E3H | | | | TYPE: RW | | | | |
|--------------|----------|----------|----------|----------|----------|----------|----------|----------|
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | DATA4(7) | DATA4(6) | DATA4(5) | DATA4(4) | DATA4(3) | DATA4(2) | DATA4(1) | DATA4(0) |
| DEFAULT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

DESCRIPTION

Bit 7-0 DATA4<7:0>

15.2.9.6 DATA5_REG: DATA5 DATA REGISTER

| ADDRESS: E4H | | | | TYPE: RW | | | | |
|--------------|----------|----------|----------|----------|----------|----------|----------|----------|
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | DATA5(7) | DATA5(6) | DATA5(5) | DATA5(4) | DATA5(3) | DATA5(2) | DATA5(1) | DATA5(0) |
| DEFAULT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

DESCRIPTION

Bit 7-0 DATA5<7:0>

15.2.9.7 DATA6_REG: DATA6 DATA REGISTER

| ADDRESS: E5H | | | | TYPE: RW | | | | |
|--------------|----------|----------|----------|----------|----------|----------|----------|----------|
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | DATA6(7) | DATA6(6) | DATA6(5) | DATA6(4) | DATA6(3) | DATA6(2) | DATA6(1) | DATA6(0) |
| DEFAULT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

DESCRIPTION

Bit 7-0 DATA6<7:0>

15.2.9.8 DATA7_REG: DATA7 DATA REGISTER

| ADDRESS: E6H | | | | TYPE: RW | | | | |
|--------------|----------|----------|----------|----------|----------|----------|----------|----------|
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | DATA7(7) | DATA7(6) | DATA7(5) | DATA7(4) | DATA7(3) | DATA7(2) | DATA7(1) | DATA7(0) |
| DEFAULT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

DESCRIPTION

Bit 7-0 DATA7<7:0>

Power Management System

15.2.9.9 DATA8_REG: DATA8 DATA REGISTER

| ADDRESS: E7H | | | | TYPE: RW | | | | |
|--------------|----------|----------|----------|----------|----------|----------|----------|----------|
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | DATA8(7) | DATA8(6) | DATA8(5) | DATA8(4) | DATA8(3) | DATA8(2) | DATA8(1) | DATA8(0) |
| DEFAULT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

DESCRIPTION

Bit 7-0 DATA8<7:0>

15.2.9.10 DATA9_REG: DATA9 DATA REGISTER

| ADDRESS: E8H | | | | TYPE: RW | | | | |
|--------------|----------|----------|----------|----------|----------|----------|----------|----------|
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | DATA9(7) | DATA9(6) | DATA9(5) | DATA9(4) | DATA9(3) | DATA9(2) | DATA9(1) | DATA9(0) |
| DEFAULT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

DESCRIPTION

Bit 7-0 DATA9<7:0>

15.2.9.11 DATA10_REG: DATA10 DATA REGISTER

| ADDRESS: E9H | | | | TYPE: RW | | | | |
|--------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | DATA10(7) | DATA10(6) | DATA10(5) | DATA10(4) | DATA10(3) | DATA10(2) | DATA10(1) | DATA10(0) |
| DEFAULT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

DESCRIPTION

Bit 7-0 DATA10<7:0>

15.2.9.12 DATA11_REG: DATA11 DATA REGISTER

| ADDRESS: EAH | | | | TYPE: RW | | | | |
|--------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | DATA11(7) | DATA11(6) | DATA11(5) | DATA11(4) | DATA11(3) | DATA11(2) | DATA11(1) | DATA11(0) |
| DEFAULT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Power Management System

DESCRIPTION

Bit 7-0 DATA11<7:0>

15.2.9.13 **DATA12_REG: DATA12 DATA REGISTER**

| ADDRESS: EBH | | | | TYPE: RW | | | | |
|--------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | DATA12(7) | DATA12(6) | DATA12(5) | DATA12(4) | DATA12(3) | DATA12(2) | DATA12(1) | DATA12(0) |
| DEFALULT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

DESCRIPTION

Bit 7-0 DATA12<7:0>

15.2.9.14 **DATA13_REG: DATA13 DATA REGISTER**

| ADDRESS: ECH | | | | TYPE: RW | | | | |
|--------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | DATA13(7) | DATA13(6) | DATA13(5) | DATA13(4) | DATA13(3) | DATA13(2) | DATA13(1) | DATA13(0) |
| DEFALULT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

DESCRIPTION

Bit 7-0 DATA13<7:0>

15.2.9.15 **DATA14_REG: DATA14 DATA REGISTER**

| ADDRESS: EDH | | | | TYPE: RW | | | | |
|--------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | DATA14(7) | DATA14(6) | DATA14(5) | DATA14(4) | DATA14(3) | DATA14(2) | DATA14(1) | DATA14(0) |
| DEFALULT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

DESCRIPTION

Bit 7-0 DATA14<7:0>

Power Management System

15.2.9.16 DATA15_REG: DATA15 DATA REGISTER

| ADDRESS: EDH | | | | TYPE: RW | | | | |
|--------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | DATA15(7) | DATA15(6) | DATA15(5) | DATA15(4) | DATA15(3) | DATA15(2) | DATA15(1) | DATA15(0) |
| DEFAULT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

DESCRIPTION

Bit 7-0 DATA15<7:0>

15.2.9.17 DATA16_REG: DATA16 DATA REGISTER

| ADDRESS: EFH | | | | TYPE: RW | | | | |
|--------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | DATA16(7) | DATA16(6) | DATA16(5) | DATA16(4) | DATA16(3) | DATA16(2) | DATA16(1) | DATA16(0) |
| DEFAULT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

DESCRIPTION

Bit 7-0 DATA16<7:0>

15.2.9.18 DATA17_REG: DATA17 DATA REGISTER

| ADDRESS: F0H | | | | TYPE: RW | | | | |
|--------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | DATA17(7) | DATA17(6) | DATA17(5) | DATA17(4) | DATA17(3) | DATA17(2) | DATA17(1) | DATA17(0) |
| DEFAULT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

DESCRIPTION

Bit 7-0 DATA17<7:0>

15.2.9.19 DATA18_REG: DATA18 DATA REGISTER

| ADDRESS: F1H | | | | TYPE: RW | | | | |
|--------------|------|------|------|----------|------|------|------|------|
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |

Power Management System

| | | | | | | | | |
|---------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| SYMBOL | DATA18(7) | DATA18(6) | DATA18(5) | DATA18(4) | DATA18(3) | DATA18(2) | DATA18(1) | DATA18(0) |
| DEFAULT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

DESCRIPTION

Bit 7-0 DATA18<7:0>

15.2.9.20 **DATA19_REG: DATA19 DATA REGISTER**

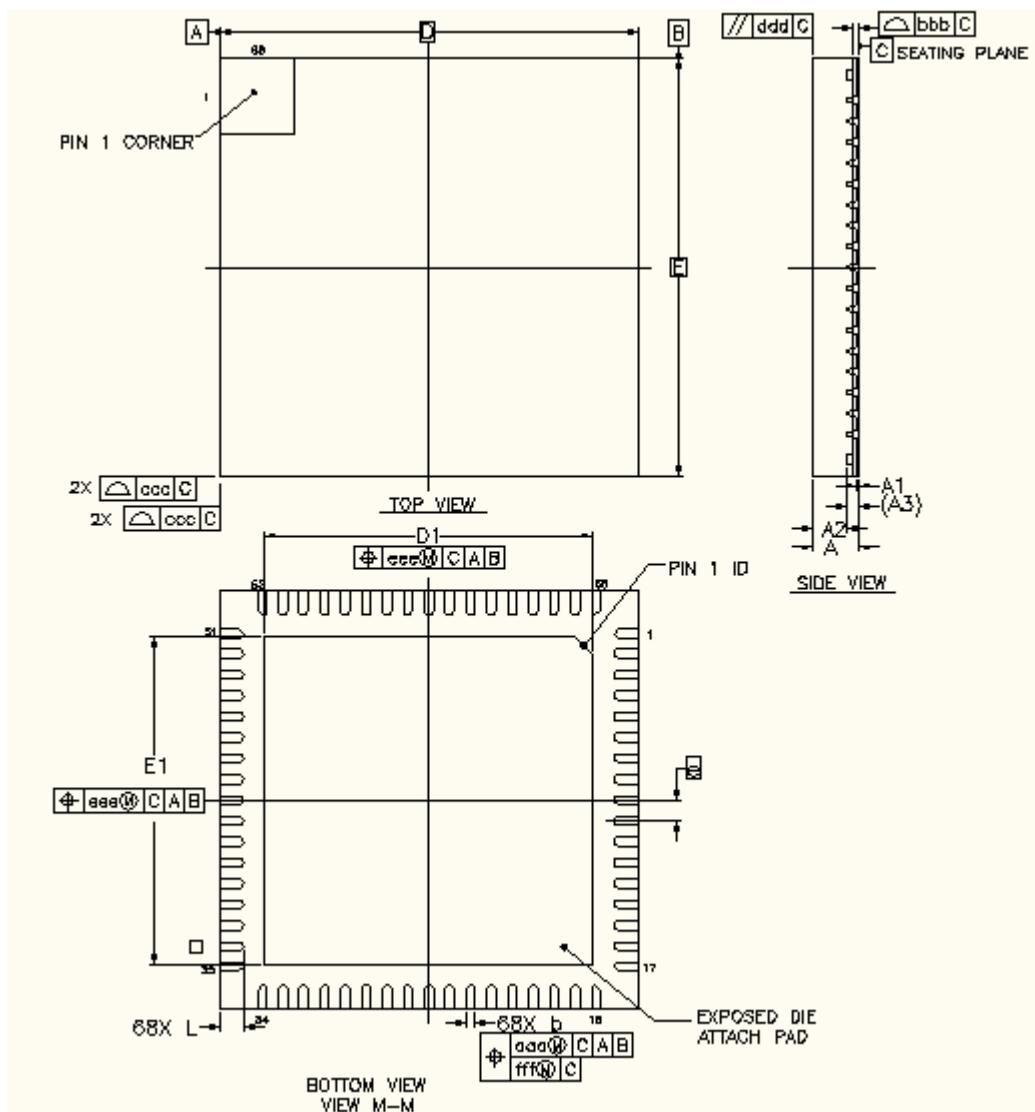
| ADDRESS: F2H | | | | TYPE: RW | | | | |
|--------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | DATA19(7) | DATA19(6) | DATA19(5) | DATA19(4) | DATA19(3) | DATA19(2) | DATA19(1) | DATA19(0) |
| DEFAULT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

DESCRIPTION

Bit 7-0 DATA19<7:0>

Power Management System

16 PACKAGE INFORMATION



QFN68 7mm X 7mm

| DESCRIPTION | SYMBOL | MILLIMETER | | |
|--------------------|--------|------------|----------------------|------|
| | | MIN | NOM | MAX |
| TOTAL THICKNESS | A | 0.70 | 0.75 | 0.80 |
| STAND OFF | A1 | 0 | 0.035 | 0.05 |
| MOLD THICKNESS | A2 | - | 0.55 | 0.57 |
| MATERIAL THICKNESS | A3 | - | 0.203 _{REF} | - |
| PACKAGE SIZE | D | - | 7 _{BSC} | - |

Power Management System

| | | | | |
|----------------------|-----|------|---------------------|------|
| | E | - | 7_{BSC} | - |
| EP SIZE | D1 | 5.39 | 5.49 | 5.59 |
| | E1 | 5.39 | 5.49 | 5.59 |
| LEAD LENGTH | L | 0.30 | 0.4 | 0.50 |
| LEAD PITCH | e | | 0.35 _{BSC} | |
| LEAD WIDTH | b | 0.1 | 0.15 | 0.2 |
| LEAD OSITION OFFSET | aaa | | 0.07 | |
| LEAD COPLANARITY | bbb | | 0.08 | |
| PACKAGE EDGE PROFILE | ccc | | 0.10 | |
| MOLD FLATNESS | ddd | | 0.10 | |
| EP POSITION OFFSET | eee | | 0.10 | |
| | fff | | 0.05 | |

Note:

1. Coplanarity applies to leads, corner leads and die attach pad.
2. Dimension b applies to metalized terminal and is measured between 0.15mm and 0.30mm from the terminal tip. If the terminal has the optional radius on the other end of the terminal, the dimension b should not be measure in that radius area.