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Table of Content

Table of Content.....	3
Figure Index	6
Table Index	9
NOTICE.....	19
Chapter 1 USB2.0 OTG.....	20
1.1 Overview	20
1.2 Block Diagram	20
1.3 USB OTG2.0 Controller	22
1.4 USB OTG2.0 PHY.....	26
1.5 UART BYPASS FUNCITON	28
1.6 Register Description	29
1.7 Interface description	161
1.8 Application Note.....	162
Chapter 2 USB2.0 Host(0)	164
2.1 Overview	164
2.2 Block Diagram	164
2.3 USB Host2.0 PHY	164
2.4 Interface description	164
2.5 Application Note.....	165
Chapter 3 USB2.0 Host(1)	166
3.1 Overview	166
3.2 Block Diagram	166
3.3 USB Host2.0 Controller.....	166
3.4 USB Host2.0 PHY	166
3.5 Register Description	166
3.6 Interface description	166
3.7 Application Note.....	167
Chapter 4 Mobile Storage Host Controller(SDMMC & SDIO)	168
4.1 Overview	168
4.2 Block Diagram	168
4.3 Function Description.....	169
4.4 Register Description	188
4.5 Interface Description	222
4.6 Application Notes	224
Chapter 5 Dynamic Memory Interface (DMC).....	248
5.1 Overview	248
5.2 Block Diagram	249
5.3 Function description	249
5.4 DDR PHY.....	250
5.5 Register description.....	263
5.6 Interface description	437
5.7 Application Notes	438
Chapter 6 Nand Flash Controller(NandC).....	454
6.1 Overview	454
6.2 Block Diagram	455
6.3 Function Description.....	455

6.4 Register Description	456
6.5 Interface Description	578
6.6 Application Notes	580
Chapter 7 Interconnect	590
7.1 Overview	590
7.2 Block Diagram	590
7.3 Function Description(main interconnect)	590
7.4 Register Description(main interconnect).....	596
7.5 Function Description(peri interconnect).....	602
7.6 Register Description(peri interconnect)	602
7.7 Application Notes	604
Chapter 8 Visual Output Processor (VOP).....	606
8.1 Overview	606
8.2 Block Diagram	609
8.3 Function Description.....	609
8.4 Register Description	633
8.5 Timing Diagram	693
8.6 Interface Description	698
8.7 Application Notes	700
Chapter 9 HDMI Transmitter	708
9.1 Overview	708
9.2 Block Diagram	708
9.3 Function Description.....	708
9.4 Register Description	713
9.5 Interface Description	833
9.6 Application Notes	833
Chapter 10 LVDS.....	839
10.1 Overview.....	839
10.2 Block Diagram	839
10.3 Function Description	840
10.4 Register Description.....	844
10.5 Interface Description	852
10.6 Application Notes	852
Chapter 11 eDP Controller	853
11.1 Overview.....	853
11.2 Block Diagram	854
11.3 Function Description	856
11.4 Interface Description	1007
11.5 Application Notes	1008
Chapter 12 MIPI D-PHY	1009
12.1 Overview.....	1009
12.2 Block Diagram	1009
12.3 Function Description	1010
12.4 Test and Contrl modes Description.....	1018
12.5 Application Notes	1070
Chapter 13 MIPI CSI Host Controller	1082
13.1 Overview.....	1082
13.2 Block Diagram	1082

13.3 Function Description	1083
13.4 Register Description.....	1084
Chapter 14 MIPI DSI Host Controller	1094
14.1 Overview.....	1094
14.2 Block Diagram	1094
14.3 Function Description	1095
14.4 Register Description.....	1102
14.5 Application Notes	1136
Chapter 15 Raster Graphic Acceleration (RGA).....	1138
15.1 Overview.....	1138
15.2 Block Diagram	1139
15.3 Function Description	1140
15.4 Register description	1144
15.5 Programming Guide	1164
Chapter 16 VPU Combo	1166
16.1 Overview.....	1166
16.2 Block Diagram	1167
16.3 Function Description	1168
16.4 Register description	1175
16.5 Application Notes	1345
Chapter 17 Image Enhancement Processor (IEP)	1348
17.1 Overview.....	1348
17.2 Block Diagram	1349
17.3 Function description	1350
17.4 Register description	1351
17.5 Application Notes	1385
Chapter 18 Video Input Processor (VIP).....	1386
18.1 Overview.....	1386
18.2 Block Diagram	1386
18.3 Function description	1386
18.4 Register description	1388
18.5 Interface description	1396
18.6 Application Notes	1397
Chapter 19 Encryption and Decryption (Crypto)	1398
19.1 Overview.....	1398
19.2 Block Diagram	1398
19.3 Register description	1398
19.4 Application Note	1419
Chapter 20 Process Voltage Temperature Monitor (PVTM)	1421
20.1 Overview.....	1421
20.2 Block Diagram	1421

Figure Index

Fig. 1-1 USB OTG 2.0 Architecture	20
Fig. 1-2 UTMI interface – Transmit timing for a data packet.....	21
Fig. 1-3 UTMI interface – Receive timing for a data packet	22
Fig. 1-4 USB OTG2.0 Controller Architecture	23
Fig. 1-5 DFIFO single-port synchronous SRAM interface	24
Fig. 1-6 USB OTG 2.0 Controller host mode FIFO address mapping.....	25
Fig. 1-7 USB OTG 2.0 Controller device mode FIFO address mapping.....	26
Fig. 1-8 USB OTG 2.0 PHY Architecture.....	27
Fig. 1-9 USB OTG 2.0 PHY power supply and power up sequence	27
Fig. 1-10 UART Application	29
Fig. 1-11 UART Timing Sequence	29
Fig. 1-12 Resume Timing Sequence	162
Fig. 1-13 Reset a port when receiving	163
Fig. 1-14 Reset a port when transmitting	163
Fig. 2-1 USB HOST 2.0 Architecture	164
Fig. 3-1 USB HOST 2.0 Architecture	166
Fig. 4-1 Host Controller Block Diagram	169
Fig. 4-2 SD/MMC Card-Detect Signal	172
Fig. 4-3 Host Controller Command Path State Machine.....	174
Fig. 4-4 Host Controller Data Transmit State Machine	176
Fig. 4-5 Host Controller Data Receive State Machine.....	178
Fig. 4-6 Dual-Buffer Descriptor Structure	184
Fig. 4-7 Chain Descriptor Structure	184
Fig. 4-8 Descriptor Formats for 32-bit AHB Address Bus Width	184
Fig. 4-9 SD/MMC Card-Detect and Write-Protect	224
Fig. 4-10 SD/MMC Card Termination.....	225
Fig. 4-11 Host Controller Initialization Sequence	227
Fig. 4-12 Voltage Switching Command Flow Diagram.....	236
Fig. 4-13 ACMD41 Argument.....	237
Fig. 4-14 ACMD41 Response(R3)	237
Fig. 4-15 Voltage Switch Normal Scenario	237
Fig. 4-16 Voltage Switch Error Scenario	239
Fig. 4-17 CASES for eMMC 4.5 START bit	240
Fig. 4-18 Clock Generation Unit	242
Fig. 4-19 Card Detection Method 2.....	246
Fig. 4-20 Card Detection Method 4.....	247
Fig. 5-1 Protocol controller architecture	249
Fig. 5-2 PHY controller architecture.....	249
Fig. 5-3 Protocol controller architecture	250
Fig. 5-4 DDR PHY architecture.....	251
Fig. 5-5 DDR PHY master DLL architecture diagram	253
Fig. 5-6 DDR PHY master-slave DLL architecture diagram.....	256
Fig. 5-7 Strobe Gating Requirements During Read Operations	261
Fig. 5-8 DQS gating – passive windowing mode	261
Fig. 5-9 DQS gating – active windowing mode	262
Fig. 5-10 Protocol controller architecture	440
Fig. 5-11 DLL reset requirements.....	443
Fig. 5-12 DLL reset requirements.....	444
Fig. 5-13 Impedance Calibration Circuit	446
Fig. 5-14 I/O cell arrangement with retention	448
Fig. 5-15 Sequence of Events to Enter and Exit Retention.....	448
Fig. 6-1 NandC Block Diagram.....	455
Fig. 6-2 NandC Address Assignment.....	585
Fig. 6-3 NandC DataFormat	585
Fig. 6-4 NandC LLP Data Format.....	588

Fig. 7-1 Block Diagram.....	590
Fig. 7-2 DDR interleaved example.....	596
Fig. 7-3 Idle request	605
Fig. 7-4 DDR timing example	605
Fig. 8-1 VOP Block Diagram	609
Fig. 8-2 RGB data format.....	609
Fig. 8-3 YUV data format.....	610
Fig. 8-4 BPP little/big endian data format.....	610
Fig. 8-5 LCDC Internal DMA	611
Fig. 8-6 VOP Direct Path Interface	611
Fig. 8-7 De-flicker	622
Fig. 8-8 Virtual display	623
Fig. 8-9 X-Mirror and Y-Mirror	623
Fig. 8-10 overlay	624
Fig. 8-11 post scaling timing	626
Fig. 8-12 Transparency Color Key	627
Fig. 8-13 alpha configuration flow	628
Fig. 8-14 Dither down directy	631
Fig. 8-15 frc pattern diagram	632
Fig. 8-16 dsp_out_mode description	633
Fig. 8-17 LCDC RGB interface timing (SDR).....	695
Fig. 8-18 LCDC RGB interface timing (DDR)	696
Fig. 8-19 LCDC MCU interface (i80) timing	697
Fig. 8-20 LCDC DPI Programming flow.....	702
Fig. 8-21 LCDC RGB mode Programming flow	704
Fig. 8-22 LCDC RGB mode Programming flow	705
Fig. 8-23 normal mode left-right type display	706
Fig. 8-24 overlap mode left-right type display	706
Fig. 8-25 command mode flow	707
Fig. 9-1 HDMI TX Block Diagram.....	708
Fig. 9-2 HDMI Video Data Processing	709
Fig. 9-3 HDMI Video Processing Timing	709
Fig. 9-4 HDMI Audio Data Processing Diagram	710
Fig. 9-5 HDMI Audio Clock Regeneration Model	712
Fig. 10-1 LVDS Block Diagram.....	839
Fig. 10-2 LVDS in SoC.....	840
Fig. 10-3 LVDS output data timing	840
Fig. 10-4 LVDS h_bp timing diagram	844
Fig. 11-1 eDP TX controller Block Diagram	854
Fig. 11-2 DP_TX clock domain.....	855
Fig. 11-3 eDP PHY block diagram	855
Fig. 11-4 eDP in SoC.....	856
Fig. 11-5 Block diagram of Video Interface.....	856
Fig. 11-6 Video interface signals for slave mode – YCbCr 4:4:4 and YCbCr 4:2:2 pixel bit format	857
Fig. 11-7 10-bpc mode pixel bit format.....	857
Fig. 11-8 8-bpc pixel bit format	858
Fig. 11-9 Active symbol count implementation.....	858
Fig. 11-10 The structure of video FIFO for video in slave mode	858
Fig. 11-11 First part structure of video FIFO	859
Fig. 11-12 Double byte active symbol count implementation.....	859
Fig. 11-13 Audio data interface block diagram	859
Fig. 11-14 M_VID Generation	860
Fig. 11-15 Transfer unit.....	869
Fig. 11-16 TU in Main Link vs. Video Stream	870
Fig. 11-17 Symbol BE and BS vs. Video Stream	870
Fig. 11-18 Main Link Attribute Insertion in Main Link	870

Fig. 11-19 Inter-lane Skewing	871
Fig. 11-20 Audio_TimeStamp Packet	872
Fig. 11-21 Data Mapping within the Four Byte Payload of an Audio_Stream Packet	873
Fig. 11-22 AUX CH Request Transaction Data Format	876
Fig. 11-23 AUX CH Reply Transaction Data Format	876
Fig. 11-24 Diagram of AUX CH Module.....	877
Fig. 11-25 Action Flow Sequences of the Source upon Hot Plug Detect Event	877
Fig. 11-26 Link Training Initial and Clock Recovery Training	878
Fig. 11-27 Equalizer Training	879
Fig. 11-28 High-speed Link Down-spreading Frequency vs, Time.....	880
Fig. 11-29 interface timing of SRAM interface	880
Fig. 11-30 Interrupt Status Registers and Mask Registers.....	924
Fig. 12-1 MIPI D-PHY detailed block diagram.....	1009
Fig. 12-2 MIPI D-PHY Initialization from Shutdown to Idle Modes	1012
Fig. 12-3 Power-Up Sequence for Slave Operation.....	1015
Fig. 12-4 HS Data Transfer Sequence	1016
Fig. 12-5 HS Data Transfer State Diagram.....	1017
Fig. 12-6 Escape Mode Sequences State Diagram	1018
Fig. 12-7 Testability Interface Timing Diagram	1019
Fig. 12-8 Two Consecutive Test Codes Handling	1020
Fig. 12-9 PLL System-Level Block Diagram.....	1071
Fig. 12-10 Resistor Tuning Circuitry.....	1076
Fig. 13-1 MIPI CSI-2 Host Controller architecture.....	1082
Fig. 14-1 MIPI Controller architecture	1094
Fig. 14-2 24bpp APB Pixel to Byte Organization	1097
Fig. 14-3 18 bpp APB Pixel to Byte Organization	1098
Fig. 14-4 16 bpp APB Pixel to Byte Organization	1098
Fig. 14-5 12 bpp APB Pixel to Byte Organization	1098
Fig. 14-6 8bpp APB Pixel to Byte Organization	1099
Fig. 14-7 Command Transmission Periods within the Image Area.....	1099
Fig. 14-8 Location in the Image Area.....	1101
Fig. 15-1 RGA2 Block Diagram	1139
Fig. 15-2 RGA2 in SOC.....	1139
Fig. 15-3 RGA Input Data Format	1140
Fig. 15-4 RGA Dither effect	1141
Fig. 15-5 RGA Gradient Fill	1143
Fig. 15-6 HDMI TX Software Main Sequence Diagram	1164
Fig. 15-7 RGA command line and command counter	1165
Fig. 15-8 RGA command sync generation	1165
Fig. 16-1 VPU Combo in SOC	1167
Fig. 16-2 VPU Combo Block Diagram	1168
Fig. 16-3 structure of two-level page table	1171
Fig. 16-4 Dataflow of HW performs entropy decoding in video decoder	1172
Fig. 16-5 Dataflow of SW performs entropy decoding in video decoder	1174
Fig. 16-6 HEVC Common Configuration Flow	1346
Fig. 17-1 IEP block diagram	1349
Fig. 18-1 VIP block diagram	1386
Fig. 18-2 Timing diagram for VIP when vsync low active	1387
Fig. 18-3 Timing diagram for VIP when vsync high active	1387
Fig. 18-4 Timing diagram for VIP when href high active	1387
Fig. 18-5 Timing diagram for VIP when href low active	1387
Fig. 18-6 Timing diagram for VIP when Y data first	1387
Fig. 18-7 Timing diagram for VIP when U data first	1387
Fig. 18-8 CCIR656 timing	1388
Fig. 18-9 Raw Data or JPEG Timing	1388
Fig. 19-1 Crypto Architecture	1398

Table Index

Table 1-1 USB OTG 2.0 PHY power supply timing parameter	27
Table 1-2 USB OTG 2.0 Interface Description	161
Table 2-1 USB HOST 2.0 Interface Description	164
Table 3-1 USB HOST 2.0 Interface Description	166
Table 4-1 Bits in Interrupt Status Register.....	171
Table 4-2 Auto-Stop Generation.....	179
Table 4-3 Non-data Transfer Commands and Requirements	180
Table 4-4 Bits in IDMAC DES0 Element	184
Table 4-5 Bits in IDMAC DES1 Element	185
Table 4-6 Bits in IDMAC DES2 Element	186
Table 4-7 Bits in IDMAC DES3 Element	186
Table 4-8 IOMUX Settings for SDMMC.....	222
Table 4-9 IOMUX Settings for SDIO0	222
Table 4-10 IOMUX Settings for SDIO1	223
Table 4-11 IOMUX Settings for eMMC	224
Table 4-12 Recommended Usage of use_hold_reg	226
Table 4-13 Command Settings for No-Data Command.....	229
Table 4-14 Command Setting for Single or Multiple-Block Read	231
Table 4-15 Command Settings for Single or Multiple-Block Write	232
Table 4-16 PBL and Watermark Levels	242
Table 4-17 Configuration for SDMMC Clock Generation.....	242
Table 4-18 Configuration for SDIO0 Clock Generation	243
Table 4-19 Configuration for SDIO1 Clock Generation	244
Table 4-20 Configuration for eMMC Clock Generation	244
Table 4-21 Register for SDMMC Card Detection Method 3	246
Table 5-1 DDR PHYtrim and test MDLL control	254
Table 5-2 charge pump current trim in dll_ctrl	254
Table 5-3 DLL digital test control in dll_ctrl.....	254
Table 5-4 DLL analog test control in dll_ctrl	254
Table 5-5 bias generator trim in dll_ctrl	255
Table 5-6 MDLL feedback trim in dll_ctrl	255
Table 5-7 MDLL bypass mode frequency range in dll_ctrl.....	255
Table 5-8 fdtrm control bits in dll_ctrl	256
Table 5-9 DDR PHYMSDLL control for trim and test.....	257
Table 5-10 MSDLL digital test control in dll_ctrl.....	257
Table 5-11 MSDLL analog test control in dll_ctrl	258
Table 5-12 MSDLL lock detector enable in dll_ctrl	259
Table 5-13 slave auto_startup bypass in dll_ctrl	259
Table 5-14 slave DLL phase trim in dll_ctrl	259
Table 5-15 phase selection for dqs gating	261
Table 5-16 dynamic strobe drift indicators.....	262
Table 6-1 NandC Address Mapping	456
Table 6-2 NandC0 Interface Description	578
Table 6-3 NandC1 Interface Description	579
Table 6-4 NandC Interface Connection.....	580
Table 6-5 NandC Page/Spare size for flash	586
Table 7-1 Master NIU	590
Table 7-2 slave NIU	591
Table 7-3 Clock and Power domain.....	592
Table 7-4 DDR configuration	594
Table 7-5 DDR Stride	594
Table 7-6 Service module	596
Table 7-7 Service_bus block.....	596
Table 7-8 Service_core block.....	597
Table 7-9 Service_dmac block	597

Table 7-10 Service_gpu block.....	597
Table 7-11 Service_hevc block	597
Table 7-12 Service_peri block.....	597
Table 7-13 Service_vio block.....	597
Table 8-1 alpha blending mode settings	627
Table 8-2 LCDC0 RGB interface(SDR) signal timing constant.....	695
Table 8-3 LCDC0 RGB interface (DDR) signal timing constant.....	696
Table 8-4 LCDC1 RGB interface signal timing constant	697
Table 8-5 LCDC0 RGB interface signal timing constant	697
Table 8-6 LCDC1 RGB interface signal timing constant	698
Table 8-7 Gather configuration for all format	701
Table 8-8 effective immediately register table.....	707
Table 9-1 HDMI Supported Input Video Formats.....	709
Table 9-2 HDMI TX I2S 2 Channel Audio Sampling Frequency	711
Table 9-3 HDMI TX I2S 8 Channel Audio Sampling Frequency	711
Table 9-4 HDMI SPDIF Sampling Frequency at Each Video Format	711
Table 9-5 HDMI CTS and N table.....	712
Table 10-1 MSB mapping relationship (single channel mode)	840
Table 10-2 MSB mapping relationship (double channel mode)	841
Table 11-1 Brief function description of each module in top level	854
Table 11-2 Examples of M_AUD and N_AUD	861
Table 11-3 Video Data Mapping to Main Link.....	863
Table 11-4 Control Symbols for Framing	869
Table 11-5 Header Bytes of Audio_Stream Packet	872
Table 11-6 Audio_Stream Packet over the Main Link for One or Two or Four Channel Audio	873
Table 11-7 Audio Stream Packet over the Main Link for Three to Eight Channel Audio.....	873
Table 11-8 Bit Definition of the Payload of an Audio_Stream Packet with IEC60958-like Coding	874
Table 11-9 HDCP Key Arrangement	880
Table 11-10 DP_TX Version (DP_TX_VERSION)	891
Table 11-11 Function Enable Register 1(FUNC_EN_1)	892
Table 11-12 Function Enable Register 2 (FUNC_EN_2)	892
Table 11-13 Video Control Register 1 (VIDEO_CTL_1)	893
Table 11-14 Video Control Register 2 (VIDEO_CTL_2).....	893
Table 11-15 Video Control Register 3 (VIDEO_CTL_3).....	894
Table 11-16 Video Control Register 4 (VIDEO_CTL_4).....	894
Table 11-17 Video Control Register 8 (VIDEO_CTL_8).....	895
Table 11-18 Video Control Register 10 (VIDEO_CTL_10)	895
Table 11-19 Total Line Low Byte Configure Register (TOTAL_LINE_CFG_L)	896
Table 11-20 Total Line High Byte Configure Register (TOTAL_LINE_CFG_H).....	896
Table 11-21 Active Line Low Byte Configure Register (ACTIVE_LINE_CFG_L).....	896
Table 11-22 Active Line High Byte Configure Register (ACTIVE_LINE_CFG_H)	897
Table 11-23 Vertical Front Porch Configure Register (V_F_PORCH_CFG)	897
Table 11-24 Vertical Sync Width Configure Register (V_SYNC_WIDTH_CFG).....	897
Table 11-25 Vertical Back Porch Configure Register (V_B_PORCH_CFG).....	897
Table 11-26 Total Pixel Low Byte Configure Register (TOTAL_PIXEL_CFG_L)	898
Table 11-27 Total Pixel High Byte Configure Register (TOTAL_PIXEL_CFG_H).....	898
Table 11-28 Active Pixel Low Byte Configure Register (ACTIVE_PIXEL_CFG_L)	898
Table 11-29 Active Pixel High Byte Configure Register (ACTIVE_PIXEL_CFG_H)	899
Table 11-30 Horizon Front Porch Low Byte Configure Register (H_F_PORCH_CFG_L)	899
Table 11-31 Horizon Front Porch High Byte Configure Register (H_F_PORCH_CFG_H)	899
Table 11-32 Horizon Sync Width Low Byte Configure Register (H_SYNC_CFG_L).....	900
Table 11-33 Horizon Sync Width High Byte Configure Register (H_SYNC_CFG_H)	900
Table 11-34 Horizon Back Porch Low Byte Configure Register (H_B_PORCH_CFG_L)	900
Table 11-35 Horizon Back Porch High Byte Configure Register (H_B_PORCH_CFG_H)	900
Table 11-36 Video Status Register (VIDEO_STATUS).....	901

Table 11-37 Total Line Status Low Byte Register (TOTAL_LINE_STA_L)	901
Table 11-38 Total Line Status High Byte Register (TOTAL_LINE_STA_H)	901
Table 11-39 Active Line Status Low Byte Register (ACTIVE_LINE_STA_L)	902
Table 11-40 Active Line Status High Byte Register (ACTIVE_LINE_STA_H)	902
Table 11-41 Vertical Front Porch Status Register (V_F_PORCH_STA)	902
Table 5-42 Vertical Sync Width Status Register (V_SYNC_STA)	902
Table 11-43 Vertical Back Porch Status Register (V_B_PORCH_STA)	903
Table 11-44 Total Pixel Status Low Byte Register (TOTAL_PIXEL_STA_L)	903
Table 11-45 Total Pixel Status High Byte Register (TOTAL_PIXEL_STA_H)	903
Table 11-46 Active Pixel Status Low Byte Register (ACTIVE_PIXEL_STA_L)	903
Table 11-47 Active Pixel Status High Byte Register (ACTIVE_PIXEL_STA_H)	904
Table 11-48 Horizon Front Porch Status Low Byte Register (H_F_PORCH_STA_L)	904
Table 11-49 Horizon Front Porch Status High Byte Register (H_F_PORCH_STA_H)	904
Table 11-50 Horizon Sync Width Status Low Byte Register (H_SYNC_STA_L)	904
Table 11-51 Horizon Sync Width Status High Byte Register (H_SYNC_STA_H)	905
Table 11-52 Horizon Back Porch Status Low Byte Register (H_B_PORCH_STA_L)	905
Table 11-53 Horizon Back Porch Status High Byte Register (H_B_PORCH_STA_H)	905
Table 11-54 SPDIF Audio Control Register 0 (SPDIF_AUDIO_CTL_0)	905
Table 11-55 DP Audio Control Register 1 (DP_AUDIO_CTL_1)	906
Table 11-56 SPDIF Audio Status Register 0 (SPDIF_AUDIO_STA_0)	906
Table 11-57 Audio SPDIF Status Register 1 (SPDIF_AUDIO_STA_1)	907
Table 11-58 SPDIF Error Threshold Register (SPDIF_ERR_THRD)	907
Table 11-59 SPDIF Error Counter Register (SPDIF_ERR_CNT)	907
Table 11-60 Audio BIST Control Register (AUDIO_BIST_CTL)	908
Table 11-61 Audio Input Clock Frequency Counter Register_1(AUD_FREQ_CNT_1)	908
Table 11-62 Audio Input Clock Frequency Counter Register_2(AUD_FREQ_CNT_2)	908
Table 11-63 PLL control Register_1(PLL_REG_1)	908
Table 11-64 PLL control Register_2(PLL_REG_2)	909
Table 11-65 PLL control Register_3(PLL_REG_3)	909
Table 11-66 PLL control Register_4(PLL_REG_4)	910
Table 5-67 PLL control Register_5(PLL_REG_5)	910
Table 11-68 PLL control Register_mac(PLL_REG_mac)	910
Table 11-69 Freq Register (FREQ_IN_REG)	911
Table 11-70 Freq Register (P_REG_FRQ)	911
Table 11-71 Freq Register (P_REG_FRQ_COUNT_RDY)	911
Table 11-72 Freq Register (P_BAND_DEC_RESET)	912
Table 11-73 SSC control Register_2(SSC_REG)	912
Table 11-74 TX_COMMON Register (TX_COMMON)	912
Table 11-75 TX_COMMON2 Register (TX_COMMON2)	913
Table 11-76 TX_COMMON3 Register (TX_COMMON3)	913
Table 11-77 DP_AUX Register (DP_AUX)	914
Table 11-78 DP_BIAS Register (DP_BIAS)	914
Table 11-79 DP_TEST Register (DP_TEST)	915
Table 11-80 DP_PD Register (DP_PD)	915
Table 11-81 DP_RESERV1 Register (DP_RESERV1)	916
Table 11-82 DP_RESERV2 Register (DP_RESERV2)	916
Table 11-83 AVI InfoFrame Packet Data Byte (AVI_DB1 ~ AVI_DB13)	917
Table 11-84 Audio InfoFrame Packet Data Byte (AUDIO_DB1 ~ AUDIO_DB10)	917
Table 11-85 InfoFrame Packet Type Code (IF_TYPE)	917
Table 11-86 InfoFrame Packet Data Byte (IF_PKT_DB1~25)	917
Table 11-87 MPEG Source InfoFrame Packet Data Byte (MPEG_DB1 ~ MPEG_DB10)	918
Table 11-88 Reuse SPD Header Bytes registers(HB0—HB3)	918
Table 11-89 REUSE SPD Parity Bytes registers(PB0—PB3)	918
Table 11-90 PSR Frame Update Control Register	918
Table 11-91 VSC Shadow Data Bytes Register	919
Table 11-92 VSC Shadow Parity Bytes Register	919
Table 11-93 Audio I2S Channel Status Register 1 (AUDIO_I2S_CH_STA1)	919

Table 11-94 Audio I2S Channel Status Register 2 (AUDIO_I2S_CH_STA2)	919
Table 11-95 Audio I2S Channel Status Register 3 (AUDIO_I2S_CH_STA3)	920
Table 11-96 Audio I2S Channel Status Register 4 (AUDIO_I2S_CH_STA4)	920
Table 11-97 Audio I2S Channel Status Register 5 (AUDIO_I2S_CH_STA5)	920
Table 11-98 Lane Map Register (LANE_MAP).....	921
Table 11-99 Analog Control Register 2 (ANALOG_CTL_2).....	921
Table 11-100 Hidden Register (INT_STATE_0)	921
Table 11-101 Interrupt Status Register (INT_STATE_1).....	922
Table 11-102 Common Interrupt Status Register 1 (COMMON_INT_STA_1).....	922
Table 11-103 Common Interrupt Status Register 2 (COMMON_INT_STA_2).....	924
Table 11-104 Common Interrupt Status Register 3 (COMMON_INT_STA_3).....	925
Table 11-105 Common Interrupt Status Register 4 (COMMON_INT_STA_4).....	926
Table 11-106 SPDIF Biphase Interrupt Status Register (SPDIF_BIPHASE_INT_STA).....	926
Table 11-107 DisplayPort Interrupt Status Register (DP_INT_STA).....	927
Table 11-108 Interrupt Mask Register (COMMON_INT_MASK_1).....	927
Table 11-109 Interrupt Mask Register (COMMON_INT_MASK_2).....	928
Table 11-110 Interrupt Mask Register (COMMON_INT_MASK_3).....	928
Table 11-111 Interrupt Mask Register (COMMON_INT_MASK_4).....	928
Table 11-112 DP Interrupt Mask Register (DP_INT_STA_MASK).....	928
Table 11-113 Interrupt Control Register (INT_CTL).....	929
Table 11-114 HDCP Status Register (HDCP_STA)	929
Table 11-115 HDCP Control Register 0 (HDCP_CTL_0)	929
Table 11-116 HDCP Control Register 1 (HDCP_CTL_1)	930
Table 11-117 HDCP AKSV Register 0(AKSV0)	931
Table 11-118 HDCP AKSV Register 1(AKSV1)	931
Table 11-119 HDCP AKSV Register 2(AKSV2)	931
Table 11-120 HDCP AKSV Register 3(AKSV3)	931
Table 11-121 HDCP AKSV Register 4(AKSV4)	931
Table 11-122 HDCP AN Register 0(AN0).....	931
Table 11-123 HDCP AN Register 1(AN1).....	932
Table 11-124 HDCP AN Register 2(AN2).....	932
Table 11-125 HDCP AN Register 3(AN3).....	932
Table 11-126 HDCP AN Register 4(AN4).....	932
Table 11-127 HDCP AN Register 5(AN5).....	932
Table 11-128 HDCP AN Register 6(AN6).....	932
Table 11-129 HDCP AN Register 7(AN7).....	933
Table 11-130 BKSV Register 0(BKSV0)	933
Table 11-131 HDCP BKSV Register 1(BKSV1)	933
Table 11-132 HDCP BKSV Register 2(BKSV2)	933
Table 11-133 HDCP BKSV Register 3(BKSV3)	933
Table 11-134 HDCP BKSV Register 4(BKSV4)	934
Table 11-135 HDCP RI Register 0(RI0)	934
Table 11-136 HDCP RI Register 1(RI1)	934
Table 11-137 Receiver BCAPS Register (HW_RX_CAPS).....	934
Table 11-138 HDCP Receiver BINFO Register 0(HW_RX_BINFO_0).....	934
Table 11-139 HDCP Receiver BINFO Register 1(HW_RX_BINFO_1).....	934
Table 11-140 HDCP Debug Control Register (HW_SKIP_RPT_ZERO_DEV)	935
Table 11-141 SPSRAM Access Configure Register 1 (SPSRAM_CFG_1)	935
Table 11-142 HDCP auth debug register (HDCP_AUTH_DBG)	935
Table 11-143 HDCP enc debug register (HDCP_ENC_DBG)	935
Table 11-144 HDCP Embedded "Blue Screen" Content Registers 0 (HDCP_VID_0).....	936
Table 11-145 HDCP Embedded "Blue Screen" Content Registers 1 (HDCP_VID_1).....	936
Table 11-146 HDCP Embedded "Blue Screen" Content Registers 2 (HDCP_VID_2).....	936
Table 11-147 HDCP AM0 Register 0 (HDCP_AM0_0).....	936
Table 11-148 HDCP AM0 Register 1 (HDCP_AM0_1).....	936
Table 11-149 HDCP AM0 Register 2 (HDCP_AM0_2).....	937
Table 11-150 HDCP AM0 Register 3 (HDCP_AM0_3).....	937

Table 11-151 HDCP AM0 Register 4, reg (HDCP_AM0_4)	937
Table 11-152 HDCP AM0 Register 5 (HDCP_AM0_5).....	937
Table 11-153 HDCP AM0 Register 6 (HDCP_AM0_6).....	937
Table 11-154 HDCP AM0 Register 7 (HDCP_AM0_7).....	938
Table 11-155 HDCP Wait R0 Timing Register (HW_WRITE_AKSV_WAIT)	938
Table 11-156 LINK_CHECK_TIMER Register (LINK_CHECK_TIMER)	938
Table 11-157 HDCP Repeater Ready Wait Timer Register (HW_RPTR_RDY_TIMER)	938
Table 11-158 READY_POLL_TIMER Register (READY_POLL_TIMER)	939
Table 11-159 HDCP HIDDEN Register (HDCP_HIDDEN_REG).....	939
Table 11-160 HDCP B INITIAIL VALUE Register (HDCP_B_INIT_RND0).....	939
Table 11-161 HDCP B INITIAIL VALUE Register (HDCP_B_INIT_RND1).....	939
Table 11-162 HDCP B INITIAIL VALUE Register (HDCP_B_INIT_RND2).....	940
Table 11-163 HDCP B INITIAIL VALUE Register (HDCP_B_INIT_RND3).....	940
Table 11-164 HDCP B INITIAIL VALUE Register (HDCP_B_INIT_RND4).....	940
Table 11-165 HDCP B INITIAIL VALUE Register (HDCP_B_INIT_RND5).....	940
Table 11-166 HDCP B INITIAIL VALUE Register (HDCP_B_INIT_RND6).....	940
Table 11-167 HDCP B INITIAIL VALUE Register (HDCP_B_INIT_RND7).....	941
Table 11-168 HDCP B INITIAIL VALUE Register (HDCP_B_INIT_RND8).....	941
Table 11-169 HDCP K INITIAIL VALUE Register (HDCP_K_INIT_RND0).....	941
Table 11-170 HDCP K INITIAIL VALUE Register (HDCP_K_INIT_RND1).....	941
Table 11-171 HDCP K INITIAIL VALUE Register (HDCP_K_INIT_RND2).....	941
Table 11-172 HDCP K INITIAIL VALUE Register (HDCP_K_INIT_RND3).....	942
Table 11-173 HDCP K INITIAIL VALUE Register (HDCP_K_INIT_RND4).....	942
Table 11-174 HDCP K INITIAIL VALUE Register (HDCP_K_INIT_RND5).....	942
Table 11-175 HDCP K INITIAIL VALUE Register (HDCP_K_INIT_RND6).....	942
Table 11-176 HDCP K INITIAIL VALUE Register (HDCP_K_INIT_RND7).....	943
Table 11-177 HDCP K INITIAIL VALUE Register (HDCP_K_INIT_RND8).....	943
Table 11-178 HDCP K INITIAIL VALUE Register (HDCP_K_INIT_RND9).....	943
Table 11-179 HDCP K INITIAIL VALUE Register (HDCP_K_INIT_RND10)	943
Table 11-180 System Control Register #1 (SYS_CTL_1).....	943
Table 11-181 DP System Control Register #2 (SYS_CTL_2)	944
Table 11-182 DP System Control Register #3 (SYS_CTL_3)	944
Table 11-183 DP System Control Register #4 (SYS_CTL_4)	945
Table 11-184 DP Video Control Register (DP_VID_CTL)	946
Table 11-185 DP Audio Control Register (DP_AUD_CTL)	947
Table 11-186 Packet Send Control Register (PKT_SEND_CTL)	947
Table 11-187 DisplayPort HDCP Control Register (DP_HDCP_CTL).....	948
Table 11-188 SPDIF Phase 1 Control Register (SPDIF_PHASE1_CTL_0)	949
Table 11-189 SPDIF Phase 1 Control ENABLE Register 0 (SPDIF_PHASE1_CTL_1)	949
Table 11-190 SPDIF Phase 2 Control Register 0 (SPDIF_PHASE2_CTL_0).....	950
Table 11-191 SPDIF Phase 2 Control Register 1 (SPDIF_PHASE2_CTL_1)	951
Table 11-192 SPDIF Phase 3 Control Register 0 (SPDIF_PHASE3_CTL_0)	951
Table 11-193 SPDIF Phase 3 Control Register 1 (SPDIF_PHASE3_CTL_1)	952
Table 11-194 DP Main Link Bandwidth Setting Register (LINK_BW_SET)	952
Table 11-195 DP Main Link Lane Count Register (LANE_COUNT_SET).....	952
Table 11-196 DP Training Pattern Set Register (DP_TRAINING_PTN_SET)	953
Table 11-197 DP Lane 0 Link Training Control Register (DP_LN0_LINK_TRAINING_CTL)	953
Table 11-198 DP Lane 1 Link Training Control Register (DP_LN1_LINK_TRAINING_CTL)	954
Table 11-199 DP Lane 2 Link Training Control Register (DP_LN2_LINK_TRAINING_CTL)	955
Table 11-200 DP Lane 3 Link Training Control Register (DP_LN3_LINK_TRAINING_CTL)	956
Table 11-201 DP HW LINK TRAINING_CONTROL Register (DP_HW_LINK_TRAINING_CTL)	957
Table 11-202 DP Debug Register Register #1 (DP_DEBUG_CTL)	958
Table 11-203 DP HPD De-glitch Low Byte Register (HPD_DEGLITCH_L)	959
Table 11-204 DP HPD De-glitch High Byte Register (HPD_DEGLITCH_H)	959
Table 11-205 DP POLLING_PERIOD Register (POLLING_PERIOD)	959
Table 11-206 DP Link Debug Control Register (DP_LINK_DEBUG_CTL)	959
Table 11-207 DP SINK_COUNT Register (SINK_COUNT)	960

Table 11-208 DP IRQ_VECTOR Register (IRQ_VECTOR).....	960
Table 11-209 DP_LINK_STATUS0 Register (DP_LINK_STATUS0)	960
Table 11-210 DP_LINK_STATUS1 Register (DP_LINK_STATUS1)	961
Table 11-211 DP ALIGN_STATUS Register (ALIGN_STATUS).....	961
Table 11-212 DP DP_SINK_STATUS Register (DP_SINK_STATUS)	961
Table 11-213 M_VID Configure Register #0 (M_VID_0).....	961
Table 11-214 DP M_VID Configure Register #1 (M_VID_1).....	962
Table 11-215 DP M_VID Configure Register #2 (M_VID_2).....	962
Table 11-216 DP N_VID Configure Register #0 (N_VID_0).....	962
Table 11-217 DP N_VID Configure Register #1 (N_VID_1).....	962
Table 11-218 DP N_VID Configure Register #2 (N_VID_2).....	962
Table 11-219 DP M_VID_MON register (M_VID_MON).....	963
Table 11-220 DP FIFO Threshold Register (DP_VIDEO_FIFO_THRD)	963
Table 11-221 DP GNS Control Register (DP_GNS_CTRL).....	963
Table 11-222 DP Audio Margin Register (DP_AUDIO_MARGIN)	964
Table 11-223 DP M_AUD_MON register (M_AUD_MON).....	964
Table 11-224 DP M_AUD Configure Register #0 (M_AUD_0)	964
Table 11-225 DP M_AUD Configure Register #1 (M_AUD_1)	965
Table 11-226 DP M_AUD Configure Register #2 (M_AUD_2)	965
Table 11-227 DP N_AUD Configure Register #0 (N_AUD_0).....	965
Table 11-228 DP N_AUD Configure Register #1 (N_AUD_1).....	965
Table 11-229 DP N_AUD Configure Register #2 (N_AUD_2).....	965
Table 11-230 DP M Value Calculation Control Register (DP_M_CAL_CTL).....	965
Table 11-231 DP M_VID Value Calculation Control Register (M_VID_GEN_FILTER_TH)	966
Table 11-232 DP M_AUD Value Calculation Control Register (M_AUD_GEN_FILTER_TH)	966
Table 11-233 AUX Channel Access Status Register (AUX_CH_STA)	966
Table 11-234 AUX Channel Access Error Code Register (AUX_ERR_NUM)	967
Table 11-235 DP AUX CH DEFER Control Register (AUX_CH_DEFER_CTL)	967
Table 11-236 DP AUX RX Command Register (AUX_RX_COMM)	968
Table 11-237 DP Buffer Data Count Register (BUFFER_DATA_CTL).....	968
Table 11-238 DP AUX Channel Control Register 1 (AUX_CH_CTL_1).....	968
Table 11-239 DP AUX CH Address Register #0 (AUX_ADDR_7_0)	968
Table 11-240 DP AUX CH Address Register #1 (AUX_ADDR_15_8)	969
Table 11-241 DP AUX CH Address Register #2 (AUX_ADDR_19_16).....	969
Table 11-242 DP AUX CH Control Register 2 (AUX_CH_CTL_2)	969
Table 11-243 DP AUX Buffer Data Register (BUF_DATA_0 ~ BUF_DATA_15)	970
Table 11-244 General control register (SOC_GENERAL_CTL).....	970
Table 11-245 ATE test control register (ATE_TEST_CTL)	970
Table 11-246 ATE test status register (ATE_TEST_STATUS)	971
Table 11-247 ATE test error counter register (ATE_TEST_ERR_CNT)	971
Table 11-248 DP test 80bit pattern0 (DP_TEST_80B_PATTERN0)	971
Table 11-249 DP test 80bit pattern1 (DP_TEST_80B_PATTERN1)	971
Table 11-250 DP test 80bit pattern2 (DP_TEST_80B_PATTERN2)	971
Table 11-251 DP test HBR2 SR COUNT (DP_TEST_HBR2_PATTERN)	972
Table 11-252 Audio Control register (AUD_CTL)	972
Table 11-253 CRC check control register (CRC_CON)	972
Table 11-254 CRC Result (CRC_RESULT)	972
Table 11-255 Analog Control Register 5 (ANALOG_CTL_5)	972
Table 11-256 Analog Control Register 6 (ANALOG_CTL_6)	973
Table 11-257 Analog Control Register 7 (ANALOG_CTL_7)	973
Table 11-258 Analog Control Register 8 (ANALOG_CTL_8)	973
Table 11-259 Analog Control Register 9 (ANALOG_CTL_9)	974
Table 11-260 Analog Control Register 10 (ANALOG_CTL_10)	974
Table 11-261 Analog Control Register 11 (ANALOG_CTL_11)	974
Table 11-262 Analog Control Register 12 (ANALOG_CTL_12)	974
Table 11-263 Analog Control Register 13 (ANALOG_CTL_13)	974
Table 11-264 Analog Control Register 14 (ANALOG_CTL_14)	975

Table 11-265 Analog Control Register 15 (ANALOG_CTL_15)	975
Table 11-266 Analog Control Register 16 (ANALOG_CTL_16)	975
Table 11-267 Analog Control Register 17 (ANALOG_CTL_17)	975
Table 11-268 Analog Control Register 18 (ANALOG_CTL_18)	976
Table 11-269 Analog Control Register 19 (ANALOG_CTL_19)	976
Table 11-270 Analog Control Register 20 (ANALOG_CTL_20)	976
Table 11-271 Analog Control Register 21 (ANALOG_CTL_21)	976
Table 11-272 Analog Control Register 22 (ANALOG_CTL_22)	976
Table 11-273 Analog Control Register 23 (ANALOG_CTL_23)	977
Table 11-274 Analog Control Register 24 (ANALOG_CTL_24)	977
Table 11-275 Analog Control Register 25 (ANALOG_CTL_25)	977
Table 11-276 Analog Control Register 26 (ANALOG_CTL_26)	977
Table 11-277 Analog Control Register 27 (ANALOG_CTL_27)	978
Table 11-278 Analog Control Register 28 (ANALOG_CTL_28)	978
Table 11-279 Analog Control Register 29 (ANALOG_CTL_29)	978
Table 11-280 Analog Control Register 30 (ANALOG_CTL_30)	978
Table 11-281 Analog Control Register 31 (ANALOG_CTL_31)	979
Table 11-282 Analog Control Register 32 (ANALOG_CTL_32)	979
Table 11-283 Analog Control Register 33 (ANALOG_CTL_33)	979
Table 11-284 Analog Control Register 34 (ANALOG_CTL_34)	979
Table 11-285 Analog Control Register 35 (ANALOG_CTL_35)	979
Table 11-286 Analog Control Register 36 (ANALOG_CTL_36)	980
Table 11-287 Analog Control Register 37 (ANALOG_CTL_37)	980
Table 11-288 Analog Control Register 38 (ANALOG_CTL_38)	980
Table 11-289 Analog Control Register 39 (ANALOG_CTL_39)	980
Table 11-290 Analog Control Register 40 (ANALOG_CTL_40)	981
Table 11-291 Analog Control Register 41 (ANALOG_CTL_41)	981
Table 11-292 Analog Control Register 42 (ANALOG_CTL_42)	981
Table 11-293 Analog Control Register 43 (ANALOG_CTL_43)	982
Table 11-294 Analog Control Register 44 (ANALOG_CTL_44)	982
Table 11-295 Analog Control Register 45 (ANALOG_CTL_45)	982
Table 11-296 Analog Control Register 46 (ANALOG_CTL_46)	982
Table 11-297 Analog Control Register 47 (ANALOG_CTL_47)	982
Table 11-298 Analog Control Register 48 (ANALOG_CTL_48)	983
Table 11-299 Analog Control Register 49 (ANALOG_CTL_49)	983
Table 11-300 I2S_CTRL (I2S_CTRL)	983
Table 11-301 I2S_CH_SWAP (I2S_CH_SWAP)	984
Table 11-302 I2S_CH_CTRL (I2S_CH_CTRL)	984
Table 11-303 I2S_CH_CTRL1 (I2S_CH_CTRL1)	984
Table 11-304 LINK_POLICY (LINK_POLICY)	984
Table 12-1 Register Config For D-PHY Mode Select	1011
Table 12-2 Frequency Ranges	1013
Table 12-3 Power-Up Sequence Timings	1016
Table 12-4 Possible Escape Mode Sequences for Data Lanes	1018
Table 12-5 Configuration and Test Interface Signals	1020
Table 12-6 Supported Test Codes for Test Mode	1021
Table 12-7 LP Driver Wake Up Timer Counter after Exiting ULPS Test Data	1023
Table 12-8 LP Driver Wake Up Timer Counter after Exiting ULPS Testdout	1024
Table 12-9 Timer Control Test Data	1024
Table 12-10 Timer Control Testout	1024
Table 12-11 Delay between Enable Calibration and Starting Calibration Timer Control testData	1024
Table 12-12 Delay between Enable Calibration and Starting Calibration Timer Control Testdout	1024
Table 12-13 Relinquish Control if PHY is Configured as TX Test Data	1024
Table 12-14 Relinquish Control if PHY is Configured as TX Testdout	1025
Table 12-15 Tta-go Timer Counter Test Data	1025

Table 12-16 Tta-go Timer Counter Testdout.....	1025
Table 12-17 Tta-sure Timer Counter Test Data.....	1025
Table 12-18 Tta-sure Timer Counter Testdout	1025
Table 12-19 Turnaround Request Delay Control Test Data	1025
Table 12-20 Turnaround Request Delay Control Test Testdout.....	1026
Table 12-21 Delay between HS Receiver Power On and Enabling Calibration Timer Control Test Data	1026
Table 12-22 Delay between HS Receiver Power On and Enabling Calibration Timer Control Testdout	1026
Table 12-23 Relinquish Control when PHY is Configured as RX Test Data:	1026
Table 12-24 Relinquish Control when PHY is Configured as RX Testdout	1026
Table 12-25 Stop State Watchdog Timer Control Test Data	1027
Table 12-26 Stop State Watchdog Timer Control Testdout Set 0	1027
Table 12-27 Stop State Watchdog Timer Control Testdout Set 1	1027
Table 12-28 Stop State Watchdog Timer Control Testdout Set 2	1027
Table 12-29 Stop State Watchdog Timer Enable and Contention Detection Test Data	1027
Table 12-30 Stop State Watchdog Timer Enable and Contention Detection Testdout	1028
Table 12-31 BIST Mode Testdout.....	1028
Table 12-32 BIST Mode testdout.....	1028
Table 12-33 PLL Bias Current Selector/Filter Capacitance Control/VCO Control TestData	1028
Table 12-34 PLL Bias Current Selector/Filter Capacitance Control/VCO Control Testdout	1029
Table 12-35 PLL CP Control / PLL Lock Bypass for Initialization and for ULP TestData....	1029
Table 12-36 PLL CP Control / PLL Lock Bypass for Initialization and for ULP Testdout	1029
Table 12-37 PLL LPF and CP Control TestData	1030
Table 12-38 PLL LPF and CP Control Testdout.....	1030
Table 12-39 PLL Digital Testability TestData	1030
Table 12-40 PLL Digital Testability Testdout	1031
Table 12-41 PLL Phase Error Control TestData	1031
Table 12-42 PLL Phase Error Control Testdout	1031
Table 12-43 PLL Phase Error Control Testdout	1031
Table 12-44 PLL Locking Filter TestData	1032
Table 12-45 PLL Locking Filter Testdout	1032
Table 12-46 PLL Unlocking Filter TestData	1032
Table 12-47 PLL Unlocking Filter Testdout	1032
Table 12-48 PLL Input Divider Ratio TestData	1032
Table 12-49 PLL Input Divider Ratio Testdout	1032
Table 12-50 PLL Loop Divider Ratio TestData	1033
Table 12-51 PLL Loop Divider Ratio Testdout	1033
Table 12-52 PLL Loop Divider Ratio Testdout	1033
Table 12-53 PLL Input and Loop Divider Ratios Control TestData.....	1033
Table 12-54 PLL Input and Loop Divider Ratios Control Testdout.....	1034
Table 12-55 Bandgap and Bias Control TestData	1034
Table 12-56 Bandgap and Bias Control Testdout.....	1034
Table 12-57 Termination Resistor Control TestData	1035
Table 12-58 Termination Resistor Control Testdout	1035
Table 12-59 Termination Resistor Control Testdout	1035
Table 12-60 AFE/BIAS/Bandgap Analog Programmability TestData	1036
Table 12-61 AFE/BIAS/Bandgap Analog Programmability Testdout	1037
Table 12-62 AFE/BIAS/Bandgap Analog Programmability Testdout	1037
Table 12-63 HS TX and Bias Power on Control of Clock Lane TestData	1037
Table 12-64 HS TX and Bias Power on Control of Clock Lane Testdout	1037
Table 12-65 LP RX Control of Clock Lane TestData	1038
Table 12-66 LP RX Control of Clock Lane Testdout	1038
Table 12-67 LP TX Control of Clock Lane TestData	1039
Table 12-68 LP TX Control of Clock Lane Testdout	1039
Table 12-69 LP TX Control of Clock Lane TestData	1040
Table 12-70 LP TX Control of Clock Lane Testdout	1040

Table 12-71 HS RX Control of Clock Lane TestData	1040
Table 12-72 HS RX Control of Clock Lane Testdout	1041
Table 12-73 CLKP/CLKN Swap for Clock Lane + Tclk_miss Control TestData	1041
Table 12-74 CLKP/CLKN Swap for Clock Lane + Tclk_miss Control Testdout.....	1041
Table 12-75 Calibration Machine Outputs Observability of Clock Lane Testdout	1042
Table 12-76 H S TX and Bias Power on Control of Lane 0 TestData.....	1042
Table 12-77 H S TX and Bias Power on Control of Lane 0 Testdout	1042
Table 12-78 L P RX Control of Lane 0 TestData.....	1043
Table 12-79 L P RX Control of Lane 0 Testdout.....	1043
Table 12-80 LP TX Control of Lane 0 TestData.....	1044
Table 12-81 LP TX Control of Lane 0 Testdout.....	1044
Table 12-82 LP TX Control of Lane 0 TestData.....	1044
Table 12-83 LP TX Control of Lane 0 Testdout.....	1045
Table 12-84 HS RX Control of Lane 0 TestData.....	1045
Table 12-85 HS RX Control of Lane 0 Testdout	1046
Table 12-86 DATAP/DATAN Swap for Lane 0 TestData	1046
Table 12-87 DATAP/DATAN Swap for Lane 0 Testdout.....	1046
Table 12-88 HS RX Lane 0 Outputs and Calibration Errors Observability Testdout.....	1046
Table 12-89 B IST Control and Observability on Lane 0 TestData	1047
Table 12-90 BIST Control and Observability on Lane 0 Testdout	1047
Table 12-91 HS TX and Bias Power on Control of Lane 1 TestData.....	1047
Table 12-92 HS TX and Bias Power on Control of Lane 1 Testdout	1048
Table 12-93 L P RX Control of Lane 1 TestData.....	1048
Table 12-94 L P RX Control of Lane 1 Testdout.....	1049
Table 12-95 H P TX Control of Lane 1 TestData	1049
Table 12-96 H P TX Control of Lane 1 Testdout.....	1050
Table 12-97 L P TX Control of Lane 1 TestData.....	1050
Table 12-98 L P TX Control of Lane 1 Testdout	1050
Table 12-99 H S RX Control of Lane 1 TestData:	1050
Table 12-100 H S RX Control of Lane 1 Testdout	1051
Table 12-101 DATAP/DATAN Swap for Lane 1 TestData.....	1051
Table 12-102 DATAP/DATAN Swap for Lane 1 Testdout	1052
Table 12-103 HS RX Lane 1 Outputs and Calibration Errors Observability Testdout	1052
Table 12-104 BIST Control and Observability on Lane 1 TestData	1052
Table 12-105 BIST Control and Observability on Lane 1 Testdout.....	1052
Table 12-106 HS TX Clock Lane Request State Time (TLP) Control TestData	1053
Table 12-107 HS TX Clock Lane Request State Time (TLP) Control Testdout	1053
Table 12-108 HS TX Clock Lane Prepare State Time (TCLK-prepare) Control TestData... .	1053
Table 12-109 HS TX Clock Lane Prepare State Time (TCLK-prepare) Control Testdout... .	1054
Table 12-110 HS TX Clock Lane HS-Zero State Time (TCLK-zero) Control TestData.....	1054
Table 12-111 HS TX Clock Lane HS-Zero State Time (TCLK-zero) Control Testdout.....	1054
Table 12-112 HS TX Clock Lane Trail State Time (TCLK-TRAIL) Control TestData	1054
Table 12-113 HS TX Clock Lane Trail State Time (TCLK-TRAIL) Control Testdout	1055
Table 12-114 HS TX Clock Lane Exit State Time (THS-EXIT) Control TestData	1055
Table 12-115 HS TX Clock Lane Exit State Time (THS-EXIT) Control Testdout.....	1055
Table 12-116 HS TX Clock Lane Clock Post Time (TCLK-POST) Control TestData.....	1056
Table 12-117 HS TX Clock Lane Clock Post Time (TCLK-POST) Control Testdout	1056
Table 12-118 HS TX Data Lane Request State Time (TLP) Control TestData	1056
Table 12-119 HS TX Data Lane Request State Time (TLP) Control Testdout	1056
Table 12-120 HS TX Data Lanes Prepare State Time (THS-PREPARE) Control TestData .	1057
Table 12-121 HS TX Data Lanes Prepare State Time (THS-PREPARE) Control Testdout..	1057
Table 12-122 HS TX TX Data Lanes THS-ZERO State Time (THS-ZERO) Control TestData	1057
Table 12-123 HS TX TX Data Lanes THS-ZERO State Time (THS-ZERO) Control Testdout	1058
Table 12-124 HS TX Data Lanes Trail State Time (THS-TRAIL) Control TestData	1058
Table 12-125 HS TX Data Lanes Trail State Time (THS-TRAIL) Control Testdout	1058
Table 12-126 HS TX Data Lanes Exit State Time (THS-EXIT) Control TestData	1058
Table 12-127 HS TX Data Lanes Exit State Time (THS-EXIT) Control Testdout	1059

Table 12-128 HS RX Data Lanes Settle State Time (THS-settle) Control TestData.....	1059
Table 12-129 HS RX Data Lanes Settle State Time (THS-settle) Control Testdout.....	1059
Table 12-130 HS RX Data Lanes Settle State Time (THS-settle) Control TestData.....	1059
Table 12-131 HS RX Data Lanes Settle State Time (THS-settle) Control Testdout.....	1060
Table 12-132 LP RX Control of Lane 2 TestData	1060
Table 12-133 LP RX Control of Lane 2 Testdout	1061
Table 12-134 LP TX Control of Lane 2 TestData	1061
Table 12-135 LP TX Control of Lane 2 Testdout	1062
Table 12-136 LP TX Control of Lane 2 TestData	1062
Table 12-137 LP TX Control of Lane 2 Testdout	1062
Table 12-138 HS RX Control of Lane 2 TestData	1062
Table 12-139 HS RX Control of Lane 2 Testdout	1063
Table 12-140 DATAP/DATAN Swap for Lane 2 TestData	1064
Table 12-141 DATAP/DATAN Swap for Lane 2 Testdout	1064
Table 12-142 HS RX Lane 2 Outputs and Calibration Errors Observability Testdout	1064
Table 12-143 BIST Control and Observability on Lane 2 TestData	1064
Table 12-144 BIST Control and Observability on Lane 2 Testdout.....	1065
Table 12-145 HS TX and Bias Power on Control of Lane 3 Testdata	1065
Table 12-146 HS TX and Bias Power on Control of Lane 3 Testdout	1065
Table 12-147 LP RX Control of Lane 3TestData.....	1066
Table 12-148 LP RX Control of Lane 3 Testdout	1066
Table 12-149 LP TX Control of Lane 3 TestData	1067
Table 12-150 LP TX Control of Lane 3 Testdout	1067
Table 12-151 LP TX Control of Lane 3 TestData	1067
Table 12-152 LP TX Control of Lane 3 Testdout	1068
Table 12-153 HS RX Control of Lane 3 TestData	1068
Table 12-154 HS RX Control of Lane 3 Testdout	1069
Table 12-155 DATAP/DATAN Swap for Lane 3 TestData	1069
Table 12-156 DATAP/DATAN Swap for Lane 3 Testdout	1069
Table 12-157 HS RX Lane 3 Outputs and Calibration Errors Observability Testdout	1069
Table 12-158 BIST Control and Observability on Lane 3 Test Data	1070
Table 12-159 BIST Control and Observability on Lane 3 Testdout.....	1070
Table 12-160 VCO Ranges	1071
Table 12-161 Division Ratios for the Attachable PLL	1072
Table 12-162 PLL CP and LPF Control Bits	1072
Table 12-163 PLL Settings for 27 MHz Reference Clock and Selectable Ranges	1073
Table 12-164 DC Specifications.....	1077
Table 12-165 Switching Characteristics	1079
Table 12-166 AC Specifications.....	1080
Table 13-1 Supported Camera Settings.....	1083
Table 13-2 Errors Identified by the CSI-2 Host Controller	1083
Table 14-1 Color table	1095
Table 15-1 RGA ROP Boolean operations	1144
Table 16-1 H264 decoder external memory accessing contexts	1172
Table 16-2 VP8 decoder external memory accessing contexts	1174
Table 16-3 H264 encoder external memory accessing contexts	1175
Table 16-4 vp8 encoder external memory accessing contexts	1175

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Chapter 1 USB2.0 OTG

1.1 Overview

USB OTG 2.0 is a Dual-Role Device controller, which supports both device and host functions and is fully compliant with OTG Supplement to USB2.0 specification, and support high-speed (480Mbps), full-speed (12Mbps), low-speed (1.5Mbps) transfer.

USB OTG 2.0 is optimized for portable electronic devices, point-to-point applications (no hub, direct connection to device) and multi-point applications to devices. USB OTG 2.0 interface supports both device and host functions and is fully compliant with OTG Supplement to USB2.0 specification, and support high-speed (480Mbps), full-speed (12Mbps), low-speed (1.5Mbps) transfer. It is optimized for portable electronic device, point-to-point applications (no hub, direct connection to device) and multi-point applications to devices.

The USB OTG 2.0 supports following features:

- Compliant with the OTG Supplement to the USB2.0 Specification
- Operates in High-Speed and Full-Speed mode
- Support 9 channels in host mode
- 9 Device mode endpoints in addition to control endpoint 0, 4 in, 3 out and 2 IN/OUT
- Built-in one 1024x35 bits FIFO
- Internal DMA with scatter/gather function
- Supports packet-based, dynamic FIFO memory allocation for endpoints for flexible, efficient use of RAM
- Support dynamic FIFO sizing
- Support Battery Charge
- Support UART Bypass function

1.2 Block Diagram

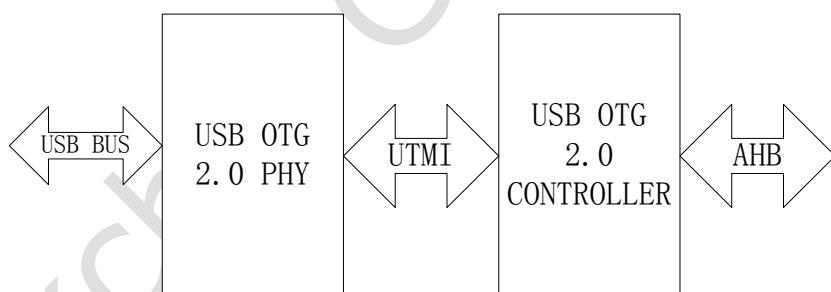


Fig. 1-1 USB OTG 2.0 Architecture

Fig.19-1 shows the architecture of USB OTG 2.0. It is broken up into two separate units: USB OTG 2.0 controller and USB OTG 2.0 PHY. The two units are interconnected with UTMI interface.

1.2.1 USB OTG 2.0 Controller Function

The USB OTG 2.0 Controller controls SIE (Serial Interface Engine) logic, the endpoint logic, the channel logic and the internal DMA logic.

The SIE logic contains the USB PID and address recognition logic, and other sequencing and state machine logic to handle USB packets and transactions. Generally the SIE Logic is required for any USB implementation while the number and types of endpoints will vary as function of application and performance requirements.

The endpoint logic contains the endpoint specific logic: endpoint number recognition, FIFOs and FIFO control, etc.

The channel Logic contains the channel tasks schedule, FIFOs and FIFO control, etc.

The internal DMA logic controls data transaction between system memory and USB FIFOs.

1.2.2 USB OTG 2.0 PHY Function

The USB OTG 2.0 PHY handles the low level USB protocol and signaling. This includes features such as; data serialization and deserialization, bit stuffing and clock recovery and synchronization. The primary focus of this block is to shift the clock domain of the data from the USB 2.0 rate to the frequency of UTMI clock which is 30MHz.

1.2.3 UTMI Interface

- Transmit

Transmit must be asserted to enable any transmissions.

The USB OTG2.0 CONTROLLER asserts TXValid to begin a transmission and negates TXValid to end a transmission. After the USB OTG2.0 CONTROLLER asserts TXValid it can assume that the transmission has started when it detects TXReady asserted.

The USB OTG2.0 CONTROLLER assumes that the USB OTG2.0 PHY has consumed a data byte if TXReady and TXValid are asserted.

The USB OTG2.0 CONTROLLER must have valid packet information (PID) asserted on the Data In bus coincident with the assertion of TXValid. Depending on the USB OTG2.0 PHY implementation, TXReady may be asserted by the Transmit State Machine as soon as one CLK after the assertion of TXValid. TXValid and TXReady are sampled on the rising edge of CLK.

The Transmit State Machine does NOT automatically generate Packet ID's (PIDs) or CRC. When transmitting, the USB OTG2.0 CONTROLLER is always expected to present a PID as the first byte of the data stream and if appropriate, CRC as the last bytes of the data stream.

The USB OTG2.0 CONTROLLER must use LineState to verify a Bus Idle condition before asserting TXValid in the TX Wait state.

The state of TXReady in the TX Wait and Send SYNC states is undefined. An MTU implementation may prepare for the next transmission immediately after the Send EOP state and assert TXReady in the TX Wait state. An MTU implementation may also assert TXReady in the Send SYNC state. The first assertion of TXReady is Macrocell implementation dependent. The USB OTG2.0 CONTROLLER must prepare DataIn for the first byte to be transmitted before asserting TXValid.

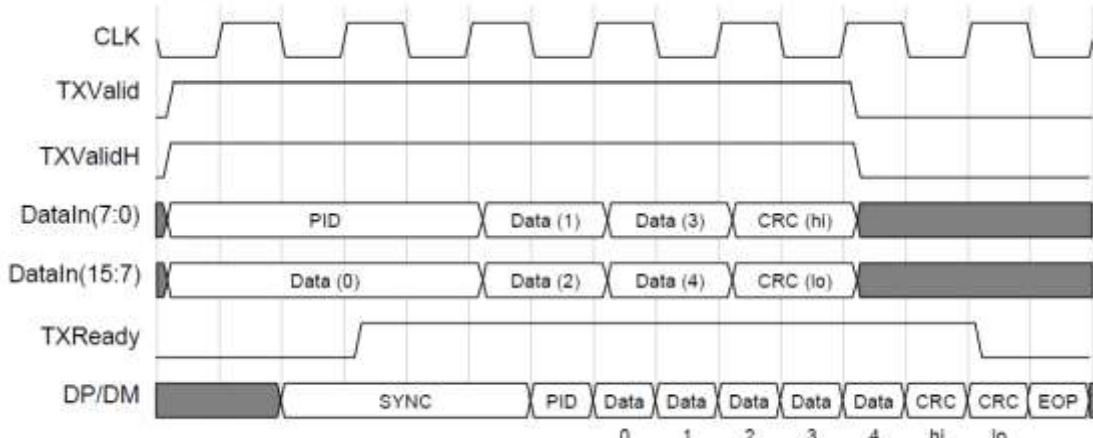


Fig. 1-2 UTMI interface – Transmit timing for a data packet

- Receive

RXActive and RXValid are sampled on the rising edge of CLK.

In the RX Wait state the receiver is always looking for SYNC.

The USB OTG 2.0 PHY asserts RXActive when SYNC is detected (Strip SYNC state).

The USB OTG 2.0 PHY negates RXActive when an EOP is detected (Strip EOP state).

When RxActive is asserted, RXValid will be asserted if the RX Holding Register is full.

RXValid will be negated if the RX Holding Register was not loaded during the previous byte time.

This will occur if 8 stuffed bits have been accumulated.

The USB OTG2.0 Controller must be ready to consume a data byte if RXActive and RXValid are asserted (RX Data state).

In FS mode, if a bit stuff error is detected then the Receive State Machine will negate RXActive

and RXValid, and return to the RX Wait state.

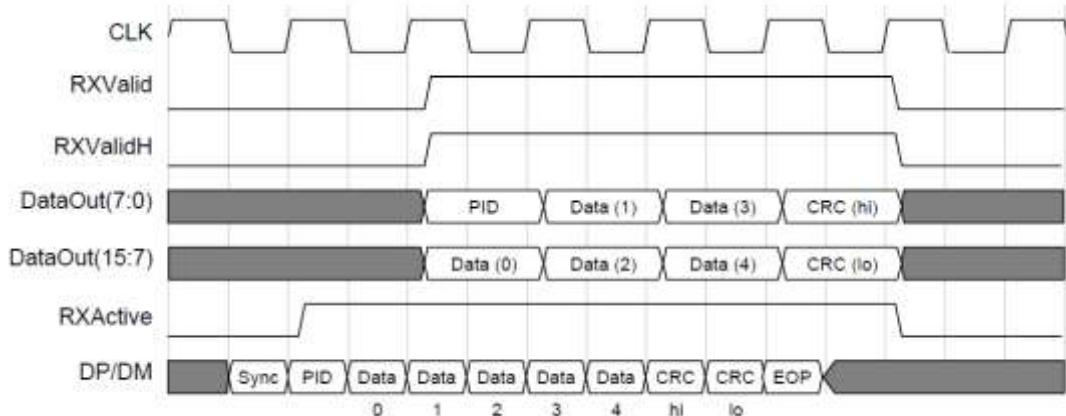


Fig. 1-3 UTMI interface – Receive timing for a data packet

1.3 USB OTG2.0 Controller

Fig.2-4 shows the main components and flow of the USB OTG 2.0 controller system.

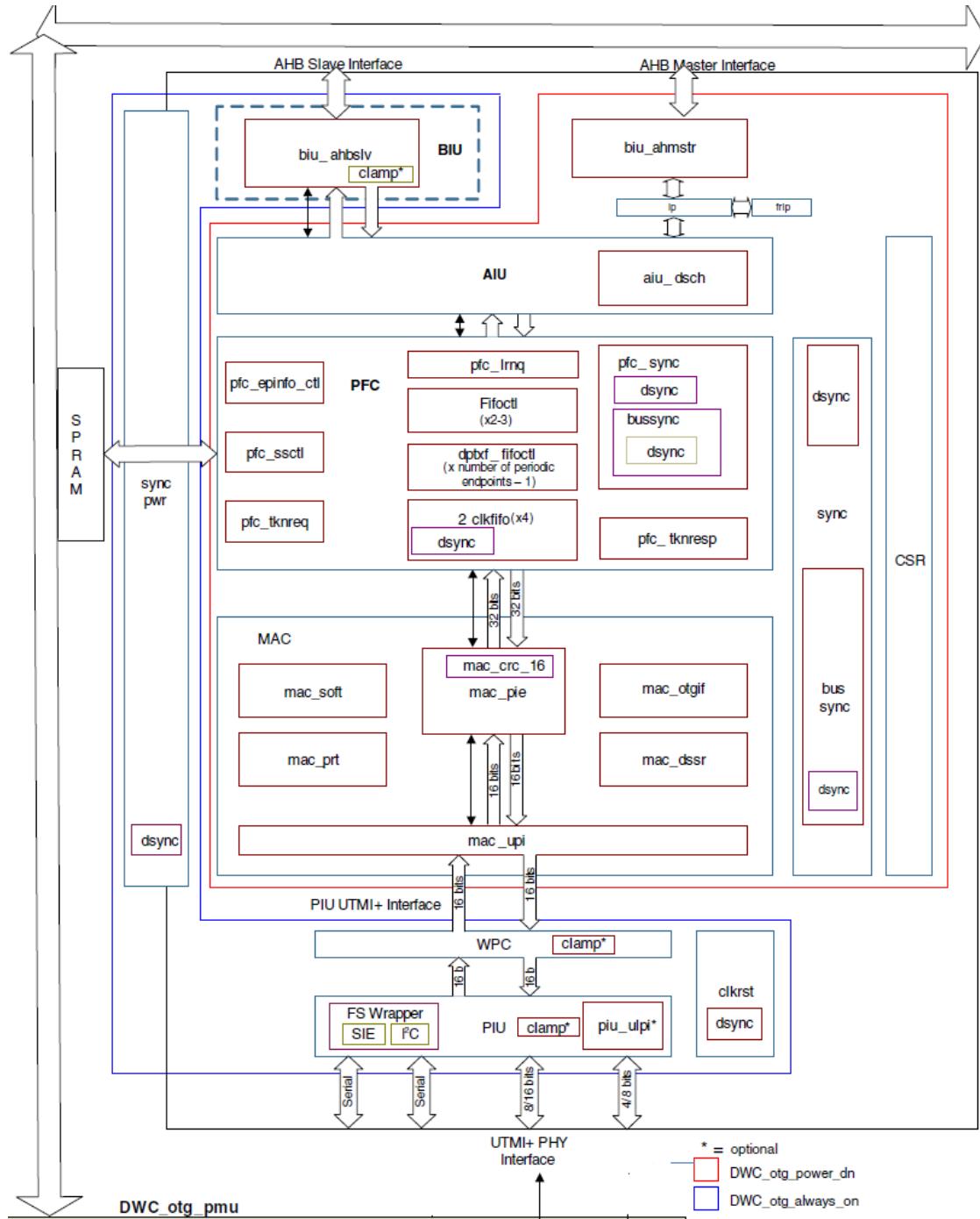


Fig. 1-4 USB OTG2.0 Controller Architecture

1). AHB Slave Bus Interface Unit (BIUS)

The AHB Slave interface unit converts AHB cycles to CSR write/read, Data-FIFO read/write, and DFIFO push/pop signals.

2) Control and Status Registers (CSR)

The CSR block resides in the AHB clock domain, and contains all registers except the Power and Clock Gating Control Register (PCGCCTL) and bits 31:29 of the Core Interrupt register (GINTSTS).

3) Application Interface Unit (AIU)

The application Interface Unit (AIU) consists of the following interfaces:

- AHB Master
- AHB Slave
- Packet FIFO Controller
- Control and Status registers

4). DMA Scheduler (DSCH)

This block is used only in DMA mode. It controls the transfer of data packets between the system memory and the USB OTG 2.0 Controller for both Internal and External DMA.

5). Packet FIFO Controller (PFC)

Several FIFOs are used in Device and Host modes to store data inside the core before transmitting it on either the AHB or the USB. PFC connect the Data FIFO interface to an industry-standard, single-port synchronous SRAM. Address, write data, and control outputs are driven late by the USB OTG 2.0 Controller, but in time to meet the SRAM setup requirements. Input read data is expected late from the SRAM and registered inside the core before being used.

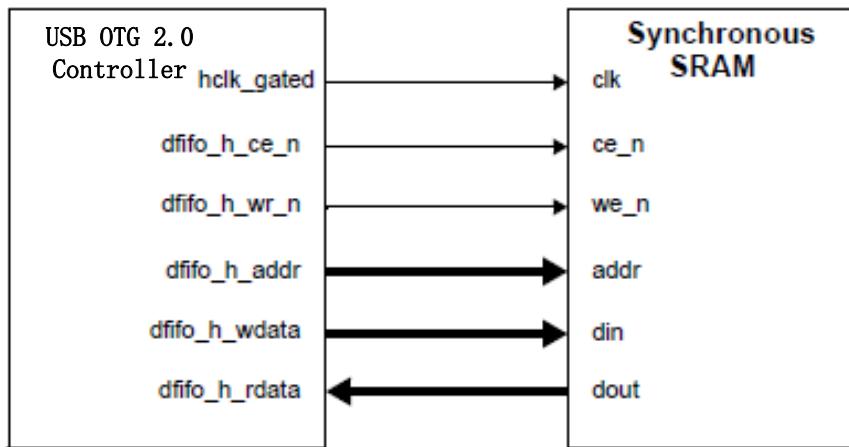


Fig. 1-5 DFIFO single-port synchronous SRAM interface

6).Media Access Controller (MAC)

The Media Access Controller (MAC) module handles USB transactions, and device, host, and OTG protocols.

7) PHY Interface Unit (PIU)

The core uses 16-bit UTMI+ Interface.

8) Wakeup and Power Controller (WPC)

When the USB is suspended or the session is not valid, the PHY is driven into Suspend mode and the PHY clock is stopped to reduce PHY and the core power consumption. To reduce power consumption further, the core also supports AHB clock gating and partial power-down.

1.3.1 Host Architecture

The host uses one transmit FIFO for all non-periodic OUT transactions and one transmit FIFO for all periodic OUT transactions. These transmit FIFOs are used as transmit buffers to hold the data (payload of the transmit packet) to be transmitted over USB.

The host pipes the USB transactions through Request queues (one for periodic and one for non-periodic). Each entry in the Request - queue holds the IN or OUT channel number along with other information to perform a transaction on the USB. The order in which the requests are written into the queue determines the sequence of transactions on the USB. The host processes the periodic Request queue first, followed by the non-periodic Request queue, at the beginning of each (micro) frame.

The host uses one Receive-FIFO for all periodic and non-periodic transactions. The FIFO is used as a Receive-buffer to hold the received data (payload of the received packet) from the USB until it is transferred to the system memory. The status of each packet received also goes into the FIFO. The status entry holds the IN channel number along with other information, such as received byte count and validity status, to perform a transaction on the AHB.

1.3.2 Device Architecture

The core uses Dedicated Transmit FIFO Operation. In this mode, there are individual transmit FIFOs for each IN endpoint.

The OTG device uses a single receive FIFO to receive the data for all the OUT endpoints. The

receive FIFO holds the status of the received data packet, such as byte count, data PID and the validity of the received data. The DMA or the application reads the data out of the receive FIFO as it is received.

1.3.3 FIFO Mapping

- Fig.19-6 shows FIFO mapping in Host mode.

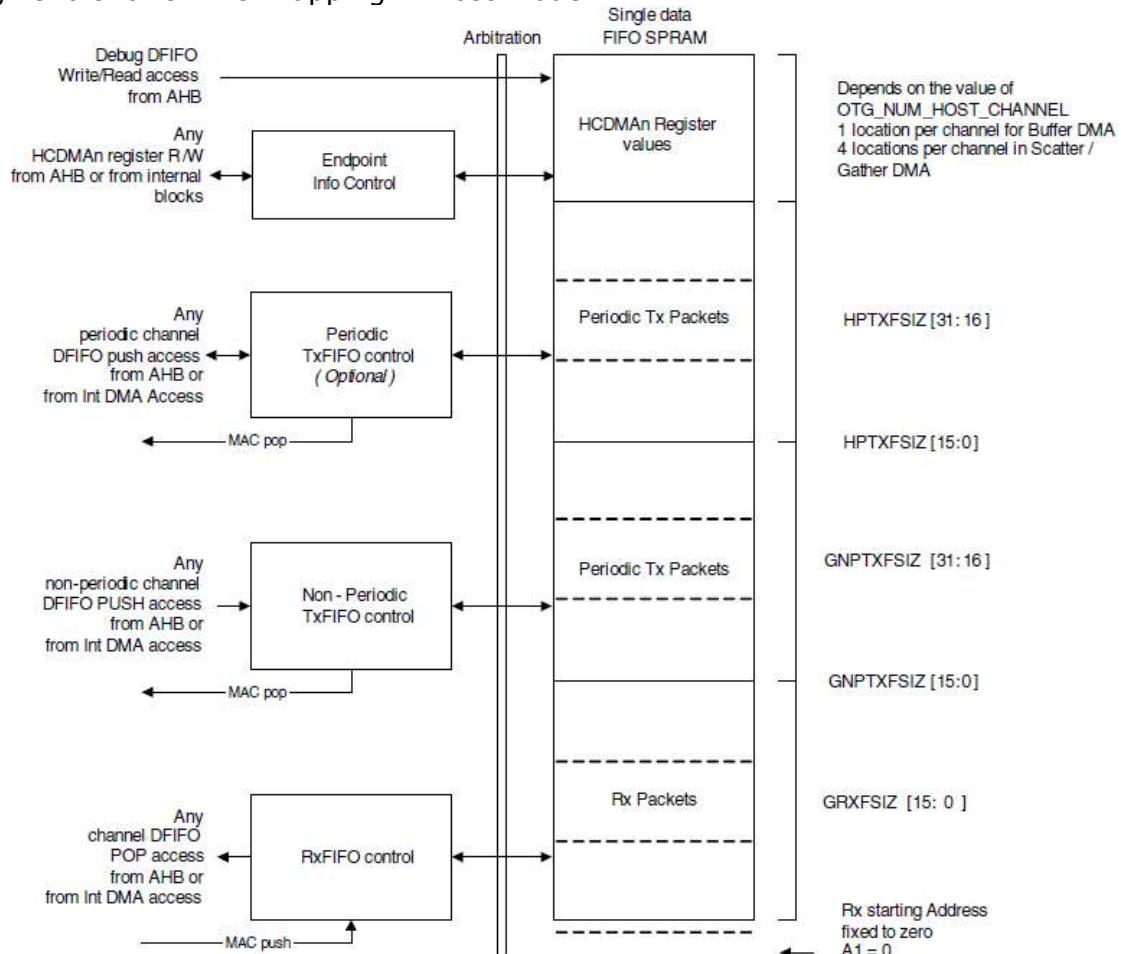


Fig. 1-6 USB OTG 2.0 Controller host mode FIFO address mapping

Note: When the device is operating in Internal DMA mode, the last locations of the SPRAM are used to store the DMAADDR values for each channel.

- Fig.2-7 shows FIFO mapping in Device mode.

When the device is operating in non-Descriptor Internal DMA mode, the last locations of the SPRAM are used to store the DMAADDR values for each channel. When the device is operating in Descriptor mode, then the last locations of the SPRAM store the Base Descriptor address, Current Descriptor address, Current Buffer address, and status quad let information for each endpoint direction.

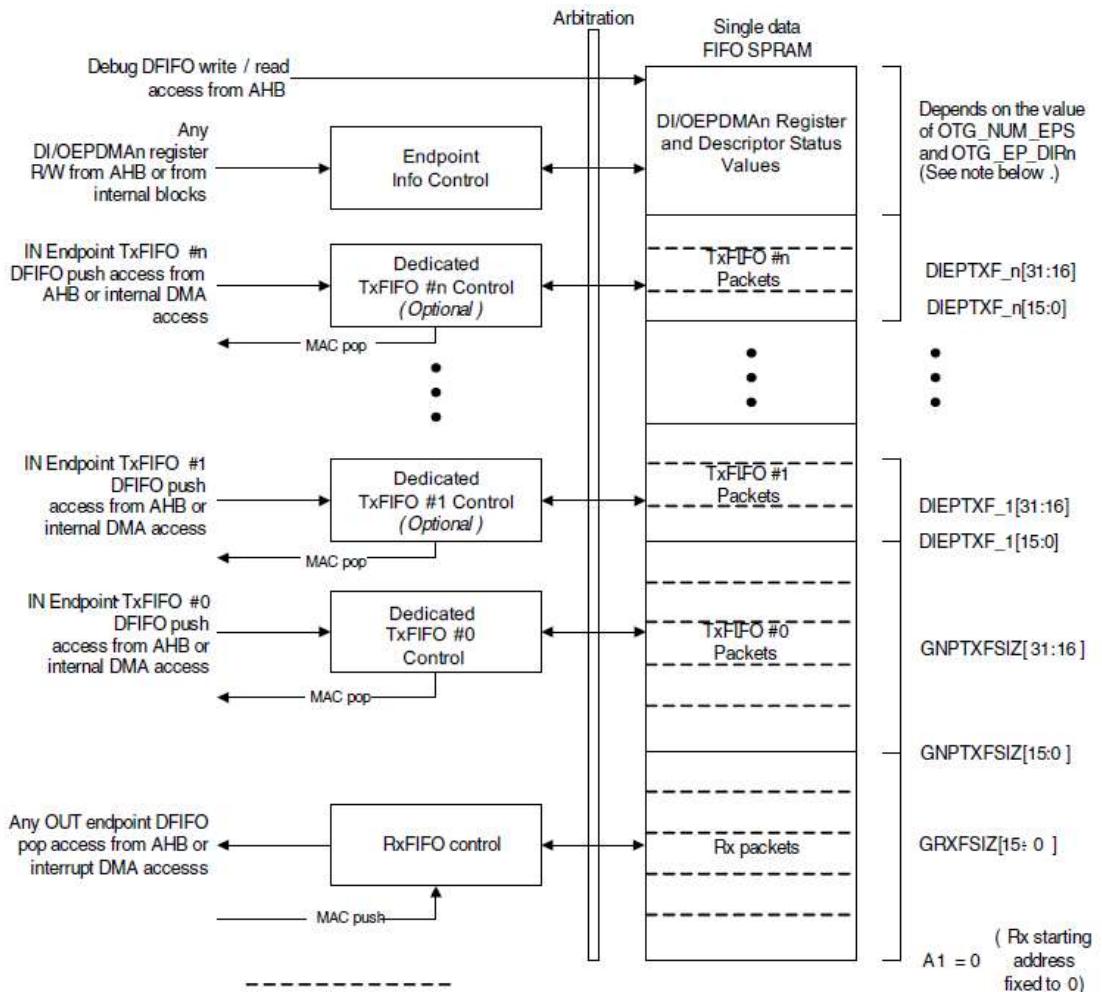


Fig. 1-7 USB OTG 2.0 Controller device mode FIFO address mapping

Note: When the device is operating in non-Scatter Gather Internal DMA mode, the last locations of the SPRAM are used to store the DMAADDR values for each Endpoint (1 location per endpoint). When the device is operating in Scatter Gather mode, then the last locations of the SPRAM store the Base Descriptor address, Current Descriptor address, Current Buffer address, and status quadlet information for each endpoint direction (4 locations per Endpoint). If an Endpoint is bidirectional, then 4 locations will be used for IN, and another 4 for OUT).

1.4 USB OTG2.0 PHY

The USB OTG 2.0 PHY connects a USB OTG controller to a USB system. It is a complete mixed-signal IP designed to implement OTG connectivity in a System-on-Chip (SOC) design targeted to a specific fabrication process using core and 2.5-V thick-oxide devices. The USB 2.0 PHY supports the USB2.0 480-Mbps protocol and data rate, and is backward compatible with the USB 1.1 1.5-Mbps and 12-Mbps protocol and data rates.

1.4.1 Block Diagram

Fig.2-8 shows the USB OTG 2.0 PHY functional block diagram for a one-port macro.

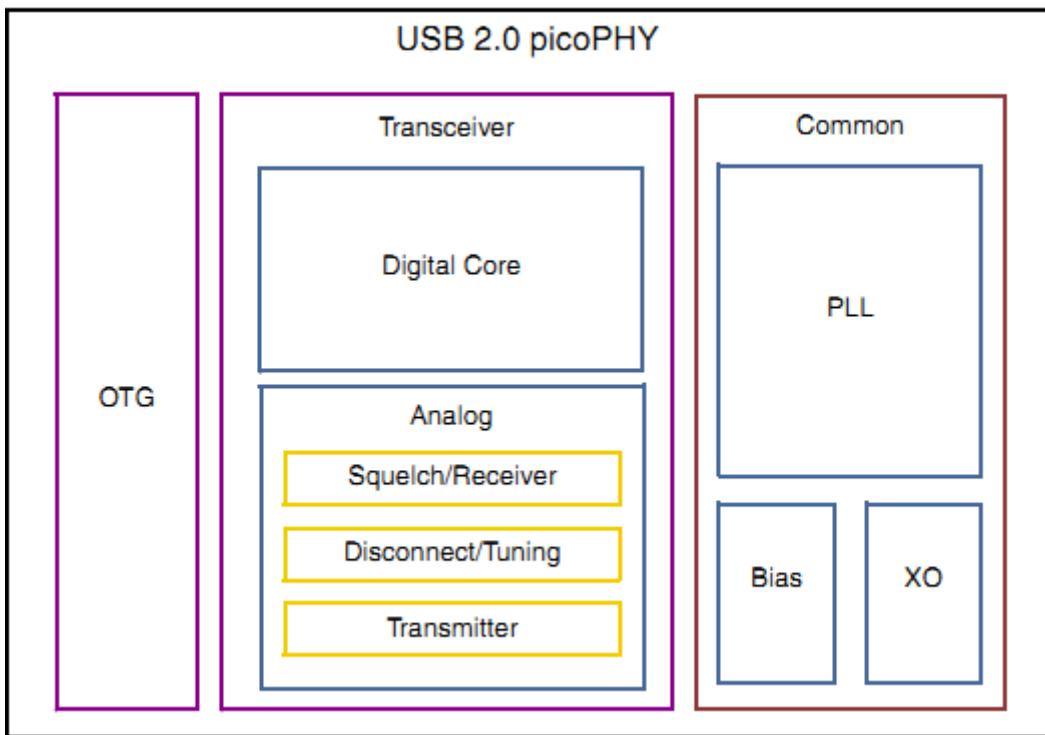


Fig. 1-8 USB OTG 2.0 PHY Architecture

The USB OTG 2.0 PHY consists of three basic components: the Common block, Transceiver block, and OTG block.

- Common block: This block contains design components that can be reused for multiple transceivers.
- Transceiver block: This block contains the bulk of USB OTG 2.0 PHY circuitry for data processing and transfers.
- OTG block: This block enables A-devices and B-devices to initiate the Session Request Protocol (SRP), and dual-Role devices to initiate the Host Negotiation Protocol (HNP).

1.4.2 Powering Up and Powering Down

- Powering UP

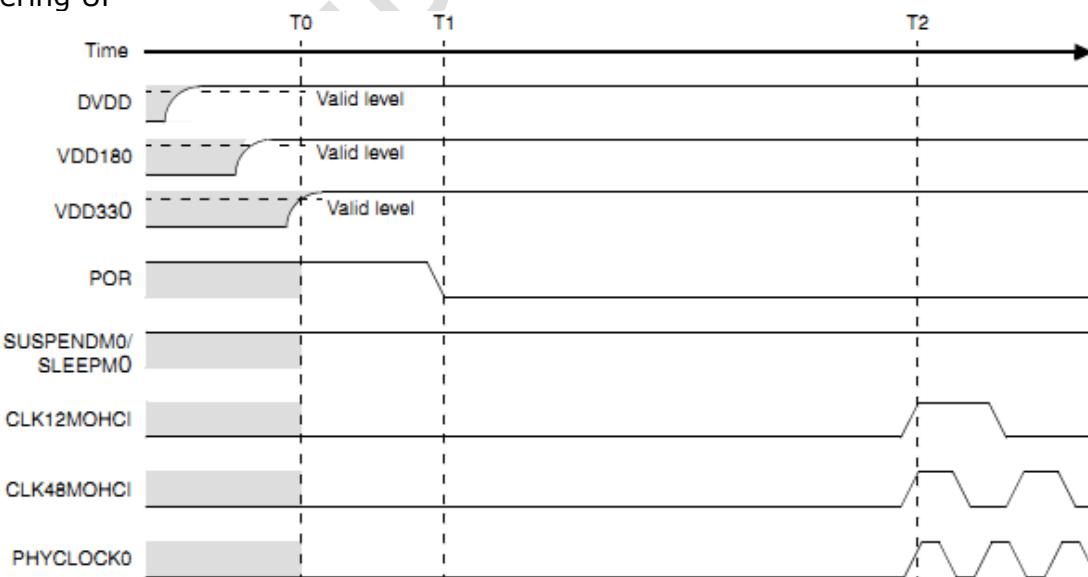


Fig. 1-9 USB OTG 2.0 PHY power supply and power up sequence

Table 1-1 USB OTG 2.0 PHY power supply timing parameter

Timing Parameter	Description	Value
T0	Power-on reset (POR) is initiated.	0 (reference)
T1	T1 indicates when POR can be set to 1'b0. (To provide examples, values for T2 and T3 are also shown where $T1 = T0 + 30 \mu s$.) In general, T1 must be $\geq T0 + 10 \mu s$.	$T0 + 10 \mu s \leq T1$
T2	T2 indicates when PHYCLOCK0, CLK48MOHCl, and CLK12MOHCl are available at the macro output, based on the USB 2.0 picoPHY reference clock source.	<p>Crystal:</p> <ul style="list-style-type: none"> ▪ When $T1 = T0 + 10 \mu s$: $T2 < T1 + 805 \mu s = T0 + 815 \mu s$ ▪ When $T1 = T0 + 30 \mu s$: $T2 < T1 + 805 \mu s = T0 + 835 \mu s$ <p>External board clock or CLKCORE:</p> <ul style="list-style-type: none"> ▪ When $T1 = T0 + 10 \mu s$: $T2 < T1 + 45 \mu s = T0 + 55 \mu s$ ▪ When $T1 = T0 + 30 \mu s$: $T2 < T1 + 45 \mu s = T0 + 75 \mu s$

1.4.3 Removing Power Supplies for Power Saving

There is no requirement on the power-down sequence for the USB groups. Customers can decide which voltage to be down first based on the application, it is recommended to keep the time between collapsing of power supplies as short as possible

1.5 UART BYPASS FUNCITON

When in UART bypass mode, UART2 is connect to USB interface; Otherwise, UART2 use normal UART interface.

Signal	CONNECT	I/O	Description
BYPASSDMDATA0	uart2_sout	I	Data for DM0 Transmitter Digital Bypass
BYPASSDMENO	uoc0_con0[8]	I	DM0 Transmitter Digital Bypass Enable
BYPASSSEL0	uoc0_con0[9]	I	Transmitter Digital Bypass mode Enable
FSVPLUS0	uart2_sin	O	Single-Ended D- Indicator The controller signal indicates the state of the DP during normal operation or UART data reception
OTGDISABLE0	uoc0_con0[4]	I	1'b1: OTG0 disable; 1'b0: OTG0 normal mode
COMMONONNN	uoc0_con0[0]	I	Common Block Power-Down Control This signal controls the power-down signals in PLL blocks when the USB PHY is in Suspend Mode. 1: PLL blocks are powered down. 0: PLL blocks remain powered This signal is a strapping option that must be set prior to a power-on reset and remain static during normal operation.

Note: USB OTG2.0 PHY support UART Bypass Function.

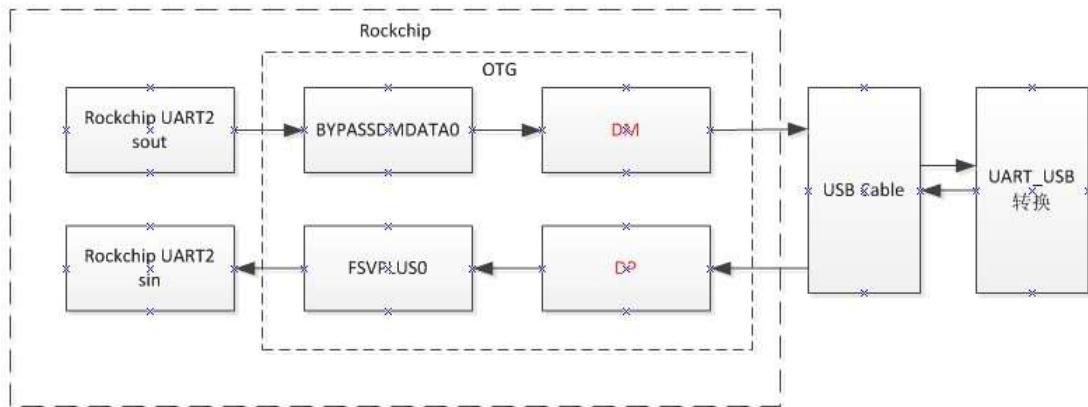


Fig. 1-10 UART Application

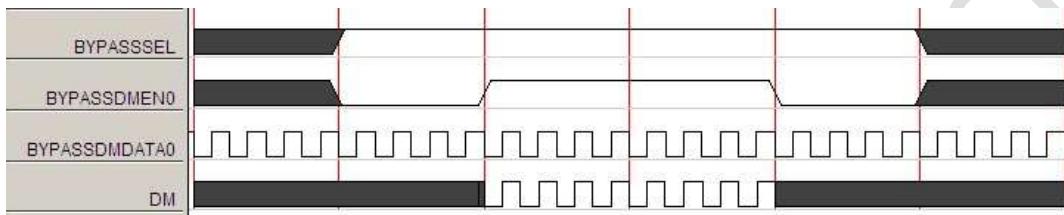


Fig. 1-11 UART Timing Sequence

To use UART and Auto resume functions:

1. Disable the OTG block by setting OTGDISABLE0 to 1'b1.
2. Disable the pull-up resistance on the D+ line by setting OPMODE0[1:0] to 2'b01.
3. To ensure that the XO, Bias, and PLL blocks are powered down in Suspend mode, set COMMONONN to 1'b1.
4. Place the USB PHY in Suspend mode by setting SUSPENDDM0 to 1'b0.
5. Set BYPASSEL0 to 1'b1.
6. To transmit data, controls BYPASSDMEN0, and BYPASSDMDATA0.
To receive data, monitor FSVPLUS0.

To return to normal operating mode:

1. Ensure that there is no activity on the USB.
2. Set BYPASSEL0 to 1'b0.
3. setting SUSPENDDM0 to 1'b1. Resume the USB PHY.
4. set COMMONONN to 1'b0.
5. set OTGDISABLE0 to 1'b0.

1.6 Register Description

1.6.1 Register Summary

Name	Offset	Size	Reset Value	Description
USBOTG_GOTGCTL	0x0000	W	0x00000000	Control and Status Register
USBOTG_GOTGINT	0x0004	W	0x00000000	Interrupt Register
USBOTG_GAHBCFG	0x0008	W	0x00000000	AHB Configuration Register
USBOTG_GUSBCFG	0x000c	W	0x00001400	USB Configuration Register
USBOTG_GRSTCTL	0x0010	W	0x80000000	Reset Register
USBOTG_GINTSTS	0x0014	W	0x00000000	Interrupt Register
USBOTG_GINTMSK	0x0018	W	0x00000000	Interrupt Mask Register
USBOTG_GRXSTSR	0x001c	W	0x00000000	Receive Status Debug Read Register

Name	Offset	Size	Reset Value	Description
USBOTG_GRXSTSP	0x0020	W	0x00000000	Receive Status Read and Pop Register
USBOTG_GRXFSIZ	0x0024	W	0x00000000	Receive FIFO Size Register
USBOTG_GNPTXFSIZ	0x0028	W	0x00000000	Non-Periodic Transmit FIFO Size Register
USBOTG_GNPTXSTS	0x002c	W	0x00000000	Non-Periodic Transmit FIFO/Queue Status Register
USBOTG_GI2CCTL	0x0030	W	0x11000000	I2C Address Register
USBOTG_GPVNDCTL	0x0034	W	0x00000000	PHY Vendor Control Register
USBOTG_GGPIO	0x0038	W	0x00000000	General Purpose Input / Output Register
USBOTG_GUID	0x003c	W	0x00000000	User ID Register
USBOTG_GSNPSID	0x0040	W	0x00004f54	Core ID Register
USBOTG_GHWCFG1	0x0044	W	0x00000000	User HW Config1 Register
USBOTG_GHWCFG2	0x0048	W	0x00000000	User HW Config2 Register
USBOTG_GHWCFG3	0x004c	W	0x00000000	User HW Config3 Register
USBOTG_GHWCFG4	0x0050	W	0x00000000	User HW Config4 Register
USBOTG_GLPMCFG	0x0054	W	0x00000000	Core LPM Configuration Register
USBOTG_GPWRDN	0x0058	W	0x00000000	Global Power Down Register
USBOTG_GDFIFO CFG	0x005c	W	0x00000000	Global DFIFO Software Configuration Register
USBOTG_GADPCTL	0x0060	W	0x00000000	ADP Timer, Control and Status Register
USBOTG_HPTXFSIZ	0x0100	W	0x00000000	Host Periodic Transmit FIFO Size Register
USBOTG_DIEPTXFn	0x0104+4*(n-1)	W	0x00000000	Device Periodic Transmit FIFO-n Size Register n = 1 - 15
USBOTG_HCFG	0x0400	W	0x00000000	Host Configuration Register
USBOTG_HFIR	0x0404	W	0x00000000	Host Frame Interval Register
USBOTG_HFNUM	0x0408	W	0x0000ffff	Host Frame Number/Frame Time Remaining Register
USBOTG_HPTXSTS	0x0410	W	0x00000000	Host Periodic Transmit FIFO/Queue Status Register
USBOTG_HAINT	0x0414	W	0x00000000	Host All Channels Interrupt Register
USBOTG_HAINTMSK	0x0418	W	0x00000000	Host All Channels Interrupt Mask Register
USBOTG_HPRT	0x0440	W	0x00000000	Host Port Control and Status Register
USBOTG_HCCHARn	0x0500+0x20*n	W	0x00000000	Host Channel-n Characteristics Register n = 0 - 15

Name	Offset	Size	Reset Value	Description
USBOTG_HCSPLTn	0x0504+0 x20*n	W	0x00000000	Host Channel-n Split Control Register n = 0 - 15
USBOTG_HCINTn	0x0508+0 x20*n	W	0x00000000	Host Channel-n Interrupt Register n = 0 - 15
USBOTG_HCINTMSKn	0x050c+0 x20*n	W	0x00000000	Host Channel-n Interrupt Mask Register n = 0 - 15
USBOTG_HCTSIZn	0x0510+0 x20*n	W	0x00000000	Host Channel-n Transfer Size Register n = 0 - 15
USBOTG_HCDMAAn	0x0514+0 x20*n	W	0x00000000	Host Channel-n DMA Address Register n = 0 - 15
USBOTG_HCDMABn	0x051c+0 x20*n	W	0x00000000	Host Channel-n DMA Buffer Address Register n = 0 - 15
USBOTG_DCFG	0x0800	W	0x08200000	Device Configuration Register
USBOTG_DCTL	0x0804	W	0x00002000	Device Control Register
USBOTG_DSTS	0x0808	W	0x00000000	Device Status Register
USBOTG_DIEPMSK	0x0810	W	0x00000000	Device IN Endpoint common interrupt mask register
USBOTG_DOEPMSK	0x0814	W	0x00000000	Device OUT Endpoint common interrupt mask register
USBOTG_DAINT	0x0818	W	0x00000000	Device All Endpoints interrupt register
USBOTG_DAINTMSK	0x081c	W	0x00000000	Device All Endpoint interrupt mask register
USBOTG_DTKNQR1	0x0820	W	0x00000000	Device IN token sequence learning queue read register1
USBOTG_DTKNQR2	0x0824	W	0x00000000	Device IN token sequence learning queue read register2
USBOTG_DVBUSDIS	0x0828	W	0x00000b8f	Device VBUS discharge time register
USBOTG_DVBU SPULSE	0x082c	W	0x00000000	Device VBUS Pulsing Timer Register
USBOTG_DTHRCTL	0x0830	W	0x08100020	Device Threshold Control Register
USBOTG_DIEPEMPMSK	0x0834	W	0x00000000	Device IN endpoint FIFO empty interrupt mask register
USBOTG_DEACHINT	0x0838	W	0x00000000	Device each endpoint interrupt register
USBOTG_DEACHINTMSK	0x083c	W	0x00000000	Device each endpoint interrupt register mask

Name	Offset	Size	Reset Value	Description
USBOTG_DIEPEACHMSKn	0x0840+4*n	W	0x00000000	Device each IN endpoint -n interrupt Register n = 0 - 15
USBOTG_DOEPEACHMSKn	0x0880+4*n	W	0x00000000	Device each out endpoint-n interrupt register n = 0 - 15
USBOTG_DIEPCTL0	0x0900	W	0x00008000	Device control IN endpoint 0 control register
USBOTG_DIEPINTn	0x0908+0x20*n	W	0x00000000	Device Endpoint-n Interrupt Register n = 0 - 15
USBOTG_DIEPTSIZn	0x0910+0x20*n	W	0x00000000	Device endpoint n transfer size register n = 0 - 15
USBOTG_DIEPDMAAn	0x0914+0x20*n	W	0x00000000	Device endpoint-n DMA address register n = 0 - 15
USBOTG_DTXFSTS _n	0x0918+0x20*n	W	0x00000000	Device IN endpoint transmit FIFO status register n = 0 - 15
USBOTG_DIEPDMABn	0x091c	W	0x00000000	Device endpoint-n DMA buffer address register
USBOTG_DIEPCTL _n	0x0920+0x20*(n-1)	W	0x00000000	Device endpoint-n control register n = 1 - 15
USBOTG_DOEPCTL0	0x0b00	W	0x00000000	Device control OUT endpoint 0 control register
USBOTG_DOEPINTn	0x0b08+0x20*n	W	0x00000000	Device endpoint-n control register n = 0 - 15
USBOTG_DOEPTSIZn	0x0b10+0x20*n	W	0x00000000	Device endpoint n transfer size register n = 0 - 15
USBOTG_DOEPDMAAn	0x0b14+0x20*n	W	0x00000000	Device Endpoint-n DMA Address Register n = 0 - 15
USBOTG_DOEPDMABn	0x0b1c+0x20*n	W	0x00000000	Device endpoint-n DMA buffer address register n = 0 - 15
USBOTG_DOEPCTL _n	0x0b20+0x20*(n-1)	W	0x00000000	Device endpoint-n control register n = 1 - 15
USBOTG_PCGCR	0x0b24	W	0x200b8000	Power and clock gating control register

Notes: **Size** : **B** - Byte (8 bits) access, **HW** - Half WORD (16 bits) access, **W** - WORD (32 bits) access

1.6.2 Detail Register Description

USBOTG_GOTGCTL

Address: Operational Base + offset (0x0000)

Control and Status Register

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27	RW	0x0	<p>ChirpEn Chirp on enable</p> <p>This bit when programmed to 1'b1 results in the core asserting chirp_on before sending an actual Chirp "K" signal on USB. This bit is present only if OTG_BC_SUPPORT = 1. If OTG_BC_SUPPORT != 1, this bit is a reserved bit.</p>
26:22	RO	0x00	<p>MultValidBc Multi Valued ID pin</p> <p>Battery Charger ACA inputs in the following order:</p> <ul style="list-style-type: none"> Bit 26 - rid_float. Bit 25 - rid_gnd Bit 24 - rid_a Bit 23 - rid_b Bit 22 - rid_c <p>These bits are present only if OTG_BC_SUPPORT = 1. Otherwise, these bits are reserved and will read 5'h0.</p>
21	RO	0x0	reserved
20	RW	0x0	<p>OTGVer OTG version</p> <p>Indicates the OTG revision.</p> <p>1'b0: OTG Version 1.3. In this version the core supports Data line pulsing and VBus pulsing for SRP.</p> <p>1'b1: OTG Version 2.0. In this version the core supports only Data line pulsing for SRP.</p>

Bit	Attr	Reset Value	Description
19	RO	0x0	<p>BSesVld B-session valid Indicates the Device mode transceiver status. 1'b0: B-session is not valid. 1'b1: B-session is valid.</p> <p>In OTG mode, you can use this bit to determine if the device is connected or disconnected. Note: If you do not enable OTG features (such as SRP and HNP), the read reset value will be 1. The vbus assigns the values internally for non-SRP or non-HNP configurations.</p>
18	RO	0x0	<p>ASesVld A-session valid Indicates the Host mode transceiver status. 1'b0: A-session is not valid 1'b1: A-session is valid</p> <p>Note: If you do not enable OTG features (such as SRP and HNP), the read reset value will be 1. The vbus assigns the values internally for non-SRP or non-HNP configurations.</p>
17	RO	0x0	<p>DbnTime Long/short debounce time Indicates the debounce time of a detected connection. 1'b0: Long debounce time, used for physical connections (100 ms + 2.5 us) 1'b1: Short debounce time, used for soft connections (2.5 us)</p>
16	RO	0x0	<p>ConIDSts Connector ID Status Indicates the connector ID status on a connect event. 1'b0: The core is in A-Device mode 1'b1: The core is in B-Device mode</p>
15:12	RO	0x0	reserved
11	RW	0x0	<p>DevHNPEn Device HNP Enable The application sets this bit when it successfully receives a SetFeature. SetHNPEnable command from the connected USB host. 1'b0: HNP is not enabled in the application 1'b1: HNP is enabled in the application</p>

Bit	Attr	Reset Value	Description
10	RW	0x0	<p>HstSetHNPEn Host set HNP enable The application sets this bit when it has successfully enabled HNP (using the SetFeature.SetHNPEnable command) on the connected device. 1'b0: Host Set HNP is not enabled 1'b1: Host Set HNP is enabled</p>
9	RW	0x0	<p>HNPReq HNP request The application sets this bit to initiate an HNP request to the connected USB host. The application can clear this bit by writing a 0 when the Host Negotiation Success Status Change bit in the OTG Interrupt register (GOTGINT.HstNegSucStsChng) is set. The core clears this bit when the HstNegSucStsChng bit is cleared. 1'b0: No HNP request 1'b1: HNP request</p>
8	RO	0x0	<p>HstNegScs Host Negotiation Success The core sets this bit when host negotiation is successful. The core clears this bit when the HNP Request (HNPReq) bit in this register is set. 1'b0: Host negotiation failure 1'b1: Host negotiation success</p>
7:2	RO	0x0	reserved

Bit	Attr	Reset Value	Description
1	RW	0x0	<p>SesReq Session Request</p> <p>The application sets this bit to initiate a session request on the USB. The application can clear this bit by writing a 0 when the Host Negotiation Success Status Change bit in the OTG Interrupt register (GOTGINT.HstNegSucStsChng) is set. The core clears this bit when the HstNegSucStsChng bit is cleared. If you use the USB 1.1 Full-Speed Serial Transceiver interface to initiate the session request, the application must wait until the VBUS discharges to 0.2 V, after the B-Session Valid bit in this register (GOTGCTL.BSesVld) is cleared. This discharge time varies between different PHYs and can be obtained from the PHY vendor.</p> <p>1'b0: No session request 1'b1: Session request</p>
0	RO	0x0	<p>SesReqScs Session Request Success</p> <p>The core sets this bit when a session request initiation is successful.</p> <p>1'b0: Session request failure 1'b1: Session request success</p>

USBOTG_GOTGINT

Address: Operational Base + offset (0x0004)

Interrupt Register

Bit	Attr	Reset Value	Description
31:21	RO	0x0	reserved
20	W1C	0x0	<p>MultiValueChg Multi-Valued input changed</p> <p>This bit when set indicates that there is a change in the value of at least one ACA pin value. This bit is present only if OTG_BC_SUPPORT = 1, otherwise it is reserved.</p>

Bit	Attr	Reset Value	Description
19	W1C	0x0	DbnceDone Debounce Done The core sets this bit when the debounce is completed after the device connection. The application can start driving USB reset after seeing this interrupt. This bit is only valid when the HNP Capable or SRP Capable bit is set in the Core USB Configuration register (GUSBCFG.HNPCap or GUSBCFG.SRPCap, respectively).
18	W1C	0x0	ADevTOUTChg A-Device Timeout Change The core sets this bit to indicate that the A-device has timed out while waiting for the B-device to connect.
17	W1C	0x0	HstNegDet Host Negotiation Detected The core sets this bit when it detects a host negotiation request on the USB
16:10	RO	0x0	reserved
9	W1C	0x0	HstNegSucStsChng Host Negotiation Success Status Change The core sets this bit on the success or failure of a USB host negotiation request. The application must read the Host Negotiation Success bit of the OTG Control and Status register (GOTGCTL.HstNegScs) to check for success or failure
8	W1C	0x0	SesReqSucStsChng Session Request Success Status Change The core sets this bit on the success or failure of a session request. The application must read the Session Request Success bit in the OTG Control and Status register (GOTGCTL.SesReqScs) to check for success or failure.
7:3	RO	0x0	reserved
2	W1C	0x0	SesEndDet Session End Detected The core sets this bit when the utmisrp_bvalid signal is deasserted
1:0	RO	0x0	reserved

USBOTG_GAHBCFG

Address: Operational Base + offset (0x0008)

AHB Configuration Register

Bit	Attr	Reset Value	Description
31:23	RO	0x0	reserved
22	RW	0x0	<p>NotiAllDmaWrit Notify All Dma Write Transactions This bit is programmed to enable the System DMA Done functionality for all the DMA write Transactions corresponding to the Channel/Endpoint. This bit is valid only when GAHBCFG.RemMemSupp is set to 1. GAHBCFG.NotiAllDmaWrit = 1.</p> <p>HSOTG core asserts int_dma_req for all the DMA write transactions on the AHB interface along with int_dma_done, chep_last_transact and chep_number signal informations. The core waits for sys_dma_done signal for all the DMA write transactions in order to complete the transfer of a particular Channel/Endpoint.</p> <p>GAHBCFG.NotiAllDmaWrit = 0.</p> <p>HSOTG core asserts int_dma_req signal only for the last transaction of DMA write transfer corresponding to a particular Channel/Endpoint. Similarly, the core waits for sys_dma_done signal only for that transaction of DMA write to complete the transfer of a particular Channel/Endpoint.</p>
21	RW	0x0	<p>RemMemSupp Remote Memory Support This bit is programmed to enable the functionality to wait for the system DMA Done Signal for the DMA Write Transfers.</p> <p>GAHBCFG.RemMemSupp=1.</p> <p>The int_dma_req output signal is asserted when HSOTG DMA starts write transfer to the external memory. When the core is done with the Transfers it asserts int_dma_done signal to flag the completion of DMA writes from HSOTG. The core then waits for sys_dma_done signal from the system to proceed further and complete the Data Transfer corresponding to a particular Channel/Endpoint.</p> <p>GAHBCFG.RemMemSupp=0.</p> <p>The int_dma_req and int_dma_done signals are not asserted and the core proceeds with the assertion of the XferComp interrupt as soon as the DMA write transfer is done at the HSOTG Core Boundary and it does not wait for the sys_dma_done signal to complete the DATA transfers.</p>
20:9	RO	0x0	reserved

Bit	Attr	Reset Value	Description
8	RW	0x0	<p>PTxFEmpLvl Periodic TxFIFO Empty Level Indicates when the Periodic TxFIFO Empty Interrupt bit in the Core Interrupt register (GINTSTS.PTxFEmp) is triggered. This bit is used only in Slave mode.</p> <p>1'b0: GINTSTS.PTxFEmp interrupt indicates that the Periodic TxFIFO is half empty 1'b1: GINTSTS.PTxFEmp interrupt indicates that the Periodic TxFIFO is completely empty</p>
7	RW	0x0	<p>NPTxFEmpLvl Non-Periodic TxFIFO Empty Level This bit is used only in Slave mode. In host mode and with Shared FIFO with device mode, this bit indicates when the Non-Periodic TxFIFO Empty Interrupt bit in the Core Interrupt register GINTSTS.NPTxFEmp) is triggered. With dedicated FIFO in device mode, this bit indicates when IN endpoint Transmit FIFO empty interrupt (DIEPINTn.TxFEmp) is triggered.</p> <p>Host mode and with Shared FIFO with device mode: 1'b0: GINTSTS.NPTxFEmp interrupt indicates that the Non-Periodic TxFIFO is half empty 1'b1: GINTSTS.NPTxFEmp interrupt indicates that the Non-Periodic TxFIFO is completely empty</p> <p>Dedicated FIFO in device mode: 1'b0: DIEPINTn.TxFEmp interrupt indicates that the IN Endpoint TxFIFO is half empty 1'b1: DIEPINTn.TxFEmp interrupt indicates that the IN Endpoint TxFIFO is completely empty</p>
6	RO	0x0	reserved
5	RW	0x0	<p>DMAEn DMA Enable 1'b0: Core operates in Slave mode 1'b1: Core operates in a DMA mode</p> <p>This bit is always 0 when Slave-Only mode has been selected.</p>

Bit	Attr	Reset Value	Description
4:1	RW	0x0	<p>HBstLen Burst Length/Type This field is used in both External and Internal DMA modes. In External DMA mode, these bits appear on dma_burst[3:0] ports, External DMA Mode defines the DMA burst length in terms of 32-bit words:</p> <p>4'b0000: 1 word 4'b0001: 4 words 4'b0010: 8 words 4'b0011: 16 words 4'b0100: 32 words 4'b0101: 64 words 4'b0110: 128 words 4'b0111: 256 words Others: Reserved</p> <p>Internal DMA Mode AHB Master burst type:</p> <p>4'b0000: Single 4'b0001: INCR 4'b0011: INCR4 4'b0101: INCR8 4'b0111: INCR16 Others: Reserved</p>
0	RW	0x0	<p>GlblIntrMsk Global Interrupt Mask The application uses this bit to mask or unmask the interrupt line assertion to itself. Irrespective of this bit's setting, the interrupt status registers are updated by the core.</p> <p>1'b0: Mask the interrupt assertion to the application. 1'b1: Unmask the interrupt assertion to the application.</p>

USBOTG_GUSBCFG

Address: Operational Base + offset (0x000c)

USB Configuration Register

Bit	Attr	Reset Value	Description
31	RW	0x0	<p>CorruptTxpacket Corrupt Tx packet This bit is for debug purposes only. Never set this bit to 1.</p>

Bit	Attr	Reset Value	Description
30	RW	0x0	<p>ForceDevMode Force Device Mode Writing a 1 to this bit forces the core to device mode irrespective of utmiotg_iddig input pin. 1'b0: Normal Mode 1'b1: Force Device Mode After setting the force bit, the application must wait at least 25 ms before the change to take effect. When the simulation is in scale down mode, waiting for 500 us is sufficient. This bit is valid only when OTG_MODE = 0, 1 or 2. In all other cases, this bit reads 0.</p>
29	RW	0x0	<p>ForceHstMode Force Host Mode Writing a 1 to this bit forces the core to host mode irrespective of utmiotg_iddig input pin. 1'b0: Normal Mode 1'b1: Force Host Mode After setting the force bit, the application must wait at least 25 ms before the change to take effect. When the simulation is in scale down mode, waiting for 500 us is sufficient. This bit is valid only when OTG_MODE =0, 1 or 2. In all other cases, this bit reads 0.</p>
28	RW	0x0	<p>TxEndDelay Tx End Delay Writing a 1 to this bit enables the TxEndDelay timers in the core. 1'b0: Normal mode 1'b1: Introduce Tx end delay timers</p>
27	RW	0x0	<p>IC_USB_TrafficCtl IC_USB Traffic Pull Remove Control When this bit is set, pullup/pulldown resistors are detached from the USB during traffic signaling. This bit is valid only when configuration parameter OTG_ENABLE_IC_USB = 1 and register field GUSBCFG.IC_USBCap is set to 1.</p>

Bit	Attr	Reset Value	Description
26	RW	0x0	<p>IC_USBCap IC_USB-Capable The application uses this bit to control the IC_USB capabilities. 1'b0: IC_USB PHY Interface is not selected. 1'b1: IC_USB PHY Interface is selected. This bit is writable only if OTG_ENABLE_IC_USB=1 and OTG_FSPHY_INTERFACE!=0. The reset value depends on the configuration parameter OTG_SELECT_IC_USB when OTG_ENABLE_IC_USB = 1. In all other cases, this bit is set to 1'b0 and the bit is read only.</p>
25	RW	0x0	<p>ULPIIfDis ULPI Interface Protect Disable Controls circuitry built into the PHY for protecting the ULPI interface when the link tri-states STP and data. Any pull-ups or pull-downs employed by this feature can be disabled. Please refer to the ULPI Specification for more detail. 1'b0: Enables the interface protect circuit 1'b1: Disables the interface protect circuit</p>
24	RW	0x0	<p>IndPassThrough Indicator Pass Through Controls whether the Complement Output is qualified with the Internal Vbus Valid comparator before being used in the Vbus State in the RX CMD. Please refer to the ULPI Specification for more detail. 1'b0: Complement Output signal is qualified with the Internal VbusValid comparator. 1'b1: Complement Output signal is not qualified with the Internal VbusValid comparator.</p>
23	RW	0x0	<p>IndComple Indicator Complement Controls the PHY to invert the ExternalVbusIndicator input signal, generating the Complement Output. Please refer to the ULPI Specification for more detail 1'b0: PHY does not invert External Vbus Indicator signal 1'b1: PHY does invert External Vbus Indicator signal</p>
22	RW	0x0	<p>TermSelDLPulse TermSel DLine Pulsing Selection This bit selects utmi_termselect to drive data line pulse during SRP. 1'b0: Data line pulsing using utmi_txvalid (default). 1'b1: Data line pulsing using utmi_termsel.</p>

Bit	Attr	Reset Value	Description
21	RW	0x0	<p>ULPIExtVbusIndicator ULPI External VBUS Indicator This bit indicates to the ULPI PHY to use an external VBUS over-current indicator. 1'b0: PHY uses internal VBUS valid comparator. 1'b1: PHY uses external VBUS valid comparator. (Valid only when RTL parameter OTG_HSPHY_INTERFACE = 2 or 3)</p>
20	RW	0x0	<p>ULPIExtVbusDrv ULPI External VBUS Drive This bit selects between internal or external supply to drive 5V on VBUS,in ULPI PHY. 1'b0: PHY drives VBUS using internal charge pump (default). 1'b1: PHY drives VBUS using external supply. (Valid only when RTL parameter OTG_HSPHY_INTERFACE = 2 or 3)</p>
19	RW	0x0	<p>ULPIClkSusM ULPI Clock SuspendM This bit sets the ClockSuspendM bit in the Interface Control register on the ULPI PHY. This bit applies only in serial or carkit modes. 1'b0: PHY powers down internal clock during suspend. 1'b1: PHY does not power down internal clock. (Valid only when RTL parameter OTG_HSPHY_INTERFACE = 2 or 3)</p>
18	RW	0x0	<p>ULPIAutoRes ULPI Auto Resume This bit sets the AutoResume bit in the Interface Control register on the ULPI PHY. 1'b0: PHY does not use AutoResume feature. 1'b1: PHY uses AutoResume feature. (Valid only when RTL parameter OTG_HSPHY_INTERFACE = 2 or 3)</p>

Bit	Attr	Reset Value	Description
17	RW	0x0	<p>ULPIFsLs ULPI FS/LS Select The application uses this bit to select the FS/LS serial interface for the ULPI PHY. This bit is valid only when the FS serial transceiver is selected on the ULPI PHY.</p> <p>1'b0: ULPI interface 1'b1: ULPI FS/LS serial interface (Valid only when RTL parameters OTG_HSPHY_INTERFACE = 2 or 3 and OTG_FSPHY_INTERFACE = 1, 2, or 3)</p>
16	RW	0x0	<p>OtgI2CSel UTMIFS or I2C Interface Select The application uses this bit to select the I2C interface.</p> <p>1'b0: UTMI USB 1.1 Full-Speed interface for OTG signals 1'b1: I2C interface for OTG signals This bit is writable only if I2C and UTMIFS were specified for Enable I2C Interface? (parameter OTG_I2C_INTERFACE = 2). Otherwise, reads return 0.</p>
15	RW	0x0	<p>PhyLPwrClkSel PHY Low-Power Clock Select Selects either 480-MHz or 48-MHz (low-power) PHY mode. In FS and LS modes, the PHY can usually operate on a 48-MHz clock to save power.</p> <p>1'b0: 480-MHz Internal PLL clock 1'b1: 48-MHz External Clock In 480 MHz mode, the UTMI interface operates at either 60 or 30-MHz, depending upon whether 8- or 16-bit data width is selected. In 48-MHz mode, the UTMI interface operates at 48 MHz in FS and LS modes. This bit drives the utmi_fs_ls_low_power core output signal, and is valid only for UTMI+ PHYs.</p>
14	RO	0x0	reserved

Bit	Attr	Reset Value	Description
13:10	RW	0x5	<p>USBTrdTim USB Turnaround Time Sets the turnaround time in PHY clocks. Specifies the response time for a MAC request to the Packet FIFO Controller (PFC) to fetch data from the DFIF(SPRAM). This must be programmed to 4'h5: When the MAC interface is 16-bit UTMI+. 4'h9: When the MAC interface is 8-bit UTMI+.</p> <p>Note: The values above are calculated for the minimum AHB frequency of 30 MHz. USB turnaround time is critical for certification where long cables and 5-Hubs are used, so if you need the AHB to run at less than 30 MHz, and if USB turnaround time is not critical, these bits can be programmed to a larger value.</p>
9	RW	0x0	<p>HNPCap HNP-Capable The application uses this bit to control the Otg core's HNP capabilities. 1'b0: HNP capability is not enabled. 1'b1: HNP capability is enabled. This bit is writable only if an HNP mode was specified for Mode of Operation (parameter OTG_MODE). Otherwise, reads return 0.</p>
8	RW	0x0	<p>SRPCap SRP-Capable The application uses this bit to control the Otg core SRP capabilities. If the core operates as a non-SRP-capable B-device, it cannot request the connected A-device (host) to activate VBUS and start a session. 0: SRP capability is not enabled. 1: SRP capability is enabled. This bit is writable only if an SRP mode was specified for Mode of Operation (parameter OTG_MODE). Otherwise, reads return 0.</p>
7	RW	0x0	<p>DDRSel ULPI DDR Select The application uses this bit to select a Single Data Rate (SDR) or Double Data Rate (DDR) or ULPI interface. 1'b0: Single Data Rate ULPI Interface, with 8-bit-wide data bus 1'b1: Double Data Rate ULPI Interface, with 4-bit-wide data bus</p>

Bit	Attr	Reset Value	Description
6	RW	0x0	<p>PHYSel</p> <p>USB 2.0 High-Speed PHY or USB 1.1 Full-Speed Serial Transceiver</p> <p>The application uses this bit to select either a high-speed UTMI+ or ULPI PHY, or a full-speed transceiver.</p> <p>1'b0: USB 2.0 high-speed UTMI+ or ULPI PHY 1'b1: USB 1.1 full-speed serial transceiver</p> <p>If a USB 1.1 Full-Speed Serial Transceiver interface was not selected (parameter OTG_FSPHY_INTERFACE = 0), this bit is always 0, with Write Only access. If a high-speed PHY interface was not selected (parameter OTG_HSPHY_INTERFACE = 0), this bit is always 1, with Write Only access.</p> <p>If both interface types were selected (parameters have non-zero values), the application uses this bit to select which interface is active, and access is Read and Write.</p>
5	RW	0x0	<p>FSIntf</p> <p>Full-Speed Serial Interface Select</p> <p>The application uses this bit to select either a unidirectional or bidirectional USB 1.1 full-speed serial transceiver interface.</p> <p>1'b0: 6-pin unidirectional full-speed serial interface 1'b1: 3-pin bidirectional full-speed serial interface</p> <p>If a USB 1.1 Full-Speed Serial Transceiver interface was not selected (parameter OTG_FSPHY_INTERFACE = 0), this bit is always 0, with Write Only access. If a USB 1.1 FS interface was selected (parameter OTG_FSPHY_INTERFACE! = 0), then the application can set this bit to select between the 3- and 6-pin interfaces, and access is Read and Write.</p>

Bit	Attr	Reset Value	Description
4	RW	0x0	<p>ULPI_UTMI_Sel ULPI or UTMI+ Select The application uses this bit to select either a UTMI+ interface or ULPI Interface. 1'b0: UTMI+ Interface 1'b1: ULPI Interface</p> <p>This bit is writable only if UTMI+ and ULPI was specified for High-Speed PHY Interface(s) (parameter OTG_HSPHY_INTERFACE = 3). Otherwise, reads return either 0 or 1, depending on the interface selected using the OTG_HSPHY_INTERFACE parameter.</p>
3	RW	0x0	<p>PHYIf PHY Interface The application uses this bit to configure the core to support a UTMI+ PHY with an 8- or 16-bit interface. When a ULPI PHY is chosen, this must be set to 8-bit mode. 1'b0: 8 bits 1'b1: 16 bits</p> <p>This bit is writable only if UTMI+ and ULPI were selected (parameter OTG_HSPHY_DWIDTH = 3). Otherwise, this bit returns the value for the power-on interface selected during configuration.</p>

Bit	Attr	Reset Value	Description
2:0	RW	0x0	<p>TOutCal HS/FS Timeout Calibration The number of PHY clocks that the application programs in this field is added to the high-speed/full-speed inter-packet timeout duration in the core to account for any additional delays introduced by the PHY. This can be required, because the delay introduced by the PHY in generating the line state condition can vary from one PHY to another. The USB standard timeout value for high-speed operation is 736 to 816 (inclusive) bit times. The USB standard timeout value for full-speed operation is 16 to 18 (inclusive) bit times. The application must program this field based on the speed of enumeration. The number of bit times added per PHY clock are: High-speed operation: One 30-MHz PHY clock = 16 bit times One 60-MHz PHY clock = 8 bit times Full-speed operation: One 30-MHz PHY clock = 0.4 bit times One 60-MHz PHY clock = 0.2 bit times One 48-MHz PHY clock = 0.25 bit times</p>

USBOTG_GRSTCTL

Address: Operational Base + offset (0x0010)

Reset Register

Bit	Attr	Reset Value	Description
31	RO	0x1	AHBIdle AHB Master Idle Indicates that the AHB Master State Machine is in the IDLE condition.
30	RO	0x0	DMAReq DMA Request Signal Indicates that the DMA request is in progress. Used for debug.
29:11	RO	0x0	reserved

Bit	Attr	Reset Value	Description
10:6	RW	0x00	<p>TxFNum Tx FIFO Number This is the FIFO number that must be flushed using the Tx FIFO Flush bit. This field must not be changed until the core clears the Tx FIFO Flush bit.</p> <p>5'h0: Non-periodic Tx FIFO flush in Host mode; Non-periodic Tx FIFO flush in device mode when in shared FIFO operation. Tx FIFO 0 flush in device mode when in dedicated FIFO mode.</p> <p>5'h1: Periodic Tx FIFO flush in Host mode: Periodic Tx FIFO 1 flush in Device mode when in shared FIFO operation; TX FIFO 1 flush in device mode when in dedicated FIFO mode.</p> <p>5'h2: Periodic Tx FIFO 2 flush in Device mode when in shared FIFO operation: TX FIFO 2 flush in device mode when in dedicated FIFO mode.</p> <p>...</p> <p>5'hF: Periodic Tx FIFO 15 flush in Device mode when in shared FIFO operation: TX FIFO 15 flush in device mode when in dedicated FIFO mode.</p> <p>5'h10: Flush all the transmit FIFOs in device or host mode.</p>
5	RWSC	0x0	<p>TxFFlsh Tx FIFO Flush This bit selectively flushes a single or all transmit FIFOs, but cannot do so if the core is in the midst of a transaction. The application must write this bit only after checking that the core is neither writing to the Tx FIFO nor reading from the Tx FIFO. Verify using these registers: Read NAK Effective Interrupt ensures the core is not reading from the FIFO. Write GRSTCTL.AHBIdle ensures the core is not writing anything to the FIFO. Flushing is normally recommended when FIFOs are re-configured or when switching between Shared FIFO and Dedicated Transmit FIFO operation. FIFO flushing is also recommended during device endpoint disable. The application must wait until the core clears this bit before performing any operations. This bit takes eight clocks to clear, using the slower clock of phy_clk or hclk.</p>

Bit	Attr	Reset Value	Description
4	RWSC	0x0	RxFFlsh Rx FIFO Flush The application can flush the entire Rx FIFO using this bit, but must first ensure that the core is not in the middle of a transaction. The application must only write to this bit after checking that the core is neither reading from the Rx FIFO nor writing to the Rx FIFO. The application must wait until the bit is cleared before performing any other operations. This bit requires 8 clocks (slowest of PHY or AHB clock) to clear.
3	RWSC	0x0	INTknQFlsh IN Token Sequence Learning Queue Flush This bit is valid only if OTG_ENDED_TX_FIFO = 0. The application writes this bit to flush the IN Token Sequence Learning Queue.
2	W1C	0x0	FrmCntrRst Host Frame Counter Reset The application writes this bit to reset the (micro) frame number counter inside the core. When the (micro) frame counter is reset, the subsequent SOF sent out by the core has a (micro) frame number of 0.
1	RWSC	0x0	Reset A write to this bit issues a soft reset to the Otg_power_dn module of the core.

Bit	Attr	Reset Value	Description
0	RWSC	0x0	<p>CSftRst Core Soft Reset Resets the hclk and phy_clock domains as follows: Clears the interrupts and all the CSR registers except the following register bits:</p> <ul style="list-style-type: none"> PCGCCTL.RstPdwnModule PCGCCTL.GateHclk PCGCCTL.PwrClmp PCGCCTL.StopPPhyLPwrClkSelClk GUSBCFG.PhyLPwrClkSel GUSBCFG.DDRSel GUSBCFG.PHYSel GUSBCFG.FSIntf GUSBCFG.ULPI_UTMI_Sel GUSBCFG.PHYIf HCFG.FSLSPClkSel DCFG.DevSpd GPIO GPWRDN GADPCTL <p>All module state machines (except the AHB Slave Unit) are reset to the IDLE state, and all the transmit FIFOs and the receive FIFO are flushed. Any transactions on the AHB Master are terminated as soon as possible, after gracefully completing the last data phase of an AHB transfer. Any transactions on the USB are terminated immediately. When Hibernation or ADP feature is enabled, the PMU module is not reset by the Core Soft Reset. The application can write to this bit any time it wants to reset the core. This is a self-clearing bit and the core clears this bit after all the necessary logic is reset in the core, which can take several clocks, depending on the current state of the core. Once this bit is cleared software must wait at least 3 PHY clocks before doing any access to the PHY domain (synchronization delay). Software must also check that bit 31 of this register is 1 (AHB Master is IDLE) before starting any operation. Typically software reset is used during software development and also when you dynamically change the PHY selection bits in the USB configuration registers listed above. When you change the PHY, the corresponding clock for the PHY is selected and used in the PHY domain. Once a new clock is selected, the PHY domain has to be reset for proper operation.</p>

USBOTG_GINTSTS

Address: Operational Base + offset (0x0014)

Interrupt Register

Bit	Attr	Reset Value	Description
31	W1C	0x0	<p>WkUpInt Resume/Remote Wakeup Detected Interrupt Wakeup Interrupt during Suspend (L2) or LPM(L1) state.</p> <p>During Suspend(L2): Device Mode: This interrupt is asserted only when Host Initiated Resume is detected on USB. Host Mode: This interrupt is asserted only when Device Initiated Remote Wakeup is detected on USB.</p> <p>During LPM(L1): Device Mode: This interrupt is asserted for either Host Initiated Resume or Device Initiated Remote Wakeup on USB. Host Mode: This interrupt is asserted for either Host Initiated Resume or Device Initiated Remote Wakeup on USB.</p>
30	W1C	0x0	SessReqInt Session Request/New Session Detected Interrupt In Host mode, this interrupt is asserted when a session request is detected from the device. In Host mode, this interrupt is asserted when a session request is detected from the device. In Device mode, this interrupt is asserted when the utmisrp_bvalid signal goes high.
29	W1C	0x0	DisconnectInt Disconnect Detected Interrupt This interrupt is asserted when a device disconnect is detected.
28	W1C	0x0	ConIDStsChng Connector ID Status Change This interrupt is asserted when there is a change in connector ID status.

Bit	Attr	Reset Value	Description
27	W1C	0x0	LPM_Int LPM Transaction Received Interrupt Device Mode : This interrupt is asserted when the device receives an LPM transaction and responds with a non-ERRORed response. Host Mode : This interrupt is asserted when the device responds to an LPM transaction with a non-ERRORed response or when the host core has completed LPM transactions for the programmed number of times (GLPMCFG.RetryCnt). This field is valid only if the Core LPM Configuration register's LPMCapable (LPMCap) field is set to 1.
26	RO	0x0	PTxFEmp Periodic TxFIFO Empty This interrupt is asserted when the Periodic Transmit FIFO is either half or completely empty and there is space for at least one entry to be written in the Periodic Request Queue. The half or completely empty status is determined by the Periodic TxFIFO Empty Level bit in the Core AHB Configuration register (GAHBCFG.PTxFEmpLvl).
25	RO	0x0	HChInt Host Channels Interrupt The core sets this bit to indicate that an interrupt is pending on one of the channels of the core (in Host mode). The application must read the Host All Channels Interrupt (HAINT) register to determine the exact number of the channel on which the interrupt occurred, and then read the corresponding Host Channel-n Interrupt (HCINTn) register to determine the exact cause of the interrupt. The application must clear the appropriate status bit in the HCINTn register to clear this bit.
24	RO	0x0	PrtInt Host Port Interrupt The core sets this bit to indicate a change in port status of one of the OTG core ports in Host mode. The application must read the Host Port Control and Status (HPRT) register to determine the exact event that caused this interrupt. The application must clear the appropriate status bit in the Host Port Control and Status register to clear this bit.

Bit	Attr	Reset Value	Description
23	RW	0x0	ResetDet Reset Detected Interrupt The core asserts this interrupt in Device mode when it detects a reset on the USB in Partial Power-Down mode when the device is in Suspend. This interrupt is not asserted in Host mode.
22	W1C	0x0	FetSusp Data Fetch Suspended This interrupt is valid only in DMA mode. This interrupt indicates that the core has stopped fetching data for IN endpoints due to the unavailability of TxFIFO space or Request Queue space. This interrupt is used by the application for an endpoint mismatch algorithm.
21	W1C	0x0	incomlP Incomplete Periodic Transfer In Host mode, the core sets this interrupt bit when there are incomplete periodic transactions still pending which are scheduled for the current micro-frame. Incomplete Isochronous OUT Transfer (incompISOOUT) The Device mode, the core sets this interrupt to indicate that there is at least one isochronous OUT endpoint on which the transfer is not completed in the current micro-frame. This interrupt is asserted along with the End of Periodic Frame Interrupt (EOPF) bit in this register.
20	W1C	0x0	incompISOIN Incomplete Isochronous IN Transfer The core sets this interrupt to indicate that there is at least one isochronous IN endpoint on which the transfer is not completed in the current micro-frame. This interrupt is asserted along with the End of Periodic Frame Interrupt (EOPF) bit in this register. Note: This interrupt is not asserted in Scatter/Gather DMA mode.

Bit	Attr	Reset Value	Description
19	RO	0x0	OEPInt OUT Endpoints Interrupt The core sets this bit to indicate that an interrupt is pending on one of the OUT endpoints of the core (in Device mode). The application must read the Device All Endpoints Interrupt (DAINT) register to determine the exact number of the OUT endpoint on which the interrupt occurred, and then read the corresponding Device OUT Endpoint-n Interrupt (DOEPINTn) register to determine the exact cause of the interrupt. The application must clear the appropriate status bit in the corresponding DOEPINTn register to clear this bit.
18	RO	0x0	IEPInt IN Endpoints Interrupt The core sets this bit to indicate that an interrupt is pending on one of the IN endpoints of the core (in Device mode). The application must read the Device All Endpoints Interrupt (DAINT) register to determine the exact number of the IN endpoint on which the interrupt occurred, and then read the corresponding Device IN Endpoint-n Interrupt (DIEPINTn) register to determine the exact cause of the interrupt. The application must clear the appropriate status bit in the corresponding DIEPINTn register to clear this bit.
17	W1C	0x0	EPMIs Endpoint Mismatch Interrupt Note: This interrupt is valid only in shared FIFO operation. Indicates that an IN token has been received for a non-periodic endpoint, but the data for another endpoint is present in the top of the Non-periodic Transmit FIFO and the IN endpoint mismatch count programmed by the application has expired.
16	W1C	0x0	RstrDoneInt Restore Done Interrupt The core sets this bit to indicate that the restore command after Hibernation was completed by the core. The core continues from Suspended state into the mode dictated by PCGCCTL.RestoreMode field. This bit is valid only when Hibernation feature is enabled.

Bit	Attr	Reset Value	Description
15	W1C	0x0	EOPF End of Periodic Frame Interrupt Indicates that the period specified in the Periodic Frame Interval field of the Device Configuration register (DCFG.PerFrInt) has been reached in the current microframe.
14	W1C	0x0	ISOOutDrop Isochronous OUT Packet Dropped Interrupt The core sets this bit when it fails to write an isochronous OUT packet into the Rx FIFO because the Rx FIFO does not have enough space to accommodate a maximum packet size packet for the isochronous OUT endpoint.
13	W1C	0x0	EnumDone Enumeration Done The core sets this bit to indicate that speed enumeration is complete. The application must read the Device Status (DSTS) register to obtain the enumerated speed.
12	W1C	0x0	USBRst USB Reset The core sets this bit to indicate that a reset is detected on the USB.
11	W1C	0x0	USBSusp USB Suspend The core sets this bit to indicate that a suspend was detected on the USB. The core enters the Suspended state when there is no activity on the utmi_linestate signal for an extended period of time.
10	W1C	0x0	ErlySusp Early Suspend The core sets this bit to indicate that an Idle state has been detected on the USB for 3 ms.
9	W1C	0x0	I2CINT I2C Interrupt The core sets this interrupt when I2C access is completed on the I2C interface. This field is used only if the I2C interface was enabled . Otherwise, reads return 0.

Bit	Attr	Reset Value	Description
8	W1C	0x0	<p>ULPICKINT ULPI Carkit Interrupt This field is used only if the Carkit interface was enabled . Otherwise, reads return 0. The core sets this interrupt when a ULPI Carkit interrupt is received. The core's PHY sets ULPI Carkit interrupt in UART or Audio mode. I2C Carkit Interrupt (I2CCKINT) This field is used only if the I2C interface was enabled . Otherwise, reads return 0. The core sets this interrupt when a Carkit interrupt is received. The core's PHY sets the I2C Carkit interrupt in Audio mode.</p>
7	RO	0x0	<p>GOUTNakEff Global OUT NAK Effective Indicates that the Set Global OUT NAK bit in the Device Control register DCTL.SGOUTNak), set by the application, has taken effect in the core. This bit can be cleared by writing the Clear Global OUT NAK bit in the Device Control register (DCTL.CGOUTNak).</p>
6	RO	0x0	<p>GINNakEff Global IN Non-Periodic NAK Effective Indicates that the Set Global Non-periodic IN NAK bit in the Device Control register (DCTL.SGNPInNak), set by the application, has taken effect in the core. That is, the core has sampled the Global IN NAK bit set by the application. This bit can be cleared by clearing the Clear Global Nonperiodic IN NAK bit in the Device Control register (DCTL.CGNPInNak). This interrupt does not necessarily mean that a NAK handshake is sent out on the USB. The STALL bit takes precedence over the NAK bit.</p>
5	RO	0x0	<p>NPTxFEmp Non-Periodic Tx FIFO Empty This interrupt is valid only when OTG_EN_DED_TX_FIFO = 0. This interrupt is asserted when the Non-periodic Tx FIFO is either half or completely empty, and there is space for at least one entry to be written to the Non-periodic Transmit Request Queue. The half or completely empty status is determined by the Non-periodic Tx FIFO Empty Level bit in the Core AHB Configuration register(GAHBCFG.NPTxFEmpLvl).</p>

Bit	Attr	Reset Value	Description
4	RO	0x0	RxFLvl RxFIFO Non-Empty Indicates that there is at least one packet pending to be read from the RxFIFO.
3	W1C	0x0	Sof Start of (micro)Frame In Host mode, the core sets this bit to indicate that an SOF (FS), micro-SOF(HS), or Keep-Alive (LS) is transmitted on the USB. The application must write a 1 to this bit to clear the interrupt. In Device mode, in the core sets this bit to indicate that an SOF token has been received on the USB. The application can read the Device Status register to get the current (micro) frame number. This interrupt is seen only when the core is operating at either HS or FS.
2	RO	0x0	OTGInt OTG Interrupt The core sets this bit to indicate an OTG protocol event. The application must read the OTG Interrupt Status (GOTGINT) register to determine the exact event that caused this interrupt. The application must clear the appropriate status bit in the GOTGINT register to clear this bit.
1	W1C	0x0	ModeMis Mode Mismatch Interrupt The core sets this bit when the application is trying to access: A Host mode register, when the core is operating in Device mode; A Device mode register, when the core is operating in Host mode. The register access is completed on the AHB with an OKAY response, but is ignored by the core internally and does not affect the operation of the core.
0	RO	0x0	CurMod Current Mode of Operation Indicates the current mode. 1'b0: Device mode 1'b1: Host mode

USBOTG_GINTMSK

Address: Operational Base + offset (0x0018)

Interrupt Mask Register

Bit	Attr	Reset Value	Description
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Bit	Attr	Reset Value	Description
31	RW	0x0	WkUpIntMsk Resume/Remote Wakeup Detected Interrupt Mask
30	RW	0x0	SessReqIntMsk Session Request/New Session Detected Interrupt Mask
29	RW	0x0	DisconnIntMsk Disconnect Detected Interrupt Mask
28	RW	0x0	ConIDStsChngMsk Connector ID Status Change Mask
27	RW	0x0	LPM_IntMsk LPM Transaction Received Interrupt Mask
26	RW	0x0	PTxFEmpMsk Periodic TxFIFO Empty Mask
25	RW	0x0	HChIntMsk Host Channels Interrupt Mask
24	RW	0x0	PrtIntMsk Host Port Interrupt Mask
23	RW	0x0	ResetDetMsk Reset Detected Interrupt Mask
22	RW	0x0	FetSuspMsk Data Fetch Suspended Mask
21	RW	0x0	incomlPMSk_incompISOOUTMsk Incomplete Periodic Transfer Mask(Host only) Incomplete Isochronous OUT Transfer Mask(Device only)
20	RW	0x0	incompISOINMsk Incomplete Isochronous IN Transfer Mask
19	RW	0x0	OEPIntMsk OUT Endpoints Interrupt Mask
18	RW	0x0	IEPIntMsk IN Endpoints Interrupt Mask
17	RW	0x0	EPMisMsk Endpoint Mismatch Interrupt Mask
16	RW	0x0	RstrDoneIntMsk Restore Done Interrupt Mask This field is valid only when Hibernation feature is enabled.
15	RW	0x0	EOPFMsk End of Periodic Frame Interrupt Mask
14	RW	0x0	ISOOutDropMsk Isochronous OUT Packet Dropped Interrupt Mask
13	RW	0x0	EnumDoneMsk Enumeration Done Mask

Bit	Attr	Reset Value	Description
12	RW	0x0	USBRstMsk USB Reset Mask
11	RW	0x0	USBSuspMsk USB Suspend Mask
10	RW	0x0	ErlySuspMsk Early Suspend Mask
9	RW	0x0	I2CIIntMsk I2C Interrupt Mask
8	RW	0x0	ULPICKINTMsk_I2CCKINTMsk ULPI Carkit Interrupt Mask (ULPICKINTMsk) I2C Carkit Interrupt Mask (I2CCKINTMsk)
7	RW	0x0	GOUTNakEffMsk Global OUT NAK Effective Mask
6	RW	0x0	GINNakEffMsk Global Non-periodic IN NAK Effective Mask
5	RW	0x0	NPTxFEmpMsk Non-periodic TxFIFO Empty Mask
4	RW	0x0	RxFLvIMsk Receive FIFO Non-Empty Mask
3	RW	0x0	SofMsk Start of (micro)Frame Mask
2	RW	0x0	OTGIntMsk OTG Interrupt Mask
1	RW	0x0	ModeMisMsk Mode Mismatch Interrupt Mask
0	RO	0x0	reserved

USBOTG_GRXSTSR

Address: Operational Base + offset (0x001c)

Receive Status Debug Read Register

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24:21	RO	0x0	FN Frame Number (Device Only)This is the least significant 4 bits of the (micro) frame number in which the packet is received on the USB. This field is supported only when isochronous OUT endpoints are supported.

Bit	Attr	Reset Value	Description
20:17	RO	0x0	<p>PktSts Packet Status Indicates the status of the received packet(Host Only)</p> <p>4'b0010: IN data packet received 4'b0011: IN transfer completed (triggers an interrupt) 4'b0101: Data toggle error (triggers an interrupt) 4'b0111: Channel halted (triggers an interrupt)</p> <p>Others: Reserved</p> <p>Indicates the status of the received packet(Device only)</p> <p>4'b0001: Global OUT NAK (triggers an interrupt) 4'b0010: OUT data packet received 4'b0011: OUT transfer completed (triggers an interrupt) 4'b0100: SETUP transaction completed (triggers an interrupt) 4'b0110: SETUP data packet received</p> <p>Others: Reserved</p>
16:15	RO	0x0	<p>DPID Data PID Indicates the Data PID of the received packet</p> <p>2'b00: DATA0 2'b10: DATA1 2'b01: DATA2 2'b11: MDATA</p>
14:4	RW	0x000	<p>BCnt Byte Count Indicates the byte count of the received data packet.</p>
3:0	RO	0x0	<p>ChNum_EPNum Channel Number(Host) Endpoint Number(Device)</p> <p>(Host Only) Indicates the channel number to which the current received packet belongs. (Device Only) Indicates the endpoint number to which the current received packet belongs.</p>

USBOTG_GRXSTSP

Address: Operational Base + offset (0x0020)
Receive Status Read and Pop Register

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24:21	RO	0x0	FN Frame Number (Device Only) This is the least significant 4 bits of the (micro) frame number in which the packet is received on the USB. This field is supported only when isochronous OUT endpoints are supported.
20:17	RO	0x0	PktSts Packet Status Indicates the status of the received packet(Host Only) 4'b0010: IN data packet received 4'b0011: IN transfer completed (triggers an interrupt) 4'b0101: Data toggle error (triggers an interrupt) 4'b0111: Channel halted (triggers an interrupt) Others: Reserved Indicates the status of the received packet(Device only) 4'b0001: Global OUT NAK (triggers an interrupt) 4'b0010: OUT data packet received 4'b0011: OUT transfer completed (triggers an interrupt) 4'b0100: SETUP transaction completed (triggers an interrupt) 4'b0110: SETUP data packet received Others: Reserved
16:15	RO	0x0	DPID Data PID Indicates the Data PID of the received OUT data packet 2'b00: DATA0 2'b10: DATA1 2'b01: DATA2 2'b11: MDATA
14:4	RO	0x000	BCnt Byte Count Indicates the byte count of the received data packet.

Bit	Attr	Reset Value	Description
3:0	RO	0x0	ChNum_EPNum Channel Number(Host) Endpoint Number(Device) (Host Only) Indicates the channel number to which the current received packet belongs. (Device Only) Indicates the endpoint number to which the current received packet belongs.

USBOTG_GRXFSIZ

Address: Operational Base + offset (0x0024)

Receive FIFO Size Register

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:0	RW	0x0000	RxFDep Rx FIFO Depth This value is in terms of 32-bit words. Minimum value is 16, Maximum value is 32,768. The power-on reset value of this register is specified as the Largest Rx Data FIFO Depth. If Enable Dynamic FIFO Sizing? was deselected, these flops are optimized, and reads return the power-on value. If Enable Dynamic FIFO Sizing? was selected , you can write a new value in this field. You can write a new value in this field. Programmed values must not exceed the power-on value.

USBOTG_GNPTXFSIZ

Address: Operational Base + offset (0x0028)

Non-Periodic Transmit FIFO Size Register

Bit	Attr	Reset Value	Description
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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	<p>NPTxFDep Non-periodic TxFIFO For host mode, this field is always valid. For Device mode, this field is valid only when OTG_ENDED_TX_FIFO==0. This value is in terms of 32-bit words. Minimum value is 16 Maximum value is 32,768</p> <p>This field is determined by Enable Dynamic FIFO Sizing.</p> <p>OTG_DFIFO_DYNAMIC = 0: These flops are optimized, and reads return the Power on value.</p> <p>OTG_DFIFO_DYNAMIC = 1: The application can write a new value in this field.</p> <p>Programmed values must not exceed the power-on value.</p> <p>The power-on reset value of this field is specified by OTG_ENDED_TX_FIFO:</p> <p>OTG_ENDED_TX_FIFO = 0: The reset value is the Largest Non-periodic Tx Data FIFO Depth parameter, OTG_TX_NPERIO_DFIFO_DEPTH.</p> <p>OTG_ENDED_TX_FIFO = 1: The reset value is parameter OTG_TX_HNPERIO_DFIFO_DEPTH.</p>
15:0	RW	0x0000	<p>NPTxFSAddr Non-periodic Transmit RAM For host mode, this field is always valid. This field contains the memory start address for Non-periodic Transmit FIFO RAM. This field is determined by Enable Dynamic FIFO Sizing?(OTG_DFIFO_DYNAMIC):</p> <p>OTG_DFIFO_DYNAMIC = 0: These flops are optimized, and reads return the power-on value.</p> <p>OTG_DFIFO_DYNAMIC = 1: The application can write a new value in this field.</p> <p>Programmed values must not exceed the power-on value.</p> <p>The power-on reset value of this field is specified by Largest Rx Data FIFO Depth (parameter OTG_RX_DFIFO_DEPTH).</p>

USBOTG_GNPTXSTS

Address: Operational Base + offset (0x002c)

Non-Periodic Transmit FIFO/Queue Status Register

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RO	0x00	<p>NPTxQTop Top of the Non-periodic Transmit Request Queue</p> <p>Entry in the Non-periodic Tx Request Queue that is currently being processed by the MAC.</p> <p>Bits [30:27]: Channel/endpoint number</p> <p>Bits [26:25]:</p> <ul style="list-style-type: none"> 2'b00: IN/OUT token 2'b01: Zero-length transmit packet (device IN/host OUT) 2'b10: PING/CSPLIT token 2'b11: Channel halt command <p>Bit [24]: Terminate (last entry for selected channel/endpoint)</p>
23:16	RO	0x00	<p>NPTxQSpAvail Non-periodic Transmit Request Queue Space Available</p> <p>Indicates the amount of free space available in the Non-periodic Transmit Request Queue.</p> <p>This queue holds both IN and OUT requests in Host mode. Device mode has only IN requests.</p> <ul style="list-style-type: none"> 8'h0: Non-periodic Transmit Request Queue is full 8'h1: 1 location available 8'h2: 2 locations available n: n locations available (0 <=n <= 8) Others: Reserved
15:0	RO	0x0000	<p>NPTxFSpAvail Non-periodic TxFIFO Space Avail</p> <p>Indicates the amount of free space available in the Non-periodic TxFIFO. Values are in terms of 32-bit words.</p> <ul style="list-style-type: none"> 16'h0: Non-periodic TxFIFO is full 16'h1: 1 word available 16'h2: 2 words available 16'hn: n words available (where 0 <=n <=32,768) 16'h8000: 32,768 words available Others: Reserved

USBOTG_GI2CCTL

Address: Operational Base + offset (0x0030)

I2C Address Register

Bit	Attr	Reset Value	Description
31	RWSC	0x0	BsyDne I2C Busy/Done The application sets this bit to 1'b1 to start a request on the I2C interface. When the transfer is complete, the core de-asserts this bit to 1'b0. As long as the bit is set, indicating that the I2C interface is busy, the application cannot start another request on the interface.
30	RW	0x0	RW Read/Write Indicator Indicates whether a read or write register transfer must be performed on the interface. Read/write bursting is not supported for registers. 1'b1: Read 1'b0: Write
29	RO	0x0	reserved
28	RW	0x1	I2CDatSe0 I2C DatSe0 USB Mode Selects the FS interface USB mode. 1'b1: VP_VM USB mode 1'b0: DAT_SE0 USB mode
27:26	RW	0x0	I2CDevAdr I2C Device Address Selects the address of the I2C Slave on the USB 1.1 full-speed serial transceiver that the core uses for OTG signaling. 2'b00: 7'h2C 2'b01: 7'h2D 2'b10: 7'h2E 2'b11: 7'h2F
25	RW	0x0	I2CSuspCtl I2C Suspend Control Selects how Suspend is connected to a full-speed transceiver in I2C mode. 1'b0: Use the dedicated utmi_suspend_n pin 1'b1: Use an I2C write to program the Suspend bit in the PHY register

Bit	Attr	Reset Value	Description
24	RO	0x1	Ack I2C ACK Indicates whether an ACK response was received from the I2C Slave. This bit is valid when BsyDne is cleared by the core, after application has initiated an I2C access. 1'b0: NAK 1'b1: ACK
23	RW	0x0	I2CEn I2C Enable Enables the I2C Master to initiate I2C transactions on the I2C interface
22:16	RW	0x00	Addr I2C Address This is the 7-bit I2C device address used by software to access any external I2C Slave, including the I2C Slave on a USB 1.1 OTG full-speed serial transceiver. Software can change this address to access different I2C Slaves.
15:8	RW	0x00	RegAddr I2C Register Addr This field programs the address of the register to be read from or written to.
7:0	RW	0x00	RWData I2C Read/Write Data After a register read operation, this field holds the read data for the application. During a write operation, the application can use this register to program the write data to be written to a register. During writes, this field holds the write data.

USBOTG_GPVNDCTL

Address: Operational Base + offset (0x0034)

PHY Vendor Control Register

Bit	Attr	Reset Value	Description
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Bit	Attr	Reset Value	Description
31	RWSC	0x0	DisUlpiDrv Disable ULPI Drivers This field is used only if the Carkit interface was enabled (OTG_ULPI_CARKIT = 1). Otherwise, reads return 0. The application sets this bit when it has finished processing the ULPI Carkit Interrupt (GINTSTS.ULPICKINT). When set, the Otg core disables drivers for output signals and masks input signal for the ULPI interface. Otg clears this bit before enabling the ULPI interface.
30:28	RO	0x0	reserved
27	RWSC	0x0	VStsDone VStatus Done The core sets this bit when the vendor control access is done. This bit is cleared by the core when the application sets the New Register Request bit (bit 25).
26	RO	0x0	VStsBsy VStatus Busy The core sets this bit when the vendor control access is in progress and clears this bit when done.
25	RWSC	0x0	NewRegReq New Register Request The application sets this bit for a new vendor control access.
24:23	RO	0x0	reserved
22	RW	0x0	RegWr Register Write Set this bit for register writes, and clear it for register reads.
21:16	RW	0x00	RegAddr Register Address The 6-bit PHY register address for immediate PHY Register Set access. Set to 6'h2F for Extended PHY Register Set access.
15:8	RW	0x00	VCtrl UTMI+ Vendor Control Register Address The 4-bit register address a vendor defined 4-bit parallel output bus. Bits 11:8 of this field are placed on utmi_vcontrol[3:0]. ULPI Extended Register Address (ExtRegAddr) The 6-bit PHY extended register address.

Bit	Attr	Reset Value	Description
7:0	RW	0x00	RegData Register Data Contains the write data for register write. Read data for register read, valid when VStatus Done is set.

USBOTG_GGPIO

Address: Operational Base + offset (0x0038)

General Purpose Input/Output Register

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	GPO General Purpose Output This field is driven as an output from the core, gp_o[15:0]. The application can program this field to determine the corresponding value on the gp_o[15:0] output.
15:0	RO	0x0000	GPI General Purpose Input This field's read value reflects the gp_i[15:0] core input value.

USBOTG_GUID

Address: Operational Base + offset (0x003c)

User ID Register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	UserID Application-programmable ID field.

USBOTG_GSNPSID

Address: Operational Base + offset (0x0040)

Core ID Register

Bit	Attr	Reset Value	Description
31:0	RO	0x00004f54	CoreID Release number of the core being used

USBOTG_GHWCFG1

Address: Operational Base + offset (0x0044)

User HW Config1 Register

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	<p>epdir Endpoint Direction This 32-bit field uses two bits per endpoint to determine the endpoint direction.</p> <p>Endpoint Bits [31:30]: Endpoint 15 direction Bits [29:28]: Endpoint 14 direction ... Bits [3:2]: Endpoint 1 direction Bits[1:0]: Endpoint 0 direction (always BIDIR)</p> <p>Direction 2'b00: BIDIR (IN and OUT) endpoint 2'b01: IN endpoint 2'b10: OUT endpoint 2'b11: Reserved</p>

USBOTG_GHWCFG2

Address: Operational Base + offset (0x0048)

User HW Config2 Register

Bit	Attr	Reset Value	Description
31	RO	0x0	OTG_ENABLE_IC_USB IC_USB mode specified for mode of operation (parameter OTG_ENABLE_IC_USB). To choose IC_USB_MODE, both OTG_FSPHY_INTERFACE and OTG_ENABLE_IC_USB must be 1.
30:26	RO	0x00	TknQDepth Device Mode IN Token Sequence Learning Queue Depth Range: 0-30
25:24	RO	0x0	PTxQDepth Host Mode Periodic Request Queue Depth 2'b00: 2 2'b01: 4 2'b10: 8 Others: Reserved
23:22	RO	0x0	NPTxQDepth Non-periodic Request Queue Depth 2'b00: 2 2'b01: 4 2'b10: 8 Others: Reserved
21	RO	0x0	reserved

Bit	Attr	Reset Value	Description
20	RO	0x0	MultiProcIntrpt Multi-Processor Interrupt Enabled 1'b0: No 1'b1: Yes
19	RO	0x0	DynFifoSizing Dynamic FIFO Sizing Enabled 1'b0: No 1'b1: Yes
18	RO	0x0	PerioSupport Periodic OUT Channels Supported in Host Mode 1'b0: No 1'b1: Yes
17:14	RO	0x0	NumHstChnl Number of Host Channels Indicates the number of host channels supported by the core in Host mode. The range of this field is 0-15: 0 specifies 1 channel, 15 specifies 16 channels.
13:10	RO	0x0	NumDevEps Number of Device Endpoints Indicates the number of device endpoints supported by the core in Device mode in addition to control endpoint 0. The range of this field is 1-15.
9:8	RO	0x0	FSPhyType Full-Speed PHY Interface Type 2'b00: Full-speed interface not supported 2'b01: Dedicated full-speed interface 2'b10: FS pins shared with UTMI+ pins 2'b11: FS pins shared with ULPI pins
7:6	RO	0x0	HSPhyType High-Speed PHY Interface Type 2'b00: High-Speed interface not supported 2'b01: UTMI+ 2'b10: ULPI 2'b11: UTMI+ and ULPI
5	RO	0x0	SingPnt Point-to-Point 1'b0: Multi-point application (hub and split support) 1'b1: Single-point application (no hub and no split support)

Bit	Attr	Reset Value	Description
4:3	RO	0x0	OtgArch Architecture 2'b00: Slave-Only 2'b01: External DMA 2'b10: Internal DMA Others: Reserved
2:0	RO	0x0	OtgMode Mode of Operation 3'b000: HNP- and SRP-Capable OTG (Host and Device) 3'b001: SRP-Capable OTG (Host and Device) 3'b010: Non-HNP and Non-SRP Capable OTG (Host and Device) 3'b011: SRP-Capable Device 3'b100: Non-OTG Device 3'b101: SRP-Capable Host 3'b110: Non-OTG Host Others: Reserved

USBOTG_GHWCFG3

Address: Operational Base + offset (0x004c)

User HW Config3 Register

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	DfifoDepth DFIFO Depth This value is in terms of 32-bit words. Minimum value is 32 Maximum value is 32,768
15	RO	0x0	OTG_ENABLE_LPM LPM mode specified for Mode of Operation (parameter OTG_ENABLE_LPM).
14	RO	0x0	OTG_BC_SUPPORT This bit indicates the HS OTG controller support for Battery Charger. 1'b0: No Battery Charger Support 1'b1: Battery Charger support present.
13	RO	0x0	Reserved
12	RO	0x0	OTG_AD_P_SUPPORT This bit indicates whether ADP logic is present within or external to the HS OTG controller 1'b0: No ADP logic present with HSOTG controller 1'b1: ADP logic is present along with HSOTG controller.

Bit	Attr	Reset Value	Description
11	RO	0x0	RstType Reset Style for Clocked always Blocks in RTL 1'b0: Asynchronous reset is used in the core 1'b1: Synchronous reset is used in the core
10	RO	0x0	OptFeature Optional Features Removed Indicates whether the User ID register, GPIO interface ports, and SOF toggle and counter ports were removed for gate count optimization by enabling Remove Optional Features? 1'b0: No 1'b1: Yes
9	RO	0x0	VndctlSupt Vendor Control Interface Support 1'b0: Vendor Control Interface is not available on the core. 1'b1: Vendor Control Interface is available.
8	RO	0x0	I2CIntSel I2C Selection 1'b0: I2C Interface is not available on the core. 1'b1: I2C Interface is available on the core.
7	RO	0x0	OtgEn OTG Function Enabled The application uses this bit to indicate the Otg core's OTG capabilities. 1'b0: Not OTG capable 1'b1: OTG Capable
6:4	RO	0x0	PktSizeWidth Width of Packet Size Counters 3'b000: 4 bits 3'b001: 5 bits 3'b010: 6 bits 3'b011: 7 bits 3'b100: 8 bits 3'b101: 9 bits 3'b110: 10 bits Others: Reserved

Bit	Attr	Reset Value	Description
3:0	RO	0x0	XferSizeWidth Width of Transfer Size Counters 4'b0000: 11 bits 4'b0001: 12 bits ... 4'b1000: 19 bits Others: Reserved

USBOTG_GHWCFG4

Address: Operational Base + offset (0x0050)

User HW Config4 Register

Bit	Attr	Reset Value	Description
31	RO	0x0	SGDMA Scatter/Gather DMA 1'b1: Dynamic configuration
30	RO	0x0	SGDMACon Scatter/Gather DMA configuration 1'b0: Non-Scatter/Gather DMA configuration 1'b1: Scatter/Gather DMA configuration
29:26	RO	0x0	INEps Number of Device Mode IN Endpoints Including Control Endpoint Range 0 -15 0:1 IN Endpoint 1:2 IN Endpoints 15:16 IN Endpoints
25	RW	0x0	DedFifoMode Enable Dedicated Transmit FIFO for device IN Endpoints 1'b0: Dedicated Transmit FIFO Operation not enabled. 1'b1: Dedicated Transmit FIFO Operation enabled.
24	RW	0x0	SessEndFltr session_end Filter Enabled 1'b0: No filter 1'b1: Filter
23	RW	0x0	BValidFltr "b_valid" Filter Enabled 1'b0: No filter 1'b1: Filter

Bit	Attr	Reset Value	Description
22	RO	0x0	AValidFltr "a_valid" Filter Enabled 1'b0: No filter 1'b1: Filter
21	RO	0x0	VBusValidFltr "vbus_valid" Filter Enabled 1'b0: No filter 1'b1: Filter
20	RO	0x0	IddgFltr "iddig" Filter Enable 1'b0: No filter 1'b1: Filter
19:16	RO	0x0	NumCtlEps Number of Device Mode Control Endpoints in Addition to Endpoint Range: 0-15
15:14	RO	0x0	PhyDataWidth UTMI+ PHY/ULPI-to-Internal UTMI+ Wrapper Data Width When a ULPI PHY is used, an internal wrapper converts ULPI to UTMI+. 2'b00: 8 bits 2'b01: 16 bits 2'b10: 8/16 bits, software selectable Others: Reserved
13:7	RO	0x0	reserved
6	RO	0x0	EnHiber Enable Hibernation 1'b0: Hibernation feature not enabled 1'b1: Hibernation feature enabled
5	RO	0x0	AhbFreq Minimum AHB Frequency Less Than 60 MHz 1'b0: No 1'b1: Yes
4	RO	0x0	EnParPwrDown Enable Partial Power Down 1'b0: Partial Power Down Not Enabled 1'b1: Partial Power Down Enabled
3:0	RO	0x0	NumDevPerioEps Number of Device Mode Periodic IN Endpoints Range: 0-15

USBOTG_GLPMCFG

Address: Operational Base + offset (0x0054)
Core LPM Configuration Register

Bit	Attr	Reset Value	Description
31	RW	0x0	Reserved
30	RW	0x0	Reserved
29:28	RO	0x0	reserved
27:25	RO	0x0	LPM_RetryCnt_Stats LPM Retry Count Status Number of LPM host retries remaining to be transmitted for the current LPM sequence.
24	RW	0x0	SndLPM Send LPM Transaction Host Mode: When the application software sets this bit, an LPM transaction containing two tokens, EXT and LPM, is sent. The hardware clears this bit once a valid response (STALL, NYET, or ACK) is received from the device or the core has finished transmitting the programmed number of LPM retries. Note: This bit must only be set when the host is connected to a local port.
23:21	RWSC	0x0	LPM_Retry_Cnt LPM Retry Count When the device gives an ERROR response, this is the number of additional LPM retries that the host performs until a valid device response (STALL, NYET, or ACK) is received.
20:17	RW	0x0	LPM_Chnl_Indx LPM Channel Index The channel number on which the LPM transaction must be applied while sending an LPM transaction to the local device. Based on the LPM channel index, the core automatically inserts the device address and endpoint number programmed in the corresponding channel into the LPM transaction.
16	RO	0x0	L1ResumeOK Sleep State Resume OK Indicates that the application or host can start a resume from the Sleep state. This bit is valid in the LPM Sleep (L1) state. It is set in Sleep mode after a delay of 50 us (TL1Residency). The bit is reset when SlpSts is 0 1'b1: The application/core can start resume from the Sleep state 1'b0: The application/core cannot start resume from the Sleep state

Bit	Attr	Reset Value	Description
15	RO	0x0	<p>SlpSts Port Sleep Status Device Mode: This bit is set as long as a Sleep condition is present on the USB bus. The core enters the Sleep state when an ACK response is sent to an LPM transaction and the timer TL1TokenRetry. has expired. To stop the PHY clock, the application must set the Port Clock Stop bit, which asserts the PHY Suspend input pin. The application must rely on SlpSts and not ACK in CoreL1Res to confirm transition into sleep.</p> <p>The core comes out of sleep: When there is any activity on the USB line_state When the application writes to the Remote Wakeup Signaling bit in the Device Control register (DCTL.RmtWkUpSig) or when the application resets or soft-disconnects the device.</p> <p>Host Mode: The host transitions to the Sleep (L1) state as a sideeffect of a successful LPM transaction by the core to the local port with an ACK response from the device. The read value of this bit reflects the port's current sleep status. The core clears this bit after: The core detects a remote L1 Wakeup signal The application sets the Port Reset bit or the Port L1Resume bit in the HPRT register or The application sets the L1Resume/ Remote Wakeup Detected Interrupt bit or Disconnect Detected Interrupt bit in the Core Interrupt register (GINTSTS.L1WkUpInt or GINTSTS.DisconnInt, respectively).</p> <p>Values: 1'b0: Core not in L1 1'b1: Core in L1</p>
14:13	RO	0x0	<p>CoreL1Res LPM Response Device Mode: The core's response to the received LPM transaction is reflected in these two bits. Host Mode: The handshake response received from the local device for LPM transaction.</p> <p>2'b11: ACK 2'b10: NYET 2'b01: STALL 2'b00: ERROR (No handshake response)</p>

Bit	Attr	Reset Value	Description																																																			
12:8	RW	0x00	<p>HIRD_Thres HIRD Threshold Device Mode: The core asserts L1SuspendM to put the PHY into Deep Low-Power mode in L1 when the HIRD value is greater than or equal to the value defined in this field (GLPMCFG.HIRD_Thres[3:0]), and HIRD_Thres[4] is set to 1'b1.</p> <p>Host Mode: The core asserts L1SuspendM to put the PHY into Deep Low-Power mode in L1 when HIRD_Thres[4] is set to 1'b1. HIRD_Thres[3:0] specifies the time for which resume signaling is to be reflected by the host TL1HubDrvResume2) on the USB when it detects device-initiated resume. HIRD_Thres must not be programmed with a value greater than 4'b1100 in Host mode, because this exceeds maximum T_{L1HubDrvResume2}.</p> <table> <thead> <tr> <th>No</th> <th>HIRD_Thres[3:0]</th> <th>resume time(us)</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>4'b0000</td> <td>60</td> </tr> <tr> <td>2</td> <td>4'b0001</td> <td>135</td> </tr> <tr> <td>3</td> <td>4'b0010</td> <td>210</td> </tr> <tr> <td>4</td> <td>4'b0011</td> <td>285</td> </tr> <tr> <td>5</td> <td>4'b0100</td> <td>360</td> </tr> <tr> <td>6</td> <td>4'b0101</td> <td>435</td> </tr> <tr> <td>7</td> <td>4'b0110</td> <td>510</td> </tr> <tr> <td>8</td> <td>4'b0111</td> <td>585</td> </tr> <tr> <td>9</td> <td>4'b1000</td> <td>660</td> </tr> <tr> <td>10</td> <td>4'b1001</td> <td>735</td> </tr> <tr> <td>11</td> <td>4'b1010</td> <td>810</td> </tr> <tr> <td>12</td> <td>4'b1011</td> <td>885</td> </tr> <tr> <td>13</td> <td>4'b1100</td> <td>960</td> </tr> <tr> <td>14</td> <td>4'b1101</td> <td>invalid</td> </tr> <tr> <td>15</td> <td>4'b1110</td> <td>invalid</td> </tr> <tr> <td>16</td> <td>4'b1111</td> <td>invalid</td> </tr> </tbody> </table>	No	HIRD_Thres[3:0]	resume time(us)	1	4'b0000	60	2	4'b0001	135	3	4'b0010	210	4	4'b0011	285	5	4'b0100	360	6	4'b0101	435	7	4'b0110	510	8	4'b0111	585	9	4'b1000	660	10	4'b1001	735	11	4'b1010	810	12	4'b1011	885	13	4'b1100	960	14	4'b1101	invalid	15	4'b1110	invalid	16	4'b1111	invalid
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Bit	Attr	Reset Value	Description
7	RW	0x0	<p>EnbISlpM Enable utmi_sleep_n For ULPI interface: The application uses this bit to write to the function control [7] in the L1 state, to enable the PHY to go into Low Power mode. For the host, this bit is valid only in Local Device mode.</p> <p>1'b0: Writes to the ULPI Function Control Bit [7] are disabled.</p> <p>1'b1: The core is enabled to write to the ULPI Function Control Bit [7], which enables the PHY to enter Low-Power mode.</p> <p>Note: When a ULPI interface is configured, enabling this bit results in a write to Bit 7 of the ULPI Function Control register. The ULPI PHY supports writing to this bit, and in the L1 state asserts SleepM when utmi_l1_suspend_n cannot be asserted. When a ULPI interface is configured, this bit must always be set if you are using the ULPI PHY. Note: For ULPI interface, do not clear this bit during the resume. For all other interfaces: The application uses this bit to control utmi_sleep_n assertion to the PHY in the L1 state. For the host, this bit is valid only in Local Device mode.</p> <p>1'b0: utmi_sleep_n assertion from the core is not transferred to the external PHY.</p> <p>1'b1: utmi_sleep_n assertion from the core is transferred to the external PHY when utmi_l1_suspend_n cannot be asserted.</p>
6	RW	0x0	<p>bRemoteWake RemoteWakeEnable Host Mode: The remote wakeup value to be sent in the LPM transaction's wIndex field. Device Mode: This field is updated with the received bRemoteWake LPM token's bmAttribute when an ACK/NYET/STALL response is sent to an LPM transaction.</p>

Bit	Attr	Reset Value	Description																																																			
5:2	RW	0x0	<p>HIRD Host-Initiated Resume Duration Host Mode: The value of HIRD to be sent in an LPM transaction. This value is also used to initiate resume for a duration $.T_{L1HubDrvResume1}$ for host initiated resume. Device Mode: This field is updated with the Received LPM Token HIRD bmAttribute when an ACK/NYET/STALL response is sent to an LPM transaction</p> <table> <thead> <tr> <th>Sl. No</th> <th>HIRD[3:0]</th> <th>THIRD (us)</th> </tr> </thead> <tbody> <tr><td>1</td><td>4'b0000</td><td>50</td></tr> <tr><td>2</td><td>4'b0001</td><td>125</td></tr> <tr><td>3</td><td>4'b0010</td><td>200</td></tr> <tr><td>4</td><td>4'b0011</td><td>275</td></tr> <tr><td>5</td><td>4'b0100</td><td>350</td></tr> <tr><td>6</td><td>4'b0101</td><td>425</td></tr> <tr><td>7</td><td>4'b0110</td><td>500</td></tr> <tr><td>8</td><td>4'b0111</td><td>575</td></tr> <tr><td>9</td><td>4'b1000</td><td>650</td></tr> <tr><td>10</td><td>4'b1001</td><td>725</td></tr> <tr><td>11</td><td>4'b1010</td><td>800</td></tr> <tr><td>12</td><td>4'b1011</td><td>875</td></tr> <tr><td>13</td><td>4'b1100</td><td>950</td></tr> <tr><td>14</td><td>4'b1101</td><td>1025</td></tr> <tr><td>15</td><td>4'b1110</td><td>1100</td></tr> <tr><td>16</td><td>4'b1111</td><td>1175</td></tr> </tbody> </table>	Sl. No	HIRD[3:0]	THIRD (us)	1	4'b0000	50	2	4'b0001	125	3	4'b0010	200	4	4'b0011	275	5	4'b0100	350	6	4'b0101	425	7	4'b0110	500	8	4'b0111	575	9	4'b1000	650	10	4'b1001	725	11	4'b1010	800	12	4'b1011	875	13	4'b1100	950	14	4'b1101	1025	15	4'b1110	1100	16	4'b1111	1175
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Bit	Attr	Reset Value	Description
1	RW	0x0	<p>AppL1Res LPM response programmed by application Handshake response to LPM token pre-programmed by device application software. The response depends on GLPMCFG.LPMCap. If GLPMCFG.LPMCap is 1'b0, the core always responds with a NYET. If GLPMCFG.LPMCap is 1'b1, the core responds as follows:</p> <p>1'b1: ACK. Even though an ACK is pre-programmed, the core responds with an ACK only on a successful LPM transaction. The LPM transaction is successful if: There are no PID/CRC5 errors in both the EXT token and the LPM token (else ERROR); A valid bLinkState = 0001B (L1) is received in the LPM transaction (else STALL); No data is pending in the Transmit queue (else NYET)</p> <p>1'b0: NYET. The pre-programmed software bit is overridden for response to LPM token when: (1) The received bLinkState is not L1 (STALL response); (2) An error is detected in either of the LPM token packets due to corruption (ERROR response).</p>
0	RW	0x0	<p>LPMCap LPM-Capable The application uses this bit to control the OTG core LPM capabilities. If the core operates as a non-LPM-capable host, it cannot request the connected device/hub to activate LPM mode. If the core operates as a non-LPM-capable device, it cannot respond to any LPM transactions.</p> <p>1'b0: LPM capability is not enabled. 1'b1: LPM capability is enabled.</p> <p>This bit is writable only if an LPM mode was specified for Mode of Operation (parameter OTG_ENABLE_LPM). Otherwise, reads return 0.</p>

USBOTG_GPWRDN

Address: Operational Base + offset (0x0058)

Global Power Down Register

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved

Bit	Attr	Reset Value	Description
28:24	RO	0x00	<p>MultValIdBC Multi Valued ID pin Battery Charger ACA inputs in the following order: Bit 26 - rid_float. Bit 25 - rid_gnd Bit 24 - rid_a Bit 23 - rid_b Bit 22 - rid_c These bits are present only if OTG_BC_SUPPORT = 1. Otherwise, these bits are reserved and will read 5'h0.</p>
23	W1C	0x0	<p>ADPInt ADP Interupt This bit is set whenever there is a ADP event.</p>
22	RO	0x0	<p>BSessVld B Session Valid This field reflects the B session valid status signal from the PHY. 1'b0: B-Valid is 0. 1'b1: B-Valid is 1. This bit is valid only when GPWRDN.PMUActv is 1.</p>
21	RO	0x0	<p>IDDIG This bit indicates the status of the signal IDDIG. The application must read this bit after receiving GPWRDN.StsChngInt and decode based on the previous value stored by the application. Indicates the current mode. 1'b1: Device mode 1'b0: Host mode This bit is valid only when GPWRDN.PMUActv is 1.</p>
20:19	RO	0x0	<p>LineState This field indicates the current linestate on USB as seen by the PMU module. 2'b00: DM = 0, DP = 0. 2'b01: DM = 0, DP = 1. 2'b10: DM = 1, DP = 0. 2'b11: Not-defined. This bit is valid only when GPWRDN.PMUActv is 1.</p>
18	RW	0x0	<p>StsChngIntMsk Mask For StsChng Interrupt</p>

Bit	Attr	Reset Value	Description
17	W1C	0x0	<p>StsChngInt This field indicates a status change in either the IDDIG or BSessVld signal. 1'b0: No Status change 1'b1: status change detected After receiving this interrupt the application should read the GPWRDN register and interpret the change in IDDIG or BSesVld with respect to the previous value stored by the application.</p>
16	RW	0x0	<p>SRPDetectMsk Mask For SRPDetect Interrupt</p>
15	W1C	0x0	<p>SRPDetect This field indicates that SRP has been detected by the PMU. This field generates an interrupt. After detecting SRP during hibernation the application should not restore the core. The application should get into the initialization process. 1'b0: SRP not detected 1'b1: SRP detected</p>
14	RW	0x0	<p>ConnDetMsk Mask for ConnectDet interrupt This bit is valid only when OTG_EN_PWROPT = 2.</p>
13	W1C	0x0	<p>ConnectDet This field indicates that a new connect has been detected 1'b0: Connect not detected 1'b1: Connect detected This bit is valid only when OTG_EN_PWROPT = 2.</p>
12	RW	0x0	<p>DisconnectDetectMsk Mask For DisconnectDetect Interrupt This bit is valid only when OTG_EN_PWROPT = 2.</p>
11	W1C	0x0	<p>DisconnectDetect This field indicates that Disconnect has been detected by the PMU. This field generates an interrupt. After detecting disconnect during hibernation the application must not restore the core, but instead start the initialization process. 1'b0: Disconnect not detected 1'b1: Disconnect detected This bit is valid only when OTG_EN_PWROPT = 2.</p>
10	RW	0x0	<p>ResetDetMsk Mask For ResetDetected interrupt.This bit is valid only when OTG_EN_PWROPT = 2.</p>

Bit	Attr	Reset Value	Description
9	W1C	0x0	<p>ResetDetected</p> <p>This field indicates that Reset has been detected by the PMU module. This field generates an interrupt.</p> <p>1'b0: Reset Not Detected 1'b1: Reset Detected</p> <p>This bit is valid only when OTG_EN_PWROPT = 2.</p>
8	RW	0x0	<p>LineStageChangeMsk</p> <p>Mask For LineStateChange interrupt</p> <p>This bit is valid only when OTG_EN_PWROPT = 2.</p>
7	W1C	0x0	<p>LnStsChng</p> <p>Line State Change</p> <p>This interrupt is asserted when there is a Linestate Change detected by the PMU. The application should read GPWRDN.Linestate to determine the current linestate on USB.</p> <p>1'b0: No LineState change on USB 1'b1: LineState change on USB</p> <p>This bit is valid only when GPWRDN.PMUActv is 1. This bit is valid only when OTG_EN_PWROPT = 2.</p>
6	RW	0x0	<p>DisableVBUS</p> <p>The application should program this bit if HPRT0.PrtPwr was programmed to 0 before entering Hibernation. This is to indicate PMU whether session was ended before entering Hibernation.</p> <p>1'b0: HPRT0.PrtPwr was not programed to 0. 1'b1: HPRT0.PrtPwr was programmed to 0.</p>
5	RW	0x0	<p>PwrDnSwtch</p> <p>Power Down Switch</p> <p>This bit indicates to the OTG core VDD switch is in ON/OFF state</p> <p>1'b0: OTG is in ON state 1'b1: OTG is in OFF state</p> <p>Note: This bit must not be written to during normal mode of operation.</p>
4	RW	0x0	<p>PwrDnRst_n</p> <p>Power Down ResetN</p> <p>The application must program this bit to reset the DWC OTG core during the Hibernation exit process or during ADP when powering up the core (in case the DWC OTG core was powered off during ADP process).</p> <p>1'b1: OTG is in normal operation 1'b0: reset OTG</p> <p>Note: This bit must not be written to during normal mode of operation.</p>

Bit	Attr	Reset Value	Description
3	RW	0x0	<p>PwrDnClmp Power Down Clamp</p> <p>The application must program this bit to enable or disable the clamps to all the outputs of the DWC OTG core module to prevent the corruption of other active logic.</p> <p>1'b0: Disable PMU power clamp 1'b1: Enable PMU power clamp</p>
2	RW	0x0	<p>Restore</p> <p>The application should program this bit to enable or disable restore mode from the PMU module.</p> <p>1'b0: OTG in normal mode of operation 1'b1: OTG in restore mode</p> <p>Note: This bit must not be written to during normal mode of operation. This bit is valid only when OTG_EN_PWR_OPT = 2.</p>
1	RW	0x0	<p>PMUActv PMU Active</p> <p>This is bit is to enable or disable the PMU logic.</p> <p>1'b0: Disable PMU module 1'b1: Enable PMU module</p> <p>Note: This bit must not be written to during normal mode of operation.</p>
0	RW	0x0	<p>PMUIntSel PMU Interrupt Select</p> <p>When the hibernation functionality is selected using the configuration option OTG_EN_PWR_OPT = 2, a write to this bit with 1'b1 enables the PMU to generate interrupts to the application. During this state all interrupts from the core module are blocked to the application. Note: This bit must be set to 1'b1 before the core is put into hibernation</p> <p>1'b0: Internal OTG_core interrupt is selected 1'b1: the external OTG_pmu interrupt is selected</p> <p>Note: This bit must not be written to during normal mode of operation.</p>

USBOTG_GDFIFO CFG

Address: Operational Base + offset (0x005c)

Global DFIFO Software Config Register

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	<p>EPInfoBaseAddr</p> <p>This field provides the start address of the EP info controller.</p>

Bit	Attr	Reset Value	Description
15:0	RW	0x0000	GDFIFOcfg This field is for dynamic programming of the DFIFO Size. This value takes effect only when the application programs a non-zero value to this register. The core does not have any corrective logic if the FIFO sizes are programmed incorrectly.

USBOTG_GADPCTL

Address: Operational Base + offset (0x0060)

ADP Timer,Control and Status Register

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:27	RWSC	0x0	AR Access Request 2'b00 Read/Write Valid (updated by the core) 2'b01 Read 2'b10 Write 2'b11 Reserved
26	RW	0x0	AdpTmoutMsk ADP Timeout Interrupt Mask When this bit is set, it unmasks the interrupt because of AdpTmoutInt. This bit is valid only if OTG_Ver = 1'b1(GOTGCTL[20]).
25	RW	0x0	AdpSnsIntMsk ADP Sense Interrupt Mask When this bit is set, it unmasks the interrupt due to AdpSnsInt. This bit is valid only if OTG_Ver = 1'b1(GOTGCTL[20]).
24	RW	0x0	AdpPrbIntMsk ADP Probe Interrupt Mask When this bit is set, it unmasks the interrupt due to AdpPrbInt. This bit is valid only if OTG_Ver = 1'b1(GOTGCTL[20]).
23	W1C	0x0	AdpTmoutInt ADP Timeout Interrupt This bit is relevant only for an ADP probe. When this bit is set, it means that the ramp time has completed (GADPCTL.RTIM has reached its terminal value of 0x7FF). This is a debug feature that allows software to read the ramp time after each cycle. This bit is valid only if OTG_Ver = 1'b1.

Bit	Attr	Reset Value	Description
22	W1C	0x0	AdpSnsInt ADP Sense Interrupt When this bit is set, it means that the VBUS voltage is greater than VadpSns value or VadpSns is reached. This bit is valid only if OTG_Ver = 1'b1 (GOTGCTL[20]).
21	W1C	0x0	AdpPrbInt ADP Probe Interrupt When this bit is set, it means that the VBUS voltage is greater than VadpPrb or VadpPrb is reached. This bit is valid only if OTG_Ver = 1'b1 (GOTGCTL[20]).
20	RW	0x0	ADPEn ADP Enable When set, the core performs either ADP probing or sensing based on EnaPrb or EnaSns. This bit is valid only if OTG_Ver = 1'b1 (GOTGCTL[20]).
19	RWSC	0x0	ADPRes ADP Reset When set, ADP controller is reset. This bit is auto-cleared after the reset procedure is complete in ADP controller. This bit is valid only if OTG_Ver = 1'b1 (GOTGCTL[20]).
18	RW	0x0	EnaSns Enable Sense When programmed to 1'b1, the core performs a sense operation. This bit is valid only if OTG_Ver = 1'b1 (GOTGCTL[20]).
17	RW	0x0	EnaPrb Enable Probe When programmed to 1'b1, the core performs a probe operation. This bit is valid only if OTG_Ver = 1'b1 (GOTGCTL[20]).

Bit	Attr	Reset Value	Description
16:6	RO	0x000	<p>RTIM RAMP TIME</p> <p>These bits capture the latest time it took for VBUS to ramp from VADP_SINK to VADP_PRB. The bits are defined in units of 32 kHz clock cycles as follows:</p> <ul style="list-style-type: none"> 3'b000 - 1 cycles 3'b001 - 2 cycles 3'b010 - 3 cycles and so on till 0x7FF - 2048 cycles <p>A time of 1024 cycles at 32 kHz corresponds to a time of 32 msec.</p> <p>(Note for scaledown ramp_timeout = prb_delta == 2'b00 => 200 cycles prb_delta == 2'b01 => 100 cycles prb_delta == 2'b01 => 50 cycles prb_delta == 2'b01 => 25 cycles.)</p>
5:4	RW	0x0	<p>PrbPer Probe Period</p> <p>These bits sets the TadpPrd as follows:</p> <ul style="list-style-type: none"> 2'b00 - 0.625 to 0.925 sec (typical 0.775 sec) 2'b01 - 1.25 to 1.85 sec (typical 1.55 sec) 2'b10 - 1.9 to 2.6 sec (typical 2.275 sec) 2'b11 - Reserved <p>(PRB_PER is also scaledown prb_per== 2'b00 => 400 ADP clocks prb_per== 2'b01 => 600 ADP clocks prb_per== 2'b10 => 800 ADP clocks prb_per==2'b11 => 1000 ADP clocks)</p>
3:2	RW	0x0	<p>PrbDelta Probe Delta</p> <p>These bits set the resolution for RTIM value. The bits are defined in units of 32 kHz clock cycles as follows:</p> <ul style="list-style-type: none"> 2'b00 - 1 cycles 2'b01 - 2 cycles 2'b10 - 3 cycles 2'b11 - 4 cycles <p>For example if this value is chosen to 2'b01, it means that RTIM increments for every three 32Khz clock cycles.</p>

Bit	Attr	Reset Value	Description
1:0	RW	0x0	<p>PrbDschg Probe Discharge</p> <p>These bits set the times for TadpDschg. These bits are defined as follows:</p> <ul style="list-style-type: none"> 2'b00 4 msec (Scaledown 2 32Khz clock cycles) 2'b01 8 msec (Scaledown 4 32Khz clock cycles) 2'b10 16 msec (Scaledown 8 32Khz clock cycles) 2'b11 32 msec (Scaledown 16 32Khz clock cycles)

USBOTG_HPTXFSIZ

Address: Operational Base + offset (0x0100)

Host Periodic Transmit FIFO Size Register

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	<p>PTxFSize Host Periodic TxFIFO Depth</p> <p>This value is in terms of 32-bit words.</p> <p>Minimum value is 16</p> <p>Maximum value is 32,768</p> <p>The power-on reset value of this register is specified as the Largest Host Mode Periodic Tx Data FIFO Depth (parameter OTG_TX_HPERIO_DFIFO_DEPTH). If Enable Dynamic FIFO Sizing? Was deselected (parameter OTG_DFIFO_DYNAMIC = 0), these flops are optimized, and reads return the power-on value. If Enable Dynamic FIFO Sizing? was selected (parameter OTG_DFIFO_DYNAMIC = 1), you can write a new value in this field. Programmed values must not exceed the power-on value set .</p>

Bit	Attr	Reset Value	Description
15:0	RW	0x0000	<p>PTxFStAddr Host Periodic TxFIFO Start Address The power-on reset value of this register is the sum of the Largest Rx Data FIFO Depth and Largest Non-periodic Tx Data FIFO Depth specified.</p> <p>These parameters are: In shared FIFO operation: OTG_RX_DFIFO_DEPTH + OTG_TX_NPERIO_DFIFO_DEPTH. In dedicated FIFO mode: OTG_RX_DFIFO_DEPTH + OTG_TX_HNPERIO_DFIFO_DEPTH.</p> <p>If Enable Dynamic FIFO Sizing? was deselected (parameter OTG_DFIFO_DYNAMIC = 0), these flops are optimized, and reads return the power-on value. If Enable Dynamic FIFO Sizing? was selected (parameter OTG_DFIFO_DYNAMIC = 1), you can write a new value in this field. Programmed values must not exceed the power-on value.</p>

USBOTG_DIEPTXFn

Address: Operational Base + offset (0x0104+0x4*(n-1)), n = 1 - 15

Device Periodic Transmit FIFO-n Size Register

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	<p>INEP1TxFDep IN Endpoint TxFIFO Depth This value is in terms of 32-bit words. Minimum value is 16 Maximum value is 32,768</p> <p>The power-on reset value of this register is specified as the Largest IN Endpoint FIFO number Depth (parameter OTG_TX_DINEP_DFIFO_DEPTH_n)(0 < n <= 15). If Enable Dynamic FIFO Sizing? was deselected (parameter OTG_DFIFO_DYNAMIC = 0), these flops are optimized, and reads return the Power-on value. If Enable Dynamic FIFO Sizing? was selected (parameter OTG_DFIFO_DYNAMIC = 1), you can write a new value in this field. Programmed values must not exceed the Power-on value .</p>

Bit	Attr	Reset Value	Description
15:0	RW	0x0000	<p>INEP1TxFStAddr IN Endpoint FIFO1 Transmit RAM Start Address This field contains the memory start address for IN endpoint Transmit FIFO (0 < n <= 15). The power-on reset value of this register is specified as the Largest Rx Data FIFO Depth (parameter OTG_RX_DFIFO_DEPTH). OTG_RX_DFIFO_DEPTH + SUM 0 to n-1 (OTG_DINEP_TXFIFO_DEPTH_n) For example start address of IN endpoint FIFO 1 is OTG_RX_DFIFO_DEPTH + OTG_DINEP_TXFIFO_DEPTH_0. The start address of IN endpoint FIFO 2 is OTG_RX_DFIFO_DEPTH + OTG_DINEP_TXFIFO_DEPTH_0 + OTG_DINEP_TXFIFO_DEPTH_1. If Enable Dynamic FIFO Sizing? was deselected (parameter OTG_DFIFO_DYNAMIC = 0), these flops are optimized, and reads return the power-on value. If Enable Dynamic FIFO Sizing? was selected (parameter OTG_DFIFO_DYNAMIC = 1), and you have programmed a new value for Rx FIFO depth, you can write that value in this field. Programmed values must not exceed the power-on value set .</p>

USBOTG_HCFG

Address: Operational Base + offset (0x0400)

Host Configuration Register

Bit	Attr	Reset Value	Description
31:27	RO	0x0	reserved
26	RW	0x0	<p>PerSchedEna Enable Periodic Scheduling Applicable in Scatter/Gather DMA mode only. Enables periodic scheduling within the core. Initially, the bit is reset. The core will not process any periodic channels. As soon as this bit is set, the core will get ready to start scheduling periodic channels and sets HCFG.PerSchedStat. The setting of HCFG.PerSchedStat indicates the core has enabled periodic scheduling. Once HCFG.PerSchedEna is set, the application is not supposed to again reset the bit unless HCFG.PerSchedStat is set. As soon as this bit is reset, the core will get ready to stop scheduling periodic channels and resets HCFG.PerSchedStat. In non-Scatter/Gather DMA mode, this bit is reserved.</p>

Bit	Attr	Reset Value	Description
25:24	RW	0x0	<p>FrListEn</p> <p>Frame List Entries</p> <p>The value in the register specifies the number of entries in the Frame list. This field is valid only in Scatter/Gather DMA mode.</p>
23	RW	0x0	<p>DescDMA</p> <p>Enable Scatter/gather DMA in Host mode</p> <p>When the Scatter/Gather DMA option selected during configuration of the RTL, the application can set this bit during initialization to enable the Scatter/Gather DMA operation. NOTE: This bit must be modified only once after a reset. The following combinations are available for programming:</p> <ul style="list-style-type: none"> GAHBCFG.DMAEn=0, HCFG.DescDMA=0 => Slave mode GAHBCFG.DMAEn=0, HCFG.DescDMA=1 => Invalid GAHBCFG.DMAEn=1, HCFG.DescDMA=0 => Buffered DMA mode GAHBCFG.DMAEn=1, HCFG.DescDMA=1 => Scatter/Gather DMA mode <p>In non-Scatter/Gather DMA mode, this bit is reserved.</p>
22:16	RO	0x0	reserved
15:8	RW	0x00	<p>ResValid</p> <p>Resume Validation Period</p> <p>This field is effective only when HCFG.Ena32KHzS is set. It controls the resume period when the core resumes from suspend. The core counts the ResValid number of clock cycles to detect a valid resume when this is set.</p>
7	RW	0x0	<p>Ena32KHzS</p> <p>Enable 32-KHz Suspend Mode</p> <p>This bit can only be set if the USB 1.1 Full-Speed Serial Transceiver Interface has been selected. If USB 1.1 Full-Speed Serial Transceiver Interface has not been selected, this bit must be zero. When the USB 1.1 Full-Speed Serial Transceiver Interface is chosen and this bit is set, the core expects the 48-MHz PHY clock to be switched to 32 KHz during a suspend.</p>
6:3	RO	0x0	reserved

Bit	Attr	Reset Value	Description
2	RW	0x0	<p>FSLSSupp FS- and LS-Only Support The application uses this bit to control the core enumeration speed. Using this bit, the application can make the core enumerate as a FS host, even if the connected device supports HS traffic. Do not make changes to this field after initial programming.</p> <p>1'b0: HS/FS/LS, based on the maximum speed supported by the connected device 1'b1: FS/LS-only, even if the connected device can support HS</p>
1:0	RW	0x0	<p>FSLSPclkSel FS/LS PHY Clock Select 2'b00: PHY clock is running at 30/60 MHz 2'b01: PHY clock is running at 48 MHz Others: Reserved</p>

USBOTG_HFIR

Address: Operational Base + offset (0x0404)

Host Frame Interval Register

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:0	RW	0x0000	<p>FrInt Frame Interval The value that the application programs to this field specifies the interval between two consecutive SOFs (FS) or micro-SOFs (HS) or Keep-Alive tokens (HS). This field contains the number of PHY clocks that constitute the required frame interval. The default value set in this field for a FS operation when the PHY clock frequency is 60 MHz. The application can write a value to this register only after the Port Enable bit of the Host Port Control and Status register (HPRT.PrtEnaPort) has been set. If no value is programmed, the core calculates the value based on the PHY clock specified in the FS/LS PHY Clock Select field of the Host Configuration register (HCFG.FSLSPclkSel). Do not change the value of this field after the initial configuration.</p> <p>125 us * (PHY clock frequency for HS) 1 ms * (PHY clock frequency for FS/LS)</p>

USBOTG_HFNUM

Address: Operational Base + offset (0x0408)

Host Frame Number/Frame Time Remaining Register

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	FrRem Frame Time Remaining Indicates the amount of time remaining in the current micro-frame (HS) or frame (FS/LS), in terms of PHY clocks. This field decrements on each PHY clock. When it reaches zero, this field is reloaded with the value in the Frame Interval register and a new SOF is transmitted on the USB.
15:0	RO	0xffff	FrNum Frame Number This field increments when a new SOF is transmitted on the USB, and is reset to 0 when it reaches 16'h3FFF. This field is writable only if Remove Optional Features? was not selected (OTG_RM_OTG_FEATURES = 0). Otherwise, reads return the frame number value.

USBOTG_HPTXSTS

Address: Operational Base + offset (0x0410)

Host Periodic Transmit FIFO/Queue Status Register

Bit	Attr	Reset Value	Description
31:24	RO	0x00	PTxQTop Top of the Periodic Transmit Request Queue This indicates the entry in the Periodic Tx Request Queue that is currently being processed by the MAC. This register is used for debugging. Bit [31]: Odd/Even (micro)frame 1'b0: send in even (micro)frame 1'b1: send in odd (micro)frame Bits [30:27]: Channel/endpoint number Bits [26:25]: Type 2'b00: IN/OUT 2'b01: Zero-length packet 2'b10: CSPLIT 2'b11: Disable channel command Bit [24]: Terminate (last entry for the selected channel/endpoint)

Bit	Attr	Reset Value	Description
23:16	RO	0x00	<p>PTxQSpAvail Periodic Transmit Request Queue Space Available Indicates the number of free locations available to be written in the Periodic Transmit Request Queue. This queue holds both IN and OUT requests.</p> <ul style="list-style-type: none"> 8'h0: Periodic Transmit Request Queue is full 8'h1: 1 location available 8'h2: 2 locations available n: n locations available (0 <=n <= 16) Others: Reserved
15:0	RW	0x0000	<p>PTxFSpAvail Periodic Transmit Data FIFO Space Available Indicates the number of free locations available to be written to in the Periodic TxFIFO. Values are in terms of 32-bit words</p> <ul style="list-style-type: none"> . 16'h0: Periodic TxFIFO is full . 16'h1: 1 word available . 16'h2: 2 words available . 16'hn: n words available (where 0 . n . 32,768) . 16'h8000: 32,768 words available . Others: Reserved

USBOTG_HAIN

Address: Operational Base + offset (0x0414)

Host All Channels Interrupt Register

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:0	RO	0x0000	<p>HAIN Channel Interrupts One bit per channel: Bit 0 for Channel 0 Bit 1 for Channel 1 Bit 15 for Channel 15</p>

USBOTG_HAINMSK

Address: Operational Base + offset (0x0418)

Host All Channels Interrupt Mask Register

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved

Bit	Attr	Reset Value	Description
15:0	RW	0x0000	HAINTMsk Channel Interrupt Mask One bit per channel: Bit 0 for channel 0, bit 15 for channel 15

USBOTG_HPRT

Address: Operational Base + offset (0x0440)

Host Port Control and Status Register

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:17	RO	0x0	PrtSpd Port Speed Indicates the speed of the device attached to this port. 2'b00: High speed 2'b01: Full speed 2'b10: Low speed 2'b11: Reserved
16:13	RW	0x0	PrtTstCtl Port Test Control The application writes a nonzero value to this field to put the port into a Test mode, and the corresponding pattern is signaled on the port. 4'b0000: Test mode disabled 4'b0001: Test_J mode 4'b0010: Test_K mode 4'b0011: Test_SE0_NAK mode 4'b0100: Test_Packet mode 4'b0101: Test_Force_Enable Others: Reserved
12	RWSC	0x0	PrtPwr Port Power The application uses this field to control power to this port (write 1'b1 to set to 1'b1 and write 1'b0 to set to 1'b0), and the core can clear this bit on an over current condition. 1'b0: Power off 1'b1: Power on
11:10	RO	0x0	PrtLnsts Port Line Status Indicates the current logic level USB data lines Bit [10]: Logic level of D+ Bit [11]: Logic level of D
9	RO	0x0	reserved

Bit	Attr	Reset Value	Description
8	RW	0x0	<p>PrtRst Port Reset</p> <p>When the application sets this bit, a reset sequence is started on this port. The application must time the reset period and clear this bit after the reset sequence is complete.</p> <p>1'b0: Port not in reset 1'b1: Port in reset</p> <p>To start a reset on the port, the application must leave this bit set for at least the minimum duration mentioned below, as specified in the USB 2.0 specification, Section 7.1.7.5. The application can leave it set for another 10 ms in addition to the required minimum duration, before clearing the bit, even though there is no maximum limit set by the USB standard.</p> <p>High speed: 50 ms Full speed/Low speed: 10 ms</p>
7	RWSC	0x0	<p>PrtSusp Port Suspend</p> <p>The application sets this bit to put this port in Suspend mode. The core only stops sending SOFs when this is set. To stop the PHY clock, the application must set the Port Clock Stop bit, which asserts the suspended input pin of the PHY.</p> <p>The read value of this bit reflects the current suspend status of the port. This bit is cleared by the core after a remote wakeup signal is detected or the application sets the Port Reset bit or Port Resume bit in this register or the Resume/Remote Wakeup Detected Interrupt bit or Disconnect Detected Interrupt bit in the Core Interrupt register (GINTSTS.WkUpInt or GINTSTS.DisconnInt, respectively).</p> <p>1'b0: Port not in Suspend mode 1'b1: Port in Suspend mode</p>

Bit	Attr	Reset Value	Description
6	RWSC	0x0	<p>PrtRes Port Resume The application sets this bit to drive resume signaling on the port. The core continues to drive the resume signal until the application clears this bit.</p> <p>If the core detects a USB remote wakeup sequence, as indicated by the Port Resume/Remote Wakeup Detected Interrupt bit of the Core Interrupt register (GINTSTS.WkUpInt), the core starts driving resume signaling without application intervention and clears this bit when it detects a disconnect condition. The read value of this bit indicates whether the core is currently driving resume signaling.</p> <p>1'b0: No resume driven 1'b1: Resume driven</p> <p>When LPM is enabled and the core is in the L1 (Sleep) state, setting this bit results in the following behavior:</p> <p>The core continues to drive the resume signal until a pre-determined time specified in the GLPMCFG.HIRD_Thres[3:0] field.</p> <p>If the core detects a USB remote wakeup sequence, as indicated by the Port L1 Resume/Remote L1 Wakeup Detected Interrupt bit of the Core Interrupt register (GINTSTS.L1WkUpInt), the core starts driving resume signaling without application intervention and clears this bit at the end of the resume. The read value of this bit indicates whether the core is currently driving resume signaling.</p> <p>1'b0: No resume driven 1'b1: Resume driven</p>
5	W1C	0x0	<p>PrtOvrCurrChng Port Overcurrent Change The core sets this bit when the status of the Port Overcurrent Active bit (bit 4) in this register changes.</p>

Bit	Attr	Reset Value	Description
4	RO	0x0	PrtOvrCurrAct Port Overcurrent Active Indicates the overcurrent condition of the port. 1'b0: No overcurrent condition 1'b1: Overcurrent condition
3	W1C	0x0	PrtEnChng Port Enable/Disable Change The core sets this bit when the status of the Port Enable bit [2] of this register changes.
2	W1C	0x0	PrtEna Port Enable A port is enabled only by the core after a reset sequence, and is disabled by an overcurrent condition, a disconnect condition, or by the application clearing this bit. The application cannot set this bit by a register write. It can only clear it to disable the port. This bit does not trigger any interrupt to the application. 1'b0: Port disabled 1'b1: Port enabled
1	W1C	0x0	PrtConnDet Port Connect Detected The core sets this bit when a device connection is detected to trigger an interrupt to the application using the Host Port Interrupt bit of the Core Interrupt register (GINTSTS.PrtInt). The application must write a 1 to this bit to clear the interrupt.
0	RO	0x0	PrtConnSts Port Connect Status 1'b0: No device is attached to the port. 1'b1: A device is attached to the port.

USBOTG_HCCHARn

Address: Operational Base + offset (0x0500)

Host Channel-n Characteristics Register

Bit	Attr	Reset Value	Description
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Bit	Attr	Reset Value	Description
31	RWSC	0x0	<p>ChEna Channel Enable When Scatter/Gather mode is enabled 1'b0: Indicates that the descriptor structure is not yet ready. 1'b1: Indicates that the descriptor structure and data buffer with data is setup and this channel can access the descriptor.</p> <p>When Scatter/Gather mode is disabled, This field is set by the application and cleared by the OTG host.</p> <p>1'b0: Channel disabled 1'b1: Channel enabled</p>
30	RWSC	0x0	<p>ChDis Channel Disable The application sets this bit to stop transmitting/receiving data on a channel, even before the transfer for that channel is complete. The application must wait for the Channel Disabled interrupt before treating the channel as disabled.</p>
29	RW	0x0	<p>OddFrm Odd Frame This field is set (reset) by the application to indicate that the OTG host must perform a transfer in an odd (micro) frame. This field is applicable for only periodic (isochronous and interrupt) transactions.</p> <p>1'b0: Even (micro)frame 1'b1: Odd (micro)frame</p> <p>This field is not applicable for Scatter/Gather DMA mode and need not be programmed by the application and is ignored by the core.</p>
28:22	RW	0x00	<p>DevAddr Device Address This field selects the specific device serving as the data source or sink.</p>

Bit	Attr	Reset Value	Description
21:20	RW	0x0	<p>MC_EC Multi Count (MC) / Error Count (EC) When the Split Enable bit of the Host Channel-n Split Control register (HCSPLTn.SpltEna) is reset (1'b0), this field indicates to the host the number of transactions that must be executed per micro-frame for this periodic endpoint. For non periodic transfers, this field is used only in DMA mode, and specifies the number packets to be fetched for this channel before the internal DMA engine changes arbitration.</p> <p>2'b00: Reserved This field yields undefined results. 2'b01: 1 transaction 2'b10: 2 transactions to be issued for this endpoint per micro-frame 2'b11: 3 transactions to be issued for this endpoint per micro-frame</p> <p>When HCSPLTn.SpltEna is set (1'b1), this field indicates the number of immediate retries to be performed for a periodic split transactions on transaction errors. This field must be set to at least 2'b01.</p>
19:18	RW	0x0	<p>EPType Endpoint Type Indicates the transfer type selected.</p> <p>2'b00: Control 2'b01: Isochronous 2'b10: Bulk 2'b11: Interrupt</p>
17	RW	0x0	<p>LSpdDev Low-Speed Device This field is set by the application to indicate that this channel is communicating to a low-speed device.</p>
16	RO	0x0	reserved
15	RW	0x0	<p>EPDir Endpoint Direction Indicates whether the transaction is IN or OUT.</p> <p>1'b0: OUT 1'b1: IN</p>

Bit	Attr	Reset Value	Description
14:11	RW	0x0	EPNum Endpoint Number Indicates the endpoint number on the device serving as the data source or sink.
10:0	RW	0x000	MPS Maximum Packet Size Indicates the maximum packet size of the associated endpoint.

USBOTG_HCSPLTn

Address: Operational Base + offset (0x0504)

Host Channel-n Split Control Register

Bit	Attr	Reset Value	Description
31	RW	0x0	SplEna Split Enable The application sets this field to indicate that this channel is enabled to perform split transactions.
30:17	RO	0x0	reserved
16	RW	0x0	CompSplt Do Complete Split The application sets this field to request the OTG host to perform a complete split transaction.
15:14	RW	0x0	XactPos Transaction Position This field is used to determine whether to send all, first, middle, or last payloads with each OUT transaction. 2'b11: All. This is the entire data payload is of this transaction (which is less than or equal to 188 bytes). 2'b10: Begin. This is the first data payload of this transaction (which is larger than 188 bytes). 2'b00: Mid. This is the middle payload of this transaction (which is larger than 188bytes). 2'b01: End. This is the last payload of this transaction (which is larger than 188 bytes).
13:7	RW	0x00	HubAddr Hub Address This field holds the device address of the transaction translator's hub.
6:1	RO	0x0	reserved

Bit	Attr	Reset Value	Description
0	RW	0x0	PrtAddr Port Address This field is the port number of the recipient transaction translator.

USBOTG_HCINTn

Address: Operational Base + offset (0x0508)

Host Channel-n Interrupt Register

Bit	Attr	Reset Value	Description
31:14	RO	0x0	reserved
13	W1C	0x0	DESC_LST_ROLLIntr Descriptor rollover interrupt This bit is valid only when Scatter/Gather DMA mode is enabled. The core sets this bit when the corresponding channel's descriptor list rolls over. For non-Scatter/Gather DMA mode, this bit is reserved.
12	W1C	0x0	XCS_XACT_ERR Excessive Transaction Error This bit is valid only when Scatter/Gather DMA mode is enabled. The core sets this bit when 3 consecutive transaction errors occurred on the USB bus. XCS_XACT_ERR will not be generated for Isochronous channels. For non-Scatter/Gather DMA mode, this bit is reserved.
11	W1C	0x0	BNAIntr BNA (Buffer Not Available) Interrupt This bit is valid only when Scatter/Gather DMA mode is enabled. The core generates this interrupt when the descriptor accessed is not ready for the Core to process. BNA will not be generated for Isochronous channels. For non-Scatter/Gather DMA mode, this bit is reserved.
10	W1C	0x0	DataTglErr Data Toggle Error In Scatter/Gather DMA mode, the interrupt due to this bit is masked in the core.
9	W1C	0x0	FrmOvrun Frame Overrun In Scatter/Gather DMA mode, the interrupt due to this bit is masked in the core

Bit	Attr	Reset Value	Description
8	W1C	0x0	BblErr Babble Error In Scatter/Gather DMA mode, the interrupt due to this bit is masked in the core.
7	W1C	0x0	XactErr Transaction Error Indicates one of the following errors occurred on the USB: CRC check failure, Timeout, Bit stuff error, False EOP. In Scatter/Gather DMA mode, the interrupt due to this bit is masked in the core.
6	WO	0x0	NYET NYET Response Received Interrupt In Scatter/Gather DMA mode, the interrupt due to this bit is masked in the core.
5	W1C	0x0	ACK ACK Response Received/Transmitted Interrupt In Scatter/Gather DMA mode, the interrupt due to this bit is masked in the core.
4	W1C	0x0	NAK NAK Response Received Interrupt In Scatter/Gather DMA mode, the interrupt due to this bit is masked in the core.
3	W1C	0x0	STALL STALL Response Received Interrupt In Scatter/Gather DMA mode, the interrupt due to this bit is masked in the core.
2	W1C	0x0	AHBErr AHB Error This is generated only in DMA mode when there is an AHB error during AHB read/write. The application can read the corresponding channel's DMA address register to get the error address.

Bit	Attr	Reset Value	Description
1	W1C	0x0	ChHltd Channel Halted In non-Scatter/Gather DMA mode, it indicates the transfer completed abnormally either because of any USB transaction error or in response to disable request by the application or because of a completed transfer. In Scatter/Gather DMA mode, this indicates that transfer completed due to any of the following: EOL being set in descriptor, AHB error, Excessive transaction errors, In response to disable request by the application, Babble, Stall, Buffer Not Available (BNA)
0	W1C	0x0	XferCompl Transfer Completed For Scatter/Gather DMA mode, it indicates that current descriptor processing got completed with IOC bit set in its descriptor. In non-Scatter/Gather DMA mode, it indicates that Transfer completed normally without any errors.

USBOTG_HCINTMSKn

Address: Operational Base + offset (0x050c)

Host Channel-n Interrupt Mask Register

Bit	Attr	Reset Value	Description
31:14	RO	0x0	reserved
13	RW	0x0	DESC_LST_ROLLIntrMsk Descriptor rollover interrupt Mask register This bit is valid only when Scatter/Gather DMA mode is enabled. In non-Scatter/Gather DMA mode, this bit is reserved.
12	RO	0x0	reserved
11	RW	0x0	BNAIntrMsk BNA (Buffer Not Available) Interrupt mask register This bit is valid only when Scatter/Gather DMA mode is enabled. In non-Scatter/Gather DMA mode, this bit is reserved.
10	RW	0x0	DataTglErrMsk Data Toggle Error Mask This bit is not applicable in Scatter/Gather DMA mode.

Bit	Attr	Reset Value	Description
9	RW	0x0	FrmOvrnMsk Frame Overrun Mask This bit is not applicable in Scatter/Gather DMA mode.
8	RW	0x0	BblErrMsk Babble Error Mask This bit is not applicable in Scatter/Gather DMA mode.
7	RW	0x0	XactErrMsk Transaction Error Mask This bit is not applicable in Scatter/Gather DMA mode
6	RW	0x0	NyetMsk NYET Response Received Interrupt Mask This bit is not applicable in Scatter/Gather DMA mode.
5	RW	0x0	AckMsk ACK Response Received/Transmitted Interrupt Mask This bit is not applicable in Scatter/Gather DMA mode.
4	RW	0x0	NakMsk NAK Response Received Interrupt Mask This bit is not applicable in Scatter/Gather DMA mode.
3	RW	0x0	StallMsk STALL Response Received Interrupt Mask This bit is not applicable in Scatter/Gather DMA mode.
2	RW	0x0	AHBErrMsk AHB Error Mask Note: This bit is only accessible when OTG_ARCHITECTURE = 2
1	RW	0x0	ChHltedMsk Channel Halted Mask
0	RW	0x0	XferComplMsk Transfer Completed Mask This bit is valid only when Scatter/Gather DMA mode is enabled. In non-Scatter/Gather DMA mode, this bit is reserved.

USBOTG_HCTSIZn

Address: Operational Base + offset (0x0510)

Host Channel-n Transfer Size Register

Bit	Attr	Reset Value	Description
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Bit	Attr	Reset Value	Description
31	RW	0x0	<p>DoPng Do Ping</p> <p>This bit is used only for OUT transfers. Setting this field to 1 directs the host to do PING protocol. Note: Do not set this bit for IN transfers. If this bit is set for IN transfers it disables the channel.</p>
30:29	RW	0x0	<p>Pid PID</p> <p>The application programs this field with the type of PID to use for the initial transaction. The host maintains this field for the rest of the transfer.</p> <p>2'b00: DATA0 2'b01: DATA2 2'b10: DATA1 2'b11: MDATA (non-control)/SETUP (control)</p>
28:19	RW	0x000	<p>PktCnt Packet Count</p> <p>This field is programmed by the application with the expected number of packets to be transmitted (OUT) or received (IN). The host decrements this count on every successful transmission or reception of an OUT/IN packet. Once this count reaches zero, the application is interrupted to indicate normal completion. The width of this counter is specified as Width of Packet Counters (parameter OTG_PACKET_COUNT_WIDTH).</p>
18:0	RW	0x00000	<p>XferSize Transfer Size</p> <p>For an OUT, this field is the number of data bytes the host sends during the transfer. For an IN, this field is the buffer size that the application has Reserved for the transfer. The application is expected to program this field as an integer multiple of the maximum packet size for IN transactions (periodic and non-periodic). The width of this counter is specified as Width of Transfer Size Counters (parameter OTG_TRANS_COUNT_WIDTH).</p>

USBOTG_HCDMAN

Address: Operational Base + offset (0x0514)
Host Channel-n DMA Address Register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	DMAAddr DMA Address This field holds the start address in the external memory from which the data for the endpoint must be fetched or to which it must be stored. This register is incremented on every AHB transaction.

USBOTG_HCDMABn

Address: Operational Base + offset (0x051c)

Host Channel-n DMA Buffer Address Register

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	HCDMABn Holds the current buffer address This register is updated as and when the data transfer for the corresponding end point is in progress. This register is present only in Scatter/Gather DMA mode. Otherwise this field is reserved.

USBOTG_DCFG

Address: Operational Base + offset (0x0800)

Device Configuration Register

Bit	Attr	Reset Value	Description
31:26	RW	0x02	ResValid Resume Validation Period This field controls the period when the core resumes from a suspend. When this bit is set, the core counts for the ResValid number of clock cycles to detect a valid resume. This field is effective only when DCFG.Ena32KHzSusp is set.

Bit	Attr	Reset Value	Description
25:24	RW	0x0	<p>PerSchIntvl Periodic Scheduling Interval PerSchIntvl must be programmed only for Scatter/Gather DMA mode. Description: This field specifies the amount of time the Internal DMA engine must allocate for fetching periodic IN endpoint data. Based on the number of periodic endpoints, this value must be specified as 25,50 or 75% of (micro)frame. When any periodic endpoints are active, the internal DMA engine allocates the specified amount of time in fetching periodic IN endpoint data. When no periodic endpoints are active, then the internal DMA engine services nonperiodic endpoints, ignoring this field. After the specified time within a (micro) frame, the DMA switches to fetching for nonperiodic endpoints.</p> <ul style="list-style-type: none"> 2'b00: 25% of (micro) frame. 2'b01: 50% of (micro) frame. 2'b10: 75% of (micro) frame. 2'b11: Reserved.
23	RW	0x0	<p>DescDMA Enable Scatter/Gather DMA in Device mode When the Scatter/Gather DMA option selected during configuration of the RTL, the application can set this bit during initialization to enable the Scatter/Gather DMA operation. NOTE: This bit must be modified only once after a reset. The following combinations are available for programming:</p> <ul style="list-style-type: none"> GAHBCFG.DMAEn=0,DCFG.DescDMA=0 => Slave mode GAHBCFG.DMAEn=0,DCFG.DescDMA=1 => Invalid GAHBCFG.DMAEn=1,DCFG.DescDMA=0 => Buffered DMA mode GAHBCFG.DMAEn=1,DCFG.DescDMA=1 => Scatter/Gather DMA mode

Bit	Attr	Reset Value	Description
22:18	RW	0x08	EPMisCnt IN Endpoint Mismatch Count This field is valid only in shared FIFO operation. The application programs this field with a count that determines when the core generates an Endpoint Mismatch interrupt (GINTSTS.EPMis). The core loads this value into an internal counter and decrements it. The counter is reloaded whenever there is a match or when the counter expires. The width of this counter depends on the depth of the Token Queue.
17:13	RO	0x0	reserved
12:11	RW	0x0	PerFrInt Periodic Frame Interval Indicates the time within a (micro) frame at which the application must be notified using the End Of Periodic Frame Interrupt. This can be used to determine if all the isochronous traffic for that (micro) frame is complete. 2'b00: 80% of the (micro)frame interval 2'b01: 85% 2'b10: 90% 2'b11: 95%
10:4	RW	0x00	DevAddr Device Address The application must program this field after every SetAddress control command.
3	RW	0x0	Ena32KHzS Enable 32-KHz Suspend Mode When the USB 1.1 Full-Speed Serial Transceiver Interface is chosen and this bit is set, the core expects the 48-MHz PHY clock to be switched to 32 KHz during a suspend. This bit can only be set if USB 1.1 Full-Speed Serial Transceiver Interface has been selected. If USB 1.1 Full-Speed Serial Transceiver Interface has not been selected, this bit must be zero.

Bit	Attr	Reset Value	Description
2	RW	0x0	<p>NZStsOUTHSbk Non-Zero-Length Status OUT Handshake The application can use this field to select the handshake the core sends on receiving a nonzero-length data packet during the OUT transaction of a control transfer's Status stage.</p> <p>1'b1: Send a STALL handshake on a nonzero-length status OUT transaction and do not send the received OUT packet to the application.</p> <p>1'b0: Send the received OUT packet to the application (zero-length or nonzerolength) and send a handshake based on the NAK and STALL bits for the endpoint in the Device Endpoint Control register.</p>
1:0	RW	0x0	<p>DevSpd Device Speed Indicates the speed at which the application requires the core to enumerate, or the maximum speed the application can support. However, the actual bus speed is determined only after the chirp sequence is completed, and is based on the speed of the USB host to which the core is connected.</p> <p>2'b00: High speed (USB 2.0 PHY clock is 30 MHz or 60 MHz)</p> <p>2'b01: Full speed (USB 2.0 PHY clock is 30 MHz or 60 MHz)</p> <p>2'b10: Reserved</p> <p>2'b11: Full speed (USB 1.1 transceiver clock is 48 MHz)</p>

USBOTG_DCTL

Address: Operational Base + offset (0x0804)

Device Control Register

Bit	Attr	Reset Value	Description
31:17	RO	0x0	reserved
16	RW	0x0	<p>NakOnBble Set NAK automatically on babble The core sets NAK automatically for the endpoint on which babble is received.</p>

Bit	Attr	Reset Value	Description
15	RW	0x0	<p>IgnrFrmNum Ignore frame number for isochronous endpoints in case of Scatter/Gather DMA mode.</p> <p>Do NOT program IgnrFrmNum bit to 1'b1 when the core is operating in Threshold mode.</p> <p>Note: When Scatter/Gather DMA mode is enabled this feature is not applicable to highspeed, high-bandwidth transfers. When this bit is enabled, there must be only one packet per descriptor.</p> <p>1'b0: The core transmits the packets only in the frame number in which they are intended to be transmitted.</p> <p>1'b1: The core ignores the frame number, sending packets immediately as the packets are ready.</p> <p>Scatter/Gather:</p> <p>In Scatter/Gather DMA mode, when this bit is enabled, the packets are not flushed when an ISOC IN token is received for an elapsed frame.</p> <p>When Scatter/Gather DMA mode is disabled, this field is used by the application to enable periodic transfer interrupt. The application can program periodic endpoint transfers for multiple (micro) frames.</p> <p>1'b0: Periodic transfer interrupt feature is disabled; the application must program transfers for periodic endpoints every (micro)frame</p> <p>1'b1: Periodic transfer interrupt feature is enabled; the application can program transfers for multiple (micro)frames for periodic endpoints.</p> <p>In non-Scatter/Gather DMA mode, the application receives transfer complete interrupt after transfers for multiple (micro) frames are completed.</p>

Bit	Attr	Reset Value	Description
14:13	RW	0x1	<p>GMC Global Multi Count GMC must be programmed only once after initialization. Applicable only for Scatter/Gather DMA mode. This indicates the number of packets to be serviced for that end point before moving to the next end point. It is only for nonperiodic end points.</p> <p>2'b00: Invalid. 2'b01: 1 packet. 2'b10: 2 packets. 2'b11: 3 packets.</p> <p>When Scatter/Gather DMA mode is disabled, this field is reserved. and reads 2'b00.</p>
12	RO	0x0	reserved
11	RW	0x0	<p>PWROnPrgDone Power-On Programming Done The application uses this bit to indicate that register programming is completed after a wake-up from Power Down mode.</p>
10	WO	0x0	<p>CGOUTNak Clear Global OUT NAK A write to this field clears the Global OUT NAK.</p>
9	WO	0x0	<p>SGOUTNak Set Global OUT NAK A write to this field sets the Global OUT NAK. The application uses this bit to send a NAK handshake on all OUT endpoints. The application must set this bit only after making sure that the Global OUT NAK Effective bit in the Core Interrupt Register (GINTSTS.GOUTNakEff) is cleared.</p>
8	WO	0x0	<p>CGNPInNak Clear Global Non-periodic IN NAK A write to this field clears the Global Non-periodic IN NAK.</p>

Bit	Attr	Reset Value	Description
7	WO	0x0	SGNPIInNak Set Global Non-periodic IN NAK A write to this field sets the Global Non-periodic IN NAK. The application uses this bit to send a NAK handshake on all non-periodic IN endpoints. The core can also set this bit when a timeout condition is detected on a non-periodic endpoint in shared FIFO operation. The application must set this bit only after making sure that the Global IN NAK Effective bit in the Core Interrupt Register (GINTSTS.GINNakEff) is cleared.
6:4	RW	0x0	TstCtl Test Control 3'b000: Test mode disabled 3'b001: Test_J mode 3'b010: Test_K mode 3'b011: Test_SE0_NAK mode 3'b100: Test_Packet mode 3'b101: Test_Force_Enable Others: Reserved
3	RO	0x0	GOUTNakSts Global OUT NAK Status 1'b0: A handshake is sent based on the FIFO Status and the NAK and STALL bit settings. 1'b1: No data is written to the RxFIFO, irrespective of space availability. Sends a NAK handshake on all packets, except on SETUP transactions. All isochronous OUT packets are dropped
2	RO	0x0	GNPINNakSts Global Non-periodic IN NAK Status 1'b0: A handshake is sent out based on the data availability in the transmit FIFO. 1'b1: A NAK handshake is sent out on all non-periodic IN endpoints, irrespective of the data availability in the transmit FIFO.

Bit	Attr	Reset Value	Description
1	RW	0x0	<p>SftDiscon Soft Disconnect</p> <p>The application uses this bit to signal the Otg core to do a soft disconnect. As long as this bit is set, the host does not see that the device is connected, and the device does not receive signals on the USB. The core stays in the disconnected state until the application clears this bit.</p> <p>1'b0: Normal operation. When this bit is cleared after a soft disconnect, the core drives the phy_opmode_o signal on the UTMI+ to 2'b00, which generates a device connect event to the USB host. When the device is reconnected, the USB host restarts device enumeration.</p> <p>1'b1: The core drives the phy_opmode_o signal on the UTMI+ to 2'b01, which generates a device disconnect event to the USB host.</p>
0	RW	0x0	<p>RmtWkUpSig Remote Wakeup Signaling</p> <p>When the application sets this bit, the core initiates remote signaling to wake the USB host. The application must set this bit to instruct the core to exit the Suspend state. As specified in the USB 2.0 specification, the application must clear this bit 1-15 ms after setting it. If LPM is enabled and the core is in the L1 (Sleep) state, when the application sets this bit, the core initiates L1 remote signaling to wake up the USB host. The application must set this bit to instruct the core to exit the Sleep state. As specified in the LPM specification, the hardware automatically clears this bit 50 us (TL1DevDrvResume) after being set by the application. The application must not set this bit when GLPMCFG.bRemoteWake from the previous LPM transaction is zero.</p>

USBOTG_DSTS

Address: Operational Base + offset (0x0808)

Device Status Register

Bit	Attr	Reset Value	Description
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Bit	Attr	Reset Value	Description
31:22	RO	0x0	reserved
21:8	RW	0x0000	SOFFN Frame or Micro-frame Number of the Received SOF When the core is operating at high speed, this field contains a micro-frame number. When the core is operating at full or low speed, this field contains a frame number.
7:4	RO	0x0	reserved
3	RW	0x0	ErrticErr Erratic Error The core sets this bit to report any erratic errors (phy_rxvalid_i/phy_rxvldh_i or phy_rxactive_i is asserted for at least 2 ms, due to PHY error) seen on the UTMI+. Due to erratic errors, the Otg core goes into Suspended state and an interrupt is generated to the application with Early Suspend bit of the Core Interrupt register (GINTSTS.ErlySusp). If the early suspend is asserted due to an erratic error, the application can only perform a soft disconnect recover.
2:1	RW	0x0	EnumSpd Enumerated Speed Indicates the speed at which the OTG core has come up after speed detection through a chirp sequence. 2'b00: High speed (PHY clock is running at 30 or 60 MHz) 2'b01: Full speed (PHY clock is running at 30 or 60 MHz) 2'b10: Low speed (PHY clock is running at 48 MHz, internal phy_clk at 6 MHz) 2'b11: Full speed (PHY clock is running at 48 MHz) Low speed is not supported for devices using a UTMI+ PHY.

Bit	Attr	Reset Value	Description
0	RW	0x0	SuspSts Suspend Status In Device mode, this bit is set as long as a Suspend condition is detected on the USB. The core enters the Suspended state when there is no activity on the utmi_linestate signal for an extended period of time. The core comes out of the suspend: When there is any activity on the utmi_linestate signal, When the application writes to the Remote Wakeup Signaling bit in the Device Control register (DCTL.RmtWkUpSig).

USBOTG_DIEPMSK

Address: Operational Base + offset (0x0810)

Device IN Endpoint common interrupt mask register

Bit	Attr	Reset Value	Description
31:14	RO	0x0	reserved
13	RW	0x0	NAKMsk NAK interrupt Mask
12:10	RO	0x0	reserved
9	RW	0x0	BNAInIntrMsk BNA Interrupt Mask
8	RW	0x0	TxfifoUndrnMsk Fifo Underrun Mask
7	RO	0x0	reserved
6	RW	0x0	INEPNakEffMsk IN Endpoint NAK Effective Mask
5	RW	0x0	INTknEPMisMsk IN Token received with EP Mismatch Mask
4	RW	0x0	INTknTXFEmpMsk IN Token Received When TxFIFO Empty Mask
3	RW	0x0	TimeOUTMsk Timeout Condition Mask
2	RW	0x0	AHBErrMsk AHB Error Mask
1	RW	0x0	EPDisbldMsk Endpoint Disabled Interrupt Mask
0	RW	0x0	XferComplMsk Transfer Completed Interrupt Mask

USBOTG_DOEPMSK

Address: Operational Base + offset (0x0814)

Device OUT Endpoint common interrupt mask register

Bit	Attr	Reset Value	Description
31:15	RO	0x0	reserved
14	RW	0x0	NYETMsk NYET Interrupt Mask
13	RW	0x0	NAKMsk NAK Interrupt Mask
12	RW	0x0	BbleErrMsk Babble Interrupt Mask
11:10	RO	0x0	reserved
9	RW	0x0	BnaOutIntrMsk BNA interrupt Mask
8	RW	0x0	OutPktErrMsk OUT Packet Error Mask
7	RO	0x0	reserved
6	RW	0x0	Back2BackSETup Back-to-Back SETUP Packets Received Mask Applies to control OUT endpoints only.
5	RO	0x0	reserved
4	RW	0x0	OUTTknEPdisMsk OUT Token Received when Endpoint Disabled Mask Applies to control OUT endpoints only.
3	RW	0x0	SetUPMsk SETUP Phase Done Mask Applies to control endpoints only.
2	RW	0x0	AHBErrMsk AHB Error
1	RW	0x0	EPDisblIdMsk Endpoint Disabled Interrupt Mask
0	RW	0x0	XferComplMsk Transfer Completed Interrupt Mask

USBOTG_DAIN

Address: Operational Base + offset (0x0818)

Device All Endpoints interrupt register

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	OutEPInt OUT Endpoint Interrupt Bits One bit per OUT endpoint: Bit 16 for OUT endpoint 0, bit 31 for OUT endpoint 15
15:0	RO	0x0000	InEpInt IN Endpoint Interrupt Bits One bit per IN Endpoint: Bit 0 for IN endpoint 0, bit 15 for endpoint 15

USBOTG_DAINTMSK

Address: Operational Base + offset (0x081c)

Device All Endpoint interrupt mask register

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	OutEpMsk OUT EP Interrupt Mask Bits One per OUT Endpoint: Bit 16 for OUT EP 0, bit 31 for OUT EP 15
15:0	RW	0x0000	InEpMsk IN EP Interrupt Mask Bits One bit per IN Endpoint: Bit 0 for IN EP 0, bit 15 for IN EP 15

USBOTG_DTKNQR1

Address: Operational Base + offset (0x0820)

Device IN token sequence learning queue read register1

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	EPTkn Endpoint Token Four bits per token represent the endpoint number of the token: Bits [31:28]: Endpoint number of Token 5 Bits [27:24]: Endpoint number of Token 4 Bits [15:12]: Endpoint number of Token 1 Bits [11:8]: Endpoint number of Token 0
7	RO	0x0	WrapBit Wrap Bit This bit is set when the write pointer wraps. It is cleared when the learning queue is cleared.
6:5	RO	0x0	reserved
4:0	RO	0x00	INTknWPtr IN Token Queue Write Pointer

USBOTG_DTKNQR2

Address: Operational Base + offset (0x0824)

Device IN token sequence learning queue read register2

Bit	Attr	Reset Value	Description
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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	EPTkn Endpoint Token Four bits per token represent the endpoint number of the token: Bits [31:28]: Endpoint number of Token 13 Bits [27:24]: Endpoint number of Token 12 Bits [7:4]: Endpoint number of Token 7 Bits [3:0]: Endpoint number of Token 6

USBOTG_DVBUSDIS

Address: Operational Base + offset (0x0828)

Device VBUS discharge time register

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:0	RW	0x0b8f	DVBUSDis Device VBUS Discharge Time Specifies the VBUS discharge time after VBUS pulsing during SRP. This value equals: VBUS discharge time in PHY clocks / 1,024. The value you use depends whether the PHY is operating at 30 MHz (16-bit data width) or 60 MHz (8-bit data width). Depending on your VBUS load, this value can need adjustment.

USBOTG_DVBUSPULSE

Address: Operational Base + offset (0x082c)

Device VBUS Pulsing Timer Register

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:0	RW	0x000	DVBUSPulse Device VBUS Pulsing Time Specifies the VBUS pulsing time during SRP. This value equals: VBUS pulsing time in PHY clocks / 1,024. The value you use depends whether the PHY is operating at 30 MHz (16-bit data width) or 60 MHz (8-bit data width).

USBOTG_DTHRCTL

Address: Operational Base + offset (0x0830)

Device Threshold Control Register

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved

Bit	Attr	Reset Value	Description
27	RW	0x1	ArbPrkEn Arbiter Parking Enable This bit controls internal DMA arbiter parking for IN endpoints. When threshold is enabled and this bit is set to one, then the arbiter parks on the IN endpoint for which there is a token received on the USB. This is done to avoid getting into under-run conditions. By default the parking is enabled.
26	RO	0x0	reserved
25:17	RW	0x008	RxThrLen Receive Threshold Length This field specifies Receive threshold size in DWORDS. This field also specifies the amount of data received on the USB before the core can start transmitting on the AHB. The threshold length has to be at least eight DWORDS. The recommended value for ThrLen is to be the same as the programmed AHB Burst Length (GAHBCFG.HBstLen).
16	RW	0x0	RxThrEn Receive Threshold Enable When this bit is set, the core enables thresholding in the receive direction.
15:13	RO	0x0	reserved

Bit	Attr	Reset Value	Description
12:11	RW	0x0	<p>AHBThrRatio AHB Threshold Ratio These bits define the ratio between the AHB threshold and the MAC threshold for the transmit path only. The AHB threshold always remains less than or equal to the USB threshold, because this does not increase overhead. Both the AHB and the MAC threshold must be DWORD-aligned. The application needs to program TxThrLen and the AHBThrRatio to make the AHB Threshold value DWORD aligned. If the AHB threshold value is not DWORD aligned, the core might not behave correctly. When programming the TxThrLen and AHBThrRatio, the application must ensure that the minimum AHB threshold value does not go below 8 DWORDS to meet the USB turnaround time requirements.</p> <p>2'b00: AHB threshold = MAC threshold 2'b01: AHB threshold = MAC threshold / 2 2'b10: AHB threshold = MAC threshold / 4 2'b11: AHB threshold = MAC threshold / 8</p>
10:2	RW	0x008	<p>TxThrLen Transmit Threshold Length This field specifies Transmit threshold size in DWORDS. This field also forms the MAC threshold and specifies the amount of data, in bytes, to be in the corresponding endpoint transmit FIFO before the core can start a transaction on the USB. When the value of AHBThrRatio is 2'h00, the threshold length must be at least 8 DWORDS. If the AHBThrRatio is nonzero, the application must ensure that the AHB threshold value does not go below the recommended 8 DWORDs. This field controls both isochronous and non-isochronous IN endpoint thresholds. The recommended value for ThrLen is to be the same as the programmed AHB Burst Length (GAHBCFG.HBstLen).</p>
1	RW	0x0	<p>ISOThrEn ISO IN Endpoints Threshold Enable When this bit is set, the core enables threshold for isochronous IN endpoints.</p>

Bit	Attr	Reset Value	Description
0	RW	0x0	NonISOThrEn Non-ISO IN Endpoints Threshold Enable When this bit is set, the core enables threshold for Non Isochronous IN endpoints.

USBOTG_DIEPEMPMSK

Address: Operational Base + offset (0x0834)

Device IN endpoint FIFO empty interrupt mask register

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:0	RW	0x0000	InEpTxfEmpMsk IN EP Tx FIFO Empty Interrupt Mask Bits These bits act as mask bits for DIEPINTn. TxFEmp interrupt One bit per IN Endpoint: Bit 0 for IN endpoint 0 ... Bit 15 for endpoint 15

USBOTG_DEACHINT

Address: Operational Base + offset (0x0838)

Device each endpoint interrupt register

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	EchOutEPInt OUT Endpoint Interrupt Bits One bit per OUT endpoint: Bit 16 for OUT endpoint 0 ... Bit 31 for OUT endpoint 15
15:0	RO	0x0000	EchInEpInt IN Endpoint Interrupt Bits One bit per IN Endpoint: Bit 0 for IN endpoint 0 ... Bit 15 for endpoint 15

USBOTG_DEACHINTMSK

Address: Operational Base + offset (0x083c)

Device each endpoint interrupt register mask

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	EchOutEpMsk OUT EP Interrupt Mask Bits One per OUT Endpoint: Bit 16 for IN endpoint 0 ... Bit 31 for endpoint 15

Bit	Attr	Reset Value	Description
15:0	RW	0x0000	EchInEpMsk IN EP Interrupt Mask Bits One bit per IN Endpoint: Bit 0 for IN endpoint 0 ... Bit 15 for endpoint 15

USBOTG_DIEPEACHMSKn

Address: Operational Base + offset (0x0840)

Device each IN endpoint -n interrupt Register

Bit	Attr	Reset Value	Description
31:14	RO	0x0	reserved
13	RW	0x0	NAKMsk NAK interrupt Mask
12:10	RO	0x0	reserved
9	RW	0x0	BNAInIntrMsk BNA interrupt Mask
8	RW	0x0	TxfifoUndrnMsk Fifo Under run Mask
7	RO	0x0	reserved
6	RW	0x0	INEPNakEffMsk IN Endpoint NAK Effective Mask
5	RW	0x0	INTknEPMisMsk IN Token received with EP Mismatch Mask
4	RW	0x0	INTknTXFEmpMsk IN Token Received When TxFIFO Empty Mask
3	RW	0x0	TimeOUTMsk Timeout Condition Mask(Non-isochronous endpoints)
2	RW	0x0	AHBErrMsk AHB Error Mask
1	RW	0x0	EPDisbldMsk Endpoint Disabled Interrupt Mask
0	RW	0x0	XferComplMsk Transfer Completed Interrupt Mask

USBOTG_DOEPEACHMSKn

Address: Operational Base + offset (0x0880)

Device each out endpoint-n interrupt register

Bit	Attr	Reset Value	Description
31:15	RO	0x0	reserved
14	RW	0x0	NYETMsk NYET interrupt Mask

Bit	Attr	Reset Value	Description
13	RW	0x0	NAKMsk NAK interrupt Mask
12	RW	0x0	BbleErrMsk Babble interrupt Mask
11:10	RO	0x0	reserved
9	RW	0x0	BnaOutIntrMsk BNA interrupt Mask
8	RW	0x0	OutPktErrMsk OUT Packet Error Mask
7	RO	0x0	reserved
6	RW	0x0	Back2BackSETup Back-to-Back SETUP Packets Received Mask Applies to control OUT endpoints only.
5	RO	0x0	reserved
4	RW	0x0	OUTTknEPdisMsk OUT Token Received when Endpoint Disabled Mask Applies to control OUT endpoints only.
3	RW	0x0	SetUPMsk SETUP Phase Done Mask Applies to control endpoints only.
2	RW	0x0	AHBErrMsk AHB Error
1	RW	0x0	EPDisbldMsk Endpoint Disabled Interrupt Mask
0	RW	0x0	XferComplMsk Transfer Completed Interrupt Mask

USBOTG_DIEPCTL0

Address: Operational Base + offset (0x0900)

Device control IN endpoint 0 control register

Bit	Attr	Reset Value	Description
31	R/WSC	0x0	EPEna Endpoint Enable When Scatter/Gather DMA mode is enabled, for IN endpoints this bit indicates that the descriptor structure and data buffer with data ready to transmit is setup. When Scatter/Gather DMA mode is disabled-such as in buffer-pointer based DMA mode-this bit indicates that data is ready to be transmitted on the endpoint. The core clears this bit before setting the following interrupts on this endpoint: Endpoint Disabled; Transfer Completed.

Bit	Attr	Reset Value	Description
30	RWSC	0x0	EPDis Endpoint Disable The application sets this bit to stop transmitting data on an endpoint, even before the transfer for that endpoint is complete. The application must wait for the Endpoint Disabled interrupt before treating the endpoint as disabled. The core clears this bit before setting the Endpoint Disabled Interrupt. The application must set this bit only if Endpoint Enable is already set for this endpoint.
29:28	RO	0x0	reserved
27	WO	0x0	SNAK Set NAK A write to this bit sets the NAK bit for the endpoint. Using this bit, the application can control the transmission of NAK handshakes on an endpoint. The core can also set this bit for an endpoint after a SETUP packet is received on that endpoint.
26	WO	0x0	CNAK Clear NAK A write to this bit clears the NAK bit for the endpoint.
25:23	RO	0x0	reserved
22	RW	0x0	TxFNum Tx FIFO Number For Shared FIFO operation, this value is always set to 0, indicating that control IN endpoint 0 data is always written in the Non-Periodic Transmit FIFO. For Dedicated FIFO operation, this value is set to the FIFO number that is assigned to IN Endpoint 0.
21	RWSC	0x0	Stall STALL Handshake The application can only set this bit, and the core clears it, when a SETUP token is received for this endpoint. If a NAK bit, Global Non-periodic IN NAK, or Global OUT NAK is set along with this bit, the STALL bit takes priority.
20	RO	0x0	reserved

Bit	Attr	Reset Value	Description
19:18	RO	0x0	EPType Endpoint Type Hardcoded to 00 for control
17	RO	0x0	NAKsts NAK Status Indicates the following: 1'b0: The core is transmitting non-NAK handshakes based on the FIFO status 1'b1: The core is transmitting NAK handshakes on this endpoint. When this bit is set, either by the application or core, the core stops transmitting data, even if there is data available in the TxFIFO. Irrespective of this bit's setting, the core always responds to SETUP data packets with an ACK handshake.
16	RO	0x0	reserved
15	RO	0x1	USBActEP USB Active Endpoint This bit is always set to 1, indicating that control endpoint 0 is always active in all configurations and interfaces.
14:11	RW	0x0	NextEp Next Endpoint Applies to non-periodic IN endpoints only. Indicates the endpoint number to be fetched after the data for the current endpoint is fetched. The core can access this field, even when the Endpoint Enable (EPEna) bit is not set. This field is not valid in Slave mode. Note: This field is valid only for Shared FIFO operations.
10:2	RO	0x0	reserved
1:0	RW	0x0	MPS Maximum Packet Size Applies to IN and OUT endpoints. The application must program this field with the maximum packet size for the current logical endpoint. 2'b00: 64 bytes 2'b01: 32 bytes 2'b10: 16 bytes 2'b11: 8 bytes

USBOTG_DIEPINTn

Address: Operational Base + offset (0x0908)

Device Endpoint-n Interrupt Register

Bit	Attr	Reset Value	Description
31:15	RO	0x0	reserved
14	W1C	0x0	NYETInrpt NYET interrupt The core generates this interrupt when a NYET response is transmitted for a non-isochronous OUT endpoint.
13	W1C	0x0	NAKInrpt NAK interrupt The core generates this interrupt when a NAK is transmitted or received by the device. In case of isochronous IN endpoints the interrupt gets generated when a zero length packet is transmitted due to un-availability of data in the TXFifo.
12	W1C	0x0	BbleErrInrpt BbleErr (Babble Error) interrupt The core generates this interrupt when babble is received for the endpoint.
11	W1C	0x0	PktDrpSts Packet Dropped Status This bit indicates to the application that an ISOC OUT packet has been dropped. This bit does not have an associated mask bit and does not generate an interrupt. Dependency: This bit is valid in non-Scatter/Gather DMA mode when periodic transfer interrupt feature is selected.
10	RO	0x0	reserved
9	W1C	0x0	BNAIntr BNA (Buffer Not Available) Interrupt The core generates this interrupt when the descriptor accessed is not ready for the Core to process, such as Host busy or DMA done Dependency: This bit is valid only when Scatter/Gather DMA mode is enabled.

Bit	Attr	Reset Value	Description
8	W1C	0x0	TxfifoUndrn FIFO Under-run Applies to IN endpoints only. The core generates this interrupt when it detects a transmit FIFO under-run condition for this endpoint. Dependency: This interrupt is valid only when both of the following conditions are true: Parameter OTG_ENDED_TX_FIFO==1; Threshold is enabled; OUT Packet Error(OutPktErr). Applies to OUT endpoints only. This interrupt is asserted when the core detects an overflow or a CRC error for an OUT packet. Dependency: This interrupt is valid only when both of the following conditions are true: Parameter OTG_ENDED_TX_FIFO==1; Threshold is enabled.
7	W1C	0x0	TxFEmp Transmit FIFO Empty This bit is valid only for IN Endpoints. This interrupt is asserted when the TxFIFO for this endpoint is either half or completely empty. The half or completely empty status is determined by the TxFIFO Empty Level bit in the Core AHB Configuration register (GAHBCFG.NPTxFEmpLvl)).

Bit	Attr	Reset Value	Description
6	W1C	0x0	<p>INEPNakEff IN Endpoint NAK Effective Applies to periodic IN endpoints only. This bit can be cleared when the application clears the IN endpoint NAK by writing to DIEPCTLn.CNAK. This interrupt indicates that the core has sampled the NAK bit set (either by the application or by the core). The interrupt indicates that the IN endpoint NAK bit set by the application has taken effect in the core. This interrupt does not guarantee that a NAK handshake is sent on the USB. A STALL bit takes priority over a NAK bit. This bit is applicable only when the endpoint is enabled.</p> <p>Back-to-Back SETUP Packets Received (Back2BackSETup) Applies to Control OUT endpoints only. This bit indicates that the core has received more than three back-to-back SETUP packets for this particular endpoint.</p>
5	W1C	0x0	<p>INTknEPMis IN Token Received with EP Mismatch Applies to non-periodic IN endpoints only. Indicates that the data in the top of the non-periodic TxFIFO belongs to an endpoint other than the one for which the IN token was received. This interrupt is asserted on the endpoint for which the IN token was received.</p> <p>Status Phase Received For Control Write (StsPhseRcvd) This interrupt is valid only for Control OUT endpoints and only in Scatter Gather DMA mode. This interrupt is generated only after the core has transferred all the data that the host has sent during the data phase of a control write transfer, to the system memory buffer. The interrupt indicates to the application that the host has switched from data phase to the status phase of a Control Write transfer. The application can use this interrupt to ACK or STALL the Status phase, after it has decoded the data phase. This is applicable only in case of Scatter Gather DMA mode.</p>

Bit	Attr	Reset Value	Description
4	W1C	0x0	INTknTxFEmp IN Token Received When TxFIFO is Empty Indicates that an IN token was received when the associated TxFIFO periodic/nonperiodic) was empty. This interrupt is asserted on the endpoint for which the IN token was received. OUT Token Received When Endpoint Disabled (OUTTknEPdis) Indicates that an OUT token was received when the endpoint was not yet enabled. This interrupt is asserted on the endpoint for which the OUT token was received.
3	W1C	0x0	TimeOUT Timeout Condition In shared TX FIFO mode, applies to non-isochronous IN endpoints only. In dedicated FIFO mode, applies only to Control IN endpoints. In Scatter/Gather DMA mode, the TimeOUT interrupt is not asserted. Indicates that the core has detected a timeout condition on the USB for the last IN token on this endpoint. SETUP Phase Done (SetUp) Applies to control OUT endpoints only. Indicates that the SETUP phase for the control endpoint is complete and no more back-to-back SETUP packets were received for the current control transfer. On this interrupt, the application can decode the received SETUP data packet.
2	W1C	0x0	AHBErr AHB Error Applies to IN and OUT endpoints. This is generated only in Internal DMA mode when there is an AHB error during an AHB read/write. The application can read the corresponding endpoint DMA address register to get the error address.
1	W1C	0x0	EPDisbld Endpoint Disabled Interrupt Applies to IN and OUT endpoints. This bit indicates that the endpoint is disabled per the application's request.

Bit	Attr	Reset Value	Description
0	W1C	0x0	XferCompl Transfer Completed Interrupt Applies to IN and OUT endpoints. When Scatter/Gather DMA mode is enabled: For IN endpoint this field indicates that the requested data from the descriptor is moved from external system memory to internal FIFO. For OUT endpoint this field indicates that the requested data from the internal FIFO is moved to external system memory. This interrupt is generated only when the corresponding endpoint descriptor is closed, and the IOC bit for the corresponding descriptor is set. When Scatter/Gather DMA mode is disabled, this field indicates that the programmed transfer is complete on the AHB as well as on the USB, for this endpoint.

USBOTG_DIEPTSIZEn

Address: Operational Base + offset (0x0910)

Device endpoint n transfer size register

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved

Bit	Attr	Reset Value	Description
30:29	RW	0x0	<p>MC Multi Count Applies to IN endpoints only. For periodic IN endpoints, this field indicates the number of packets that must be transmitted per microframe on the USB. The core uses this field to calculate the data PID for isochronous IN endpoints.</p> <p>2'b01: 1 packet 2'b10: 2 packets 2'b11: 3 packets</p> <p>For non-periodic IN endpoints, this field is valid only in Internal DMA mode. It specifies the number of packets the core must fetch for an IN endpoint before it switches to the endpoint pointed to by the Next Endpoint field of the Device Endpoint-n Control register (DIEPCTLn.NextEp). Received Data PID (RxDPID)</p> <p>Applies to isochronous OUT endpoints only. This is the data PID received in the last packet for this endpoint.</p> <p>2'b00: DATA0 2'b01: DATA2 2'b10: DATA1 2'b11: MDATA</p> <p>SETUP Packet Count (SUPCnt).Applies to control OUT Endpoints only. This field specifies the number of back-to-back SETUP data packets the endpoint can receive.</p> <p>2'b01: 1 packet 2'b10: 2 packets 2'b11: 3 packets</p>

Bit	Attr	Reset Value	Description
28:19	RW	0x000	PktCnt Packet Count Indicates the total number of USB packets that constitute the Transfer Size amount of data for this endpoint. The power-on value is specified for Width of Packet Counters during coreConsultant configuration (parameter OTG_PACKET_COUNT_WIDTH). IN Endpoints: This field is decremented every time a packet (maximum size or short packet) is read from the TxFIFO. OUT Endpoints: This field is decremented every time a packet (maximum size or short packet) is written to the RxFIFO.
18:0	RW	0x00000	XferSize Transfer Size This field contains the transfer size in bytes for the current endpoint. The power-on value is specified for Width of Transfer Size Counters during configuration (parameter OTG_TRANS_COUNT_WIDTH). The core only interrupts the application after it has exhausted the transfer size amount of data. The transfer size can be set to the maximum packet size of the endpoint, to be interrupted at the end of each packet. IN Endpoints: The core decrements this field every time a packet from the external memory is written to the TxFIFO. OUT Endpoints: The core decrements this field every time a packet is read from the RxFIFO and written to the external memory.

USBOTG_DIEPDMA_n

Address: Operational Base + offset (0x0914)

Device endpoint-n DMA address register

Bit	Attr	Reset Value	Description
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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	DMAAddr DMA Address Holds the start address of the external memory for storing or fetching endpoint data. Note: For control endpoints, this field stores control OUT data packets as well as SETUP transaction data packets. When more than three SETUP packets are received back-to-back, the SETUP data packet in the memory is overwritten. This register is incremented on every AHB transaction. The application can give only a DWORD-aligned address. When Scatter/Gather DMA mode is not enabled, the application programs the start address value in this field. When Scatter/Gather DMA mode is enabled, this field indicates the base pointer for the descriptor list.

USBOTG_DTXFSTS_n

Address: Operational Base + offset (0x0918)

Device IN endpoint transmit FIFO status register

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:0	RW	0x0000	INEPTxFSpcAvail IN Endpoint TxFIFO Space Avail Indicates the amount of free space available in the Endpoint TxFIFO. Values are in terms of 32-bit words. 16'h0: Endpoint TxFIFO is full 16'h1: 1 word available 16'h2: 2 words available 16'hn: n words available (where 0 . n . 32,768) 16'h8000: 32,768 words available Others: Reserved

USBOTG_DIEPDMA_{Bn}

Address: Operational Base + offset (0x091c)

Device endpoint-n DMA buffer address register

Bit	Attr	Reset Value	Description
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Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	DMABufferAddr DMA Buffer Address Holds the current buffer address. This register is updated as and when the data transfer for the corresponding end point is in progress. This register is present only in Scatter/Gather DMA mode. Otherwise this field is reserved.

USBOTG_DIEPCTLn

Address: Operational Base + offset (0x0920)

Device endpoint-n control register

Bit	Attr	Reset Value	Description
31	RWSC	0x0	EPEna Endpoint Enable Applies to IN and OUT endpoints. When Scatter/Gather DMA mode is enabled, For IN endpoints this bit indicates that the descriptor structure and data buffer with data ready to transmit is setup. For OUT endpoint it indicates that the descriptor structure and data buffer to receive data is setup. When Scatter/Gather DMA mode is enabled-such as for buffer-pointer based DMA mode: For IN endpoints, this bit indicates that data is ready to be transmitted on the endpoint ; For OUT endpoints, this bit indicates that the application has allocated the memory to start receiving data from the USB. The core clears this bit before setting any of the following interrupts on this endpoint: SETUP Phase Done, Endpoint Disabled, Transfer Completed. Note: For control endpoints in DMA mode, this bit must be set to be able to transfer SETUP data packets in memory.

Bit	Attr	Reset Value	Description
30	RWSC	0x0	EPDis Endpoint Disable Applies to IN and OUT endpoints. The application sets this bit to stop transmitting/receiving data on an endpoint, even before the transfer for that endpoint is complete. The application must wait for the Endpoint Disabled interrupt before treating the endpoint as disabled. The core clears this bit before setting the Endpoint Disabled interrupt. The application must set this bit only if Endpoint Enable is already set for this endpoint.
29	WO	0x0	SetD1PID Set DATA1 PID Applies to interrupt/bulk IN and OUT endpoints only. Writing to this field sets the Endpoint Data PID (DPID) field in this register to DATA1. This field is applicable both for Scatter/Gather DMA mode and non-Scatter/Gather DMA mode. Set Odd (micro) frame (SetOddFr). Applies to isochronous IN and OUT endpoints only. Writing to this field sets the Even/Odd (micro) frame (EO_FrNum) field to odd (micro) frame. This field is not applicable for Scatter/Gather DMA mode.

Bit	Attr	Reset Value	Description
28	WO	0x0	SetDOPID Set DATA0 PID Applies to interrupt/bulk IN and OUT endpoints only. Writing to this field sets the Endpoint Data PID (DPID) field in this register to DATA0. This field is applicable both for Scatter/Gather DMA mode and non-Scatter/Gather DMA mode. In non-Scatter/Gather DMA mode: Set Even (micro) frame (SetEvenFr) Applies to isochronous IN and OUT endpoints only. Writing to this field sets the Even/Odd (micro) frame (EO_FrNum) field to even (micro) frame. When Scatter/Gather DMA mode is enabled, this field is reserved. The frame number in which to send data is in the transmit descriptor structure. The frame in which to receive data is updated in receipt descriptor structure.
27	WO	0x0	SNAK Set NAK Applies to IN and OUT endpoints. A write to this bit sets the NAK bit for the endpoint. Using this bit, the application can control the transmission of NAK handshakes on an endpoint. The core can also set this bit for OUT endpoints on a Transfer Completed interrupt, or after a SETUP is received on the endpoint.
26	WO	0x0	CNAK Clear NAK Applies to IN and OUT endpoints. A write to this bit clears the NAK bit for the endpoint.

Bit	Attr	Reset Value	Description
25:22	RW	0x0	<p>TxFNum Tx FIFO Number Shared FIFO Operation: non-periodic endpoints must set this bit to zero. Periodic endpoints must map this to the corresponding Periodic Tx FIFO number. 4'h0: Non-Periodic Tx FIFO; Others: Specified Periodic Tx FIFO number. Note: An interrupt IN endpoint can be configured as a non-periodic endpoint for applications such as mass storage. The core treats an IN endpoint as a non-periodic endpoint if the TxFNum field is set to 0. Otherwise, a separate periodic FIFO must be allocated for an interrupt IN endpoint, and the number of this FIFO must be programmed into the TxFNum field. Configuring an interrupt IN endpoint as a non-periodic endpoint saves the extra periodic FIFO area. Dedicated FIFO Operation: these bits specify the FIFO number associated with this endpoint. Each active IN endpoint must be programmed to a separate FIFO number. This field is valid only for IN endpoints.</p>
21	RW	0x0	<p>Stall STALL Handshake Applies to non-control, non-isochronous IN and OUT endpoints only. The application sets this bit to stall all tokens from the USB host to this endpoint. If a NAK bit, Global Non-periodic IN NAK, or Global OUT NAK is set along with this bit, the STALL bit takes priority. Only the application can clear this bit, never the core. Applies to control endpoints only. The application can only set this bit, and the core clears it, when a SETUP token is received for this endpoint. If a NAK bit, Global Non-periodic IN NAK, or Global OUT NAK is set along with this bit, the STALL bit takes priority. Irrespective of this bit's setting, the core always responds to SETUP data packets with an ACK handshake.</p>

Bit	Attr	Reset Value	Description
20	RW	0x0	Snp Snoop Mode Applies to OUT endpoints only. This bit configures the endpoint to Snoop mode. In Snoop mode, the core does not check the correctness of OUT packets before transferring them to application memory.
19:18	RW	0x0	EPType Endpoint Type Applies to IN and OUT endpoints. This is the transfer type supported by this logical endpoint. 2'b00: Control 2'b01: Isochronous 2'b10: Bulk 2'b11: Interrupt
17	RO	0x0	NAKSts NAK Status Applies to IN and OUT endpoints. Indicates the following: 1'b0: The core is transmitting non-NAK handshakes based on the FIFO status. 1'b1: The core is transmitting NAK handshakes on this endpoint. When either the application or the core sets this bit: The core stops receiving any data on an OUT endpoint, even if there is space in the RxFIFO to accommodate the incoming packet. For non-isochronous IN endpoints: The core stops transmitting any data on an IN endpoint, even if there data is available in the TxFIFO. For isochronous IN endpoints: The core sends out a zero-length data packet, even if there data is available in the TxFIFO. Irrespective of this bit's setting, the core always responds to SETUP data packets with an ACK handshake.

Bit	Attr	Reset Value	Description
16	RO	0x0	<p>DPID Endpoint Data PID Applies to interrupt/bulk IN and OUT endpoints only. Contains the PID of the packet to be received or transmitted on this endpoint. The application must program the PID of the first packet to be received or transmitted on this endpoint, after the endpoint is activated. The applications use the SetD1PID and SetD0PID fields of this register to program either DATA0 or DATA1 PID.</p> <p>1'b0: DATA0 1'b1: DATA1</p> <p>This field is applicable both for Scatter/Gather DMA mode and non-Scatter/Gather DMA mode. Even/Odd (Micro)Frame (EO_FrNum) In non-Scatter/Gather DMA mode:</p> <p>Applies to isochronous IN and OUT endpoints only. Indicates the (micro) frame number in which the core transmits/receives isochronous data for this endpoint. The application must program the even/odd (micro) frame number in which it intends to transmit/receive isochronous data for this endpoint using the SetEvnFr and SetOddFr fields in this register.</p> <p>1'b0: Even (micro)frame 1'b1: Odd (micro)frame</p> <p>When Scatter/Gather DMA mode is enabled, this field is reserved. The frame number in which to send data is provided in the transmit descriptor structure. The frame in which data is received is updated in receive descriptor structure.</p>
15	RWSC	0x0	<p>USBActEP USB Active Endpoint Applies to IN and OUT endpoints. Indicates whether this endpoint is active in the current configuration and interface. The core clears this bit for all endpoints (other than EP 0) after detecting a USB reset. After receiving the SetConfiguration and SetInterface commands, the application must program endpoint registers accordingly and set this bit.</p>

Bit	Attr	Reset Value	Description
14:11	RW	0x0	NextEp Next Endpoint Applies to non-periodic IN endpoints only. Indicates the endpoint number to be fetched after the data for the current endpoint is fetched. The core can access this field, even when the Endpoint Enable (EPEna) bit is low. This field is not valid in Slave mode operation. Note: This field is valid only for Shared FIFO operations.
10:0	RW	0x000	MPS Maximum Packet Size Applies to IN and OUT endpoints. The application must program this field with the maximum packet size for the current logical endpoint. This value is in bytes.

USBOTG_DOEPCCTL0

Address: Operational Base + offset (0x0b00)

Device control OUT endpoint 0 control register

Bit	Attr	Reset Value	Description
31	RWSC	0x0	EPEna Endpoint Enable When Scatter/Gather DMA mode is enabled, for OUT endpoints this bit indicates that the descriptor structure and data buffer to receive data is setup. When Scatter/Gather DMA mode is disabled? such as for buffer-pointer based DMA mode)-this bit indicates that the application has allocated the memory to start receiving data from the USB. The core clears this bit before setting any of the following interrupts on this endpoint: SETUP Phase Done, Endpoint Disabled, Transfer Completed. Note: In DMA mode, this bit must be set for the core to transfer SETUP data packets into memory.
30	WO	0x0	EPDis Endpoint Disable The application cannot disable control OUT endpoint 0.
29:28	RO	0x0	reserved

Bit	Attr	Reset Value	Description
27	WO	0x0	SNAK Set NAK A write to this bit sets the NAK bit for the endpoint. Using this bit, the application can control the transmission of NAK handshakes on an endpoint. The core can also set bit on a Transfer Completed interrupt, or after a SETUP is received on the endpoint.
26	WO	0x0	CNAK Clear NAK A write to this bit clears the NAK bit for the endpoint.
25:22	RO	0x0	reserved
21	RWSC	0x0	Stall STALL Handshake The application can only set this bit, and the core clears it, when a SETUP token is received for this endpoint. If a NAK bit or Global OUT NAK is set along with this bit, the STALL bit takes priority. Irrespective of this bit's setting, the core always responds to SETUP data packets with an ACK handshake.
20	RW	0x0	Snp Snoop Mode This bit configures the endpoint to Snoop mode. In Snoop mode, the core does not check the correctness of OUT packets before transferring them to application memory.
19:18	RO	0x0	EPType Endpoint Type Hardcoded to 2'b00 for control.
17	RO	0x0	NAKsts NAK Status Indicates the following: 1'b0: The core is transmitting non-NAK handshakes based on the FIFO status. 1'b1: The core is transmitting NAK handshakes on this endpoint. When either the application or the core sets this bit, the core stops receiving data, even if there is space in the RxFIFO to accommodate the incoming packet. Irrespective of this bit setting, the core always responds to SETUP data packets with an ACK handshake.

Bit	Attr	Reset Value	Description
16	RO	0x0	reserved
15	RO	0x0	USBActEP USB Active Endpoint This bit is always set to 1, indicating that a control endpoint 0 is always active in all configurations and interfaces.
14:2	RO	0x0	reserved
1:0	RO	0x0	MPS Maximum Packet Size The maximum packet size for control OUT endpoint 0 is the same as what is programmed in control IN Endpoint 0. 2'b00: 64 bytes 2'b01: 32 bytes 2'b10: 16 bytes 2'b11: 8 bytes

USBOTG_DOEPINTn

Address: Operational Base + offset (0x0b08)

Device endpoint-n control register

Bit	Attr	Reset Value	Description
31:15	RO	0x0	reserved
14	W1C	0x0	NYETIntrpt NYET interrupt The core generates this interrupt when a NYET response is transmitted for a non-isochronous OUT endpoint.
13	W1C	0x0	NAKIntrpt NAK interrupt The core generates this interrupt when a NAK is transmitted or received by the device. In case of isochronous IN endpoints the interrupt gets generated when a zero length packet is transmitted due to un-availability of data in the TXFifo.
12	W1C	0x0	BbleErrIntrpt BbleErr (Babble Error) interrupt The core generates this interrupt when babble is received for the endpoint.

Bit	Attr	Reset Value	Description
11	W1C	0x0	PktDrpSts Packet Dropped Status This bit indicates to the application that an ISOC OUT packet has been dropped. This bit does not have an associated mask bit and does not generate an interrupt. Dependency: This bit is valid in non-Scatter/Gather DMA mode when periodic transfer interrupt feature is selected.
10	RO	0x0	reserved
9	W1C	0x0	BNAIntr BNA (Buffer Not Available) Interrupt The core generates this interrupt when the descriptor accessed is not ready for the Core to process, such as Host busy or DMA done. Dependency: This bit is valid only when Scatter/Gather DMA mode is enabled.
8	W1C	0x0	TxfifoUndrn FIFO Underrun Applies to IN endpoints only. The core generates this interrupt when it detects a transmit FIFO under-run condition for this endpoint. Dependency: This interrupt is valid only when both of the following conditions are true: Parameter OTG_ENDED_TX_FIFO==1, Threshold is enabled, OUT Packet Error (OutPktErr). Applies to OUT endpoints only. This interrupt is asserted when the core detects an overflow or a CRC error for an OUT packet. Dependency: This interrupt is valid only when both of the following conditions are true: Parameter OTG_ENDED_TX_FIFO==1, Thresholding is enabled.
7	W1C	0x0	TxFEmp Transmit FIFO Empty This bit is valid only for IN Endpoints. This interrupt is asserted when the TxFIFO for this endpoint is either half or completely empty. The half or completely empty status is determined by the TxFIFO Empty Level bit in the Core AHB Configuration register(GAHBCFG.NPTxFEmpLvl)).

Bit	Attr	Reset Value	Description
6	W1C	0x0	<p>INEPNakEff IN Endpoint NAK Effective Applies to periodic IN endpoints only. This bit can be cleared when the application clears the IN endpoint NAK by writing to DIEPCTLn.CNAK. This interrupt indicates that the core has sampled the NAK bit set (either by the application or by the core). The interrupt indicates that the IN endpoint NAK bit set by the application has taken effect in the core. This interrupt does not guarantee that a NAK handshake is sent on the USB. A STALL bit takes priority over a NAK bit. This bit is applicable only when the endpoint is enabled. Back-to-Back SETUP Packets Received (Back2BackSETup) Applies to Control OUT endpoints only. This bit indicates that the core has received more than three back-to-back SETUP packets for this particular endpoint.</p>
5	W1C	0x0	<p>INTknEPMis IN Token Received with EP Mismatch Applies to non-periodic IN endpoints only. Indicates that the data in the top of the non-periodic TxFIFO belongs to an endpoint other than the one for which the IN token was received. This interrupt is asserted on the endpoint for which the IN token was received. Status Phase Received For Control Write (StsPhseRcvd) This interrupt is valid only for Control OUT endpoints and only in Scatter Gather DMA mode.</p>
4	W1C	0x0	<p>INTknTxFEmp IN Token Received When TxFIFO is Empty Indicates that an IN token was received when the associated TxFIFO periodic/non-periodic was empty. This interrupt is asserted on the endpoint for which the IN token was received. OUT Token Received When Endpoint Disabled (OUTTknEPdis) Indicates that an OUT token was received when the endpoint was not yet enabled. This interrupt is asserted on the endpoint for which the OUT token was received.</p>

Bit	Attr	Reset Value	Description
3	W1C	0x0	<p>TimeOUT Timeout Condition In shared TX FIFO mode, applies to non-isochronous IN endpoints only. In dedicated FIFO mode, applies only to Control IN endpoints. In Scatter/Gather DMA mode, the Timeout interrupt is not asserted.</p> <p>Indicates that the core has detected a timeout condition on the USB for the last IN token on this endpoint. SETUP Phase Done (SetUp). Applies to control OUT endpoints only.</p> <p>Indicates that the SETUP phase for the control endpoint is complete and no more back-to-back SETUP packets were received for the current control transfer. On this interrupt, the application can decode the received SETUP data packet.</p>
2	W1C	0x0	<p>AHBErr AHB Error Applies to IN and OUT endpoints. This is generated only in Internal DMA mode when there is an AHB error during an AHB read/write. The application can read the corresponding endpoint DMA address register to get the error address.</p>
1	W1C	0x0	<p>EPDisbld Endpoint Disabled Interrupt Applies to IN and OUT endpoints. This bit indicates that the endpoint is disabled per the application's request.</p>

Bit	Attr	Reset Value	Description
0	W1C	0x0	XferCompl Transfer Completed Interrupt Applies to IN and OUT endpoints. When Scatter/Gather DMA mode is enabled For IN endpoint this field indicates that the requested data from the descriptor is moved from external system memory to internal FIFO. For OUT endpoint this field indicates that the requested data from the internal FIFO is moved to external system memory. This interrupt is generated only when the corresponding endpoint descriptor is closed, and the IOC bit for the corresponding descriptor is set. When Scatter/Gather DMA mode is disabled, this field indicates that the programmed transfer is complete on the AHB as well as on the USB, for this endpoint.

USBOTG_DOEPTSIZn

Address: Operational Base + offset (0x0b10)

Device endpoint n transfer size register

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved

Bit	Attr	Reset Value	Description
30:29	RW	0x0	<p>MC Multi Count Applies to IN endpoints only. For periodic IN endpoints, this field indicates the number of packets that must be transmitted per micro-frame on the USB. The core uses this field to calculate the data PID for isochronous IN endpoints.</p> <p>2'b01: 1 packet 2'b10: 2 packets 2'b11: 3 packets</p> <p>For non-periodic IN endpoints, this field is valid only in Internal DMA mode. It specifies the number of packets the core must fetch for an IN endpoint before it switches to the endpoint pointed to by the Next Endpoint field of the Device Endpoint-n Control register (DIEPCTLn.NextEp). Received Data PID (RxDPID)</p> <p>Applies to isochronous OUT endpoints only. This is the data PID received in the last packet for this endpoint.</p> <p>2'b00: DATA0 2'b01: DATA2 2'b10: DATA1 2'b11: MDATA</p> <p>SETUP Packet Count (SUPCnt).Applies to control OUT Endpoints only. This field specifies the number of back-to-back SETUP data packets the endpoint can receive.</p> <p>2'b01: 1 packet 2'b10: 2 packets 2'b11: 3 packets</p>

Bit	Attr	Reset Value	Description
28:19	RW	0x000	PktCnt Packet Count Indicates the total number of USB packets that constitute the Transfer Size amount of data for this endpoint. The power-on value is specified for Width of Packet Counters (parameter OTG_PACKET_COUNT_WIDTH). IN Endpoints: This field is decremented every time a packet (maximum size or short packet) is read from the TxFIFO. OUT Endpoints: This field is decremented every time a packet (maximum size or short packet) is written to the RxFIFO.
18:0	RW	0x00000	XferSize Transfer Size This field contains the transfer size in bytes for the current endpoint. The power-on value is specified for Width of Transfer Size Counters (parameter OTG_TRANS_COUNT_WIDTH). The core only interrupts the application after it has exhausted the transfer size amount of data. The transfer size can be set to the maximum packet size of the endpoint, to be interrupted at the end of each packet. IN Endpoints: The core decrements this field every time a packet from the external memory is written to the TxFIFO. OUT Endpoints: The core decrements this field every time a packet is read from the RxFIFO and written to the external memory.

USBOTG_DOEPDMAn

Address: Operational Base + offset (0x0b14)

Device Endpoint-n DMA Address Register

Bit	Attr	Reset Value	Description
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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	DMAAddr DMA Address Holds the start address of the external memory for storing or fetching endpoint data. Note: For control endpoints, this field stores control OUT data packets as well as SETUP transaction data packets. When more than three SETUP packets are received back-to-back, the SETUP data packet in the memory is overwritten. This register is incremented on every AHB transaction. The application can give only a DWORD-aligned address. When Scatter/Gather DMA mode is not enabled, the application programs the start address value in this field. When Scatter/Gather DMA mode is enabled, this field indicates the base pointer for the descriptor list.

USBOTG_DOEPDMA_n

Address: Operational Base + offset (0x0b1c)

Device endpoint-n DMA buffer address register

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	DMABufferAddr DMA Buffer Address Holds the current buffer address. This register is updated as and when the data transfer for the corresponding end point is in progress. This register is present only in Scatter/Gather DMA mode. Otherwise this field is reserved.

USBOTG_DOEPCTL_n

Address: Operational Base + offset (0x0b20)

Device endpoint-n control register

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31	RWSC	0x0	<p>EPEna Endpoint Enable Applies to IN and OUT endpoints. When Scatter/Gather DMA mode is enabled, For IN endpoints this bit indicates that the descriptor structure and data buffer with data ready to transmit is setup. For OUT endpoint it indicates that the descriptor structure and data buffer to receive data is setup. When Scatter/Gather DMA mode is enabled-such as for buffer-pointer based DMA mode: For IN endpoints, this bit indicates that data is ready to be transmitted on the endpoint; For OUT endpoints, this bit indicates that the application has allocated the memory to start receiving data from the USB. The core clears this bit before setting any of the following interrupts on this endpoint: SETUP Phase Done, Endpoint Disabled, Transfer Completed. Note: For control endpoints in DMA mode, this bit must be set to be able to transfer SETUP data packets in memory.</p>
30	RWSC	0x0	<p>EPDis Endpoint Disable Applies to IN and OUT endpoints. The application sets this bit to stop transmitting/receiving data on an endpoint, even before the transfer for that endpoint is complete. The application must wait for the Endpoint Disabled interrupt before treating the endpoint as disabled. The core clears this bit before setting the Endpoint Disabled interrupt. The application must set this bit only if Endpoint Enable is already set for this endpoint.</p>

Bit	Attr	Reset Value	Description
29	RO	0x0	SetD1PID Field0001 Abstract Applies to interrupt/bulk IN and OUT endpoints only. Writing to this field sets the Endpoint Data PID (DPID) field in this register to DATA1. This field is applicable both for Scatter/Gather DMA mode and non-Scatter/Gather DMA mode. Set Odd (micro) frame (SetOddFr). Applies to isochronous IN and OUT endpoints only. Writing to this field sets the Even/Odd (micro) frame (EO_FrNum) field to odd (micro) frame. This field is not applicable for Scatter/Gather DMA mode.
28	WO	0x0	SetD0PID Set DATA0 PID Applies to interrupt/bulk IN and OUT endpoints only. Writing to this field sets the Endpoint Data PID (DPID) field in this register to DATA0. This field is applicable both for Scatter/Gather DMA mode and non-Scatter/Gather DMA mode. In non-Scatter/Gather DMA mode: Set Even (micro) frame (SetEvenFr) Applies to isochronous IN and OUT endpoints only. Writing to this field sets the Even/Odd (micro) frame (EO_FrNum) field to even (micro) frame. When Scatter/Gather DMA mode is enabled, this field is reserved. The frame number in which to send data is in the transmit descriptor structure. The frame in which to receive data is updated in receipt descriptor structure.
27	WO	0x0	SNAK Set NAK Applies to IN and OUT endpoints. A write to this bit sets the NAK bit for the endpoint. Using this bit, the application can control the transmission of NAK handshakes on an endpoint. The core can also set this bit for OUT endpoints on a Transfer Completed interrupt, or after a SETUP is received on the endpoint.

Bit	Attr	Reset Value	Description
26	WO	0x0	CNAK Clear NAK Applies to IN and OUT endpoints. A write to this bit clears the NAK bit for the endpoint.
25:22	RW	0x0	TxFNum TxFIFO Number Shared FIFO Operation: non-periodic endpoints must set this bit to zero. Periodic endpoints must map this to the corresponding Periodic TxFIFO number. 4'h0: Non-Periodic TxFIFO; Others: Specified Periodic TxFIFO number. Note: An interrupt IN endpoint can be configured as a non-periodic endpoint for applications such as mass storage. The core treats an IN endpoint as a non-periodic endpoint if the TxFNum field is set to 0. Otherwise, a separate periodic FIFO must be allocated for an interrupt IN endpoint using coreConsultant, and the number of this FIFO must be programmed into the TxFNum field. Configuring an interrupt IN endpoint as a non-periodic endpoint saves the extra periodic FIFO area. Dedicated FIFO Operation: these bits specify the FIFO number associated with this endpoint. Each active IN endpoint must be programmed to a separate FIFO number. This field is valid only for IN endpoints.

Bit	Attr	Reset Value	Description
21	RW	0x0	<p>Stall STALL Handshake</p> <p>Applies to non-control, non-isochronous IN and OUT endpoints only. The application sets this bit to stall all tokens from the USB host to this endpoint. If a NAK bit, Global Non-periodic IN NAK, or Global OUT NAK is set along with this bit, the STALL bit takes priority. Only the application can clear this bit, never the core.</p> <p>Applies to control endpoints only. The application can only set this bit, and the core clears it, when a SETUP token is received for this endpoint. If a NAK bit, Global Non-periodic IN NAK, or Global OUT NAK is set along with this bit, the STALL bit takes priority. Irrespective of this bit's setting, the core always responds to SETUP data packets with an ACK handshake.</p>
20	RW	0x0	<p>Snp Snoop Mode</p> <p>Applies to OUT endpoints only. This bit configures the endpoint to Snoop mode. In Snoop mode, the core does not check the correctness of OUT packets before transferring them to application memory.</p>
19:18	RW	0x0	<p>EPType Endpoint Type</p> <p>Applies to IN and OUT endpoints. This is the transfer type supported by this logical endpoint.</p> <ul style="list-style-type: none"> 2'b00: Control 2'b01: Isochronous 2'b10: Bulk 2'b11: Interrupt

Bit	Attr	Reset Value	Description
17	RO	0x0	NAKSts NAK Status Applies to IN and OUT endpoints. Indicates the following: 1'b0: The core is transmitting non-NAK handshakes based on the FIFO status. 1'b1: The core is transmitting NAK handshakes on this endpoint. When either the application or the core sets this bit: The core stops receiving any data on an OUT endpoint, even if there is space in the RxFIFO to accommodate the incoming packet.

Bit	Attr	Reset Value	Description
16	RO	0x0	<p>DPID Endpoint Data PID Applies to interrupt/bulk IN and OUT endpoints only. Contains the PID of the packet to be received or transmitted on this endpoint. The application must program the PID of the first packet to be received or transmitted on this endpoint, after the endpoint is activated. The applications use the SetD1PID and SetD0PID fields of this register to program either DATA0 or DATA1 PID.</p> <p>1'b0: DATA0 1'b1: DATA1</p> <p>This field is applicable both for Scatter/Gather DMA mode and non-Scatter/Gather DMA mode. Even/Odd (Micro) Frame (EO_FrNum). In non-Scatter/Gather DMA mode: Applies to isochronous IN and OUT endpoints only. Indicates the (micro) frame number in which the core transmits/receives isochronous data for this endpoint. The application must program the even/odd (micro) frame number in which it intends to transmit/receive isochronous data for this endpoint using the SetEvnFr and SetOddFr fields in this register.</p> <p>1'b0: Even (micro)frame 1'b1: Odd (micro)frame</p> <p>When Scatter/Gather DMA mode is enabled, this field is reserved. The frame number in which to send data is provided in the transmit descriptor structure. The frame in which data is received is updated in receive descriptor structure.</p>
15	RWSC	0x0	<p>USBActEP USB Active Endpoint Applies to IN and OUT endpoints. Indicates whether this endpoint is active in the current configuration and interface. The core clears this bit for all endpoints (other than EP 0) after detecting a USB reset. After receiving the SetConfiguration and SetInterface commands, the application must program endpoint registers accordingly and set this bit.</p>

Bit	Attr	Reset Value	Description
14:11	RW	0x0	NextEp Next Endpoint Applies to non-periodic IN endpoints only. Indicates the endpoint number to be fetched after the data for the current endpoint is fetched. The core can access this field, even when the Endpoint Enable (EPEna) bit is low. This field is not valid in Slave mode operation. Note: This field is valid only for Shared FIFO operations.
10:0	RW	0x000	MPS Maximum Packet Size Applies to IN and OUT endpoints. The application must program this field with the maximum packet size for the current logical endpoint. This value is in bytes.

USBOTG_PCGCR

Address: Operational Base + offset (0x0b24)

Power and clock gating control register

Bit	Attr	Reset Value	Description
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Bit	Attr	Reset Value	Description
31:14	RW	0x0802e	<p>RestoreValue Restore Value (Applicable only when Hibernation is enabled (OTG_EN_PWROPT=2). Defines port clock select for different speeds.</p> <ul style="list-style-type: none"> [31] if_dev_mode <ul style="list-style-type: none"> - 1: Device mode, core restored as device - 0: Host mode, core restored as host [30:29] p2hd_prt_spd (PRT speed) <ul style="list-style-type: none"> - 00: HS - 01: FS - 10: LS - 11: Reserved [28:27] p2hd_dev_enum_spd (Device enumerated speed) <ul style="list-style-type: none"> - 00: HS - 01: FS (30/60 MHz clock) - 10: LS - 11: FS (48 MHz clock) [26:20] mac_dev_addr (MAC device address) Device address [19] mac_termselect (Termination selection) <ul style="list-style-type: none"> - 0: HS_TERM (Program for High Speed) - 1: FS_TERM (Program for Full Speed) [18:17] mac_xcvrselect (Transceiver select) <ul style="list-style-type: none"> - 00: HS_XCVR (High Speed) - 01: FS_XCVR (Full Speed) - 10: LS_XCVR (Low Speed) - 11: LFS_XCVR (Reserved) [16] sh2pl_prt_ctl[0] <ul style="list-style-type: none"> - 1: port_power enabled - 0: port_power disabled [15:14] prt_clk_sel (Refer prt_clk_sel table)
13	RW	0x0	<p>EssRegRestored Essential Register Values Restored (Applicable only when Hibernation is enabled (OTG_EN_PWROPT=2). When a value of 1 is written to this field, it indicates that register values of essential registers have been restored.</p>
12:10	RO	0x0	reserved

Bit	Attr	Reset Value	Description
9	RO	0x0	<p>RestoreMode Restore Mode (Applicable only when Hibernation is enabled (OTG_EN_PWRROPT=2). The application should program this bit to specify the restore mode during RESTORE POINT before programming PCGCCTL.EssRegRest bit is set.</p> <p>Host Mode: 1'b0: Host Initiated Resume, Host Initiated Reset 1'b1: Device Initiated Remote Wake up</p> <p>Device Mode: 1'b0: Device Initiated Remote Wake up 1'b1: Host Initiated Resume, Host Initiated Reset</p>
8	RW	0x0	<p>ResetAfterSusp Reset After Suspend Applicable in Partial power-down mode. In partial power-down mode of operation, this bit needs to be set in host mode before clamp is removed if the host needs to issue reset after suspend. If this bit is not set, then the host issues resume after suspend. This bit is not applicable in device mode and non-partial power-down mode. In Hibernation mode, this bit needs to be set at RESTORE_POINT before PCGCCTL.EssRegRestored is set. In this case, PCGCCTL.restore_mode needs to be set to wait_restore.</p>
7	RO	0x0	<p>L1Suspended Deep Sleep This bit indicates that the PHY is in deep sleep when in L1 state.</p>
6	RO	0x0	<p>PhySleep PHY in Sleep This bit indicates that the PHY is in the Sleep state.</p>
5	RW	0x0	<p>Enbl_L1Gating Enable Sleep Clock Gating When this bit is set, core internal clock gating is enabled in Sleep state if the core cannot assert utmi_l1_suspend_n. When this bit is not set, the PHY clock is not gated in Sleep state.</p>
4	RO	0x0	reserved

Bit	Attr	Reset Value	Description
3	RW	0x0	RstPdwnModule Reset Power-Down Modules This bit is valid only in Partial Power-Down mode. The application sets this bit when the power is turned off. The application clears this bit after the power is turned on and the PHY clock is up.
2	RW	0x0	PwrClmp Power Clamp This bit is valid only in Partial Power-Down mode (OTG_EN_PWRLOPT = 1). The application sets this bit before the power is turned off to clamp the signals between the power-on modules and the power-off modules. The application clears the bit to disable the clamping before the power is turned on.
1	RW	0x0	GateHclk Gate Hclk The application sets this bit to gate hclk to modules other than the AHB Slave and Master and wakeup logic when the USB is suspended or the session is not valid. The application clears this bit when the USB is resumed or a new session starts.
0	RW	0x0	StopPclk Stop Pclk The application sets this bit to stop the PHY clock (phy_clk) when the USB is suspended, the session is not valid, or the device is disconnected. The application clears this bit when the USB is resumed or a new session starts.

1.7 Interface description

Table 1-2 USB OTG 2.0 Interface Description

Module Pin	Direction	Pad Name	pinmux
OTG_VSSAC	AG	OTG_VSSAC	-
OTG_DVSS	DG	OTG_DVSS	-
OTG_DVDD	DP	OTG_DVDD	-
OTG_VDD18	AP	OTG_VDD18	-
OTG_DM	A	OTG_DM	-
OTG_RKELVIN	A	OTG_RKELVIN	-

Module Pin	Direction	Pad Name	pinmux
OTG_DP	A	OTG_DP	-
OTG_VSSA	AG	OTG_VSSA	-
OTG_VBUS	A	OTG_VBUS	-
OTG_VDD33	AP	OTG_VDD33	-
OTG_ID	A	OTG_ID	-
OTG_drv_vbus	O	IO_UART3GPSrtsn_USBdrvbus0_GPIO30gpio7b2	

Note: **A**—Analog pad ; **AP**—Analog power; **AG**—Analog ground ; **DP**—Digital power ; **DG**— Digital ground;

1.8 Application Note

1.8.1 Resume from Suspend Mode

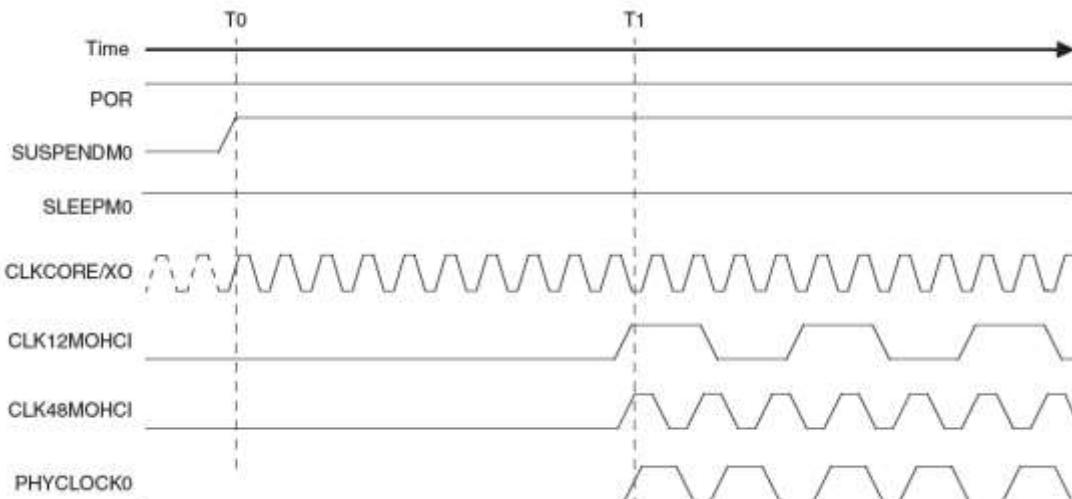


Fig. 1-12 Resume Timing Sequence

When COMMONONNN = 1'b1, $T_1 < T_0 + 805 \mu s$

When COMMONONNN = 1'b0, $T_1 < T_0 + 16 \mu s$

1.8.2 Reset a port

Because the assertion of PORTRESET can occur during data reception or transmission, PORTRESET must be de-asserted as follows:

- ❖ Reception:
 - ◆ FS device: After a minimum of 3 μs of stable SE0 on LINESTATE [1:0]
 - ◆ FS/LS host: After a minimum of 8 bit times of J state on LINESTATE [1:0]
 - ◆ HS host/device: A minimum of 150 μs after asserting PORTRESET
- ❖ Transmission:
 - ◆ FS device: After the controller sets both TXVALID and TXVALIDH to 1'b0, followed by a minimum of 3 μs of stable SE0 on LINESTATE [1:0]
 - ◆ FS/LS host: After the controller sets both TXVALID0 and TXVALIDH0 to 1'b0, followed by a minimum of 8 bit times of J state on LINESTATE [1:0]
 - ◆ HS host/device: A minimum of 150 μs after the controller sets both TXVALID0 and TXVALIDH0 to 1'b0. The preceding requirements ensure that there is no activity on the USB when PORTRESET0 is de-asserted.

To avoid any data glitches during port reset, the controller must place the USB 2.0 PHY into a safe state. A safe state for host and device ports is defined as follows:

- ❖ Host: The USB 2.0 PHY is set to Non-Driving (OPMODE [1:0] = 2'b01), and the 15-k Ω

pull-down resistors are enabled (DPPULLDOWN and DMPULLDOWN = 1'b1).

❖ Device: The USB 2.0 PHY is set to Non-Driving (OPMODE [1:0] = 2'b01), which disconnects the 1.5-kΩ resistor from the D+ line.

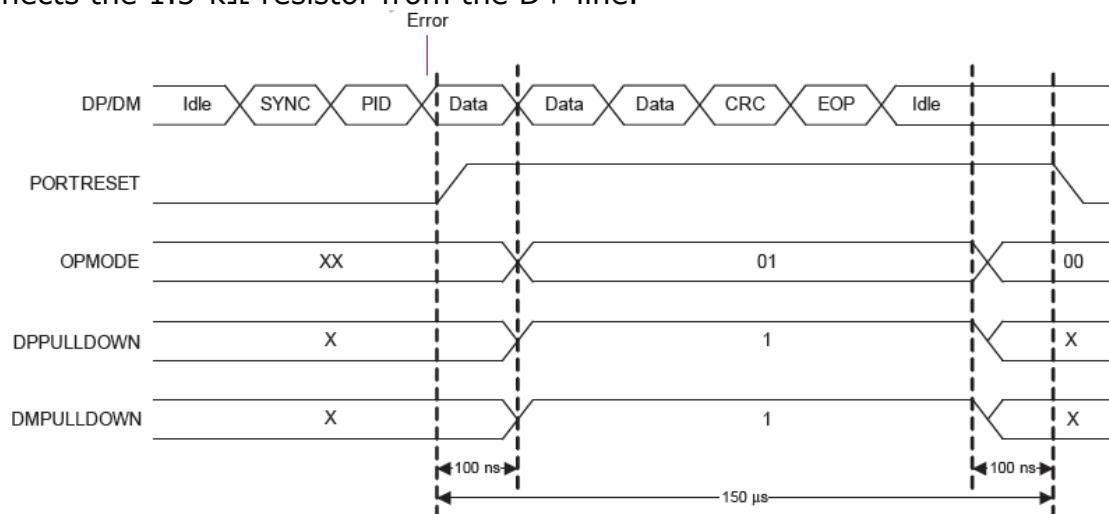


Fig. 1-13 Reset a port when receiving

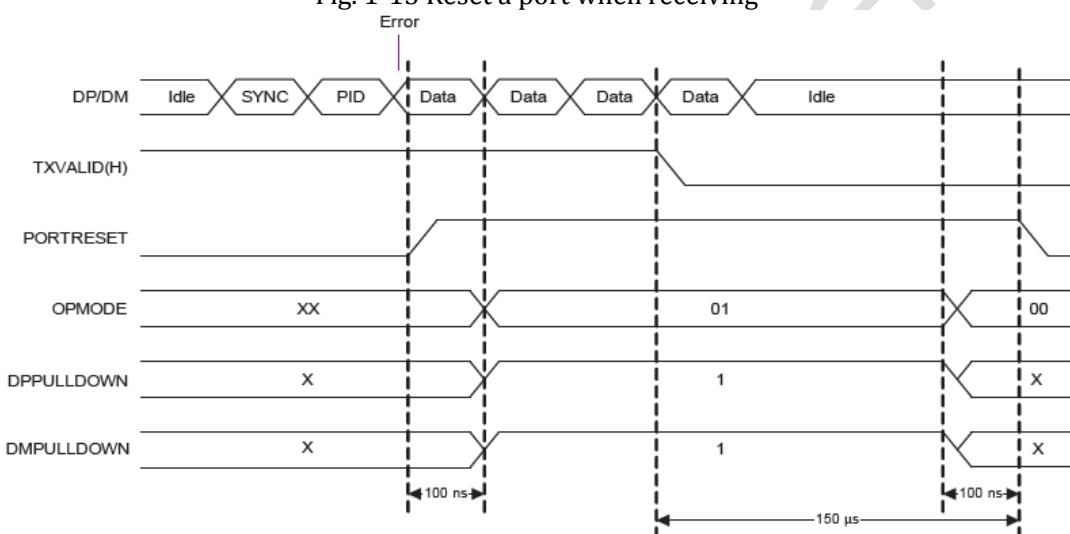


Fig. 1-14 Reset a port when transmitting

1.8.3 VBUS threshold

High (min) = 1.7 V

Low (max) = 0.9 V

Chapter 2 USB2.0 Host(0)

2.1 Overview

USB HOST0 supports Non_OTG Host functions and is fully compliant with USB2.0 specification, and support high-speed(480Mbps) transfer. It is optimized for point-to-point applications (no hub, direct connection to device).

2.1.1 Features

- Compliant with the USB2.0 Specification
- Operates in Non_OTG Host mode
- Operates in High-Speed mode
- Support 512x64 data buffer and 68x32 descriptor buffer .
- Support EHCI for High-Speed transfer

2.2 Block Diagram

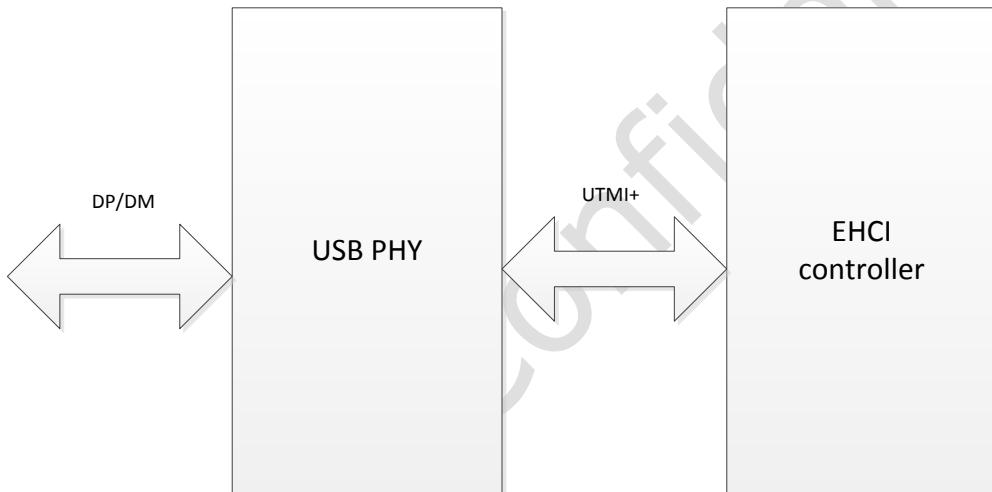


Fig. 2-1 USB HOST 2.0 Architecture

2.3 USB Host2.0 PHY

Much the same as USB OTG PHY with no Device Mode supported. See Chapter OTG for more information.

USB Host2.0 PHY doesn't support UART-DEBUG function.

2.4 Interface description

Table 2-1 USB HOST 2.0 Interface Description

Module Pin	Direction	Pad Name	pinmux
HOST0_VSSAC	AG	HOST0_VSSAC	-
HOST0_DVSS	DG	HOST0_DVSS	-
HOST0_DVDD	DP	HOST0_DVDD	-
HOST0_VDD18	AP	HOST0_VDD18	-
HOST0_DM	A	HOST0_DM	-
HOST0_RKELVIN	A	HOST0_RKELVIN	-
HOST0_DP	A	HOST0_DP	-
HOST0_VSSA	AG	HOST0_VSSA	-

Module Pin	Direction	Pad Name	pinmux
HOST0_VBUS	A	HOST0_VBUS	-
HOST0_VDD33	AP	HOST0_VDD33	-

Note: **A**—Analog pad ; **AP**—Analog power; **AG**—Analog ground ; **DP**—Digital power ; **DG**— Digital ground;

2.5 Application Note

See Chapter OTG for more information.

2.5.1 Reset a port

CRU_SOFRST8_CON contains HOST0 reset signal description. Please refer to "Chapter CRU" for more details.

2.5.2 Relative GRF Registers

GRF_UOC1_CON0 ~GRF_UOC1_CON4 is HOST0 register.

Please refer to "Chapter GRF" for more details.

Chapter 3 USB2.0 Host(1)

3.1 Overview

USB HOST1 supports Non OTG Host functions and is fully compliant with USB2.0 specification, and support high-speed (480Mbps), full-speed (12Mbps), low-speed (1.5Mbps) transfer. It is optimized for point-to-point applications (no hub, direct connection to device).

The USB HOST 2.0 supports following features:

- Compliant with the USB2.0 Specification
- Operates in Non_OTG Host mode
- Operates in High-Speed, Full-Speed, Low-speed mode
- Support 16 channels in host mode
- Built-in one 1024x35 bits FIFO
- Internal DMA with no scatter/gather function
- Support dynamic FIFO adjustment

3.2 Block Diagram

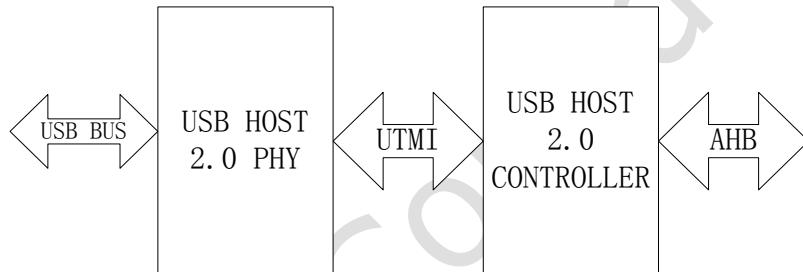


Fig. 3-1 USB HOST 2.0 Architecture

Fig.21-1 shows the architecture of USB HOST 2.0. It is broken up into two separate units: USB HOST 2.0 controller and USB HOST 2.0 PHY. The two units are interconnected with 16-bits UTMI interface.

3.3 USB Host2.0 Controller

Much the same as USB OTG with no Device Mode supported. See Chapter 19 for more information.

3.4 USB Host2.0 PHY

Much the same as USB OTG PHY with no Device Mode supported. See Chapter OTG for more information.

USB Host2.0 PHY doesn't support UART-DEBUG function.

3.5 Register Description

The Controller Registers are much the same as OTG with no Device-Mode supported. The registers of Device are not available. See Ch26 for more information.

The phy registers are in GRF. Please refer to this chapter for more detail.

3.6 Interface description

Table 3-1 USB HOST 2.0 Interface Description

Module Pin	Direction	Pad Name	pinmux
HOST1_VSSAC	AG	HOST1_VSSAC	-

Module Pin	Direction	Pad Name	pinmux
HOST1_DVSS	DG	HOST1_DVSS	-
HOST1_DVDD	DP	HOST1_DVDD	-
HOST1_VDD18	AP	HOST1_VDD18	-
HOST1_DM	A	HOST1_DM	-
HOST1_RKELVIN	A	HOST1_RKELVIN	-
HOST1_DP	A	HOST1_DP	-
HOST1_VSSA	AG	HOST1_VSSA	-
HOST1_VBUS	A	HOST1_VBUS	-
HOST1_VDD33	AP	HOST1_VDD33	-

Note: **A**—Analog pad ; **AP**—Analog power; **AG**—Analog ground ;**DP**—Digital power ;**DG**—Digital ground;

3.7 Application Note

Pls refer to Ch OTG for more information.

Chapter 4 Mobile Storage Host Controller(SDMMC & SDIO)

4.1 Overview

The Mobile Storage Host Controller is designed to support Secure Digital memory (SD- max version 3.01) with 1 bits or 4 bits data width, Multimedia Card(MMC-max version 4.51) with 1 bits or 4 bits or 8 bits data width.

The Host Controller supports following features:

- Bus Interface Features:
 - Supports AMBA AHB interface for master and slave
 - Supports internal DMA interface(IDMAC)
 - ◆ Supports 16/32-bit data transfers
 - ◆ Single-channel; single engine used for Transmit and Receive, which are mutually exclusive
 - ◆ Dual-buffer and chained descriptor linked list
 - ◆ Each descriptor can transfer up to 4KB of data in chained mode and 8KB of data in dual-buffer mode
 - ◆ Programmable burst size for optimal host bus utilization
 - Supports combined single FIFO for both transmit and receive operations
 - Supports FIFO size of 256x32
 - Supports FIFO over-run and under-run prevention by stopping card clock
- Card Interface Features:
 - Supports Secure Digital memory protocol commands
 - Supports Secure Digital I/O protocol commands
 - Supports Multimedia Card protocol commands
 - Supports Command Completion Signal and interrupts to host
 - Supports CRC generation and error detection
 - Supports programmable baud rate
 - Supports power management and power switch
 - Supports card detection and initialization
 - Supports write protection
 - Supports hardware reset
 - Supports SDIO interrupts in 1-bit and 4-bit modes
 - Supports 4-bit mode in SDIO3.0
 - Supports SDIO suspend and resume operation
 - Supports SDIO read wait
 - Supports block size of 1 to 65,535 bytes
 - Supports 1-bit, 4-bit and 8-bit SDR modes
 - Supports 4-bit DDR,8-bit DDR, as defined by SD3.0 and MMC4.41
 - Supports boot in 1-bit, 4-bit and 8-bit SDR modes
 - Supports Packed Commands, CMD21, CMD49
- Clock Interface Features:
 - Supports 0/90/180/270-degree phase shift operation for sample clock(cclk_in_sample) and drive clock(cclk_in_drv) relative to function clock(cclk_in) respectively
 - Supports phase tuning using delay line for sample clock(cclk_in_sample) and drive clock(cclk_in_drv) relative to function clock (cclk_in) respectively. The max number of delay element number is 256.

The Host Controller is instantiated for SDMMC, SDIO0, SDIO1, EMMC in RK3288. The interface difference between these instances is shown in "Interface Description".

4.2 Block Diagram

The Host Controller consists of the following main functional blocks.

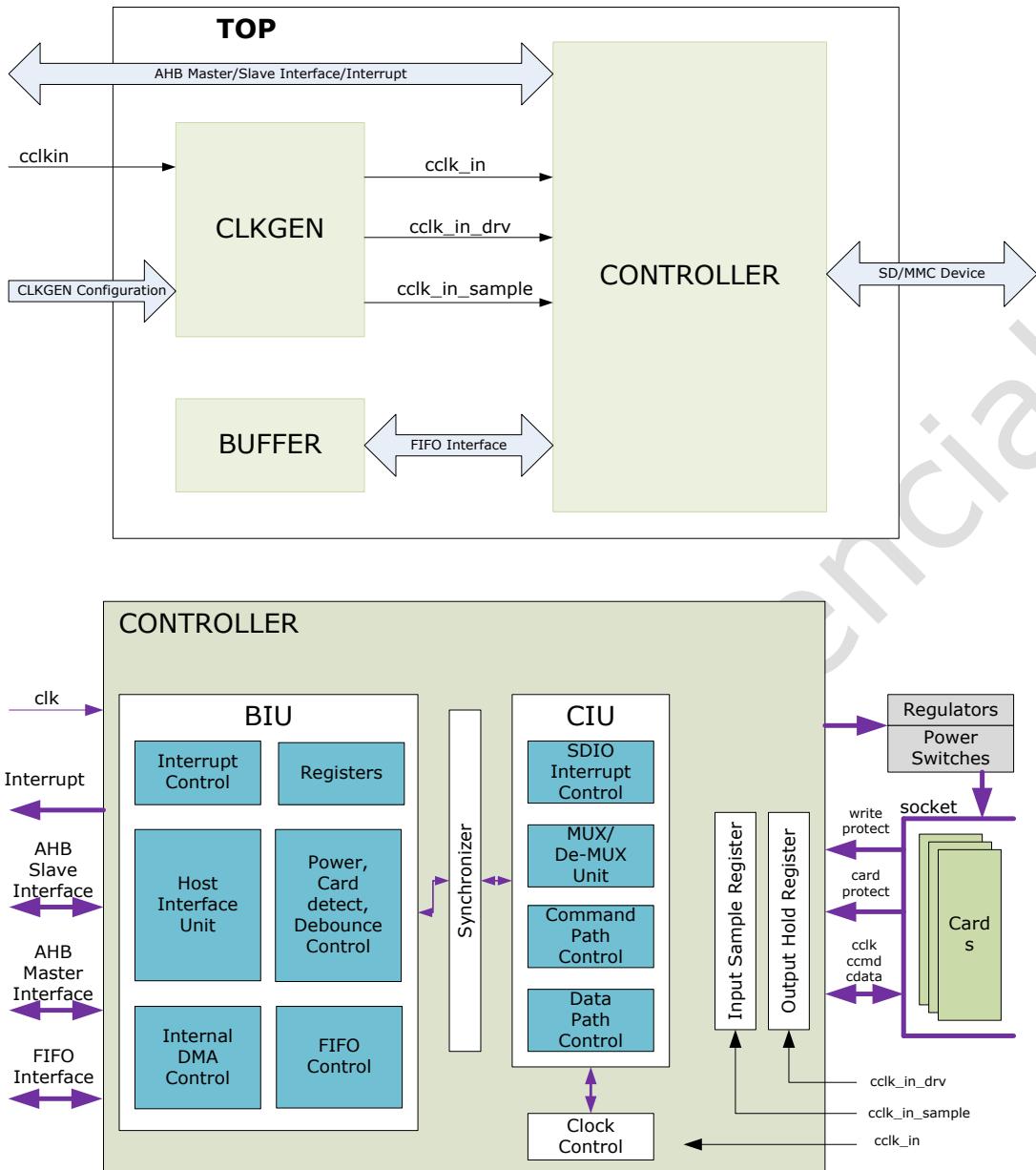


Fig. 4-1 Host Controller Block Diagram

- Clock Generate Unit(CLKGEN): generates card interface clock **cclk_in/** **cclk_sample/cclk_drv** based on **cclkin** and configuration information.
- Asynchronous dual-port memory(BUFFER): Uses a two-clock synchronous read and synchronous write dual-port RAM. One of the ports is connected to the host clock, and the second port is connected to the card clock.
- Bus Interface Unit (BIU): Provides AMBA AHB interfaces for register and data read/writes.
- Card Interface Unit (CIU): Takes care of the SD/MMC protocols and provides clock management.

4.3 Function Description

4.3.1 Bus Interface Unit

The Bus Interface Unit provides the following functions:

- Host interface
- Interrupt control
- Register access
- External FIFO access

Power control and card detection

1. Host Interface Unit

The Host Interface Unit is an AHB slave interface, which provides the interface between the SD/MMC card and the host bus. You can configure the host interface as either an AHB.

2. Register Unit

The register unit is part of the bus interface unit; it provides read and write access to the registers.

All registers reside in the Bus Interface Unit clock domain. When a command is sent to a card by setting the start_bit, which is bit[31] of the CMD register, all relevant registers needed for the CIU operation are transferred to the CIU block. During this time, the registers that are transferred from the BIU to the CIU should not be written. The software should wait for the hardware to clear the start bit before writing to these registers again. The register unit has a hardware locking feature to prevent illegal writes to registers. The lock is necessary in order to avoid metastability violations, both because the host and card clock domains are different and to prevent illegal software operations.

Once a command start is issued by setting the start_bit of the CMD register, the following registers cannot be reprogrammed until the command is accepted by the card interface unit:

- CMD – Command
- CMDARG – Command Argument
- BYTCNT – Byte Count
- BLKSIZ – Block Size
- CLKDIV – Clock Divider
- CLKENA – Clock Enable
- CLKSRC – Clock Source
- TMOUT – Timeout
- CTYPE – Card Type

The hardware resets the start_bit once the CIU accepts the command. If a host write to any of these registers is attempted during this locked time, then the write is ignored and the hardware lock error bit is set in the raw interrupt status register. Additionally, if the interrupt is enabled and not masked for a hardware lock error, then an interrupt is sent to the host.

When the Card Interface Unit is in an idle state, it typically takes the following number of clocks for the command handshake, where clk is the BIU clock and cclk_in is the CIU clock:

$3(\text{clk}) + 3(\text{cclk_in})$

Once a command is accepted, you can send another command to the CIU-which has a one-deep command queue-under the following conditions:

If the previous command was not a data transfer command, the new command is sent to the SD/MMC card once the previous command completes.

If the previous command is a data transfer command and if wait_prvdata_complete (bit[13]) of the Command register is set for the new command, the new command is sent to the SD/MMC card only when the data transfer completes.

If the wait_prvdata_complete is 0, then the new command is sent to the SD/MMC card as soon as the previous command is sent. Typically, you should use this only to stop or abort a previous data transfer or query the card status in the middle of a data transfer.

3. Interrupt Controller Unit

The interrupt controller unit generates an interrupt that depends on the controller raw interrupt status, the interrupt-mask register, and the global interrupt-enable register bit. Once an interrupt condition is detected, it sets the corresponding interrupt bit in the raw interrupt status register. The raw interrupt status bit stays on until the software clears the bit by writing a 1 to the interrupt bit; a 0 leaves the bit untouched.

The interrupt port, int, is an active-high, level-sensitive interrupt. The interrupt port is active only when any bit in the raw interrupt status register is active, the corresponding interrupt mask bit is 1, and the global interrupt enable bit is 1. The interrupt port is registered in order to avoid any combinational glitches.

The int_enable is reset to 0 on power-on, and the interrupt mask bits are set to 32'h0, which

masks all the interrupts.

Notes:

Before enabling the interrupt, it is always recommended that you write 32'hffff_ffff to the raw interrupt status register in order to clear any pending unserviced interrupts. When clearing interrupts during normal operation, ensure that you clear only the interrupt bits that you serviced.

The SDIO Interrupts, Receive FIFO Data Request (RXDR), and Transmit FIFO Data Request (TXDR) are set by level-sensitive interrupt sources. Therefore, the interrupt source should be first cleared before you can clear the interrupt bit of the Raw Interrupt register. For example, on seeing the Receive FIFO Data Request (RXDR) interrupt, the FIFO should be emptied so that the "FIFO count greater than the RX-Watermark" condition, which triggers the interrupt, becomes inactive. The rest of the interrupts are triggered by a single clock-pulse-width source.

Table 4-1 Bits in Interrupt Status Register

Bits	Interrupt	Description
24	sdio_interrupt	Interrupt from SDIO card. In MMC-Ver3.3-only mode, these bits are always 0
16	Card no-busy	If card exit busy status, the interrupt happened
15	End Bit Error (read) /Write no CRC (EBE)	Error in end-bit during read operation, or no data CRC or negative CRC received during write operation. <i>Notes: For MMC CMD19, there may be no CRC status returned by the card. Hence, EBE is set for CMD19. The application should not treat this as an error.</i>
14	Auto Command Done (ACD)	Stop/abort commands automatically sent by card unit and not initiated by host; similar to Command Done (CD) interrupt.
13	Start Bit Error (SBE)	Error in data start bit when data is read from a card. In 4-bit mode, if all data bits do not have start bit, then this error is set.
12	Hardware Locked write Error (HLE)	During hardware-lock period, write attempted to one of locked registers.
11	FIFO Underrun/ Overrun Error (FRUN)	Host tried to push data when FIFO was full, or host tried to read data when FIFO was empty. Typically this should not happen, except due to error in software. Card unit never pushes data into FIFO when FIFO is full, and pop data when FIFO is empty.
10	Data Starvation by Host Timeout (HTO)	To avoid data loss, card clock out (cclk_out) is stopped if FIFO is empty when writing to card, or FIFO is full when reading from card. Whenever card clock is stopped to avoid data loss, data-starvation timeout counter is started with data-timeout value. This interrupt is set if host does not fill data into FIFO during write to card, or does not read from FIFO during read from card before timeout period. Even after timeout, card clock stays in stopped state, with CIU state machines waiting. It is responsibility of host to push or pop data into FIFO upon interrupt, which automatically restarts cclk_out and card state machines. Even if host wants to send stop/abort command, it still needs to ensure it has to push or pop FIFO so that clock starts in order for stop/abort command to send on cmd signal along with data that is sent or received on data line.
9	Data Read Timeout (DRTO)	Data timeout occurred. Data Transfer Over (DTO) also set if data timeout occurs.
8	Response Timeout (RTO)	Response timeout occurred. Command Done (CD) also set if response timeout occurs. If command involves data transfer and when response times out, no data transfer is attempted by Host Controller.
7	Data CRC Error (DCRC)	Received Data CRC does not match with

Bits	Interrupt	Description
		locally-generated CRC in CIU.
6	Response CRC Error (RCRC)	Response CRC does not match with locally-generated CRC in CIU.
5	Receive FIFO Data Request (RXDR)	Interrupt set during read operation from card when FIFO level is greater than Receive-Threshold level.
4	Transmit FIFO Data Request (TXDR)	Interrupt set during write operation to card when FIFO level reaches less than or equal to Transmit-Threshold level.
3	Data Transfer Over (DTO)	Data transfer completed, even if there is Start Bit Error or CRC error. This bit is also set when "read data-timeout" occurs. <i>Notes: DTO bit is set at the end of the last data block, even if the device asserts MMC busy after the last data block.</i>
2	Command Done(CD)	Command sent to card and got response from card, even if Response Error or CRC error occurs. Also set when response timeout occurs
1	Response Error (RE)	Error in received response set if one of following occurs: Transmission bit != 0 Command index mismatch End-bit != 1
0	Card-Detect (CDT)	When card inserted or removed, this interrupt occurs. Software should read card-detect register (CDETECT, 0x50) to determine current card status.

4. FIFO Controller Unit

The FIFO controller interfaces the external FIFO to the host interface and the card controller unit. When FIFO overrun and under-run conditions occur, the card clock stops in order to avoid data loss.

The FIFO uses a two-clock synchronous read and synchronous write dual-port RAM. One of the ports is connected to the host clock, clk, and the second port is connected to the card clock, cclk_in.

Notes: The FIFO controller does not support simultaneous read/write access from the same port. For debugging purposes, the software may try to write into the FIFO and read back the data; results are indeterminate, since the design does not support read/write access from the same port.

5. Power Control and Card Detection Unit

The register unit has registers that control the power. Power to each card can be selectively turned on or off.

The card detection unit looks for any changes in the card-detect signals for card insertion or card removal. It filters out the debounces associated with mechanical insertion or removal, and generates one interrupt to the host. You can program the debounce filter value.

On power-on, the controller should read in the card_detect port and store the value in the memory. Upon receiving a card-detect interrupt, it should again read the card_detect port and XOR with the previous card-detect status to find out which card has interrupted. If more than one card is simultaneously removed or inserted, there is only one card-detect interrupt; the XOR value indicates which cards have been disturbed. The memory should be updated with the new card-detect value.

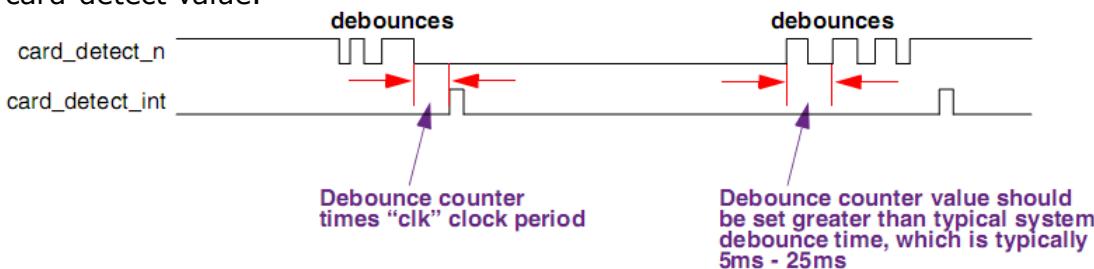


Fig. 4-2 SD/MMC Card-Detect Signal

4.3.2 Card Interface Unit

The Card Interface Unit (CIU) interfaces with the Bus Interface Unit (BIU) and the devices. The host writes command parameters to the BIU control registers, and these parameters are then passed to the CIU. Depending on control register values, the CIU generates SD/MMC command and data traffic on a selected card bus according to SD/MMC protocol. The Host Controller accordingly controls the command and data path.

The following software restrictions should be met for proper CIU operation:

- Only one data transfer command can be issued at a time.

- During an open-ended card write operation, if the card clock is stopped because the FIFO is empty, the software must first fill the data into the FIFO and start the card clock. It can then issue only a stop/abort command to the card.

- When issuing card reset commands (CMD0, CMD15 or CMD52_reset) while a card data transfer is in progress, the software must set the stop_abort_cmd bit in the Command register so that the Host Controller can stop the data transfer after issuing the card reset command.

- When the data end bit error is set in the RINTSTS register, the Host Controller does not guarantee SDIO interrupts. The software should ignore the SDIO interrupts and issue the stop/abort command to the card, so that the card stops sending the read data.

- If the card clock is stopped because the FIFO is full during a card read, the software should read at least two FIFO locations to start the card clock.

The CIU block consists of the following primary functional blocks:

- Command path

- Data path

- SDIO interrupt control

- Clock control

- Mux/demux unit

Command Path

The command path performs the following functions:

- Loads clock parameters

- Loads card command parameters

- Sends commands to card bus (ccmd_out line)

- Receives responses from card bus (ccmd_in line)

- Sends responses to BIU

- Drives the P-bit on command line

A new command is issued to the Host Controller by programming the BIU registers and setting the start_cmd bit in the Command register. The BIU asserts start_cmd, which indicates that a new command is issued to the SD/MMC device. The command path loads this new command (command, command argument, timeout) and sends acknowledge to the BIU by asserting cmd_taken.

Once the new command is loaded, the command path state machine sends a command to the device bus-including the internally generated CRC7-and receives a response, if any. The state machine then sends the received response and signals to the BIU that the command is done, and then waits for eight clocks before loading a new command.

Load Command Parameters

One of the following commands or responses is loaded in the command path:

- New command from BIU – When start_cmd is asserted, then the start_cmd bit is set in the Command register.

- Internally-generated auto-stop command – When the data path ends, the stop command request is loaded.

- IRQ response with RCA 0x000 – When the command path is waiting for an IRQ response from the MMC card and a “send irq response” request is signaled by the BIU, then the send_irq_response bit is set in the control register.

Loading a new command from the BIU in the command path depends on the following Command register bit settings:

`update_clock_registers_only` – If this bit is set in the Command register, the command path updates only the clock enable, clock divider, and clock source registers. If this bit is not set, the command path loads the command, command argument, and timeout registers; it then starts processing the new command.

`wait_prvdata_complete` – If this bit is set, the command path loads the new command under one of the following conditions:

Immediately, if the data path is free (that is, there is no data transfer in progress), or if an open-ended data transfer is in progress (`byte_count = 0`).

After completion of the current data transfer, if a predefined data transfer is in progress.

Send Command and Receive Response

Once a new command is loaded in the command path, `update_clock_registers_only` bit is unset – the command path state machine sends out a command on the device bus; the command path state machine is illustrated in following figure.

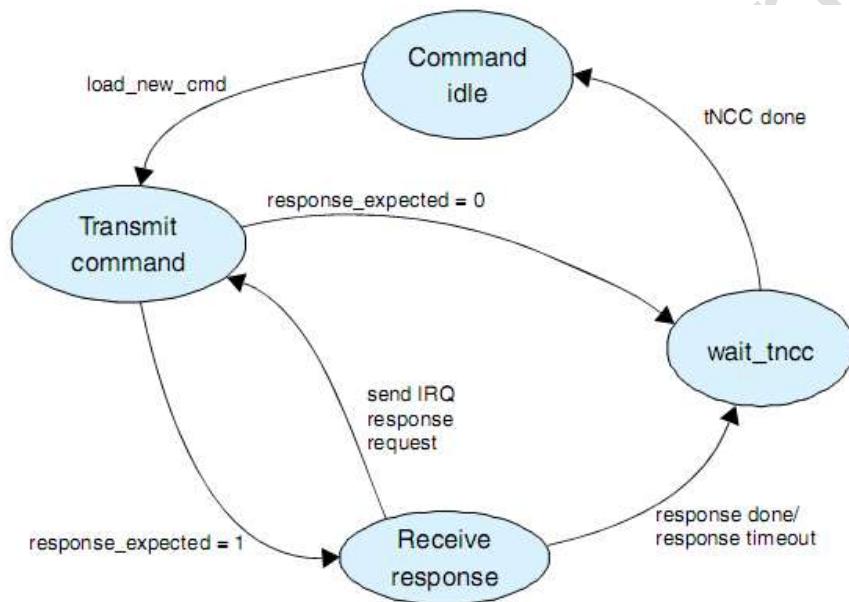


Fig. 4-3 Host Controller Command Path State Machine

The command path state machine performs the following functions, according to Command register bit values:

`send_initialization` – Initialization sequence of 80 clocks is sent before sending the command.

`response_expected` – Response is expected for the command. After the command is sent out, the command path state machine receives a 48-bit or 136-bit response and sends it to the BIU. If the start bit of the card response is not received within the number of clocks programmed in the timeout register, then the response timeout and command done bit is set in the Raw Interrupt Status register as a signal to the BIU. If the response-expected bit is not set, the command path sends out a command and signals a response done to the BIU; that is, the command done bit is set in the Raw Interrupt Status register.

`response_length` – If this bit is set, a 136-bit response is received; if it is not set, a 48-bit response is received.

`check_response_crc` – If this bit is set, the command path compares CRC7 received in the response with the internally-generated CRC7. If the two do not match, the response CRC error is signaled to the BIU; that is, the response CRC error bit is set in the Raw Interrupt Status register.

Send Response to BIU

If the response_expected bit is set in the Command register, the received response is sent to the BIU. The Response0 register is updated for a short response, and the Response3, Response2, Response1, and Response0 registers are updated on a long response, after which the Command Done bit is set. If the response is for an auto_stop command sent by the CIU, the response is saved in the Response1 register, after which the Auto Command Done bit is set. Additionally, the command path checks for the following:

Transmission bit = 0

Command index matches command index of the sent command

End bit = 1 in received card response

The command index is not checked for a 136-bit response or if the check_response_crc bit is unset. For a 136-bit response and reserved CRC 48-bit responses, the command index is reserved—that is, 111111.

Polling Command Completion Signal

The device generates the Command Completion Signal in order to notify the host controller of the normal command completion or command termination.

Command Completion Signal Detection and Interrupt to Host Processor

If the ccs_expected bit is set in the Command register, the Command Completion Signal (CCS) from the device is indicated by setting the Data Transfer Over (DTO) bit in the RINTSTS register. The Host Controller generates a Data Transfer Over (DTO) interrupt if this interrupt is not masked.

Command Completion Signal Timeout

If the command expects a CCS from the device—if the ccs_expected bit is set in the Command register—the command state machine waits for the CCS and remains in a wait_CCS state. If the device fails to send out the CCS, the host software should implement a timeout mechanism to free the command and data path. The host controller does not implement a hardware timer; it is the responsibility of the host software to maintain a software timer.

In the event of a CCS timeout, the host should issue a CCSD by setting the send_ccsd bit in the CTRL register. The host controller command state machine sends the CCSD to the device and exits to an idle state. After sending the CCSD, the host should also send a CMD12 to the device in order to abort the outstanding command.

Send Command Completion Signal Disable

If the send_ccsd bit is set in the CTRL register, the host sends a Command Completion Signal Disable (CCSD) pattern on the CMD line. The host can send the CCSD while waiting for the CCS or after a CCS timeout happens.

After sending the CCSD pattern, the host sets the Command Done (CD) bit in RINTSTS and also generates an interrupt to the host if the Command Done interrupt is not masked.

Data Path

The data path block pops the data FIFO and transmits data on cdata_out during a write data transfer, or it receives data on cdata_in and pushes it into the FIFO during a read data transfer. The data path loads new data parameters—that is, data expected, read/write data transfer, stream/block transfer, block size, byte count, card type, timeout registers—whenever a data transfer command is not in progress.

If the data_expected bit is set in the Command register, the new command is a data transfer command and the data path starts one of the following:

Transmit data if the read/write bit = 1

Data receive if read/write bit = 0

Data Transmit

The data transmit state machine, illustrated in following figure, starts data transmission two clocks after a response for the data write command is received; this occurs even if the command path detects a response error or response CRC error. If a response is not received from the card because of a response timeout, data is not transmitted. Depending upon the

value of the transfer_mode bit in the Command register, the data transmit state machine puts data on the card data bus in a stream or in block(s).

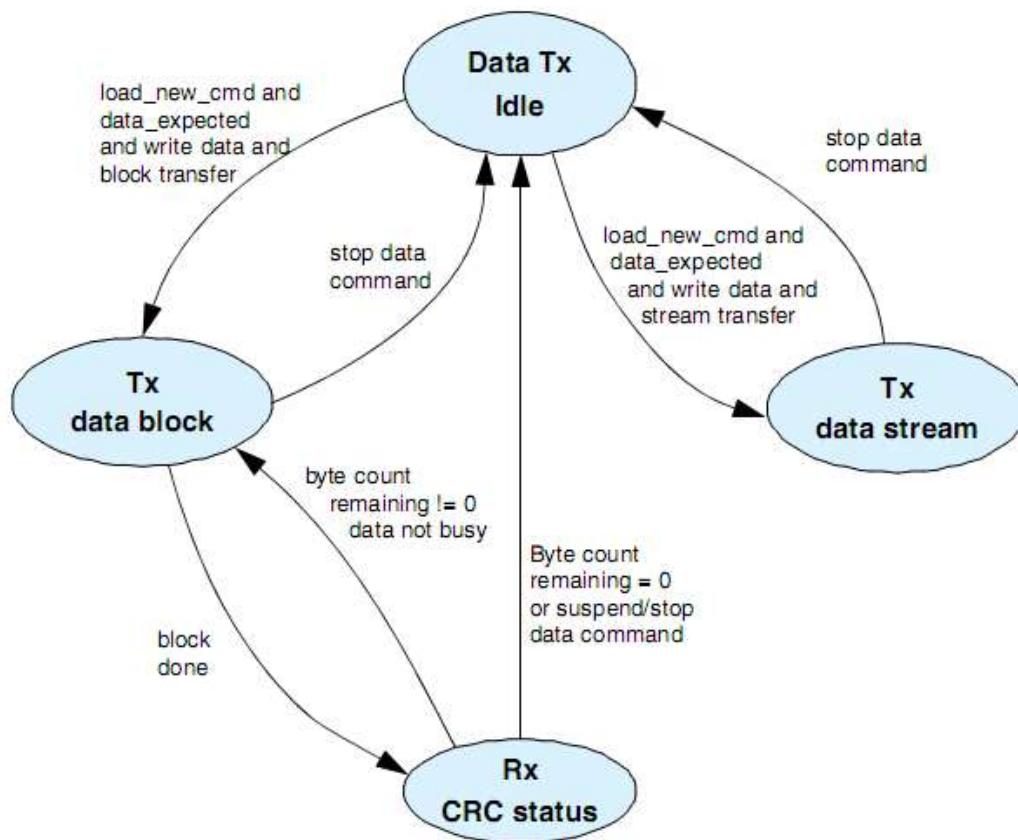


Fig. 4-4 Host Controller Data Transmit State Machine

Stream Data Transmit

If the transfer_mode bit in the Command register is set to 1, it is a stream-write data transfer. The data path pops the FIFO from the BIU and transmits in a stream to the card data bus. If the FIFO becomes empty, the card clock is stopped and restarted once data is available in the FIFO. If the byte_count register is programmed to 0, it is an open-ended stream-write data transfer. During this data transfer, the data path continuously transmits data in a stream until the host software issues a stop command. A stream data transfer is terminated when the end bit of the stop command and end bit of the data match over two clocks.

If the byte_count register is programmed with a non-zero value and the send_auto_stop bit is set in the Command register, the stop command is internally generated and loaded in the command path when the end bit of the stop command occurs after the last byte of the stream write transfer matches.

This data transfer can also terminate if the host issues a stop command before all the data bytes are transferred to the card bus.

Single Block Data

If the transfer_mode bit in the Command register is set to 0 and the byte_count register value is equal to the value of the block_size register, a single-block write-data transfer occurs. The data transmit state machine sends data in a single block, where the number of bytes equals the block size, including the internally-generated CRC16.

If the CTYPE register bit for the selected card – indicated by the card_num value in the Command register – is set for a 1-bit, 4-bit, or 8-bit data transfer, the data is transmitted on 1, 4, or 8 data lines, respectively, and CRC16 is separately generated and transmitted for 1, 4, or 8 data lines, respectively.

After a single data block is transmitted, the data transmit state machine receives the CRC status from the card and signals a data transfer to the BIU; this happens when the data-transfer-over bit is set in the RINTSTS register.

If a negative CRC status is received from the card, the data path signals a data CRC error to the BIU by setting the data CRC error bit in the RINTSTS register.

Additionally, if the start bit of the CRC status is not received by two clocks after the end of the data block, a CRC status start bit error is signaled to the BIU by setting the write-no-CRC bit in the RINTSTS register.

Multiple Block Data

A multiple-block write-data transfer occurs if the transfer_mode bit in the Command register is set to 0 and the value in the byte_count register is not equal to the value of the block_size register. The data transmit state machine sends data in blocks, where the number of bytes in a block equals the block size, including the internally-generated CRC16.

If the CTYPE register bit for the selected card – indicated by the card_num value in the Command register – is set to 1-bit, 4-bit, or 8-bit data transfer, the data is transmitted on 1, 4, or 8 data lines, respectively, and CRC16 is separately generated and transmitted on 1, 4, or 8 data lines, respectively.

After one data block is transmitted, the data transmit state machine receives the CRC status from the card. If the remaining byte_count becomes 0, the data path signals to the BIU that the data transfer is done; this happens when the data-transfer-over bit is set in the RINTSTS register.

If the remaining data bytes are greater than 0, the data path state machine starts to transmit another data block.

If a negative CRC status is received from the card, the data path signals a data CRC error to the BIU by setting the data CRC error bit in the RINTSTS register, and continues further data transmission until all the bytes are transmitted.

Additionally, if the CRC status start bit is not received by two clocks after the end of a data block, a CRC status start bit error is signaled to the BIU by setting the write-no-CRC bit in the RINTSTS register; further data transfer is terminated.

If the send_auto_stop bit is set in the Command register, the stop command is internally generated during the transfer of the last data block, where no extra bytes are transferred to the card. The end bit of the stop command may not exactly match the end bit of the CRC status in the last data block.

If the block size is less than 4, 16, or 32 for card data widths of 1 bit, 4 bits, or 8 bits, respectively, the data transmit state machine terminates the data transfer when all the data is transferred, at which time the internally generated stop command is loaded in the command path.

If the byte_count is 0 – the block size must be greater than 0 – it is an open-ended block transfer. The data transmit state machine for this type of data transfer continues the block-write data transfer until the host software issues a stop or abort command.

Data Receive

The data-receive state machine, illustrated in following figure, receives data two clock cycles after the end bit of a data read command, even if the command path detects a response error or response CRC error. If a response is not received from the card because a response timeout occurs, the BIU does not receive a signal that the data transfer is complete; this happens if the command sent by the Host Controller is an illegal operation for the card, which keeps the card from starting a read data transfer.

If data is not received before the data timeout, the data path signals a data timeout to the BIU and an end to the data transfer done. Based on the value of the transfer_mode bit in the Command register, the data-receive state machine gets data from the card data bus in a stream or block(s).

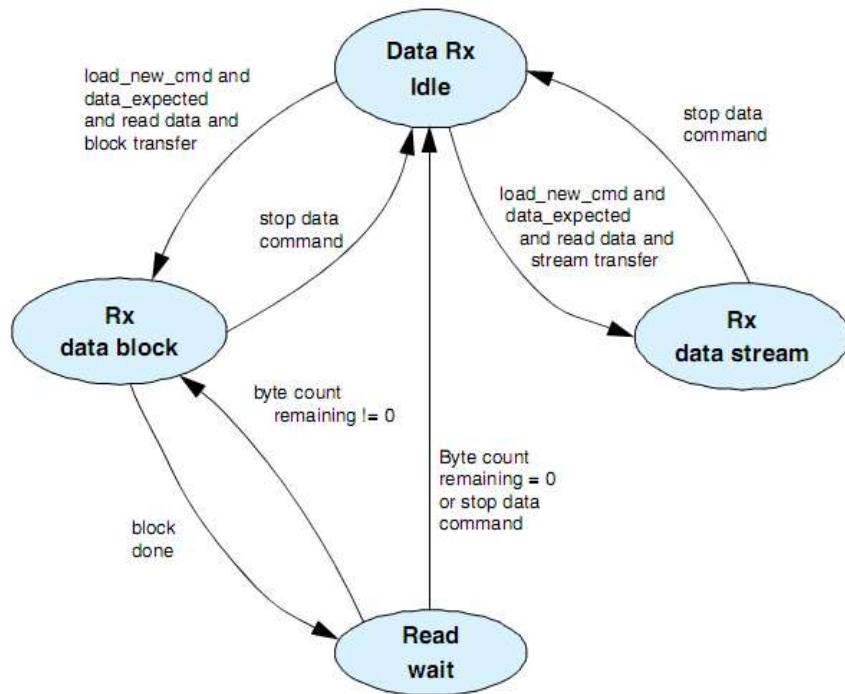


Fig. 4-5 Host Controller Data Receive State Machine

Stream Data Read

A stream-read data transfer occurs if the transfer_mode bit in the Command register equals 1, at which time the data path receives data from the card and pushes it to the FIFO. If the FIFO becomes full, the card clock stops and restarts once the FIFO is no longer full.

An open-ended stream-read data transfer occurs if the byte_count register equals 0. During this type of data transfer, the data path continuously receives data in a stream until the host software issues a stop command. A stream data transfer terminates two clock cycles after the end bit of the stop command.

If the byte_count register contains a non-zero value and the send_auto_stop bit is set in the Command register, a stop command is internally generated and loaded into the command path, where the end bit of the stop command occurs after the last byte of the stream data transfer is received. This data transfer can terminate if the host issues a stop or abort command before all the data bytes are received from the card.

Single-Block Data Read

A single-block read-data transfer occurs if the transfer_mode bit in the Command register is set to 0 and the value of the byte_count register is equal to the value of the block_size register. When a start bit is received before the data times out, data bytes equal to the block size and CRC16 are received and checked with the internally-generated CRC16.

If the CTYPE register bit for the selected card – indicated by the card_num value in the Command register – is set to a 1-bit, 4-bit, or 8-bit data transfer, data is received from 1, 4, or 8 data lines, respectively, and CRC16 is separately generated and checked for 1, 4, or 8 data lines, respectively. If there is a CRC16 mismatch, the data path signals a data CRC error to the BIU. If the received end bit is not 1, the BIU receives an end-bit error.

Multiple-Block Data Read

If the transfer_mode bit in the Command register is set to 0 and the value of the byte_count register is not equal to the value of the block_size register, it is a multiple-block read-data transfer. The data-receive state machine receives data in blocks, where the number of bytes in a block is equal to the block size, including the internally-generated CRC16.

If the CTYPE register bit for the selected card – indicated by the card_num value in the Command register – is set to a 1-bit, 4-bit, or 8-bit data transfer, data is received from 1, 4, or 8 data lines, respectively, and CRC16 is separately generated and checked for 1, 4, or 8 data lines, respectively.

After a data block is received, if the remaining byte_count becomes 0, the data path signals a data transfer to the BIU.

If the remaining data bytes are greater than 0, the data path state machine causes another data block to be received. If CRC16 of a received data block does not match the internally-generated CRC16, a data CRC error to the BIU and data reception continue further data transmission until all bytes are transmitted.

Additionally, if the end of a received data block is not 1, data on the data path signals terminate the bit error to the CIU and the data-receive state machine terminates data reception, waits for data timeout, and signals to the BIU that the data transfer is complete.

If the send_auto_stop bit is set in the Command register, the stop command is internally generated when the last data block is transferred, where no extra bytes are transferred from the card; the end bit of the stop command may not exactly match the end bit of the last data block.

If the requested block size for data transfers to cards is less than 4, 16, or 32 bytes for 1-bit, 4-bit, or 8-bit data transfer modes, respectively, the data-transmit state machine terminates the data transfer when all data is transferred, at which point the internally-generated stop command is loaded in the command path. Data received from the card after that are then ignored by the data path.

If the byte_count is 0—the block size must be greater than 0—it is an open-ended block transfer. For this type of data transfer, the data-receive state machine continues the block-read data transfer until the host software issues a stop or abort command.

Auto-Stop

The Host Controller internally generates a stop command and is loaded in the command path when the send_auto_stop bit is set in the Command register.

The software should set the send_auto_stop bit according to details listed in following table.

Table 4-2 Auto-Stop Generation

Card type	Transfer type	Byte Count	send_auto_stop bit set	Comments
MMC	Stream read	0	No	Open-ended stream
MMC	Stream read	>0	Yes	Auto-stop after all bytes transfer
MMC	Stream write	0	No	Open-ended stream
MMC	Stream write	>0	Yes	Auto-stop after all bytes transfer
MMC	Single-block read	>0	No	Byte count =0 is illegal
MMC	Single-block write	>0	No	Byte count =0 is illegal
MMC	Multiple-block read	0	No	Open-ended multiple block
MMC	Multiple-block read	>0	Yes ^①	Pre-defined multiple block
MMC	Multiple-block write	0	No	Open-ended multiple block
MMC	Multiple-block write	>0	Yes ^①	Pre-defined multiple block
SDMEM	Single-block read	>0	No	Byte count =0 is illegal
SDMEM	Single-block write	>0	No	Byte count =0 illegal
SDMEM	Multiple-block read	0	No	Open-ended multiple block
SDMEM	Multiple-block read	>0	Yes	Auto-stop after all bytes transfer
SDMEM	Multiple-block write	0	No	Open-ended multiple block
SDMEM	Multiple-block write	>0	Yes	Auto-stop after all bytes transfer
SDIO	Single-block read	>0	No	Byte count =0 is illegal
SDIO	Single-block write	>0	No	Byte count =0 illegal
SDIO	Multiple-block read	0	No	Open-ended multiple block
SDIO	Multiple-block read	>0	No	Pre-defined multiple block
SDIO	Multiple-block write	0	No	Open-ended multiple block

Card type	Transfer type	Byte Count	send_auto_stop bit set	Comments
SDIO	Multiple-block write	>0	No	Pre-defined multiple block

① :The condition under which the transfer mode is set to block transfer and byte_count is equal to block size is treated as a single-block data transfer command for both MMC and SD cards. If byte_count = n*block_size (n = 2, 3, ...), the condition is treated as a predefined multiple-block data transfer command. In the case of an MMC card, the host software can perform a predefined data transfer in two ways: 1) Issue the CMD23 command before issuing CMD18/CMD25 commands to the card – in this case, issue MD18/CMD25 commands without setting the send_auto_stop bit. 2) Issue CMD18/CMD25 commands without issuing CMD23 command to the card, with the send_auto_stop bit set. In this case, the multiple-block data transfer is terminated by an internally-generated auto-stop command after the programmed byte count.

The following list conditions for the auto-stop command.

Stream read for MMC card with byte count greater than 0 – The Host Controller generates an internal stop command and loads it into the command path so that the end bit of the stop command is sent out when the last byte of data is read from the card and no extra data byte is received. If the byte count is less than 6 (48 bits), a few extra data bytes are received from the card before the end bit of the stop command is sent.

Stream write for MMC card with byte count greater than 0 - The Host Controller generates an internal stop command and loads it into the command path so that the end bit of the stop command is sent when the last byte of data is transmitted on the card bus and no extra data byte is transmitted. If the byte count is less than 6 (48 bits), the data path transmits the data last in order to meet the above condition.

Multiple-block read memory for SD card with byte count greater than 0 – If the block size is less than 4 (single-bit data bus), 16 (4-bit data bus), or 32 (8-bit data bus), the auto-stop command is loaded in the command path after all the bytes are read. Otherwise, the top command is loaded in the command path so that the end bit of the stop command is sent after the last data block is received.

Multiple-block write memory for SD card with byte count greater than 0 – If the block size is less than 3 (single-bit data bus), 12 (4-bit data bus), or 24 (8-bit data bus), the auto-stop command is loaded in the command path after all data blocks are transmitted. Otherwise, the stop command is loaded in the command path so that the end bit of the stop command is sent after the end bit of the CRC status is received.

Precaution for host software during auto-stop – Whenever an auto-stop command is issued, the host software should not issue a new command to the SD/MMC device until the auto-stop is sent by the Host Controller and the data transfer is complete. If the host issues a new command during a data transfer with the auto-stop in progress, an auto-stop command may be sent after the new command is sent and its response is received; this can delay sending the stop command, which transfers extra data bytes. For a stream write, extra data bytes are erroneous data that can corrupt the card data. If the host wants to terminate the data transfer before the data transfer is complete, it can issue a stop or abort command, in which case the Host Controller does not generate an auto-stop command.

Non-Data Transfer Commands that Use Data Path

Some non-data transfer commands (non-read/write commands) also use the data path. Following table lists the commands and register programming requirements for them.

Table 4-3 Non-data Transfer Commands and Requirements

	CMD27	CMD30	CMD42	ACMD13	ACMD22	ACMD51
Command register programming						
cmd_index	6'h1B	6'h1E	6'h2A	6'h0D	6'h16	6'h33
response_expect	1	1	1	1	1	1
rResponse_length	0	0	0	0	0	0
check_response_crc	1	1	1	1	1	1
data_expected	1	1	1	1	1	1
read/write	1	0	1	0	0	0

transfer_mode	0	0	0	0	0	0
send_auto_stop	0	0	0	0	0	0
wait_prevdata_complete	0	0	0	0	0	0
stop_abort_cmd	0	0	0	0	0	0

Command Argument register programming

	stuff bits	32-bit writeprotect dataaddress	stuff bits	stuff bits	stuff bits	stuff bits
--	------------	---------------------------------------	------------	------------	------------	------------

Block Size register programming

	16	4	Num_bytes ^①	64	4	8
--	----	---	------------------------	----	---	---

Byte Count register programming

	16	4	Num_bytes ^①	64	4	8
--	----	---	------------------------	----	---	---

①: Num_bytes = No. of bytes specified as per the lock card data structure (Refer to the SD specification and the MMC specification)

SDIO Interrupt Control

Interrupts for SD cards are reported to the BIU by asserting an interrupt signal for two clock cycles. SDIO cards signal an interrupt by asserting cdata_in low during the interrupt period; an interrupt period for the selected card is determined by the interrupt control state machine. An interrupt period is always valid for non-active or non-selected cards, and 1-bit data mode for the selected card. An interrupt period for a wide-bus active or selected card is valid for the following conditions:

- Card is idle

- Non-data transfer command in progress

- Third clock after end bit of data block between two data blocks

- From two clocks after end bit of last data until end bit of next data transfer command

Bear in mind that, in the following situations, the controller does not sample the SDIO interrupt of the selected card when the card data width is 4 bits. Since the SDIO interrupt is level-triggered, it is sampled in a further interrupt period and the host does not lose any SDIO interrupt from the card.

Read/Write Resume – The CIU treats the resume command as a normal data transfer command. SDIO interrupts during the resume command are handled similarly to other data commands. According to the SDIO specification, for the normal data command the interrupt period ends after the command end bit of the data command; for the resume command, it ends after the response end bit. In the case of the resume command, the Controller stops the interrupt sampling period after the resume command end bit, instead of stopping after the response end bit of the resume command.

Suspend during read transfer – If the read data transfer is suspended by the host, the host sets the abort_read_data bit in the controller to reset the data state machine. In the CIU, the SDIO interrupts are handled such that the interrupt sampling starts after the abort_read_data bit is set by the host. In this case the controller does not sample SDIO interrupts between the period from response of the suspend command to setting the abort_read_data bit, and starts sampling after setting the abort_read_data bit.

Clock Control

The clock control block provides different clock frequencies required for SD/MMC cards. The cclk_in signal is the source clock ($cclk_in \geq$ card max operating frequency) for clock divider of the clock control block. This source clock (cclk_in) is used to generate different card clock frequencies (cclk_out). The card clock can have different clock frequencies, since the card can be a low-speed card or a full-speed card. The Host Controller provides one clock signal (cclk_out).

The clock frequency of a card depends on the following clock control registers:

Clock Divider register – Internal clock dividers are used to generate different clock frequencies required for card. The division factor for each clock divider can be programmed by writing to the Clock Divider register. The clock divider is an 8-bit value that provides a

clock division factor from 1 to 510; a value of 0 represents a clock-divider bypass, a value of 1 represents a divide by 2, a value of 2 represents a divide by 4, and so on.

Clock Control register – cclk_out can be enabled or disabled for each card under the following conditions:

clk_enable – cclk_out for a card is enabled if the clk_enable bit for a card in the Clock Control register is programmed (set to 1) or disabled (set to 0).

Low-power mode – Low-power mode of a card can be enabled by setting the low-power mode bit of the Clock Control register to 1. If low-power mode is enabled to save card power, the cclk_out is disabled when the card is idle for at least 8 card clock cycles. It is enabled when a new command is loaded and the command path goes to a non-idle state.

Additionally, cclk_out is disabled when an internal FIFO is full – card read (no more data can be received from card) – or when the FIFO is empty – card write (no data is available for transmission). This helps to avoid FIFO overrun and underrun conditions. It is used by the command and data path to qualify cclk_in for driving outputs and sampling inputs at the programmed clock frequency for the selected card, according to the Clock Divider and Clock Source register values.

Under the following conditions, the card clock is stopped or disabled, along with the active clk_en, for the selected card:

Clock can be disabled by writing to Clock Enable register (clk_en bit = 1).

If low-power mode is selected and card is idle, or not selected for 8 clocks.

FIFO is full and data path cannot accept more data from the card and data transfer is incomplete –to avoid FIFO overrun.

FIFO is empty and data path cannot transmit more data to the card and data transfer is incomplete – to avoid FIFO underrun.

Error Detection

Response

Response timeout – Response expected with response start bit is not received within programmed number of clocks in timeout register.

Response CRC error – Response is expected and check response CRC requested; response CRC7 does not match with the internally-generated CRC7.

Response error – Response transmission bit is not 0, command index does not match with the command index of the send command, or response end bit is not 1.

Data transmit

No CRC status – During a write data transfer, if the CRC status start bit is not received two clocks after the end bit of the data block is sent out, the data path does the following:

Signals no CRC status error to the BIU

Terminates further data transfer

Signals data transfer done to the BIU

Negative CRC – If the CRC status received after the write data block is negative (that is, not 010), a data CRC error is signaled to the BIU and further data transfer is continued.

Data starvation due to empty FIFO – If the FIFO becomes empty during a write data transmission, or if the card clock is stopped and the FIFO remains empty for data timeout clocks, then a data-starvation error is signaled to the BIU and the data path continues to wait for data in the FIFO.

Data receive

Data timeout – During a read-data transfer, if the data start bit is not received before the number of clocks that were programmed in the timeout register, the data path does the following:

Signals data-timeout error to the BIU

Terminates further data transfer

Signals data transfer done to BIU

Data start bit error – During a 4-bit or 8-bit read-data transfer, if the all-bit data line does not have a start bit, the data path signals a data start bit error to the BIU and waits for a data timeout, after which it signals that the data transfer is done.

Data CRC error – During a read-data-block transfer, if the CRC16 received does not match with the internally generated CRC16, the data path signals a data CRC error to the BIU and

continues further data transfer.

Data end-bit error – During a read-data transfer, if the end bit of the received data is not 1, the data path signals an end-bit error to the BIU, terminates further data transfer, and signals to the BIU that the data transfer is done.

Data starvation due to FIFO full – During a read data transmission and when the FIFO becomes full, the card clock is stopped. If the FIFO remains full for data timeout clocks, a data starvation error is signaled to the BIU (Data Starvation by Host Timeout bit is set in RINTSTS Register) and the data path continues to wait for the FIFO to start to empty.

4.3.3 Internal Direct Memory Access Controller (IDMAC)

The Internal Direct Memory Access Controller (IDMAC) has a Control and Status Register (CSR) and a single Transmit/Receive engine, which transfers data from host memory to the device port and vice versa. The controller utilizes a descriptor to efficiently move data from source to destination with minimal Host CPU intervention. You can program the controller to interrupt the Host CPU in situations such as data Transmit and Receive transfer completion from the card, as well as other normal or error conditions.

The IDMAC and the Host driver communicate through a single data structure. CSR addresses 0x80 to 0x98 are reserved for host programming.

The IDMAC transfers the data received from the card to the Data Buffer in the Host memory, and it transfers Transmit data from the Data Buffer in the Host memory to the FIFO. Descriptors that reside in the Host memory act as pointers to these buffers.

A data buffer resides in physical memory space of the Host and consists of complete data or partial data. Buffers contain only data, while buffer status is maintained in the descriptor. Data chaining refers to data that spans multiple data buffers. However, a single descriptor cannot span multiple data.

A single descriptor is used for both reception and transmission. The base address of the list is written into Descriptor List Base Address Register (DBADDR @0x88). A descriptor list is forward linked. The Last Descriptor can point back to the first entry in order to create a ring structure. The descriptor list resides in the physical memory address space of the Host. Each descriptor can point to a maximum of two data buffers.

1. IDMAC CSR Access

When an IDMAC is introduced, an additional CSR space resides in the IDMAC that controls the IDMAC functionality. The host accesses the new CSR space in addition to the existing control register set in the BIU. The IDMAC CSR primarily contains descriptor information. For a write operation to the CSR, the respective CSR logic of the IDMAC and BIU decodes the address before accepting. For a read operation from the CSR, the appropriate CSR read path is enabled. You can enable or disable the IDMAC operation by programming bit[25] in the CTRL register of the BIU. This allows the data transfer by accessing the slave interface on the AMBA bus if the IDMAC is present but disabled. When IDMAC is enabled, the FIFO cannot be accessed through the slave interface.

2. Descriptors

- Descriptor structures

The IDMAC uses these types of descriptor structures:

- Dual-Buffer Structure – The distance between two descriptors is determined by the Skip Length value programmed in the Descriptor Skip Length (DSL) field of the Bus Mode Register (BMOD @0x80).

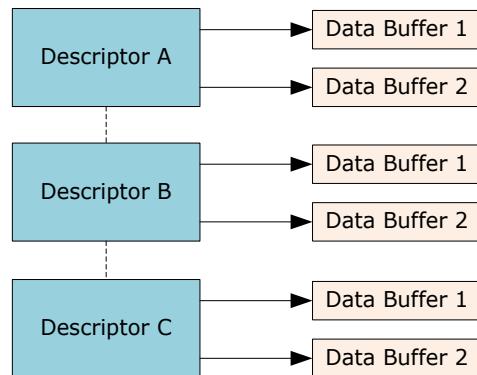


Fig. 4-6 Dual-Buffer Descriptor Structure

- Chain Structure – Each descriptor points to a unique buffer and the next descriptor.

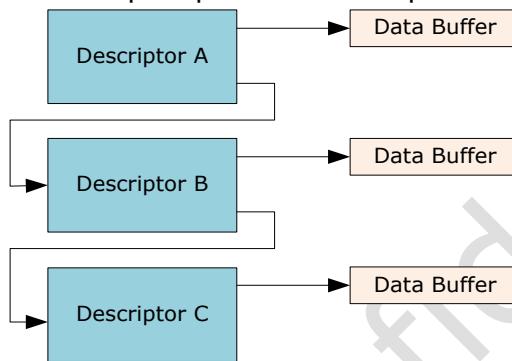


Fig. 4-7 Chain Descriptor Structure

- Descriptor formats

Following figure illustrates the internal formats of a descriptor. The descriptor addresses must be aligned to the bus width used for 32-bit AHB data buses. Each descriptor contains 16 bytes of control and status information. DES0 is a notation used to denote the [31:0] bits, DES1 to denote [63:32] bits, DES2 to denote [95:64] bits, DES3 to denote [127:96] bits.

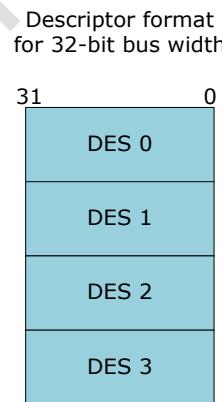


Fig. 4-8 Descriptor Formats for 32-bit AHB Address Bus Width

- The DES0 element in the IDMAC contains control and status information.

Table 4-4 Bits in IDMAC DES0 Element

Bits	Name	Description
31	OWN	When set, this bit indicates that the descriptor is owned by the IDMAC. When this bit is reset, it indicates that the descriptor is owned by

Bits	Name	Description
		the Host. The IDMAC clears this bit when it completes the data transfer.
30	Card Error Summary (CES)	These error bits indicate the status of the transaction to or from the card. These bits are also present in RINTSTS Indicates the logical OR of the following bits: EBE: End Bit Error RTO: Response Time out RCRC: Response CRC SBE: Start Bit Error DRTO: Data Read Timeout DCRC: Data CRC for Receive RE: Response Error
29:6	Reserved	-
5	End of Ring (ER)	When set, this bit indicates that the descriptor list reached its final descriptor. The IDMAC returns to the base address of the list, creating a Descriptor Ring. This is meaningful for only a dual-buffer descriptor structure.
4	Second Address Chained (CH)	When set, this bit indicates that the second address in the descriptor is the Next Descriptor address rather than the second buffer address. When this bit is set, BS2 (DES1[25:13]) should be all zeros.
3	First Descriptor (FS)	When set, this bit indicates that this descriptor contains the first buffer of the data. If the size of the first buffer is 0, next Descriptor contains the beginning of the data.
2	Last Descriptor (LD)	This bit is associated with the last block of a DMA transfer. When set, the bit indicates that the buffers pointed to by this descriptor are the last buffers of the data. After this descriptor is completed, the remaining byte count is 0. In other words, after the descriptor with the LD bit set is completed, the remaining byte count should be 0.
1	Disable Interrupt on Completion (DIC)	When set, this bit will prevent the setting of the TI/RI bit of the IDMAC Status Register (IDSTS) for the data that ends in the buffer pointed to by this descriptor.
0	Reserved	-

- The DES1 element contains the buffer size.

Table 4-5 Bits in IDMAC DES1 Element

Bits	Name	Description
31:26	Reserved	-
25:13	Buffer 2 Size (BS2)	These bits indicate the second data buffer byte size. The buffer size must be a multiple of 2, 4, or 8, depending upon the bus widths—16, 32, and 64, respectively. In the case where the buffer size is not a multiple of 2, 4, or 8, the resulting behavior is undefined. If this field is 0, the DMA ignores this buffer and

Bits	Name	Description
		proceeds to the next buffer in case of a dual-buffer structure. This field is not valid for chain structure; that is, if DES0[4] is set.
12:0	Buffer 1 Size (BS1)	Indicates the data buffer byte size, which must be a multiple of 2, 4, or 8 bytes, depending upon the bus widths—16, 32, and 64, respectively. In the case where the buffer size is not a multiple of 2, 4, or 8, the resulting behavior is undefined. This field should not be zero. Note: If there is only one buffer to be programmed, you need to use only the Buffer 1, and not Buffer 2.

- The DES2 element contains the address pointer to the data buffer.

Table 4-6 Bits in IDMAC DES2 Element

Bits	Name	Description
31:26	Reserved	
25:13	Buffer 2 Size (BS2)	These bits indicate the second data buffer byte size. The buffer size must be a multiple of 2, 4, or 8, depending upon the bus widths—16, 32, and 64, respectively. In the case where the buffer size is not a multiple of 2, 4, or 8, the resulting behavior is undefined. If this field is 0, the DMA ignores this buffer and proceeds to the next buffer in case of a dual-buffer structure. This field is not valid for chain structure; that is, if DES0[4] is set.
12:0	Buffer 1 Size (BS1)	Indicates the data buffer byte size, which must be a multiple of 2, 4, or 8 bytes, depending upon the bus widths—16, 32, and 64, respectively. In the case where the buffer size is not a multiple of 2, 4, or 8, the resulting behavior is undefined. This field should not be zero. Note: If there is only one buffer to be programmed, you need to use only the Buffer 1, and not Buffer 2.

- The DES3 element contains the address pointer to the next descriptor if the present descriptor is not the last descriptor in a chained descriptor structure or the second buffer address for a dual-buffer structure.

Table 4-7 Bits in IDMAC DES3 Element

Bits	Name	Description
31:0	Buffer Address Pointer 2/ Next Descriptor Address (BAP2)	These bits indicate the physical address of the second buffer when the dual-buffer structure is used. If the Second Address Chained (DES0[4]) bit is set, then this address contains the pointer to the physical memory where the Next Descriptor is present. If this is not the last descriptor, then the Next Descriptor address pointer must be bus-width aligned.

3. Initialization

IDMAC initialization occurs as follows:

Write to IDMAC Bus Mode Register—BMOD to set Host bus access parameters.

Write to IDMAC Interrupt Enable Register—IDINTEN to mask unnecessary interrupt causes.

The software driver creates either the Transmit or the Receive descriptor list. Then it writes to IDMAC Descriptor List Base Address Register (DBADDR), providing the IDMAC with the starting address of the list.

The IDMAC engine attempts to acquire descriptors from the descriptor lists.

- **Host Bus Burst Access**

The IDMAC attempts to execute fixed-length burst transfers on the AHB Master interface if configured using the FB bit of the IDMAC Bus Mode register. The maximum burst length is indicated and limited by the PBL field. The descriptors are always accessed in the maximum possible burst-size for the 16-bytes to be read— 16*8/bus-width.

The IDMAC initiates a data transfer only when sufficient space to accommodate the configured burst is available in the FIFO or the number of bytes to the end of data, when less than the configured burst-length.

The IDMAC indicates the start address and the number of transfers required to the AHB Master Interface. When the AHB Interface is configured for fixed-length bursts, then it transfers data using the best combination of INCR4/8/16 and SINGLE transactions. Otherwise, in no fixed-length bursts, it transfers data using INCR (undefined length) and SINGLE transactions.

- **Host Data Buffer Alignment**

The Transmit and Receive data buffers in host memory must be aligned, depending on the data width.

- **Buffer Size Calculations**

The driver knows the amount of data to transmit or receive. For transmitting to the card, the IDMAC transfers the exact number of bytes to the FIFO, indicated by the buffer size field of DES1.

If a descriptor is not marked as last-LS bit of DES0-then the corresponding buffer(s) of the descriptor are full, and the amount of valid data in a buffer is accurately indicated by its buffer size field. If a descriptor is marked as last, then the buffer cannot be full, as indicated by the buffer size in DES1. The driver is aware of the number of locations that are valid in this case.

- **Transmission**

IDMAC transmission occurs as follows:

The Host sets up the elements (DES0-DES3) for transmission and sets the OWN bit (DES0[31]). The Host also prepares the data buffer.

The Host programs the write data command in the CMD register in BIU.

The Host will also program the required transmit threshold level (TX_WMark field in FIFOTH register).

The IDMAC determines that a write data transfer needs to be done as a consequence of step 2.

The IDMAC engine fetches the descriptor and checks the OWN bit. If the OWN bit is not set, it means that the host owns the descriptor. In this case the IDMAC enters suspend state and asserts the Descriptor Unable interrupt in the IDSTS register. In such a case, the host needs to release the IDMAC by writing any value to the poll demand register.

It will then wait for Command Done (CD) bit and no errors from BIU which indicates that a transfer can be done.

The IDMAC engine will now wait for a DMA interface request from BIU. This request will be generated based on the programmed transmit threshold value. For the last bytes of data which can't be accessed using a burst, SINGLE transfers are performed on AHB Master Interface.

The IDMAC fetches the Transmit data from the data buffer in the Host memory and transfers to the FIFO for transmission to card.

When data spans across multiple descriptors, the IDMAC will fetch the next descriptor and continue with its operation with the next descriptor. The Last Descriptor bit in the descriptor indicates whether the data spans multiple descriptors or not.

When data transmission is complete, status information is updated in IDSTS register by setting Transmit Interrupt, if enabled. Also, the OWN bit is cleared by the IDMAC by performing a write transaction to DES0.

- Reception

IDMAC reception occurs as follows:

The Host sets up the element (DES0-DES3) for reception, sets the OWN (DES0[31]).

The Host programs the read data command in the CMD register in BIU.

The Host will program the required receive threshold level (RX_WMark field in FIFO TH register).

The IDMAC determines that a read data transfer needs to be done as a consequence of step 2.

The IDMAC engine fetches the descriptor and checks the OWN bit. If the OWN bit is not set, it means that the host owns the descriptor. In this case the DMA enters suspend state and asserts the Descriptor Unable interrupt in the IDSTS register. In such a case, the host needs to release the IDMAC by writing any value to the poll demand register.

It will then wait for Command Done (CD) bit and no errors from BIU which indicates that a transfer can be done.

The IDMAC engine will now wait for a DMA interface request from BIU. This request will be generated based on the programmed receive threshold value. For the last bytes of data which can't be accessed using a burst, SINGLE transfers are performed on AHB.

The IDMAC fetches the data from the FIFO and transfer to Host memory.

When data spans across multiple descriptors, the IDMAC will fetch the next descriptor and continue with its operation with the next descriptor. The Last Descriptor bit in the descriptor indicates whether the data spans multiple descriptors or not.

When data reception is complete, status information is updated in IDSTS register by setting Receive Interrupt, if enabled. Also, the OWN bit is cleared by the IDMAC by performing a write transaction to DES0.

- Interrupts

Interrupts can be generated as a result of various events. IDSTS register contains all the bits that might cause an interrupt. IDINTEN register contains an Enable bit for each of the events that can cause an interrupt.

There are two groups of summary interrupts-Normal and Abnormal-as outlined in IDSTS register. Interrupts are cleared by writing a 1 to the corresponding bit position. When all the enabled interrupts within a group are cleared, the corresponding summary bit is cleared. When both the summary bits are cleared, the interrupt signal dmac_intr_o is de-asserted.

Interrupts are not queued and if the interrupt event occurs before the driver has responded to it, no additional interrupts are generated. For example, Receive Interrupt—IDSTS[1] indicates that one or more data was transferred to the Host buffer.

An interrupt is generated only once for simultaneous, multiple events. The driver must scan IDSTS register for the interrupt cause.

4.4 Register Description

4.4.1 Register Summary

Name	Offset	Size	Reset Value	Description
SDMMC_CTRL	0x0000	W	0x01000000	Control register
SDMMC_PWREN	0x0004	W	0x00000000	Power-enable register
SDMMC_CLKDIV	0x0008	W	0x00000000	Clock-divider register
SDMMC_CLKSRC	0x000c	W	0x00000000	SD Clock Source Register
SDMMC_CLKENA	0x0010	W	0x00000000	Clock-enable register
SDMMC_TMOUT	0x0014	W	0xfffffff40	Time-out register
SDMMC_CTYPE	0x0018	W	0x00000000	Card-type register
SDMMC_BLKSIZ	0x001c	W	0x00000200	Block-size register
SDMMC_BYTCNT	0x0020	W	0x00000200	Byte-count register
SDMMC_INTMASK	0x0024	W	0x00000000	Interrupt-mask register

Name	Offset	Size	Reset Value	Description
SDMMC_CMDARG	0x0028	W	0x00000000	Command-argument register
SDMMC_CMD	0x002c	W	0x00000000	Command register
SDMMC_RESP0	0x0030	W	0x00000000	Response-0 register
SDMMC_RESP1	0x0034	W	0x00000000	Response-1 register
SDMMC_RESP2	0x0038	W	0x00000000	Response-2 register
SDMMC_RESP3	0x003c	W	0x00000000	Response-3 register
SDMMC_MINTSTS	0x0040	W	0x00000000	Masked interrupt-status register
SDMMC_RINTSTS	0x0044	W	0x00000000	Raw interrupt-status register
SDMMC_STATUS	0x0048	W	0x00000406	Status register
SDMMC_FIFOTH	0x004c	W	0x00000000	FIFO threshold register
SDMMC_CDETECT	0x0050	W	0x00000000	Card-detect register
SDMMC_WRTPRT	0x0054	W	0x00000000	Write-protect register
SDMMC_TCBCNT	0x005c	W	0x00000000	Transferred CIU card byte count
SDMMC_TBBCNT	0x0060	W	0x00000000	Transferred host/DMA to/from BIU-FIFO byte count
SDMMC_DEBNCE	0x0064	W	0x00ffffff	Card detect debounce register
SDMMC_USRID	0x0068	W	0x07967797	User ID register
SDMMC_VERID	0x006c	W	0x5342270a	Synopsys version ID register
SDMMC_HCON	0x0070	W	0x00000000	Hardware Configuration Register
SDMMC_UHS_REG	0x0074	W	0x00000000	UHS-1 register
SDMMC_RST_N	0x0078	W	0x00000001	Hardware reset register
SDMMC_BMOD	0x0080	W	0x00000000	Bus Mode Register
SDMMC_PLDMND	0x0084	W	0x00000000	Poll Demand Register
SDMMC_DBADDR	0x0088	W	0x00000000	Descriptor List Base Address Register
SDMMC_IDSTS	0x008c	W	0x00000000	Internal DMAC Status Register
SDMMC_IDINTEN	0x0090	W	0x00000000	Internal DMAC Interrupt Enable Register
SDMMC_DSCADDR	0x0094	W	0x00000000	Current Host Descriptor Address Register
SDMMC_BUFADDR	0x0098	W	0x00000000	Current Buffer Descriptor Address Register
SDMMC_CARDTHRCTL	0x0100	W	0x00000000	Card read threshold enable
SDMMC_BACK_END_POWER	0x0104	W	0x00000000	Back-end power
SDMMC_UHS_REG_EXT	0x0108	W	0x00000000	UHS Register
SDMMC_EMMC_DDR_REG	0x010c	W	0x00000000	eMMC 4.5 DDR START Bit Detection Control Register
SDMMC_ENABLE_SHIFT	0x0110	W	0x00000000	Enable Phase Shift Register
SDMMC_FIFO_BASE	0x0200	W	0x00000000	FIFO Base Address

Notes: Size : **B** - Byte (8 bits) access, **HW** - Half WORD (16 bits) access, **W** -WORD (32 bits) access

4.4.2 Detail Register Description

SDMMC_CTRL

Address: Operational Base + offset (0x0000)

Control register

Bit	Attr	Reset Value	Description
31:26	RO	0x0	reserved
25	RW	0x0	use_internal_dmac Present only for the Internal DMAC configuration; else, it is reserved. 0: The host performs data transfers through the slave interface 1: Internal DMAC used for data transfe
24	RW	0x1	enable_OD_pullup External open-drain pullup: 0: Disable 1: Enable Inverted value of this bit is output to ccmd_od_pullup_en_n port. When bit is set, command output always driven in open-drive mode; that is, DWC_mobile_storage drives either 0 or high impedance, and does not drive hard 1.
23:20	RW	0x0	Card_voltage_b Card regulator-B voltage setting; output to card_volt_b port. Optional feature; ports can be used as general-purpose outputs.
19:16	RW	0x0	Card_voltage_a Card regulator-A voltage setting; output to card_volt_a port. Optional feature; ports can be used as general-purpose outputs.
15:12	RO	0x0	reserved
11	RW	0x0	ceata_device_interrupt_status 0: Interrupts not enabled in CE-ATA device (nIEN = 1 in ATA control register) 1: Interrupts are enabled in CE-ATA device (nIEN = 0 in ATA control register) Software should appropriately write to this bit after power-on reset or any other reset to CE-ATA device. After reset, usually CE-ATA device interrupt is disabled (nIEN = 1). If the host enables CE-ATA device interrupt, then software should set this bit.

Bit	Attr	Reset Value	Description
10	RW	0x0	<p>send_auto_stop_ccsd 0: Clear bit if DWC_mobile_storage does not reset the bit. 1: Send internally generated STOP after sending CCSD to CE-ATA device. NOTE: Always set send_auto_stop_ccsd and send_ccsd bits together send_auto_stop_ccsd should not be set independent of send_ccsd.</p> <p>When set, DWC_Mobile_Storage automatically sends internally-generated STOP command (CMD12) to CE-ATA device. After sending internally-generated STOP command, Auto Command Done (ACD) bit in RINTSTS is set and generates interrupt to host if Auto Command Done interrupt is not masked. After sending the CCSD, DWC_mobile_storage automatically clears send_auto_stop_ccsd bit.</p>
9	RW	0x0	<p>send_ccsd 0: Clear bit if DWC_mobile_storage does not reset the bit. 1: Send Command Completion Signal Disable (CCSD) to CE-ATA device</p> <p>When set, DWC_mobile_storage sends CCSD to CE-ATA device. Software sets this bit only if current command is expecting CCS (that is, RW_BLK) and interrupts are enabled in CE-ATA device. Once the CCSD pattern is sent to device, DWC_mobile_storage automatically clears send_ccsd bit. It also sets Command Done (CD) bit in RINTSTS register and generates interrupt to host if Command Done interrupt is not masked.</p> <p>NOTE: Once send_ccsd bit is set, it takes two card clock cycles to drive the CCSD on the CMD line. Due to this, during the boundary conditions it may happen that CCSD is sent to the CE-ATA device, even if the device signalled CCS</p>

Bit	Attr	Reset Value	Description
8	RW	0x0	abort_read_data 0: no change 1: after suspend command is issued during read-transfer, software polls card to find when suspend happened. Once suspend occurs, software sets bit to reset data state-machine, which is waiting for next block of data. Bit automatically clears once data state machine resets to idle. Used in SDIO card suspend sequence.
7	RW	0x0	send_irq_response 0: no change 1: send auto IRQ response Bit automatically clears once response is sent. To wait for MMC card interrupts, host issues CMD40, and SDMMC Controller waits for interrupt response from MMC card(s). In meantime, if host wants SDMMC Controller to exit waiting for interrupt state, it can set this bit, at which time SDMMC Controller command state-machine sends CMD40 response on bus and returns to idle state.
6	RW	0x0	read_wait 0: clear read wait 1: assert read wait For sending read-wait to SDIO cards
5	RW	0x0	dma_enable 0: disable DMA transfer mode 1: enable DMA transfer mode Even when DMA mode is enabled, host can still push/pop data into or from FIFO; this should not happen during the normal operation. If there is simultaneous FIFO access from host/DMA, the data coherency is lost. Also, there is no arbitration inside SDMMC Controller to prioritize simultaneous host/DMA access.
4	RW	0x0	int_enable Global interrupt enable/disable bit: 0: disable interrupts 1: enable interrupts The int port is 1 only when this bit is 1 and one or more unmasked interrupts are set.
3	RO	0x0	reserved

Bit	Attr	Reset Value	Description
2	W1C	0x0	<p>dma_reset 0: no change 1: reset internal DMA interface control logic To reset DMA interface, firmware should set bit to 1. This bit is auto-cleared after two AHB clocks. The DMA should be reset before it switches from no-dma mode into dma mode.</p>
1	W1C	0x0	<p>fifo_reset 0: no change 1: reset to data FIFO To reset FIFO pointers To reset FIFO, firmware should set bit to 1. This bit is auto-cleared after completion of reset operation</p>
0	W1C	0x0	<p>controller_reset 0: no change 1: reset SDMMC controller To reset controller, firmware should set bit to 1. This bit is auto-cleared after two AHB and two cclk_in clock cycles. This resets: * BIU/CIU interface * CIU and state machines * abort_read_data, send_irq_response, and read_wait bits of Control register * start_cmd bit of Command register Does not affect any registers or DMA interface, or FIFO or host interrupts</p>

SDMMC_PWREN

Address: Operational Base + offset (0x0004)

Power-enable register

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	<p>power_enable Power on/off switch for the card. Once power is turned on, firmware should wait for regulator/switch ramp-up time before trying to initialize card. 0: power off 1: power on Bit values output to card_power_en port.</p>

SDMMC_CLKDIV

Address: Operational Base + offset (0x0008)

Clock-divider register

Bit	Attr	Reset Value	Description
31:24	RW	0x00	clk_divider3 Clock divider-3 value. For example, value of 0 means divide by $2^0 = 0$ (no division, bypass), value of 1 means divide by $2^1 = 2$, value of "ff"means divide by $2^{255} = 510$, and so on In MMC-Ver3.3-only mode, bits not implemented because only one clock divider is supported. In our design, the divider is 0 or 1 supported.
23:16	RW	0x00	clk_divider2 Clock divider-2 value. Clock division is 2^n . For example, value of 0 means divide by $2^0 = 0$ (no division, bypass), value of 1 means divide by $2^1 = 2$, value of "ff"means divide by $2^{255} = 510$, and so on In MMC-Ver3.3-only mode, bits not implemented because only one clock divider is supported. In our design, the divider is 0 or 1 supported.
15:8	RW	0x00	clk_divider1 Clock divider-1 value. Clock division is 2^n . For example, value of 0 means divide by $2^0 = 0$ (no division, bypass), value of 1 means divide by $2^1 = 2$, value of "ff"means divide by $2^{255} = 510$, and so on In MMC-Ver3.3-only mode, bits not implemented because only one clock divider is supported. In our design, the divider is 0 or 1 supported.
7:0	RW	0x00	clk_divider0 Clock divider-0 value. Clock division is 2^n . For example, value of 0 means divide by $2^0 = 0$ (no division, bypass), value of 1 means divide by $2^1 = 2$, value of "ff"means divide by $2^{255} = 510$, and so on. In our design, the divider is 0 or 1 supported.

SDMMC_CLKSRC

Address: Operational Base + offset (0x000c)

SD Clock Source Register

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved

Bit	Attr	Reset Value	Description
1:0	RW	0x0	<p>clk_source Clock divider source for up to 16 SD cards supported. Each card has two bits assigned to it. For example, bits[1:0] assigned for card-0, which maps and internally routes clock divider[3:0] outputs to cclk_out[15:0] pins, depending on bit value.</p> <ul style="list-style-type: none"> 00 –Clock divider 0 01 –Clock divider 1 10 –Clock divider 2 11 –Clock divider 3 <p>In our design, the cclk_out is always from clock divider 0, and this register is not implemented.</p>

SDMMC_CLKENA

Address: Operational Base + offset (0x0010)

Clock-enable register

Bit	Attr	Reset Value	Description
31:17	RO	0x0	reserved
16	RW	0x0	<p>cclk_low_power Low-power control for SD card clock and MMC card clock supported. 0: non-low-power mode 1: low-power mode; stop clock when card in IDLE (should be normally set to only MMC and SD memory cards; for SDIO cards, if interrupts must be detected, clock should not be stopped).</p>
15:1	RO	0x0	reserved
0	RW	0x0	<p>cclk_enable Clock-enable control for SD card clock and MMC card clock supported. 0: clock disabled 1: clock enabled</p>

SDMMC_TMOUT

Address: Operational Base + offset (0x0014)

Time-out register

Bit	Attr	Reset Value	Description
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Bit	Attr	Reset Value	Description
31:8	RW	0xffffffff	<p>data_timeout Value for card Data Read Timeout; same value also used for Data Starvation by Host timeout. Value is in number of card output clocks cclk_out of selected card.</p> <p>Note: The software timer should be used if the timeout value is in the order of 100 ms. In this case, read data timeout interrupt needs to be disabled.</p>
7:0	RW	0x40	<p>response_timeout Response timeout value. Value is in number of card output clocks -cclk_out.</p>

SDMMC_CTYPE

Address: Operational Base + offset (0x0018)

Card-type register

Bit	Attr	Reset Value	Description
31:17	RO	0x0	reserved
16	RW	0x0	<p>card_width_8 Indicates if card is 8-bit: 0: non 8-bit mode 1: 8-bit mode</p>
15:1	RO	0x0	reserved
0	RW	0x0	<p>card_width Indicates if card is 1-bit or 4-bit: 0: 1-bit mode 1: 4-bit mode</p>

SDMMC_BLKSIZ

Address: Operational Base + offset (0x001c)

Block-size register

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:0	RW	0x0200	<p>block_size Block size</p>

SDMMC_BYTCNT

Address: Operational Base + offset (0x0020)

Byte-count register

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:0	RW	0x00000200	<p>byte_count Number of bytes to be transferred; should be integer multiple of Block Size for block transfers.</p> <p>For undefined number of byte transfers, byte count should be set to 0. When byte count is set to 0, it is responsibility of host to explicitly send stop/abort command to terminate data transfer.</p>

SDMMC_INTMASK

Address: Operational Base + offset (0x0024)

Interrupt-mask register

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24	RW	0x0	<p>sdio_int_mask Mask SDIO interrupts. When masked, SDIO interrupt detection for that card is disabled. A 0 masks an interrupt, and 1 enables an interrupt.</p>
23:17	RO	0x0	reserved
16	RW	0x0	<p>data_nobusy_int_mask 0: data no busy interrupt not masked 1: data no busy interrupt masked</p>
15:0	RW	0x0000	<p>int_mask Bits used to mask unwanted interrupts. Value of 0 masks interrupt; value of 1 enables interrupt. bit 15: End-bit error (read)/Write no CRC (EBE) bit 14: Auto command done (ACD) bit 13: Start-bit error (SBE) bit 12: Hardware locked write error (HLE) bit 11: FIFO underrun/overrun error (FRUN) bit 10: Data starvation-by-host timeout (HTO) /Volt_switch_int bit 9: Data read timeout (DRTO) bit 8: Response timeout (RTO) bit 7: Data CRC error (DCRC) bit 6: Response CRC error (RCRC) bit 5: Receive FIFO data request (RXDR) bit 4: Transmit FIFO data request (TXDR) bit 3: Data transfer over (DTO) bit 2: Command done (CD) bit 1: Response error (RE) bit 0: Card detect (CD)</p>

SDMMC_CMDARG

Address: Operational Base + offset (0x0028)

Command-argument register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	cmd_arg Value indicates command argument to be passed to card.

SDMMC_CMD

Address: Operational Base + offset (0x002c)

Command register

Bit	Attr	Reset Value	Description
31	RW	0x0	start_cmd Start command. Once command is taken by CIU, bit is cleared. When bit is set, host should not attempt to write to any command registers. If write is attempted, hardware lock error is set in raw interrupt register. Once command is sent and response is received from SD_MMC cards, Command Done bit is set in raw interrupt register.
30	RO	0x0	reserved
29	RW	0x0	use_hold_reg Use Hold Register 0: CMD and DATA sent to card bypassing HOLD Register 1: CMD and DATA sent to card through the HOLD Register Note: a. Set to 1'b1 for SDR12 and SDR25 (with non-zero phase-shifted cclk_in_drv); zero phase shift is not allowed in these modes. b. Set to 1'b0 for SDR50, SDR104, and DDR50 (with zero phase-shifted cclk_in_drv) c. Set to 1'b1 for SDR50, SDR104, and DDR50 (with non-zero phase-shifted cclk_in_drv)
28	RW	0x0	volt_switch Voltage switch bit. 0: no voltage switching 1: voltage switching enabled; must be set for CMD11 only
27	RW	0x0	boot_mode Boot Mode. 0: mandatory Boot operation 1: alternate Boot operation

Bit	Attr	Reset Value	Description
26	RW	0x0	disable_boot Disable Boot. When software sets this bit along with start_cmd, CIU terminates the boot operation. Do NOT set disable_boot and enable_boot together.
25	RW	0x0	expect_boot_ack Expect Boot Acknowledge. When Software sets this bit along with enable_boot, CIU expects a boot acknowledge start pattern of 0-1-0 from the selected card.
24	RW	0x0	enable_boot Enable Boot—this bit should be set only for mandatory boot mode. When Software sets this bit along with start_cmd, CIU starts the boot sequence for the corresponding card by asserting the CMD line low. Do NOT set disable_boot and enable_boot together.
23	RW	0x0	ccs_expected 0: Interrupts are not enabled in CE-ATA device (nIEN = 1 in ATA control register), or command does not expect CCS from device 1: Interrupts are enabled in CE-ATA device (nIEN = 0), and RW_BLK command expects command completion signal from CE-ATA device If the command expects Command Completion Signal (CCS) from the CE-ATA device, the software should set this control bit. DWC_mobile_storage sets Data Transfer Over (DTO) bit in RINTSTS register and generates interrupt to host if Data Transfer Over interrupt is not masked.
22	RW	0x0	read_ceata_device 0: Host is not performing read access (RW_REG or RW_BLK) towards CE-ATA device 1: Host is performing read access (RW_REG or RW_BLK) towards CE-ATA device Software should set this bit to indicate that CE-ATA device is being accessed for read transfer. This bit is used to disable read data timeout indication while performing CE-ATA read transfers. Maximum value of I/O transmission delay can be no less than 10 seconds. DWC_mobile_storage should not indicate read data timeout while waiting for data from CE-ATA device.

Bit	Attr	Reset Value	Description
21	RW	0x0	<p>update_clock_registers_only 0: normal command sequence 1: do not send commands, just update clock register value into card clock domain</p> <p>Following register values transferred into card clock domain: CLKDIV, CLRSRC, CLKENA.</p> <p>Changes card clocks (change frequency, truncate off or on, and set low-frequency mode); provided in order to change clock frequency or stop clock without having to send command to cards.</p> <p>During normal command sequence, when update_clock_registers_only = 0, following control registers are transferred from BIU to CIU: CMD, CMDARG, TMOUT, CTYPE, BLKSIZ, BYTCNT. CIU uses new register values for new command sequence to card.</p> <p>When bit is set, there are no Command Done interrupts because no command is sent to SD_MMC_CEATA cards.</p>
20:16	RW	0x00	<p>card_number</p> <p>Card number in use. Represents physical slot number of card being accessed. In MMC-Ver3.3-only mode, up to 30 cards are supported; in SD-only mode, up to 16 cards are supported.</p> <p>Registered version of this is reflected on dw_dma_card_num and ge_dma_card_num ports, which can be used to create separate DMA requests, if needed.</p> <p>In addition, in SD mode this is used to mux or demux signals from selected card because each card is interfaced to DWC_mobile_storage by separate bus.</p>
15	RW	0x0	<p>send_initialization</p> <p>0: do not send initialization sequence (80 clocks of 1) before sending this command</p> <p>1: send initialization sequence before sending this command</p> <p>After power on, 80 clocks must be sent to card for initialization before sending any commands to card. Bit should be set while sending first command to card so that controller will initialize clocks before sending command to card. This bit should not be set for either of the boot modes (alternate or mandatory).</p>

Bit	Attr	Reset Value	Description
14	RW	0x0	<p>stop_abort_cmd</p> <p>0: neither stop nor abort command to stop current data transfer in progress. If abort is sent to function-number currently selected or not in data-transfer mode, then bit should be set to 0.</p> <p>1: stop or abort command intended to stop current data transfer in progress.</p> <p>When open-ended or predefined data transfer is in progress, and host issues stop or abort command to stop data transfer, bit should be set so that command/data state-machines of CIU can return correctly to idle state. This is also applicable for Boot mode transfers. To Abort boot mode, this bit should be set along with CMD[26] = disable_boot.</p>
13	RW	0x0	<p>wait_prvdata_complete</p> <p>0: send command at once, even if previous data transfer has not completed</p> <p>1: wait for previous data transfer completion before sending command</p> <p>The wait_prvdata_complete = 0 option typically used to query status of card during data transfer or to stop current data transfer; card_number should be same as in previous command.</p>
12	RW	0x0	<p>send_auto_stop</p> <p>0: no stop command sent at end of data transfer</p> <p>1: send stop command at end of data transfer</p> <p>When set, SDMMC Controller sends stop command to SD_MMC cards at end of data transfer.</p> <ul style="list-style-type: none"> * when send_auto_stop bit should be set, since some data transfers do not need explicit stop commands * open-ended transfers that software should explicitly send to stop command <p>Additionally, when "resume" is sent to resume –suspended memory access of SD-Combo card –bit should be set correctly if suspended data transfer needs send_auto_stop.</p> <p>Don't care if no data expected from card.</p>
11	RW	0x0	<p>transfer_mode</p> <p>0: block data transfer command</p> <p>1: stream data transfer command</p> <p>Don't care if no data expected.</p>

Bit	Attr	Reset Value	Description
10	RW	0x0	wr 0: read from card 1: write to card Don't care if no data expected from card.
9	RW	0x0	data_expected 0: no data transfer expected (read/write) 1: data transfer expected (read/write)
8	RW	0x0	check_response_crc 0: do not check response CRC 1: check response CRC Some of command responses do not return valid CRC bits. Software should disable CRC checks for those commands in order to disable CRC checking by controller
7	RW	0x0	response_length 0: short response expected from card 1: long response expected from card
6	RW	0x0	response_expect 0: no response expected from card 1: response expected from card
5:0	RW	0x00	cmd_index Command index

SDMMC_RESP0

Address: Operational Base + offset (0x0030)

Response-0 register

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	response0 Bit[31:0] of response

SDMMC_RESP1

Address: Operational Base + offset (0x0034)

Response-1 register

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	response Register represents bit[63:32] of long response. When CIU sends auto-stop command, then response is saved in register. Response for previous command sent by host is still preserved in Response 0 register. Additional auto-stop issued only for data transfer commands, and response type is always "short" for them.

SDMMC_RESP2

Address: Operational Base + offset (0x0038)

Response-2 register

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	response2 Bit[95:64] of long response

SDMMC_RESP3

Address: Operational Base + offset (0x003c)

Response-3 register

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	response3 Bit[127:96] of long response

SDMMC_MINTSTS

Address: Operational Base + offset (0x0040)

Masked interrupt-status register

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24	RO	0x0	sdio_interrupt Interrupt from SDIO card; SDIO interrupt for card enabled only if corresponding sdio_int_mask bit is set in Interrupt mask register (mask bit 1 enables interrupt; 0 masks interrupt). 0: no SDIO interrupt from card 1: SDIO interrupt from card
23:17	RO	0x0	reserved
16	RW	0x0	data_nobusy_int_status Data no busy Interrupt Status

Bit	Attr	Reset Value	Description
15:0	RO	0x0000	<p>int_status Interrupt enabled only if corresponding bit in interrupt mask register is set.</p> <p>bit 15: End-bit error (read)/Write no CRC (EBE) bit 14: Auto command done (ACD) bit 13: Start-bit error (SBE) bit 12: Hardware locked write error (HLE) bit 11: FIFO underrun/overrun error (FRUN) bit 10: Data starvation-by-host timeout (HTO)</p> <p>/Volt_switch_int</p> <p>bit 9: Data read timeout (DRTO) bit 8: Response timeout (RTO) bit 7: Data CRC error (DCRC) bit 6: Response CRC error (RCRC) bit 5: Receive FIFO data request (RXDR) bit 4: Transmit FIFO data request (TXDR) bit 3: Data transfer over (DTO) bit 2: Command done (CD) bit 1: Response error (RE) bit 0: Card detect (CD)</p>

SDMMC_RINTSTS

Address: Operational Base + offset (0x0044)

Raw interrupt-status register

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24	RO	0x0	<p>sdio_interrupt Interrupt from SDIO card; Writes to these bits clear them. Value of 1 clears bit and 0 leaves bit intact.</p> <p>0: no SDIO interrupt from card 1: SDIO interrupt from card</p>
23:17	RO	0x0	reserved
16	RW	0x0	<p>data_nobusy_int_status Data no busy interrupt status</p>

Bit	Attr	Reset Value	Description
15:0	RO	0x0000	<p>int_status</p> <p>Writes to bits clear status bit. Value of 1 clears status bit, and value of 0 leaves bit intact. Bits are logged regardless of interrupt mask status.</p> <p>bit 15: End-bit error (read)/Write no CRC (EBE)</p> <p>bit 14: Auto command done (ACD)</p> <p>bit 13: Start-bit error (SBE)</p> <p>bit 12: Hardware locked write error (HLE)</p> <p>bit 11: FIFO underrun/overrun error (FRUN)</p> <p>bit 10: Data starvation-by-host timeout (HTO) /Volt_switch_int</p> <p>bit 9: Data read timeout (DRTO)</p> <p>bit 8: Response timeout (RTO)</p> <p>bit 7: Data CRC error (DCRC)</p> <p>bit 6: Response CRC error (RCRC)</p> <p>bit 5: Receive FIFO data request (RXDR)</p> <p>bit 4: Transmit FIFO data request (TXDR)</p> <p>bit 3: Data transfer over (DTO)</p> <p>bit 2: Command done (CD)</p> <p>bit 1: Response error (RE)</p> <p>bit 0: Card detect (CD)</p>

SDMMC_STATUS

Address: Operational Base + offset (0x0048)

Status register

Bit	Attr	Reset Value	Description
31	RO	0x0	dma_req DMA request signal state
30	RO	0x0	dma_ack DMA acknowledge signal state
29:17	RO	0x0000	fifo_count Number of filled locations in FIFO
16:11	RO	0x00	response_index Index of previous response, including any auto-stop sent by core
10	RO	0x1	data_state_mc_busy Data transmit or receive state-machine is busy
9	RO	0x0	data_busy Inverted version of raw selected card_data[0] 0: card data not busy 1: card data busy default value is 1 or 0 depending on cdata_in

Bit	Attr	Reset Value	Description
8	RO	0x0	<p>data_3_status Raw selected card_data[3]; checks whether card is present 0: card not present 1: card present default value is 1 or 0 depending on cdata_in</p>
7:4	RO	0x0	<p>command_fsm_states Command FSM states: 0: idle 1: send init sequence 2: Tx cmd start bit 3: Tx cmd tx bit 4: Tx cmd index + arg 5: Tx cmd crc7 6: Tx cmd end bit 7: Rx resp start bit 8: Rx resp IRQ response 9: Rx resp tx bit 10: Rx resp cmd idx 11: Rx resp data 12: Rx resp crc7 13: Rx resp end bit 14: Cmd path wait NCC 15: Wait; CMD-to-response turnaround The command FSM state is represented using 19 bits. The STATUS Register[7:4] has 4 bits to represent the command FSM states. Using these 4 bits, only 16 states can be represented. Thus three states cannot be represented in the STATUS[7:4] register. The three states that are not represented in the STATUS Register[7:4] are:</p> <ul style="list-style-type: none"> * Bit 16 –Wait for CCS * Bit 17 –Send CCSD * Bit 18 –Boot Mode <p>Due to this, while command FSM is in “Wait for CCS state”or “Send CCSD”or “Boot Mode”, the Status register indicates status as 0 for the bit field [7:4].</p>
3	RO	0x0	fifo_full FIFO is full status
2	RO	0x1	fifo_empty FIFO is empty status

Bit	Attr	Reset Value	Description
1	RO	0x1	fifo_tx_watermark FIFO reached Transmit watermark level; not qualified with data transfer
0	RO	0x0	fifo_rx_watermark FIFO reached Receive watermark level; not qualified with data transfer

SDMMC_FIFOTH

Address: Operational Base + offset (0x004c)

FIFO threshold register

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved

Bit	Attr	Reset Value	Description
30:28	RW	0x0	<p>dma_multiple_transaction_size Burst size of multiple transaction; should be programmed same as DMA controller multiple-transaction-size SRC/DEST_MSIZE.</p> <p>3'b000: 1 transfers 3'b001: 4 3'b010: 8 3'b011: 16 3'b100: 32 3'b101: 64 3'b110: 128 3'b111: 256</p> <p>The unit for transfer is the H_DATA_WIDTH parameter. A single transfer (dw_dma_single assertion in case of Non DW DMA interface) would be signalled based on this value.</p> <p>Value should be sub-multiple of $(RX_WMark + 1) * (F_DATA_WIDTH/H_DATA_WIDTH)$ and $(FIFO_DEPTH - TX_WMark) * (F_DATA_WIDTH/ H_DATA_WIDTH)$</p> <p>For example, if FIFO_DEPTH = 16, FDATA_WIDTH == H_DATA_WIDTH</p> <p>Allowed combinations for MSize and TX_WMark are:</p> <ul style="list-style-type: none"> MSize = 1, TX_WMARK = 1-15 MSize = 4, TX_WMark = 8 MSize = 4, TX_WMark = 4 MSize = 4, TX_WMark = 12 MSize = 8, TX_WMark = 8 MSize = 8, TX_WMark = 4 <p>Allowed combinations for MSize and RX_WMark are:</p> <ul style="list-style-type: none"> MSize = 1, RX_WMARK = 0-14 MSize = 4, RX_WMark = 3 MSize = 4, RX_WMark = 7 MSize = 4, RX_WMark = 11 MSize = 8, RX_WMark = 7 <p>Recommended:</p> <p>MSize = 8, TX_WMark = 8, RX_WMark = 7</p>

Bit	Attr	Reset Value	Description
27:16	RW	0x000	<p>rx_wmark FIFO threshold watermark level when receiving data to card.</p> <p>When FIFO data count reaches greater than this number, DMA/FIFO request is raised. During end of packet, request is generated regardless of threshold programming in order to complete any remaining data.</p> <p>In non-DMA mode, when receiver FIFO threshold (RXDR) interrupt is enabled, then interrupt is generated instead of DMA request. During end of packet, interrupt is not generated if threshold programming is larger than any remaining data. It is responsibility of host to read remaining bytes on seeing Data Transfer Done interrupt.</p> <p>In DMA mode, at end of packet, even if remaining bytes are less than threshold, DMA request does single transfers to flush out any remaining bytes before Data Transfer Done interrupt is set.</p> <p>12 bits-1 bit less than FIFO-count of status register, which is 13 bits.</p> <p>Limitation: RX_WMark <= FIFO_DEPTH-2</p> <p>Recommended: (FIFO_DEPTH/2) - 1; (means greater than (FIFO_DEPTH/2) - 1)</p> <p>NOTE: In DMA mode during CCS time-out, the DMA does not generate the request at the end of packet, even if remaining bytes are less than threshold. In this case, there will be some data left in the FIFO. It is the responsibility of the application to reset the FIFO after the CCS timeout.</p>
15:12	RO	0x0	reserved

Bit	Attr	Reset Value	Description
11:0	RW	0x000	<p>tx_wmark FIFO threshold watermark level when transmitting data to card.</p> <p>When FIFO data count is less than or equal to this number, DMA/FIFO request is raised. If Interrupt is enabled, then interrupt occurs. During end of packet, request or interrupt is generated, regardless of threshold programming.</p> <p>In non-DMA mode, when transmit FIFO threshold (TXDR) interrupt is enabled, then interrupt is generated instead of DMA request. During end of packet, on last interrupt, host is responsible for filling FIFO with only required remaining bytes (not before FIFO is full or after CIU completes data transfers, because FIFO may not be empty).</p> <p>In DMA mode, at end of packet, if last transfer is less than burst size, DMA controller does single cycles until required bytes are transferred.</p> <p>12 bits -1 bit less than FIFO-count of status register, which is 13 bits.</p> <p>Limitation: TX_WMark >= 1;</p> <p>Recommended: FIFO_DEPTH/2; (means less than or equal to FIFO_DEPTH/2)</p>

SDMMC_CDETECT

Address: Operational Base + offset (0x0050)

Card-detect register

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RO	0x0	card_detect_n Value on card_detect_n input ports; read-only bits. 0 represents presence of card.

SDMMC_WRTPRT

Address: Operational Base + offset (0x0054)

Write-protect register

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	write_protect Value on card_write_prt input port. 1 represents write protection.

SDMMC_TCBCNT

Address: Operational Base + offset (0x005c)

Transferred CIU card byte count

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	<p>trans_card_byte_count Number of bytes transferred by CIU unit to card.</p> <p>In 32-bit or 64-bit AMBA data-bus-width modes, register should be accessed in full to avoid read-coherency problems. In 16-bit AMBA data-bus-width mode, internal 16-bit coherency register is implemented. User should first read lower 16 bits and then higher 16 bits. When reading lower 16 bits, higher 16 bits of counter are stored in temporary register. When higher 16 bits are read, data from temporary register is supplied.</p> <p>Both TCBCNT and TBBCNT share same coherency register.</p> <p>When AREA_OPTIMIZED parameter is 1, register should be read only after data transfer completes; during data transfer, register returns 0.</p>

SDMMC_TBBCNT

Address: Operational Base + offset (0x0060)

Transferred host/DMA to/from BIU-FIFO byte count

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	<p>trans_fifo_byte_count Number of bytes transferred between Host/DMA memory and BIU FIFO.</p> <p>In 32-bit or 64-bit AMBA data-bus-width modes, register should be accessed in full to avoid read-coherency problems. In 16-bit AMBA data-bus-width mode, internal 16-bit coherency register is implemented. User should first read lower 16 bits and then higher 16 bits. When reading lower 16 bits, higher 16 bits of counter are stored in temporary register. When higher 16 bits are read, data from temporary register is supplied.</p> <p>Both TCBCNT and TBBCNT share same coherency register.</p>

SDMMC_DEBNCE

Address: Operational Base + offset (0x0064)

Card detect debounce register

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved

Bit	Attr	Reset Value	Description
23:0	RW	0xffffffff	debounce_count Number of host clocks (clk) used by debounce filter logic; typical debounce time is 5-25 ms.

SDMMC_USRID

Address: Operational Base + offset (0x0068)

User ID register

Bit	Attr	Reset Value	Description
31:0	RW	0x07967797	usrid User identification register; value set by user. Default reset value can be picked by user while configuring core before synthesis. Can also be used as scratch pad register by user. The default value is determined by Configuration Value.

SDMMC_VERID

Address: Operational Base + offset (0x006c)

Synopsys version ID register

Bit	Attr	Reset Value	Description
31:0	RO	0x5342270a	verid Version identification register; register value is hard-wired. Can be read by firmware to support different versions of core.

SDMMC_HCON

Address: Operational Base + offset (0x0070)

Hardware Configuration Register

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	<p>HCON Configuration Dependent. Hardware configurations selected by user before synthesizing core. Register values can be used to develop configuration-independent software drivers.</p> <ul style="list-style-type: none"> [0]: CARD_TYPE <ul style="list-style-type: none"> 0: MMC_ONLY 1: SD_MMC [5:1]: NUM_CARDS - 1 [6]: H_BUS_TYPE <ul style="list-style-type: none"> 0: APB 1: AHB [9:7]: H_DATA_WIDTH <ul style="list-style-type: none"> 000: 16 bits 001: 32 bits 010: 64 bits others: reserved [15:10]: H_ADDR_WIDTH <ul style="list-style-type: none"> 0 to 7: reserved 8: 9 bits 9: 10 bits ... 31: 32 bits 32 to 63: reserved [17:16]: DMA_INTERFACE <ul style="list-style-type: none"> 00: none 01: DW_DMA 10: GENERIC_DMA 11: NON-DW-DMA [20:18]: GE_DMA_DATA_WIDTH <ul style="list-style-type: none"> 000: 16 bits 001: 32 bits 010: 64 bits others: reserved [21]: FIFO_RAM_INSIDE <ul style="list-style-type: none"> 0: outside 1: inside [22]: IMPLEMENT_HOLD_REG <ul style="list-style-type: none"> 0: no hold register 1: hold register [23]: SET_CLK_FALSE_PATH <ul style="list-style-type: none"> 0: no false path 1: false path set [25:24]: NUM_CLK_DIVIDER-1 [26]: AREA_OPTIMIZED <ul style="list-style-type: none"> 0: no area optimization 1: Area optimization

SDMMC_UHS_REG

Address: Operational Base + offset (0x0074)

UHS-1 register

Bit	Attr	Reset Value	Description
31:17	RO	0x0	reserved
16	RW	0x0	<p>ddr_reg DDR mode. Determines the voltage fed to the buffers by an external voltage regulator.</p> <p>0: non-DDR mode 1: DDR mode</p> <p>UHS_REG [16] should be set for card.</p>
15:1	RO	0x0	reserved
0	RW	0x0	<p>volt_reg High Voltage mode. Determines the voltage fed to the buffers by an external voltage regulator.</p> <p>0: buffers supplied with 3.3V Vdd 1: buffers supplied with 1.8V Vdd</p> <p>These bits function as the output of the host controller and are fed to an external voltage regulator. The voltage regulator must switch the voltage of the buffers of a particular card to either 3.3V or 1.8V, depending on the value programmed in the register.</p> <p>VOLT_REG[0] should be set to 1'b1 for card in order to make it operate for 1.8V.</p>

SDMMC_RST_N

Address: Operational Base + offset (0x0078)

Hardware reset register

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x1	<p>card_reset Hardware reset.</p> <p>0: active mode 1: reset</p> <p>These bits cause the cards to enter pre-idle state, which requires them to be re-initialized.</p> <p>CARD_RESET[0] should be set to 1'b1 to reset card.</p>

SDMMC_BMOD

Address: Operational Base + offset (0x0080)

Bus Mode Register

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:11	RO	0x0	reserved
10:8	RO	0x0	<p>PBL Programmable Burst Length. These bits indicate the maximum number of beats to be performed in one IDMAC transaction. The IDMAC will always attempt to burst as specified in PBL each time it starts a Burst transfer on the host bus. The permissible values are 1, 4, 8, 16, 32, 64, 128 and 256. This value is the mirror of MSIZE of FIFOTH register. In order to change this value, write the required value to FIFOTH register. This is an encode value as follows.</p> <ul style="list-style-type: none"> 000 – 1 transfers 001 – 4 transfers 010 – 8 transfers 011 – 16 transfers 100 – 32 transfers 101 – 64 transfers 110 – 128 transfers 111 – 256 transfers <p>Transfer unit is either 16, 32, or 64 bits, based on HDATA_WIDTH. PBL is a read-only value and is applicable only for Data Access; it does not apply to descriptor accesses.</p>
7	RW	0x0	DE IDMAC Enable. When set, the IDMAC is enabled.
6:2	RW	0x00	DSL Descriptor Skip Length. Specifies the number of HWord/Word/Dword (depending on 16/32/64-bit bus) to skip between two unchained descriptors. This is applicable only for dual buffer structure.
1	RW	0x0	FB Fixed Burst. Controls whether the AHB Master interface performs fixed burst transfers or not. When set, the AHB will use only SINGLE, INCR4, INCR8 or INCR16 during start of normal burst transfers. When reset, the AHB will use SINGLE and INCR burst transfer operations.

Bit	Attr	Reset Value	Description
0	RW	0x0	SWR Software Reset. When set, the DMA Controller resets all its internal registers It is automatically cleared after 1 clock cycle

SDMMC_PLDMND

Address: Operational Base + offset (0x0084)

Poll Demand Register

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	PD Poll Demand. If the OWN bit of a descriptor is not set, the FSM goes to the Suspend state. The host needs to write any value into this register for the IDMAC FSM to resume normal descriptor fetch operation. This is a write only register.

SDMMC_DBADDR

Address: Operational Base + offset (0x0088)

Descriptor List Base Address Register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	SDL Start of Descriptor List. Contains the base address of the First Descriptor. The LSB bits [0/1/2:0] for 16/32/64-bit bus-width) are ignored and taken as all-zero by the IDMAC internally. Hence these LSB bits are read-only.

SDMMC_IDSTS

Address: Operational Base + offset (0x008c)

Internal DMAC Status Register

Bit	Attr	Reset Value	Description
31:17	RO	0x0	reserved
16:13	RO	0x0	FSM DMAC FSM present state. 0: DMA_IDLE 1: DMA_SUSPEND 2: DESC_RD 3: DESC_CHK 4: DMA_RD_REQ_WAI 5: DMA_WR_REQ_WAI 6: DMA_RD 7: DMA_WR 8: DESC_CLOSE

Bit	Attr	Reset Value	Description
12:10	RO	0x0	<p>EB Error Bits. Indicates the type of error that caused a Bus Error. Valid only with atal Bus Error bit—IDSTS[2] (IDSTS64[2], in case of 64-bit address configuration) set. This field does not generate an interrupt.</p> <p>1: Host Abort received during transmission 2: Host Abort received during reception Others: Reserved</p>
9	RW	0x0	<p>AIS Abnormal Interrupt Summary. Logical OR of the following: IDSTS[2] Fatal Bus Interrupt IDSTS[4] DU bit Interrupt Only unmasked bits affect this bit. This is a sticky bit and must be cleared each time a corresponding bit that causes AIS to be set is cleared. Writing a 1 clears this bit.</p>
8	RW	0x0	<p>NIS Normal Interrupt Summary. Logical OR of the following: IDSTS[0] Transmit Interrupt IDSTS[1] Receive Interrupt Only unmasked bits affect this bit. This is a sticky bit and must be cleared each time a corresponding bit that causes NIS to be set is cleared. Writing a 1 clears this bit.</p>
7:6	RO	0x0	reserved

Bit	Attr	Reset Value	Description
5	RW	0x0	CES Card Error Summary. Indicates the status of the transaction to/from the card; also present in RINTSTS. Indicates the logical OR of the following bits: <ul style="list-style-type: none"> ■ EBE –End Bit Error ■ RTO –Response Timeout/Boot Ack Timeout ■ RCRC –Response CRC ■ SBE –Start Bit Error ■ DRTO –Data Read Timeout/BDS timeout ■ DCRC –Data CRC for Receive ■ RE –Response Error Writing a 1 clears this bit. The abort condition of the IDMAC depends on the setting of this CES bit. If the CES bit is enabled, then the IDMAC aborts on a “response error”; however, it will not abort if the CES bit is cleared
4	RW	0x0	DU Descriptor Unavailable Interrupt. This bit is set when the descriptor is unavailable due to OWN bit = 0 (DES0[31] =0). Writing a 1 clears this bit.
3	RO	0x0	reserved
2	RW	0x0	FBE Fatal Bus Error Interrupt. Indicates that a Bus Error occurred (IDSTS[12:10]) (IDSTS64[12:10], in case of 64-bit address configuration). When this bit is set, the DMA disables all its bus accesses. Writing a 1 clears this bit.
1	RW	0x0	RI Receive Interrupt. Indicates the completion of data reception for a descriptor. Writing a 1 clears this bit.
0	RW	0x0	TI Transmit Interrupt. Indicates that data transmission is finished for a descriptor. Writing 1 clears this bit

SDMMC_IDINTEN

Address: Operational Base + offset (0x0090)

Internal DMAC Interrupt Enable Register

Bit	Attr	Reset Value	Description
31:10	RO	0x0	reserved

Bit	Attr	Reset Value	Description
9	RW	0x0	AI Abnormal Interrupt Summary Enable. When set, an abnormal interrupt is enabled. This bit enables the following bits: <ul style="list-style-type: none"> ■ IDINTEN[2] Fatal Bus Error Interrupt ■ IDINTEN[4] DU Interrupt
8	RW	0x0	NI Normal Interrupt Summary Enable. When set, a normal interrupt is enabled. When reset, a normal interrupt is disabled. This bit enables the following bits: <ul style="list-style-type: none"> ■ IDINTEN[0] Transmit Interrupt ■ IDINTEN[1] Receive Interrup
7:6	RO	0x0	reserved
5	RW	0x0	CES Card Error summary Interrupt Enable. When set, it enables the Card Interrupt summary
4	RW	0x0	DU Descriptor Unavailable Interrupt. When set along with Abnormal Interrupt Summary Enable, the DU interrupt is enabled
3	RO	0x0	reserved
2	RW	0x0	FBE Fatal Bus Error Enable. When set with Abnormal Interrupt Summary Enable, the Fatal Bus Error Interrupt is enabled. When reset, Fatal Bus Error Enable Interrupt is disabled.
1	RW	0x0	RI Receive Interrupt Enable. When set with Normal Interrupt Summary Enable, Receive Interrupt is enabled. When reset, Receive Interrupt is disabled
0	RW	0x0	TI Transmit Interrupt Enable. When set with Normal Interrupt Summary Enable, Transmit Interrupt is enabled. When reset, Transmit Interrupt is disabled.

SDMMC_DSCADDR

Address: Operational Base + offset (0x0094)

Current Host Descriptor Address Register

Bit	Attr	Reset Value	Description
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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	HDA Host Descriptor Address Pointer. Cleared on reset. Pointer updated by IDMAC during operation. This register points to the start address of the current descriptor read by the IDMAC

SDMMC_BUFAADDR

Address: Operational Base + offset (0x0098)

Current Buffer Descriptor Address Register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	HBA Host Buffer Address Pointer. Cleared on Reset. Pointer updated by IDMAC during operation. This register points to the current Data Buffer Address being accessed by the IDMAC

SDMMC_CARDTHRCTL

Address: Operational Base + offset (0x0100)

Card read threshold enable

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	CardRdThreshold Card Read Threshold size
15:2	RO	0x0	reserved
1	RW	0x0	BsyClrIntEn Busy Clear Interrupt generation: 0: Busy Clear Interrupt disabled 1: Busy Clear Interrupt enabled Note: The application can disable this feature if it does not want to wait for a Busy Clear Interrupt. For example, in a multi-card scenario, the application can switch to the other card without waiting for a busy to be completed. In such cases, the application can use the polling method to determine the status of busy. By default this feature is disabled and backward-compatible to the legacy drivers where polling is used.

Bit	Attr	Reset Value	Description
0	RW	0x0	CardRdThrEn Card Read Threshold Enable. 0: Card Read Threshold disabled 1: Card Read Threshold enabled. Host Controller initiates Read Transfer only if CardRdThreshold amount of space is available in receive FIFO.

SDMMC_BACK_END_POWER

Address: Operational Base + offset (0x0104)

Back-end power

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	back_end_power Back end power 0: Off; Reset 1: Back-end Power supplied to card application

SDMMC_UHS_REG_EXT

Address: Operational Base + offset (0x0108)

UHS Register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Reserved

SDMMC_EMMC_DDR_REG

Address: Operational Base + offset (0x010c)

eMMC 4.5 DDR START Bit Detection Control Register

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	HALF_START_BIT Control for start bit detection mechanism inside DWC_mobile_storage based on duration of start bit; each bit refers to one slot. For eMMC 4.5, start bit can be: 0: Full cycle (HALF_START_BIT = 0) 1: Less than one full cycle (HALF_START_BIT = 1) Set HALF_START_BIT=1 for eMMC 4.5 and above; set to 0 for SD applications.

SDMMC_ENABLE_SHIFT

Address: Operational Base + offset (0x0110)

Enable Phase Shift Register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Reserved

SDMMC_FIFO_BASE

Address: Operational Base + offset (0x0200)

FIFO Base Address

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	fifo_base_addr FIFO base address.

4.5 Interface Description

The interface and IOMUX setting for SDMMC, SDIO0, SDIO1, EMMC are shown as follows.

4.5.1 SDMMC IOMUX

Table 4-8 IOMUX Settings for SDMMC

Module Pin	Direction	Pad Name	IOMUX Setting
sdmmc_cclk	O	IO_SDMMC0clkout_JTAGtdo_SDCAR Dgpio6c4	GRF_GPIO6C_IOMUX[9:8]= 2'b01
sdmmc_ccmd	I/O	IO_SDMMC0cmd_SDCARDgpio6c5	GRF_GPIO6C_IOMUX[11:10]]=2'b01
sdmmc_cdat_a0	I/O	IO_SDMMC0data0_JTAGtms_SDCAR Dgpio6c0	GRF_GPIO6C_IOMUX[1:0]= 2'b01
sdmmc_cdat_a1	I/O	IO_SDMMC0data1_JTAGtrstn_SDCA RDgpio6c1	GRF_GPIO6C_IOMUX[3:2]= 2'b01
sdmmc_cdat_a2	I/O	IO_SDMMC0data2_JTAGtdi_SDCARD gpio6c2	GRF_GPIO6C_IOMUX[5:4]= 2'b01
sdmmc_cdat_a3	I/O	IO_SDMMC0data3_JTAGtck_SDCAR Dgpio6c3	GRF_GPIO6C_IOMUX[7:6]= 2'b01
sdmmc_cdetectn	I	IO_SDMMC0detectn_SDCARDgpio6c6	GRF_GPIO6C_IOMUX[13:12]]=2'b01

4.5.2 SDIO0 IOMUX

Table 4-9 IOMUX Settings for SDIO0

Module Pin	Direction	Pad Name	IOMUX Setting
sdio0_cclk	O	IO_SDIO0clkout_WIFIgpio4d1	GRF_GPIO4D_IOMUX[3:2]=2'b01
sdio0_ccmd	I/O	IO_SDIO0cmd_WIFIgpio4d0	GRF_GPIO4D_IOMUX[1:0]=2'b01
sdio0_cdata0	I/O	IO_SDIO0data0_WIFIgpio4c4	GRF_GPIO4C_IOMUX[9:8]=2'b01
sdio0_cdata1	I/O	IO_SDIO0data1_WIFIgpio4	GRF_GPIO4C_IOMUX[11:10]=2'b

Module Pin	Direction	Pad Name	IOMUX Setting
		c5	01
sdio0_cdata2	I/O	IO_SDIO0data2_WIFIgpio4 c6	GRF_GPIO4C_IOMUX[13:12]=2'b01
sdio0_cdata3	I/O	IO_SDIO0data3_WIFIgpio4 c7	GRF_GPIO4C_IOMUX[15:14]=2'b01
sdio0_cdetectn	I	IO_SDIO0detectn_WIFIgpio4d2	GRF_GPIO4D_IOMUX[5:4]=2'b01
sdio0_wprt	I	IO_SDIO0wrprt_WIFIgpio4d3	GRF_GPIO4D_IOMUX[7:6]=2'b01
sdio0_int_n	I	IO_SDIO0intn_WIFIgpio4d6	GRF_GPIO4D_IOMUX[13:12]=2'b01
sdio0_pwren	O	IO_SDIO0pwren_WIFIgpio4d4	GRF_GPIO4D_IOMUX[9:8]=2'b01
sdio0_bkpwr	O	IO_SDIO0bkpwr_WIFIgpio4d5	GRF_GPIO4D_IOMUX[11:10]=2'b01

4.5.3 SDIO1 IOMUX

Table 4-10 IOMUX Settings for SDIO1

Module Pin	Direction	Pad Name	IOMUX Setting
sdio1_cclk	O	IO_FLASH1csn1_HOSTdout13_MACcrs_SDIO1 clkout_FLASH1gpio4a7	GRF_GPIO4AH_IOMUX[15:12]=4'h4
sdio1_ccmd	I/O	IO_FLASH1csn0_HOSTdout12_MACrxclk_SDIO1cmd_FLASH1gpio4a6	GRF_GPIO4AH_IOMUX[11:8]=4'h4
sdio1_cd ata0	I/O	IO_FLASH1data0_HOSTdout0_MACtxd2_SDIO1data0_FLASH1gpio3d0	GRF_GPIO3DL_IOMUX[3:0]=4'h4
sdio1_cd ata1	I/O	IO_FLASH1data1_HOSTdout1_MACtxd3_SDIO1data1_FLASH1gpio3d1	GRF_GPIO3DL_IOMUX[7:4]=4'h4
sdio1_cd ata2	I/O	IO_FLASH1data2_HOSTdout2_MACrxsd2_SDIO1data2_FLASH1gpio3d2	GRF_GPIO3DL_IOMUX[11:8]=4'h4
sdio1_cd ata3	I/O	IO_FLASH1data3_HOSTdout3_MACrxsd3_SDIO1data3_FLASH1gpio3d3	GRF_GPIO3DL_IOMUX[15:12]=4'h4
sdio1_cdetectn	I	IO_FLASH1data4_HOSTdout4_MACtxd0_SDIO1detectn_FLASH1gpio3d4	GRF_GPIO3DH_IOMUX[3:0]=4'h4
sdio1_wprt	I	IO_FLASH1data5_HOSTdout5_MACtxd1_SDIO1wrprt_FLASH1gpio3d5	GRF_GPIO3DH_IOMUX[7:4]=4'h4
sdio1_int_n	I	IO_FLASH1data7_HOSTdout7_MACrxsd1_SDIO1intn_FLASH1gpio3d7	GRF_GPIO3DH_IOMUX[15:12]=4'h4
sdio1_pwren	O	IO_FLASH1csn2_HOSTdout15_MACtxclk_SDIO1pwren_FLASH1gpio4b1	GRF_GPIO4BL_IOMUX[7:4]=4'h4
sdio1_bkpwr	O	IO_FLASH1data6_HOSTdout6_MACrxsd0_SDIO1bkpwr_FLASH1gpio3d6	GRF_GPIO3DH_IOMUX[11:8]=4'h4

4.5.4 eMMC IOMUX

Table 4-11 IOMUX Settings for eMMC

Module Pin	Direction	Pad Name	IOMUX Setting
emmc_cclk	O	IO_FLASH0dqs_EMMCclkout_FLASH0 gpio3c2	GRF_GPIO3C_IOMUX[5:4]= 2'b10
emmc_ccmd	I/O	IO_FLASH0csn2_EMMCcmd_FLASH0g pio3c0	GRF_GPIO3C_IOMUX[1:0]= 2'b10
emmc_cdata0	I/O	IO_FLASH0data0_EMMCdata0_FLASH 0gpio3a0	GRF_GPIO3A_IOMUX[1:0]= 2'b10
emmc_cdata1	I/O	IO_FLASH0data1_EMMCdata1_FLASH 0gpio3a1	GRF_GPIO3A_IOMUX[3:2]= 2'b10
emmc_cdata2	I/O	IO_FLASH0data2_EMMCdata2_FLASH 0gpio3a2	GRF_GPIO3A_IOMUX[5:4]= 2'b10
emmc_cdata3	I/O	IO_FLASH0data3_EMMCdata3_FLASH 0gpio3a3	GRF_GPIO3A_IOMUX[7:6]= 2'b10
emmc_cdata4	I/O	IO_FLASH0data4_EMMCdata4_FLASH 0gpio3a4	GRF_GPIO3A_IOMUX[9:8]= 2'b10
emmc_cdata5	I/O	IO_FLASH0data5_EMMCdata5_FLASH 0gpio3a5	GRF_GPIO3A_IOMUX[11:10] =2'b10
emmc_cdata6	I/O	IO_FLASH0data6_EMMCdata6_FLASH 0gpio3a6	GRF_GPIO3A_IOMUX[13:12] =2'b10
emmc_cdata7	I/O	IO_FLASH0data7_EMMCdata7_FLASH 0gpio3a7	GRF_GPIO3A_IOMUX[15:14] =2'b10
emmc_rstn	O	IO_FLASH0csn3_EMMCrstnout_FLASH 0gpio3c1	GRF_GPIO3C_IOMUX[3:2]= 2'b10
emmc_pwr_en	O	IO_FLASH0wp_EMMCpwren_FLASH0g pio3b1	GRF_GPIO3B_IOMUX[3:2]= 2'b10

Notes: Direction: **I**- Input, **O**- Output, **I/O**- Input/Output

4.6 Application Notes

4.6.1 Card-Detect and Write-Protect Mechanism

Following figure illustrates how the SD/MMC card detection and write-protect signals are connected. Most of the SD/MMC sockets have card-detect pins. When no card is present, card_detect_n is 1 due to the pull-up. When the card is inserted, the card-detect pin is shorted to ground, which makes card_detect_n go to 0. Similarly in SD cards, when the write-protect switch is toward the left, it shorts the write_protect port to ground.

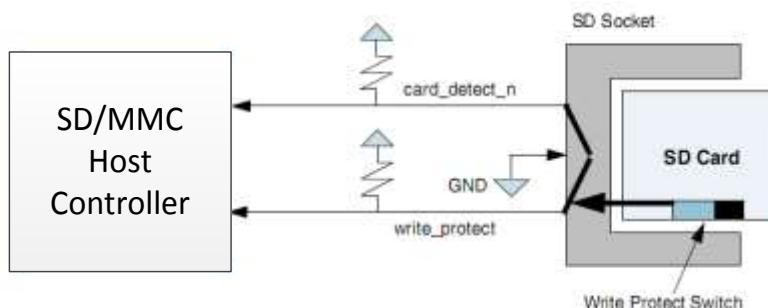


Fig. 4-9 SD/MMC Card-Detect and Write-Protect

4.6.2 SD/MMC Termination Requirement

Following Figure illustrates the SD/MMC termination requirements, which is required to pull up ccmd and cdata lines on the device bus. The recommended specification for pull-up on the ccmd line (R_{CMD}) is 4.7K - 100K for MMC, and 10K - 100K for an SD. The recommended pull-up on the cdata line (R_{DAT}) is 50K - 100K.

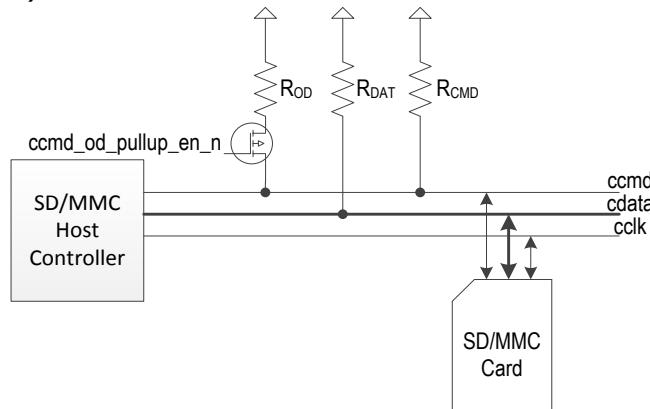


Fig. 4-10 SD/MMC Card Termination

1. R_{CMD} and R_{OD} Calculation

The SD/MMC card enumeration happens at a very low frequency – 100-400KHz. Since the MMC bus is a shared bus between multiple cards, during enumeration open-drive mode is used to avoid bus conflict. Cards that drive 0 win over cards that drive “z”. The pull-up in the command line pulls the bus to 1 when all cards drive “z”. During normal data transfer, the host chooses only one card and the card driver switches to push-pull mode.

For example, if enumeration is done at 400KHz and the total bus capacitance is 200 pf, the pull-up needed during enumeration is:

$$\begin{aligned} 2.2 \text{ RC} &= \text{rise-time} = 1/400\text{KHz} \\ R &= 1/(2.2 * C * 100\text{KHz}) \\ &= 1/(2.2 * 200 * 10^{**-12} * 400 * 10^{**3}) \\ &= 1/(17.6 * 10^{**-5}) \\ &= 5.68\text{K} \end{aligned}$$

The R_{OD} and R_{CMD} should be adjusted in such a way that the effective pull-up is at the maximum 5.68K during enumeration. If there are only a few cards in the bus, a fixed R_{CMD} resistor is sufficient and there is no need for an additional R_{OD} pull-up during enumeration. You should also ensure the effective pull-up will not violate the I_{OL} rating of the drivers.

In SD mode, since each card has a separate bus, the capacitance is less, typically in the order of 20-30pf (host capacitance + card capacitance + trace + socket capacitance). For example, if enumeration is done at 400KHz and the total bus capacitance is 20pf, the pull-up needed during enumeration is:

$$\begin{aligned} 2.2 \text{ RC} &= \text{rise-time} = 1/400\text{KHz} \\ R &= 1/(2.2 * C * 100\text{KHz}) \\ &= 1/(2.2 * 20 * 10^{**-12} * 400 * 10^{**3}) \\ &= 1/(1.76 * 10^{**-5}) \\ &= 56.8\text{K} \end{aligned}$$

Therefore, a fixed 56.8K permanent R_{CMD} is sufficient in SD mode to enumerate the cards. The driver of the SD/MMC on the “command” port needs to be only a push-pull driver. During enumeration, the SD/MMC emulates an open-drain driver by driving only a 0 or a “z” by controlling the ccmd_out and ccmd_out_en signals.

4.6.3 Software/Hardware Restriction

Before issuing a new data transfer command, the software should ensure that the card is not busy due to any previous data transfer command. Before changing the card clock frequency, the software must ensure that there are no data or command transfers in progress.

If the card is enumerated in SDR50, or DDR50 mode, then the application must program the use_hold_reg bit[29] in the CMD register to 1'b0 (phase shift of cclk_in_drv = 0) or 1'b1 (phase shift of cclk_in_drv>0). If the card is enumerated in SDR12 or SDR25 mode, the application must program the use_hold_reg bit[29] in the CMD register to 1'b1.

This programming should be done for all data transfer commands and non-data commands that are sent to the card. When the use_hold_reg bit is programmed to 1'b0, the Host Controller bypasses the Hold Registers in the transmit path. The value of this bit should not be changed when a Command or Data Transfer is in progress. For more details on using use_hold_reg and the implementation requirements for meeting the Card input hold time, refer to "Recommended Usage" in following table.

Table 4-12 Recommended Usage of use_hold_reg

No.	Speed Mode	use_hold_reg	cclk_in (MHz)	clk_in_drv (MHz)	clk_divider	Phase shift
1	SDR104	1'b0	200	200	0	0
2	SDR104	1'b1	200	200	0	Tunable> 0
3	SDR50	1'b0	100	100	0	0
4	SDR50	1'b1	100	100	0	Tunable> 0
5	DDR50 (8bit)	1'b0	100	100	1	0
6	DDR50 (8bit)	1'b1	100	100	1	Tunable> 0
7	DDR50 (4bit)	1'b0	50	50	0	0
8	DDR50 (4bit)	1'b1	50	50	0	Tunable> 0
9	SDR25	1'b1	50	50	0	Tunable> 0
10	SDR12	1'b1	50	50	1	Tunable> 0

To avoid glitches in the card clock outputs, the software should use the following steps when changing the card clock frequency:

- 1) Before disable the clocks, ensure that the card is not busy due to any previous data command. To determine this, check for 0 in bit9 of STATUS register.
- 2) Update the Clock Enable register to disable all clocks. To ensure completion of any previous command before this update, send a command to the CIU to update the clock registers by setting:

- start_cmd bit
- "update clock registers only" bits
- "wait_previous data complete" bit

Wait for the CIU to take the command by polling for 0 on the start_cmd bit.

- 3) Set the start_cmd bit to update the Clock Divider and/or Clock Source registers, and send a command to the CIU in order to update the clock registers; wait for the CIU to take the command.
- 4) Set start_cmd to update the Clock Enable register in order to enable the required clocks and send a command to the CIU to update the clock registers; wait for the CIU to take the command.

In non-DMA mode, while reading from a card, the Data Transfer Over (RINTSTS[3]) interrupt occurs as soon as the data transfer from the card is over. There still could be some data left in the FIFO, and the RX_WMark interrupt may or may not occur, depending on the remaining bytes in the FIFO. Software should read any remaining bytes upon seeing the Data Transfer Over (DTO) interrupt. While using the external DMA interface for reading from a card, the DTO interrupt occurs only after all the data is flushed to memory by the DMA interface unit.

While writing to a card in external DMA mode, if an undefined-length transfer is selected by setting the Byte Count Register to 0, the DMA logic will likely request more data than it will send

to the card, since it has no way of knowing at which point the software will stop the transfer. The DMA request stops as soon as the DTO is set by the CIU.

If the software issues a controller_reset command by setting control register bit[0] to 1, all the CIU state machines are reset; the FIFO is not cleared. The DMA sends all remaining bytes to the host. In addition to a card-reset, if a FIFO reset is also issued, then:

- Any pending DMA transfer on the bus completes correctly
- DMA data read is ignored
- Write data is unknown(x)

Additionally, if dma_reset is also issued, any pending DMA transfer is abruptly terminated. When the DW-DMA is used, the DMA controller channel should also be reset and reprogrammed.

If any of the previous data commands do not properly terminate, then the software should issue the FIFO reset in order to remove any residual data, if any, in the FIFO. After asserting the FIFO reset, you should wait until this bit is cleared.

One data-transfer requirement between the FIFO and host is that the number of transfers should be a multiple of the FIFO data width (32bits). For example, you want to write only 15 bytes to an SD/MMC card (BYTCNT), the host should write 16 bytes to the FIFO or program the DMA to do 16-byte transfers. The software can still program the Byte Count register to only 15, at which point only 15 bytes will be transferred to the card. Similarly, when 15 bytes are read from a card, the host should still read all 16 bytes from the FIFO.

It is recommended that you not change the FIFO threshold register in the middle of data transfers.

4.6.4 Programming Sequence

1. Initialization

Following figure illustrates the initialization flow.

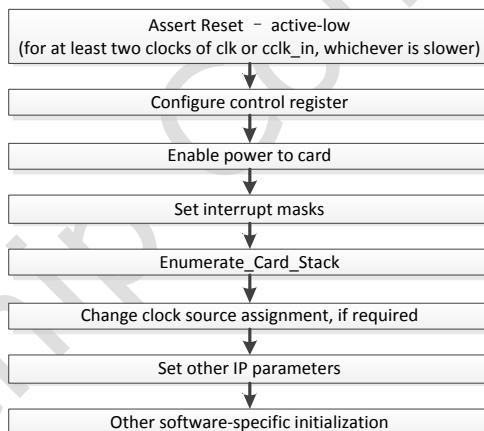


Fig. 4-11 Host Controller Initialization Sequence

Once the power and clocks are stable, reset_n should be asserted(active-low) for at least two clocks of clk or cclk_in, whichever is slower. The reset initializes the registers, ports, FIFO-pointers, DMA interface controls, and state-machines in the design. After power-on reset, the software should do the following:

Configure control register – For MMC mode, enable the open-drain pullup by setting enable_OD_pullup(bit24) in the control register.

Enable power to cards – Before enabling the power, confirm that the voltage setting to the voltage regulators is correct. Enable power to the connected cards by setting the corresponding bit to 1 in the Power Enable register. Wait for the power ramp-up time.

Set masks for interrupts by clearing appropriate bits in the Interrupt Mask register. Set the global int_enable bit of the Control register. It is recommended that you write 0xffff_ffff to the Raw Interrupt register in order to clear any pending interrupts before setting the int_enable bit.

Enumerate card stack – Each card is enumerated according to card type; for details, refer to “Enumerated Card Stack”. For enumeration, you should restrict the clock frequency to 400KHz.

Changing clock source assignment – set the card frequency using the clock-divider and clock-source registers; for details, refer to “Clock Programming”. MMC cards operate at a maximum of 20MHz (at maximum of 52MHz in high-speed mode). SD mode operates at a maximum of 25MHz (at maximum of 50MHz in high-speed mode).

Set other parameters, which normally do not need to be changed with every command, with a typical value such as timeout values in cclk_out according to SD/MMC specifications.

ResponseTimeOut = 0x64

DateTimeOut = highest of one of the following:

$(10*((TAAC*Fop)+(100*NSAC)))$

Host FIFO read/write latency from FIFO empty/full

Set the debounce value to 25ms(default:0xffff) in host clock cycle units in the DEBNCE register.

FIFO threshold value in bytes in the FIFOTH register.

2. Enumerated Card Stack

The card stack does the following:

- Enumerates all connected cards
- Sets the RCA for the connected cards
- Reads card-specific information
- Stores card-specific information locally

Enumeration depends on the operating mode of the SD/MMC card; the card type is first identified and the appropriate card enumeration routine is called.

- 1) Check if the card is connected.
- 2) Clear the card type register to set the card width as a single bit. For the given card number, clear the corresponding bits in the card_type register. Clear the register bit for a 1-bit, 4-bit bus width. For example, for card number=1, clear bit 0 and bit 16 of the card_type register.
- 3) Set clock frequency to $F_{OD}=400\text{KHz}$, maximum – Program clock divider0 (bits 0-7 in the CLKDIV register) value to one-half of the cclk_in frequency divided by 400KHz. For example, if cclk_in is 20MHz, then the value is $20,000/(2*400)=25$.
- 4) Identify the card type; that is, SD, MMC, or SDIO.
 - a. Send CMD5 first. If a response is received, then the card is SDIO
 - b. If not, send CMD8 with the following Argument

Bit[31:12] = 20'h0 //reserved bits
 Bit[11:8] = 4'b0001 //VHS value
 Bit[7:0] = 8'b10101010 //Preferred Check Pattern by SD2.0
 - c. If Response is received the card supports High Capacity SD2.0 then send ACMD41 with the following Argument

Bit[31] = 1'b0; //Reserved bits
 Bit[30] = 1'b1; //High Capacity Status
 Bit[29:24] = 6'h0; //Reserved bits
 Bit[23:0] = Supported Voltage Range
 - d. If Response is received for ACMD41 then the card is SD. Otherwise the card is MMC.
 - e. If response is not received for initial CMD8 then card does not support High Capacity SD2.0, then issue CMD0 followed by ACMD41 with the following Argument

Bit[31] = 1'b0; //Reserved bits
 Bit[30] = 1'b0; //High Capacity Status
 Bit[29:24] = 6'h0; //Reserved bits
 Bit[23:0] = Supported Voltage Range
- 5) Enumerate the card according to the card type.
- 6) Use a clock source with a frequency = F_{OD} (that is, 400KHz) and use the following enumeration command sequence:
 - SD card – Send CMD0, CMD8, ACMD41, CMD2, CMD3.
 - MMC – Send CMD0, CMD1, CMD2, CMD3.

3. Power Control

You can implement power control using the following registers, along with external circuitry:

Control register bits card_voltage_a and card_voltage_b – Status of these bits is reflected at the IO pins. The bits can be used to generate or control the supply voltage that the memory cards require.

Power enable register – Control power to individual cards.

Programming these two register depends on the implemented external circuitry. While turning on or off the power enable, you should confirm that power supply settings are correct. Power to all cards usually should be disabled while switching off the power.

4. Clock Programming

The Host Controller supports one clock sources. The clock to an individual card can be enabled or disabled. Registers that support this are:

CLKDIV – Programs individual clock source frequency. CLKDIV limited to 0 or 1 is recommended.

CLKSRC – Assign clock source for each card.

CLKENA – Enables or disables clock for individual card and enables low-power mode, which automatically stops the clock to a card when the card is idle for more than 8 clocks.

The Host Controller loads each of these registers only when the start_cmd bit and the Update_clk_regs_only bit in the CMD register are set. When a command is successfully loaded, the Host Controller clears this bit, unless the Host Controller already has another command in the queue, at which point it gives an HLE(Hardware Locked Error).

Software should look for the start_cmd and the Update_clk_regs_only bits, and should also set the wait_prvdata_complete bit to ensure that clock parameters do not change during data transfer. Note that even though start_cmd is set for updating clock registers, the Host Controller does not raise a command_done signal upon command completion.

The following shows how to program these registers:

Confirm that no card is engaged in any transaction; if there is a transaction, wait until it finishes.

Stop all clocks by writing xxxx0000 to the CLKENA register. Set the start_cmd, Update_clk_regs_only, and wait_prvdata_complete bits in the CMD register. Wait until start_cmd is cleared or an HLE is set; in case of an HLE, repeat the command.

Program the CLKDIV and CLKSRC registers, as required. Set the start_cmd, Update_clk_regs_only, and wait_prvdata_complete bits in the CMD register. Wait until start_cmd is cleared or an HLE is set; in case of an HLE, repeat the command.

Re-enable all clocks by programming the CLKENA register. Set the start_cmd, Update_clk_regs_only, and wait_prvdata_complete bits in the CMD register. Wait until start_cmd is cleared or an HLE is set; in case of an HLE, repeat the command.

5. No-Data Command With or Without Response Sequence

To send any non-data command, the software needs to program the CMD register @0x2C and the CMDARG register @0x28 with appropriate parameters. Using these two registers, the Host Controller forms the command and sends it to the command bus. The Host Controller reflects the errors in the command response through the error bits of the RINTSTS register.

When a response is received – either erroneous or valid – the Host Controller sets the command_done bit in the RINTSTS register. A short response is copied in Response Register0, while along response is copied to all four response registers @0x30, 0x34, 0x38, and 0x3C. The Response3 register bit 31 represents the MSB, and the Response0 register bit 0 represents the LSB of a long response.

For basic commands or non-data commands, follow these steps:

Program the Command register @0x28 with the appropriate command argument parameter.

Program the Command register @0x2C with the settings in following table.

Table 4-13 Command Settings for No-Data Command

Parameter	Value	Description
Default		
start_cmd	1	-
use_hold_reg	1/0	Choose value based on speed mode being used; ref to "use_hold_reg" on CMD register
update_clk_regs_only	0	No clock parameters update command

Parameter	Value	Description
data_expected	0	No data command
card number	0	Actual card number(one controller only connect one card, the num is No. 0)
cmd_index	command-index	-
send_initialization	0	Can be 1, but only for card reset commands, such as CMD0
stop_abort_cmd	0	Can be 1 for commands to stop data transfer, such as CMD12
response_length	0	Can be 1 for R2(long) response
response_expect	1	Can be 0 for commands with no response; for example, CMD0, CMD4, CMD15, and so on
User-selectable		
wait_prvdata_complete	1	Before sending command on command line, host should wait for completion of any data command in process, if any (recommended to always set this bit, unless the current command is to query status or stop data transfer when transfer is in progress)
check_response_crc	1	If host should crosscheck CRC of response received

Wait for command acceptance by host. The following happens when the command is loaded into the Host Controller:

- Host Controller accepts the command for execution and clears the start_cmd bit in the CMD register, unless one command is in process, at which point the Host Controller can load and keep the second command in the buffer.
- If the Host Controller is unable to load the command – that is, a command is already in progress, a second command is in the buffer, and a third command is attempted – then it generates an HLE (hardware-locked error).

Check if there is an HLE.

Wait for command execution to complete. After receiving either a response from a card or response timeout, the Host Controller sets the command_done bit in the RINTSTS register. Software can either poll for this bit or respond to a generated interrupt.

Check if response_timeout error, response_CRC error, or response error is set. This can be done either by responding to an interrupt raised by these errors or by polling bits 1, 6, and 8 from the RINTSTS register @0x44. If no response error is received, then the response is valid. If required, the software can copy the response from the response registers @0x30-0x3C.

Software should not modify clock parameters while a command is being executed.

Data Transfer Commands

Data transfer commands transfer data between the memory card and the Host Controller. To send a data command, the Host Controller needs a command argument, total data size, and block size. Software can receive or send data through the FIFO.

Before a data transfer command, software should confirm that the card is not busy and is in a transfer state, which can be done using the CMD13 and CMD7 commands, respectively.

For the data transfer commands, it is important that the same bus width that is programmed in the card should be set in the card type register @0x18.

The Host Controller generates an interrupt for different conditions during data transfer, which are reflected in the RINTSTS register @0x44 as:

Data_Transfer_Over (bit 3) – When data transfer is over or terminated. If there is a response timeout error, then the Host Controller does not attempt any data transfer and the “Data Transfer Over” bit is never set.

Transmit_FIFO_Data_request (bit 4) – FIFO threshold for transmitting data was reached; software is expected to write data, if available, in FIFO.

Receive_FIFO_Data_request (bit 5) – FIFO threshold for receiving data was reached; software is expected to read data from FIFO.

Data starvation by Host timeout (bit 10) – FIFO is empty during transmission or is full during reception. Unless software writes data for empty condition or reads data for full

condition, the Host Controller cannot continue with data transfer. The clock to the card has been stopped.

Data read timeout error (bit 9) – Card has not sent data within the timeout period.

Data CRC error (bit 7) – CRC error occurred during data reception.

Start bit error (bit 13) – Start bit was not received during data reception.

End bit error (bit 15) – End bit was not received during data reception or for a write operation; a CRC error is indicated by the card.

Conditions 6, 7, and 8 indicate that the received data may have errors. If there was a response timeout, then no data transfer occurred.

Single-Block or Multiple-Block Read

Steps involved in a single-block or multiple-block read are:

Write the data size in bytes in the BYTCNT register @0x20.

Write the block size in bytes in the BLKSIZ register @0x1C. The Host Controller expects data from the card in blocks of size BLKSIZ each.

Program the CMDARG register @0x28 with the data address of the beginning of a data read.

Program the Command register with the parameters listed in following table. For SD and MMC cards, use CMD17 for a single-block read and CMD18 for a multiple-block read. For SDIO cards, use CMD53 for both single-block and multiple-block transfers.

Table 4-14 Command Setting for Single or Multiple-Block Read

Parameter	Value	Description
Default		
start_cmd	1	-
use_hold_reg	1/0	Choose value based on speed mode being used; ref to "use_hold_reg" on CMD register
update_clk_regs_only	0	No clock parameters update command
card number	0	Actual card number (one controller only connect one card, the num is No.0)
send_initialization	0	Can be 1, but only for card reset commands, such as CMD0
stop_abort_cmd	0	Can be 1 for commands to stop data transfer, such as CMD12
send_auto_stop	0/1	-
transfer_mode	0	Block transfer
read_write	0	Read from card
data_expected	1	Data command
response_length	0	Can be 1 for R2(long) response
response_expect	1	Can be 0 for commands with no response; for example, CMD0, CMD4, CMD15, and so on
User-selectable		
cmd_index	command-index	-
wait_prvdata_complete	1	0- Sends command immediately 1- Sends command after previous data transfer ends
check_response_crc	1	0- Host Controller should not check response CRC 1- Host Controller should check response CRC

After writing to the CMD register, the Host Controller starts executing the command; when the command is sent to the bus, the command_done interrupt is generated.

Software should look for data error interrupts; that is, bits 7, 9, 13, and 15 of the RINTSTS register. If required, software can terminate the data transfer by sending a STOP command.

Software should look for Receive_FIFO_Data_request and/or data starvation by host timeout conditions. In both cases, the software should read data from the FIFO and make space in the FIFO for receiving more data.

When a Data_Transfer_Over interrupt is received, the software should read the remaining data from the FIFO.

Single-Block or Multiple-Block Write

Steps involved in a single-block or multiple-block write are:

Write the data size in bytes in the BYTCNT register @0x20.

Write the block size in bytes in the BLKSIZ register @0x1C; the Host Controller sends data in blocks of size BLKSIZ each.

Program CMDARG register @0x28 with the data address to which data should be written.

Write data in the FIFO; it is usually best to start filling data the full depth of the FIFO.

Program the Command register with the parameters listed in following table.

Table 4-15 Command Settings for Single or Multiple-Block Write

Parameter	Value	Description
Default		
start_cmd	1	-
use_hold_reg	1/0	Choose value based on speed mode being used; ref to "use_hold_reg" on CMD register
update_clk_regs_only	0	No clock parameters update command
card number	0	Actual card number(one controller only connect one card, the num is No. 0)
send_initialization	0	Can be 1, but only for card reset commands, such as CMD0
stop_abort_cmd	0	Can be 1 for commands to stop data transfer, such as CMD12
send_auto_stop	0/1	-
transfer_mode	0	Block transfer
read_write	1	Write to card
data_expected	1	Data command
response_length	0	Can be 1 for R2(long) response
response_expect	1	Can be 0 for commands with no response; for example, CMD0, CMD4, CMD15, and so on
User-selectable		
cmd_index	command-index	-
wait_prvdata_complete	1	0- Sends command immediately 1- Sends command after previous data transfer ends
check_response_crc	1	0- Host Controller should not check response CRC 1- Host Controller should check response CRC

After writing to the CMD register, Host Controller starts executing a command; when the command is sent to the bus, a command_done interrupt is generated.

Software should look for data error interrupts; that is, for bits 7, 9, and 15 of the RINTSTS register. If required, software can terminate the data transfer by sending the STOP command.

Software should look for Transmit_FIFO_Data_Request and/or timeout conditions from data starvation by the host. In both cases, the software should write data into the FIFO.

When a Data_Transfer_Over interrupt is received, the data command is over. For an open-ended block transfer, if the byte count is 0, the software must send the STOP command. If the byte count is not 0, then upon completion of a transfer of a given number of bytes, the Host Controller should send the STOP command, if necessary. Completion of the AUTO-STOP command is reflected by the Auto_command_done interrupt – bit 14 of the RINTSTS register. A response to AUTO_STOP is stored in RESP1 @0x34.

Stream Read

A stream read is like the block read mentioned in "Single-Block or Multiple-Block Read", except for the following bits in the Command register:

```
transfer_mode = 1; //Stream transfer
cmd_index = CMD20;
```

A stream transfer is allowed for only a single-bit bus width.

Stream Write

A stream write is exactly like the block write mentioned in "Single-Block or Multiple-Block Write", except for the following bits in the Command register:

```
transfer_mode = 1;//Stream transfer
cmd_index = CMD11;
```

In a stream transfer, if the byte count is 0, then the software must send the STOP command. If the byte count is not 0, then when a given number of bytes completes a transfer, the Host Controller sends the STOP command. Completion of this AUTO_STOP command is reflected by the Auto_command_done interrupt. A response to an AUTO_STOP is stored in the RESP1 register@0x34.

A stream transfer is allowed for only a single-bit bus width.

Packed Commands

In order to reduce overhead, read and write commands can be packed in groups of commands—either all read or all write—that transfer the data for all commands in the group in one transfer on the bus.

Packed commands can be of two types:

- Packed Write: CMD23 →CMD25
- Packed Read: CMD23 → CMD25 → CMD23 → CMD18

Packed commands are put in packets by the application software and are transparent to the core.

Sending Stop or Abort in Middle of Transfer

The STOP command can terminate a data transfer between a memory card and the Controller, while the ABORT command can terminate an I/O data transfer for only the SDIO_IOONLY and SDIO_COMBO cards.

Send STOP command – Can be sent on the command line while a data transfer is in progress; this command can be sent at any time during a data transfer.

You can also use an additional setting for this command in order to set the Command register bits (5-0) to CMD12 and set bit 14 (stop_abort_cmd) to 1. If stop_abort_cmd is not set to 1, the Controller does not know that the user stopped a data transfer. Reset bit 13 of the Command register (wait_prvdata_complete) to 0 in order to make the Controller send the command at once, even though there is a data transfer in progress.

Send ABORT command – Can be used with only an SDIO_IOONLY or SDIO_COMBO card. To abort the function that is transferring data, program the function number in ASx bits (CCCR register of card, address 0x06, bits (0-2) using CMD52.

Suspend or Resume Sequence

In an SDIO card, the data transfer between an I/O function and the Controller can be temporarily halted using the SUSPEND command; this may be required in order to perform a high-priority data transfer with another function. When desired, the data transfer can be resumed using the RESUME command.

The following functions can be implemented by programming the appropriate bits in the CCCR register (Function 0) of the SDIO card. To read from or write to the CCCR register, use the CMD52 command.

SUSPEND data transfer – Non-data command

Check if the SDIO card supports the SUSPEND/RESUME protocol; this can be done through the SBS bit in the CCCR register @0x08 of the card.

Check if the data transfer for the required function number is in process; the function number that is currently active is reflected in bits 0-3 of the CCCR register @0x0D. Note that if the BS bit (address 0xc::bit 0) is 1, then only the function number given by the FSx bits is valid.

To suspend the transfer, set BR (bit 2) of the CCCR register @0x0C.

Poll for clear status of bits BR (bit 1) and BS (bit 0) of the CCCR @0x0C. The BS (Bus Status) bit is 1 when the currently-selected function is using the data bus; the BR (Bus Release) bit remains 1 until the bus release is complete. When the BR and BS bits are 0, the data transfer from the selected function has been suspended.

RESUME data transfer – This is a data command

Check that the card is not in a transfer state, which confirms that the bus is free for data transfer.

If the card is in a disconnect state, select it using CMD7. The card status can be retrieved in response to CMD52/CMD53 commands.

Check that a function to be resumed is ready for data transfer; this can be confirmed by reading the RFx flag in CCCR @0x0F. If RF = 1, then the function is ready for data transfer. To resume transfer, use CMD52 to write the function number at FSx bits (0-3) in the CCCR register @0x0D. Form the command argument for CMD52 and write it in CMDARG @0x28. Write the block size in the BLKSIZ register @0x1C; data will be transferred in units of this block size.

Write the byte count in the BYTCNT register @0x20. This is the total size of the data; that is, the remaining bytes to be transferred. It is the responsibility of the software to handle the data.

Program Command register; similar to a block transfer.

When the Command register is programmed, the command is sent and the function resumes data transfer. Read the DF flag (Resume Data Flag). If it is 1, then the function has data for the transfer and will begin a data transfer as soon as the function or memory is resumed. If it is 0, then the function has no data for the transfer.

If the DF flag is 0, then in case of a read, the Host Controller waits for data. After the data timeout period, it gives a data timeout error.

Read_Wait Sequence

Read_wait is used with only the SDIO card and can temporarily stall the data transfer—either from function or memory—and allow the host to send commands to any function within the SDIO device. The host can stall this transfer for as long as required. The Host Controller provides the facility to signal this stall transfer to the card. The steps for doing this are:

Check if the card supports the read_wait facility; read SRW (bit 2) of the CCCR register @0x08. If this bit is 1, then all functions in the card support the read_wait facility. Use CMD52 to read this bit.

If the card supports the read_wait signal, then assert it by setting the read_wait (bit 6) in the CTRL register @0x00.

Clear the read_wait bit in the CTRL register.

Controller/DMA/FIFO Reset Usage

Controller reset – Resets the controller by setting the controller_reset bit (bit 0) in the CTRL register; this resets the CIU and state machines, and also resets the BIU-to-CIU interface. Since this reset bit is self-clearing, after issuing the reset, wait until this bit is cleared.

FIFO reset - Resets the FIFO by setting the fifo_reset bit (bit 1) in the CTRL register; this resets the FIFO pointers and counters of the FIFO. Since this reset bit is self-clearing, after issuing the reset, wait until this bit is cleared.

In external DMA transfer mode, even when the FIFO pointers are reset, if there is a DMA transfer in progress, it could push or pop data to or from the FIFO; the DMA itself completes correctly. In order to clear the FIFO, the software should issue an additional FIFO reset and clear any FIFO underrun or overrun errors in the RAWINTS register caused by the DMA transfers after the FIFO was reset.

Card Read Threshold

When an application needs to perform a Single or Multiple Block Read command, the application must program the CardThrCtl register with the appropriate Card Read Threshold size (CardRdThreshold) and set the Card Read Threshold Enable (CardRdThrEnable) bit to 1'b1. This additional programming ensures that the Host controller sends a Read Command only if there is space equal to the CardRDThreshold available in the Rx FIFO. This in turn ensures that the card clock is not stopped in the middle a block of data being transmitted from the card. The Card Read Threshold can be set to the block size of the transfer, which guarantees that there is a minimum of one block size of space in the RxFIFO before the controller enables the card clock. The Card Read Threshold is required when the Round Trip Delay is greater than 0.5cclk_in period.

Error Handling

The Host Controller implements error checking; errors are reflected in the RAWINTS

register@0x44 and can be communicated to the software through an interrupt, or the software can poll for these bits. Upon power-on, interrupts are disabled (int_enable in the CTRL register is 0), and all the interrupts are masked (bits 0-31 of the INTMASK register; default is 0).

Error handling:

- Response and data timeout errors – For response timeout, software can retry the command. For data timeout, the Host Controller has not received the data start bit – either for the first block or the intermediate block – within the timeout period, so software can either retry the whole data transfer again or retry from a specified block onwards. By reading the contents of the TCBCNT later, the software can decide how many bytes remain to be copied.
- Response errors – Set when an error is received during response reception. In this case, the response that copied in the response registers is invalid. Software can retry the command.
- Data errors – Set when error in data reception are observed; for example, data CRC, start bit not found, end bit not found, and so on. These errors could be set for any block-first block, intermediate block, or last block. On receipt of an error, the software can issue a STOP or ABORT command and retry the command for either whole data or partial data.
- Hardware locked error – Set when the Host Controller cannot load a command issued by software. When software sets the start_cmd bit in the CMD register, the Host Controller tries to load the command. If the command buffer is already filled with a command, this error is raised. The software then has to reload the command.
- FIFO underrun/overrun error – If the FIFO is full and software tries to write data in the FIFO, then an overrun error is set. Conversely, if the FIFO is empty and the software tries to read data from the FIFO, an underrun error is set. Before reading or writing data in the FIFO, the software should read the fifo_empty or fifo_full bits in the Status register.
- Data starvation by host timeout – Raised when the Host Controller is waiting for software intervention to transfer the data to or from the FIFO, but the software does not transfer within the stipulated timeout period. Under this condition and when a read transfer is in process, the software should read data from the FIFO and create space for further data reception. When a transmit operation is in process, the software should fill data in the FIFO in order to start transferring data to the card.
- CRC Error on Command – If a CRC error is detected for a command, the CE-ATA device does not send a response, and a response timeout is expected from the Host Controller. The ATA layer is notified that an MMC transport layer error occurred.

Notes: During a multiple-block data transfer, if a negative CRC status is received from the device, the data path signals a data CRC error to the BIU by setting the data CRC error bit in the RINTSTS register. It then continues further data transmission until all the bytes are transmitted.

4.6.5 Voltage Switching

The Host Controller supports SD 3.0 Ultra High Speed (UHS-1) and is capable of voltage switching in SD-mode, which can be applied to SD High-Capacity (SDHC) and SD Extended Capacity (SDXC) cards. UHS-1 supports only 4-bit mode.

SD 3.0 UHS-1 supports the following transfer speed modes for UHS-50 and/or UHS-104 cards:

- DS – default-speed up to 25MHz, 3.3V signaling
- HS – high-speed up to 50MHz, 3.3V signaling
- SDR12 – SDR up to SDR 25MHz, 1.8V signaling
- SDR25 – SDR up to 50MHz, 1.8V signaling
- SDR50 – SDR up to 100MHz, 1.8V signaling
- DDR50 – DDR up to 50MHz, 1.8V signaling

Voltage selection can be done in only SD mode. The first CMD0 selects the bus mode-either SD mode or SPI mode. The card must be in SD mode in order for 1.8V signaling mode to apply, during which time the card cannot be switched to SPI mode or 3.3V signaling without a power cycle.

If the System BIOS in an embedded system already knows that it is connected to an SD 3.0 card, then the driver programs the Controller to initiate ACMD41. The software knows from the response of ACMD41 whether or not the card supports voltage switching to 1.8V.

If bit 32 of ACMD41 response is 1'b1: card supports voltage switching and next command-CMD11-invokes voltage switching sequence. After CMD11 is started, the software must program the VOLT_REG register in the CSR space with the appropriate card number.

If bit 32 of ACMD41 response is 1'b0: card does not support voltage switching and CMD11 should not be started.

If the card and host controller accept voltage switching, then they support UHS-1 modes of data transfer. After the voltage switch to 1.8V, SDR12 is the default speed.

Since the UHS-1 can be used in only 4-bit mode, the software must start ACMD6 and change the card data width to 4-bit mode; ACMD6 is driven in any of the UHS-1 speeds. If the host wants to select the DDR mode of data transfer, then the software must program the DDR_REG register in the CSR space with the appropriate card number.

To choose from any of the SDR or DDR modes, appropriate values should be programmed in the CLKDIV register.

Voltage Switch Operation

The Voltage Switch operation must be performed in SD mode only.

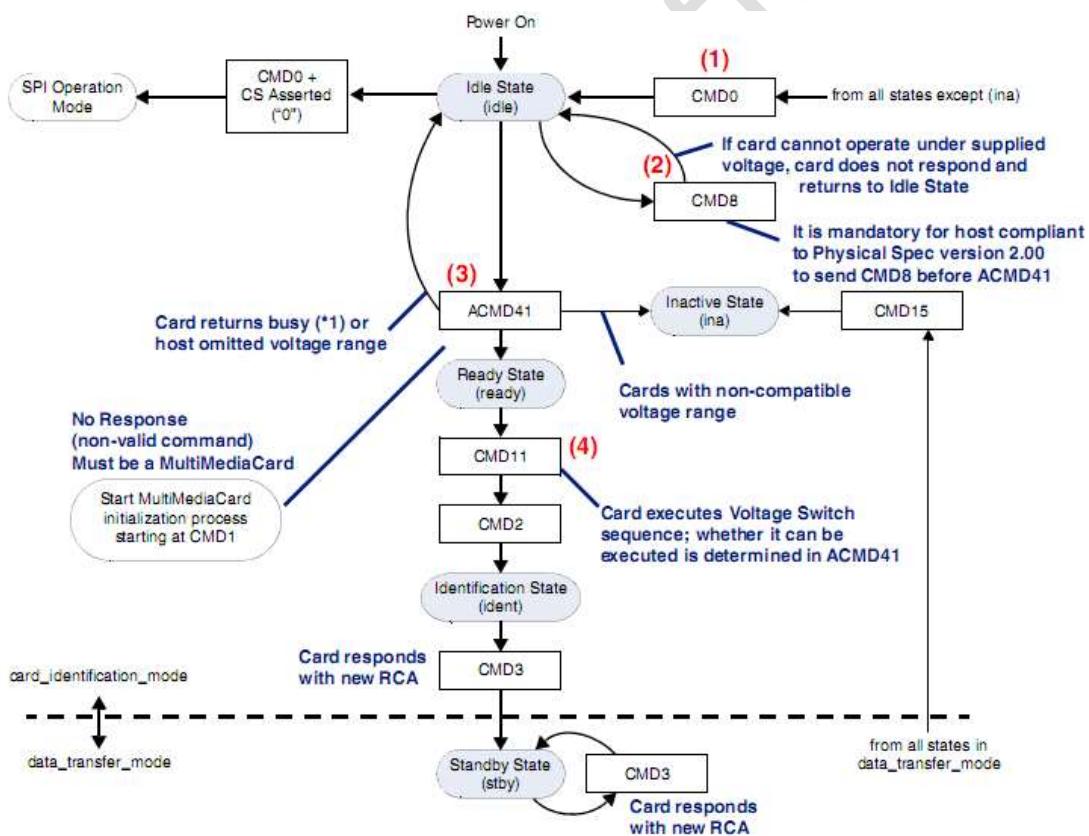


Fig. 4-12 Voltage Switching Command Flow Diagram

The following outlines the steps for the voltage switch programming sequence

Software Driver starts CMD0, which selects the bus mode as SD.

After the bus is in SD card mode, CMD8 is started in order to verify if the card is compatible with the SD Memory Card Specification, Version 2.00. CMD8 determines if the card is capable of working within the host supply voltage specified in the VHS (19:16) field of the CMD; the card supports the current host voltage if a response to CMD8 is received.

ACMD 41 is started. The response to this command informs the software if the card

supports voltage switching; bits 38, 36, and 32 are checked by the card argument of ACMD41; refer to following figure.

47	46	45-40	39	38	37	36	35-33	32	31-16	15-08	07-01	00
S	D	Index	Busy 31	HCS 30	(FB) 29	XPC 28	Reserved 27-25	S18R 24	OCR 23-08	Reserved 07-00	CRC7	E
0	1	101001	0	X	0	X	000	X	xxxxh	0000000	xxxxxx	1

Host Capacity Support
 0b: SDSC-only Host
 1b: SDHC or SDXC supported

SCXC Power Control
 0b: Power saving
 1b: Maximum performance

S18R: Switching to 1.8V Request
 0b: Use current signal voltage
 1b: Switch to 1.8V signal voltage

Fig. 4-13 ACMD41 Argument

Bit 30 informs the card if host supports SDHC/SDXC or not; this bit should be set to 1'b1.
 Bit 28 can be either 1 or 0.

Bit 24 should be set to 1'b1, indicating that the host is capable of voltage switching; refer to Figure 1-16.

47	46	45-40	39	38	37	36-33	32	31-16	15-08	07-01	00	
S	D	Index	Busy 31	CCS 30	Rsvd 29	Reserved 28-25	S18R 24	OCR 23-08	Reserved 07-00	CRC7	E	
0	0	111111	X	X	0	0000	X	xxxxh	0000000	1111111	1	

Busy Status
 0b: On Initialization
 1b: Initialization complete

Card Capacity Status
 0b: SDSC
 1b: SCHC or SCXC

S18R: Switching to 1.8V Accepted
 0b: Continues current voltage signalling
 1b: Ready for switching signal voltage

Fig. 4-14 ACMD41 Response(R3)

Bit 30 – If set to 1'b1, card supports SDHC/SDXC; if set to 1'b0, card supports only SDSC
 Bit 24 – If set to 1'b1, card supports voltage switching and is ready for the switch
 Bit 31 – If set to 1'b1, initialization is over; if set to 1'b0, means initialization in process
 If the card supports voltage switching, then the software must perform the steps discussed for either the “Voltage Switch Normal Scenario” or the “Voltage Switch Error Scenario”.

Voltage Switch Normal Scenario

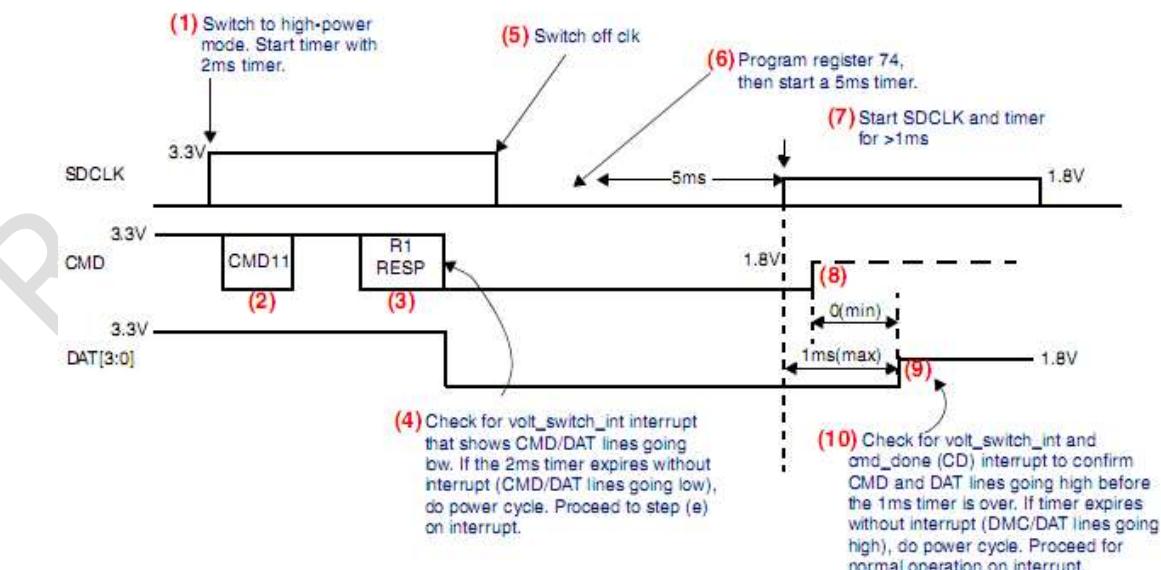


Fig. 4-15 Voltage Switch Normal Scenario

The host programs CLKENA—cclk_low_power register—with zero (0) for the corresponding card, which makes the host controller move to high-power mode. The application should start a timer with a recommended value of 2ms; this value of 2 ms is determined as below:

Total clk required for CMD11 = 48 clks

Total clk required for RESP R1 = 48 clks

Maximum clk delay between MCD11 end to start of RESP1 = 60 clks

Total = 48+48 + 60 = 160

Minimum frequency during enumeration is 100 KHz; that is, 10us

Total time = 160 * 10us = 1600us = 1. 6ms ~ 2ms

The host issues CMD11 to start the voltage switch sequence. Set bit 28 to 1'b1 in CMD when setting CMD11; for more information on setting bits, refer to "Boot Operation".

The card returns R1 response; the host controller does not generate cmd_done interrupt on receiving R1 response.

The card drives CMD and DAT [3:0] to low immediately after the response. The host controller generates interrupt (VOLT_SWITCH_INT) once the CMD or DAT [3:0] line goes low. The application should wait for this interrupt. If the 2ms timer expires without an interrupt (CMD/DAT lines going low), do a power cycle.

Note: Before doing a power cycle, switch off the card clock by programming CLKENA register

Proceed to step (5) on getting an interrupt (VOLT_SWITCH_INT).

Note: This interrupt must be cleared once this interrupt is received. Additionally, this interrupt should not be masked during the voltage switch sequence.

If the timer expires without interrupt (CMD/DAT lines going low), perform a power cycle.

Proceed to step (5) on interrupt.

Program the CLKENA, cclk_enable register, with 0 for the corresponding card; the host stops supplying SDCLK.

Program VOLT_REG to the required values for the corresponding card. The application must program the newly-defined VOLT_REG register to assign 1 for the bit corresponding to the card number. The application should start a timer > 5ms.

After the 5ms timer expires, the host voltage regulator is stable. Program CLKENA, cclk_enable register, with 1 for the corresponding card; the host starts providing SDCLK at 1. 8V; this can be at zero time after VOLT_REG has been programmed. When the CLKENA register is programmed, the application should start another timer > 1ms.

By detecting SDCLK, the card drives CMD to high at 1. 8V for at least one clock and then stops driving (tri-state); CMD is triggered by the rising edge of SDCLK (SDR timing).

If switching to 1. 8V signaling is completed successfully, the card drives DAT [3:0] to high at 1. 8V for at least one clock and then stops driving (tri-state); DAT [3:0] is triggered by the rising edge of SDCLK (SDR timing). DAT[3:0] must be high within 1ms from the start of SDCLK.

The host controller generates a voltage switch interrupt (VOLT_SWITCH_INT) and a command done (CD) interrupt once the CMD and DAT[3:0] lines go high. The application should wait for this interrupt to confirm CMD and DAT lines going high before the 1ms timer is done.

If the timer expires without the voltage switch interrupt (VOLT_SWITCH_INT), a power cycle should be performed. Program the CLKENA register to stop the clock for the corresponding card number. Wait for the cmd_done (CD) interrupt. Proceed for normal operation on interrupt.

After the sequence is completed, the host and the card start communication in SDR12 timing.

Voltage Switch Error Scenario

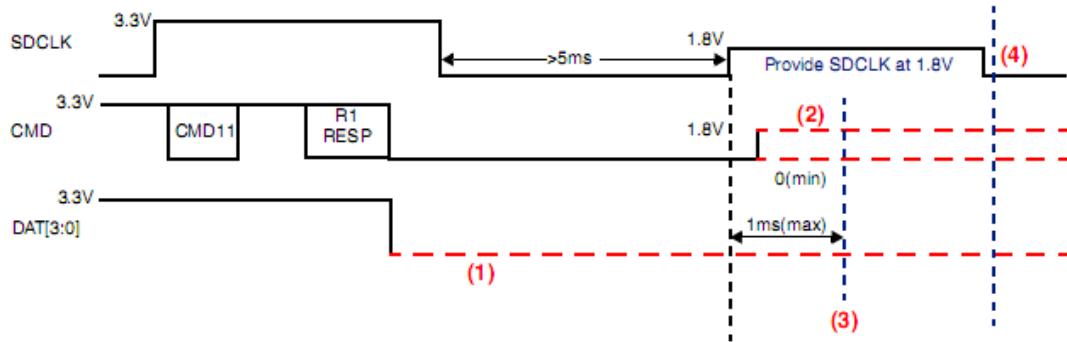


Fig. 4-16 Voltage Switch Error Scenario

If the interrupt (VOLT_SWITCH_INT) does not come, then the 2 ms timer should time out and a power cycle should be initiated.

Note: Before performing a power cycle, switch off the card clock by programming CLKENA register; no cmd_done (CD) interrupt is generated.

Additionally, if the card detects a voltage error at any point in between steps (5) and (7) in Figure 17-17, the card keeps driving DAT[3:0] to low until card power off.

CMD can be low or tri-state.

The host controller generates a voltage switch interrupt once the CMD and DAT[3:0] lines go high. The application should check for an interrupt to confirm CMD and DAT lines going high before the 1 ms timer is done.

If the 1 ms timer expires without interrupt (VOLT_SWITCH_INT) and cmd_done (CD), a power cycle should be performed. Program the CLKENA register to stop SDCLK of the corresponding card. Wait for the cmd_done interrupt. Proceed for normal operation on interrupt.

If DAT[3:0] is low, the host drives SDCLK to low and then stops supplying the card power.

Note: The card checks voltages of its own regulator output and host signals to ensure they are less than 2.5V. Errors are indicated by (1) and (2) in Figure 7-18.

If voltage switching is accepted by the card, the default speed is SDR12.

Command Done is given:

If voltage switching is properly done, CMD and DAT line goes high.

If switching is not complete, the 1ms timer expires, and the card clk is switched off.

Note: No other CMD should be driven before the voltage switching operation is completed and Command Done is received.

The application should use CMD6 to check and select the particular function; the function appropriate-speed should be selected.

After the function switches, the application should program the correct value in the CLKDIV register, depending on the function chosen. Additionally, if Function 0x4 of the Access mode is chosen—that is, DDR50, then the application should also program 1'b1 in DDR_REG for the card number that has been selected for DDR50 mode.

4.6.6 Back-End Power

Each device needs one bit to control the back-end power supply for an embedded device; this bit does not control the VDDH of the host controller. A back_end_power register enables software programming for back-end power. The value on this register is output to the back_end_power signal, which can be used to switch power on and off the embedded device.

4.6.7 DDR Operation

4-bit DDR Programming Sequence

DDR programming should be done only after the voltage switch operation has completed. The following outlines the steps for the DDR programming sequence:

Once the voltage switch operation is complete, the user must program VOLT_REG to the required values for the corresponding card.

To start a card to work in DDR mode, the application must program a bit of the newly

defined VOLT_REG[31:16] register with a value of 1'b1.

The bit that the user programs depends on which card is to be accessed in DDR mode.

To move back to SDR mode, a power cycle should be run on the card—putting the card in SDR12 mode—and only then should VOLT_REG[31:16] be set back to 1'b0 for the appropriate card.

8-bit DDR Programming Sequence

The following outlines the steps for the 8-bit DDR programming sequence:

The cclk_in signal should be twice the speed of the required cclk_out. Thus, if the cclk_out signal is required to be 50 MHz, the cclk_in signal should be 100 MHz.

The CLKDIV register should always be programmed with a value higher than zero (0); that is, a clock divider should always be used for 8-bit DDR mode.

The application must program the UHS_REG [31:16] register (DDR_REG bits) by assigning it with a value of 1 for the bit corresponding to the card number; this causes the selected card to start working in DDR mode.

Depending on the card number, the CTYPE [31:16] bits should be set in order to make the host work in the 8-bit mode.

eMMC4.5 DDR START Bit

The eMMC4.5 changes the START bit definition in the following manner:

Receiver samples the START bit on the rising edge.

On the next rising edge after sampling the START bit, the receiver must sample the data.

Removes requirement of the START bit and END bit to be high for one full cycle.

Notes: The Host Controller does not support a START bit duration higher than one clock cycle. START bit durations of one or less than one clock cycle are supported and can be defined at the time of startup by programming the EMMC_DDR_REG register.

Following figure illustrates cases for the definition change of the START bit with eMMC4.5; it also illustrates how some of these cases can fail in sampling when higher-value delays are considered for I/O PADs.

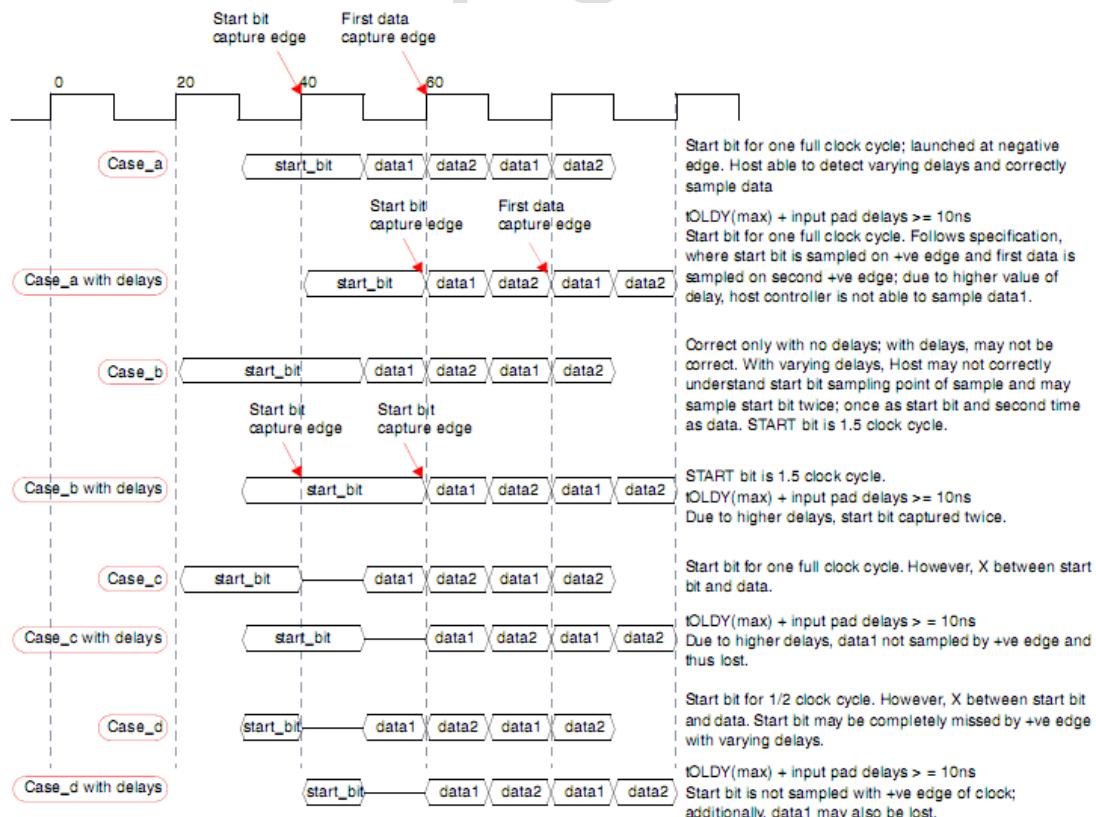


Fig. 4-17 CASES for eMMC 4.5 START bit

Reset Command/Moving from DDR50 to SDR12

To reset the mode of operation from DDR50 to SDR12, the following sequence of operations has to be done by the application:

Issue CMD0.

When CMD0 is received, the card changes from DDR50 to SDR12.

Program the CLKDIV register with an appropriate value.

Set DDR_REG to 0.

Note: The VOLT_REG register should not be programmed to 0 while switching from DDR50 to SDR12, since the card is still operating in 1.8V mode after receiving CMD0.

4.6.8 H/W Reset Operation

When the RST_n signal goes low, the card enters a pre-idle state from any state other than the inactive state.

H/W Reset Programming Sequence

The following outlines the steps for the H/W reset programming sequence:

Program CMD12 to end any transfer in process.

Wait for DTO, even if no response is sent back by the card.

Set the following resets:

DMA reset- CTRL[2]

FIFO reset – CTRL[1] bits

Note: The above steps are required only if a transfer is in process.

Program the CARD_RESET register with a value of 0; this can be done at any time when the card is connected to the controller. This programming asserts the RST_n signal and resets the card.

Wait for minimum of 1 μ s or cclk_in period, whichever is greater

After a minimum of 1 μ s, the application should program a value of 0 into the CARD_RESET register. This de-asserts the RST_n signal and takes the card out of reset.

The application can program a new CMD only after a minimum of 200 μ s after the de-assertion of the RST_n signal, as per the MMC 4.41 standard.

Note: For backward compatibility, the RST_n signal is temporarily disabled in the card by default. The host may need to set the signal as either permanently enabled or permanently disabled before it uses the card.

4.6.9 FBE Scenarios

An FBE occurs due to an AHB error response on the AHB bus. This is a system error, so the software driver should not perform any further programming to the Host. The only recovery mechanism from such scenarios is to do one of the following:

- Issue a hard reset by asserting the reset_n signal
- Do a program controller reset by writing to the CTRL[0] register

FIFO Overflow and Underflow

During normal data transfer conditions, FIFO overflow and underflow will not occur. However if there is a programming error, then FIFO overflow/underflow can result. For example, consider the following scenarios.

- For transmit: PBL=4, Tx watermark = 1. For the above programming values, if the FIFO has only one location empty, it issues a dma_req to IDMAC FSM. Due to PBL value=4, the IDMAC FSM performs 4 pushes into the FIFO. This will result in a FIFO overflow interrupt.
- For receive: PBL=4, Rx watermark = 1. For the above programming values, if the FIFO has only one location filled, it issues a dma_req to IDMAC FSM. Due to PBL value=4, the IDMAC FSM performs 4 pops to the FIFO. This will result in a FIFO underflow interrupt.

The driver should ensure that the number of bytes to be transferred as indicated in the descriptor should be a multiple of 4bytes with respect to H_DATA_WIDTH=32. For example, if the BYTCNT = 13, the number of bytes indicated in the descriptor should be 16 for H_DATA_WIDTH=32.

Programming of PBL and Watermark Levels

The DMAC performs data transfers depending on the programmed PBL and threshold values.

Table 4-16 PBL and Watermark Levels

PBL (Number of transfers)	Tx/Rx Watermark Value
1	greater than or equal to 1
4	greater than or equal to 4
8	greater than or equal to 8
16	greater than or equal to 16
32	greater than or equal to 32
64	greater than or equal to 64
128	greater than or equal to 128
256	greater than or equal to 256

4.6.10 Variable Delay/Clock Generation

Variable delay mechanism for the cclk_in_drv is optional, but it can be useful in order to meet a range of hold-time requirements across modes. Variable delay mechanism for the cclk_in_sample is mandatory and is required to achieve the correct sampling point for data.

cclk_in/cclk_in_sample/ cclk_in_drv is generated by Clock Generation Unit (CLKGEN) with variable delay mechanism, which includes Phase Shift Unit and Delay Line Unit selectable.

The Phase Shift Unit can shift cclk_in_sample/cclk_in_drv by 0/90/180/270-degree relative to cclk_in, controlled by *sample_degree/drv_degree*.

The Delay Line Unit can delay cclk_in_sample/cclk_in_drv relative to cclk_in in the unit of delay element when *sample_sel/drv_sel* is 1. The numberof delay element to be used is determined by *sample_delaynum/drv_delay*.

cclk_in is generated by cclkin divided by 2. cclk_in_drv and cclk_in_sample clocks are phase-shifted with delayed versions of cclk_in. All clocks are recommended to have a 50% duty cycle; DDR modes must have 50% duty cycles.

The architecture is as follows.

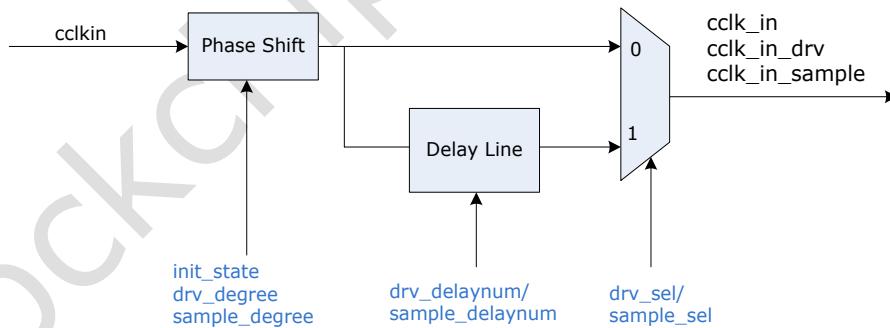


Fig. 4-18 Clock Generation Unit

The control signals for different Host Controller instance are shown as follows:

Table 4-17 Configuration for SDMMC Clock Generation

Signal Name	Source	Default	Description
init_state	CRU_SDMMC_CON0[0]	0	Soft initial state for phase shift.
drv_degree [1:0]	CRU_SDMMC_CON0[2:1]	2	Phase shift for cclk_in_drv. 0: 0-degree 1: 90-degree 2: 180-degree

Signal Name	Source	Default	Description
			3: 270-degree
drv_delaynum [7:0]	CRU_SDMMC_CON0[10:3]	0	Element number in delay line for cclk_in_drv
drv_sel	CRU_SDMMC_CON0[11]	0	cclk_in_drv source selection: 0: use clock after phase_shift 1: use clock after phase_shift and delay line
sample_degree [1:0]	CRU_SDMMC_CON1[1:0]	0	Phase shift for cclk_in_sample. 0: 0-degree 1: 90-degree 2: 180-degree 3: 270-degree
sample_delaynum [7:0]	CRU_SDMMC_CON1[9:2]	0	Element number in delay line for cclk_in_sample
sample_sel	CRU_SDMMC_CON1[10]	0	cclk_in_sample source selection: 0: use clock after phase_shift 1: use clock after phase_shift and delay line

Table 4-18 Configuration for SDIO0 Clock Generation

Signal Name	Source	Default	Description
init_state	CRU_SDIO0_CON0[0]	0	Soft initial state for phase shift.
drv_degree [1:0]	CRU_SDIO0_CON0[2:1]	2	Phase shift for cclk_in_drv. 0: 0-degree 1: 90-degree 2: 180-degree 3: 270-degree
drv_delaynum [7:0]	CRU_SDIO0_CON0[10:3]	0	Element number in delay line for cclk_in_drv
drv_sel	CRU_SDIO0_CON0[11]	0	cclk_in_drv source selection: 0: use clock after phase_shift 1: use clock after phase_shift and delay line
sample_degree [1:0]	CRU_SDIO0_CON1[1:0]	0	Phase shift for cclk_in_sample. 0: 0-degree 1: 90-degree 2: 180-degree 3: 270-degree
sample_delaynum [7:0]	CRU_SDIO0_CON1[9:2]	0	Element number in delay line for cclk_in_sample
sample_sel	CRU_SDIO0_CON1[10]	0	cclk_in_sample source selection: 0: use clock after phase_shift 1: use clock after phase_shift and delay line

Table 4-19 Configuration for SDIO1 Clock Generation

Signal Name	Source	Default	Description
init_state	CRU_SDIO1_CON0[0]	0	Soft initial state for phase shift.
drv_degree [1:0]	CRU_SDIO1_CON0[2:1]	2	Phase shift for cclk_in_drv. 0: 0-degree 1: 90-degree 2: 180-degree 3: 270-degree
drv_delaynum [7:0]	CRU_SDIO1_CON0[10:3]	0	Element number in delay line for cclk_in_drv
drv_sel	CRU_SDIO1_CON0[11]	0	cclk_in_drv source selection: 0: use clock after phase_shift 1: use clock after phase_shift and delay line
sample_degree [1:0]	CRU_SDIO1_CON1[1:0]	0	Phase shift for cclk_in_sample. 0: 0-degree 1: 90-degree 2: 180-degree 3: 270-degree
sample_delaynum [7:0]	CRU_SDIO1_CON1[9:2]	0	Element number in delay line for cclk_in_sample
sample_sel	CRU_SDIO1_CON1[10]	0	cclk_in_sample source selection: 0: use clock after phase_shift 1: use clock after phase_shift and delay line

Table 4-20 Configuration for eMMC Clock Generation

Signal Name	Source	Default	Description
init_state	CRU_EMMC_CON0[0]	0	Soft initial state for phase shift.
drv_degree [1:0]	CRU_EMMC_CON0[2:1]	2	Phase shift for cclk_in_drv. 0: 0-degree 1: 90-degree 2: 180-degree 3: 270-degree
drv_delaynum [7:0]	CRU_EMMC_CON0[10:3]	0	Element number in delay line for cclk_in_drv
drv_sel	CRU_EMMC_CON0[11]	0	cclk_in_drv source selection: 0: use clock after phase_shift 1: use clock after phase_shift and delay line
sample_degree [1:0]	CRU_EMMC_CON1[1:0]	0	Phase shift for cclk_in_sample. 0: 0-degree 1: 90-degree 2: 180-degree

Signal Name	Source	Default	Description
			3: 270-degree
sample_delaynum [7:0]	CRU_EMMC_CON1[9:2]	0	Element number in delay line for cclk_in_sample
sample_sel	CRU_EMMC_CON1[10]	0	cclk_in_sample source selection: 0: use clock after phase_shift 1: use clock after phase_shift and delay line

The following outlines the steps for clock generation sequence:

Assert init_state to soft reset the CLKGEN.

Configure drv_degree/sample_degree.

If fine adjustment required, delay line can be used by configuring drv_delaynum/sample_delaynum and drv_sel/sample_sel.

Dis-assert init_state to start CLKGEN.

4.6.11 Variable Delay Tuning

Tuning is defined by SD and MMC cards to determine the correct sampling point required for the host, especially for the speed modes SDR104 and HS200 where the output delays from the cards can be up to 2 UI. Tuning is required for other speed modes—such as DDR50—even though the output delay from the card is less than one cycle.

Command for tuning is different for different cards.

SD Memory Card:

CMD19 – SD card for SDR50 and SDR104 speed modes. Tuning data is defined by card specifications.

CMD6 – SD card for speed modes not supporting CMD19. Tuning data is the 64byte SD status.

Multimedia Card:

CMD21 – MMC card for HS200 speed mode. Tuning data is defined by card specifications.

CMD8 – MMC card for speed modes not supporting CMD21. Tuning data is 512 byte ExtCSD data.

The following is the procedure for variable delay tuning:

Set a phase shift of 0-degree on cclk_in_sample.

Send the Tuning command to the card; the card in turn sends an R1 response on the CMD line and tuning data on the DAT line.

If the host sees any of the errors—start bit error, data crc error, end bit error, data read time-out, response crc error, response error—then the sampling point is incorrect.

Send CMD12 to bring the host controller state machines to idle.

The card may treat CMD12 as an invalid command because the card has successfully sent the tuning data, and it cannot send a response.

The host controller may generate a response time-out interrupt that must be cleared by software.

Repeat steps 2) to 4) by increasing the phase shift value or delay element number on cclk_in_sample until the correct sampling point is received such that the host does not see any of the errors.

Mark this phase shift value as the starting point of the sampling window.

Repeat steps 2 to 4 by increasing the phase shift value or delay element number on cclk_in_sample until the host sees the errors starting to come again or the phase shift value reaches 360-degree.

Mark the last successful phase shift value as the ending point of the sampling window.

A window is established where the tuning block is matched. For example, for a scenario where the tuning block is received correctly for a phase shift window of 90-degree and 180-degree, then an appropriate sampling point is established as 135-degree. Once a sampling point is

established, no errors should be visible in the tuning block.

4.6.12 Package Command

In order to reduce overhead, read and write commands can be packed in groups of commands—either all read or all write—that transfer the data for all commands in the group in one transfer on the bus.

Packed commands can be of two types:

- Packed Write: CMD23 → CMD25
- Packed Read: CMD23 → CMD25 → CMD23 → CMD18

Packed commands are put in packets by the application software and are transparent to the core. For more information on packed commands, refer to the eMMC specification.

4.6.13 Card Detection Method

There are many methods for SDMMC/SDIO0/SDIO1 card detection.

(1) Method1: Using CDETECT register, which is value on card_detect_n input port. 0 represents presence of card. Commonly for SDMMC/SDIO0/SDIO1.

(2) Method2: Using card detection unit, outputting host interrupt (*IRQ_ID[64]/[65]/[66]*). The card detection unit looks for any changes in the card-detect signals for card insertion or card removal. It filters out the debounces associated with mechanical insertion or removal, and generates one interrupt to the host. You can program the debounce filter value in DEBNCE[23:0]. Following figure illustrates the timing for card-detect signals. Commonly for SDMMC/SDIO0/SDIO1.

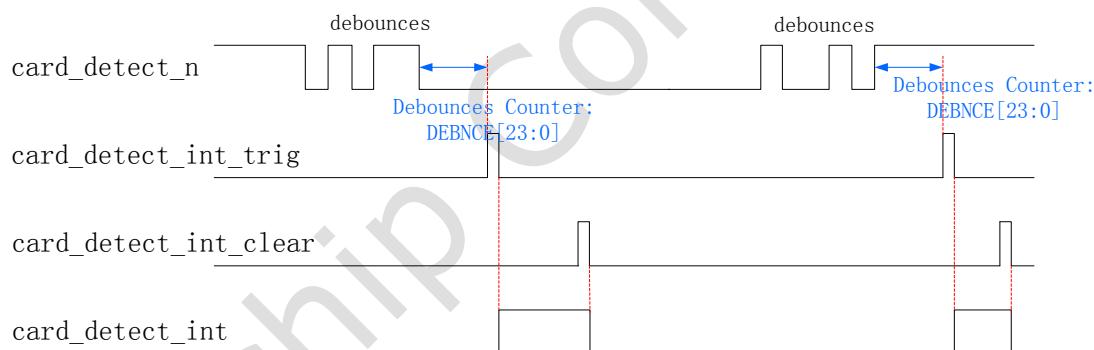


Fig. 4-19 Card Detection Method 2

- Method3: Using card detection unit in GRF, outputting *sdmmc_detect_dual_edge_int(IRQ_ID[138])*, only available for SDMMC. Similar to Method2, except that the debounce is selecting from 5ms/15ms/35ms/50ms; and the insertion/removal detection interrupt can be enabled or cleared respectively. The detailed register information is:

Table 4-21 Register for SDMMC Card Detection Method 3

Signal Name	Source	Default	Description
sd_detectn_rise_edge_irq_en	GRF_SOC_CON11[0]	0	sdmmc detect_n signal rise edge interrupt enable. 1'b1: enable 1'b0: disable
sd_detectn_rise_edge_irq_pd	GRF_SOC_CON11[1]	0	sdmmc detect_n rise edge interrupt pending status. Write 1 to clear the status.
sd_detectn_fall_edge_irq_en	GRF_SOC_CON11[2]	0	sdmmc detect_n signal fall edge

Signal Name	Source	Default	Description
			interrupt enable. 1'b1: enable 1'b0: disable
sd_detectn_fall_edge_irq_pd	GRF_SOC_CON11[3]	0	sdmmc detect_n fall edge interrupt pending status. Write 1 to clear the status.
grf_filter_cnt_sel	GRF_SOC_CON12[1:0]	0	the counter select for sd card detect filter: 2'b00: 5ms 2'b01: 15ms 2'b10: 35ms 2'b11: 50ms

- Method4: Using card_detect_n for interrupt source, connecting to *IRQ_ID[131]/[132]/[133]* directly. Commonly for SDMMC/SDIO0/SDIO1.

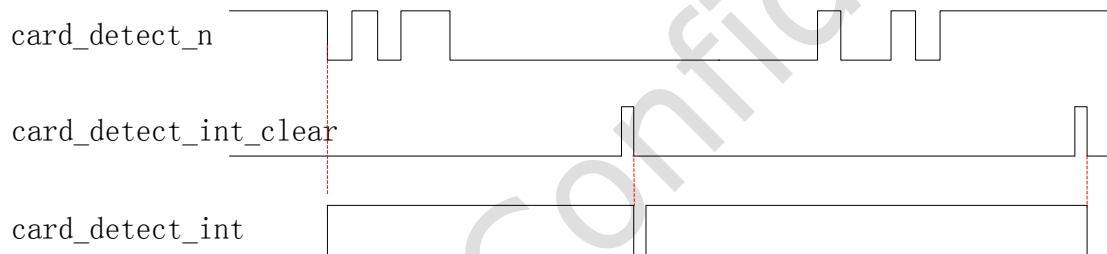


Fig. 4-20 Card Detection Method 4

Chapter 5 Dynamic Memory Interface (DMC)

5.1 Overview

The DMC includes two section: dynamic ram protocol controller(PCTL) and phy controller (PHYCTL).

The PCTL SoC application bus interface supports a lowest-latency native application interface (NIF). To maximize data transfer efficiency, NIF commands transfer data without flow control. To simplify command processing, the NIF accepts addresses in rank, bank, row, column format.

The PHYCTL provides control features to ease the customer implementation of digitally controlled features of the PHY such as initialization, DQS gate training, and programmable configuration controls. The PHYCTL has built-in self test features to provide support for production testing of the compatible PHY. It also provides a DFI 2.1 interface to the PHY.

The DMC supports the following features:

- Complete, integrated, single-vendor DDR3, DDR3L, LPDDR2, LPDDR3 solution
- DFI 2.1 interface compatibility
- Up to 1066 Mbps in 1:1 frequency ratio, using a 533MHz controller clock and 533MHz memory clock
- Dual channel, each channel up to 32 bits, totally support 64 bits data width
- Support for x8, x16, and x32 memories
- Each channel has separately controller and PHY
- Up to 2 memory ranks for each channel; devices within a rank tie to a common chip select
- Up to 8 open memory banks, maximum of eight per rank
- Per-NIF transaction controllable bank management policies: open-page, close-page
- Low area, low power architecture with minimal buffering on the data, avoiding duplication of storage resources within the system
- PCTL NIF slave interface facilitates easy integration with an external scheduler or standard on-chip buses
- Efficient DDR protocol implementation with in-order column (Read and Write) commands and out-of-order Activate and Precharge commands
- Three clock cycles best case command latency (best case is when a command is to an open page and the shift array in the PCTL is empty).
- 1T or 2T memory command timing
- Automatic clock stop, power-down and self-refresh entry and exit.
- Clock stop is LPDDR2/LPDDR3 only
- Software and hardware driven self-refresh entry and exit
- Programmable memory initialization
- Partial population of memories, where not all DDR byte lanes are populated with memory chips
- Programmable per rank memory ODT(On-Die Termination) support for reads and writes
- APB interface for controller software-accessible registers
- Programmable data training interface
- Assists in training of the data eye of the memory channel
- Provides a method for testing large sections of memory
- Support for industry standard UDIMMs (Unbuffered DIMMs) and RDIMMs (Registered DIMMs)
- Automatic DQS gate training and drift compensation
- At-speed built-in-self-test(BIST) loopback testing on both the address and data channels for DDR PHYs
- PHY control and configuration registers
- Support 2G memory wrap function

5.2 Block Diagram

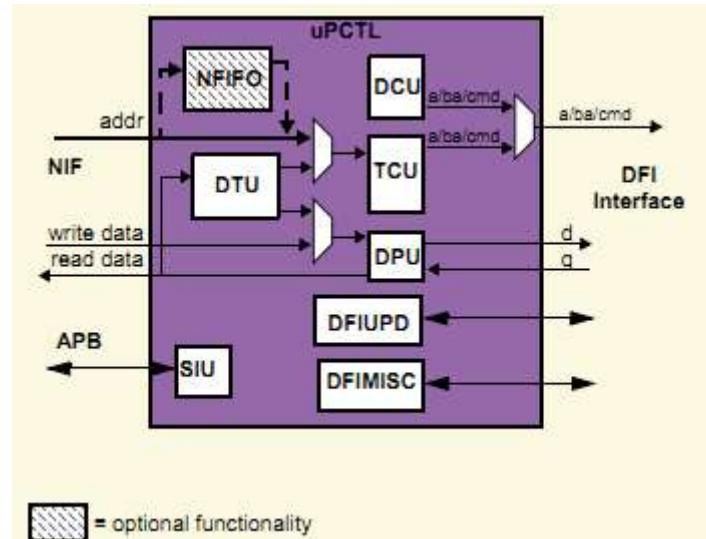


Fig. 5-1 Protocol controller architecture

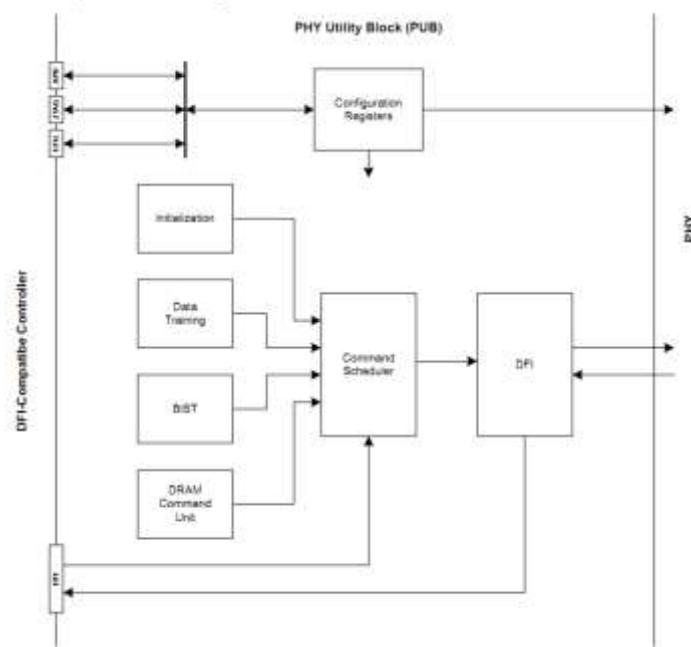


Fig. 5-2 PHY controller architecture

5.3 Function description

PCTL operations are defined in terms of the current state of the Operational State Machine. Software can move PCTL in any of the operational states by issuing commands via the SCTL register. Transitions from one operational state to the other occur pass through a “transitional” state. Transitional states are exited automatically by the PCTL after all the necessary actions required to change operational state have been completed. The current operational state of PCTL is reported by the STAT register and is also available from the p_ctl_stat output. PCTL supports the following operational states:

Init_mem - This state is the default state entered after reset. All writable registers can be programmed. While in this state software can program PCTL and initialize the PHY and the memories. The memories are not refreshed and data that has previously been written to the memories may be lost as a result. The Init_mem state is also used when it is desirable to stop any automatic PCTL function that directly affects the memories, like Power Down and Refresh, or when software reset of the memory subsystem has to be executed.

Config - This state is used to suspend temporarily the normal NIF traffic and allow software to reprogram PCTL and memories if necessary, while still keeping active the periodic generation of Refresh cycles to the memories. Power Down entry and exit sequences are possible while in Config state.

Access - This is the operational state where NIF transactions are accepted by the PCTL and converted into memory read and writes. None of the registers can be programmed except SCFG, SCTL, ECCCLR and DTU* registers.

Low_power - Memories are in self refresh mode. The PCTL does not generate refresh cycles while in this state.

Access and Low_power states can also be entered and exited by the hardware low power signals (c_*). In case of conflicting software and hardware low-power commands, the resulting operational state taken by the controller can be either one of the two conflicting requests. Figure 13-3 illustrates the operational and transitional states.

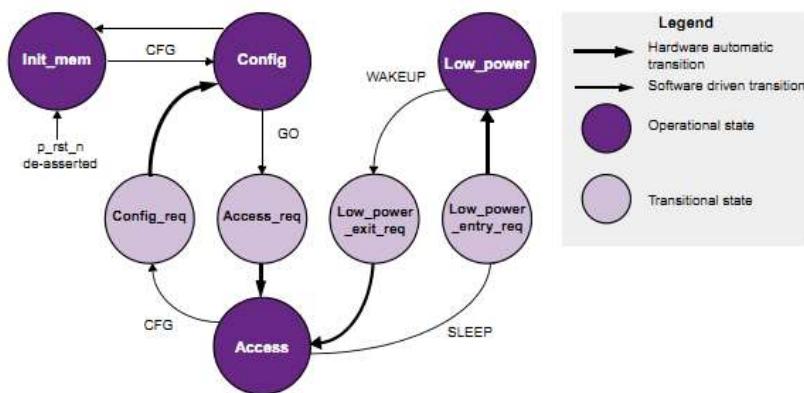


Fig. 5-3 Protocol controller architecture

The PHYCTL provides control features to ease the customer implementation of digitally controlled PHY features such as read DQS training, data eye training, output impedance calibration, and so on. The PHTCTL has built-in self test features to provide support for production testing of PHY. It also provides a DFI 2.1 interface to the PHY. The PHYCTL performs, in sequence, various tasks required by the PHY before it can commence normal DDR operations. SDRAM memory read/write access through the DDR PHY is primarily through a DFI 2.1 interface on the PHYCTL. Therefore, the memory controller used with the PHY must be DFI 2.1 compatible.

Access to the PHYCTL internal control features and registers is through a dedicated configuration port, which can be either APB or CFG (generic configuration interface). An optional JTAG interface can also be compiled in as an additional second configuration port to co-exist with either the APB or CFG main configuration ports. The PHYCTL is driven off two clocks, the controller clock (ctl_clk) and the configuration clock $pclk$ for an APB interface. The controller clock is the same clock driving the memory controller and will be the same frequency as the SDRAM clock (ck). The configuration clock can run at a frequency equal to or less than the controller clock. The configuration clock drives all non-DDR timing logic, such as configuration registers, PHY initialization, output impedance, and so on.

5.4 DDR PHY

5.4.1 DDR PHY Overview

In order to facilitate robust system timing and ease of use, DMC interface and control architecture utilizes a mixture of soft-IP and hard-IP design elements. The main control logic (Memory Controller) is supplied as soft-IP. The PHY is comprised of hard-IP components that include double-data rate Interface Timing Modules(ITM), input and output path DLLs, and application-specific SSTL I/Os.

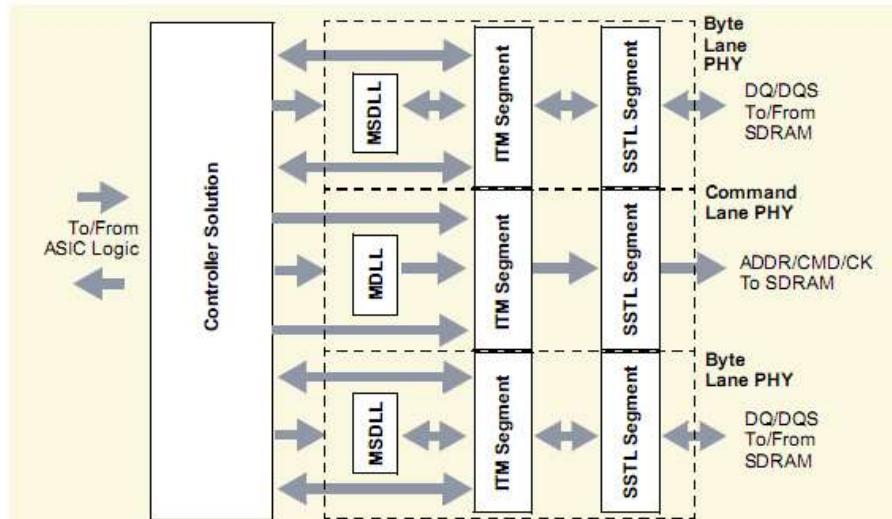


Fig. 5-4 DDR PHY architecture

In order to maximize system timing margins on the command/write path, inputs to the SDRAM are provided with the clock or data strobe centered in the associated data eye. The ITM components perform timing translation for the various signal groups of the interface. The hardened ITM approach ensures minimal pin to pin skew while allowing optimal circuit design for drive and capture circuitry. A DLL is utilized to facilitate the clock centering. In the Command Lane, a master DLL (MDLL) is utilized. In the Byte Lane, the master portion of a master/slave DLL macrocell (MSDLL) is utilized.

On the read path, read data from the SDRAM is arriving from the SDRAM edge aligned with the data strobes. In order to maintain maximum system timing margins on the input path, the data strobes are translated to the center of the data eye. The MSDL macrocell associated with each Byte Lane contains a master DLL and 2 slave DLLs (mirror delay lines). The slave DLL portion of the MSDL macrocell is utilized to facilitate the clock centering. DQS and DQS_b strobe inputs each utilize one of these slave DLL functions. The captured double data rate inputs are then converted to single data rate and passed onto the DDR Controller RTL logic. The ITM facilitates both data capture and DDR to SDR conversion.

The physical interface between the DDR controller and DDR SDRAMs uses DDR-specific SSTL I/O buffers with programmable on-die termination (ODT). These I/Os operate at either 1.8V for LPDDR/DDR2 interfacing (SSTL_18).

DMC interface and control architecture follows a common signal grouping philosophy. A Byte Lane is a complete eight-bit data unit consisting of the associated DQ, DM, and DQS/DQS_b signals. A 32-bit system would consist of four Byte Lanes. A Command Lane is a complete command and address unit including also clock signals. There would normally be only one Command Lane in a particular DDR SDRAM interface. All clock and data signals relative to a Lane, either Byte or Command, are isolated to within that Lane only. Timing critical clock and data signals do not traverse between Lanes. Implementation of a memory interface involves placing the Command Lane components, placing the Byte Lane components, and standard synthesis/place and route to complete the design.

Each SSTL cell communicating with the SDRAM has an associated ITM component. The ITM library consists of individual components designed specifically for signal groups of address and command, data & data mask, and data strobes. In order to ensure low pin to pin skews and facilitate ease of implementation, the ITM components are tileable. DLL output clock distribution is embedded within the ITM components.

5.4.2 Lane-Based Architecture

Byte Lane PHY

The data bus interface to the external memory is organized into self-contained units referred to herein as Byte Lanes. The external memory components are designed to support Byte Lanes for optimal system timing. The partitioning of the data word into discrete Byte Lanes allows pin to pin skew to be managed across a much smaller group of signals than would typically be required.

All components of the Byte Lane PHY are designed to permit connectivity by abutment. The ITM

connects by abutment to the SSTL I/O, and the DLL connects by abutment to the ITM. The SDRAM contains data strobes associated with each 8 bits of data and there is a timing skew allowance between the main clock signal to the SDRAM and its data strobe inputs during a Write command (tDQSS). 8bit memory components provide a single DQS.

A Byte Lane consists of the following I/O slots:

- 8 data bits (DQ)
- data strobe bits (DQS / DQS_b)
- 1 data mask bit (DM)
- I/O power and ground cells
- Core power and ground cells

Each functional I/O slot has an associated ITM module, including DQ, DM, and DQS/DQS_b. The ITMs provide a mechanism for monitoring read timing drift, which can be used to adjust timing to maintain optimum system margins. Drift analysis and compensation is performed by the controller on a per Byte Lane basis. The ITM components contain the functions to monitor DQS drift and permit timing adjustment, the controller provides the analysis and control for these functions. These functions operate dynamically for each data bit of every user-issued Read command. There are no overhead penalties in channel bandwidth or utilization incurred by the use of these functions.

The memory interface (PHY) architecture is based on the concept of independent, but related, signal groups to provide the highest level of system timing performance. In order to maintain robust system timing, all clock and data signals relevant to a Byte Lane remain within that Byte Lane. These signals are not shared between other Byte Lanes or between a Byte Lane and a Command Lane. Alternate approaches require clock distribution networks that span the full length of the interface including all address, command, and data signals. These large clock distribution networks are difficult for the user to design and implement, and add an additional component of pin to pin skew to the critical timing budget.

A DLL macrocell (MSDLL) consisting of a master DLL and 2 slave DLLs (mirror delay lines) is utilized at each Byte Lane to facilitate optimal PHY timing for drive and capture of DDR data streams, and allows the Lanes to be independent. The master DLL section provides outputs for DDR data stream creation to the SDRAMs and acts as a reference for the slave delay line sections. The slave delay line sections translate the incoming DQS/DQS_b into the center of the read data eye to maximize read system timing margins.

The user is permitted to fine tune the relationship of the DQS and DQ signals to maximize read system timing margin. The DLL includes adjustability of the slave delay lines for the DQS and DQS_b signals, which provide byte-wide timing adjustments. The ITMs include adjustability of the read DQS/DQS_b strobe timing, which provides byte-wide timing adjustments. The ITMs include adjustability of the read DQ signal timing, which provides per-bit timing adjustability. To permit Lane-independent timing adjustments, DLL adjustment bits are provided by the controller per Byte Lane and ITM adjustment bits are provided per bit.

DMC interface and control solution allows memory systems with a word width narrower than the design. Our system is designed with a 32 bit data width and it can then be utilized with either 16 bit or 32 bit memory systems. The controller contains register settings to allow the desired operational mode to be set in the final device.

The DDR-specific SSTL I/Os include programmable ODT and output impedance selection. The ODT and output impedances can be dynamically calibrated to compensate for variations in voltage and temperature. The ODT feature can be disabled by the controller. When ODT is enabled by the controller, the SSTL I/O automatically enables its internal ODT circuitry when in input mode and disable this circuitry when in output mode, as determined by the output enable signal. The initial programming and subsequent calibration of the ODT and output impedance is achieved through the use of an impedance control loop that can be triggered to calibrate the ODT and output impedance values at the I/Os based on the desired impedance value when compared to an precision external resistor. All the necessary pieces of the impedance control loop are included in the SSTL I/O library.

There are four Byte Lanes in our chip of 32 bit memory system.

Command Lane PHY

The control and address interface to the external memory is organized into a self-contained unit referred to herein as a Command Lane. DMC interface contains a single Command Lane

and four Byte Lanes.

All components of the Command Lane PHY are designed to permit connectivity by abutment. The ITM connects by abutment to the SSTL I/O, and the DLL connects by abutment to the ITM. A typical Command Lane consists of the following I/O slots:

- Memory clocks (CK/CK_b)
- Command signals (RAS_b, CAS_b, WE_b)
- 1 or more clock enable (CKE)
- 1 or more on-die termination (ODT)
- chip select (CS_b)
- bank address (BA)
- 16 row/column address (A)
- I/O power and ground cells
- Core power and ground cells

The system clock input is used to provide the source clock for the memory interface. Memory controller supports 2 SDRAM ranks. There is one CKE, ODT, and CS_b signal provided for each rank.

Each functional I/O slot has an associated ITM module, with exception of the system clock input. A master DLL (MDLL) is utilized with the Command Lane to facilitate optimal PHY timing for drive of DDR data streams, and allows the Lane to be independent. The DLL macrocells provide two 0 degree phase outputs, one which can be used to drive the controller logic. The Command Lane MDLL is used for this purpose.

To permit Lane-independent timing adjustments, DLL and ITM adjustment bits are provided by the controller separately for Command and Byte Lanes.

5.4.3 Master DLL(MDLL)

Master DLL for DDR2, and LPDDR applications is a Delay Locked Loop that takes an input reference clock (clk_in) and generates four clock outputs, each delayed in quarter clock cycle (90°) increments. These four clock phases (clk_0, clk_90, clk_180, clk_270) can be generated with very high accuracy and low jitter across a wide range of frequencies.

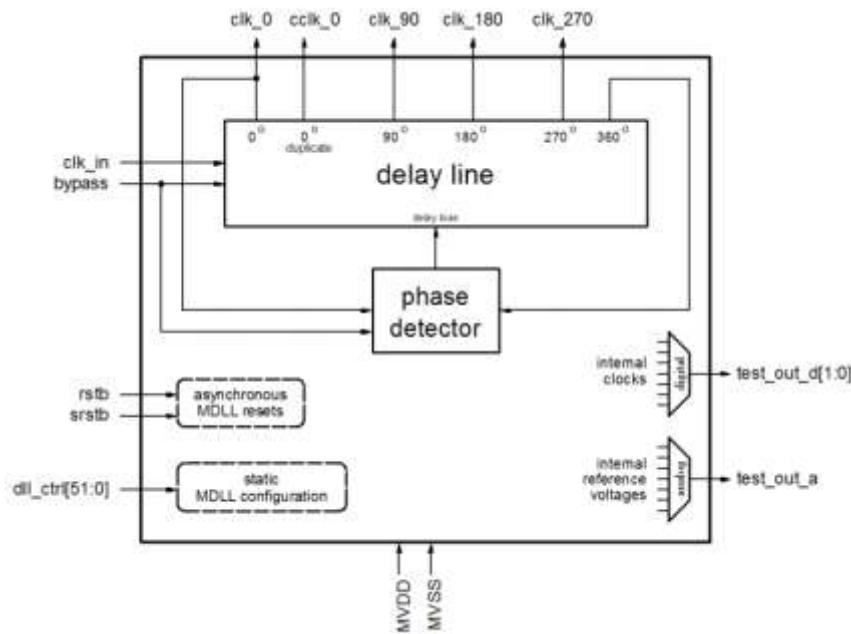


Fig. 5-5 DDR PHY master DLL architecture diagram

A number of test modes and configuration settings are included:

A bypass mode shuts down all analog circuitry, and directly buffers the input clock and strobes with appropriate delays and inversions to the output clocks and strobes. This mode can be used for low speed functional or IDDQ testing.

A digital test output (test_out_d) provides direct observability of several internal reference clock and timing nodes.

An analog test output (test_out_a) provides direct observability of several internal reference voltages.

Master DLL Control for Trim and Test

The performance and testing of the MDLL can be accessed through the dll_ctrl bus.

Table 5-1 DDR PHYtrim and test MDLL control

Static Input	Field	Description
dll_ctrl	[1:0]	Reserved
	[4:2]	ipump_trm[2:0] Charge pump current trim
	[5]	test_ctrl_en Test control enable for analog and digital test outputs
	[8:6]	test_ctrl_d[2:0] Digital test control. Selects the digital signal to be viewed at the digital test output
	[10:9]	test_ctrl_a[1:0] Analog test control. Selects the analog signal to be viewed at the analog test output
	[11]	Reserved
	[14:12]	bias_trm[2:0] Bias generator frequency trim
	[19,15]	fdtrm[1:0] Bypass mode fixed delay trim
	[22:20]	bias_trm[6:4] Bias generator control voltage trim
	[23]	bps200 Bypass frequency select
	[28:24]	Reserved
	[29]	Reserved
	[37:30]	Reserved
	[43:38]	fb_trm[5:0] Feedback delay adjust
	[49:44]	Reserved
	[50]	test_hizb_a Analog test output tri-stated control
	[51]	Reserved

Charge Pump Current Trim:

Table 5-2 charge pump current trim in dll_ctrl

Field	Setting	Function	Suggested Default
ipump_trm[2:0]	000	Maximum current	000
	111	Minimum current	

Digital Test Control:

Table 5-3 DLL digital test control in dll_ctrl

test_ctrl_en	test_ctrl_d[2:0]	Function	Suggested Default
0	xxx	digital test outputs disabled (drive '0')	0,000
1	000	0° output clock (clk_0)	
1	001	90° output clock (clk_90)	
1	010	180° output clock (clk_180)	
1	011	270° output clock (clk_270)	
1	100	360° internal clock (clk_360_int)	
1	101	Speed-up pulse (spdup)	
1	110	Slow-down pulse (slwdn)	
1	111	Asic output clock (cclk_0)	

Analog Test Control:

Table 5-4 DLL analog test control in dll_ctrl

test_hizb_a	test_ctrl_en	test_ctrl_a[1:0]	Function	Suggested Default
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test_hizb_a	test_ctrl_en	test_ctrl_a[1:0]	Function	Suggested Default
0	x	xx	Tri-state	0,0,00
1	0	xx	MVSS	
1	1	00	Filter output (Vc)	
1	1	01	Replica bias output for NMOS (Vbn)	
1	1	10	Replica bias output for PMOS (Vbp)	
1	1	11	MVDD	

Bias Generator Trim:

The bias generator trim capability can be used to adjust the behavior of the bias voltages being supplied to the delay line. Characteristics of the DLL that may warrant an adjustment of this trim value include the inability to lock due to a slow clock (suggest decreasing Vc adjust), inability to lock due to fast clock (suggest increasing Vc adjust) and increase noise margin on bias voltages (suggest decreasing Fmax adjust). The bit fields described in the following table can be set to any value between 000(binary) and 111(binary).

Table 5-5 bias generator trim in dll_ctrl

Field	Setting	Function	Suggested Default
bias_trm[2:0]	000	Fmax trim: minimum adjust	111
	111	Fmax trim: maximum adjust	
bias_trm[6:4]	000	Vc level trim: minimum adjust	011
	111	Vc level trim: maximum adjust	

Feedback Trim:

The feedback trim capability can be used in the event that an adjustment is desired in the phase detector feedback of the DLL. Characteristics of the DLL that may warrant an adjustment of this trim value include non-optimal phase alignment. The lower 3 bits (2:0) are used for feed-back delay trimming and the upper 3 bits (5:3) are used for feed-forward delay trimming. The feed-back trimming is used to decrease total delay, decreasing the amount of delay between phase outputs. The feed-forward trimming is used to increase total delay, increasing the amount of delay between phase outputs. For each 3-bit field, the inputs can be set to any value between 000(binary) and 111(binary).

Table 5-6 MDLL feedback trim in dll_ctrl

Field	Setting	Function	Suggested Default
fb_trm[5:3] (feed-forward path)	000	Minimum additional delay	000
	111	Maximum additional delay	
fb_trm[2:0] (feed-back path)	000	Minimum additional delay	000
	111	Maximum additional delay	

Bypass Mode

The DLL has a bypass mode which allows phased clocks to be generated with analog locking circuitry disabled. This mode may be used for low-speed functional testing and for IDDq testing. Bypass mode can also be used when operating with LPDDR SDRAMs. When bypass mode is enabled, all analog circuitry is disabled, and all static current paths are shut down.

Bypass mode has two settings for the clk_90 delay to optimize it for two different frequency ranges.

Table 5-7 MDLL bypass mode frequency range in dll_ctrl

Field	Setting	Function	Suggested Default
bps200	0	0 to 100MHz	0
	1	0 to 200MHz	

It is also possible to trim the 90-degree delay using the fdtrm control bits.

Table 5-8 fdtrm control bits in dll_ctrl

Field	Setting	Function	Suggested Default
fdtrm[1:0]	00	nominal delay	00
	01	nominal delay - 10%	
	10	nominal delay + 10%	
	11	nominal delay + 20%	

5.4.4 Master-Slave DLL(MSDLL)

Master-Slave DLL for DDR2, and LPDDR applications is an integrated Delay Locked Loop and a pair of slave delays. The Delay Locked Loop (DLL) takes an input reference clock (clk_in), and generates four clock outputs, each delayed in quarter clock cycle (90°) increments. These four clock phases (clk_0, clk_90, clk_180, clk_270) can be generated with very high accuracy and low jitter across a wide range of frequencies.

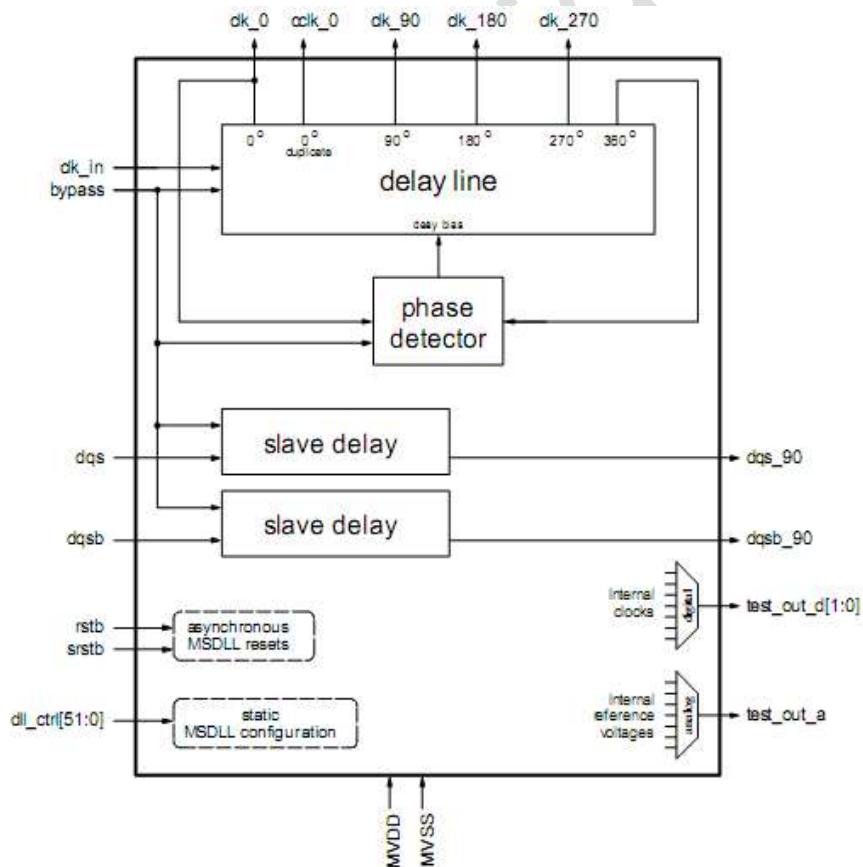


Fig. 5-6 DDR PHY master-slave DLL architecture diagram

The slave delay pair uses timing reference from the delay line to provide a highly accurate 90° delay to dqs and dqsbt inputs (generating dqs_90 and dqsbt_90 respectively).

A number of test modes and configuration settings are included:

A bypass mode shuts down all analog circuitry, and directly buffers the input clock and strobes with appropriate delays and inversions to the output clocks and strobes. This mode can be used for low speed functional or IDDQ testing.

A digital test output (test_out_d) provides direct observability of several internal reference clock and timing nodes.

An analog test output (test_out_a) provides direct observability of several internal reference voltages.

The primary application for MSDLL is a DDR2 Byte Lane PHY with Interface Timing Modules (ITMs).

MSDLL Control for Trim and Test

The performance and testing of the MSDLL can be accessed through the dll_ctrl bus. Many of these controls are the same as the MDLL, therefore, this section only describes the settings that are different.

Table 5-9 DDR PHYMSDLL control for trim and test

Static Input	Field	Description
	[1:0]	Reserved
	[4:2] ipump_trm[2:0]	Charge pump current trim
	[5] test_ctrl_en	Test control enable for analog and digital test outputs
	[8:6] test_ctrl_d[2:0]	Digital test control. Selects the digital signal to be viewed at the digital test output
	[10:9] test_ctrl_a[1:0]	Analog test control. Selects the analog signal to be viewed at the analog test output
	[11] test_ctrl_switch	Test control switch. Selects the analog and digital test signals of master or slave
	[14:12] bias_trm[2:0]	Master bias generator frequency trim
	[19,15] fdtrm[1:0]	Master bypass fixed delay trim
	[18:16] bias_trm[6:4]	Master bias generator control voltage trim
	[22:20] sl_bias_trm[2:0]	Slavebias generator control voltage trim
	[23] bps200	Bypass frequency select
	[26:24] sl_bias_trm[6:4]	Slave bias generator control voltage trim
	[28:27] fdtrm_sl[1:0]	Slave bypass fixed delay trim
	[29] lock_det_en	Lock detector enable
	[31:30]	Reserved
	[37:32] sl_fb_trm[5:0]	Slave feedback delay adjust
	[43:38] fb_trm[5:0]	Master feedback delay adjust
	[45:44] sl_bypass_start_up[1:0]	Slave auto-startup bypass
	[49:46] sl_phase_trm[3:0]	Slave phase lock trim
	[50] test_hizb_a	Analog test output tri-stated control
	[51]	Reserved

MSDLL Digital Test Control:

Table 5-10 MSDLL digital test control in dll_ctrl

test_ctrl_en	test_ctrl_switch	test_ctrl_d[2:0]	Function	Suggested Default
0	x	xx	digital test outputs disabled (drive '0')	0,0,000
1	0	000	0°output clock (clk_0)	
1		001	90°output clock (clk_90)	
1		010	180° output clock	

test_ctrl_en	test_ctrl_switch	test_ctrl_d[2:0]	Function	Suggested Default
			(clk_180)	
1		011	270° output clock (clk_270)	
1		100	360° internal clock (clk_360_int)	
1		101	Master speed-up pulse (spdup)	
1		110	Master slow-down pulse (slwdn)	
1		111	Output clock (cclk_0)	
1	1	000	Input signal dqs	
1		001	Slave input clock reference (clk_90_in)	
1		010	Slave internal feedback clock (clk_0_out)	
1		011	Output signal dqsb_90	
1		100	Output signal dqs_90	
1		101	Slave speed-up pulse (spdup)	
1		110	Slave slow-down pulse (slwdn)	
1		111	Auto-lock enable signal	

MSDLL Analog Test Control:

Table 5-11 MSDLL analog test control in dll_ctrl

test_hizb_a	test_ctrl_en	test_ctrl_switch	test_ctrl_a[1:0]	Function	Suggested Default
0	x	x	xx	Tri-state	0,0,0,00
1	0	x	xx	MVSS	
1	1		00	Master Filter output (Vc)	
1	1	0	01	Master Replica bias output for NMOS (Vbn)	
1	1		10	Master Replica bias output for PMOS (Vbp)	
1	1		11	MVDD	
1	1	1	00	Slave Filter output (Vc)	
1	1		01	Slave Replica bias output	

test_hizb_a	test_ctrl_en	test_ctrl_switch	test_ctrl_a[1:0]	Function	Suggested Default
				for NMOS (Vbn)	
1	1		10	Slave Replica bias output for PMOS (Vbp)	
1	1		11	MVDD	

MSDLL Lock Detector Enable:

This setting enables start of the slave DLL section after the master DLL section has reached lock. Characteristics of the DLL that may warrant an adjustment of this trim value include the slave DLL delay remaining in it's reset state (minimum delay, much less than 90 degrees) after the DLL lock time.

Table 5-12 MSDLL lock detector enable in dll_ctrl

Field	Setting	Function	Suggested Default
lock_det_en	0	Disable lock detector	0
	1	Enable lock detector	

Slave Auto-Startup Bypass:

By default, the slave DLL automatically starts to lock during the time the master is locking, after the master has begun to approach lock. This setting permits the user to manually start-up the slave DLL. To bypass the automatic startup, this setting should be set to '10'. Once the specified number of clocks has passed for the master DLL to achieve lock, the user sets this field to '11' to permit the slave DLL to startup. The user then waits for the specified number of clocks for the slave DLL to lock before proceeding. Characteristics of the slave DLL that might warrant a manual startup of the slave DLL include the inability for the slave DLL to produce a consistent and/or correct phase difference between the input signal and the output signal.

Table 5-13 slave_auto_startup_bypass in dll_ctrl

sl_bypass_start_up[1:0]	Function	Suggested Default
0X	Slave DLL automatically starts up	00
10	Slave DLL's automatic startup is disabled; the phase detector is disabled	
11	Slave DLL's automatic startup is disabled; the phase detector is enabled	

Slave DLL Phase Trim:

Selects the phase difference between the input signal and the corresponding output signal of the slave DLL. This setting applies to the dqs to dqs_90 and dqsb to dqsb_90 paths. The nominal phase difference is 90 degrees. Users may select to modify this value to account for factors external to the DLL, which require the DLL to produce a delay of greater than or less than the nominal 90 degrees. When modifying the value of these bits, the user does not need to issue a reset to the DLL but should wait the equivalent of the DLL lock time before the slave DLL circuitry is used (such as, receiving Read data from an SDRAM) to ensure the DLL has adequate time to stabilize with the new settings.

Table 5-14 slave DLL phase trim in dll_ctrl

sl_phase_trm[3:0]	Phase Difference (degrees)	Suggested Default
0000	90	0000
0001	72	

sl_phase_trm[3:0]	Phase Difference (degrees)	Suggested Default
0010	54	
0011	36	
0100	108	
0101	90	
0110	72	
0111	54	
1000	126	
1001	108	
1010	90	
1011	72	
1100	144	
1101	126	
1110	108	
1111	90	

MSDLL Bypass Mode

The DLL bypass mode, when enabled, shuts down all analog delay paths and phase detection circuitry and generates output clocks as directly buffered and inverted versions of clk_in. Bypass mode can be used for low-speed functional testing or for IDDQ testing. Bypass mode can also be used when operating with LPDDR SDRAMs. When bypass mode is enabled, all analog circuitry is disabled, and all static current paths are shut down. Phased outputs are generated during bypass with inverters and standard delays:

```

clk_0    = buffered clk_in
clk_90   = delayed version of clk_0
clk_180  = inverted clk_0
clk_270  = inverted clk_90
cclk_0   = buffered clk_in
dqs_90   = delayed version of dqs
dqsb_90  = delayed version of dqsb

```

Bypass mode has two settings for the clk_90 delay to optimize it for two different frequency ranges same as MDLL.

It is also possible to trim the MDLL 90 degree delay using the fdtrm control bits same as MDLL. And it is also possible to trim the MSDLL 90 degree delay using the fdtrm_sl control bits same as fdtrm.

5.4.5 DQS Gating

DDR2 systems use a bidirectional data strobe which is driven by the host during memory writes, and by the SDRAM during memory reads. During active read commands, the ITMS basically acts as a buffer for the incoming DQS/DQS_b. A turn-around time exists between operations when neither device is driving the bus, and the strobe traces are held by termination circuitry at a mid-rail voltage.

While the DQS lines are held at mid-rail during inactive periods, an unknown value X is being received by the SSTL inputs. To prevent X from causing false transitions and other negative effects within the read path, the input read dqs strobe path is disabled when there is no active read data. The ITMS provides the functions to enable/disable this path, while the control of these functions is provided by the memory controller logic. A basic view of the enable/disable requirements is shown in following figure.

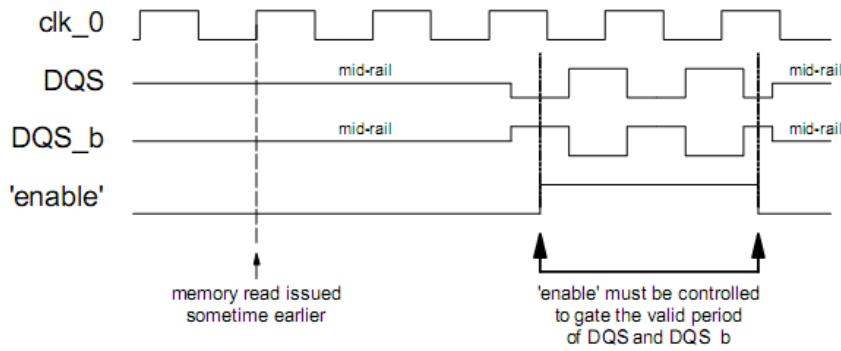


Fig. 5-7 Strobe Gating Requirements During Read Operations

After a read is issued, the SDRAM drives DQS and DQS_b for a number of clock cycles equal to the read burst length. Differing SDRAM CAS latencies, clock cycle times, board trace lengths, and other analog factors between controller and SDRAM result in a variable latency between when the read was issued, and when the returning DQS/DQS_b strobes reach the ITMS. The goal of DQS gating is to control a window, which enables and disables the input read dqs path only when the DQS lines are active, not when they are at mid-rail. There is a pre-preamble and post-preamble surrounding the active DQS edges that is used as the point to perform the enabling and disabling of this window.

There are two windowing schemes supported by the ITMS - passive windowing and active windowing - which are selected by input *dqs_config*.

Passive Windowing

In the passive windowing mode (*dqs_config* = 1), the controller asserts *dqs_en* at the start of the window and de-asserts *dqs_en* at the end of the window. This provides the coarse (clock-cycle) position of the enable and disable edges. Fine tuning (1/4 clock cycle) of the window placement is selected by *phase_sel[1:0]*.

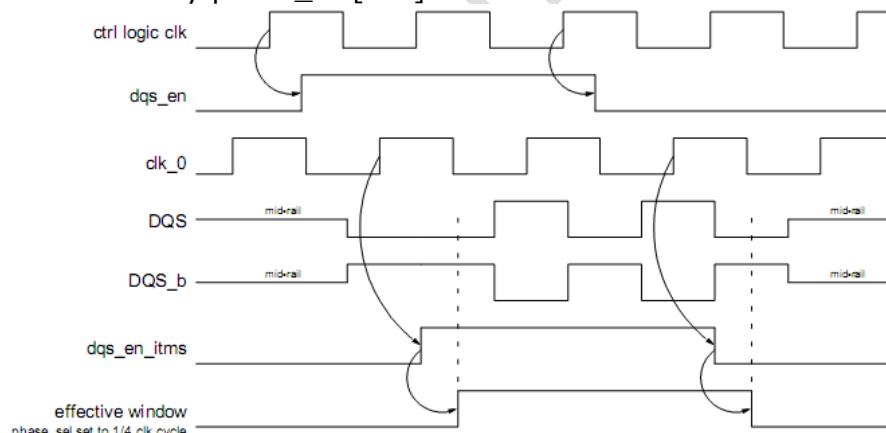


Fig. 5-8 DQS gating - passive windowing mode

The *phase_sel[1:0]* settings are provided.

Table 5-15 phase selection for dqs gating

phase_sel[1:0] Phase Selection		
Setting	Selected Phase	Offset
00	clk_90 (90 deg)	1/4 clock cycle
01	clk_180 (180 deg)	1/2 clock cycle
10	clk_270 (270 deg)	3/4 clock cycle
11	clk_0 (360 deg)	1 clock cycle

Active Windowing

The active windowing mode addresses the fact that the postamble is shorter than the preamble. The optimal window position for the preamble and postamble are not necessarily the same. In the active windowing mode (*dqs_config* = 0), the controller asserts *dqs_en* for one clock cycle at the start of the window and asserts *dqs_dis* for one clock cycle at the end of the window. Internal to ITMS, the assertion of *dqs_dis* is shifted by a further 180 degrees to account for the

fact that DQS_b occurs 180 degrees later than DQS. This provides the coarse (clock-cycle) position of the enable and disable edges.

Fine tuning (1/4 clock cycle) of the window placement is selected by phase_sel[1:0]. The effective window is opened in the same manner as in the passive windowing mode, such as dqs_en assertion plus the phase_sel offset. To close the window, the controller asserts dqs_dis to inform the ITMS to expect the last DQS_b rising edge of the burst. The phase_sel setting is applied to this to set the effective time at which to expect the last DQS_b rising edge. The last DQS_b rising edge of the burst is also the last data of the burst. This last DQS_b rising edge is used to close the window. Thus, the window is self-closing.

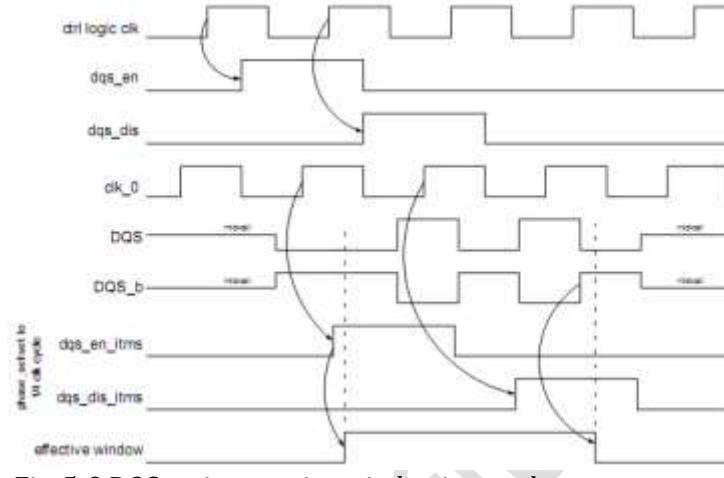


Fig. 5-9 DQS gating – active windowing mode

5.4.6 Dynamic Strobe Drift Detection

DDR2 systems can have a long round-trip path from the controller clock output (CK), to the SDRAM, and back to the controller data strobe input (DQS). The sum of potential variations in this path can exceed 25% of a clock cycle at high frequencies (>300MHz), so some compensation should be made if the path delay increases or decreases slowly, but significantly, during normal operation.

The ITMS component has a two-bit strobe drift indicator (dqs_drift), which changes value in grey code if the returning strobe drifts across internal 90° timing reference boundaries. The absolute value of this indicator is not important, but the change in value over time is.

Table 5-16 dynamic strobe drift indicators

dqs_drift[1:0]		DQS Drift Direction	Required Changes
Old Value	New Value		
00	01	forward	increase read data latency by 90 degrees
	10	backward	decrease read data latency by 90 degrees
01	11	forward	increase read data latency by 90 degrees
	00	backward	decrease read data latency by 90 degrees
10	00	forward	increase read data latency by 90 degrees
	11	backward	decrease read data latency by 90 degrees
11	10	forward	increase read data latency by 90 degrees
	01	backward	decrease read data latency by 90 degrees

5.5 Register description

5.5.1 Registers Summary

Name	Offset	Size	Reset Value	Description
DDR_PCTL_SCFG	0x0000	W	0x00000300	State Configuration Register
DDR_PCTL_SCTL	0x0004	W	0x00000000	Operational State Control Register
DDR_PCTL_STAT	0x0008	W	0x00000000	Operational State Status Register
DDR_PCTL_INTRSTAT	0x000c	W	0x00000000	Interrupt Status Register
DDR_PCTL_MCMD	0x0040	W	0x00100000	Memory Command Register
DDR_PCTL_POWCTL	0x0044	W	0x00000000	Power Up Control Register
DDR_PCTL_POWSTAT	0x0048	W	0x00000000	Power Up Status Register
DDR_PCTL_CMDTSTAT	0x004c	W	0x00000000	Command Timers Status Register
DDR_PCTL_CMDTSTATEN	0x0050	W	0x00000000	Command Timers Status Enable Register
DDR_PCTL_MRRCFG0	0x0060	W	0x00000000	Mode Register Read Configuration 0
DDR_PCTL_MRRSTAT0	0x0064	W	0x00000000	Mode Register Read Status 0 Register
DDR_PCTL_MRRSTAT1	0x0068	W	0x00000000	Mode Register Read Status 0 Register
DDR_PCTL_MCFG	0x0080	W	0x00040020	Memory Configuration Register
DDR_PCTL_PPFCFG	0x0084	W	0x00000000	Partially Populated Memories Configuration Register
DDR_PCTL_MSTAT	0x0088	W	0x00000000	Memory Status Register
DDR_PCTL_LPDDR2ZQCFG	0x008c	W	0xab0a560a	LPDDR2 ZQ Configuration Register
DDR_PCTL_MCFG1	0x007c	W	0x00000000	Memory Configuration 1 Register
DDR_PCTL_DTUPDES	0x0094	W	0x00000000	DTU Status Register
DDR_PCTL_DTUNA	0x0098	W	0x00000000	DTU Number of Addresses Created Register
DDR_PCTL_DTUNE	0x009c	W	0x00000000	DTU Number of Errors Register
DDR_PCTL_DTUPRD0	0x00a0	W	0x00000000	DTU Parallel Read 0 Register
DDR_PCTL_DTUPRD1	0x00a4	W	0x00000000	DTU Parallel Read 1 Register
DDR_PCTL_DTUPRD2	0x00a8	W	0x00000000	DTU Parallel Read 2 Register
DDR_PCTL_DTUPRD3	0x00ac	W	0x00000000	DTU Parallel Read 3 Register
DDR_PCTL_DTUAWDT	0x00b0	W	0x00000290	DTU Address Width Register
DDR_PCTL_TOGCNT1U	0x00c0	W	0x00000064	Toggle Counter 1us Register
DDR_PCTL_TINIT	0x00c4	W	0x000000c8	t_init Timing Register
DDR_PCTL_TRSTH	0x00c8	W	0x00000000	t_rsth Timing Register
DDR_PCTL_TOGCNT100N	0x00cc	W	0x00000001	Toggle Counter 100ns
DDR_PCTL_TREFI	0x00d0	W	0x00000001	t_refi Timing Register
DDR_PCTL_TMRD	0x00d4	W	0x00000001	t_mrd Timing Register
DDR_PCTL_TRFC	0x00d8	W	0x00000001	t_rfc Timing Register

Name	Offset	Size	Reset Value	Description
DDR_PCTL_TRP	0x00dc	W	0x00010006	t_trp Timing Register
DDR_PCTL_TRTW	0x00e0	W	0x00000002	t_rtw Timing Register
DDR_PCTL_TAL	0x00e4	W	0x00000000	AL Register
DDR_PCTL_TCL	0x00e8	W	0x00000004	CL Timing Register
DDR_PCTL_TCWL	0x00ec	W	0x00000003	CWL Timing Register
DDR_PCTL_TRAS	0x00f0	W	0x00000010	t_ras Timing Register
DDR_PCTL_TRC	0x00f4	W	0x00000016	t_rc Timing Register
DDR_PCTL_TRCD	0x00f8	W	0x00000006	t_rcd Timing Register
DDR_PCTL_TRRD	0x00fc	W	0x00000004	t_rrd Timing Register
DDR_PCTL_TRTP	0x0100	W	0x00000003	t_rtp Timing Register
DDR_PCTL_TWR	0x0104	W	0x00000006	t_wr Register
DDR_PCTL_TWTR	0x0108	W	0x00000004	t_wtr Timing Register
DDR_PCTL_TEXSR	0x010c	W	0x00000001	t_exsr Timing Register
DDR_PCTL_TXP	0x0110	W	0x00000001	t_xp Timing Register
DDR_PCTL_TXPDLL	0x0114	W	0x00000000	t_xpdll Timing Register
DDR_PCTL_TZQCS	0x0118	W	0x00000000	t_zqcs Timing Register
DDR_PCTL_TZQCSI	0x011c	W	0x00000000	t_zqcsi Timing Register
DDR_PCTL_TDQS	0x0120	W	0x00000001	t_dqs Timing Register
DDR_PCTL_TCKSRE	0x0124	W	0x00000000	t_cksrc Timing Register
DDR_PCTL_TCKSRX	0x0128	W	0x00000000	t_cksrcx Timing Register
DDR_PCTL_TCKE	0x012c	W	0x00000003	t_cke Timing Register
DDR_PCTL_TMOD	0x0130	W	0x00000000	t_mod Timing Register
DDR_PCTL_TRSTL	0x0134	W	0x00000000	Reset Low Timing Register
DDR_PCTL_TZQCL	0x0138	W	0x00000000	t_zqcl Timing Register
DDR_PCTL_TMRR	0x013c	W	0x00000002	t_mrr Timing Register
DDR_PCTL_TCKESR	0x0140	W	0x00000004	t_ckesr Timing Register
DDR_PCTL_TDPD	0x0144	W	0x00000000	t_dpd Timing Register
DDR_PCTL_DTUWACTL	0x0200	W	0x00000000	DTU Write Address Control
DDR_PCTL_DTURACTL	0x0204	W	0x00000000	DTU Read Address Control Register
DDR_PCTL_DTUCFG	0x0208	W	0x00000000	DTU Configuration Control Register
DDR_PCTL_DTUECTL	0x020c	W	0x00000000	DTU Execute Control Register
DDR_PCTL_DTUWD0	0x0210	W	0x00000000	DTU Write Data #0 Register
DDR_PCTL_DTUWD1	0x0214	W	0x00000000	DTU Write Data #1 Register
DDR_PCTL_DTUWD2	0x0218	W	0x00000000	DTU Write Data #2 Register
DDR_PCTL_DTUWD3	0x021c	W	0x00000000	DTU Write Data #3 Register
DDR_PCTL_DTUWDM	0x0220	W	0x00000000	DTU Write Data Mask Register
DDR_PCTL_DTURD0	0x0224	W	0x00000000	DTU Read Data #0 Register
DDR_PCTL_DTURD1	0x0228	W	0x00000000	DTU Read Data #1 Register
DDR_PCTL_DTURD2	0x022c	W	0x00000000	DTU Read Data #2 Register
DDR_PCTL_DTURD3	0x0230	W	0x00000000	DTU Read Data #3 Register

Name	Offset	Size	Reset Value	Description
DDR_PCTL_DTULFSRWD	0x0234	W	0x00000000	DTU LFSR Seed for Write Data Generation Register
DDR_PCTL_DTULFSRRD	0x0238	W	0x00000000	DTU LFSR Seed for Read Data Generation Register
DDR_PCTL_DTUEAF	0x023c	W	0x00000000	DTU Error Address FIFO Register
DDR_PCTL_DFITCTRLDELAY	0x0240	W	0x00000002	DFI tctrl_delay Register
DDR_PCTL_DFIODTCFG	0x0244	W	0x00000000	DFI ODT Configuration
DDR_PCTL_DFIODTCFG1	0x0248	W	0x06060000	DFI ODT Timing Configuration 1 (for Latency and Length)
DDR_PCTL_DFIODTRANKMAP	0x024c	W	0x00008421	DFI ODT Rank Mapping
DDR_PCTL_DFITPHYWRDATA	0x0250	W	0x00000001	DFI tphy_wrdata Register
DDR_PCTL_DFITPHYWRLAT	0x0254	W	0x00000001	DFI tphy_wrlat Register
DDR_PCTL_DFITRDDATAEN	0x0260	W	0x00000001	DFI trddata_en Register
DDR_PCTL_DFITPHYRDLAT	0x0264	W	0x0000000f	DFI tphy_rdlat Register
DDR_PCTL_DFITPHYUPDTYPE0	0x0270	W	0x00000010	DFI tphyupd_type0 Register
DDR_PCTL_DFITPHYUPDTYPE1	0x0274	W	0x00000010	DFI tphyupd_type1 Register
DDR_PCTL_DFITPHYUPDTYPE2	0x0278	W	0x00000010	DFI tphyupd_type2 Register
DDR_PCTL_DFITPHYUPDTYPE3	0x027c	W	0x00000010	DFI tphyupd_type3 Register
DDR_PCTL_DFITCTRLUPDMIN	0x0280	W	0x00000010	DFI tctrlupd_min Register
DDR_PCTL_DFITCTRLUPDMAX	0x0284	W	0x00000040	DFI tctrlupd_max Register
DDR_PCTL_DFITCTRLUPDDL	0x0288	W	0x00000008	DFI tctrlupddly Register
DDR_PCTL_DFIUPDCFG	0x0290	W	0x00000003	DFI Update Configuration Register
DDR_PCTL_DFITREFMSKI	0x0294	W	0x00000000	DFI Masked Refresh Interval
DDR_PCTL_DFITCTRLUPDI	0x0298	W	0x00000000	DFI tctrlupd_interval Register
DDR_PCTL_DFITRCFG0	0x02ac	W	0x00000000	DFI Training Configuration 0 Register
DDR_PCTL_DFITRSTAT0	0x02b0	W	0x00000000	DFI Training Status 0 Register
DDR_PCTL_DFITRWRLVLEN	0x02b4	W	0x00000000	DFI Training dfi_wrlvl_en Register
DDR_PCTL_DFITRRDLVLVLEN	0x02b8	W	0x00000000	DFI Training dfi_rdlvl_en Register
DDR_PCTL_DFITRRDLVLGATEEN	0x02bc	W	0x00000000	DFI Training dfi_rdlvl_gate_en Register
DDR_PCTL_DFISTSTAT0	0x02c0	W	0x00000000	DFI Status Status 0 Register
DDR_PCTL_DFISTCFG0	0x02c4	W	0x00000000	DFI Status Configuration 0 Register

Name	Offset	Size	Reset Value	Description
DDR_PCTL_DFISTCFG1	0x02c8	W	0x00000000	DFI Status Configuration 1 Register
DDR_PCTL_DFITDRAMCLKEN	0x02d0	W	0x00000002	DFI tdram_clk_enable Register
DDR_PCTL_DFITDRAMCLKDIS	0x02d4	W	0x00000002	DFI tdram_clk_disable Register
DDR_PCTL_DFISTCFG2	0x02d8	W	0x00000000	DFI Status Configuration 2 Register
DDR_PCTL_DFISTPARCLR	0x02dc	W	0x00000000	DFI Status Parity Clear Register
DDR_PCTL_DFISTPARLOG	0x02e0	W	0x00000000	DFI Status Parity Log Register
DDR_PCTL_DFLPCFG0	0x02f0	W	0x00070000	DFI Low Power Configuration 0 Register
DDR_PCTL_DFITRWRLVLRESPO	0x0300	W	0x00000000	DFI Training dfi_wrlvl_resp Status 0 Register
DDR_PCTL_DFITRWRLVLRESP1	0x0304	W	0x00000000	DFI Training dfi_wrlvl_resp Status 1 Register
DDR_PCTL_DFITRWRLVLRESP2	0x0308	W	0x00000000	DFI Training dfi_wrlvl_resp Status 2 Register
DDR_PCTL_DFITRRDLVLRESPO	0x030c	W	0x00000000	DFI Training dfi_rdlvl_resp Status 0 Register
DDR_PCTL_DFITRRDLVLRESP1	0x0310	W	0x00000000	DFI Training dfi_rdlvl_resp Status 1 Register
DDR_PCTL_DFITRRDLVLRESP2	0x0314	W	0x00000000	DFI Training dfi_rdlvl_resp Status 2 Register
DDR_PCTL_DFITRWRLVLDELAY0	0x0318	W	0x00000000	DFI Training dfi_wrlvl_delay Configuration 0 Register
DDR_PCTL_DFITRWRLVLDELAY1	0x031c	W	0x00000000	DFI Training dfi_wrlvl_delay Configuration 1 Register
DDR_PCTL_DFITRWRLVLDELAY2	0x0320	W	0x00000000	DFI Training dfi_wrlvl_delay Configuration 2 Register
DDR_PCTL_DFITRRDLVLDELAY0	0x0324	W	0x00000000	DFI Training dfi_rdlvl_delay Configuration 0 Register
DDR_PCTL_DFITRRDLVLDELAY1	0x0328	W	0x00000000	DFI Training dfi_rdlvl_delay Configuration 1 Register
DDR_PCTL_DFITRRDLVLDELAY2	0x032c	W	0x00000000	DFI Training dfi_rdlvl_delay Configuration 2 Register
DDR_PCTL_DFITRRDLVLGATEDELAY0	0x0330	W	0x00000000	DFI Training dfi_rdlvl_gate_delay Configuration 0
DDR_PCTL_DFITRRDLVLGATEDELAY1	0x0334	W	0x00000000	DFI Training dfi_rdlvl_gate_delay Configuration 1
DDR_PCTL_DFITRRDLVLGATEDELAY2	0x0338	W	0x00000000	DFI Training dfi_rdlvl_gate_delay Configuration 2
DDR_PCTL_DFITRCMD	0x033c	W	0x00000000	DFI Training Command Register

Name	Offset	Size	Reset Value	Description
DDR_PCTL_IPVR	0x03f8	W	0x00000000	IP Version Register
DDR_PCTL_IPTR	0x03fc	W	0x44574300	IP Type Register

Name	Offset	Size	Reset Value	Description
DDR_PUBL RIDR	0x0000	W	0x00100140	Revision Identification Register
DDR_PUBL PIR	0x0004	W	0x00000000	PHY Initialization Register
DDR_PUBL PGCR	0x0008	W	0x01bc2e04	PHY General Configuration Register
DDR_PUBL PGSR	0x000c	W	0x00000000	PHY General Status Register
DDR_PUBL DLLGCR	0x0010	W	0x03737000	DLL General Control Register
DDR_PUBL ACDLLCR	0x0014	W	0x40000000	AC DLL Control Register
DDR_PUBL PTR0	0x0018	W	0x0022af9b	PHY Timing Register 0
DDR_PUBL PTR1	0x001c	W	0x0604111d	PHY Timing Register 1
DDR_PUBL PTR2	0x0020	W	0x042da072	PHY Timing Register 2
DDR_PUBL ACIOCR	0x0024	W	0x33c03812	AC I/O Configuration Register
DDR_PUBL DXCCR	0x0028	W	0x00000800	DATX8 Common Configuration Register
DDR_PUBL DSGCR	0x002c	W	0xfa00001f	DDR System General Configuration Register
DDR_PUBL DCR	0x0030	W	0x0000000b	DRAM Configuration Register
DDR_PUBL DTPO0	0x0034	W	0x3092666e	DRAM Timing Parameters Register 0
DDR_PUBL DTPO1	0x0038	W	0x09830090	DRAM Timing Parameters Register 1
DDR_PUBL DTPO2	0x003c	W	0x1001a0c8	DRAM Timing Parameters Register 2
DDR_PUBL MR0	0x0040	W	0x00000a52	Mode Register 0
DDR_PUBL MR1	0x0044	W	0x00000000	Mode Register 1
DDR_PUBL MR2	0x0048	W	0x00000000	Mode Register 2
DDR_PUBL MR3	0x004c	W	0x00000000	Mode Register 3
DDR_PUBL ODTCR	0x0050	W	0x00210000	ODT Configuration Register
DDR_PUBL DTAR	0x0054	W	0x00000000	Data Training Address Register
DDR_PUBL DTDR0	0x0058	W	0xdd22ee11	Data Training Data Register 0
DDR_PUBL DTDR1	0x005c	W	0x7788bb44	Data Training Data Register 1
DDR_PUBL DCUAR	0x00c0	W	0x00000000	DCU Address Register
DDR_PUBL DCUDR	0x00c4	W	0x00000000	DCU Data Register
DDR_PUBL DCURR	0x00c8	W	0x00000000	DCU Run Register
DDR_PUBL DCULR	0x00cc	W	0x00000000	DCU Loop Register
DDR_PUBL DCUGCR	0x00d0	W	0x00000000	DCU General Configuration Register
DDR_PUBL DCUTPR	0x00d4	W	0x00000000	DCU Timing Parameters Registers
DDR_PUBL DCUSR0	0x00d8	W	0x00000000	DCU Status Register 0
DDR_PUBL DCUSR1	0x00dc	W	0x00000000	DCU Status Register 1
DDR_PUBL BISTR0	0x0100	W	0x00000000	BIST Run Register
DDR_PUBL BISTMSK0	0x0104	W	0x00000000	BIST Mask Register 0
DDR_PUBL BISTMSK1	0x0108	W	0x00000000	BIST Mask Register 1
DDR_PUBL BISTWCR	0x010c	W	0x00000020	BIST Word Count Register

Name	Offset	Size	Reset Value	Description
DDR_PUBL_BISTLSR	0x0110	W	0x1234abcd	BIST LFSR Seed Register
DDR_PUBL_BISTAR0	0x0114	W	0x00000000	BIST Address Register 0
DDR_PUBL_BISTAR1	0x0118	W	0x00000000c	BIST Address Register 1
DDR_PUBL_BISTAR2	0x011c	W	0x7fffffff	BIST Address Register 2
DDR_PUBL_BISTUDPR	0x0120	W	0xfffff0000	BIST User Data Pattern Register
DDR_PUBL_BISTGSR	0x0124	W	0x00000000	BIST General Status Register
DDR_PUBL_BISTWER	0x0128	W	0x00000000	BIST Word Error Register
DDR_PUBL_BISTBER0	0x012c	W	0x00000000	BIST Bit Error Register 0
DDR_PUBL_BISTBER1	0x0130	W	0x00000000	BIST Bit Error Register 1
DDR_PUBL_BISTBER2	0x0134	W	0x00000000	BIST Bit Error Register 2
DDR_PUBL_BISTWCSR	0x0138	W	0x00000000	BIST Word Count Status Register
DDR_PUBL_BISTFWR0	0x013c	W	0x00000000	BIST Fail Word Register 0
DDR_PUBL_BISTFWR1	0x0140	W	0x00000000	BIST Fail Word Register 1
DDR_PUBL_ZQ0CR0	0x0180	W	0x0000014a	ZQ 0 Impedance Control Register 0
DDR_PUBL_ZQ0CR1	0x0184	W	0x0000007b	ZQ 0 Impedance Control Register 1
DDR_PUBL_ZQ0SR0	0x0188	W	0x00000000	ZQ 0 Impedance Status Register 0
DDR_PUBL_ZQ0SR1	0x018c	W	0x00000000	ZQ 0 Impedance Status Register 1
DDR_PUBL_ZQ1CR0	0x0190	W	0x0000014a	ZQ 1 Impedance Control Register 0
DDR_PUBL_ZQ1CR1	0x0194	W	0x0000007b	ZQ 1 Impedance Control Register 1
DDR_PUBL_ZQ1SR0	0x0198	W	0x00000000	ZQ 1 Impedance Status Register 0
DDR_PUBL_ZQ1SR1	0x019c	W	0x00000000	ZQ 1 Impedance Status Register 1
DDR_PUBL_ZQ2CR0	0x01a0	W	0x0000014a	ZQ 2 Impedance Control Register 0
DDR_PUBL_ZQ2CR1	0x01a4	W	0x0000007b	ZQ 2 Impedance Control Register 1
DDR_PUBL_ZQ2SR0	0x01a8	W	0x00000000	ZQ 2 Impedance Status Register 0
DDR_PUBL_ZQ2SR1	0x01ac	W	0x00000000	ZQ 2 Impedance Status Register 1
DDR_PUBL_ZQ3CR0	0x01b0	W	0x0000014a	ZQ 3 Impedance Control Register 0
DDR_PUBL_ZQ3CR1	0x01b4	W	0x0000007b	ZQ 3 Impedance Control Register 1
DDR_PUBL_ZQ3SR0	0x01b8	W	0x00000000	ZQ 3 Impedance Status Register 0
DDR_PUBL_ZQ3SR1	0x01bc	W	0x00000000	ZQ 3 Impedance Status Register 1
DDR_PUBL_DX0GCR	0x01c0	W	0x00000681	DATX8 0 General Configuration Register
DDR_PUBL_DX0GSR0	0x01c4	W	0x00000000	DATX8 0 General Status Register 0
DDR_PUBL_DX0GSR1	0x01c8	W	0x00000000	DATX8 0 General Status Register 1
DDR_PUBL_DX0DLLCR	0x01cc	W	0x40000000	DATX8 0 DLL Control Register
DDR_PUBL_DX0DQTR	0x01d0	W	0xffffffff	DATX8 0 DQ Timing Register
DDR_PUBL_DX0DQSTR	0x01d4	W	0x3db05000	DATX8 0 DQS Timing Register
DDR_PUBL_DX1GCR	0x0200	W	0x00000681	DATX8 1 General Configuration Register
DDR_PUBL_DX1GSR0	0x0204	W	0x00000000	DATX8 1 General Status Register 0
DDR_PUBL_DX1GSR1	0x0208	W	0x00000000	DATX8 1 General Status Register 1
DDR_PUBL_DX1DLLCR	0x020c	W	0x40000000	DATX8 1 DLL Control Register
DDR_PUBL_DX1DQTR	0x0210	W	0xffffffff	DATX8 1 DQ Timing Register

Name	Offset	Size	Reset Value	Description
DDR_PUBL_DX1DQSTR	0x0214	W	0x3db05000	DATX8 1 DQS Timing Register
DDR_PUBL_DX2GCR	0x0240	W	0x00000681	DATX8 2 General Configuration Register
DDR_PUBL_DX2GSR0	0x0244	W	0x00000000	DATX8 2 General Status Register 0
DDR_PUBL_DX2GSR1	0x0248	W	0x00000000	DATX8 2 General Status Register 1
DDR_PUBL_DX2DLLCR	0x024c	W	0x40000000	DATX8 2 DLL Control Register
DDR_PUBL_DX2DQTR	0x0250	W	0xffffffff	DATX8 2 DQ Timing Register
DDR_PUBL_DX2DQSTR	0x0254	W	0x3db05000	DATX8 2 DQS Timing Register
DDR_PUBL_DX3GCR	0x0280	W	0x00000681	DATX8 3 General Configuration Register
DDR_PUBL_DX3GSR0	0x0284	W	0x00000000	DATX8 3 General Status Register 0
DDR_PUBL_DX3GSR1	0x0288	W	0x00000000	DATX8 3 General Status Register 1
DDR_PUBL_DX3DLLCR	0x028c	W	0x40000000	DATX8 3 DLL Control Register
DDR_PUBL_DX3DQTR	0x0290	W	0xffffffff	DATX8 3 DQ Timing Register
DDR_PUBL_DX3DQSTR	0x0294	W	0x3db05000	DATX8 3 DQS Timing Register

Notes: **S**ize: **B** - Byte (8 bits) access, **HW** - Half WORD (16 bits) access, **W** -WORD (32 bits) access

5.5.2 Detail Registers Description

DDR_PCTL_SCFG

Address: Operational Base + offset (0x0000)

State Configuration Register

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:8	RW	0x3	<p>bbflags_timing</p> <p>The n_bbflags is a NIF output vector which provides combined information about the status of each memory bank. The de-assertion is based on when precharge, activates, reads/writes are scheduled by the TCU block.</p> <p>It may be possible to de-assert n_bbflags earlier than calculated by the TCU block. Programming bbflags_timing is used to achieve this. The maximum recommended value is: UPCTL_TCU_SED_P - TRP.t_rp.</p> <p>The programmed value is the maximum number of "early" cycles that n_bbflags maybe de-asserted. The actual achieved de-assertion depends on the traffic profile.</p> <p>In 1:2 mode the maximum allowed programmable value is 4'b0111</p> <p>In 1:1 mode the value can be 4'b1111</p>
7	RO	0x0	reserved

Bit	Attr	Reset Value	Description
6	RW	0x0	nfifo_nif1_dis For internal use only for NFIFO testing. 1'b0: Only supported setting 1'b1: For internal use only
5:1	RO	0x0	reserved
0	RW	0x0	hw_low_power_en Enables the hardware low-power interface. Allows the system to request via hardware (c_sysreq input) to enter the memories into Self-Refresh. The handshaking between the request and acknowledge hardware low power signals (c_sysreq and c_sysack, respectively) is always performed, but the uPCTL response depends on the value set on this register field and by the value driven on the c_active_in input pin. 1'b0: Disabled. Requests are always denied and uPCTL is unaffected by c_sysreq 1'b1: Enabled. Requests are accepted or denied, depending on the current operational state of uPCTL and on the value of c_active_in

DDR_PCTL_SCTL

Address: Operational Base + offset (0x0004)

Operational State Control Register

Bit	Attr	Reset Value	Description
31:3	RO	0x0	reserved
2:0	RW	0x0	state_cmd Issues an operational state transition request to the uPCTL. 3'b000: INIT (move to Init_mem from Config) 3'b001: CFG (move to Config from Init_mem or Access) 3'b010: GO (move to Access from Config) 3'b011: SLEEP (move to Low_power from Access) 3'b100: WAKEUP (move to Access from Low_power) Others: Reserved

DDR_PCTL_STAT

Address: Operational Base + offset (0x0008)

Operational State Status Register

Bit	Attr	Reset Value	Description
31:7	RO	0x0	reserved

Bit	Attr	Reset Value	Description								
6:4	RO	0x0	<p>lp_trig Reports the status of what triggered an entry to Low_power state. Is only set if in Low_power state. The individual bits report the following:</p> <ul style="list-style-type: none"> - lp_trig[2]: Software driven due to SCTL.state_cmd==SLEEP - lp_trig[1]: Hardware driven due to Hardware Low Power Interface - lp_trig[0]: Hardware driven due to Auto Self Refresh (MCFG1.sr_idle>0) <p><i>Note: if more than one trigger happens at the exact same time, more than one bit of lp_trig may be asserted high.</i></p>								
3	RO	0x0	reserved								
2:0	RO	0x0	<p>ctl_stat Returns the current operational state of the uPCTL.</p> <table> <tr><td>3'b000: Init_mem</td></tr> <tr><td>3'b001: Config</td></tr> <tr><td>3'b010: Config_req</td></tr> <tr><td>3'b011: Access</td></tr> <tr><td>3'b100: Access_req</td></tr> <tr><td>3'b101: Low_power</td></tr> <tr><td>3'b110: Low_power_entry_req</td></tr> <tr><td>3'b111: Low_power_exit_req</td></tr> </table>	3'b000: Init_mem	3'b001: Config	3'b010: Config_req	3'b011: Access	3'b100: Access_req	3'b101: Low_power	3'b110: Low_power_entry_req	3'b111: Low_power_exit_req
3'b000: Init_mem											
3'b001: Config											
3'b010: Config_req											
3'b011: Access											
3'b100: Access_req											
3'b101: Low_power											
3'b110: Low_power_entry_req											
3'b111: Low_power_exit_req											

DDR_PCTL_INTRSTAT

Address: Operational Base + offset (0x000c)

Interrupt Status Register

Bit	Attr	Reset Value	Description		
31:2	RO	0x0	reserved		
1	RO	0x0	<p>parity_intr Indicates that a DFI parity error has been detected</p> <table> <tr><td>1'b0: No error</td></tr> <tr><td>1'b1: Parity error</td></tr> </table>	1'b0: No error	1'b1: Parity error
1'b0: No error					
1'b1: Parity error					
0	RO	0x0	<p>ecc_intr Indicates that an ECC error has been detected</p> <table> <tr><td>1'b0: No error</td></tr> <tr><td>1'b1: Parity error</td></tr> </table>	1'b0: No error	1'b1: Parity error
1'b0: No error					
1'b1: Parity error					

DDR_PCTL_MCMD

Address: Operational Base + offset (0x0040)

Memory Command Register

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31	RWSC	0x0	<p>start_cmd</p> <p>Start command. When this bit is set to 1, the command operation defined in the cmd_opcode field is started. This bit is automatically cleared by the uPCTL after the command is finished. The application can poll this bit to determine when uPCTL is ready to accept another command. This bit cannot be cleared to 1'b0 by software.</p>
30:28	RO	0x0	reserved
27:24	RW	0x0	<p>cmd_add_del</p> <p>Set the additional delay associated with each command to 2^n internal timers clock cycles, where n is the bit field value. If n=0, the delay is 0. Max value is n=10.</p>
23:20	RW	0x1	<p>rank_sel</p> <p>Rank select for the command to be executed.</p> <p>4'b0001: Rank 0 4'b0010: Rank 1 4'b0100: Rank 2 4'b1000: Rank 3 4'b0000: Reserved</p> <p>Multiple 1'b1s in rank_sel mean multiple ranks are selected, which is useful broadcasting commands in parallel to multiple ranks during initialization and configuration of the memories.</p> <p>If MCMD.cmd_opcode=RSTL, all ranks should be selected as it cannot be performed to individual ranks.</p>
19:17	RW	0x0	<p>bank_addr</p> <p>Mode Register address driven on the memory bank address bits, BA1, BA0, during a Mode Register Set operation, defined by cmd_opcode=MRS. For other values of cmd_opcode, this field is ignored.</p> <p>3'b000: MR0 (MR in DDR2) 3'b001: MR1 (EMR in DDR2) 3'b010: MR2 (EMR(2) in DDR2) 3'b011: MR3 (EMR(3) in DDR2) Others: Reserved</p>

Bit	Attr	Reset Value	Description
16:4	RW	0x0000	cmd_addr Mode Register value driven on the memory address bits, A12 to A0, during a Mode Register Set operation defined by cmd_opcode=MRS. For other values of cmd_opcode this field is ignored. Refer to the memory specification for the correct settings of the various bits of this field during a MRS operation. If LPDDR2, this fields is merged into bank_addr - lpddr2_addr.
3:0	RW	0x0	cmd_opcode Command to be issued to the memory. 4'b0000: Deselect. This is only used for timing purposes, no actual direct Deselect command is passed to the memories 4'b0001: Precharge All (PREA) 4'b0010: Refresh (REF) 4'b0011: Mode Register Set (MRS) - is MRW in LPDDR2, MRS otherwise 4'b0100: ZQ Calibration Short (ZQCS, only applies to LPDDR2/DDR3) 4'b0101: ZQ Calibration Long (ZQCL, only applies to LPDDR2/DDR3) 4'b0110: Software Driven Reset (RSTL, only applies to DDR3) 4'b0111: Reserved 4'b1000: Mode Register Read (MRR) - is MRR in LPDDR2, is SRR in mDRR and is MPR in DDR3 4'b1001: Deep Power Down Entry (DPDE, only applies to mDDR/LPDDR2) Others: Reserved

DDR_PCTL_POWCTL

Address: Operational Base + offset (0x0044)

Power Up Control Register

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RWSC	0x0	power_up_start Start the memory power up sequence. When this bit is set to 1'b1, uPCTL starts the CKE and RESET power up sequence to the memories. This bit is automatically cleared by uPCTL after the sequence is completed. This bit cannot be cleared to 1'b0 by software.

DDR_PCTL_POWSTAT

Address: Operational Base + offset (0x0048)

Power Up Status Register

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RO	0x0	power_up_done Returns the status of the memory power-up sequence. 1'b0: Power-up sequence has not been performed 1'b1: Power-up sequence has been performed

DDR_PCTL_CMDTSTAT

Address: Operational Base + offset (0x004c)

Command Timers Status Register

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RO	0x0	cmd_tstat Returns the status of the timers for memory commands. This ANDs all the command timers together. 1'b0: One or more command timers has not expired 1'b1: All command timers have expired

DDR_PCTL_CMDTSTATEN

Address: Operational Base + offset (0x0050)

Command Timers Status Enable Register

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	cmd_tstat_en Enables the generation of the status of the timers for memory commands. Is enabled before CMDTSTAT register is read. 1'b0: Disabled 1'b1: Enabled

DDR_PCTL_MRRCFG0

Address: Operational Base + offset (0x0060)

Mode Register Read Configuration 0

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved

Bit	Attr	Reset Value	Description
3:0	RW	0x0	mrr_byte_sel Selects which byte's data to store when performing an MRR command via MCMD. LegalValues: 0 .. 8

DDR_PCTL_MRRSTAT0

Address: Operational Base + offset (0x0064)

Mode Register Read Status 0 Register

Bit	Attr	Reset Value	Description
31:24	RO	0x00	mrrstat_beat3 MRR/MPR read data beat 3
23:16	RO	0x00	mrrstat_beat2 MRR/MPR read data beat 2
15:8	RO	0x00	mrrstat_beat1 MRR/MPR read data beat 1
7:0	RO	0x00	mrrstat_beat0 MRR/MPR read data beat 0

DDR_PCTL_MRRSTAT1

Address: Operational Base + offset (0x0068)

Mode Register Read Status 0 Register

Bit	Attr	Reset Value	Description
31:24	RO	0x00	mrrstat_beat7 MRR/MPR read data beat 7
23:16	RO	0x00	mrrstat_beat6 MRR/MPR read data beat 6
15:8	RO	0x00	mrrstat_beat5 MRR/MPR read data beat 5
7:0	RO	0x00	mrrstat_beat4 MRR/MPR read data beat 4

DDR_PCTL_MCFG

Address: Operational Base + offset (0x0080)

Memory Configuration Register

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:24	RW	0x00	mddr_lpddr2_clock_stop_idle Clock stop idle period in n_clk cycles. Memories are placed into clock stop mode if the NIF is idle for mddr_lpddr2_clkstop_idle n_clk cycles. The automatic clock stop function is disabled when mddr_lpddr2_clkstop_idle=0. Clock stop mode is only applicable in mDDR/LPDDR2.
23:22	RW	0x0	mddr_lpddr2_en mDDR/LPDDR2 Enable. Enables support for mDDR or LPDDR2. 2'b00: mDDR/LPDDR2 Disabled 2'b10: mDDR Enabled 2'b11: LPDDR2 Enabled Others: Reserved.
21:20	RW	0x0	mddr_lpddr2_bl mDDR/LPDDR2 Burst Length. The BL setting must be consistent with the value programmed into the BL field of MR. 2'b00: BL2, Burst length of 2 (MR.BL=3'b001, mDDR only) 2'b01: BL4, Burst length of 4 (MR.BL=3'b010, for mDDR and LPDDR2) 2'b10: BL8, Burst length of 8 (MR.BL=3'b011, for mDDR and LPDDR2) 2'b11: BL16, Burst length of 16 (MR.BL=3'b100, for mDDR and LPDDR2) This value is effective only if MCFG.mddr_lpddr2_en[1]=1'b1. Otherwise, MCFG.mem_bl is used to define uPCTL's Burst Length (for DDR2/DDR3).
19:18	RW	0x1	tfaw_cfg Sets tFAW to be 4, 5 or 6 times tRRD. 2'b00: set tFAW=4*tRRD 2'b01: set tFAW=5*tRRD 2'b10: set tFAW=6*tRRD
17	RW	0x0	pd_exit_mode Selects the mode for Power Down Exit. For DDR2/DDR3, the power down exit mode setting in uPCTL must be consistent with the value programmed into the power down exit mode bit of MR0. For mDDR/LPDDR2, only fast exit mode is valid. 1'b0: slow exit 1'b1: fast exit

Bit	Attr	Reset Value	Description
16	RW	0x0	pd_type Sets the Power down type. 1'b0: Precharge Power Down 1'b1: Active Power Down
15:8	RW	0x00	pd_idle Power-down idle period in n_clk cycles. Memories are placed into power-down mode if the NIF is idle for pd_idle n_clk cycles. The automatic power down function is disabled when pd_idle=0.
7	RO	0x0	reserved
6	RW	0x0	lpddr2_s4 Enables LPDDR2-S4 support. 1'b0: LPDDR2-S4 disabled (LPDDR2-S2 enabled) 1'b1: LPDDR2-S4 enabled
5	RW	0x1	ddr3_en Select DDR2 or DDR3 protocol. Ignored, if mDDR or LPDDR2 support is enabled. 1'b0: DDR2 Protocol Rules 1'b1: DDR3 Protocol Rules
4	RW	0x0	stagger_cs For multi-rank commands from the DCU, stagger the assertion of CS_N to odd and even ranks by one n_clk cycle. This is useful when using RDIMMs, when multi-rank commands may be interpreted as writes to control words in the register chip. 1'b0: Do not stagger CS_N 1'b1: Stagger CS_N
3	RW	0x0	two_t_en Enables 2T timing for memory commands. 1'b0: Disabled 1'b1: Enabled
2	RW	0x0	bl8int_en Setting this bit enables the BL8 interrupt function of DDR2. This is the capability to early terminate a BL8 after only 4 DDR beats by issuing the next command two cycles earlier. This functionality is only available for DDR2 memories and this setting is ignored for mDDR/LPDDR2 and DDR3. 1'b0: Disabled 1'b1: Enabled

Bit	Attr	Reset Value	Description
1	RW	0x0	<p>cke_or_en</p> <p>This bit is intended to be set for 4-rank RDIMMs, which have a 2-bit CKE input. If set, dfi_cke[0] is asserted to enable either of the even ranks (0 and 2), while dfi_cke[1] is asserted to enable either of the odd ranks (1 and 3). dfi_cke[3:2] are inactive (0)</p> <p>1'b0: Disabled 1'b1: Enabled</p>
0	RW	0x0	<p>mem_bl</p> <p>DDR Burst Length. The BL setting in DDR2 / DDR3 must be consistent with the value programmed into the BL field of MR0.</p> <p>1'b0: BL4, Burst length of 4 (MR0.BL=3'b010, DDR2 only) 1'b1: BL8, Burst length of 8 (MR0.BL=3'b011 for DDR2, MR0.BL=2'b00 for DDR3)</p>

DDR_PCTL_PPCFG

Address: Operational Base + offset (0x0084)

Partially Populated Memories Configuration Register

Bit	Attr	Reset Value	Description
31:9	RO	0x0	reserved
8:1	RW	0x00	<p>rpmem_dis</p> <p>Reduced Population Disable bits. Setting these bits disables the corresponding NIF/DDR data lanes from writing or reading data. Lane 0 is always present, hence only 8 bits are required for the remaining lanes including the ECC lane.</p> <p>In 1:2 mode bit 0 of rpmem_dis covers n_wdata/n_rdata/m_ctl_d/m_phy_q[63:32], bit 1 [95:64] etc.</p> <p>In 1:1 mode bit 0 of rpmem_dis covers n_wdata/n_rdata/m_ctl_d/m_phy_q[31:16], bit 2 [47:32] etc.</p> <p>There are no restrictions on which byte lanes can be disabled, other than byte lane 0 is required. Gaps between enabled byte lanes are allowed.</p> <p>For each bit:</p> <p>1'b0: lane exists 1'b1: lane is disabled</p>

Bit	Attr	Reset Value	Description
0	RW	0x0	<p>ppmem_en</p> <p>Partially Population Enable bit. Setting this bit enables the partial population of external memories where the entire application bus is routed to a reduced size memory system. The lower half of the SDRAM data bus, bit 0 up to bit UPCTL_M_DW/2-1, is the active portion when Partially Populated memories are enabled.</p> <p>1'b0: Disabled 1'b1: Enabled</p>

DDR_PCTL_MSTAT

Address: Operational Base + offset (0x0088)

Memory Status Register

Bit	Attr	Reset Value	Description
31:3	RO	0x0	reserved
2	RO	0x0	<p>self_refresh</p> <p>Indicates if uPCTL, through auto self refresh, has placed the memories in Self Refresh.</p> <p>1'b0: Memory is not in Self Refresh 1'b1: Memory is in Self Refresh</p>
1	RO	0x0	<p>clock_stop</p> <p>Indicates if uPCTL has placed the memories in Clock Stop.</p> <p>1'b0: Memory is not in Clock Stop 1'b1: Memory is in Clock Stop</p>
0	RO	0x0	<p>power_down</p> <p>Indicates if uPCTL has placed the memories in Power Down.</p> <p>1'b0: Memory is not in Power Down 1'b1: Memory is in Power-Down</p>

DDR_PCTL_LPDDR2ZQCFG

Address: Operational Base + offset (0x008c)

LPDDR2 ZQ Configuration Register

Bit	Attr	Reset Value	Description
31:24	RW	0xab	<p>zqcl_op</p> <p>Value to drive on memory address bits [19:12] for an automatic hardware generated ZQCL command (LPDDR2). Corresponds to OP7 .. OP0 of Mode Register Write (MRW) command which is used to send ZQCL command to memory.</p>

Bit	Attr	Reset Value	Description
23:16	RW	0x0a	zqcl_ma Value to drive on memory address bits [11:4] for an automatic hardware generated ZQCL command (LPDDR2). Corresponds to MA7 .. MA0 of Mode Register Write (MRW) command which is used to send ZQCL command to memory.
15:8	RW	0x56	zqcs_op Value to drive on memory address bits [19:12] for an automatic hardware generated ZQCS command (LPDDR2). Corresponds to OP7 .. OP0 of Mode Register Write (MRW) command which is used to send ZQCS command to memory.
7:0	RW	0x0a	zqcs_ma Value to drive on memory address bits [11:4] for an automatic hardware generated ZQCS command (LPDDR2). Corresponds to MA7 .. MA0 of Mode Register Write (MRW) command which is used to send ZQCS command to memory.

DDR_PCTL_MCFG1

Address: Operational Base + offset (0x0090)

Memory Configuration 1 Register

Bit	Attr	Reset Value	Description
31	RW	0x0	hw_exit_idle_en When this bit is programmed to 1'b1 the c_active_in pin can be used to exit from the automatic clock stop, power down or self-refresh modes.
30:24	RO	0x0	reserved
23:16	RW	0x00	hw_idle Hardware idle period. The c_active output is driven high if the NIF is idle in Access state for hw_idle * 32 * n_clk cycles. The hardware idle function is disabled when hw_idle=0.
15:8	RO	0x0	reserved
7:0	RW	0x00	sr_idle Self Refresh idle period. Memories are placed into Self-Refresh mode if the NIF is idle in Access state for sr_idle * 32 * n_clk cycles. The automatic self refresh function is disabled when sr_idle=0.

DDR_PCTL_DTUPDES

Address: Operational Base + offset (0x0094)

DTU Status Register

Bit	Attr	Reset Value	Description
31:14	RO	0x0	reserved
13	RO	0x0	dtu_rd_missing Indicates if one or more read beats of data did not return from memory
12:9	RO	0x0	dtu_eaffl Indicates the number of entries in the FIFO that is holding the log of error addresses for data comparison
8	RO	0x0	dtu_random_error Indicates that the random data generated had some failures when written and read to the memories
7	RO	0x0	dtu_err_b7 Detected at least 1 bit error for bit 7 in the programmable data buffers
6	RO	0x0	dtu_err_b6 Detected at least 1 bit error for bit 6 in the programmable data buffers
5	RO	0x0	dtu_err_b5 Detected at least 1 bit error for bit 5 in the programmable data buffers
4	RO	0x0	dtu_err_b4 Detected at least 1 bit error for bit 4 in the programmable data buffers
3	RO	0x0	dtu_err_b3 Detected at least 1 bit error for bit 3 in the programmable data buffers
2	RO	0x0	dtu_err_b2 Detected at least 1 bit error for bit 2 in the programmable data buffers
1	RO	0x0	dtu_err_b1 Detected at least 1 bit error for bit 1 in the programmable data buffers
0	RO	0x0	dtu_err_b0 Detected at least 1 bit error for bit 0 in the programmable data buffers

DDR_PCTL_DTUNA

Address: Operational Base + offset (0x0098)

DTU Number of Addresses Created Register

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	dtu_num_address Indicates the number of addresses that were created on the NIF interface during random data generation

DDR_PCTL_DTUNE

Address: Operational Base + offset (0x009c)

DTU Number of Errors Register

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	dtu_num_errors Indicates the number of errors that were detected on the readback of the NIF data during random data generation.

DDR_PCTL_DTUPRDO

Address: Operational Base + offset (0x00a0)

DTU Parallel Read 0 Register

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	dtu_allbits_1 Allows all the bit ones from each of the 16 received read bytes to be read in parallel. Used as part of read data eye training where a transition is required to be monitored to train the eye.
15:0	RO	0x0000	dtu_allbits_0 Allows all the bit zeros from each of the 16 received read bytes to be read in parallel. Used as part of read data eye training where a transition is required to be monitored to train the eye.

DDR_PCTL_DTUPRD1

Address: Operational Base + offset (0x00a4)

DTU Parallel Read 1 Register

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	dtu_allbits_3 Allows all the bit threes from each of the 16 received read bytes to be read in parallel. Used as part of read data eye training where a transition is required to be monitored to train the eye.
15:0	RO	0x0000	dtu_allbits_2 Allows all the bit twos from each of the 16 received read bytes to be read in parallel. Used as part of read data eye training where a transition is required to be monitored to train the eye.

DDR_PCTL_DTUPRD2

Address: Operational Base + offset (0x00a8)

DTU Parallel Read 2 Register

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	dtu_allbits_5 Allows all the bit fives from each of the 16 received read bytes to be read in parallel. Used as part of read data eye training where a transition is required to be monitored to train the eye.
15:0	RO	0x0000	dtu_allbits_4 Allows all the bit fours from each of the 16 received read bytes to be read in parallel. Used as part of read data eye training where a transition is required to be monitored to train the eye.

DDR_PCTL_DTUPRD3

Address: Operational Base + offset (0x00ac)

DTU Parallel Read 3 Register

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	dtu_allbits_7 Allows all the bit sevens from each of the 16 received read bytes to be read in parallel. Used as part of read data eye training where a transition is required to be monitored to train the eye.
15:0	RO	0x0000	dtu_allbits_6 Allows all the bit sixes from each of the 16 received read bytes to be read in parallel. Used as part of read data eye training where a transition is required to be monitored to train the eye.

DDR_PCTL_DTUAWDT

Address: Operational Base + offset (0x00b0)

DTU Address Width Register

Bit	Attr	Reset Value	Description
31:11	RO	0x0	reserved
10:9	RW	0x1	number_ranks Number of supported memory ranks. 2'b00: 1 rank 2'b01: 2 ranks 2'b10: 3 ranks 2'b11: 4 ranks
8	RO	0x0	reserved

Bit	Attr	Reset Value	Description
7:6	RW	0x2	row_addr_width Width of the memory row address bits. 2'b00: 13 bits wide 2'b01: 14 bits wide 2'b10: 15 bits wide 2'b11: 16 bits wide
5	RO	0x0	reserved
4:3	RW	0x2	bank_addr_width Width of the memory bank address bits. 2'b00: 2 bits wide (4 banks) 2'b01: 3 bits wide (8 banks) Others: Reserved
2	RO	0x0	reserved
1:0	RW	0x0	column_addr_width Width of the memory column address bits. 2'b00: 7 bits wide 2'b01: 8 bits wide 2'b10: 9 bits wide 2'b11: 10 bits wide

DDR_PCTL_TOGCNT1U

Address: Operational Base + offset (0x00c0)

Toggle Counter 1us Register

Bit	Attr	Reset Value	Description
31:10	RO	0x0	reserved
9:0	RW	0x064	toggle_counter_1u The number of internal timers clock cycles

DDR_PCTL_TINIT

Address: Operational Base + offset (0x00c4)

t_init Timing Register

Bit	Attr	Reset Value	Description
31:9	RO	0x0	reserved
8:0	RW	0x0c8	t_init Defines the time period (in us) to hold dfi_cke and dfi_reset_n stable during the memory power up sequence. The value programmed must correspond to at least 200us. The actual time period defined is TINIT * TOGCNT1U * internal timers clock period.

DDR_PCTL_TRSTH

Address: Operational Base + offset (0x00c8)
t_rsth Timing Register

Bit	Attr	Reset Value	Description
31:10	RO	0x0	reserved
9:0	RW	0x000	t_rsth Defines the time period (in us) to hold the dfi_reset_n signal high after it is de-asserted during the DDR3 Power Up/Reset sequence. The value programmed for DDR3 must correspond to minimum 500us of delay. For mDDR and DDR2, this register should be programmed to 0. The actual time period defined is TRSTH * TOGCNT1U * internal timers clock period.

DDR_PCTL_TOGCNT100N

Address: Operational Base + offset (0x00cc)
Toggle Counter 100ns

Bit	Attr	Reset Value	Description
31:7	RO	0x0	reserved
6:0	RW	0x01	toggle_counter_100n The number of internal timers clock cycles

DDR_PCTL_TREFI

Address: Operational Base + offset (0x00d0)
t_refi Timing Register

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RW	0x01	t_refi Defines the time period (in 100ns units) of the Refresh interval. The actual time period defined is TREFI * TOGCNT100N * internal timers clock period.

DDR_PCTL_TMRD

Address: Operational Base + offset (0x00d4)
t_mrd Timing Register

Bit	Attr	Reset Value	Description
31:3	RO	0x0	reserved

Bit	Attr	Reset Value	Description
2:0	RW	0x1	t_mrd Mode Register Set command cycle time in memory clock cycles. mDDR: Time from MRS to any valid command LPDDR2: Time from MRS (MRW) to any valid command DDR2: Time from MRS to any valid command DDR3: Time from MRS to MRS command mDDR Legal Values: 2 LPDDR2 Legal Values: 5 DDR2 Legal Values: 2..3 DDR3 Legal Values: 2..4

DDR_PCTL_TRFC

Address: Operational Base + offset (0x00d8)

t_rfc Timing Register

Bit	Attr	Reset Value	Description
31:9	RO	0x0	reserved
8:0	RW	0x001	t_rfc Refresh to Active/Refresh command time in memory clock cycles. mDDR Legal Values: 7..28 LPDDR2 Legal Values: 15..112 DDR2 Legal Values: 15..131 DDR3 Legal Values: 36.. 374

DDR_PCTL_TRP

Address: Operational Base + offset (0x00dc)

t_trp Timing Register

Bit	Attr	Reset Value	Description
31:18	RO	0x0	reserved
17:16	RW	0x1	prea_extra Additional cycles required for a Precharge All (PREA) command - in addition to t_rp. In terms of memory clock cycles. mDDR Value: 0 LPDDR2 Value: Value that corresponds (tRPab -tRPpb). Rounded up in terms of memory clock cycles. Values can be 0, 1, 2. DDR2 Value: 1 if 8 Banks, 0 otherwise DDR3 Value: 0
15:4	RO	0x0	reserved

Bit	Attr	Reset Value	Description
3:0	RW	0x6	t_rp Precharge period in memory clock cycles. For LPDDR2, this should be set to TRPpb. mDDR Legal Values: 2..3 LPDDR2 Legal Values: 3..13 DDR2 Legal Values: 3..7 DDR3 Legal Values: 5..14

DDR_PCTL_TRTW

Address: Operational Base + offset (0x00e0)

t_rtw Timing Register

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved
3:0	RW	0x2	t_rtw Read to Write turnaround time in memory clock cycles. mDDR Legal Values: 3..11 LPDDR2 Legal Values: 1..11 DDR2 Legal Values: 2..10 DDR3 Legal Values: 2..10

DDR_PCTL_TAL

Address: Operational Base + offset (0x00e4)

AL Register

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved
3:0	RW	0x0	t_al Additive Latency in memory clock cycles. For DDR2 this must match the value programmed into the AL field of MR1. For DDR3 this must be 0, CL-1, CL-2 depending weather the AL value in MR1 is 0,1, or 2 respectively. CL is the CAS latency programmed into MR0. For mDDR and LPDDR2, there is no AL field in the mode registers, and this setting should be set to 0 mDDR Legal Values: 0 LPDDR2 Legal Values: 0 DDR2 Legal Values: AL DDR3 Legal Values: 0, CL-1, CL-2 (depending on AL=0,1,2 in MR1)

DDR_PCTL_TCL

Address: Operational Base + offset (0x00e8)

CL Timing Register

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved
3:0	RW	0x4	t_cl CAS Latency in memory clock cycles. If mDDR/DDR2/DDR3, the uPCTL setting must match the value programmed into the CL field of MR0. If LPDDR2, the uPCTL setting must match RL (ReadLatency), where RL is the value programmed into the "RL & W" field of MR2 mDDR/DDR2/3 Legal Value: CL LPDDR2 Legal Value: RL

DDR_PCTL_TCWL

Address: Operational Base + offset (0x00ec)

CWL Timing Register

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved
3:0	RW	0x3	t_cwl CAS Write Latency in memory clock cycles. For mDDR, the setting must be 1. For LPDDR2 the setting must match WL (Write Latency), where WL is the value programmed into the "RL & WL" field of MR2. For DDR2 the setting must match CL-1, where CL is the value programmed into the CL field of MR0. For DDR3, the setting must match the value programmed in the memory CWL field of MR2. mDDR Legal Value: 1 LPDDR2 Legal Values: WL DDR2 Legal Value: CL-1 DDR3 Legal Value: CWL

DDR_PCTL_TRAS

Address: Operational Base + offset (0x00f0)

t_ras Timing Register

Bit	Attr	Reset Value	Description
31:6	RO	0x0	reserved

Bit	Attr	Reset Value	Description
5:0	RW	0x10	t_ras Activate to Precharge command time in memory clock cycles. mDDR Legal Values: 4..8 LPDDR2 Legal Values: 7..23 DDR2 Legal Values: 8..24 DDR3 Legal Values: 15..38

DDR_PCTL_TRC

Address: Operational Base + offset (0x00f4)

t_rc Timing Register

Bit	Attr	Reset Value	Description
31:6	RO	0x0	reserved
5:0	RW	0x16	t_rc Row Cycle time in memory clock cycles. Specifies the minimum Activate to Activate distance for accesses to same bank. mDDR Legal Values: 5..11 LPDDR2 Legal Values: 10..36 DDR2 Legal Values: 11..31 DDR3 Legal Values: 20..52

DDR_PCTL_TRCD

Address: Operational Base + offset (0x00f8)

t_rcd Timing Register

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved
3:0	RW	0x6	t_rcd Row to Column delay in memory clock cycles. Specifies the minimum Activate to Column distance. mDDR Legal Values: 2..3 LPDDR2 Legal Values: 3..13 DDR2 Legal Values: 3..7 DDR3 Legal Values: 5..14

DDR_PCTL_TRRD

Address: Operational Base + offset (0x00fc)

t_rrd Timing Register

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved

Bit	Attr	Reset Value	Description
3:0	RW	0x4	t_rrd Row-to-Row delay in memory clock cycles. Specifies the minimum Activate-to-Activate distance for consecutive accesses to different banks in the same rank. mDDR Legal Values: 1..2 LPDDR2 Legal Values: 2..6 DDR2 Legal Values: 2..6 DDR3 Legal Values: 4..8

DDR_PCTL_TRTP

Address: Operational Base + offset (0x0100)

t_rtp Timing Register

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved
3:0	RW	0x3	t_rtp Read to Precharge time in memory clock cycles. Specifies the minimum distance Read to Precharge for consecutive accesses to same bank. mDDR Value: 0 LPDDR2 Legal Values: 2..4 DDR2 Legal Values: 2..4 DDR3 Legal Values: 3..8

DDR_PCTL_TWR

Address: Operational Base + offset (0x0104)

t_wr Register

Bit	Attr	Reset Value	Description
31:5	RO	0x0	reserved
4:0	RW	0x06	t_wr Write recovery time in memory clock cycles. When using close page the uPCTL setting must be consistent with the WR field setting of MR0. mDDR Legal Values: 2..3 LPDDR2 Legal Values: 3..8 DDR2 Legal Values: 3..8 DDR3 Legal Values: 6..16

DDR_PCTL_TWTR

Address: Operational Base + offset (0x0108)

t_wtr Timing Register

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved
3:0	RW	0x4	t_wtr Write to Read turnaround time, in memory clock cycles. mDDR Legal Values: 1..2 LPDDR2 Legal Values: 2..4 DDR2 Legal Values: 2..4 DDR3 Legal Values: 3..8

DDR_PCTL_TEXSR

Address: Operational Base + offset (0x010c)

t_exsr Timing Register

Bit	Attr	Reset Value	Description
31:10	RO	0x0	reserved
9:0	RW	0x001	t_exsr Exit Self Refresh to first valid command delay, in memory clock cycles. For mDDR, this should be programmed to match tXSR. For LPDDR2, this should be programmed to match tXSR. For DDR2, this should be programmed to match tXSRD (SRE to read-related command) as defined by the memory device specification. For DDR3, this should be programmed to match tXSDL (SRE to a command requiring DLL locked) as defined by the memory device specification. mDDR Legal Values: 17..40 LPDDR2 Legal Values: 17..117 DDR2 Typical Value: 200 DDR3 Typical Value: 512

DDR_PCTL_TXP

Address: Operational Base + offset (0x0110)

t_xp Timing Register

Bit	Attr	Reset Value	Description
31:3	RO	0x0	reserved
2:0	RW	0x1	t_xp Exit Power Down to first valid command delay when DLL is on (fast exit), measured in memory clock cycles. Legal Values: 1..7

DDR_PCTL_TXPDLL

Address: Operational Base + offset (0x0114)

t_xpdll Timing Register

Bit	Attr	Reset Value	Description
31:6	RO	0x0	reserved
5:0	RW	0x00	t_xpdll Exit Power Down to first valid command delay when DLL is off (slow exit), measured in memory clock cycles. mDDR/LPDDR2 Value: 0 DDR2/DDR3 Legal Values: 3..63

DDR_PCTL_TZQCS

Address: Operational Base + offset (0x0118)

t_zqcs Timing Register

Bit	Attr	Reset Value	Description
31:7	RO	0x0	reserved
6:0	RW	0x00	t_zqcs SDRAM ZQ Calibration Short period, in memory clock cycles. Should be programmed to match the tZQCS timing value as defined in the memory specification. mDDR Value: 0 LPDDR2 Legal Values: 15..48 DDR2 Value: 0 DDR3 Typical Value: 64

DDR_PCTL_TZQCSI

Address: Operational Base + offset (0x011c)

t_zqcsi Timing Register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	t_zqcsi SDRAM ZQCS interval, measured in Refresh interval units. The total time period defined is TZQCSI*TREFI * TOGCNT100N * internal timers clock period. Programming a value of 0 in t_zqcsi disables the auto-ZQCS functionality in uPCTL. mDDR Value: 0 LPDDR2 Legal Values: 0..4294967295 DDR2 Value: 0 DDR3 Legal Values: 0..4294967295

DDR_PCTL_TDQS

Address: Operational Base + offset (0x0120)

t_dqs Timing Register

Bit	Attr	Reset Value	Description
31:3	RO	0x0	reserved
2:0	RW	0x1	t_dqs Additional data turnaround time in memory clock cycles for accesses to different ranks. Used to increase the distance between column commands to different ranks, allowing more tolerance as the driver source changes on the bidirectional DQS and/or DQ signals. mDDR Legal Values: 1..7 LPDDR2 Legal Values: 1..7 DDR2 Legal Values: 1..7 DDR3 Legal Values: 1..7

DDR_PCTL_TCKSRE

Address: Operational Base + offset (0x0124)

t_cksrc Timing Register

Bit	Attr	Reset Value	Description
31:5	RO	0x0	reserved
4:0	RW	0x00	t_cksrc In DDR3, this is the time after Self Refresh Entry that CKE is held high before going low. In memory clock cycles. Specifies the clock disable delay after SRE. This should be programmed to match the greatest value between 10ns and 5 memory clock periods. mDDR Value: 0 LPDDR2 Value: 0 DDR2 Value: 0 DDR3 Legal Values: 5..15

DDR_PCTL_TCKSRX

Address: Operational Base + offset (0x0128)

t_cksrcx Timing Register

Bit	Attr	Reset Value	Description
31:5	RO	0x0	reserved

Bit	Attr	Reset Value	Description
4:0	RW	0x00	t_cksr In DDR3, this is the time (before Self Refresh Exit) that CKE is maintained high before issuing SRX. In memory clock cycles. Specifies the clock stable time before SRX. This should be programmed to match the greatest value between 10ns and 5 memory clock periods. mDDR Value: 0 LPDDR2 Value: 0 DDR2 Value: 0 DDR3 Legal Values: 5..15

DDR_PCTL_TCKE

Address: Operational Base + offset (0x012c)

t_cke Timing Register

Bit	Attr	Reset Value	Description
31:3	RO	0x0	reserved
2:0	RW	0x3	t_cke CKE minimum pulse width in memory clock cycles. mDDR Legal Value: 2 LPDDR2 Legal Values: 3 DDR2 Legal Value: 3 DDR3 Legal Values: 3..6

DDR_PCTL_TMOD

Address: Operational Base + offset (0x0130)

t_mod Timing Register

Bit	Attr	Reset Value	Description
31:5	RO	0x0	reserved
4:0	RW	0x00	t_mod In DDR3 mode, this is the time from MRS to any valid non-MRS command (except DESELECT or NOP) in memory clock cycles. mDDR Value: 0 LPDDR2 Value: 0 DDR2 Value: 0 DDR3 Legal Values: 0..31

DDR_PCTL_TRSTL

Address: Operational Base + offset (0x0134)

Reset Low Timing Register

Bit	Attr	Reset Value	Description
31:7	RO	0x0	reserved
6:0	RW	0x00	t_rstl Memory Reset Low time, in memory clock cycles. Defines the time period to hold dfi_reset_n signal low during a software driven DDR3 Reset Operation. The value programmed must correspond to at least 100ns of delay. mDDR Value: 0 LPDDR2 Value: 0 DDR2 Value: 0 DDR3 Legal Values: 1..127

DDR_PCTL_TZQCL

Address: Operational Base + offset (0x0138)

t_zqcl Timing Register

Bit	Attr	Reset Value	Description
31:10	RO	0x0	reserved
9:0	RW	0x000	t_zqcl SDRAM ZQ Calibration Long period in memory clock cycles. If LPDDR2, should be programmed to tZQCL. If DDR3, should be programmed to match the memory tZQinit timing value for the first ZQCL command during memory initialization; should be programmed to match tZQoper timing value after reset and initialization. mDDR Value: 0 LPDDR2 Legal Values: 60..192 DDR2 Value: 0 DDR3 Legal Values: 0..1023

DDR_PCTL_TMRR

Address: Operational Base + offset (0x013c)

t_mrr Timing Register

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RW	0x02	t_mrr Time for a Mode Register Read (MRR command from MCMD)

DDR_PCTL_TCKESR

Address: Operational Base + offset (0x0140)

t_ckesr Timing Register

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved
3:0	RW	0x4	t_ckesr Minimum CKE low width for Self Refresh entry to exit timing in memory clock cycles. Recommended settings: mDDR: t_ckesr = 0 LPDDR2: t_ckesr = tCKESR setting from memories, rounded up in terms of memory cycles. DDR2: t_ckesr = 0 DDR3: t_ckesr = t_cke + 1 mDDR Value: 0 LPDDR2 Legal Values: 3..8 DDR2 Value: 0 DDR3 Legal Values: 4..7

DDR_PCTL_TDPD

Address: Operational Base + offset (0x0144)

t_dpd Timing Register

Bit	Attr	Reset Value	Description
31:10	RO	0x0	reserved
9:0	RW	0x000	t_dpd Minimum Deep Power Down time. Is in terms of us. When a MCMD.DPDE command occurs, TDPD time is waited before MCMD.start_cmd can be cleared. MCMD_cmd_add_del (if any) does not start until TDPD has completed. This ensures TDPD requirement for the memory is not violated. The actual time period defined is TDPD* TOGCNT1U * internal timers clock period. Only applies for mDDR and LPDDR2 as Deep Power Down (DPD) is only valid for these memory types. For mDDR, tDPD=0, while for LPDDR2, tDPD=500 us. For LPDDR2, if 500 us is waited externally by system, then set tDPD=0. mDDR Value: 0 LPDDR2 Legal Values: 0 or 500 DDR2 Legal Value: 0 DDR3 Legal Values: 0

DDR_PCTL_DTUWACTL

Address: Operational Base + offset (0x0200)

DTU Write Address Control

Bit	Attr	Reset Value	Description
31:30	RW	0x0	dtu_wr_rank Write rank to where data is to be targeted
29	RO	0x0	reserved
28:13	RW	0x0000	dtu_wr_row Write row to where data is to be targeted
12:10	RW	0x0	dtu_wr_bank Write bank to where data is to be targeted
9:0	RW	0x000	dtu_wr_col FWrite column to where data is to be targeted

DDR_PCTL_DTURACTL

Address: Operational Base + offset (0x0204)

DTU Read Address Control Register

Bit	Attr	Reset Value	Description
31:30	RW	0x0	dtu_rd_rank Read rank from where data comes
29	RO	0x0	reserved
28:13	RW	0x0000	dtu_rd_row Read row from where data comes
12:10	RW	0x0	dtu_rd_bank Read bank from where data comes
9:0	RW	0x000	dtu_rd_col Read column from where data comes

DDR_PCTL_DTUCFG

Address: Operational Base + offset (0x0208)

DTU Configuration Control Register

Bit	Attr	Reset Value	Description
31:23	RO	0x0	reserved
22:16	RW	0x00	dtu_row_increments Number of times to increment the row address when generating random data, up to a maximum of 127 times.
15	RW	0x0	dtu_wr_multi_rd When set puts the DTU into write once multiple reads mode
14	RW	0x0	dtu_data_mask_en Controls whether random generated data masks are transmitted. Unless enabled all data bytes are written to memory and expected to be read from memory.

Bit	Attr	Reset Value	Description
13:10	RW	0x0	dtu_target_lane Selects one of the byte lanes for data comparison into the programmable read data buffer
9	RW	0x0	dtu_generate_random Generate transfers using random data, otherwise generate transfers from the programmable write data buffers.
8	RW	0x0	dtu_incr_banks When the column address rolls over increment the bank address until we reach and conclude bank 7.
7	RW	0x0	dtu_incr_cols Increment the column address until we saturate. Return to zero if DTUCFG.dtu_incr_banks is set to 1 and we are not at bank 7.
6:1	RW	0x00	dtu_nalen Length of the NIF transfer sequence that is passed through the uPCTL for each created address.
0	RW	0x0	dtu_enable When set, allows the DTU module to take ownership of the NIF interface: 1'b1: DTU enabled 1'b0: DTU disabled

DDR_PCTL_DTUECTL

Address: Operational Base + offset (0x020c)

DTU Execute Control Register

Bit	Attr	Reset Value	Description
31:3	RO	0x0	reserved
2	R/WSC	0x0	wr_multi_rd_RST When set, resets the DTU in write once multiple reads mode, to allow a new write to be performed. This bit automatically clears.
1	R/WSC	0x0	run_error_reports When set, initiates the calculation of the error status bits. This bit automatically clears when the re-calculation is done. This is only used in debug mode to verify the comparison logic.
0	R/WSC	0x0	run_dtu When set, initiates the running of the DTU read and write transfer. This bit automatically clears when the transfers are completed.

DDR_PCTL_DTUWDO

Address: Operational Base + offset (0x0210)

DTU Write Data #0 Register

Bit	Attr	Reset Value	Description
31:24	RW	0x00	dtu_wr_byte3 Write data byte
23:16	RW	0x00	dtu_wr_byte2 Write data byte
15:8	RW	0x00	dtu_wr_byte1 Write data byte
7:0	RW	0x00	dtu_wr_byte0 Write data byte

DDR_PCTL_DTUWD1

Address: Operational Base + offset (0x0214)

DTU Write Data #1 Register

Bit	Attr	Reset Value	Description
31:24	RW	0x00	dtu_wr_byte7 Write data byte
23:16	RW	0x00	dtu_wr_byte6 Write data byte
15:8	RW	0x00	dtu_wr_byte5 Write data byte
7:0	RW	0x00	dtu_wr_byte4 Write data byte

DDR_PCTL_DTUWD2

Address: Operational Base + offset (0x0218)

DTU Write Data #2 Register

Bit	Attr	Reset Value	Description
31:24	RW	0x00	dtu_wr_byte11 Write data byte
23:16	RW	0x00	dtu_wr_byte10 Write data byte
15:8	RW	0x00	dtu_wr_byte9 Write data byte
7:0	RW	0x00	dtu_wr_byte8 Write data byte

DDR_PCTL_DTUWD3

Address: Operational Base + offset (0x021c)

DTU Write Data #3 Register

Bit	Attr	Reset Value	Description
31:24	RW	0x00	dtu_wr_byte15 Write data byte
23:16	RW	0x00	dtu_wr_byte14 Write data byte
15:8	RW	0x00	dtu_wr_byte13 Write data byte
7:0	RW	0x00	dtu_wr_byte12 Write data byte

DDR_PCTL_DTUWDM

Address: Operational Base + offset (0x0220)

DTU Write Data Mask Register

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:0	RW	0x0000	dm_wr_byte0 Write data mask bit, one bit for each byte. Each bit should be 0 for a byte lane that contains valid write data.

DDR_PCTL_DTURD0

Address: Operational Base + offset (0x0224)

DTU Read Data #0 Register

Bit	Attr	Reset Value	Description
31:24	RO	0x00	dtu_rd_byte3 Read byte
23:16	RO	0x00	dtu_rd_byte2 Read byte
15:8	RO	0x00	dtu_rd_byte1 Read byte
7:0	RO	0x00	dtu_rd_byte0 Read byte

DDR_PCTL_DTURD1

Address: Operational Base + offset (0x0228)

DTU Read Data #1 Register

Bit	Attr	Reset Value	Description
31:24	RO	0x00	dtu_rd_byte7 Read byte
23:16	RO	0x00	dtu_rd_byte6 Read byte

Bit	Attr	Reset Value	Description
15:8	RO	0x00	dtu_rd_byte5 Read byte
7:0	RO	0x00	dtu_rd_byte4 Read byte

DDR_PCTL_DTURD2

Address: Operational Base + offset (0x022c)

DTU Read Data #2 Register

Bit	Attr	Reset Value	Description
31:24	RO	0x00	dtu_rd_byte11 Read byte
23:16	RO	0x00	dtu_rd_byte10 Read byte
15:8	RO	0x00	dtu_rd_byte9 Read byte
7:0	RO	0x00	dtu_rd_byte8 Read byte

DDR_PCTL_DTURD3

Address: Operational Base + offset (0x0230)

DTU Read Data #3 Register

Bit	Attr	Reset Value	Description
31:24	RO	0x00	dtu_rd_byte15 Read byte
23:16	RO	0x00	dtu_rd_byte14 Read byte
15:8	RO	0x00	dtu_rd_byte13 Read byte
7:0	RO	0x00	dtu_rd_byte12 Read byte

DDR_PCTL_DTULFSRWD

Address: Operational Base + offset (0x0234)

DTU LFSR Seed for Write Data Generation Register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	dtu_lfsr_wseed This is the initial seed for the random write data generation LFSR (linear feedback shift register), shared with the write mask generation.

DDR_PCTL_DTULFSRRD

Address: Operational Base + offset (0x0238)

DTU LFSR Seed for Read Data Generation Register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	dtu_lfsr_rseed This is the initial seed for the random read data generation LFSR (linear feedback shift register), this is shared with the read mask generation. The read data mask is reconstructed the same as the write data mask was created, allowing the "on the fly comparison" ignore bytes which were not written.

DDR_PCTL_DTUEAF

Address: Operational Base + offset (0x023c)

DTU Error Address FIFO Register

Bit	Attr	Reset Value	Description
31:30	RO	0x0	ea_rank Indicates the rank that the error occurred in during random data generation. There could be a number of entries in this FIFO. If FIFO is empty one reads zeroes.
29	RO	0x0	reserved
28:13	RO	0x0000	ea_row Indicates the row that the error occurred in during random data generation. There could be a number of entries in this FIFO. If FIFO is empty one reads zeroes.
12:10	RO	0x0	ea_bank Indicates the bank that the error occurred in during random data generation. There could be a number of entries in this FIFO. If FIFO is empty one reads zeroes.
9:0	RO	0x000	ea_column Indicates the column address that the error occurred in during random data generation. There could be a number of entries in this FIFO. If FIFO is empty one reads zeroes.

DDR_PCTL_DFITCTRLDELAY

Address: Operational Base + offset (0x0240)

DFI tctrl_delay Register

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved
3:0	RW	0x2	tctrl_delay Specifies the number of DFI clock cycles after an assertion or deassertion of the DFI control signals that the control signals at the PHY-DRAM interface reflect the assertion or de-assertion. If the DFI clock and the memory clock are not phase-aligned, this timing parameter should be rounded up to the next integer value.

DDR_PCTL_DFIODTCFG

Address: Operational Base + offset (0x0244)

DFI ODT Configuration

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28	RW	0x0	rank3_odt_default Default ODT value of rank 3 when there is no read/write activity
27	RW	0x0	rank3_odt_write_sel Enable/disable ODT for rank 3 when a write access is occurring on this rank
26	RW	0x0	rank3_odt_write_nse Enable/disable ODT for rank 3 when a write access is occurring on a different rank
25	RW	0x0	rank3_odt_read_sel Enable/disable ODT for rank 3 when a read access is occurring on this rank
24	RW	0x0	rank3_odt_read_nsel Enable/disable ODT for rank 3 when a read access is occurring on a different rank
23:21	RO	0x0	reserved
20	RW	0x0	rank2_odt_default Default ODT value of rank 2 when there is no read/write activity
19	RW	0x0	rank2_odt_write_sel Enable/disable ODT for rank 2 when a write access is occurring on this rank
18	RW	0x0	rank2_odt_write_nse Enable/disable ODT for rank 2 when a write access is occurring on a different rank
17	RW	0x0	rank2_odt_read_sel Enable/disable ODT for rank 2 when a read access is occurring on this rank

Bit	Attr	Reset Value	Description
16	RW	0x0	rank2_odt_read_nsel Enable/disable ODT for rank 2 when a read access is occurring on a different rank
15:13	RO	0x0	reserved
12	RW	0x0	rank1_odt_default Default ODT value of rank 1 when there is no read/write activity
11	RW	0x0	rank1_odt_write_sel Enable/disable ODT for rank 1 when a write access is occurring on this rank
10	RW	0x0	rank1_odt_write_nse Enable/disable ODT for rank 1 when a write access is occurring on a different rank
9	RW	0x0	rank1_odt_read_sel Enable/disable ODT for rank 1 when a read access is occurring on this rank
8	RW	0x0	rank1_odt_read_nsel Enable/disable ODT for rank 1 when a read access is occurring on a different rank
7:5	RO	0x0	reserved
4	RW	0x0	rank0_odt_default Default ODT value of rank 0 when there is no read/write activity
3	RW	0x0	rank0_odt_write_sel Enable/disable ODT for rank 0 when a write access is occurring on this rank
2	RW	0x0	rank0_odt_write_nse Enable/disable ODT for rank 0 when a write access is occurring on a different rank
1	RW	0x0	rank0_odt_read_sel Enable/disable ODT for rank 0 when a read access is occurring on this rank
0	RW	0x0	rank0_odt_read_nsel Enable/disable ODT for rank 0 when a read access is occurring on a different rank

DDR_PCTL_DFIODTCFG1

Address: Operational Base + offset (0x0248)

DFI ODT Timing Configuration 1 (for Latency and Length)

Bit	Attr	Reset Value	Description
31:27	RO	0x0	reserved

Bit	Attr	Reset Value	Description
26:24	RW	0x6	odt_len_bl8_r ODT length for BL8 read transfers Length of dfi_odt signal for BL8 reads. This is in terms of SDR cycles. For BL4 reads, the length of dfi_odt is always 2 cycles shorter than the value in this register field.
23:19	RO	0x0	reserved
18:16	RW	0x6	odt_len_bl8_w ODT length for BL8 write transfers Length of dfi_odt signal for BL8 writes. This is in terms of SDR cycles. For BL4 writes, the length of dfi_odt is always 2 cycles shorter than the value in this register field.
15:13	RO	0x0	reserved
12:8	RW	0x00	odt_lat_r ODT latency for reads Latency after a read command that dfi_odt is set. This is in terms of SDR cycles.
7:5	RO	0x0	reserved
4:0	RW	0x00	odt_lat_w ODT latency for writes Latency after a write command that dfi_odt is set. This is in terms of SDR cycles.

DDR_PCTL_DFIODTRANKMAP

Address: Operational Base + offset (0x024c)

DFI ODT Rank Mapping

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:12	RW	0x8	odt_rank_map3 Rank mapping for dfi_odt[3] Determines whether dfi_odt[3] should be asserted Bit 15 = 1: dfi_odt[3] will be asserted to terminate rank 3 Bit 14 = 1: dfi_odt[3] will be asserted to terminate rank 2 Bit 13 = 1: dfi_odt[3] will be asserted to terminate rank 1 Bit 12 = 1: dfi_odt[3] will be asserted to terminate rank 0 This field exists only if UPCTL_M_NRANKS = 4

Bit	Attr	Reset Value	Description
11:8	RW	0x4	<p>odt_rank_map2</p> <p>Rank mapping for dfi_odt[2]</p> <p>Determines which rank access(es) will cause dfi_odt[2] to be asserted</p> <p>Bit 11 = 1: dfi_odt[2] will be asserted to terminate rank 3</p> <p>Bit 10 = 1: dfi_odt[2] will be asserted to terminate rank 2</p> <p>Bit 9 = 1: dfi_odt[2] will be asserted to terminate rank 1</p> <p>Bit 8 = 1: dfi_odt[2] will be asserted to terminate rank 0</p> <p>This field exists only if UPCTL_M_NRANKS = 4</p>
7:4	RW	0x2	<p>odt_rank_map1</p> <p>Rank mapping for dfi_odt[1]</p> <p>Determines which rank access(es) will cause dfi_odt[1] to be asserted</p> <p>Bit 7 = 1: dfi_odt[1] will be asserted to terminate rank 3</p> <p>Bit 6 = 1: dfi_odt[1] will be asserted to terminate rank 2</p> <p>Bit 5 = 1: dfi_odt[1] will be asserted to terminate rank 1</p> <p>Bit 4 = 1: dfi_odt[1] will be asserted to terminate rank 0</p>
3:0	RW	0x1	<p>odt_rank_map0</p> <p>Rank mapping for dfi_odt[0]</p> <p>Determines which rank access(es) will cause dfi_odt[0] to be asserted</p> <p>Bit 3 = 1: dfi_odt[0] will be asserted to terminate rank 3</p> <p>Bit 2 = 1: dfi_odt[0] will be asserted to terminate rank 2</p> <p>Bit 1 = 1: dfi_odt[0] will be asserted to terminate rank 1</p> <p>Bit 0 = 1: dfi_odt[0] will be asserted to terminate rank 0</p>

DDR_PCTL_DFITPHYWRDATA

Address: Operational Base + offset (0x0250)

DFI tphy_wrdata Register

Bit	Attr	Reset Value	Description
31:6	RO	0x0	reserved

Bit	Attr	Reset Value	Description
5:0	RW	0x01	tphy_wrdata Specifies the number of DFI clock cycles between when the dfi_wrdata_en signal is asserted to when the associated write data is driven on the dfi_wrdata signal. This has no impact on performance, only adjusts the relative time between enable and data transfer.

DDR_PCTL_DFITPHYWRLAT

Address: Operational Base + offset (0x0254)

DFI tphy_wrlat Register

Bit	Attr	Reset Value	Description
31:6	RO	0x0	reserved
5:0	RW	0x01	tphy_wrlat Specifies the number of DFI clock cycles between when a write command is sent on the DFI control interface and when the dfi_wrdata_en signal is asserted.

DDR_PCTL_DFITRDDATAEN

Address: Operational Base + offset (0x0260)

DFI trddata_en Register

Bit	Attr	Reset Value	Description
31:6	RO	0x0	reserved
5:0	RW	0x01	trddata_en Specifies the number of DFI clock cycles from the assertion of a read command on the DFI to the assertion of the dfi_rddata_en signal.

DDR_PCTL_DFITPHYRDLAT

Address: Operational Base + offset (0x0264)

DFI tphy_rdlat Register

Bit	Attr	Reset Value	Description
31:6	RO	0x0	reserved
5:0	RW	0x0f	tphy_rdlat Specifies the maximum number of DFI clock cycles allowed from the assertion of the dfi_rddata_en signal to the assertion of the dfi_rddata_valid signal.

DDR_PCTL_DFITPHYUPDTYPE0

Address: Operational Base + offset (0x0270)

DFI tphyupd_type0 Register

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:0	RW	0x010	tphyupd_type0 Specifies the maximum number of DFI clock cycles that the dfi_phyupd_req signal may remain asserted after the assertion of the dfi_phyupd_ack signal for dfi_phyupd_type = 0x0. The dfi_phyupd_req signal may de-assert at any cycle after the assertion of the dfi_phyupd_ack signal.

DDR_PCTL_DFITPHYUPDTYPE1

Address: Operational Base + offset (0x0274)

DFI tphyupd_type1 Register

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:0	RW	0x010	tphyupd_type1 Specifies the maximum number of DFI clock cycles that the dfi_phyupd_req signal may remain asserted after the assertion of the dfi_phyupd_ack signal for dfi_phyupd_type = 0x1. The dfi_phyupd_req signal may de-assert at any cycle after the assertion of the dfi_phyupd_ack signal.

DDR_PCTL_DFITPHYUPDTYPE2

Address: Operational Base + offset (0x0278)

DFI tphyupd_type2 Register

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:0	RW	0x010	tphyupd_type2 Specifies the maximum number of DFI clock cycles that the dfi_phyupd_req signal may remain asserted after the assertion of the dfi_phyupd_ack signal for dfi_phyupd_type = 0x2. The dfi_phyupd_req signal may de-assert at any cycle after the assertion of the dfi_phyupd_ack signal.

DDR_PCTL_DFITPHYUPDTYPE3

Address: Operational Base + offset (0x027c)

DFI tphyupd_type3 Register

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:0	RW	0x010	tphyupd_type3 Specifies the maximum number of DFI clock cycles that the dfi_phyupd_req signal may remain asserted after the assertion of the dfi_phyupd_ack signal for dfi_phyupd_type = 0x3. The dfi_phyupd_req signal may de-assert at any cycle after the assertion of the dfi_phyupd_ack signal.

DDR_PCTL_DFITCTRLUPDMIN

Address: Operational Base + offset (0x0280)

DFI tctrlupd_min Register

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:0	RW	0x0010	tctrlupd_min Specifies the minimum number of DFI clock cycles that the dfi_ctrlupd_req signal must be asserted.

DDR_PCTL_DFITCTRLUPDMAX

Address: Operational Base + offset (0x0284)

DFI tctrlupd_max Register

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:0	RW	0x0040	tctrlupd_max Specifies the maximum number of DFI clock cycles that the dfi_ctrlupd_req signal can assert.

DDR_PCTL_DFITCTRLUPDDLY

Address: Operational Base + offset (0x0288)

DFI tctrlupddly Register

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved
3:0	RW	0x8	tctrlupd_dly Delay in DFI clock cycles between time a uPCTL-initiated update could be started and time uPCTL-initiated update actually starts (dfi_ctrlupd_req going high).

DDR_PCTL_DFIUPDCFG

Address: Operational Base + offset (0x0290)

DFI Update Configuration Register

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	RW	0x1	dfi_phyupd_en Enables the support for acknowledging PHY-initiated updates: 1'b0 = Disabled 1'b1 = Enabled
0	RW	0x1	dfi_ctrlupd_en Enables the generation of uPCTL-initiated updates 1'b0: Disabled 1'b1: Enabled

DDR_PCTL_DFITREFMSKI

Address: Operational Base + offset (0x0294)

DFI Masked Refresh Interval

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RW	0x00	trefmski Time period of the masked Refresh interval. This value is only used if TREFI==0. Defines the time period (in 100ns units) of the masked Refresh (REFMSK) interval. The actual time period defined is DFITREFMSKI* TOGCNT100N * internal timers clock period.

DDR_PCTL_DFITCTRLUPDI

Address: Operational Base + offset (0x0298)

DFI tctrlupd_interval Register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	tctrlupd_interval DFI uPCTL-initiated updates interval, measured in terms of Refresh interval units. If TREFI != 0, the time period is defined as DFITCTRLUPDI*TREFI * TOGCNT100N * internal timers clock period. If TREFI == 0 and DFITREFMSKI != 0, the period changes to DFITCTRLUPDI * DFITREFMSKI * TOGCNT100N * internal timers clock period. Programming a value of 0 is the same as programming a value of 1; for instance, a uPCTL-initiated update occurs every Refresh interval.

DDR_PCTL_DFITRCFG0

Address: Operational Base + offset (0x02ac)

DFI Training Configuration 0 Register

Bit	Attr	Reset Value	Description
31:20	RO	0x0	reserved
19:16	RW	0x0	dfi_wrlvl_rank_sel Determines the value to drive on the output signal dfi_wrlvl_cs_n. The value on dfi_wrlvl_cs_n is the inverse of the setting in this field.
15:13	RO	0x0	reserved
12:4	RW	0x000	dfi_rdlvl_edge Determines the value to drive on the output signal dfi_rdlvl_edge. The value on dfi_rdlvl_edge is the same as the setting in this field.
3:0	RW	0x0	dfi_rdlvl_rank_sel Determines the value to drive on the output signal dfi_rdlvl_cs_n. The value on dfi_rdlvl_cs_n is the inverse of the setting in this field.

DDR_PCTL_DFITRSTAT0

Address: Operational Base + offset (0x02b0)

DFI Training Status 0 Register

Bit	Attr	Reset Value	Description
31:18	RO	0x0	reserved
17:16	RO	0x0	dfi_wrlvl_mode Reports the value of the input signal dfi_wrlvl_mode
15:10	RO	0x0	reserved
9:8	RO	0x0	dfi_rdlvl_gate_mode Reports the value of the input signal dfi_rdlvl_gate_mode
7:2	RO	0x0	reserved
1:0	RO	0x0	dfi_rdlvl_mode Reports the value of the input signal dfi_rdlvl_mode

DDR_PCTL_DFITRWRLVLEN

Address: Operational Base + offset (0x02b4)

DFI Training dfi_wrlvl_en Register

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:9	RO	0x0	reserved
8:0	RW	0x000	dfi_wrlvl_en Determines the value to drive on the output signal dfi_wrlvl_en

DDR_PCTL_DFITRRDLVLEN

Address: Operational Base + offset (0x02b8)

DFI Training dfi_rdlvl_en Register

Bit	Attr	Reset Value	Description
31:9	RO	0x0	reserved
8:0	RW	0x000	dfi_rdlvl_en Determines the value to drive on the output signal dfi_rdlvl_en

DDR_PCTL_DFITRRDLVLGATEEN

Address: Operational Base + offset (0x02bc)

DFI Training dfi_rdlvl_gate_en Register

Bit	Attr	Reset Value	Description
31:9	RO	0x0	reserved
8:0	RW	0x000	dfi_rdlvl_gate_en Determines the value to drive on the output signal dfi_rdlvl_gate_en

DDR_PCTL_DFISTSTAT0

Address: Operational Base + offset (0x02c0)

DFI Status Status 0 Register

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24:16	RO	0x000	dfi_data_byte_disable Reports the value of the output signal dfi_data_byte_disable
15:6	RO	0x0	reserved
5:4	RO	0x0	dfi_freq_ratio Reports the value of the output signal dfi_freq_ratio
3:2	RO	0x0	reserved
1	RO	0x0	dfi_init_start Reports the value of the output signal dfi_init_start
0	RO	0x0	dfi_init_complete Reports the value of the input signal dfi_init_complete

DDR_PCTL_DFISTCFG0

Address: Operational Base + offset (0x02c4)

DFI Status Configuration 0 Register

Bit	Attr	Reset Value	Description
31:3	RO	0x0	reserved
2	RW	0x0	<p>dfi_data_byte_disable_en Enables the driving of the dfi_data_byte_disable signal. The value driven on dfi_data_byte_disable is dependent on the setting of PPCFG register.</p> <p>1'b0: Drive dfi_data_byte_disable to default value of all zeroes 1'b1: Drive dfi_data_byte_disable according to value as defined by PPCFG register setting</p> <p><i>Note: should be set to 1'b1 only after PPCFG is correctly set</i></p>
1	RW	0x0	<p>dfi_freq_ratio_en Enables the driving of the dfi_freq_ratio signal. When enabled, the dfi_freq_ratio value driven is dependent on configuration parameter UPCTL_FREQ_RATIO: 2'b00 is driven when UPCTL_FREQ_RATIO=1; 2'b01 is driven when UPCTL_FREQ_RATIO=2.</p> <p>1'b0: Drive dfi_freq_ratio to default value of 2'b00 1'b1: Drive dfi_freq_ratio value according to how configuration parameter is set</p>
0	RW	0x0	<p>dfi_init_start Sets the value of the dfi_init_start signal</p> <p>1'b0: dfi_init_start is driven low 1'b1: dfi_init_start is driven high</p>

DDR_PCTL_DFISTCFG1

Address: Operational Base + offset (0x02c8)

DFI Status Configuration 1 Register

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	RW	0x0	<p>dfi_dram_clk_disable_en_dpd Enables support of the dfi_dram_clk_disable signal with Deep Power Down (DPD). DPD is only for mDDR/LPDDR2.</p> <p>1'b0: Disable dfi_dram_clk_disable support in relation to DPD 1'b1: Enable dfi_dram_clk_disable support in relation to DPD</p>

Bit	Attr	Reset Value	Description
0	RW	0x0	<p>dfi_dram_clk_disable_en Enables support of the dfi_dram_clk_disable signal with Self Refresh (SR).</p> <p>1'b0: Disable dfi_dram_clk_disable support in relation to SR</p> <p>1'b1: Enable dfi_dram_clk_disable support in relation to SR</p>

DDR_PCTL_DFITDRAMCLKEN

Address: Operational Base + offset (0x02d0)

DFI tdrum_clk_enable Register

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved
3:0	RW	0x2	<p>tdram_clk_enable Specifies the number of DFI clock cycles from the de-assertion of the dfi_dram_clk_disable signal on the DFI until the first valid rising edge of the clock to the DRAM memory devices, at the PHY-DRAM boundary. If the DFI clock and the memory clock are not phase aligned, this timing parameter should be rounded up to the next integer value.</p>

DDR_PCTL_DFITDRAMCLKDIS

Address: Operational Base + offset (0x02d4)

DFI tdrum_clk_disable Register

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved
3:0	RW	0x2	<p>tdram_clk_disable Specifies the number of DFI clock cycles from the assertion of the dfi_dram_clk_disable signal on the DFI until the clock to the DRAM memory devices, at the PHY-DRAM boundary, maintains a low value. If the DFI clock and the memory clock are not phase aligned, this timing parameter should be rounded up to the next integer value.</p>

DDR_PCTL_DFISTCFG2

Address: Operational Base + offset (0x02d8)

DFI Status Configuration 2 Register

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved

Bit	Attr	Reset Value	Description
1	RW	0x0	<p>parity_en</p> <p>Enables the DFI parity generation feature (driven on output signal dfi_parity_in)</p> <p>1'b0: Disable DFI parity generation</p> <p>1'b1: Enable DFI parity generation</p>
0	RW	0x0	<p>parity_intr_en</p> <p>Enable interrupt generation for DFI parity error (from input signal dfi_parity_error)</p> <p>1'b0: Disable interrupt</p> <p>1'b1: Enable interrupt</p>

DDR_PCTL_DFISTPARCLR

Address: Operational Base + offset (0x02dc)

DFI Status Parity Clear Register

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	RWSC	0x0	<p>parity_log_clr</p> <p>Set this bit to 1'b1 to clear the DFI Status Parity Log register (DFISTPARLOG)</p> <p>1'b0: Do not clear DFI status Parity Log register</p> <p>1'b1: Clear DFI status Parity Log register</p>
0	RWSC	0x0	<p>parity_intr_clr</p> <p>Set this bit to 1'b1 to clear the interrupt generated by an DFI parity error (as enabled by DFISTCFG2.parity_intr_en). It also clears the INTRSTAT.parity_intr register field. It is automatically cleared by hardware when the interrupt has been cleared.</p>

DDR_PCTL_DFISTPARLOG

Address: Operational Base + offset (0x02e0)

DFI Status Parity Log Register

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	<p>parity_err_cnt</p> <p>Increments any time the DFI parity logic detects a parity error(s) (on dfi_parity_error)</p>

DDR_PCTL_DFILPCFG0

Address: Operational Base + offset (0x02f0)

DFI Low Power Configuration 0 Register

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:28	RW	0x0	<p>dfi_lp_wakeup_dpd</p> <p>Value to drive on dfi_lp_wakeup signal when Deep Power Down mode is entered.</p> <p>Determines the DFI's tlp_wakeup time:</p> <ul style="list-style-type: none"> 4'b0000: 16 cycles 4'b0001: 32 cycles 4'b0010: 64 cycles 4'b0011: 128 cycles 4'b0100: 256 cycles 4'b0101: 512 cycles 4'b0110: 1024 cycles 4'b0111: 2048 cycles 4'b1000: 4096 cycles 4'b1001: 8192 cycles 4'b1010: 16384 cycles 4'b1011: 32768 cycles 4'b1100: 65536 cycles 4'b1101: 131072 cycles 4'b1110: 262144 cycles 4'b1111: Unlimited
27:25	RO	0x0	reserved
24	RW	0x0	<p>dfi_lp_en_dpd</p> <p>Enables DFI Low Power interface handshaking during Deep Power Down Entry/Exit</p> <ul style="list-style-type: none"> 1'b0: Disabled 1'b1: Enabled
23:20	RO	0x0	reserved
19:16	RW	0x7	<p>dfi_tlp_resp</p> <p>Setting for tlp_resp time.</p> <p>Same value is used for both Power Down and Self refresh and Deep Power Down modes.</p> <p>DFI 2.1 specification, recommends using value of 7 always.</p>

Bit	Attr	Reset Value	Description
15:12	RW	0x0	<p>dfi_lp_wakeup_sr Value to drive on dfi_lp_wakeup signal when Self Refresh mode is entered. Determines the DFI's tlp_wakeup time: 4'b0000: 16 cycles 4'b0001: 32 cycles 4'b0010: 64 cycles 4'b0011: 128 cycles 4'b0100: 256 cycles 4'b0101: 512 cycles 4'b0110: 1024 cycles 4'b0111: 2048 cycles 4'b1000: 4096 cycles 4'b1001: 8192 cycles 4'b1010: 16384 cycles 4'b1011: 32768 cycles 4'b1100: 65536 cycles 4'b1101: 131072 cycles 4'b1110: 262144 cycles 4'b1111: Unlimited</p>
11:9	RO	0x0	reserved
8	RW	0x0	<p>dfi_lp_en_sr Enables DFI Low Power interface handshaking during Self Refresh Entry/Exit 1'b0: Disabled 1'b1: Enabled</p>

Bit	Attr	Reset Value	Description
7:4	RW	0x0	<p>dfi_lp_wakeup_pd Value to drive on dfi_lp_wakeup signal when Power Down mode is entered. Determines the DFI's tlp_wakeup time: 4'b0000: 16 cycles 4'b0001: 32 cycles 4'b0010: 64 cycles 4'b0011: 128 cycles 4'b0100: 256 cycles 4'b0101: 512 cycles 4'b0110: 1024 cycles 4'b0111: 2048 cycles 4'b1000: 4096 cycles 4'b1001: 8192 cycles 4'b1010: 16384 cycles 4'b1011: 32768 cycles 4'b1100: 65536 cycles 4'b1101: 131072 cycles 4'b1110: 262144 cycles 4'b1111: Unlimited</p>
3:1	RO	0x0	reserved
0	RW	0x0	<p>dfi_lp_en_pd Enables DFI Low Power interface handshaking during Power Down Entry/Exit 1'b0: Disabled 1'b1: Enabled</p>

DDR_PCTL_DFITRWRLVLRESP0

Address: Operational Base + offset (0x0300)

DFI Training dfi_wrlvl_resp Status 0 Register

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	<p>dfi_wrlvl_resp0 Reports the status of the dfi_wrlvl_resp[31:0] signal</p>

DDR_PCTL_DFITRWRLVLRESP1

Address: Operational Base + offset (0x0304)

DFI Training dfi_wrlvl_resp Status 1 Register

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	<p>dfi_wrlvl_resp1 Reports the status of the dfi_wrlvl_resp[63:32] signal</p>

DDR_PCTL_DFITRWRLVLRESP2

Address: Operational Base + offset (0x0308)

DFI Training dfi_wrlvl_resp Status 2 Register

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RO	0x00	dfi_wrlvl_resp2 Reports the status of the dif_wrlvl_resp[71:64] signal

DDR_PCTL_DFITRRDLVLRESP0

Address: Operational Base + offset (0x030c)

DFI Training dfi_rdlvl_resp Status 0 Register

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	dfi_rdlvl_resp0 Reports the status of the dif_rdlvl_resp[31:0] signal

DDR_PCTL_DFITRRDLVLRESP1

Address: Operational Base + offset (0x0310)

DFI Training dfi_rdlvl_resp Status 1 Register

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	dfi_rdlvl_resp1 Reports the status of the dif_rdlvl_resp[63:32] signal

DDR_PCTL_DFITRRDLVLRESP2

Address: Operational Base + offset (0x0314)

DFI Training dfi_rdlvl_resp Status 2 Register

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RO	0x00	dfi_rdlvl_resp2 Reports the status of the dif_rdlvl_resp[71:64] signal

DDR_PCTL_DFITRWRLVLDELAY0

Address: Operational Base + offset (0x0318)

DFI Training dfi_wrlvl_delay Configuration 0 Register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	dfi_wrlvl_delay0 Sets the value to be driven on the signal dfi_wrlvl_delay_x[31:0]

DDR_PCTL_DFITRWRLVLDELAY1

Address: Operational Base + offset (0x031c)

DFI Training dfi_wrlvl_delay Configuration 1 Register

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	dfi_wrlvl_delay1 Sets the value to be driven on the signal dfi_wrlvl_delay_x[63:32]

DDR_PCTL_DFITRWRLVLDELAY2

Address: Operational Base + offset (0x0320)

DFI Training dfi_wrlvl_delay Configuration 2 Register

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RW	0x00	dfi_wrlvl_delay2 Sets the value to be driven on the signal dfi_wrlvl_delay_x[71:64]

DDR_PCTL_DFITRRDLVLDELAY0

Address: Operational Base + offset (0x0324)

DFI Training dfi_rdlvl_delay Configuration 0 Register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	dfi_rdlvl_delay0 Sets the value to be driven on the signal dfi_rdlvl_delay_x[31:0]

DDR_PCTL_DFITRRDLVLDELAY1

Address: Operational Base + offset (0x0328)

DFI Training dfi_rdlvl_delay Configuration 1 Register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	dfi_rdlvl_delay1 Sets the value to be driven on the signal dfi_rdlvl_delay_x[63:32]

DDR_PCTL_DFITRRDLVLDELAY2

Address: Operational Base + offset (0x032c)

DFI Training dfi_rdlvl_delay Configuration 2 Register

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RW	0x00	dfi_rdlvl_delay2 Sets the value to be driven on the signal dfi_rdlvl_delay_x[71:64]

DDR_PCTL_DFITRRDLVLGATEDELAY0

Address: Operational Base + offset (0x0330)

DFI Training dfi_rdlvl_gate_delay Configuration 0

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	dfi_rdlvl_gate_delay0 Sets the value to be driven on the signal dfi_rdlvl_gate_delay_x[31:0]

DDR_PCTL_DFITRRDLVLGATEDELAY1

Address: Operational Base + offset (0x0334)

DFI Training dfi_rdlvl_gate_delay Configuration 1

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	dfi_rdlvl_gate_delay1 Sets the value to be driven on the signal dfi_rdlvl_gate_delay_x[63:32]

DDR_PCTL_DFITRRDLVLGATEDELAY2

Address: Operational Base + offset (0x0338)

DFI Training dfi_rdlvl_gate_delay Configuration 2

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RW	0x00	dfi_rdlvl_gate_delay2 Sets the value to be driven on the signal dfi_rdlvl_gate_delay_x[71:64]

DDR_PCTL_DFITRCMD

Address: Operational Base + offset (0x033c)

DFI Training Command Register

Bit	Attr	Reset Value	Description
31	R/WSC	0x0	dfitrcmd_start DFI Training Command Start. When this bit is set to 1, the command operation defined in the dfitrcmd_opcode field is started. This bit is automatically cleared by the uPCTL after the command is finished. The application can poll this bit to determine when uPCTL is ready to accept another command. This bit cannot be cleared to 1'b0 by software.
30:13	RO	0x0	reserved
12:4	RW	0x000	dfitrcmd_en DFI Training Command Enable. Selects which bits of chosen DFI Training command to drive to 1'b1.
3:2	RO	0x0	reserved

Bit	Attr	Reset Value	Description
1:0	RW	0x0	dfitrcmd_opcode DFI Training Command Opcode. Select which DFI Training command to generate for one n_clk cycle: 2'b00: dfi_wrlvl_load 2'b01: dfi_wrlvl_strobe 2'b10: dfi_rdlvl_load 2'b11: Reserved.

DDR_PCTL_IPVR

Address: Operational Base + offset (0x03f8)

IP Version Register

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ip_version ASCII value for each number in the version, followed by a *.

DDR_PCTL_IPTR

Address: Operational Base + offset (0x03fc)

IP Type Register

Bit	Attr	Reset Value	Description
31:0	RO	0x44574300	ip_type Contains the IP's identification code, which is an ASCII value to identify the component and it is currently set to the string "DWC". This value never changes.

DDR_PUBL_RIDR

Address: Operational Base + offset (0x0000)

Revision Identification Register

Bit	Attr	Reset Value	Description
31:24	RO	0x00	UDRID User-Defined Revision ID General purpose revision identification set by the user
23:20	RO	0x1	PHYMJR PHY Major Revision Indicates major revision of the PHY such addition of the features that make the new version not compatible with previous versions

Bit	Attr	Reset Value	Description
19:16	RO	0x0	PHYMDR PHY Moderate Revision Indicates moderate revision of the PHY such as addition of new features. Normally the new version is still compatible with previous versions.
15:12	RO	0x0	PHYMNR PHY Minor Revision Indicates minor update of the PHY such as bug fixes. Normally no new features are included.
11:8	RO	0x1	PUBMJR PUB Major Revision Indicates major revision of the PUB such addition of the features that make the new version not compatible with previous versions.
7:4	RO	0x4	PUBMDR PUB Moderate Revision Indicates moderate revision of the PUB such as addition of new features. Normally the new version is still compatible with previous versions.
3:0	RO	0x0	PUBMNR PUB Minor Revision Indicates minor update of the PUB such as bug fixes. Normally no new features are included.

DDR_PUBL_PIR

Address: Operational Base + offset (0x0004)

PHY Initialization Register

Bit	Attr	Reset Value	Description
31	R/WSC	0x0	INITBYP Initialization Bypass Bypasses or stops, if set, all initialization routines currently running, including PHY initialization, DRAM initialization, and PHY training. Initialization may be triggered manually using INIT and the other relevant bits of the PIR register. This bit is self-clearing.
30	R/WSC	0x0	ZCALBYP Impedance Calibration Bypass Bypasses or stops, if set, impedance calibration of all ZQ control blocks that automatically triggers after reset. Impedance calibration may be triggered manually using INIT and ZCAL bits of the PIR register. This bit is self-clearing.

Bit	Attr	Reset Value	Description
29	RWSC	0x0	<p>LOCKBYP DLL Lock Bypass Bypasses or stops, if set, the waiting of DLLs to lock. DLL lock wait is automatically triggered after reset. DLL lock wait may be triggered manually using INIT and DLLLOCK bits of the PIR register. This bit is self-clearing.</p>
28	RWSC	0x0	<p>CLRSR Clear Status Registers A write of '1' to this bit will clear (reset to '0' all status registers, including PGSR and DXnGSR. The clear status register bit is self-clearing. This bit is primarily for debug purposes and is typically not needed during normal functional operation. It can be used when PGSR.IDONE=1, to manually clear the PGSR status bits, although starting a new init process will automatically clear the PGSR status bits. Or it can be used to manually clear the DXnGSR status bits, although starting a new data training process will automatically clear the DXnGSR status bits.</p>
27:19	RO	0x0	reserved
18	RW	0x0	<p>CTLDINIT Controller DRAM Initialization Indicates if set that DRAM initialization will be performed by the controller. Otherwise if not set it indicates that DRAM initialization will be performed using the built-in initialization sequence or using software through the configuration port.</p>
17	RW	0x0	<p>DLLBYP DLL Bypass A setting of 1 on this bit will put all PHY DLLs in bypass mode. A bypassed DLL is also powered down (disabled).</p>

Bit	Attr	Reset Value	Description
16	RW	0x0	<p>ICPC Initialization Complete Pin Configuration Specifies how the DFI 2.1 initialization complete output pin should be used to indicate the status of initialization. Valid value are: 1'b0: Asserted after PHY initialization (DLL locking and impedance calibration) is complete. 1'b1: Asserted after PHY initialization is complete and the triggered the PUBL initialization (DRAM initialization, data training, or initialization trigger with no selected initialization) is complete.</p>
15:9	RO	0x0	reserved
8	RW	0x0	<p>RVTRN Read Valid Training Executes a PUB training routine to determine the optimum position of the read valid signal for maximum system timing margins.</p>
7	RW	0x0	<p>QSTRN Read DQS Training Executes a PUBL training routine to determine the optimum position of the read data DQS strobe for maximum system timing margins.</p>
6	RW	0x0	<p>DRAMINIT DRAM Initialization Executes the DRAM initialization sequence</p>
5	RW	0x0	<p>DRAMRST DRAM Reset (DDR3 Only) Issues a reset to the DRAM (by driving the DRAM reset pin low) and wait 200us. This can be triggered in isolation or with the full DRAM initialization (DRAMINIT). For the later case, the reset is issued and 200us is waited before starting the full initialization sequence.</p>
4	RW	0x0	<p>ITMSRST Interface Timing Module Soft Reset Soft resets the interface timing modules for the data and data strobes, i.e., it asserts the ITM soft reset (srstb) signal.</p>
3	RW	0x0	<p>ZCAL Impedance Calibrate Performs PHY impedance calibration</p>
2	RW	0x0	<p>DLLLOCK DLL Lock Waits for the PHY DLLs to lock</p>

Bit	Attr	Reset Value	Description
1	RW	0x0	DLLSRST DLL Soft Rest Soft resets all PHY DLLs by driving the DLL soft reset pin
0	RW	0x0	INIT Initialization Trigger A write of '1' to this bit triggers the DDR system initialization, including PHY initialization, DRAM initialization, and PHY training. The exact initialization steps to be executed are specified in bits 1 to 6 of this register. A bit setting of 1 means the step will be executed as part of the initialization sequence, while a setting of 0 means the step will be bypassed. The initialization trigger bit is self-clearing.

DDR_PUBL_PGCR

Address: Operational Base + offset (0x0008)

PHY General Configuration Register

Bit	Attr	Reset Value	Description
31	RW	0x0	LBMODE Loopback Mode Indicates if set that the PHY/PUB is in loopback mode
30	RW	0x0	LBGDS Loopback DQS Gating Selects the DQS gating mode that should be used when the PHY is in loopback mode, including BIST loopback mode. Valid values are: 1'b0: DQS gate training will be triggered on the PUB 1'b1: DQS gate is set manually using software
29	RW	0x0	LBDQSS Loopback DQS Shift Selects how the read DQS is shifted during loopback to ensure that the read DQS is centered into the read data eye. Valid values are: 1'b0: PUB sets the read DQS delay to 0; DQS is already shifted 90 degrees by write path 1'b1: The read DQS shift is set manually through software

Bit	Attr	Reset Value	Description
28:25	RW	0x0	RFSHDT Refresh During Training A non-zero value specifies that a burst of refreshes equal to the number specified in this field should be sent to the SDRAM after training each rank except the last rank.
24	RW	0x1	PDDISDX Power Down Disabled Byte Indicates if set that the DLL and I/Os of a disabled byte should be powered down
23:22	RW	0x2	ZCKSEL Impedance Clock Divider Select Selects the divide ratio for the clock used by the impedance control logic relative to the clock used by the memory controller and SDRAM. Valid values are: 2'b00: Divide by 2 2'b01: Divide by 8 2'b10: Divide by 32 2'b11: Divide by 64
21:18	RW	0xf	RANKEN Rank Enable Specifies the ranks that are enabled for data-training. Bit 0 controls rank 0, bit 1 controls rank 1, bit 2 controls rank 2, and bit 3 controls rank 3. Setting the bit to '0' enables the rank, and setting it to '1' disables the rank.
17:16	RW	0x0	IODDRM I/O DDR Mode (D3F I/O Only) Selects the DDR mode for the I/Os
15	RW	0x0	IOLB I/O Loop-Back Select Selects where inside the I/O the loop-back of signals happens. Valid values are: 1'b0: Loopback is after output buffer; output enable must be asserted 1'b1: Loopback is before output buffer; output enable is don't care
14	RW	0x0	CKINV CK Invert Specifies if set that CK/CK# should be inverted. Otherwise CK/CK# toggles with normal polarity.

Bit	Attr	Reset Value	Description
13:12	RW	0x2	<p>CKDV CK Disable Value Specifies the static value that should be driven on CK/CK# pair(s) when the pair(s) is disabled. CKDV[0] specifies the value for CK and CKDV[1] specifies the value for CK#.</p>
11:9	RW	0x7	<p>CKEN CK Enable Controls whether the CK going to the SDRAM is enabled (toggling) or disabled (static value defined by CKDV). One bit for each of the three CK pairs.</p>
8:5	RW	0x0	<p>DTOSEL Digital Test Output Select Selects the PHY digital test output that should be driven onto PHY digital test output (phy_dto) pin: Valid values are: 4'b0000: DATX8 0 DLL digital test output 4'b0001: DATX8 1 DLL digital test output 4'b0010: DATX8 2 DLL digital test output 4'b0011: DATX8 3 DLL digital test output 4'b0100: DATX8 4 DLL digital test output 4'b0101: DATX8 5 DLL digital test output 4'b0110: DATX8 6 DLL digital test output 4'b0111: DATX8 7 DLL digital test output 4'b1000: DATX8 8 DLL digital test output 4'b1001: AC DLL digital test output 4'b1010, 4'b01111: Reserved</p>
4:3	RW	0x0	<p>DFTLMT DQS Drift Limit Specifies the expected limit of drift on read data strobes. A drift of this value or greater is reported as a drift error through the host port error flag. Valid values are: 2'b00: No limit (no error reported) 2'b01: 90 deg drift 2'b10: 180 deg drift 2'b11: 270 deg or more drift <i>Note: Although reported through the error flag, this is not an error requiring any action. It is simply an indicator that the drift is greater than expected.</i></p>

Bit	Attr	Reset Value	Description
2	RW	0x1	<p>DFTCMP DQS Drift Compensation Enables or disables DQS drift compensation. Valid values are: 1'b0: Disables data strobe drift compensation 1'b1: Enables data strobe drift compensation By default, drift compensation is enabled.</p> <p><i>Note: Drift compensation must be disabled for LPDDR2.</i></p>
1	RW	0x0	<p>DQSCFG DQS Gating Configuration Selects one of the two DQS gating schemes: 1'b0: DQS gating is shut off using the rising edge of DQS_b (active windowing mode) 1'b1: DQS gating blankets the whole burst (passive windowing mode)</p> <p><i>Note: Passive windowing must be used for LPDDR2.</i></p>
0	RW	0x0	<p>ITMDMD ITM DDR Mode Selects whether ITMS uses DQS and DQS# or it only uses DQS. Valid values are: 1'b0: ITMS uses DQS and DQS# 1'b1: ITMS uses DQS only</p> <p><i>Note: The only valid value for DDR is 1</i></p>

DDR_PUBL_PGSR

Address: Operational Base + offset (0x000c)

PHY General Status Register

Bit	Attr	Reset Value	Description
31	RO	0x0	<p>TQ Temperature Output (LPDDR Only) Connected to the DRAM TQ pin which is defined to go high when the LPDDR device temperature equals to or exceeds 85C, otherwise it is low.</p>
30:10	RO	0x0	reserved
9	RO	0x0	<p>RVEIRR Read Valid Training Intermittent Error If set, indicates that there was an intermittent error during read valid training, such as a pass was followed by a fail then followed by another pass.</p>

Bit	Attr	Reset Value	Description
8	RO	0x0	RVERR Read Valid Training Error If set, indicates that a valid read valid placement could not be found during read valid training.
7	RO	0x0	DFTERR DQS Drift Error If set, indicates that at least one of the read data strobes has drifted by more than or equal to the drift limit set in the PHY General Configuration Register (PGCR).
6	RO	0x0	DTIERR Data Training Intermittent Error If set, indicates that there was an intermittent error during data training, such as a pass was followed by a fail then followed by another pass.
5	RO	0x0	DTERR Data Training Error If set, indicates that a valid DQS gating window could not be found during data training.
4	RO	0x0	DTDONE Data Training Done Indicates, if set, that the PHY has finished doing data training
3	RO	0x0	DIDONE DRAM Initialization Done Indicates if set that DRAM initialization has completed
2	RO	0x0	ZCDONE Impedance Calibration Done Indicates if set that impedance calibration has completed
1	RO	0x0	DLDONE DLL Lock Done Indicates if set that DLL locking has completed
0	RO	0x0	IDONE Initialization Done Indicates if set that the DDR system initialization has completed. This bit is set after all the selected initialization routines in PIR register have completed.

DDR_PUBL_DLLGCR

Address: Operational Base + offset (0x0010)

DLL General Control Register

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29	RW	0x0	LOCKDET Master lock detector enable.
28	RO	0x0	reserved
27:20	RW	0x37	SBIAS Slave Bias Trim Used to trim the bias for the slave DLL
19:12	RW	0x37	MBIAS Master Bias Trim Used to trim the bias for the master DLL
11	RW	0x0	TESTSW Test Switch Selects the test signals of either the master DLL ('0') or the slave DLL ('1')
10:9	RW	0x0	ATC Analog Test Control Selects the analog signal to be output on the DLL analog test output (test_out_a) when TESTEN is high (Output is Vss when TESTEN is low). The test output either comes from the master DLL or the slave DLL, depending on the setting of the test switch (TESTSW). Both master DLL and slave DLL output similar analog test signals. Valid settings for analog test control are: 2'b00: Filter output (Vc) 2'b01: Replica bias output for NMOS (Vbn) 2'b10: Replica bias output for PMOS (Vbp) 2'b11: Vdd 00

Bit	Attr	Reset Value	Description
8:6	RW	0x0	<p>DTC Digital Test Control Selects the digital signal to be output on the DLL digital test output (test_out_d[1]) when TESTEN is high (Output is '0' when TESTEN is low).</p> <p>Valid settings for master DLL (such as, when TESTSW = '0'):</p> <ul style="list-style-type: none"> 3'b000: 0 output clock (clk_0) 3'b001: 90 output clock (clk_90) 3'b010: 180 output clock (clk_180) 3'b011: 270 output clock (clk_270) 3'b100: 360 internal clock (clk_360_int) 3'b101: Speed-up pulse (spdup) 3'b110: Slow-down pulse (slwdn) 3'b111: 0 MCTL logic clock (cclk_0) <p>Valid settings for slave DLL (such as when TESTSW = '1'):</p> <ul style="list-style-type: none"> 3'b000: Input DQS strobe (dqs) 3'b001: Input clock reference (clk_90_in) 3'b010: Internal feedback clock (clk_0_out) 3'b011: 90 output DQS_b strobe (dqsb_90) 3'b100: 90 output DQS strobe (dqs_90) 3'b101: Speed-up pulse (spdup) 3'b110: Slow-down pulse (slwdn) 3'b111: Auto-lock enable signal
5	RW	0x0	<p>TESTEN Test Enable Enables digital and analog test outputs selected by DTC and ATC respectively</p>
4:2	RW	0x0	<p>IPUMP Charge Pump Current Trim Used to trim charge pump current:</p> <ul style="list-style-type: none"> 3'b000: maximum current 3'b111: minimum current
1:0	RW	0x0	<p>DRES Delta Resistor Trim Used to trim reference current versus resistor value variation:</p> <ul style="list-style-type: none"> 2'b00: Rnom 2'b01: Rnom - 20% 2'b1x: Rnom + 20%

DDR_PUBL_ACDLLCR

Address: Operational Base + offset (0x0014)

AC DLL Control Register

Bit	Attr	Reset Value	Description
31	RW	0x0	DLLDIS DLL Disable A disabled DLL is bypassed. Default ('0') is DLL enabled
30	RW	0x1	DLLSRST DLL Soft Rest Soft resets the AC DLL by driving the DLL soft reset pin
29:19	RO	0x0	reserved
18	RW	0x0	ATESTEN Analog Test Enable Enables the analog test signal to be output on the DLL analog test output (test_out_a). The DLL analog test output is tri-stated when this bit is '0'.
17:12	RO	0x0	Reserved
11:9	RW	0x0	MFWDLY Master Feed-Forward Delay Trim Used to trim the delay in the master DLL feed-forward path: 3'b000: minimum delay 3'b111: maximum delay
8:6	RW	0x0	MFBDDLY Master Feed-Back Delay Trim Used to trim the delay in the master DLL feedback path: 3'b000: minimum delay 3'b111: maximum delay
5:0	RO	0x0	Reserved

DDR_PUBL_PTR0

Address: Operational Base + offset (0x0018)

PHY Timing Register 0

Bit	Attr	Reset Value	Description
31:22	RO	0x0	reserved
21:18	RW	0x8	tITMSRST ITM Soft Reset Time Number of controller clock cycles that the ITM soft reset pin must remain asserted when the soft reset is applied to the ITMs. This must correspond to a value that is equal to or more than 8 controller clock cycles. Default value corresponds to 8 controller clock cycles.

Bit	Attr	Reset Value	Description
17:6	RW	0xabe	tDLLLOCK DLL Lock Time Number of clock cycles for the DLL to stabilize and lock, i.e. number of clock cycles from when the DLL reset pin is de-asserted to when the DLL has locked and is ready for use. Refer to the PHY databook for the DLL lock time. Default value corresponds to 5.12us at 533MHz.
5:0	RW	0x1b	tDLLSRST DLL Soft Reset Time Number of controller clock cycles that the DLL soft reset pin must remain asserted when the soft reset is triggered through the PHY Initialization Register (PIR). This must correspond to a value that is equal to or more than 50ns or 8 controller clock cycles, whichever is bigger. Default value corresponds to 50ns at 533MHz.

DDR_PUBL_PTR1

Address: Operational Base + offset (0x001c)

PHY Timing Register 1

Bit	Attr	Reset Value	Description
31:27	RO	0x0	reserved
26:19	RW	0xc0	tDINIT1 DRAM Initialization Time 1 DRAM initialization time corresponding to the following: DDR3: CKE high time to first command (tRFC +10 ns or 5 tCK, whichever value is larger) DDR2: CKE high time to first command (400 ns) DDR: CKE high time to first command (400 ns or 1 tCK) LPDDR2: CKE low time with power and clock stable (100 ns) Default value corresponds to DDR3 360ns at 533MHz.

Bit	Attr	Reset Value	Description
18:0	RW	0x4111d	tDINIT0 DRAM Initialization Time 0 DRAM initialization time corresponding to the following: DDR3: CKE low time with power and clock stable (500 us) DDR2: CKE low time with power and clock stable (200 us) DDR: CKE low time with power and clock stable (200 us) LPDDR: CKE high time to first command (200 us) LPDDR2: CKE high time to first command (200 us) Default value corresponds to DDR3 500 us at 533MHz.

DDR_PUBL_PTR2

Address: Operational Base + offset (0x0020)

PHY Timing Register 2

Bit	Attr	Reset Value	Description
31:27	RO	0x0	reserved
26:17	RW	0x216	tDINIT3 DRAM Initialization Time 3 DRAM initialization time corresponding to the following: LPDDR2: Time from ZQ initialization command to first command (1 us) Default value corresponds to the LPDDR2 1 us at 533MHz.
16:0	RW	0x1a072	tDINIT2 DRAM Initialization Time 2 DRAM initialization time corresponding to the following: DDR3: Reset low time (200 us on power-up or 100 ns after power-up) LPDDR2: Time from reset command to end of auto initialization (1 us + 10 us = 11 us) Default value corresponds to DDR3 200 us at 533MHz.

DDR_PUBL_ACIOCR

Address: Operational Base + offset (0x0024)

AC I/O Configuration Register

Bit	Attr	Reset Value	Description
31:30	RW	0x0	ACSR Address/Command Slew Rate (D3F I/O Only) Selects slew rate of the I/O for all address and command pins, as well as the optional DIMM PAR_IN pin and LPDDR TPD pin.
29	RW	0x1	RSTIOM SDRAM Reset I/O Mode Selects SSTL mode (when set to 0) or CMOS mode (when set to 1) of the I/O for SDRAM Reset
28	RW	0x1	RSTPDR SDRAM Reset Power Down Receiver Powers down, when set, the input receiver on the I/O for SDRAM RST# pin
27	RW	0x0	RSTPDD SDRAM Reset Power Down Driver Powers down, when set, the output driver on the I/O for SDRAM RST# pin
26	RW	0x0	RSTODT SDRAM Reset On-Die Termination Enables, when set, the on-die termination on the I/O for SDRAM RST# pin
25:22	RW	0xf	RANKPDR Rank Power Down Receiver Powers down, when set, the input receiver on the I/O CKE[3:0], ODT[3:0], and CS#[3:0] pins. RANKPDR[0] controls the power down for CKE[0], ODT[0], and CS#[0], RANKPDR[1] controls the power down for CKE[1], ODT[1], and CS#[1], and so on.
21:18	RW	0x0	CSPDD CS# Power Down Driver Powers down, when set, the output driver on the I/O for CS#[3:0] pins. PDD[0] controls the power down for CS#[0], PDD[1] controls the power down for CS#[1], and so on. CKE and ODT driver power down is controlled by DSGCR register.
17:14	RW	0x0	RANKODT Rank On-Die Termination Enables, when set, the on-die termination on the I/O for CKE[3:0], ODT[3:0], and CS#[3:0] pins. RANKODT[0] controls the on-die termination for CKE[0], ODT[0], and CS#[0], RANKODT[1] controls the on-die termination for CKE[1], ODT[1], and CS#[1], and so on.

Bit	Attr	Reset Value	Description
13:11	RW	0x7	CKPDR CK Power Down Receiver Powers down, when set, the input receiver on the I/O for CK[0], CK[1], and CK[2] pins, respectively
10:8	RW	0x0	CKPDD CK Power Down Driver Powers down, when set, the output driver on the I/O for CK[0], CK[1], and CK[2] pins, respectively
7:5	RW	0x0	CKODT CK On-Die Termination Enables, when set, the on-die termination on the I/O for CK[0], CK[1], and CK[2] pins, respectively
4	RW	0x1	ACPDR AC Power Down Receiver Powers down, when set, the input receiver on the I/O for RAS#, CAS#, WE#, BA[2:0], and A[15:0] pins, as well as the optional DIMM PAR_IN pin and LPDDR TPD pin.
3	RW	0x0	ACPDD AC Power Down Driver Powers down, when set, the output driver on the I/O for RAS#, CAS#, WE#, BA[2:0], and A[15:0] pins, as well as the optional DIMM PAR_IN pin and LPDDR TPD pin.
2	RW	0x0	ACODT Address/Command On-Die Termination Enables, when set, the on-die termination on the I/O for RAS#, CAS#, WE#, BA[2:0], and A[15:0] pins, as well as the optional DIMM PAR_IN pin and LPDDR TPD pin.
1	RW	0x1	ACOE Address/Command Output Enable Enables, when set, the output driver on the I/O for all address and command pins, as well as the optional DIMM PAR_IN pin and LPDDR TPD pin.
0	RW	0x0	ACIOM Address/Command I/O Mode Selects SSTL mode (when set to 0) or CMOS mode (when set to 1) of the I/O for all address and command pins, as well as the optional DIMM PAR_IN pin and LPDDR TPD pin.

DDR_PUBL_DXCCR

Address: Operational Base + offset (0x0028)

DATX8 Common Configuration Register

Bit	Attr	Reset Value	Description
31:17	RO	0x0	reserved
16	RW	0x0	<p>AWDT Active Window Data Train Indicates if set that data training (DQS gate training and read valid training) should be performed with active DQS gate window. This is just for debug purposes. The default is to perform training with passive windowing.</p>
15	RW	0x0	<p>RVSEL ITMD Read Valid Select Selects the scheme used for ITMD read valid. Valid values are: 1'b0: ITMD read valid signal is generated by delayed DFI read enable signal. 1'b1: ITMD read valid is generated by the ITMD itself using asynchronous crossing.</p>
14	RO	0x0	reserved
13:12	RW	0x0	<p>DXSR Data Slew Rate (D3F I/O Only) Selects slew rate of the I/O for DQ, DM, and DQS/DQS# pins of all DATX8 macros.</p>
11:8	RW	0x8	<p>DQSNRES DQS# Resistor Selects the on-die pull-up/pull-down resistor for DQS# pins. Same encoding as DQSRES. <i>Note: DQS# resistor must be connected for LPDDR2</i></p>
7:4	RW	0x0	<p>DQSRES DQS Resistor Selects the on-die pull-down/pull-up resistor for DQS pins. DQSRES[3] selects pull-down (when set to 0) or pull-up (when set to 1). DQSRES[2:0] selects the resistor value as follows: 3'b000: Open: On-die resistor disconnected 3'b001: 688 ohms 3'b010: 611 ohms 3'b011: 550 ohms 3'b100: 500 ohms 3'b101: 458 ohms 3'b110: 393 ohms 3'b111: 344 ohms <i>Note: DQS resistor must be connected for LPDDR2</i></p>

Bit	Attr	Reset Value	Description
3	RW	0x0	DXPDR Data Power Down Receiver Powers down, when set, the input receiver on I/O for DQ, DM, and DQS/DQS# pins of all DATX8 macros. This bit is ORed with the PDR configuration bit of the individual DATX8.
2	RW	0x0	DXPDD Data Power Down Driver Powers down, when set, the output driver on I/O for DQ, DM, and DQS/DQS# pins of all DATX8 macros. This bit is ORed with the PDD configuration bit of the individual DATX8.
1	RW	0x0	DXIOM Data I/O Mode Selects SSTL mode (when set to 0) or CMOS mode (when set to 1) of the I/O for DQ, DM, and DQS/DQS# pins of all DATX8 macros. This bit is ORed with the IOM configuration bit of the individual DATX8.
0	RW	0x0	DXODT Data On-Die Termination Enables, when set, the on-die termination on the I/O for DQ, DM, and DQS/DQS# pins of all DATX8 macros. This bit is ORed with the ODT configuration bit of the individual DATX8.

DDR_PUBL_DSGCR

Address: Operational Base + offset (0x002c)

DDR System General Configuration Register

Bit	Attr	Reset Value	Description
31	RW	0x1	CKEOE SDRAM CKE Output Enable Enables, when set, the output driver on the I/O for SDRAM CKE pins
30	RW	0x1	RSTOE SDRAM Reset Output Enable Enables, when set, the output driver on the I/O for SDRAM RST# pin
29	RW	0x1	ODTOE SDRAM ODT Output Enable Enables, when set, the output driver on the I/O for SDRAM ODT pins

Bit	Attr	Reset Value	Description
28	RW	0x1	CKOE SDRAM CK Output Enable Enables, when set, the output driver on the I/O for SDRAM CK/CK# pins
27	RW	0x1	TPDOE SDRAM TPD Output Enable (LPDDR Only) Enables, when set, the output driver on the I/O for SDRAM TPD pin
26	RW	0x0	TPDPD DRAM TPD Power Down Driver (LPDDR Only) Powers down, when set, the output driver on the I/O for SDRAM TPD pin. Note that the power down of the receiver on the I/O for SDRAM TPD pin is controlled by ACIOCR[ACPDR] register bit.
25	RW	0x1	NL2OE Non-LPDDR2 Output Enable Enables, when set, the output driver on the I/O for non-LPDDR2 (ODT, RAS#, CAS#, WE#, and BA) pins. This may be used when a chip that is designed for both LPDDR2 and other DDR modes is being used in LPDDR2 mode. For these pins, the I/O output enable signal (OE) is an AND of this bit and the respective output enable bit in ACIOCR or DSGCR registers.
24	RW	0x0	NL2PD Non-LPDDR2 Power Down Powers down, when set, the output driver and the input receiver on the I/O for non-LPDDR2 (ODT, RAS#, CAS#, WE#, and BA) pins. This may be used when a chip that is designed for both LPDDR2 and other DDR modes is being used in LPDDR2 mode. For these pins, the I/O power down signal (PDD or PDR) is an OR of this bit and the respective power-down bit in ACIOCR register.
23:20	RW	0x0	ODTPDD ODT Power Down Driver Powers down, when set, the output driver on the I/O for ODT[3:0] pins. ODTPDD[0] controls the power down for ODT[0], ODTPDD[1] controls the power down for ODT[1], and so on.

Bit	Attr	Reset Value	Description
19:16	RW	0x0	<p>CKEPDD CKE Power Down Driver Powers down, when set, the output driver on the I/O for CKE[3:0] pins. CKEPDD[0] controls the power down for CKE[0], CKEPDD[1] controls the power down for CKE[1], and so on.</p>
15:13	RO	0x0	reserved
12	RW	0x0	<p>FXDLAT Fixed Latency Specified whether all reads should be returned to the controller with a fixed read latency. Enabling fixed read latency increases the read latency. Valid values are: 1'b0: Disable fixed read latency 1'b1: Enable fixed read latency If the design is compiled for HDR mode, then either NOBUB or FXDLAT must be set to 1.</p>
11	RW	0x0	<p>NOBUB No Bubbles Specified whether reads should be returned to the controller with no bubbles. Enabling no-bubble reads increases the read latency. Valid values are: 1'b0: Bubbles are allowed during reads 1'b1: Bubbles are not allowed during reads If the design is compiled for HDR mode, then either NOBUB or FXDLAT must be set to 1.</p>
10:8	RW	0x0	<p>DQSGE DQS Gate Early Specifies the number of clock cycles for which the DQS gating must be enabled earlier than its normal position. Only applicable when using PDQSR I/O cell, passive DQS gating and no drift compensation. This field is recommended to be set to zero for all DDR types other than LPDDR2. For LPDDR2 it should be set to (tDQSCKmax - tDQSC) divide by clock period and rounded up.</p>

Bit	Attr	Reset Value	Description
7:5	RW	0x0	DQSGX DQS Gate Extension Specifies the number of clock cycles for which the DQS gating must be extended beyond the normal burst length width. Only applicable when using PDQSR I/O cell, passive DQS gating and no drift compensation. This field is recommended to be set to zero for all DDR types other than LPDDR2. For LPDDR2 it should be set to (tDQSCKmax - tDQSCK) divide by clock period and rounded up.
4	RW	0x1	LPDLLPD Low Power DLL Power Down Specifies if set that the PHY should respond to the DFI low power opportunity request and power down the DLL of the byte if the wakeup time request satisfies the DLL lock time.
3	RW	0x1	LPIOPD Low Power I/O Power Down Specifies if set that the PHY should respond to the DFI low power opportunity request and power down the I/Os of the byte.
2	RW	0x1	ZUEN Impedance Update Enable Specifies if set that the PHY should perform impedance calibration (update) whenever there is a controller initiated DFI update request. Otherwise the PHY will ignore an update request from the controller.
1	RW	0x1	BDISEN Byte Disable Enable Specifies if set that the PHY should respond to DFI byte disable request. Otherwise the byte disable from the DFI is ignored in which case bytes can only be disabled using the DXnGCR register.
0	RW	0x1	PUREN PHY Update Request Enable Specifies if set, that the PHY should issue PHY-initiated DFI update request when there is DQS drift of more than 3/4 of a clock cycle within one continuous (back-to-back) read burst. By default the PHY issues PHY-initiated update requests and the controller should respond otherwise the PHY may return erroneous values. The option to disable it is provided only for silicon evaluation and testing.

DDR_PUBL_DCR

Address: Operational Base + offset (0x0030)

DRAM Configuration Register

Bit	Attr	Reset Value	Description
31	RW	0x0	TPD Test Power Down (LPDDR Only) If set will place the DRAM in deep power down mode
30:29	RO	0x0	reserved
28	RW	0x0	DDR2T DDR 2T Timing Indicates if set that 2T timing should be used by PUB internally generated SDRAM transactions.
27	RW	0x0	NOSRA No Simultaneous Rank Access Specifies if set that simultaneous rank access on the same clock cycle is not allowed. This means that multiple chip select signals should not be asserted at the same time. This may be required on some DIMM systems.
26:10	RO	0x0	reserved
9:8	RW	0x0	DDRTYPE DDR Type Selects the DDR type for the specified DDR mode. Valid values for LPDDR2 are: 2'b00: LPDDR2-S4 2'b01: LPDDR2-S2 2'b10: LPDDR2-NVM 2'b11: Reserved
7	RW	0x0	MPRDQ Multi-Purpose Register (MPR) DQ (DDR3 Only) Specifies the value that is driven on non-primary DQ pins during MPR reads. Valid values are: 1'b0: Primary DQ drives out the data from MPR (0-1-0-1); non-primary DQs drive '0' 1'b1: Primary DQ and non-primary DQs all drive the same data from MPR (0-1-0-1)
6:4	RW	0x0	PDQ Primary DQ (DDR3 Only) Specifies the DQ pin in a byte that is designated as a primary pin for Multi-Purpose Register (MPR) reads. Valid values are 0 to 7 for DQ[0] to DQ[7], respectively.

Bit	Attr	Reset Value	Description
3	RW	0x1	DDR8BNK DDR 8-Bank Indicates if set that the SDRAM used has 8 banks. tRPA = tRP+1 and tFAW are used for 8-bank DRAMs, other tRPA = tRP and no tFAW is used. Note that a setting of 1 for DRAMs that have fewer than 8 banks still results in correct functionality but less tighter DRAM command spacing for the parameters described here.
2:0	RW	0x3	DDRMD DDR Mode SDRAM DDR mode. Valid values are: 3'b000: LPDDR (Mobile DDR) 3'b001: DDR 3'b010: DDR2 3'b011: DDR3 3'b100: LPDDR2 (Mobile DDR2) 3'b101, 3'b111: Reserved

DDR_PUBL_DTPRO

Address: Operational Base + offset (0x0034)

DRAM Timing Parameters Register 0

Bit	Attr	Reset Value	Description
31	RW	0x0	tCCD Read to read and write to write command delay. Valid values are: 1'b0: BL/2 for DDR2 and 4 for DDR3 1'b1: BL/2 + 1 for DDR2 and 5 for DDR3
30:25	RW	0x18	tRC Activate to activate command delay (same bank). Valid values are 2 to 42.
24:21	RW	0x4	tRRD Activate to activate command delay (different banks). Valid values are 1 to 8.
20:16	RW	0x12	tRAS Activate to precharge command delay. Valid values are 2 to 31.
15:12	RW	0x6	tRCD Activate to read or write delay. Minimum time from when an activate command is issued to when a read or write to the activated row can be issued. Valid values are 2 to 11.

Bit	Attr	Reset Value	Description
11:8	RW	0x6	tRP Precharge command period The minimum time between a precharge command and any other command. Note that the Controller automatically derives tRPA for 8-bank DDR2 devices by adding 1 to tRP . Valid values are 2 to 11.
7:5	RW	0x3	tWTR Internal write to read command delay. Valid values are 1 to 6.
4:2	RW	0x3	tRTP Internal read to precharge command delay. Valid values are 2 to 6. Note that even though RTP does not apply to JEDEC DDR devices, this parameter must still be set to a minimum value of 2 for DDR because the Controller always uses the DDR2 equation, $AL + BL/2 + \max(RTP,2) - 2$, to compute the read to precharge timing (which is $BL/2$ for JEDEC DDR).
1:0	RW	0x2	tMRD Load mode cycle time The minimum time between a load mode register command and any other command. For DDR3 this is the minimum time between two load mode register commands. Valid values for DDR2 are 2 to 3. For DDR3, the value used for tMRD is 4 plus the value programmed in these bits, i.e. tMRD value for DDR3 ranges from 4 to 7.

DDR_PUBL_DTPR1

Address: Operational Base + offset (0x0038)

DRAM Timing Parameters Register 1

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:27	RW	0x1	tDQSCKmax Maximum DQS output access time from CK/CK# (LPDDR2 only). This value is used for implementing read-to-write spacing. Valid values are 1 to 7.

Bit	Attr	Reset Value	Description
26:24	RW	0x1	tDQSCK DQS output access time from CK/CK# (LPDDR2 only). This value is used for computing the read latency. Valid values are 1 to 7.. This value is derived from the corresponding parameter in the SDRAM datasheet divided by the clock cycle time without rounding up. The fractional remainder is automatically adjusted for by data training in quarter clock cycle units. If data training is not performed then this fractional remainder must be converted to quarter clock cycle units and the gating registers (DXnDQSTR) adjusted accordingly.
23:16	RW	0x83	tRFC Refresh-to-Refresh: Indicates the minimum time, in clock cycles, between two refresh commands or between a refresh and an active command. This is derived from the minimum refresh interval from the datasheet, tRFC(min), divided by the clock cycle time. The default number of clock cycles is for the largest JEDEC tRFC(min) parameter value supported.
15:12	RO	0x0	reserved
11	RW	0x0	tRTODT Read to ODT delay (DDR3 only). Specifies whether ODT can be enabled immediately after the read post-amble or one clock delay has to be added. Valid values are: 1'b0: ODT may be turned on immediately after read post-amble 1'b1: ODT may not be turned on until one clock after the read post-amble If tRTODT is set to 1, then the read-to-write latency is increased by 1 if ODT is enabled.
10:9	RW	0x0	tMOD Load mode update delay (DDR3 only). The minimum time between a load mode register command and a non-load mode register command. Valid values are: 2'b00: 12 2'b01: 13 2'b10: 14 2'b11: 15

Bit	Attr	Reset Value	Description
8:3	RW	0x12	tFAW 4-bank activate period. No more than 4-bank activate commands may be issued in a given tFAW period. Only applies to 8-bank devices. Valid values are 2 to 31.
2	RW	0x0	tRTW Read to Write command delay. Valid values are: 1'b0: standard bus turn around delay 1'b1: add 1 clock to standard bus turn around delay This parameter allows the user to increase the delay between issuing Write commands to the SDRAM when preceded by Read commands. This provides an option to increase bus turn-around margin for high frequency systems.
1:0	RW	0x0	tAOND_tAOFD ODT turn-on/turn-off delays (DDR2 only). The delays are in clock cycles. Valid values are: 2'b00: 2/2.5 2'b01: 3/3.5 2'b10: 4/4.5 2'b11: 5/5.5 Most DDR2 devices utilize a fixed value of 2/2.5. For non-standard SDRAMs, the user must ensure that the operational Write Latency is always greater than or equal to the ODT turn-on delay. For example, a DDR2 SDRAM with CAS latency set to 3 and CAS additive latency set to 0 has a Write Latency of 2. Thus 2/2.5 can be used, but not 3/3.5 or higher.

DDR_PUBL_DTPR2

Address: Operational Base + offset (0x003c)

DRAM Timing Parameters Register 2

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:19	RW	0x200	tDLLK DLL locking time. Valid values are 2 to 1023.
18:15	RW	0x3	tCKE CKE minimum pulse width. Also specifies the minimum time that the SDRAM must remain in power down or self refresh mode. For DDR3 this parameter must be set to the value of tCKESR which is usually bigger than the value of tCKE. Valid values are 2 to 15.

Bit	Attr	Reset Value	Description
14:10	RW	0x08	tXP Power down exit delay. The minimum time between a power down exit command and any other command. This parameter must be set to the maximum of the various minimum power down exit delay parameters specified in the SDRAM datasheet, i.e. max(tXP , tXARD, tXARDS) for DDR2 and max(tXP , tXPDLL) for DDR3. Valid values are 2 to 31.
9:0	RW	0x0c8	tXS Self refresh exit delay. The minimum time between a self refresh exit command and any other command. This parameter must be set to the maximum of the various minimum self refresh exit delay parameters specified in the SDRAM datasheet, i.e. max(tXSNR, tXSRD) for DDR2 and max(tXS, tXSDL) for DDR3. Valid values are 2 to 1023.

DDR_PUBL_MR0

Address: Operational Base + offset (0x0040)

Mode Register 0

Bit	Attr	Reset Value	Description
31:13	RO	0x0	reserved
12	RW	0x0	PD Power-Down Control Controls the exit time for power-down modes. Refer to SDRAM datasheet for details on power-down modes. Valid values are: 1'b0: Slow exit (DLL off) 1'b1: Fast exit (DLL on)

Bit	Attr	Reset Value	Description
11:9	RW	0x5	<p>WR Write Recovery This is the value of the write recovery in clock cycles. It is calculated by dividing the datasheet write recovery time, tWR (ns) by the datasheet clock cycle time, tCK (ns) and rounding up a non-integer value to the next integer. Valid values are: 3'b001: 5 3'b010: 6 3'b011: 7 3'b100: 8 3'b101: 10 3'b110: 12 All other settings are reserved and should not be used.</p> <p><i>NOTE: tWR (ns) is the time from the first SDRAM positive clock edge after the last data-in pair of a write command, to when a precharge of the same bank can be issued.</i></p>
8	RW	0x0	<p>DR DLL Reset Writing a '1' to this bit will reset the SDRAM DLL. This bit is self-clearing, i.e. it returns back to '0' after the DLL reset has been issued.</p>
7	RW	0x0	<p>TM Operating Mode Selects either normal operating mode (0) or test mode (1). Test mode is reserved for the manufacturer and should not be used.</p>
6:4	RW	0x5	<p>CL_1 CAS Latency The delay, in clock cycles, between when the SDRAM registers a read command to when data is available. Valid values are: 4'b0010: 5 4'b0100: 6 4'b0110: 7 4'b1000: 8 4'b1010: 9 4'b1100: 10 4'b1110: 11 All other settings are reserved and should not be used.</p>

Bit	Attr	Reset Value	Description
3	RW	0x0	BT Burst Type Indicates whether a burst is sequential (0) or interleaved (1).
2	RW	0x0	CL_0 CAS Latency merged with bit6-4
1:0	RW	0x2	BL Burst Length Determines the maximum number of column locations that can be accessed during a given read or write command. Valid values for DDR3 are: 2'b00: 8 (Fixed) 2'b01: 4 or 8 (On the fly) 2'b10: 4 (Fixed) 2'b11: Reserved

DDR_PUBL_MR1

Address: Operational Base + offset (0x0044)

Mode Register 1

Bit	Attr	Reset Value	Description
31:13	RO	0x0	reserved
12	RW	0x0	QOFF Output Enable/Disable When '0' all outputs function normal; when '1' all SDRAM outputs are disabled removing output buffer current. This feature is intended to be used for IDD characterization of read current and should not be used in normal operation.
11	RW	0x0	TDQS Termination Data Strobe When enabled ('1') TDQS provides additional termination resistance outputs that may be useful in some system configurations. Refer to the SDRAM datasheet for details.
10	RO	0x0	reserved

Bit	Attr	Reset Value	Description
9	RW	0x0	<p>RTT_2 On Die Termination Selects the effective resistance for SDRAM on die termination. Valid values are: 3'b000: ODT disabled 3'b001: RZQ/4 3'b010: RZQ/2 3'b011: RZQ/6 3'b100: RZQ/12 3'b101: RZQ/8 All other settings are reserved and should not be used.</p>
8	RO	0x0	reserved
7	RW	0x0	<p>LEVEL Write Leveling Enable Enables write-leveling when set</p>
6	RW	0x0	<p>RTT_1 On Die Termination merged with bit9.</p>
5	RW	0x0	<p>DIC_1 Output Driver Impedance Control Controls the output drive strength. Valid values are: 2'b00: Reserved for RZQ/6 2'b01: RZQ7 2'b10: Reserved 2'b11: Reserved</p>
4:3	RW	0x0	<p>AL Posted CAS Additive Latency Setting additive latency that allows read and write commands to be issued to the SDRAM earlier than normal (refer to SDRAM datasheet for details). Valid values are: 2'b00: 0 (AL disabled) 2'b01: CL - 1 2'b10: CL - 2 2'b11: Reserved</p>
2	RW	0x0	<p>RTT_0 On Die Termination merged with bit9.</p>
1	RW	0x0	<p>DIC_0 Output Driver Impedance Control Controls the output drive strength. Merged with bit5.</p>

Bit	Attr	Reset Value	Description
0	RW	0x0	DE DLL Enable/Disable Enable (0) or disable (1) the DLL. DLL must be enabled for normal operation.

DDR_PUBL_MR2

Address: Operational Base + offset (0x0048)

Mode Register 2

Bit	Attr	Reset Value	Description
31:11	RO	0x0	reserved
10:9	RW	0x0	RTTWR Dynamic ODT Selects RTT for dynamic ODT. Valid values are: 2'b00: Dynamic ODT off 2'b01: RZQ/4 2'b10: RZQ/2 2'b11: Reserved
8	RO	0x0	reserved
7	RW	0x0	SRT Self-Refresh Temperature Range Selects either normal ('0') or extended ('1') operating temperature range during self-refresh.
6	RW	0x0	ASR Auto Self-Refresh When enabled ('1'), SDRAM automatically provides self-refresh power management functions for all supported operating temperature values. Otherwise the SRT bit must be programmed to indicate the temperature range.
5:3	RW	0x0	CWL CAS Write Latency The delay, in clock cycles, between when the SDRAM registers a write command to when write data is available. Valid values are: 3'b000: 5 (tCK = 2.5ns) 3'b001: 6 (2.5ns > tCK = 1.875ns) 3'b010: 7 (1.875ns > tCK = 1.5ns) 3'b011: 8 (1.5ns > tCK = 1.25ns) All other settings are reserved and should not be used

Bit	Attr	Reset Value	Description
2:0	RW	0x0	<p>PASR Partial Array Self Refresh Specifies that data located in areas of the array beyond the specified location will be lost if self refresh is entered.</p> <p>Valid settings for 4 banks are:</p> <ul style="list-style-type: none"> 3'b000: Full Array 3'b001: Half Array (BA[1:0] = 00 & 01) 3'b010: Quarter Array (BA[1:0] = 00) 3'b011: Not defined 3'b100: 3/4 Array (BA[1:0] = 01, 10, & 11) 3'b101: Half Array (BA[1:0] = 10 & 11) 3'b110: Quarter Array (BA[1:0] = 11) 3'b111: Not defined <p>Valid settings for 8 banks are:</p> <ul style="list-style-type: none"> 3'b000: Full Array 3'b001: Half Array (BA[2:0] = 000, 001, 010 & 011) 3'b010: Quarter Array (BA[2:0] = 000, 001) 3'b011: 1/8 Array (BA[2:0] = 000) 3'b100: 3/4 Array (BA[2:0] = 010, 011, 100, 101, 110 & 111) 3'b101: Half Array (BA[2:0] = 100, 101, 110 & 111) 3'b110: Quarter Array (BA[2:0] = 110 & 111) 3'b111: 1/8 Array (BA[2:0] 111)

DDR_PUBL_MR3

Address: Operational Base + offset (0x004c)

Mode Register 3

Bit	Attr	Reset Value	Description
31:3	RO	0x0	reserved
2	RW	0x0	<p>MPR Multi-Purpose Register Enable Enables, if set, that read data should come from the Multi-Purpose Register. Otherwise read data come from the DRAM array.</p>
1:0	RW	0x0	<p>MPRLOC Multi-Purpose Register (MPR) Location Selects MPR data location: Valid value are: 2'b00: Predefined pattern for system calibration All other settings are reserved and should not be used.</p>

DDR_PUBL_ODTCR

Address: Operational Base + offset (0x0050)

ODT Configuration Register

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23:20	RW	0x2	<p>WRODT1 Write ODT</p> <p>Specifies whether ODT should be enabled ('1') or disabled ('0') on each of the up to four ranks when a write command is sent to rank 0. WRODT0, WRODT1 specify ODT settings when a write is to rank 0, rank 1 respectively. The four bits of each field each represent a rank, the LSB being rank 0 and the MSB being rank 1. Default is to enable ODT only on rank being written to.</p>
19:16	RW	0x1	<p>WRODT0 Write ODT</p> <p>Specifies whether ODT should be enabled ('1') or disabled ('0') on each of the up to four ranks when a write command is sent to rank 0. WRODT0, WRODT1 specify ODT settings when a write is to rank 0, rank 1 respectively. The four bits of each field each represent a rank, the LSB being rank 0 and the MSB being rank 1. Default is to enable ODT only on rank being written to.</p>
15:8	RO	0x0	reserved
7:4	RW	0x0	<p>RDODT1 Read ODT</p> <p>Specifies whether ODT should be enabled ('1') or disabled ('0') on each of the up to four ranks when a read command is sent to rank 1. RDODT0, RDODT1 specify ODT settings when a read is to rank 0, and rank 1, respectively. The two bits of each field each represent a rank, the LSB being rank 0 and the MSB being rank 1. Default is to disable ODT during reads.</p>
3:0	RW	0x0	<p>RDODT0 Read ODT</p> <p>Specifies whether ODT should be enabled ('1') or disabled ('0') on each of the up to four ranks when a read command is sent to rank 0. RDODT0, RDODT1 specify ODT settings when a read is to rank 0, and rank 1, respectively. The two bits of each field each represent a rank, the LSB being rank 0 and the MSB being rank 1. Default is to disable ODT during reads.</p>

DDR_PUBL_DTAR

Address: Operational Base + offset (0x0054)

Data Training Address Register

Bit	Attr	Reset Value	Description
31	RW	0x0	DTMPR Data Training Using MPR (DDR3 Only) Specifies, if set, that data-training should use the SDRAM Multi-Purpose Register (MPR) register. Otherwise data-training is performed by first writing to some locations in the SDRAM and then reading them back.
30:28	RW	0x0	DTBANK Data Training Bank Address Selects the SDRAM bank address to be used during data training
27:12	RW	0x0000	DTROW Data Training Row Address Selects the SDRAM row address to be used during data training
11:0	RW	0x000	DTCOL Data Training Column Address Selects the SDRAM column address to be used during data training. The lower four bits of this address must always be "0000"

DDR_PUBL_DTDRO

Address: Operational Base + offset (0x0058)

Data Training Data Register 0

Bit	Attr	Reset Value	Description
31:24	RW	0xdd	DTBYTE3 Data Training Data The fourth 4 bytes of data used during data training. This same data byte is used for each Byte Lane. Default sequence is a walking 1 while toggling data every data cycle.
23:16	RW	0x22	DTBYTE2 Data Training Data The third 4 bytes of data used during data training. This same data byte is used for each Byte Lane. Default sequence is a walking 1 while toggling data every data cycle.

Bit	Attr	Reset Value	Description
15:8	RW	0xee	DTBYTE1 Data Training Data The second 4 bytes of data used during data training. This same data byte is used for each Byte Lane. Default sequence is a walking 1 while toggling data every data cycle.
7:0	RW	0x11	DTBYTE0 Data Training Data The first 4 bytes of data used during data training. This same data byte is used for each Byte Lane. Default sequence is a walking 1 while toggling data every data cycle.

DDR_PUBL_DTDR1

Address: Operational Base + offset (0x005c)

Data Training Data Register 1

Bit	Attr	Reset Value	Description
31:24	RW	0x77	DTBYTE7 Data Training Data The eighth 4 bytes of data used during data training. This same data byte is used for each Byte Lane. Default sequence is a walking 1 while toggling data every data cycle.
23:16	RW	0x88	DTBYTE6 Data Training Data The seventh 4 bytes of data used during data training. This same data byte is used for each Byte Lane. Default sequence is a walking 1 while toggling data every data cycle.
15:8	RW	0xbb	DTBYTE5 Data Training Data The sixth 4 bytes of data used during data training. This same data byte is used for each Byte Lane. Default sequence is a walking 1 while toggling data every data cycle.
7:0	RW	0x44	DTBYTE4 Data Training Data The fifth 4 bytes of data used during data training. This same data byte is used for each Byte Lane. Default sequence is a walking 1 while toggling data every data cycle.

DDR_PUBL_DCUAR

Address: Operational Base + offset (0x00c0)

DCU Address Register

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11	RW	0x0	<p>ATYPE Access Type Specifies the type of access to be performed using this address. Valid values are: 1'b0: Write access 1'b1: Read access</p>
10	RW	0x0	<p>INCA Increment Address Specifies, if set, that the cache address specified in WADDR and SADDR should be automatically incremented after each access of the cache. The increment happens in such a way that all the slices of a selected word are first accessed before going to the next word.</p>
9:8	RW	0x0	<p>CSEL Cache Select Selects the cache to be accessed. Valid values are: 2'b00: Command cache 2'b01: Expected data cache 2'b10: Read data cache 2'b11: Reserved</p>
7:4	RW	0x0	<p>CSADDR Cache Slice Address Address of the cache slice to be accessed</p>
3:0	RW	0x0	<p>CWADDR Cache Word Address Address of the cache word to be accessed</p>

DDR_PUBL_DCUDR

Address: Operational Base + offset (0x00c4)

DCU Data Register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	<p>CDATA Cache Data Data to be written to or read from a cache. This data corresponds to the cache word slice specified by the DCU Address Register.</p>

DDR_PUBL_DCURR

Address: Operational Base + offset (0x00c8)

DCU Run Register

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23	RW	0x0	XCEN Expected Compare Enable Indicates if set that read data coming back from the SDRAM should be compared with the expected data
22	RW	0x0	RCEN Read Capture Enable Indicates if set that read data coming back from the SDRAM should be captured into the read data cache
21	RW	0x0	SCOF Stop Capture On Full Specifies if set that the capture of read data should stop when the capture cache is full
20	RW	0x0	SONF Stop On Nth Fail Specifies if set that the execution of commands and the capture of read data should stop when there are N read data failures. The number of failures is specified by NFAIL. Otherwise commands execute until the end of the program or until manually stopped using a STOP command.
19:12	RW	0x00	NFAIL Number of Failures Specifies the number of failures after which the execution of commands and the capture of read data should stop if SONF bit of this register is set. Execution of commands and the capture of read data will stop after (NFAIL+1) failures if SONF is set.
11:8	RW	0x0	EADDR End Address Cache word address where the execution of command should end
7:4	RW	0x0	SADDR Start Address Cache word address where the execution of commands should begin

Bit	Attr	Reset Value	Description
3:0	RW	0x0	DINST DCU Instruction Selects the DCU command to be executed: Valid values are: 4'b0000: NOP: No operation 4'b0001: Run: Triggers the execution of commands in the command cache. 4'b0010: Stop: Stops the execution of commands in the command cache. 4'b0011: Stop Loop: Stops the execution of an infinite loop in the command cache. 4'b0100: Reset: Resets all DCU run time registers. 4'b0101 - 4'b1111: Reserved

DDR_PUBL_DCULR

Address: Operational Base + offset (0x00cc)

DCU Loop Register

Bit	Attr	Reset Value	Description
31:28	RW	0x0	XLEADDR Expected Data Loop End Address The last expected data cache word address that contains valid expected data. Expected data should be looped between 0 and this address.
27:18	RO	0x0	reserved
17	RW	0x0	IDA Increment DRAM Address Indicates if set that DRAM addresses should be incremented every time a DRAM read/write command inside the loop is executed
16	RW	0x0	LINF Loop Infinite Indicates if set that the loop should be executed indefinitely until stopped by the STOP command. Otherwise the loop is execute LCNT times.
15:8	RW	0x00	LCNT Loop Count The number of times that the loop should be executed if LINF is not set
7:4	RW	0x0	LEADDR Loop End Address Command cache word address where the loop should end

Bit	Attr	Reset Value	Description
3:0	RW	0x0	LSADDR Loop Start Address Command cache word address where the loop should start

DDR_PUBL_DCUGCR

Address: Operational Base + offset (0x00d0)

DCU General Configuration Register

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:0	RW	0x0000	RCSW Read Capture Start Word The capture and compare of read data should start after Nth word. For example setting this value to 12 will skip the first 12 read data.

DDR_PUBL_DCUTPR

Address: Operational Base + offset (0x00d4)

DCU Timing Parameters Registers

Bit	Attr	Reset Value	Description
31:24	RW	0x00	tDCUT3 DCU Generic Timing Parameter 3.
23:16	RW	0x00	tDCUT2 DCU Generic Timing Parameter 2.
15:8	RW	0x00	tDCUT1 DCU Generic Timing Parameter 1.
7:0	RW	0x00	tDCUT0 DCU Generic Timing Parameter 0.

DDR_PUBL_DCUSR0

Address: Operational Base + offset (0x00d8)

DCU Status Register 0

Bit	Attr	Reset Value	Description
31:3	RO	0x0	reserved
2	RO	0x0	CFULL Capture Full Indicates if set that the capture cache is full

Bit	Attr	Reset Value	Description
1	RO	0x0	CFAIL Capture Fail Indicates if set that at least one read data word has failed
0	RO	0x0	RDONE Run Done: Indicates if set that the DCU has finished executing the commands in the command cache. This bit is also set to indicate that a STOP command has successfully been executed and command execution has stopped.

DDR_PUBL_DCUSR1

Address: Operational Base + offset (0x00dc)

DCU Status Register 1

Bit	Attr	Reset Value	Description
31:24	RO	0x00	LPCNT Loop Count Indicates the value of the loop count. This is useful when the program has stooped because of failures to assess how many reads were executed before first fail.
23:16	RO	0x00	FLCND Fail Count Number of read words that have failed
15:0	RO	0x0000	RDCNT Read Count Number of read words returned from the SDRAM

DDR_PUBL_BISTRR

Address: Operational Base + offset (0x0100)

BIST Run Register

Bit	Attr	Reset Value	Description
31:26	RO	0x0	reserved

Bit	Attr	Reset Value	Description
25:23	RW	0x0	<p>BCKSEL BIST CK Select Selects the CK to be used for capturing loopback data on the address/command lane. Valid values are:</p> <ul style="list-style-type: none"> 3'b000: CK[0] 3'b001: CK[1] 3'b010: CK[2] 3'b011: Reserved 3'b100: CK#[0] 3'b101: CK#[1] 3'b110: CK#[2] 3'b111: Reserved
22:19	RW	0x0	<p>BDXSEL BIST DATX8 Select Select the byte lane for comparison of loopback/read data. Valid values are 0 to 8.</p>
18:17	RW	0x0	<p>BDPAT BIST Data Pattern Selects the data pattern used during BIST. Valid values are:</p> <ul style="list-style-type: none"> 2'b00: Walking 0 2'b01: Walking 1 2'b10: LFSR-based pseudo-random 2'b11: User programmable
16	RW	0x0	<p>BDMEN BIST Data Mask Enable Enables if set that the data mask BIST should be included in the BIST run, i.e. data pattern generated and loopback data compared. This is valid only for loopback mode.</p>
15	RW	0x0	<p>BACEN BIST AC Enable Enables the running of BIST on the address/command lane PHY. This bit is exclusive with BDXEN, i.e. both cannot be set to '1' at the same time.</p>
14	RW	0x0	<p>BDXEN BIST DATX8 Enable Enables the running of BIST on the data byte lane PHYs. This bit is exclusive with BACEN, i.e. both cannot be set to '1' at the same time.</p>

Bit	Attr	Reset Value	Description
13	RW	0x0	BSONF BIST Stop On Nth Fail Specifies if set that the BIST should stop when an nth data word or address/command comparison error has been encountered.
12:5	RW	0x00	NFAIL Number of Failures Specifies the number of failures after which the execution of commands and the capture of read data should stop if BSONF bit of this register is set. Execution of commands and the capture of read data will stop after (NFAIL+1) failures if BSONF is set.
4	RW	0x0	BINF BIST Infinite Run Specifies if set that the BIST should be run indefinitely until when it is either stopped or a failure has been encountered. Otherwise BIST is run until number of BIST words specified in the BISTWCR register has been generated.
3	RW	0x0	BMODE BIST Mode Selects the mode in which BIST is run. Valid values are: 1'b0: Loopback mode: Address, commands and data loop back at the PHY I/Os. 1'b1: DRAM mode: Address, commands and data go to DRAM for normal memory accesses.
2:0	RW	0x0	BINST BIST Instruction Selects the BIST instruction to be executed: Valid values are: 3'b000: NOP: No operation 3'b001: Run: Triggers the running of the BIST. 3'b010: Stop: Stops the running of the BIST. 3'b011: Reset: Resets all BIST run-time registers, such as error counters. 3'b100 - 3'b111: Reserved

DDR_PUBL_BISTMSKRO

Address: Operational Base + offset (0x0104)

BIST Mask Register 0

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:28	RW	0x0	ODTMSK Mask bit for each of the up to 4 ODT bits
27:24	RW	0x0	CSMSK Mask bit for each of the up to 4 CS# bits
23:20	RW	0x0	CKEMSK Mask bit for each of the up to 4 CKE bits
19	RW	0x0	WEMSK Mask bit for the WE#
18:16	RW	0x0	BAMSK Mask bit for each of the up to 3 bank address bits
15:0	RW	0x0000	AMSK Mask bit for each of the up to 16 address bits

DDR_PUBL_BISTMSKR1

Address: Operational Base + offset (0x0108)

BIST Mask Register 1

Bit	Attr	Reset Value	Description
31	RW	0x0	TPDMSK Mask bit for the TPD. LPDDR Only.
30	RW	0x0	PARMSK Mask bit for the PAR_IN. Only for DIMM parity support.
29:20	RO	0x0	reserved
19	RW	0x0	CASMSK Mask bit for the CAS
18	RW	0x0	RASMSK Mask bit for the RAS
17:16	RW	0x0	DMMSK Mask bit for the data mask (DM) bits
15:0	RW	0x0000	DQMSK Mask bit for each of the 8 data (DQ) bits

DDR_PUBL_BISTWCR

Address: Operational Base + offset (0x010c)

BIST Word Count Register

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved

Bit	Attr	Reset Value	Description
15:0	RW	0x0020	BWCNT BIST Word Count Indicates the number of words to generate during BIST. This must be a multiple of DRAM burst length (BL) divided by 2, e.g. for BL=8, valid values are 4, 8, 12, 16, and so on.

DDR_PUBL_BISTLSR

Address: Operational Base + offset (0x0110)

BIST LFSR Seed Register

Bit	Attr	Reset Value	Description
31:0	RW	0x1234abcd	SEED LFSR seed for pseudo-random BIST patterns.

DDR_PUBL_BISTAR0

Address: Operational Base + offset (0x0114)

BIST Address Register 0

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:28	RW	0x0	BBANK BIST Bank Address Selects the SDRAM bank address to be used during BIST
27:12	RW	0x0000	BROW BIST Row Address Selects the SDRAM row address to be used during BIST
11:0	RW	0x000	BCOL BIST Column Address Selects the SDRAM column address to be used during BIST. The lower bits of this address must be "0000" for BL16, "000" for BL8, "00" for BL4 and "0" for BL2.

DDR_PUBL_BISTAR1

Address: Operational Base + offset (0x0118)

BIST Address Register 1

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved

Bit	Attr	Reset Value	Description
15:4	RW	0x000	BAINC BIST Address Increment Selects the value by which the SDRAM address is incremented for each write/read access. This value must be at the beginning of a burst boundary, i.e. the lower bits must be "0000" for BL16, "00" for BL8, "00" for BL4 and "0" for BL2.
3:2	RW	0x3	BMRANK BIST Maximum Rank Specifies the maximum SDRAM rank to be used during BIST. The default value is set to maximum ranks minus 1. Example default shown here is for a 4-rank system
1:0	RW	0x0	BRANK BIST Rank Selects the SDRAM rank to be used during BIST. Valid values range from 0 to maximum ranks minus 1.

DDR_PUBL_BISTAR2

Address: Operational Base + offset (0x011c)

BIST Address Register 2

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:28	RW	0x7	BMBANK BIST Maximum Bank Address Specifies the maximum SDRAM bank address to be used during BIST before the address increments to the next rank.
27:12	RW	0xffff	BMROW BIST Maximum Row Address Specifies the maximum SDRAM row address to be used during BIST before the address increments to the next bank.
11:0	RW	0xffff	BMCOL BIST Maximum Column Address Specifies the maximum SDRAM column address to be used during BIST before the address increments to the next row.

DDR_PUBL_BISTUDPR

Address: Operational Base + offset (0x0120)

BIST User Data Pattern Register

Bit	Attr	Reset Value	Description
31:16	RW	0xffff	BUDP1 BIST User Data Pattern 1 Data to be applied on odd DQ pins during BIST
15:0	RW	0x0000	BUDP0 BIST User Data Pattern 0 Data to be applied on even DQ pins during BIST

DDR_PUBL_BISTGSR

Address: Operational Base + offset (0x0124)

BIST General Status Register

Bit	Attr	Reset Value	Description
31:30	RO	0x0	CASBER CAS Bit Error Indicates the number of bit errors on CAS
29:28	RO	0x0	RASBER RAS Bit Error Indicates the number of bit errors on RAS
27:24	RO	0x0	DMBER DM Bit Error Indicates the number of bit errors on data mask (DM) bit. DMBER[1:0] are for the first DM beat, and DMBER[3:2] are for the second DM beat.
23:22	RO	0x0	TPDBER TPD Bit Error (LPDDR Only) Indicates the number of bit errors on TPD
21:20	RO	0x0	PARBER PAR_IN Bit Error (DIMM Only) Indicates the number of bit errors on PAR_IN
19:3	RO	0x0	reserved
2	RO	0x0	BDXERR BIST Data Error Indicates if set that there is a data comparison error in the byte lane
1	RO	0x0	BACERR BIST Address/Command Error Indicates if set that there is a data comparison error in the address/command lane
0	RO	0x0	BDONE BIST Done Indicates if set that the BIST has finished executing. This bit is reset to zero when BIST is triggered.

DDR_PUBL_BISTWER

Address: Operational Base + offset (0x0128)

BIST Word Error Register

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	DXWER Byte Word Error Indicates the number of word errors on the byte lane. An error on any bit of the data bus including the data mask bit increments the error count.
15:0	RO	0x0000	ACWER Address/Command Word Error Indicates the number of word errors on the address/command lane. An error on any bit of the address/command bus increments the error count.

DDR_PUBL_BISTBER0

Address: Operational Base + offset (0x012c)

BIST Bit Error Register 0

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ABER Address Bit Error Each group of two bits indicate the bit error count on each of the up to 16 address bits. [1:0] is the error count for A[0], [3:2] for A[1], and so on.

DDR_PUBL_BISTBER1

Address: Operational Base + offset (0x0130)

BIST Bit Error Register 1

Bit	Attr	Reset Value	Description
31:24	RO	0x00	ODTBER ODT Bit Error Each group of two bits indicates the bit error count on each of the up to 4 ODT bits. [1:0] is the error count for ODT[0], [3:2] for ODT[1], and so on.
23:16	RO	0x00	CSBER CS# Bit Error Each group of two bits indicates the bit error count on each of the up to 4 CS# bits. [1:0] is the error count for CS#[0], [3:2] for CS#[1], and so on.

Bit	Attr	Reset Value	Description
15:8	RO	0x00	CKEBER CKE Bit Error Each group of two bits indicates the bit error count on each of the up to 4 CKE bits. [1:0] is the error count for CKE[0], [3:2] for CKE[1], and so on.
7:6	RO	0x0	WEBER WE# Bit Error Indicates the number of bit errors on WE#
5:0	RO	0x00	BABER Bank Address Bit Error Each group of two bits indicates the bit error count on each of the up to 3 bank address bits. [1:0] is the error count for BA[0], [3:2] for BA[1], and so on.

DDR_PUBL_BISTBER2

Address: Operational Base + offset (0x0134)

BIST Bit Error Register 2

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	DQBER Data Bit Error The first 16 bits indicate the error count for the first data beat (i.e. the data driven out on DQ[7:0] on the rising edge of DQS). The second 16 bits indicate the error on the second data beat (i.e. the error count of the data driven out on DQ[7:0] on the falling edge of DQS). For each of the 16-bit group, the first 2 bits are for DQ[0], the second for DQ[1], and so on.

DDR_PUBL_BISTWCSR

Address: Operational Base + offset (0x0138)

BIST Word Count Status Register

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	DXWCNT Byte Word Count Indicates the number of words received from the byte lane
15:0	RO	0x0000	ACWCNT Address/Command Word Count Indicates the number of words received from the address/command lane

DDR_PUBL_BISTFWR0

Address: Operational Base + offset (0x013c)

BIST Fail Word Register 0

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28	RO	0x0	ODTWEBS Bit status during a word error for each of the up to 4 ODT bits
27:24	RO	0x0	CSWEBS Bit status during a word error for each of the up to 4 CS# bits
23:20	RO	0x0	CKEWEBS Bit status during a word error for each of the up to 4 CKE bits
19	RO	0x0	WEWEBS Bit status during a word error for the WE#
18:16	RO	0x0	BAWEBS Bit status during a word error for each of the up to 3 bank address bits
15:0	RO	0x0000	AWEBS Bit status during a word error for each of the up to 16 address bits

DDR_PUBL_BISTFWR1

Address: Operational Base + offset (0x0140)

BIST Fail Word Register 1

Bit	Attr	Reset Value	Description
31	RO	0x0	TPDWEBS Bit status during a word error for the TPD. LPDDR Only.
30	RO	0x0	PARWEBS Bit status during a word error for the PAR_IN. Only for DIMM parity support.
29:20	RO	0x0	reserved
19	RO	0x0	CASWEBS Bit status during a word error for the CAS
18	RO	0x0	RASWEBS Bit status during a word error for the RAS
17:16	RO	0x0	DMWEBS Bit status during a word error for the data mask (DM) bit. DMWEBS [0] is for the first DM beat, and DMWEBS [1] is for the second DM beat.

Bit	Attr	Reset Value	Description
15:0	RO	0x0000	DQWEBS Bit status during a word error for each of the 8 data (DQ) bits. The first 8 bits indicate the status of the first data beat (i.e. the status of the data driven out on DQ[7:0] on the rising edge of DQS). The second 8 bits indicate the status of the second data beat (i.e. the status of the data driven out on DQ[7:0] on the falling edge of DQS). For each of the 8-bit group, the first bit is for DQ[0], the second bit is for DQ[1], and so on.

DDR_PUBL_ZQ0CRO

Address: Operational Base + offset (0x0180)

ZQ 0 Impedance Control Register 0

Bit	Attr	Reset Value	Description
31	RW	0x0	ZQPD ZQ Power Down Powers down, if set, the PZQ cell.
30	RW	0x0	ZCAL Impedance Calibration Trigger A write of '1' to this bit triggers impedance calibration to be performed by the impedance control logic. The impedance calibration trigger bit is self-clearing and returns back to '0' when the calibration is complete.
29	RW	0x0	ZCALBYP Impedance Calibration Bypass Disables, if set, impedance calibration of this ZQ control block when impedance calibration is triggered globally using the ZCAL bit of PIR. Impedance calibration of this ZQ block may be triggered manually using ZCAL.
28	RW	0x0	ZDEN Impedance Over-ride Enable When this bit is set, it allows users to directly drive the impedance control using the data programmed in the ZQDATA field. Otherwise, the control is generated automatically by the impedance control logic.

Bit	Attr	Reset Value	Description
27:0	RW	0x000014a	ZDATA Impedance Over-Ride Data Data used to directly drive the impedance control. ZDATA field mapping for D3R I/Os is as follows: ZDATA[27:20] is reserved and returns zeros on reads ZDATA[19:15] is used to select the pull-up on-die termination impedance ZDATA[14:10] is used to select the pull-down on-die termination impedance ZDATA[9:5] is used to select the pull-up output impedance ZDATA[4:0] is used to select the pull-down output impedance

DDR_PUBL_ZQ0CR1

Address: Operational Base + offset (0x0184)

ZQ 0 Impedance Control Register 1

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RW	0x7b	ZPROG Impedance Divide Ratio Selects the external resistor divide ratio to be used to set the output impedance and the on-die termination as follows: ZPROG[7:4]: On-die termination divide select ZPROG[3:0]: Output impedance divide select

DDR_PUBL_ZQ0SR0

Address: Operational Base + offset (0x0188)

ZQ 0 Impedance Status Register 0

Bit	Attr	Reset Value	Description
31	RO	0x0	ZDONE Impedance Calibration Done Indicates that impedance calibration has completed
30	RO	0x0	ZERR Impedance Calibration Error If set, indicates that there was an error during impedance calibration
29:28	RO	0x0	reserved

Bit	Attr	Reset Value	Description
27:0	RO	0x00000000	ZCTRL Impedance Control Current value of impedance control. ZCTRL field mapping for D3R I/Os is as follows: ZCTRL[27:20] is reserved and returns zeros on reads ZCTRL[19:15] is used to select the pull-up on-die termination impedance ZCTRL[14:10] is used to select the pull-down on-die termination impedance ZCTRL[9:5] is used to select the pull-up output impedance ZCTRL[4:0] is used to select the pull-down output impedance

DDR_PUBL_ZQ0SR1

Address: Operational Base + offset (0x018c)

ZQ 0 Impedance Status Register 1

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:6	RO	0x0	OPU On-die termination (ODT) pull-up calibration status. Similar status encodings as ZPD.
5:4	RO	0x0	OPD On-die termination (ODT) pull-down calibration status. Similar status encodings as ZPD.
3:2	RO	0x0	ZPU Output impedance pull-up calibration status. Similar status encodings as ZPD.
1:0	RO	0x0	ZPD Output impedance pull-down calibration status. Valid status encodings are: 2'b00: Completed with no errors 2'b01: Overflow error 2'b10: Underflow error 2'b11: Calibration in progress

DDR_PUBL_ZQ1CR0

Address: Operational Base + offset (0x0190)

ZQ 1 Impedance Control Register 0

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31	RW	0x0	ZQPD ZQ Power Down Powers down, if set, the PZQ cell.
30	RW	0x0	ZCAL Impedance Calibration Trigger A write of '1' to this bit triggers impedance calibration to be performed by the impedance control logic. The impedance calibration trigger bit is self-clearing and returns back to '0' when the calibration is complete.
29	RW	0x0	ZCALBYP Impedance Calibration Bypass Disables, if set, impedance calibration of this ZQ control block when impedance calibration is triggered globally using the ZCAL bit of PIR. Impedance calibration of this ZQ block may be triggered manually using ZCAL.
28	RW	0x0	ZDEN Impedance Over-ride Enable When this bit is set, it allows users to directly drive the impedance control using the data programmed in the ZQDATA field. Otherwise, the control is generated automatically by the impedance control logic.
27:0	RW	0x000014a	ZDATA Impedance Over-Ride Data Data used to directly drive the impedance control. ZDATA field mapping for D3R I/Os is as follows: ZDATA[27:20] is reserved and returns zeros on reads ZDATA[19:15] is used to select the pull-up on-die termination impedance ZDATA[14:10] is used to select the pull-down on-die termination impedance ZDATA[9:5] is used to select the pull-up output impedance ZDATA[4:0] is used to select the pull-down output impedance

DDR_PUBL_ZQ1CR1

Address: Operational Base + offset (0x0194)

ZQ 1 Impedance Control Register 1

Bit	Attr	Reset Value	Description
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Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RW	0x7b	ZPROG Impedance Divide Ratio Selects the external resistor divide ratio to be used to set the output impedance and the on-die termination as follows: ZPROG[7:4]: On-die termination divide select ZPROG[3:0]: Output impedance divide select

DDR_PUBL_ZQ1SR0

Address: Operational Base + offset (0x0198)

ZQ 1 Impedance Status Register 0

Bit	Attr	Reset Value	Description
31	RO	0x0	ZDONE Impedance Calibration Done Indicates that impedance calibration has completed
30	RO	0x0	ZERR Impedance Calibration Error If set, indicates that there was an error during impedance calibration
29:28	RO	0x0	reserved
27:0	RO	0x00000000	ZCTRL Impedance Control Current value of impedance control. ZCTRL field mapping for D3R I/Os is as follows: ZCTRL[27:20] is reserved and returns zeros on reads ZCTRL[19:15] is used to select the pull-up on-die termination impedance ZCTRL[14:10] is used to select the pull-down on-die termination impedance ZCTRL[9:5] is used to select the pull-up output impedance ZCTRL[4:0] is used to select the pull-down output impedance

DDR_PUBL_ZQ1SR1

Address: Operational Base + offset (0x019c)

ZQ 1 Impedance Status Register 1

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved

Bit	Attr	Reset Value	Description
7:6	RO	0x0	OPU On-die termination (ODT) pull-up calibration status. Similar status encodings as ZPD.
5:4	RO	0x0	OPD On-die termination (ODT) pull-down calibration status. Similar status encodings as ZPD.
3:2	RO	0x0	ZPU Output impedance pull-up calibration status. Similar status encodings as ZPD.
1:0	RO	0x0	ZPD Output impedance pull-down calibration status. Valid status encodings are: 2'b00: Completed with no errors 2'b01: Overflow error 2'b10: Underflow error 2'b11: Calibration in progress

DDR_PUBL_ZQ2CR0

Address: Operational Base + offset (0x01a0)

ZQ 2 Impedance Control Register 0

Bit	Attr	Reset Value	Description
31	RW	0x0	ZQPD ZQ Power Down Powers down, if set, the PZQ cell.
30	RW	0x0	ZCAL Impedance Calibration Trigger A write of '1' to this bit triggers impedance calibration to be performed by the impedance control logic. The impedance calibration trigger bit is self-clearing and returns back to '0' when the calibration is complete.
29	RW	0x0	ZCALBYP Impedance Calibration Bypass Disables, if set, impedance calibration of this ZQ control block when impedance calibration is triggered globally using the ZCAL bit of PIR. Impedance calibration of this ZQ block may be triggered manually using ZCAL.

Bit	Attr	Reset Value	Description
28	RW	0x0	ZDEN Impedance Over-ride Enable When this bit is set, it allows users to directly drive the impedance control using the data programmed in the ZQDATA field. Otherwise, the control is generated automatically by the impedance control logic.
27:0	RW	0x000014a	ZDATA Impedance Over-Ride Data Data used to directly drive the impedance control. ZDATA field mapping for D3R I/Os is as follows: ZDATA[27:20] is reserved and returns zeros on reads ZDATA[19:15] is used to select the pull-up on-die termination impedance ZDATA[14:10] is used to select the pull-down on-die termination impedance ZDATA[9:5] is used to select the pull-up output impedance ZDATA[4:0] is used to select the pull-down output impedance

DDR_PUBL_ZQ2CR1

Address: Operational Base + offset (0x01a4)

ZQ 2 Impedance Control Register 1

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RW	0x7b	ZPROG Impedance Divide Ratio Selects the external resistor divide ratio to be used to set the output impedance and the on-die termination as follows: ZPROG[7:4]: On-die termination divide select ZPROG[3:0]: Output impedance divide select

DDR_PUBL_ZQ2SR0

Address: Operational Base + offset (0x01a8)

ZQ 2 Impedance Status Register 0

Bit	Attr	Reset Value	Description
31	RO	0x0	ZDONE Impedance Calibration Done Indicates that impedance calibration has completed

Bit	Attr	Reset Value	Description
30	RO	0x0	ZERR Impedance Calibration Error If set, indicates that there was an error during impedance calibration
29:28	RO	0x0	reserved
27:0	RO	0x00000000	ZCTRL Impedance Control Current value of impedance control. ZCTRL field mapping for D3R I/Os is as follows: ZCTRL[27:20] is reserved and returns zeros on reads ZCTRL[19:15] is used to select the pull-up on-die termination impedance ZCTRL[14:10] is used to select the pull-down on-die termination impedance ZCTRL[9:5] is used to select the pull-up output impedance ZCTRL[4:0] is used to select the pull-down output impedance

DDR_PUBL_ZQ2SR1

Address: Operational Base + offset (0x01ac)

ZQ 2 Impedance Status Register 1

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:6	RO	0x0	OPU On-die termination (ODT) pull-up calibration status. Similar status encodings as ZPD.
5:4	RO	0x0	OPD On-die termination (ODT) pull-down calibration status. Similar status encodings as ZPD.
3:2	RO	0x0	ZPU Output impedance pull-up calibration status. Similar status encodings as ZPD.
1:0	RO	0x0	ZPD Output impedance pull-down calibration status. Valid status encodings are: 2'b00: Completed with no errors 2'b01: Overflow error 2'b10: Underflow error 2'b11: Calibration in progress

DDR_PUBL_ZQ3CR0

Address: Operational Base + offset (0x01b0)

ZQ 3 Impedance Control Register 0

Bit	Attr	Reset Value	Description
31	RW	0x0	ZQPD ZQ Power Down Powers down, if set, the PZQ cell.
30	RW	0x0	ZCAL Impedance Calibration Trigger A write of '1' to this bit triggers impedance calibration to be performed by the impedance control logic. The impedance calibration trigger bit is self-clearing and returns back to '0' when the calibration is complete.
29	RW	0x0	ZCALBYP Impedance Calibration Bypass Disables, if set, impedance calibration of this ZQ control block when impedance calibration is triggered globally using the ZCAL bit of PIR. Impedance calibration of this ZQ block may be triggered manually using ZCAL.
28	RW	0x0	ZDEN Impedance Over-ride Enable When this bit is set, it allows users to directly drive the impedance control using the data programmed in the ZQDATA field. Otherwise, the control is generated automatically by the impedance control logic
27:0	RW	0x000014a	ZDATA Impedance Over-Ride Data Data used to directly drive the impedance control. ZDATA field mapping for D3R I/Os is as follows: ZDATA[27:20] is reserved and returns zeros on reads ZDATA[19:15] is used to select the pull-up on-die termination impedance ZDATA[14:10] is used to select the pull-down on-die termination impedance ZDATA[9:5] is used to select the pull-up output impedance ZDATA[4:0] is used to select the pull-down output impedance

DDR_PUBL_ZQ3CR1

Address: Operational Base + offset (0x01b4)

ZQ 3 Impedance Control Register 1

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RW	0x7b	ZPROG Impedance Divide Ratio Selects the external resistor divide ratio to be used to set the output impedance and the on-die termination as follows: ZPROG[7:4]: On-die termination divide select ZPROG[3:0]: Output impedance divide select

DDR_PUBL_ZQ3SR0

Address: Operational Base + offset (0x01b8)

ZQ 3 Impedance Status Register 0

Bit	Attr	Reset Value	Description
31	RO	0x0	ZDONE Impedance Calibration Done Indicates that impedance calibration has completed
30	RO	0x0	ZERR Impedance Calibration Error If set, indicates that there was an error during impedance calibration
29:28	RO	0x0	reserved
27:0	RO	0x00000000	ZCTRL Impedance Control Current value of impedance control. ZCTRL field mapping for D3R I/Os is as follows: ZCTRL[27:20] is reserved and returns zeros on reads ZCTRL[19:15] is used to select the pull-up on-die termination impedance ZCTRL[14:10] is used to select the pull-down on-die termination impedance ZCTRL[9:5] is used to select the pull-up output impedance ZCTRL[4:0] is used to select the pull-down output impedance

DDR_PUBL_ZQ3SR1

Address: Operational Base + offset (0x01bc)

ZQ 3 Impedance Status Register 1

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved

Bit	Attr	Reset Value	Description
7:6	RO	0x0	OPU On-die termination (ODT) pull-up calibration status. Similar status encodings as ZPD.
5:4	RO	0x0	OPD On-die termination (ODT) pull-down calibration status. Similar status encodings as ZPD.
3:2	RO	0x0	ZPU Output impedance pull-up calibration status. Similar status encodings as ZPD.
1:0	RO	0x0	ZPD Output impedance pull-down calibration status. Valid status encodings are: 2'b00: Completed with no errors 2'b01: Overflow error 2'b10: Underflow error 2'b11: Calibration in progress

DDR_PUBL_DX0GCR

Address: Operational Base + offset (0x01c0)

DATX8 0 General Configuration Register

Bit	Attr	Reset Value	Description
31:20	RO	0x0	reserved

Bit	Attr	Reset Value	Description
16:14 19:17	RW	0x3 0x3	<p>R0RVSL R1RVSL Rank n ITMD Read Valid System Latency Used to specify the read valid system latency relative to the ideal placement of the ITMD read valid signal when DXCCR.RVSEL is set to 0. Power-up default is 011 (i.e. ideal placement of the the read valid signal). The RVSL fields are initially set by the PUB during automatic read valid training but these values can be overwritten by a direct write to this register. Every three bits of this register control the latency of each rank. R0RVSL controls the latency of rank 0, R1RVSL controls rank 1. Valid values are:</p> <ul style="list-style-type: none"> 3'b000: read valid system latency = ideal placement - 3 3'b001: read valid system latency = ideal placement - 2 3'b010: read valid system latency = ideal placement - 1 3'b011: read valid system latency = ideal placement 3'b100: read valid system latency = ideal placement + 1 3'b101: read valid system latency = ideal placement + 2 3'b110: read valid system latency = ideal placement + 3 3'b111: Reserved
13	RW	0x0	<p>RTTOAL RTT On Additive Latency Indicates when the ODT control of DQ/DQS SSTL I/Os is set to the value in DQODT/DQSODT during read cycles. Valid values are:</p> <ul style="list-style-type: none"> 1'b0: ODT control is set to DQSODT/DQODT almost two cycles before read data preamble 1'b1: ODT control is set to DQSODT/DQODT almost one cycle before read data preamble
12:11	RW	0x0	<p>RTTOH RTT Output Hold Indicates the number of clock cycles (from 0 to 3) after the read data postamble for which ODT control should remain set to DQSODT for DQS or DQODT for DQ/DM before disabling it (setting it to '0' when using dynamic ODT control. ODT is disabled almost RTTOH clock cycles after the read postamble.</p>

Bit	Attr	Reset Value	Description
10	RW	0x1	DQRTT DQ Dynamic RTT Control Indicates, if set, that the ODT control of DQ/DM SSTL I/Os be dynamically controlled by setting it to the value in DQODT during reads and disabling it (setting it to '0' during any other cycle. If this bit is not set, then the ODT control of DQ SSTL I/Os is always set to the value in DQODT.
9	RW	0x1	DQSRTT DQS Dynamic RTT Control Indicates, if set, that the ODT control of DQS SSTL I/Os be dynamically controlled by setting it to the value in DQSODT during reads and disabling it (setting it to '0' during any other cycle. If this bit is not set, then the ODT control of DQS SSTL I/Os is always set to the value in DQSODT field.
8:7	RW	0x1	DSEN Write DQS Enable Controls whether the write DQS going to the SDRAM is enabled (toggling) or disabled (static value) and whether the DQS is inverted. DQS# is always the inversion of DQS. These values are valid only when DQS/DQS# output enable is on, otherwise the DQS/DQS# is tristated. Valid settings are: 2'b00: DQS disabled (Driven to constant 0) 2'b01: DQS toggling with inverted polarity 2'b10: DQS toggling with normal polarity (This should be the default setting) 2'b11: DQS disabled (Driven to constant 1)
6	RW	0x0	DQSRPD DQSR Power Down Powers down, if set, the PDQSR cell. This bit is ORed with the common PDR configuration bit.
5	RW	0x0	DXPDR Data Power Down Receiver Powers down, when set, the input receiver on I/O for DQ, DM, and DQS/DQS# pins of the byte. This bit is ORed with the common PDR configuration bit.
4	RW	0x0	DXPDD Data Power Down Driver Powers down, when set, the output driver on I/O for DQ, DM, and DQS/DQS# pins of the byte. This bit is ORed with the common PDD configuration bit.

Bit	Attr	Reset Value	Description
3	RW	0x0	DXIOM Data I/O Mode Selects SSTL mode (when set to 0) or CMOS mode (when set to 1) of the I/O for DQ, DM, and DQS/DQS# pins of the byte. This bit is ORed with the IOM configuration bit of the individual DATX8.
2	RW	0x0	DQODT Data On-Die Termination Enables, when set, the on-die termination on the I/O for DQ and DM pins of the byte. This bit is ORed with the common DATX8 ODT configuration bit.
1	RW	0x0	DQSODT DQS On-Die Termination Enables, when set, the on-die termination on the I/O for DQS/DQS# pin of the byte. This bit is ORed with the common DATX8 ODT configuration bit.
0	RW	0x1	DXEN Data Byte Enable Enables if set the DATX8 and SSTL I/Os used on the data byte. Setting this bit to '0' disables the byte, i.e. the byte SSTL I/Os are put in power-down mode and the DLL in the DATX8 is put in bypass mode.

DDR_PUBL_DX0GSR0

Address: Operational Base + offset (0x01c4)

DATX8 0 General Status Register 0

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24:13	RO	0x000	DTPASS DQS Gate Training Pass Count The number of passing configurations during DQS gate training. Bits [2:0] are for rank 0, bits [5:3] for rank 1, and so on.
12	RO	0x0	reserved
11:8	RO	0x0	DTIERR DQS Gate Training Intermittent Error If set, indicates that there was an intermittent error during DQS gate training of the byte, such as a pass was followed by a fail then followed by another pass. Bit [0] is for rank 0, bit 1 for rank 1, and so on.

Bit	Attr	Reset Value	Description
7:4	RO	0x0	DTERR DQS Gate Training Error If set, indicates that a valid DQS gating window could not be found during DQS gate training of the byte. Bit [0] is for rank 0, bit 1 for rank 1, and so on.
3:0	RO	0x0	DTDONE Data Training Done Indicates, if set, that the byte has finished doing data training. Bit [0] is for rank 0, bit 1 for rank 1, and so on.

DDR_PUBL_DX0GSR1

Address: Operational Base + offset (0x01c8)

DATX8 0 General Status Register 1

Bit	Attr	Reset Value	Description
31:20	RO	0x0	RVPASS Read Valid Training Pass Count The number of passing configurations during read valid training. Bits [2:0] are for rank 0, bits [5:3] for rank 1, and so on.
19:16	RO	0x0	RVIERR Read Valid Training Intermittent Error If set, indicates that there was an intermittent error during read valid training of the byte, such as a pass was followed by a fail then followed by another pass. Bit [0] is for rank 0, bit 1 for rank 1, and so on.
15:12	RO	0x0	RVERR Read Valid Training Error If set, indicates that a valid read valid placement could not be found during read valid training of the byte. Bit [0] is for rank 0, bit 1 for rank 1, and so on.
11:4	RO	0x00	DQSDFT DQS Drift Used to report the drift on the read data strobe of the data byte. Valid settings are: 2'b00: No drift 2'b01: 90 deg drift 2'b10: 180 deg drift 2'b11: 270 deg drift or more Bits [1:0] are for rank 0, bits [3:2] for rank 1, and so on.

Bit	Attr	Reset Value	Description
3:0	RO	0x0	DFTERR DQS Drift Error If set, indicates that the byte read data strobe has drifted by more than or equal to the drift limit set in the PHY General Configuration Register (PGCR). Bit [0] is for rank 0, bit 1 for rank 1, and so on.

DDR_PUBL_DX0DLLCR

Address: Operational Base + offset (0x01cc)

DATX8 0 DLL Control Register

Bit	Attr	Reset Value	Description
31	RW	0x0	DLLDIS DLL Disable A disabled DLL is bypassed. Default ('0') is DLL enabled
30	RW	0x1	DLLSRST DLL Soft Rest Soft resets the byte DLL by driving the DLL soft reset pin
29:20	RO	0x0	reserved
19	RW	0x0	SDLBMODE Slave DLL Loopback Mode If this bit is set, the slave DLL is put in loopback mode in which there is no 90 degrees phase shift on read DQS/DQS#. This bit must be set when operating the byte PHYs in loopback mode such as during BIST loopback. Applicable only to PHYs that have this feature. Refer to PHY databook.
18	RW	0x0	ATESTEN Analog Test Enable Enables the analog test signal to be output on the DLL analog test output (test_out_a). The DLL analog test output is tri-stated when this bit is '0'.

Bit	Attr	Reset Value	Description
17:14	RW	0x0	<p>SDPHASE Slave DLL Phase Trim Selects the phase difference between the input clock and the corresponding output clock of the slave DLL. Valid settings:</p> <ul style="list-style-type: none"> 4'b0000: 90 4'b0001: 72 4'b0010: 54 4'b0011: 36 4'b0100: 108 4'b0101: 90 4'b0110: 72 4'b0111: 54 4'b1000: 126 4'b1001: 108 4'b1010: 90 4'b1011: 72 4'b1100: 144 4'b1101: 126 4'b1110: 108 4'b1111: 90
13:12	RW	0x0	<p>SSTART Slave Auto Start-Up Used to control how the slave DLL starts up relative to the master DLL locking:</p> <ul style="list-style-type: none"> 2'b0X: Slave DLL automatically starts up once the master DLL has achieved lock 2'b10: The automatic startup of the slave DLL is disabled; the phase detector is disabled 2'b11: The automatic startup of the slave DLL is disabled; the phase detector is enabled
11:9	RW	0x0	<p>MFWDLY Master Feed-Forward Delay Trim Used to trim the delay in the master DLL feed-forward path:</p> <ul style="list-style-type: none"> 3'b000: minimum delay 3'b111: maximum delay
8:6	RW	0x0	<p>MFBDLY Master Feed-Back Delay Trim Used to trim the delay in the master DLL feedback path:</p> <ul style="list-style-type: none"> 3'b000: minimum delay 3'b111: maximum delay

Bit	Attr	Reset Value	Description
5:3	RW	0x0	SFWDLY Slave Feed-Forward Delay Trim Used to trim the delay in the slave DLL feed-forward path: 3'b000: minimum delay 3'b111: maximum delay
2:0	RW	0x0	SFBDLY Slave Feed-Back Delay Trim Used to trim the delay in the slave DLL feedback path: 3'b000: minimum delay 3'b111: maximum delay

DDR_PUBL_DX0DQTR

Address: Operational Base + offset (0x01d0)

DATX8 0 DQ Timing Register

Bit	Attr	Reset Value	Description
31:28	RW	0xf	DQDLY7 DQ7 Delay Used to adjust the delay of the data relative to the nominal delay that is matched to the delay of the data strobes through the slave DLL and clock tree. Every four bits of this register control the delay of a different data bit in the byte. The lower two bits of the DQDLY for each DQ bit controls the delay for the data clocked by DQS, while the higher two bits control the delay for the data clocked by DQS_b. Valid settings for each 2-bit control field are: 2'b00: nominal delay 2'b01: nominal delay + 1 step 2'b10: nominal delay + 2 steps 2'b11: nominal delay + 3 steps

Bit	Attr	Reset Value	Description
27:24	RW	0xf	<p>DQDLY6 DQ6 Delay Used to adjust the delay of the data relative to the nominal delay that is matched to the delay of the data strobes through the slave DLL and clock tree. Every four bits of this register control the delay of a different data bit in the byte.</p> <p>The lower two bits of the DQDLY for each DQ bit controls the delay for the data clocked by DQS, while the higher two bits control the delay for the data clocked by DQS_b. Valid settings for each 2-bit control field are:</p> <ul style="list-style-type: none"> 2'b00: nominal delay 2'b01: nominal delay + 1 step 2'b10: nominal delay + 2 steps 2'b11: nominal delay + 3 steps
23:20	RW	0xf	<p>DQDLY5 DQ5 Delay Used to adjust the delay of the data relative to the nominal delay that is matched to the delay of the data strobes through the slave DLL and clock tree. Every four bits of this register control the delay of a different data bit in the byte.</p> <p>The lower two bits of the DQDLY for each DQ bit controls the delay for the data clocked by DQS, while the higher two bits control the delay for the data clocked by DQS_b. Valid settings for each 2-bit control field are:</p> <ul style="list-style-type: none"> 2'b00: nominal delay 2'b01: nominal delay + 1 step 2'b10: nominal delay + 2 steps 2'b11: nominal delay + 3 steps

Bit	Attr	Reset Value	Description
19:16	RW	0xf	<p>DQDLY4 DQ4 Delay Used to adjust the delay of the data relative to the nominal delay that is matched to the delay of the data strobes through the slave DLL and clock tree. Every four bits of this register control the delay of a different data bit in the byte.</p> <p>The lower two bits of the DQDLY for each DQ bit controls the delay for the data clocked by DQS, while the higher two bits control the delay for the data clocked by DQS_b. Valid settings for each 2-bit control field are:</p> <ul style="list-style-type: none"> 2'b00: nominal delay 2'b01: nominal delay + 1 step 2'b10: nominal delay + 2 steps 2'b11: nominal delay + 3 steps
15:12	RW	0xf	<p>DQDLY3 DQ3 Delay Used to adjust the delay of the data relative to the nominal delay that is matched to the delay of the data strobes through the slave DLL and clock tree. Every four bits of this register control the delay of a different data bit in the byte.</p> <p>The lower two bits of the DQDLY for each DQ bit controls the delay for the data clocked by DQS, while the higher two bits control the delay for the data clocked by DQS_b. Valid settings for each 2-bit control field are:</p> <ul style="list-style-type: none"> 2'b00: nominal delay 2'b01: nominal delay + 1 step 2'b10: nominal delay + 2 steps 2'b11: nominal delay + 3 steps

Bit	Attr	Reset Value	Description
11:8	RW	0xf	<p>DQDLY2 DQ2 Delay Used to adjust the delay of the data relative to the nominal delay that is matched to the delay of the data strobes through the slave DLL and clock tree. Every four bits of this register control the delay of a different data bit in the byte.</p> <p>The lower two bits of the DQDLY for each DQ bit controls the delay for the data clocked by DQS, while the higher two bits control the delay for the data clocked by DQS_b. Valid settings for each 2-bit control field are:</p> <ul style="list-style-type: none"> 2'b00: nominal delay 2'b01: nominal delay + 1 step 2'b10: nominal delay + 2 steps 2'b11: nominal delay + 3 steps
7:4	RW	0xf	<p>DQDLY1 DQ1 Delay Used to adjust the delay of the data relative to the nominal delay that is matched to the delay of the data strobes through the slave DLL and clock tree. Every four bits of this register control the delay of a different data bit in the byte.</p> <p>The lower two bits of the DQDLY for each DQ bit controls the delay for the data clocked by DQS, while the higher two bits control the delay for the data clocked by DQS_b. Valid settings for each 2-bit control field are:</p> <ul style="list-style-type: none"> 2'b00: nominal delay 2'b01: nominal delay + 1 step 2'b10: nominal delay + 2 steps 2'b11: nominal delay + 3 steps

Bit	Attr	Reset Value	Description
3:0	RW	0xf	<p>DQDLY0 DQ0 Delay Used to adjust the delay of the data relative to the nominal delay that is matched to the delay of the data strobes through the slave DLL and clock tree. Every four bits of this register control the delay of a different data bit in the byte.</p> <p>The lower two bits of the DQDLY for each DQ bit controls the delay for the data clocked by DQS, while the higher two bits control the delay for the data clocked by DQS_b. Valid settings for each 2-bit control field are:</p> <ul style="list-style-type: none"> 2'b00: nominal delay 2'b01: nominal delay + 1 step 2'b10: nominal delay + 2 steps 2'b11: nominal delay + 3 steps

DDR_PUBL_DX0DQSTR

Address: Operational Base + offset (0x01d4)

DATX8 0 DQS Timing Register

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:26	RW	0xf	<p>DMDLY DM Delay Used to adjust the delay of the data mask relative to the nominal delay that is matched to the delay of the data strobes through the slave DLL and clock tree. The lower two bits of the DQMDLY controls the delay for the data clocked by DQS, while the higher two bits control the delay for the data clocked by DQS_b.</p> <p>Valid settings for each 2-bit control field are:</p> <ul style="list-style-type: none"> 2'b00: nominal delay 2'b01: nominal delay + 1 step 2'b10: nominal delay + 2 steps 2'b11: nominal delay + 3 steps

Bit	Attr	Reset Value	Description
25:23	RW	0x3	<p>DQSNDLY DQS# Delay Used to adjust the delay of the data strobes relative to the nominal delay that is matched to the delay of the data bit through the slave DLL and clock tree. DQSDLY control the delay on DQS strobe and DQSNDLY control the delay on DQS#. Valid values are:</p> <ul style="list-style-type: none"> 3'b000: nominal delay - 3 steps 3'b001: nominal delay - 2 steps 3'b010: nominal delay - 1 step 3'b011: nominal delay 3'b100: nominal delay + 1 step 3'b101: nominal delay + 2 steps 3'b110: nominal delay + 3 steps 3'b111: nominal delay + 4 steps
22:20	RW	0x3	<p>DQSDLY DQS Delay Used to adjust the delay of the data strobes relative to the nominal delay that is matched to the delay of the data bit through the slave DLL and clock tree. DQSDLY control the delay on DQS strobe and DQSNDLY control the delay on DQS#. Valid values are:</p> <ul style="list-style-type: none"> 3'b000: nominal delay - 3 steps 3'b001: nominal delay - 2 steps 3'b010: nominal delay - 1 step 3'b011: nominal delay 3'b100: nominal delay + 1 step 3'b101: nominal delay + 2 steps 3'b110: nominal delay + 3 steps 3'b111: nominal delay + 4 steps
19:16	RO	0x0	reserved

Bit	Attr	Reset Value	Description
15:14	RW	0x2	<p>R1DGPS Rank 1 DQS Gating Phase Select Selects the clock used to enable the data strobes during read so that the value of the data strobes before and after the preamble/postamble are filtered out. The RnDGPS fields are initially set by the PUBL during automatic DQS data training and subsequently updated during data strobe drift compensation. However, these values can be overwritten by a direct write to this register, and the automatic update during DQS drift compensation can be disabled using the PHY General Configuration Register (PGCR). Every two bits of this register control the DQS gating for each of the (up to) four ranks. Valid values for each 2-bit RnDGPS field are:</p> <ul style="list-style-type: none"> 2'b00: 90 deg clock (clk90) 2'b01: 180 deg clock (clk180) 2'b10: 270 deg clock (clk270) 2'b11: 360 deg clock (clk0)
13:12	RW	0x2	<p>R0DGPS Rank 0 DQS Gating Phase Select Selects the clock used to enable the data strobes during read so that the value of the data strobes before and after the preamble/postamble are filtered out. The RnDGPS fields are initially set by the PUBL during automatic DQS data training and subsequently updated during data strobe drift compensation. However, these values can be overwritten by a direct write to this register, and the automatic update during DQS drift compensation can be disabled using the PHY General Configuration Register (PGCR). Every two bits of this register control the DQS gating for each of the (up to) four ranks. Valid values for each 2-bit RnDGPS field are:</p> <ul style="list-style-type: none"> 2'b00: 90 deg clock (clk90) 2'b01: 180 deg clock (clk180) 2'b10: 270 deg clock (clk270) 2'b11: 360 deg clock (clk0)
11:6	RO	0x0	reserved

Bit	Attr	Reset Value	Description
5:3	RW	0x0	<p>R1DGSL Rank 1 DQS Gating System Latency Used to increase the number of clock cycles needed to expect valid DDR read data by up to five extra clock cycles. This is used to compensate for board delays and other system delays. Power-up default is 000 (i.e. no extra clock cycles required). The SL fields are initially set by the PUBL during automatic DQS data training but these values can be overwritten by a direct write to this register. Every three bits of this register control the latency of each of the (up to) four ranks. Valid values are:</p> <ul style="list-style-type: none"> 3'b000: No extra clock cycles 3'b001: 1 extra clock cycle 3'b010: 2 extra clock cycles 3'b011: 3 extra clock cycles 3'b100: 4 extra clock cycles 3'b101: 5 extra clock cycles 3'b110: Reserved 3'b111: Reserved
2:0	RW	0x0	<p>R0DGSL Rank 0 DQS Gating System Latency Used to increase the number of clock cycles needed to expect valid DDR read data by up to five extra clock cycles. This is used to compensate for board delays and other system delays. Power-up default is 000 (i.e. no extra clock cycles required). The SL fields are initially set by the PUBL during automatic DQS data training but these values can be overwritten by a direct write to this register. Every three bits of this register control the latency of each of the (up to) four ranks. Valid values are:</p> <ul style="list-style-type: none"> 3'b000: No extra clock cycles 3'b001: 1 extra clock cycle 3'b010: 2 extra clock cycles 3'b011: 3 extra clock cycles 3'b100: 4 extra clock cycles 3'b101: 5 extra clock cycles 3'b110: Reserved 3'b111: Reserved

DDR_PUBL_DX1GCR

Address: Operational Base + offset (0x0200)
DATX8 1 General Configuration Register

Bit	Attr	Reset Value	Description
31:20	RO	0x0	reserved
16:14 19:17	RW	0x3 0x3	<p>R0RVSL R1RVSL</p> <p>Rank n ITMD Read Valid System Latency Used to specify the read valid system latency relative to the ideal placement of the ITMD read valid signal when DXCCR.RVSEL is set to 0. Power-up default is 011 (i.e. ideal placement of the the read valid signal). The RVSL fields are initially set by the PUB during automatic read valid training but these values can be overwritten by a direct write to this register. Every three bits of this register control the latency of each rank. R0RVSL controls the latency of rank 0, R1RVSL controls rank 1.</p> <p>Valid values are:</p> <ul style="list-style-type: none"> 3'b000: read valid system latency = ideal placement - 3 3'b001: read valid system latency = ideal placement - 2 3'b010: read valid system latency = ideal placement - 1 3'b011: read valid system latency = ideal placement 3'b100: read valid system latency = ideal placement + 1 3'b101: read valid system latency = ideal placement + 2 3'b110: read valid system latency = ideal placement + 3 3'b111: Reserved
13	RW	0x0	<p>RTTOAL RTT On Additive Latency</p> <p>Indicates when the ODT control of DQ/DQS SSTL I/Os is set to the value in DQODT/DQSODT during read cycles.</p> <p>Valid values are:</p> <ul style="list-style-type: none"> 1'b0: ODT control is set to DQSODT/DQODT almost two cycles before read data preamble 1'b1: ODT control is set to DQSODT/DQODT almost one cycle before read data preamble
12:11	RW	0x0	<p>RTTOH RTT Output Hold</p> <p>Indicates the number of clock cycles (from 0 to 3) after the read data postamble for which ODT control should remain set to DQSODT for DQS or DQODT for DQ/DM before disabling it (setting it to '0' when using dynamic ODT control. ODT is disabled almost RTTOH clock cycles after the read postamble.</p>

Bit	Attr	Reset Value	Description
10	RW	0x1	DQRTT DQ Dynamic RTT Control Indicates, if set, that the ODT control of DQ/DM SSTL I/Os be dynamically controlled by setting it to the value in DQODT during reads and disabling it (setting it to '0' during any other cycle. If this bit is not set, then the ODT control of DQ SSTL I/Os is always set to the value in DQODT.
9	RW	0x1	DQSRTT DQS Dynamic RTT Control Indicates, if set, that the ODT control of DQS SSTL I/Os be dynamically controlled by setting it to the value in DQSODT during reads and disabling it (setting it to '0' during any other cycle. If this bit is not set, then the ODT control of DQS SSTL I/Os is always set to the value in DQSODT field.
8:7	RW	0x1	DSEN Write DQS Enable Controls whether the write DQS going to the SDRAM is enabled (toggling) or disabled (static value) and whether the DQS is inverted. DQS# is always the inversion of DQS. These values are valid only when DQS/DQS# output enable is on, otherwise the DQS/DQS# is tristated. Valid settings are: 2'b00: DQS disabled (Driven to constant 0) 2'b01: DQS toggling with inverted polarity 2'b10: DQS toggling with normal polarity (This should be the default setting) 2'b11: DQS disabled (Driven to constant 1)
6	RW	0x0	DQSRPD DQSR Power Down Powers down, if set, the PDQSR cell. This bit is ORed with the common PDR configuration bit.
5	RW	0x0	DXPDR Data Power Down Receiver Powers down, when set, the input receiver on I/O for DQ, DM, and DQS/DQS# pins of the byte. This bit is ORed with the common PDR configuration bit.
4	RW	0x0	DXPDD Data Power Down Driver Powers down, when set, the output driver on I/O for DQ, DM, and DQS/DQS# pins of the byte. This bit is ORed with the common PDD configuration bit.

Bit	Attr	Reset Value	Description
3	RW	0x0	DXIOM Data I/O Mode Selects SSTL mode (when set to 0) or CMOS mode (when set to 1) of the I/O for DQ, DM, and DQS/DQS# pins of the byte. This bit is ORed with the IOM configuration bit of the individual DATX8.
2	RW	0x0	DQODT Data On-Die Termination Enables, when set, the on-die termination on the I/O for DQ and DM pins of the byte. This bit is ORed with the common DATX8 ODT configuration bit.
1	RW	0x0	DQSODT DQS On-Die Termination Enables, when set, the on-die termination on the I/O for DQS/DQS# pin of the byte. This bit is ORed with the common DATX8 ODT configuration bit.
0	RW	0x1	DXEN Data Byte Enable Enables if set the DATX8 and SSTL I/Os used on the data byte. Setting this bit to '0' disables the byte, i.e. the byte SSTL I/Os are put in power-down mode and the DLL in the DATX8 is put in bypass mode.

DDR_PUBL_DX1GSR0

Address: Operational Base + offset (0x0204)

DATX8 1 General Status Register 0

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24:13	RO	0x000	DTPASS DQS Gate Training Pass Count The number of passing configurations during DQS gate training. Bits [2:0] are for rank 0, bits [5:3] for rank 1, and so on.
12	RO	0x0	reserved
11:8	RO	0x0	DTIERR DQS Gate Training Intermittent Error If set, indicates that there was an intermittent error during DQS gate training of the byte, such as a pass was followed by a fail then followed by another pass. Bit [0] is for rank 0, bit 1 for rank 1, and so on.

Bit	Attr	Reset Value	Description
7:4	RO	0x0	DTERR DQS Gate Training Error If set, indicates that a valid DQS gating window could not be found during DQS gate training of the byte. Bit [0] is for rank 0, bit 1 for rank 1, and so on.
3:0	RO	0x0	DTDONE Data Training Done Indicates, if set, that the byte has finished doing data training. Bit [0] is for rank 0, bit 1 for rank 1, and so on.

DDR_PUBL_DX1GSR1

Address: Operational Base + offset (0x0208)

DATX8 1 General Status Register 1

Bit	Attr	Reset Value	Description
31:20	RO	0x0	RVPASS Read Valid Training Pass Count The number of passing configurations during read valid training. Bits [2:0] are for rank 0, bits [5:3] for rank 1, and so on.
19:16	RO	0x0	RVIERR Read Valid Training Intermittent Error If set, indicates that there was an intermittent error during read valid training of the byte, such as a pass was followed by a fail then followed by another pass. Bit [0] is for rank 0, bit 1 for rank 1, and so on.
15:12	RO	0x0	RVERR Read Valid Training Error If set, indicates that a valid read valid placement could not be found during read valid training of the byte. Bit [0] is for rank 0, bit 1 for rank 1, and so on.
11:4	RO	0x00	DQSDFT DQS Drift Used to report the drift on the read data strobe of the data byte. Valid settings are: 2'b00: No drift 2'b01: 90 deg drift 2'b10: 180 deg drift 2'b11: 270 deg drift or more Bits [1:0] are for rank 0, bits [3:2] for rank 1, and so on.

Bit	Attr	Reset Value	Description
3:0	RO	0x0	DFTERR DQS Drift Error If set, indicates that the byte read data strobe has drifted by more than or equal to the drift limit set in the PHY General Configuration Register (PGCR). Bit [0] is for rank 0, bit 1 for rank 1, and so on.

DDR_PUBL_DX1DLLCR

Address: Operational Base + offset (0x020c)

DATX8 1 DLL Control Register

Bit	Attr	Reset Value	Description
31	RW	0x0	DLLDIS DLL Disable A disabled DLL is bypassed. Default ('0') is DLL enabled
30	RW	0x1	DLLSRST DLL Soft Rest Soft resets the byte DLL by driving the DLL soft reset pin
29:20	RO	0x0	reserved
19	RW	0x0	SDLBMODE Slave DLL Loopback Mode If this bit is set, the slave DLL is put in loopback mode in which there is no 90 degrees phase shift on read DQS/DQS#. This bit must be set when operating the byte PHYs in loopback mode such as during BIST loopback. Applicable only to PHYs that have this feature. Refer to PHY databook.
18	RW	0x0	ATESTEN Analog Test Enable Enables the analog test signal to be output on the DLL analog test output (test_out_a). The DLL analog test output is tri-stated when this bit is '0'.

Bit	Attr	Reset Value	Description
17:14	RW	0x0	<p>SDPHASE Slave DLL Phase Trim Selects the phase difference between the input clock and the corresponding output clock of the slave DLL. Valid settings:</p> <ul style="list-style-type: none"> 4'b0000: 90 4'b0001: 72 4'b0010: 54 4'b0011: 36 4'b0100: 108 4'b0101: 90 4'b0110: 72 4'b0111: 54 4'b1000: 126 4'b1001: 108 4'b1010: 90 4'b1011: 72 4'b1100: 144 4'b1101: 126 4'b1110: 108 4'b1111: 90
13:12	RW	0x0	<p>SSTART Slave Auto Start-Up Used to control how the slave DLL starts up relative to the master DLL locking:</p> <ul style="list-style-type: none"> 2'b0X: Slave DLL automatically starts up once the master DLL has achieved lock 2'b10: The automatic startup of the slave DLL is disabled; the phase detector is disabled 2'b11: The automatic startup of the slave DLL is disabled; the phase detector is enabled
11:9	RW	0x0	<p>MFWDLY Master Feed-Forward Delay Trim Used to trim the delay in the master DLL feed-forward path:</p> <ul style="list-style-type: none"> 3'b000: minimum delay 3'b111: maximum delay
8:6	RW	0x0	<p>MFBDLY Master Feed-Back Delay Trim Used to trim the delay in the master DLL feedback path:</p> <ul style="list-style-type: none"> 3'b000: minimum delay 3'b111: maximum delay

Bit	Attr	Reset Value	Description
5:3	RW	0x0	SFWDLY Slave Feed-Forward Delay Trim Used to trim the delay in the slave DLL feed-forward path: 3'b000: minimum delay 3'b111: maximum delay
2:0	RW	0x0	SFBDLY Slave Feed-Back Delay Trim Used to trim the delay in the slave DLL feedback path: 3'b000: minimum delay 3'b111: maximum delay

DDR_PUBL_DX1DQTR

Address: Operational Base + offset (0x0210)

DATX8 1 DQ Timing Register

Bit	Attr	Reset Value	Description
31:28	RW	0xf	DQDLY7 DQ7 Delay Used to adjust the delay of the data relative to the nominal delay that is matched to the delay of the data strobes through the slave DLL and clock tree. Every four bits of this register control the delay of a different data bit in the byte. The lower two bits of the DQDLY for each DQ bit controls the delay for the data clocked by DQS, while the higher two bits control the delay for the data clocked by DQS_b. Valid settings for each 2-bit control field are: 2'b00: nominal delay 2'b01: nominal delay + 1 step 2'b10: nominal delay + 2 steps 2'b11: nominal delay + 3 steps

Bit	Attr	Reset Value	Description
27:24	RW	0xf	<p>DQDLY6 DQ6 Delay Used to adjust the delay of the data relative to the nominal delay that is matched to the delay of the data strobes through the slave DLL and clock tree. Every four bits of this register control the delay of a different data bit in the byte.</p> <p>The lower two bits of the DQDLY for each DQ bit controls the delay for the data clocked by DQS, while the higher two bits control the delay for the data clocked by DQS_b. Valid settings for each 2-bit control field are:</p> <ul style="list-style-type: none"> 2'b00: nominal delay 2'b01: nominal delay + 1 step 2'b10: nominal delay + 2 steps 2'b11: nominal delay + 3 steps
23:20	RW	0xf	<p>DQDLY5 DQ5 Delay Used to adjust the delay of the data relative to the nominal delay that is matched to the delay of the data strobes through the slave DLL and clock tree. Every four bits of this register control the delay of a different data bit in the byte.</p> <p>The lower two bits of the DQDLY for each DQ bit controls the delay for the data clocked by DQS, while the higher two bits control the delay for the data clocked by DQS_b. Valid settings for each 2-bit control field are:</p> <ul style="list-style-type: none"> 2'b00: nominal delay 2'b01: nominal delay + 1 step 2'b10: nominal delay + 2 steps 2'b11: nominal delay + 3 steps

Bit	Attr	Reset Value	Description
19:16	RW	0xf	<p>DQDLY4 DQ4 Delay Used to adjust the delay of the data relative to the nominal delay that is matched to the delay of the data strobes through the slave DLL and clock tree. Every four bits of this register control the delay of a different data bit in the byte.</p> <p>The lower two bits of the DQDLY for each DQ bit controls the delay for the data clocked by DQS, while the higher two bits control the delay for the data clocked by DQS_b. Valid settings for each 2-bit control field are:</p> <ul style="list-style-type: none"> 2'b00: nominal delay 2'b01: nominal delay + 1 step 2'b10: nominal delay + 2 steps 2'b11: nominal delay + 3 steps
15:12	RW	0xf	<p>DQDLY3 DQ3 Delay Used to adjust the delay of the data relative to the nominal delay that is matched to the delay of the data strobes through the slave DLL and clock tree. Every four bits of this register control the delay of a different data bit in the byte.</p> <p>The lower two bits of the DQDLY for each DQ bit controls the delay for the data clocked by DQS, while the higher two bits control the delay for the data clocked by DQS_b. Valid settings for each 2-bit control field are:</p> <ul style="list-style-type: none"> 2'b00: nominal delay 2'b01: nominal delay + 1 step 2'b10: nominal delay + 2 steps 2'b11: nominal delay + 3 steps

Bit	Attr	Reset Value	Description
11:8	RW	0xf	<p>DQDLY2 DQ2 Delay Used to adjust the delay of the data relative to the nominal delay that is matched to the delay of the data strobes through the slave DLL and clock tree. Every four bits of this register control the delay of a different data bit in the byte.</p> <p>The lower two bits of the DQDLY for each DQ bit controls the delay for the data clocked by DQS, while the higher two bits control the delay for the data clocked by DQS_b. Valid settings for each 2-bit control field are:</p> <ul style="list-style-type: none"> 2'b00: nominal delay 2'b01: nominal delay + 1 step 2'b10: nominal delay + 2 steps 2'b11: nominal delay + 3 steps
7:4	RW	0xf	<p>DQDLY1 DQ1 Delay Used to adjust the delay of the data relative to the nominal delay that is matched to the delay of the data strobes through the slave DLL and clock tree. Every four bits of this register control the delay of a different data bit in the byte.</p> <p>The lower two bits of the DQDLY for each DQ bit controls the delay for the data clocked by DQS, while the higher two bits control the delay for the data clocked by DQS_b. Valid settings for each 2-bit control field are:</p> <ul style="list-style-type: none"> 2'b00: nominal delay 2'b01: nominal delay + 1 step 2'b10: nominal delay + 2 steps 2'b11: nominal delay + 3 steps

Bit	Attr	Reset Value	Description
3:0	RW	0xf	<p>DQDLY0 DQ0 Delay Used to adjust the delay of the data relative to the nominal delay that is matched to the delay of the data strobes through the slave DLL and clock tree. Every four bits of this register control the delay of a different data bit in the byte.</p> <p>The lower two bits of the DQDLY for each DQ bit controls the delay for the data clocked by DQS, while the higher two bits control the delay for the data clocked by DQS_b. Valid settings for each 2-bit control field are:</p> <ul style="list-style-type: none"> 2'b00: nominal delay 2'b01: nominal delay + 1 step 2'b10: nominal delay + 2 steps 2'b11: nominal delay + 3 steps

DDR_PUBL_DX1DQSTR

Address: Operational Base + offset (0x0214)

DATX8 1 DQS Timing Register

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:26	RW	0xf	<p>DMDLY Used to adjust the delay of the data mask relative to the nominal delay that is matched to the delay of the data strobes through the slave DLL and clock tree. The lower two bits of the DQMDLY controls the delay for the data clocked by DQS, while the higher two bits control the delay for the data clocked by DQS_b.</p> <p>Valid settings for each 2-bit control field are:</p> <ul style="list-style-type: none"> 2'b00: nominal delay 2'b01: nominal delay + 1 step 2'b10: nominal delay + 2 steps 2'b11: nominal delay + 3 steps

Bit	Attr	Reset Value	Description
25:23	RW	0x3	<p>DQSNDLY DQS# Delay Used to adjust the delay of the data strobes relative to the nominal delay that is matched to the delay of the data bit through the slave DLL and clock tree. DQSDLY control the delay on DQS strobe and DQSNDLY control the delay on DQS#. Valid values are:</p> <p>3'b000: nominal delay - 3 steps 3'b001: nominal delay - 2 steps 3'b010: nominal delay - 1 step 3'b011: nominal delay 3'b100: nominal delay + 1 step 3'b101: nominal delay + 2 steps 3'b110: nominal delay + 3 steps 3'b111: nominal delay + 4 steps</p>
22:20	RW	0x3	<p>DQSDLY DQS Delay Used to adjust the delay of the data strobes relative to the nominal delay that is matched to the delay of the data bit through the slave DLL and clock tree. DQSDLY control the delay on DQS strobe and DQSNDLY control the delay on DQS#. Valid values are:</p> <p>3'b000: nominal delay - 3 steps 3'b001: nominal delay - 2 steps 3'b010: nominal delay - 1 step 3'b011: nominal delay 3'b100: nominal delay + 1 step 3'b101: nominal delay + 2 steps 3'b110: nominal delay + 3 steps 3'b111: nominal delay + 4 steps</p>
19:16	RO	0x0	reserved

Bit	Attr	Reset Value	Description
15:14	RW	0x2	<p>R1DGPS</p> <p>Rank 1 DQS Gating Phase Select</p> <p>Selects the clock used to enable the data strobes during read so that the value of the data strobes before and after the preamble/postamble are filtered out. The RnDGPS fields are initially set by the PUBL during automatic DQS data training and subsequently updated during data strobe drift compensation. However, these values can be overwritten by a direct write to this register, and the automatic update during DQS drift compensation can be disabled using the PHY General Configuration Register (PGCR). Every two bits of this register control the DQS gating for each of the (up to) four ranks. Valid values for each 2-bit RnDGPS field are:</p> <ul style="list-style-type: none"> 2'b00: 90 deg clock (clk90) 2'b01: 180 deg clock (clk180) 2'b10: 270 deg clock (clk270) 2'b11: 360 deg clock (clk0)
13:12	RW	0x2	<p>R0DGPS</p> <p>Rank 0 DQS Gating Phase Select</p> <p>Selects the clock used to enable the data strobes during read so that the value of the data strobes before and after the preamble/postamble are filtered out. The RnDGPS fields are initially set by the PUBL during automatic DQS data training and subsequently updated during data strobe drift compensation. However, these values can be overwritten by a direct write to this register, and the automatic update during DQS drift compensation can be disabled using the PHY General Configuration Register (PGCR). Every two bits of this register control the DQS gating for each of the (up to) four ranks. Valid values for each 2-bit RnDGPS field are:</p> <ul style="list-style-type: none"> 2'b00: 90 deg clock (clk90) 2'b01: 180 deg clock (clk180) 2'b10: 270 deg clock (clk270) 2'b11: 360 deg clock (clk0)
11:6	RO	0x0	reserved

Bit	Attr	Reset Value	Description
5:3	RW	0x0	<p>R1DGSL Rank 1 DQS Gating System Latency Used to increase the number of clock cycles needed to expect valid DDR read data by up to five extra clock cycles. This is used to compensate for board delays and other system delays. Power-up default is 000 (i.e. no extra clock cycles required). The SL fields are initially set by the PUBL during automatic DQS data training but these values can be overwritten by a direct write to this register. Every three bits of this register control the latency of each of the (up to) four ranks. Valid values are:</p> <ul style="list-style-type: none"> 3'b000: No extra clock cycles 3'b001: 1 extra clock cycle 3'b010: 2 extra clock cycles 3'b011: 3 extra clock cycles 3'b100: 4 extra clock cycles 3'b101: 5 extra clock cycles 3'b110: Reserved 3'b111: Reserved
2:0	RW	0x0	<p>R0DGSL Rank 0 DQS Gating System Latency Used to increase the number of clock cycles needed to expect valid DDR read data by up to five extra clock cycles. This is used to compensate for board delays and other system delays. Power-up default is 000 (i.e. no extra clock cycles required). The SL fields are initially set by the PUBL during automatic DQS data training but these values can be overwritten by a direct write to this register. Every three bits of this register control the latency of each of the (up to) four ranks. Valid values are:</p> <ul style="list-style-type: none"> 3'b000: No extra clock cycles 3'b001: 1 extra clock cycle 3'b010: 2 extra clock cycles 3'b011: 3 extra clock cycles 3'b100: 4 extra clock cycles 3'b101: 5 extra clock cycles 3'b110: Reserved 3'b111: Reserved

DDR_PUBL_DX2GCR

Address: Operational Base + offset (0x0240)
DATX8 2 General Configuration Register

Bit	Attr	Reset Value	Description
31:20	RO	0x0	reserved
16:14 19:17	RW	0x3 0x3	<p>R0RVSL R1RVSL</p> <p>Rank n ITMD Read Valid System Latency Used to specify the read valid system latency relative to the ideal placement of the ITMD read valid signal when DXCCR.RVSEL is set to 0. Power-up default is 011 (i.e. ideal placement of the the read valid signal). The RVSL fields are initially set by the PUB during automatic read valid training but these values can be overwritten by a direct write to this register. Every three bits of this register control the latency of each rank. R0RVSL controls the latency of rank 0, R1RVSL controls rank 1. Valid values are:</p> <ul style="list-style-type: none"> 3'b000: read valid system latency = ideal placement - 3 3'b001: read valid system latency = ideal placement - 2 3'b010: read valid system latency = ideal placement - 1 3'b011: read valid system latency = ideal placement 3'b100: read valid system latency = ideal placement + 1 3'b101: read valid system latency = ideal placement + 2 3'b110: read valid system latency = ideal placement + 3 3'b111: Reserved
13	RW	0x0	<p>RTTOAL RTT On Additive Latency</p> <p>Indicates when the ODT control of DQ/DQS SSTL I/Os is set to the value in DQODT/DQSODT during read cycles.</p> <p>Valid values are:</p> <ul style="list-style-type: none"> 1'b0: ODT control is set to DQSODT/DQODT almost two cycles before read data preamble 1'b1: ODT control is set to DQSODT/DQODT almost one cycle before read data preamble
12:11	RW	0x0	<p>RTTOH RTT Output Hold</p> <p>Indicates the number of clock cycles (from 0 to 3) after the read data postamble for which ODT control should remain set to DQSODT for DQS or DQODT for DQ/DM before disabling it (setting it to '0' when using dynamic ODT control. ODT is disabled almost RTTOH clock cycles after the read postamble.</p>

Bit	Attr	Reset Value	Description
10	RW	0x1	DQRTT DQ Dynamic RTT Control Indicates, if set, that the ODT control of DQ/DM SSTL I/Os be dynamically controlled by setting it to the value in DQODT during reads and disabling it (setting it to '0' during any other cycle. If this bit is not set, then the ODT control of DQ SSTL I/Os is always set to the value in DQODT.
9	RW	0x1	DQSRTT DQS Dynamic RTT Control Indicates, if set, that the ODT control of DQS SSTL I/Os be dynamically controlled by setting it to the value in DQSODT during reads and disabling it (setting it to '0' during any other cycle. If this bit is not set, then the ODT control of DQS SSTL I/Os is always set to the value in DQSODT field.
8:7	RW	0x1	DSEN Write DQS Enable Controls whether the write DQS going to the SDRAM is enabled (toggling) or disabled (static value) and whether the DQS is inverted. DQS# is always the inversion of DQS. These values are valid only when DQS/DQS# output enable is on, otherwise the DQS/DQS# is tristated. Valid settings are: 2'b00: DQS disabled (Driven to constant 0) 2'b01: DQS toggling with inverted polarity 2'b10: DQS toggling with normal polarity (This should be the default setting) 2'b11: DQS disabled (Driven to constant 1)
6	RW	0x0	DQSRPD DQSR Power Down Powers down, if set, the PDQSR cell. This bit is ORed with the common PDR configuration bit.
5	RW	0x0	DXPDR Data Power Down Receiver Powers down, when set, the input receiver on I/O for DQ, DM, and DQS/DQS# pins of the byte. This bit is ORed with the common PDR configuration bit.
4	RW	0x0	DXPDD Data Power Down Driver Powers down, when set, the output driver on I/O for DQ, DM, and DQS/DQS# pins of the byte. This bit is ORed with the common PDD configuration bit.

Bit	Attr	Reset Value	Description
3	RW	0x0	DXIOM Data I/O Mode Selects SSTL mode (when set to 0) or CMOS mode (when set to 1) of the I/O for DQ, DM, and DQS/DQS# pins of the byte. This bit is ORed with the IOM configuration bit of the individual DATX8.
2	RW	0x0	DQODT Data On-Die Termination Enables, when set, the on-die termination on the I/O for DQ and DM pins of the byte. This bit is ORed with the common DATX8 ODT configuration bit.
1	RW	0x0	DQSODT DQS On-Die Termination Enables, when set, the on-die termination on the I/O for DQS/DQS# pin of the byte. This bit is ORed with the common DATX8 ODT configuration bit.
0	RW	0x1	DXEN Data Byte Enable Enables if set the DATX8 and SSTL I/Os used on the data byte. Setting this bit to '0' disables the byte, i.e. the byte SSTL I/Os are put in power-down mode and the DLL in the DATX8 is put in bypass mode.

DDR_PUBL_DX2GSR0

Address: Operational Base + offset (0x0244)

DATX8 2 General Status Register 0

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24:13	RO	0x000	DTPASS DQS Gate Training Pass Count The number of passing configurations during DQS gate training. Bits [2:0] are for rank 0, bits [5:3] for rank 1, and so on.
12	RO	0x0	reserved
11:8	RO	0x0	DTIERR DQS Gate Training Intermittent Error If set, indicates that there was an intermittent error during DQS gate training of the byte, such as a pass was followed by a fail then followed by another pass. Bit [0] is for rank 0, bit 1 for rank 1, and so on.

Bit	Attr	Reset Value	Description
7:4	RO	0x0	DTERR DQS Gate Training Error If set, indicates that a valid DQS gating window could not be found during DQS gate training of the byte. Bit [0] is for rank 0, bit 1 for rank 1, and so on.
3:0	RO	0x0	DTDONE Data Training Done Indicates, if set, that the byte has finished doing data training. Bit [0] is for rank 0, bit 1 for rank 1, and so on.

DDR_PUBL_DX2GSR1

Address: Operational Base + offset (0x0248)

DATX8 2 General Status Register 1

Bit	Attr	Reset Value	Description
31:20	RO	0x0	RVPASS Read Valid Training Pass Count The number of passing configurations during read valid training. Bits [2:0] are for rank 0, bits [5:3] for rank 1, and so on.
19:16	RO	0x0	RVIERR Read Valid Training Intermittent Error If set, indicates that there was an intermittent error during read valid training of the byte, such as a pass was followed by a fail then followed by another pass. Bit [0] is for rank 0, bit 1 for rank 1, and so on.
15:12	RO	0x0	RVERR Read Valid Training Error If set, indicates that a valid read valid placement could not be found during read valid training of the byte. Bit [0] is for rank 0, bit 1 for rank 1, and so on.
11:4	RO	0x00	DQSDFT DQS Drift Used to report the drift on the read data strobe of the data byte. Valid settings are: 2'b00: No drift 2'b01: 90 deg drift 2'b10: 180 deg drift 2'b11: 270 deg drift or more Bits [1:0] are for rank 0, bits [3:2] for rank 1, and so on.

Bit	Attr	Reset Value	Description
3:0	RO	0x0	DFTERR DQS Drift Error If set, indicates that the byte read data strobe has drifted by more than or equal to the drift limit set in the PHY General Configuration Register (PGCR). Bit [0] is for rank 0, bit 1 for rank 1, and so on.

DDR_PUBL_DX2DLLCR

Address: Operational Base + offset (0x024c)

DATX8 2 DLL Control Register

Bit	Attr	Reset Value	Description
31	RW	0x0	DLLDIS DLL Disable A disabled DLL is bypassed. Default ('0') is DLL enabled
30	RW	0x1	DLLSRST DLL Soft Rest Soft resets the byte DLL by driving the DLL soft reset pin
29:20	RO	0x0	reserved
19	RW	0x0	SDLBMODE Slave DLL Loopback Mode If this bit is set, the slave DLL is put in loopback mode in which there is no 90 degrees phase shift on read DQS/DQS#. This bit must be set when operating the byte PHYs in loopback mode such as during BIST loopback. Applicable only to PHYs that have this feature. Refer to PHY databook.
18	RW	0x0	ATESTEN Analog Test Enable Enables the analog test signal to be output on the DLL analog test output (test_out_a). The DLL analog test output is tri-stated when this bit is '0'.

Bit	Attr	Reset Value	Description
17:14	RW	0x0	<p>SDPHASE Slave DLL Phase Trim Selects the phase difference between the input clock and the corresponding output clock of the slave DLL. Valid settings:</p> <ul style="list-style-type: none"> 4'b0000: 90 4'b0001: 72 4'b0010: 54 4'b0011: 36 4'b0100: 108 4'b0101: 90 4'b0110: 72 4'b0111: 54 4'b1000: 126 4'b1001: 108 4'b1010: 90 4'b1011: 72 4'b1100: 144 4'b1101: 126 4'b1110: 108 4'b1111: 90
13:12	RW	0x0	<p>SSTART Slave Auto Start-Up Used to control how the slave DLL starts up relative to the master DLL locking:</p> <ul style="list-style-type: none"> 2'b0X: Slave DLL automatically starts up once the master DLL has achieved lock 2'b10: The automatic startup of the slave DLL is disabled; the phase detector is disabled 2'b11: The automatic startup of the slave DLL is disabled; the phase detector is enabled
11:9	RW	0x0	<p>MFWDLY Master Feed-Forward Delay Trim Used to trim the delay in the master DLL feed-forward path:</p> <ul style="list-style-type: none"> 3'b000: minimum delay 3'b111: maximum delay
8:6	RW	0x0	<p>MFBDLY Master Feed-Back Delay Trim Used to trim the delay in the master DLL feedback path:</p> <ul style="list-style-type: none"> 3'b000: minimum delay 3'b111: maximum delay

Bit	Attr	Reset Value	Description
5:3	RW	0x0	SFWDLY Slave Feed-Forward Delay Trim Used to trim the delay in the slave DLL feed-forward path: 3'b000: minimum delay 3'b111: maximum delay
2:0	RW	0x0	SFBDLY Slave Feed-Back Delay Trim Used to trim the delay in the slave DLL feedback path: 3'b000: minimum delay 3'b111: maximum delay

DDR_PUBL_DX2DQTR

Address: Operational Base + offset (0x0250)

DATX8 2 DQ Timing Register

Bit	Attr	Reset Value	Description
31:28	RW	0xf	DQDLY7 DQ7 Delay Used to adjust the delay of the data relative to the nominal delay that is matched to the delay of the data strobes through the slave DLL and clock tree. Every four bits of this register control the delay of a different data bit in the byte. The lower two bits of the DQDLY for each DQ bit controls the delay for the data clocked by DQS, while the higher two bits control the delay for the data clocked by DQS_b. Valid settings for each 2-bit control field are: 2'b00: nominal delay 2'b01: nominal delay + 1 step 2'b10: nominal delay + 2 steps 2'b11: nominal delay + 3 steps

Bit	Attr	Reset Value	Description
27:24	RW	0xf	<p>DQDLY6 DQ6 Delay Used to adjust the delay of the data relative to the nominal delay that is matched to the delay of the data strobes through the slave DLL and clock tree. Every four bits of this register control the delay of a different data bit in the byte.</p> <p>The lower two bits of the DQDLY for each DQ bit controls the delay for the data clocked by DQS, while the higher two bits control the delay for the data clocked by DQS_b. Valid settings for each 2-bit control field are:</p> <ul style="list-style-type: none"> 2'b00: nominal delay 2'b01: nominal delay + 1 step 2'b10: nominal delay + 2 steps 2'b11: nominal delay + 3 steps
23:20	RW	0xf	<p>DQDLY5 DQ5 Delay Used to adjust the delay of the data relative to the nominal delay that is matched to the delay of the data strobes through the slave DLL and clock tree. Every four bits of this register control the delay of a different data bit in the byte.</p> <p>The lower two bits of the DQDLY for each DQ bit controls the delay for the data clocked by DQS, while the higher two bits control the delay for the data clocked by DQS_b. Valid settings for each 2-bit control field are:</p> <ul style="list-style-type: none"> 2'b00: nominal delay 2'b01: nominal delay + 1 step 2'b10: nominal delay + 2 steps 2'b11: nominal delay + 3 steps

Bit	Attr	Reset Value	Description
19:16	RW	0xf	<p>DQDLY4 DQ4 Delay Used to adjust the delay of the data relative to the nominal delay that is matched to the delay of the data strobes through the slave DLL and clock tree. Every four bits of this register control the delay of a different data bit in the byte.</p> <p>The lower two bits of the DQDLY for each DQ bit controls the delay for the data clocked by DQS, while the higher two bits control the delay for the data clocked by DQS_b. Valid settings for each 2-bit control field are:</p> <ul style="list-style-type: none"> 2'b00: nominal delay 2'b01: nominal delay + 1 step 2'b10: nominal delay + 2 steps 2'b11: nominal delay + 3 steps
15:12	RW	0xf	<p>DQDLY3 DQ3 Delay Used to adjust the delay of the data relative to the nominal delay that is matched to the delay of the data strobes through the slave DLL and clock tree. Every four bits of this register control the delay of a different data bit in the byte.</p> <p>The lower two bits of the DQDLY for each DQ bit controls the delay for the data clocked by DQS, while the higher two bits control the delay for the data clocked by DQS_b. Valid settings for each 2-bit control field are:</p> <ul style="list-style-type: none"> 2'b00: nominal delay 2'b01: nominal delay + 1 step 2'b10: nominal delay + 2 steps 2'b11: nominal delay + 3 steps

Bit	Attr	Reset Value	Description
11:8	RW	0xf	<p>DQDLY2 DQ2 Delay Used to adjust the delay of the data relative to the nominal delay that is matched to the delay of the data strobes through the slave DLL and clock tree. Every four bits of this register control the delay of a different data bit in the byte.</p> <p>The lower two bits of the DQDLY for each DQ bit controls the delay for the data clocked by DQS, while the higher two bits control the delay for the data clocked by DQS_b. Valid settings for each 2-bit control field are:</p> <ul style="list-style-type: none"> 2'b00: nominal delay 2'b01: nominal delay + 1 step 2'b10: nominal delay + 2 steps 2'b11: nominal delay + 3 steps
7:4	RW	0xf	<p>DQDLY1 DQ1 Delay Used to adjust the delay of the data relative to the nominal delay that is matched to the delay of the data strobes through the slave DLL and clock tree. Every four bits of this register control the delay of a different data bit in the byte.</p> <p>The lower two bits of the DQDLY for each DQ bit controls the delay for the data clocked by DQS, while the higher two bits control the delay for the data clocked by DQS_b. Valid settings for each 2-bit control field are:</p> <ul style="list-style-type: none"> 2'b00: nominal delay 2'b01: nominal delay + 1 step 2'b10: nominal delay + 2 steps 2'b11: nominal delay + 3 steps

Bit	Attr	Reset Value	Description
3:0	RW	0xf	<p>DQDLY0 DQ0 Delay Used to adjust the delay of the data relative to the nominal delay that is matched to the delay of the data strobes through the slave DLL and clock tree.</p> <p>Every four bits of this register control the delay of a different data bit in the byte.</p> <p>The lower two bits of the DQDLY for each DQ bit controls the delay for the data clocked by DQS, while the higher two bits control the delay for the data clocked by DQS_b. Valid settings for each 2-bit control field are:</p> <ul style="list-style-type: none"> 2'b00: nominal delay 2'b01: nominal delay + 1 step 2'b10: nominal delay + 2 steps 2'b11: nominal delay + 3 steps

DDR_PUBL_DX2DQSTR

Address: Operational Base + offset (0x0254)

DATX8 2 DQS Timing Register

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:26	RW	0xf	<p>DMDLY DM Delay Used to adjust the delay of the data mask relative to the nominal delay that is matched to the delay of the data strobes through the slave DLL and clock tree. The lower two bits of the DQMDLY controls the delay for the data clocked by DQS, while the higher two bits control the delay for the data clocked by DQS_b.</p> <p>Valid settings for each 2-bit control field are:</p> <ul style="list-style-type: none"> 2'b00: nominal delay 2'b01: nominal delay + 1 step 2'b10: nominal delay + 2 steps 2'b11: nominal delay + 3 steps

Bit	Attr	Reset Value	Description
25:23	RW	0x3	<p>DQSNDLY DQS# Delay Used to adjust the delay of the data strobes relative to the nominal delay that is matched to the delay of the data bit through the slave DLL and clock tree. DQSDLY control the delay on DQS strobe and DQSNDLY control the delay on DQS#. Valid values are:</p> <ul style="list-style-type: none"> 3'b000: nominal delay - 3 steps 3'b001: nominal delay - 2 steps 3'b010: nominal delay - 1 step 3'b011: nominal delay 3'b100: nominal delay + 1 step 3'b101: nominal delay + 2 steps 3'b110: nominal delay + 3 steps 3'b111: nominal delay + 4 steps
22:20	RW	0x3	<p>DQSDLY DQS Delay Used to adjust the delay of the data strobes relative to the nominal delay that is matched to the delay of the data bit through the slave DLL and clock tree. DQSDLY control the delay on DQS strobe and DQSNDLY control the delay on DQS#. Valid values are:</p> <ul style="list-style-type: none"> 3'b000: nominal delay - 3 steps 3'b001: nominal delay - 2 steps 3'b010: nominal delay - 1 step 3'b011: nominal delay 3'b100: nominal delay + 1 step 3'b101: nominal delay + 2 steps 3'b110: nominal delay + 3 steps 3'b111: nominal delay + 4 steps
19:16	RO	0x0	reserved

Bit	Attr	Reset Value	Description
15:14	RW	0x2	<p>R1DGPS Rank 1 DQS Gating Phase Select Selects the clock used to enable the data strobes during read so that the value of the data strobes before and after the preamble/postamble are filtered out. The RnDGPS fields are initially set by the PUBL during automatic DQS data training and subsequently updated during data strobe drift compensation. However, these values can be overwritten by a direct write to this register, and the automatic update during DQS drift compensation can be disabled using the PHY General Configuration Register (PGCR). Every two bits of this register control the DQS gating for each of the (up to) four ranks. Valid values for each 2-bit RnDGPS field are:</p> <ul style="list-style-type: none"> 2'b00: 90 deg clock (clk90) 2'b01: 180 deg clock (clk180) 2'b10: 270 deg clock (clk270) 2'b11: 360 deg clock (clk0)
13:12	RW	0x2	<p>R0DGPS Rank 0 DQS Gating Phase Select Selects the clock used to enable the data strobes during read so that the value of the data strobes before and after the preamble/postamble are filtered out. The RnDGPS fields are initially set by the PUBL during automatic DQS data training and subsequently updated during data strobe drift compensation. However, these values can be overwritten by a direct write to this register, and the automatic update during DQS drift compensation can be disabled using the PHY General Configuration Register (PGCR). Every two bits of this register control the DQS gating for each of the (up to) four ranks. Valid values for each 2-bit RnDGPS field are:</p> <ul style="list-style-type: none"> 2'b00: 90 deg clock (clk90) 2'b01: 180 deg clock (clk180) 2'b10: 270 deg clock (clk270) 2'b11: 360 deg clock (clk0)
11:6	RO	0x0	reserved

Bit	Attr	Reset Value	Description
5:3	RW	0x0	<p>R1DGSL Rank 1 DQS Gating System Latency Used to increase the number of clock cycles needed to expect valid DDR read data by up to five extra clock cycles. This is used to compensate for board delays and other system delays. Power-up default is 000 (i.e. no extra clock cycles required). The SL fields are initially set by the PUBL during automatic DQS data training but these values can be overwritten by a direct write to this register. Every three bits of this register control the latency of each of the (up to) four ranks. Valid values are:</p> <ul style="list-style-type: none"> 3'b000: No extra clock cycles 3'b001: 1 extra clock cycle 3'b010: 2 extra clock cycles 3'b011: 3 extra clock cycles 3'b100: 4 extra clock cycles 3'b101: 5 extra clock cycles 3'b110: Reserved 3'b111: Reserved
2:0	RW	0x0	<p>R0DGSL Rank 0 DQS Gating System Latency Used to increase the number of clock cycles needed to expect valid DDR read data by up to five extra clock cycles. This is used to compensate for board delays and other system delays. Power-up default is 000 (i.e. no extra clock cycles required). The SL fields are initially set by the PUBL during automatic DQS data training but these values can be overwritten by a direct write to this register. Every three bits of this register control the latency of each of the (up to) four ranks. Valid values are:</p> <ul style="list-style-type: none"> 3'b000: No extra clock cycles 3'b001: 1 extra clock cycle 3'b010: 2 extra clock cycles 3'b011: 3 extra clock cycles 3'b100: 4 extra clock cycles 3'b101: 5 extra clock cycles 3'b110: Reserved 3'b111: Reserved

DDR_PUBL_DX3GCR

Address: Operational Base + offset (0x0280)

DATX8 3 General Configuration Register

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:20	RO	0x0	reserved
16:14 19:17	RW	0x3 0x3	<p>R0RVSL R1RVSL</p> <p>Rank n ITMD Read Valid System Latency Used to specify the read valid system latency relative to the ideal placement of the ITMD read valid signal when DXCCR.RVSEL is set to 0. Power-up default is 011 (i.e. ideal placement of the the read valid signal). The RVSL fields are initially set by the PUB during automatic read valid training but these values can be overwritten by a direct write to this register. Every three bits of this register control the latency of each rank. R0RVSL controls the latency of rank 0, R1RVSL controls rank 1. Valid values are:</p> <ul style="list-style-type: none"> 3'b000: read valid system latency = ideal placement - 3 3'b001: read valid system latency = ideal placement - 2 3'b010: read valid system latency = ideal placement - 1 3'b011: read valid system latency = ideal placement 3'b100: read valid system latency = ideal placement + 1 3'b101: read valid system latency = ideal placement + 2 3'b110: read valid system latency = ideal placement + 3 3'b111: Reserved
13	RW	0x0	<p>RTTOAL RTT On Additive Latency</p> <p>Indicates when the ODT control of DQ/DQS SSTL I/Os is set to the value in DQODT/DQSODT during read cycles.</p> <p>Valid values are:</p> <ul style="list-style-type: none"> 1'b0: ODT control is set to DQSODT/DQODT almost two cycles before read data preamble 1'b1: ODT control is set to DQSODT/DQODT almost one cycle before read data preamble
12:11	RW	0x0	<p>RTTOH RTT Output Hold</p> <p>Indicates the number of clock cycles (from 0 to 3) after the read data postamble for which ODT control should remain set to DQSODT for DQS or DQODT for DQ/DM before disabling it (setting it to '0' when using dynamic ODT control. ODT is disabled almost RTTOH clock cycles after the read postamble.</p>

Bit	Attr	Reset Value	Description
10	RW	0x1	DQRTT DQ Dynamic RTT Control Indicates, if set, that the ODT control of DQ/DM SSTL I/Os be dynamically controlled by setting it to the value in DQODT during reads and disabling it (setting it to '0' during any other cycle. If this bit is not set, then the ODT control of DQ SSTL I/Os is always set to the value in DQODT.
9	RW	0x1	DQSRTT DQS Dynamic RTT Control Indicates, if set, that the ODT control of DQS SSTL I/Os be dynamically controlled by setting it to the value in DQSODT during reads and disabling it (setting it to '0' during any other cycle. If this bit is not set, then the ODT control of DQS SSTL I/Os is always set to the value in DQSODT field.
8:7	RW	0x1	DSEN Write DQS Enable Controls whether the write DQS going to the SDRAM is enabled (toggling) or disabled (static value) and whether the DQS is inverted. DQS# is always the inversion of DQS. These values are valid only when DQS/DQS# output enable is on, otherwise the DQS/DQS# is tristated. Valid settings are: 2'b00: DQS disabled (Driven to constant 0) 2'b01: DQS toggling with inverted polarity 2'b10: DQS toggling with normal polarity (This should be the default setting) 2'b11: DQS disabled (Driven to constant 1)
6	RW	0x0	DQSRPD DQSR Power Down Powers down, if set, the PDQSR cell. This bit is ORed with the common PDR configuration bit.
5	RW	0x0	DXPDR Data Power Down Receiver Powers down, when set, the input receiver on I/O for DQ, DM, and DQS/DQS# pins of the byte. This bit is ORed with the common PDR configuration bit.
4	RW	0x0	DXPDD Data Power Down Driver Powers down, when set, the output driver on I/O for DQ, DM, and DQS/DQS# pins of the byte. This bit is ORed with the common PDD configuration bit.

Bit	Attr	Reset Value	Description
3	RW	0x0	DXIOM Data I/O Mode Selects SSTL mode (when set to 0) or CMOS mode (when set to 1) of the I/O for DQ, DM, and DQS/DQS# pins of the byte. This bit is ORed with the IOM configuration bit of the individual DATX8.
2	RW	0x0	DQODT Data On-Die Termination Enables, when set, the on-die termination on the I/O for DQ and DM pins of the byte. This bit is ORed with the common DATX8 ODT configuration bit.
1	RW	0x0	DQSODT DQS On-Die Termination Enables, when set, the on-die termination on the I/O for DQS/DQS# pin of the byte. This bit is ORed with the common DATX8 ODT configuration bit.
0	RW	0x1	DXEN Data Byte Enable Enables if set the DATX8 and SSTL I/Os used on the data byte. Setting this bit to '0' disables the byte, i.e. the byte SSTL I/Os are put in power-down mode and the DLL in the DATX8 is put in bypass mode.

DDR_PUBL_DX3GSR0

Address: Operational Base + offset (0x0284)

DATX8 3 General Status Register 0

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24:13	RO	0x000	DTPASS DQS Gate Training Pass Count The number of passing configurations during DQS gate training. Bits [2:0] are for rank 0, bits [5:3] for rank 1, and so on.
12	RO	0x0	reserved
11:8	RO	0x0	DTIERR DQS Gate Training Intermittent Error If set, indicates that there was an intermittent error during DQS gate training of the byte, such as a pass was followed by a fail then followed by another pass. Bit [0] is for rank 0, bit 1 for rank 1, and so on.

Bit	Attr	Reset Value	Description
7:4	RO	0x0	DTERR DQS Gate Training Error If set, indicates that a valid DQS gating window could not be found during DQS gate training of the byte. Bit [0] is for rank 0, bit 1 for rank 1, and so on.
3:0	RO	0x0	DTDONE Data Training Done Indicates, if set, that the byte has finished doing data training. Bit [0] is for rank 0, bit 1 for rank 1, and so on.

DDR_PUBL_DX3GSR1

Address: Operational Base + offset (0x0288)

DATX8 3 General Status Register 1

Bit	Attr	Reset Value	Description
31:20	RO	0x0	RVPASS Read Valid Training Pass Count The number of passing configurations during read valid training. Bits [2:0] are for rank 0, bits [5:3] for rank 1, and so on.
19:16	RO	0x0	RVIERR Read Valid Training Intermittent Error If set, indicates that there was an intermittent error during read valid training of the byte, such as a pass was followed by a fail then followed by another pass. Bit [0] is for rank 0, bit 1 for rank 1, and so on.
15:12	RO	0x0	RVERR Read Valid Training Error If set, indicates that a valid read valid placement could not be found during read valid training of the byte. Bit [0] is for rank 0, bit 1 for rank 1, and so on.
11:4	RO	0x00	DQSDFT DQS Drift Used to report the drift on the read data strobe of the data byte. Valid settings are: 2'b00: No drift 2'b01: 90 deg drift 2'b10: 180 deg drift 2'b11: 270 deg drift or more Bits [1:0] are for rank 0, bits [3:2] for rank 1, and so on.

Bit	Attr	Reset Value	Description
3:0	RO	0x0	DFTERR DQS Drift Error If set, indicates that the byte read data strobe has drifted by more than or equal to the drift limit set in the PHY General Configuration Register (PGCR). Bit [0] is for rank 0, bit 1 for rank 1, and so on.

DDR_PUBL_DX3DLLCR

Address: Operational Base + offset (0x028c)

DATX8 3 DLL Control Register

Bit	Attr	Reset Value	Description
31	RW	0x0	DLLDIS DLL Disable A disabled DLL is bypassed. Default ('0') is DLL enabled
30	RW	0x1	DLLSRST DLL Soft Rest Soft resets the byte DLL by driving the DLL soft reset pin
29:20	RO	0x0	reserved
19	RW	0x0	SDLBMODE Slave DLL Loopback Mode If this bit is set, the slave DLL is put in loopback mode in which there is no 90 degrees phase shift on read DQS/DQS#. This bit must be set when operating the byte PHYs in loopback mode such as during BIST loopback. Applicable only to PHYs that have this feature. Refer to PHY databook.
18	RW	0x0	ATESTEN Analog Test Enable Enables the analog test signal to be output on the DLL analog test output (test_out_a). The DLL analog test output is tri-stated when this bit is '0'.

Bit	Attr	Reset Value	Description
17:14	RW	0x0	<p>SDPHASE Slave DLL Phase Trim Selects the phase difference between the input clock and the corresponding output clock of the slave DLL. Valid settings:</p> <ul style="list-style-type: none"> 4'b0000: 90 4'b0001: 72 4'b0010: 54 4'b0011: 36 4'b0100: 108 4'b0101: 90 4'b0110: 72 4'b0111: 54 4'b1000: 126 4'b1001: 108 4'b1010: 90 4'b1011: 72 4'b1100: 144 4'b1101: 126 4'b1110: 108 4'b1111: 90
13:12	RW	0x0	<p>SSTART Slave Auto Start-Up Used to control how the slave DLL starts up relative to the master DLL locking:</p> <ul style="list-style-type: none"> 2'b0X: Slave DLL automatically starts up once the master DLL has achieved lock 2'b10: The automatic startup of the slave DLL is disabled; the phase detector is disabled 2'b11: The automatic startup of the slave DLL is disabled; the phase detector is enabled
11:9	RW	0x0	<p>MFWDLY Master Feed-Forward Delay Trim Used to trim the delay in the master DLL feed-forward path:</p> <ul style="list-style-type: none"> 3'b000: minimum delay 3'b111: maximum delay
8:6	RW	0x0	<p>MFBDLY Master Feed-Back Delay Trim Used to trim the delay in the master DLL feedback path:</p> <ul style="list-style-type: none"> 3'b000: minimum delay 3'b111: maximum delay

Bit	Attr	Reset Value	Description
5:3	RW	0x0	SFWDLY Slave Feed-Forward Delay Trim Used to trim the delay in the slave DLL feed-forward path: 3'b000: minimum delay 3'b111: maximum delay
2:0	RW	0x0	SFBDLY Slave Feed-Back Delay Trim Used to trim the delay in the slave DLL feedback path: 3'b000: minimum delay 3'b111: maximum delay

DDR_PUBL_DX3DQTR

Address: Operational Base + offset (0x0290)

DATX8 3 DQ Timing Register

Bit	Attr	Reset Value	Description
31:28	RW	0xf	DQDLY7 DQ7 Delay DQ Delay: Used to adjust the delay of the data relative to the nominal delay that is matched to the delay of the data strobes through the slave DLL and clock tree. Every four bits of this register control the delay of a different data bit in the byte. Used to adjust the delay of the data relative to the nominal delay that is matched to the delay of the data strobes through the slave DLL and clock tree. Every four bits of this register control the delay of a different data bit in the byte. The lower two bits of the DQDLY for each DQ bit controls the delay for the data clocked by DQS, while the higher two bits control the delay for the data clocked by DQS_b. Valid settings for each 2-bit control field are: 2'b00: nominal delay 2'b01: nominal delay + 1 step 2'b10: nominal delay + 2 steps 2'b11: nominal delay + 3 steps

Bit	Attr	Reset Value	Description
27:24	RW	0xf	<p>DQDLY6 DQ6 Delay Used to adjust the delay of the data relative to the nominal delay that is matched to the delay of the data strobes through the slave DLL and clock tree. Every four bits of this register control the delay of a different data bit in the byte.</p> <p>The lower two bits of the DQDLY for each DQ bit controls the delay for the data clocked by DQS, while the higher two bits control the delay for the data clocked by DQS_b. Valid settings for each 2-bit control field are:</p> <ul style="list-style-type: none"> 2'b00: nominal delay 2'b01: nominal delay + 1 step 2'b10: nominal delay + 2 steps 2'b11: nominal delay + 3 steps
23:20	RW	0xf	<p>DQDLY5 DQ5 Delay Used to adjust the delay of the data relative to the nominal delay that is matched to the delay of the data strobes through the slave DLL and clock tree. Every four bits of this register control the delay of a different data bit in the byte.</p> <p>The lower two bits of the DQDLY for each DQ bit controls the delay for the data clocked by DQS, while the higher two bits control the delay for the data clocked by DQS_b. Valid settings for each 2-bit control field are:</p> <ul style="list-style-type: none"> 2'b00: nominal delay 2'b01: nominal delay + 1 step 2'b10: nominal delay + 2 steps 2'b11: nominal delay + 3 steps

Bit	Attr	Reset Value	Description
19:16	RW	0xf	<p>DQDLY4 DQ4 Delay Used to adjust the delay of the data relative to the nominal delay that is matched to the delay of the data strobes through the slave DLL and clock tree. Every four bits of this register control the delay of a different data bit in the byte.</p> <p>The lower two bits of the DQDLY for each DQ bit controls the delay for the data clocked by DQS, while the higher two bits control the delay for the data clocked by DQS_b. Valid settings for each 2-bit control field are:</p> <ul style="list-style-type: none"> 2'b00: nominal delay 2'b01: nominal delay + 1 step 2'b10: nominal delay + 2 steps 2'b11: nominal delay + 3 steps
15:12	RW	0xf	<p>DQDLY3 DQ3 Delay Used to adjust the delay of the data relative to the nominal delay that is matched to the delay of the data strobes through the slave DLL and clock tree. Every four bits of this register control the delay of a different data bit in the byte.</p> <p>The lower two bits of the DQDLY for each DQ bit controls the delay for the data clocked by DQS, while the higher two bits control the delay for the data clocked by DQS_b. Valid settings for each 2-bit control field are:</p> <ul style="list-style-type: none"> 2'b00: nominal delay 2'b01: nominal delay + 1 step 2'b10: nominal delay + 2 steps 2'b11: nominal delay + 3 steps

Bit	Attr	Reset Value	Description
11:8	RW	0xf	<p>DQDLY2 DQ2 Delay Used to adjust the delay of the data relative to the nominal delay that is matched to the delay of the data strobes through the slave DLL and clock tree. Every four bits of this register control the delay of a different data bit in the byte.</p> <p>The lower two bits of the DQDLY for each DQ bit controls the delay for the data clocked by DQS, while the higher two bits control the delay for the data clocked by DQS_b. Valid settings for each 2-bit control field are:</p> <ul style="list-style-type: none"> 2'b00: nominal delay 2'b01: nominal delay + 1 step 2'b10: nominal delay + 2 steps 2'b11: nominal delay + 3 steps
7:4	RW	0xf	<p>DQDLY1 DQ1 Delay Used to adjust the delay of the data relative to the nominal delay that is matched to the delay of the data strobes through the slave DLL and clock tree. Every four bits of this register control the delay of a different data bit in the byte.</p> <p>The lower two bits of the DQDLY for each DQ bit controls the delay for the data clocked by DQS, while the higher two bits control the delay for the data clocked by DQS_b. Valid settings for each 2-bit control field are:</p> <ul style="list-style-type: none"> 2'b00: nominal delay 2'b01: nominal delay + 1 step 2'b10: nominal delay + 2 steps 2'b11: nominal delay + 3 steps

Bit	Attr	Reset Value	Description
3:0	RW	0xf	<p>DQDLY0 DQ0 Delay Used to adjust the delay of the data relative to the nominal delay that is matched to the delay of the data strobes through the slave DLL and clock tree. Every four bits of this register control the delay of a different data bit in the byte.</p> <p>The lower two bits of the DQDLY for each DQ bit controls the delay for the data clocked by DQS, while the higher two bits control the delay for the data clocked by DQS_b. Valid settings for each 2-bit control field are:</p> <ul style="list-style-type: none"> 2'b00: nominal delay 2'b01: nominal delay + 1 step 2'b10: nominal delay + 2 steps 2'b11: nominal delay + 3 steps

DDR_PUBL_DX3DQSTR

Address: Operational Base + offset (0x0294)

DATX8 3 DQS Timing Register

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:26	RW	0xf	<p>DMDLY DM Delay Used to adjust the delay of the data mask relative to the nominal delay that is matched to the delay of the data strobes through the slave DLL and clock tree. The lower two bits of the DQMDLY controls the delay for the data clocked by DQS, while the higher two bits control the delay for the data clocked by DQS_b.</p> <p>Valid settings for each 2-bit control field are:</p> <ul style="list-style-type: none"> 2'b00: nominal delay 2'b01: nominal delay + 1 step 2'b10: nominal delay + 2 steps 2'b11: nominal delay + 3 steps

Bit	Attr	Reset Value	Description
25:23	RW	0x3	<p>DQSNDLY DQS# Delay Used to adjust the delay of the data strobes relative to the nominal delay that is matched to the delay of the data bit through the slave DLL and clock tree. DQSDLY control the delay on DQS strobe and DQSNDLY control the delay on DQS#. Valid values are:</p> <ul style="list-style-type: none"> 3'b000: nominal delay - 3 steps 3'b001: nominal delay - 2 steps 3'b010: nominal delay - 1 step 3'b011: nominal delay 3'b100: nominal delay + 1 step 3'b101: nominal delay + 2 steps 3'b110: nominal delay + 3 steps 3'b111: nominal delay + 4 steps
22:20	RW	0x3	<p>DQSDLY DQS Delay Used to adjust the delay of the data strobes relative to the nominal delay that is matched to the delay of the data bit through the slave DLL and clock tree. DQSDLY control the delay on DQS strobe and DQSNDLY control the delay on DQS#. Valid values are:</p> <ul style="list-style-type: none"> 3'b000: nominal delay - 3 steps 3'b001: nominal delay - 2 steps 3'b010: nominal delay - 1 step 3'b011: nominal delay 3'b100: nominal delay + 1 step 3'b101: nominal delay + 2 steps 3'b110: nominal delay + 3 steps 3'b111: nominal delay + 4 steps
19:16	RO	0x0	reserved

Bit	Attr	Reset Value	Description
15:14	RW	0x2	<p>R1DGPS Rank 1 DQS Gating Phase Select Selects the clock used to enable the data strobes during read so that the value of the data strobes before and after the preamble/postamble are filtered out. The RnDGPS fields are initially set by the PUBL during automatic DQS data training and subsequently updated during data strobe drift compensation. However, these values can be overwritten by a direct write to this register, and the automatic update during DQS drift compensation can be disabled using the PHY General Configuration Register (PGCR). Every two bits of this register control the DQS gating for each of the (up to) four ranks. Valid values for each 2-bit RnDGPS field are:</p> <ul style="list-style-type: none"> 2'b00: 90 deg clock (clk90) 2'b01: 180 deg clock (clk180) 2'b10: 270 deg clock (clk270) 2'b11: 360 deg clock (clk0)
13:12	RW	0x2	<p>R0DGPS Rank 0 DQS Gating Phase Select Selects the clock used to enable the data strobes during read so that the value of the data strobes before and after the preamble/postamble are filtered out. The RnDGPS fields are initially set by the PUBL during automatic DQS data training and subsequently updated during data strobe drift compensation. However, these values can be overwritten by a direct write to this register, and the automatic update during DQS drift compensation can be disabled using the PHY General Configuration Register (PGCR). Every two bits of this register control the DQS gating for each of the (up to) four ranks. Valid values for each 2-bit RnDGPS field are:</p> <ul style="list-style-type: none"> 2'b00: 90 deg clock (clk90) 2'b01: 180 deg clock (clk180) 2'b10: 270 deg clock (clk270) 2'b11: 360 deg clock (clk0)
11:6	RO	0x0	reserved

Bit	Attr	Reset Value	Description
5:3	RW	0x0	<p>R1DGSL Rank 1 DQS Gating System Latency Used to increase the number of clock cycles needed to expect valid DDR read data by up to five extra clock cycles. This is used to compensate for board delays and other system delays. Power-up default is 000 (i.e. no extra clock cycles required). The SL fields are initially set by the PUBL during automatic DQS data training but these values can be overwritten by a direct write to this register. Every three bits of this register control the latency of each of the (up to) four ranks. Valid values are:</p> <ul style="list-style-type: none"> 3'b000: No extra clock cycles 3'b001: 1 extra clock cycle 3'b010: 2 extra clock cycles 3'b011: 3 extra clock cycles 3'b100: 4 extra clock cycles 3'b101: 5 extra clock cycles 3'b110: Reserved 3'b111: Reserved
2:0	RW	0x0	<p>R0DGSL Rank 0 DQS Gating System Latency Used to increase the number of clock cycles needed to expect valid DDR read data by up to five extra clock cycles. This is used to compensate for board delays and other system delays. Power-up default is 000 (i.e. no extra clock cycles required). The SL fields are initially set by the PUBL during automatic DQS data training but these values can be overwritten by a direct write to this register. Every three bits of this register control the latency of each of the (up to) four ranks. Valid values are:</p> <ul style="list-style-type: none"> 3'b000: No extra clock cycles 3'b001: 1 extra clock cycle 3'b010: 2 extra clock cycles 3'b011: 3 extra clock cycles 3'b100: 4 extra clock cycles 3'b101: 5 extra clock cycles 3'b110: Reserved 3'b111: Reserved

5.6 Interface description

DDR IOs for each channel are listed as following Table.

Pin Name	Description
CK	Active-high clock signal to the memory device.
CK_B	Active-low clock signal to the memory device.
CKE _i (i=0,1)	Active-high clock enable signal to the memory device for two chip select.
CS_B _i (i=0,1)	Active-low chip select signal to the memory device. ATThere are two chip select.
RAS_B	Active-low row address strobe to the memory device.
CAS_B	Active-low column address strobe to the memory device.
WE_B	Active-low write enable strobe to the memory device.
BA[2:0]	Bank address signal to the memory device.
A[15:0]	Address signal to the memory device.
DQ[31:0]	Bidirectional data line to the memory device.
DQS[3:0]	Active-high bidirectional data strobes to the memory device.
DQS_B[3:0]	Active-low bidirectional data strobes to the memory device.
DM[3:0]	Active-low data mask signal to the memory device.
ODT _i (i=0,1)	On-Die Termination output signal for two chip select.
RET_EN	Active-low retention latch enable input.
VREF _i (i=0,1,2)	Reference Voltage input for three regions of DDR IO.
ZQ_PIN	ZQ calibration pad which connects 240ohm±1% resistor.
RESET	DDR3 reset signal.

5.7 Application Notes

5.7.1 State transition of PCTL

To operate PCTL, the programmer must be familiar with the available operational states and how to transition to each state from the current state.

Every software programmable register is accessible only during certain operational states. For information about what registers are accessible in each state, refer to "Software Registers," which provides this information in each register description. The general rule is that the PCTL must be in the Init_mem or Config states to successfully write most of the registers.

The following tables provide the programming sequences for moving to the various states of the state machine.

Moving to the Init_mem State

Step	Application	PCTL
1	Read STAT register	Returns the current PCTL state.
2	If STATctl_stat = Init_mem, go to END.	
3	If STATctl_stat =Config, go to Step9.	
4	If STATctl_stat =Access, go to Step8.	
5	If STATctl_stat = Low_power, go to Step7.	
6	Goto Step1.	PCTL is in a Transitional state and not in any of the previous operational states.
7	Write WAKEUP to SCTL.state_cmd and poll STATctl_stat= Access.	Issues SRX, moves to the Access state, updates STATctl_stat =Access when complete.

Step	Application	PCTL
8	Write CFG to SCTL.state_cmd and poll STAT.ctl_stat= Config.	PCTL stalls the NIF; completes any pending transaction; issues PREA if required; moves into the Config state; updates STAT.ctl_stat =Config whencomplete.
9	Write INIT to SCTL.state_cmd and poll STAT.ctl_stat=Init_mem	Moves into the Init_mem state and updates STAT.ctl_stat =Init_mem.
END		PCTL is in Init_mem state.

Moving to Config State

Step	Application	PCTL
1	Read STAT register.	Returns the current PCTL state.
2	If STAT.ctl_stat= Config, goto END.	
3	If STAT.ctl_stat= Low_power, go toStep6.	
4	If STAT.ctl_stat= Init_mem or Access, go toStep7.	
5	Go to Step1.	PCTL is in a transitional state and is not in any of the previous operational states.
6	Write WAKEUP to CTL.state_cmd and poll STAT.ctl_stat= Access.	Issues SRX, moves to the Access state, and updates STAT.ctl_stat= Access when complete.
7	Write CFG to SCTL.state_cmd and poll STAT.ctl_stat= Config.	PCTL stalls the NIF; completes any pending transaction; issues PREA if required; moves into the Config state; and updates STAT.ctl_stat = Config when complete.
END		PCTL is in Config state.

Moving to Access State

Step	Application	PCTL
1	Read STATregister	Returns the current PCTL state.
2	IfSTAT.ctl_stat= Access, go to END.	
3	IfSTAT.ctl_stat= Config, go to Step9	
4	IfSTAT.ctl_stat= Init_mem, go to Step8	
5	IfSTAT.ctl_stat= Low_power, go to Step7.	
6	Goto Step1.	PCTL is in a transitional state and is not in any of the previous operational states.
7	Write WAKEUP to SCTL.state_cmd and poll STAT.ctl_stat= Access. Goto END	Issues SRX, moves to the Access state, updates STAT.ctl_stat= Access when complete.
8	Write CFG to SCTL.state_cmd and poll STAT.ctl_stat= Config.	Moves into the Config state, updates STAT.ctl_stat= Config when complete.
9	Write GO to SCTL.state_cmd and poll STAT.ctl_stat= Access.	Moves into the Access state, updates STAT.ctl_stat= Access when complete.
END		PCTL is in Access state.

Moving to Low Power State

Step	Application	PCTL
1	Read STAT register.	Returns current PCTL state.
2	If STATctl_stat =Low_power, go to END.	
3	If STATctl_stat = Access, go to Step9	
4	If STATctl_stat = Config, go to Step8	
5	If STATctl_stat = Init_mem, go to Step7.	
6	Goto Step1.	PCTL is in transitional state and is not in any of the previous operational states.
7	Write CFG to SCTL.state_cmd and poll STATctl_stat= Config.	Moves into the Config state, updates STATctl_stat = Config when complete.
8	Write GO to SCTL.state_cmd and poll STATctl_stat= Access.	Moves into the Access state, updates STATctl_stat =Access when complete.
9	Write SLEEP to SCTL.state_cmd and poll STATctl_stat= Low_power.	Issues PDX if necessary; completes any pending transactions; issues PREA command; finally, issues SRE and updates STATctl_stat = Low_power.
END		PCTL is in Low Power state

5.7.2 Initialization

Figure 1-14 shows a high-level illustration of the initialization sequence of the PHY. A detailed sequence description and timing diagrams are described in the following. This section assumes a generic configuration port and therefore cfg_clk and cfg_rst_n are shown as the configuration clock and reset, respectively. These signals must be replaced by pclk and presetn if the design is compiled to use the APB configuration port.

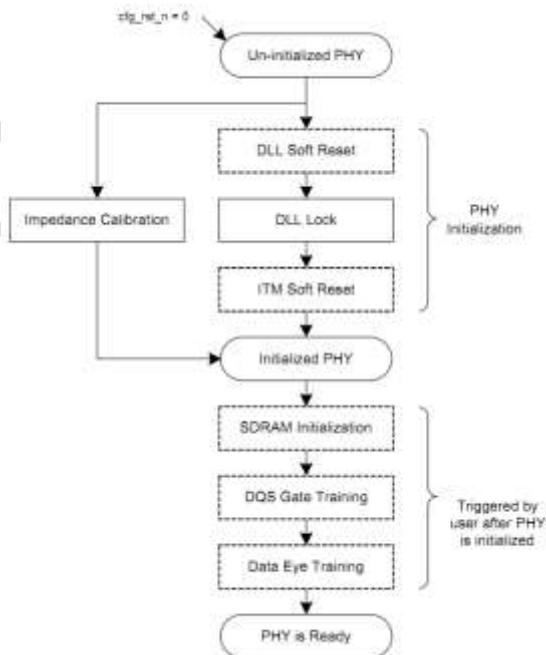


Fig. 5-10 Protocol controller architecture

PHY Initialization

The initialization sequence has two phases. The first phase happens automatically at reset and is as follows:

1. Before and during configuration reset (i.e. if cfg_rst_n is asserted), the PHY is un-initialized and remains in this state until the reset is de-asserted.
 2. At reset de-assertion, the PHY moves into the DLL initialization (lock) phase. This phase may be bypassed at any time by writing a '1' to the DLL initialization bypass register bit (PIR[LOCKBYP]).
 3. In parallel to DLL initialization, the impedance calibration phase also starts at reset de-assertion.
- This phase can also be bypassed by writing a '1' to the impedance calibration bypass register bit-PIR[ZCALBYP].
4. If the PHY initialization sequence was triggered by the user, a soft reset may optionally be selected to be issued to the ITMs. Initialization that is automatically triggered on reset does not issue a soft reset to the ITMs because the components will already have been reset by the main reset.
 5. Once the DLL initialization and impedance calibration phases are done and after the ITMs are reset, the PHY is initialized. Note that if these phases were bypassed, it is up to the user to perform them in software or trigger them at a later time before the PHY can be used.

SDRAM Initialization

The second phase of initialization starts after the PHY is initialized. Each step of this phase is triggered by the user or memory controller and is as follows:

1. Prior to normal operation, DDR SDRAMs must be initialized. The PHYCTL has a built-in SDRAM initialization routine that may be triggered by software or memory controller by writing to the PHY Initialization Register (PIR). The initialization routine built into the PHYCTL is generic and does not require any knowledge of the type or configuration of external SDRAMs to be properly executed. The routine is designed with the relevant JEDEC specifications for the fastest & slowest SDRAMs supported by the PHYCTL to result in a universal initialization sequence. This generic sequence is applicable to DDR3, DDR2, LPDDR2, LPDDR, and DDR SDRAMs.

It is recommended to use the built-in PHYCTL routine to initialize the SDRAM. However, there may be cases such as during system debug when the built-in PHYCTL DRAM initialization is not triggered and DRAM initialization is performed by software or the controller. In these cases the system must first wait for the PHY to initialize, i.e. DLL locked and impedance calibration done, then it must write a '1' to PIR[INIT] bit with PIR[CTLDINT] set to '1' (for controller initialization) or '0' (for software or PHYCTL initialization) to inform the PHYCTL that DRAM initialization will be done later, by software, the controller or by re-triggering on the PHYCTL. The software or controller then executes the initialization sequence by sending relevant commands to the DRAM, respecting the various timing requirements of the initialization sequence.

2. After the SDRAM is initialized, the user or memory controller performs, or triggers the PHYCTL to perform DQS gate training ("Built-in DQS Gate Training" on page 114). The SDRAM must be initialized before triggering DQS gate training.
3. The user or memory controller performs, or triggers the PHYCTL to perform read data eye training. Note that the current version of the PHYCTL does not have the read eye training designed in.
4. The PHY is now ready for SDRAM read/write accesses.

DDR3 Initialization Sequence

The initialization steps for DDR3 SDRAMs are as follows:

1. Optionally maintain RESET# low for a minimum of either 200 us (power-up initialization) or 100ns (power-on initialization). The PHYCTL drives RESET# low from the beginning of reset assertion and therefore this step may be skipped when DRAM initialization is triggered if enough time may already have expired to satisfy the RESET# low time.
2. After RESET# is de-asserted, wait a minimum of 500 us with CKE low.
3. Apply NOP and drive CKE high.
4. Wait a minimum of tXPR.
5. Issue a load Mode Register 2 (MR2) command.

6. Issue a load Mode Register 3 (MR3) command.
7. Issue a load Mode Register (MR1) command (to set parameters and enable DLL).
8. Issue a load Mode Register (MR0) command to set parameters and reset DLL.
9. Issue ZQ calibration command.
10. Wait 512 SDRAM clock cycles for the DLL to lock (tDLLK) and ZQ calibration (tZQinit) to finish. This wait time is relative to Step 8, i.e. relative to when the DLL reset command was issued onto the SDRAM command bus.

LPDDR2 Initialization Sequence

The initialization steps for LPDDR2 SDRAMs are as follows:

1. Wait a minimum of 100 ns (tINIT1) with CKE driven low.
2. Apply NOP and set CKE high.
3. Wait a minimum of 200 us (tINIT3).
4. Issue a RESET command.
5. Wait a minimum of 1 us + 10 us (tINIT4 + tINIT5).
6. Issue a ZQ calibration command.
7. Wait a minimum of 1 us (tZQINIT).
8. Issue a Write Mode Register to MR1.
9. Issue a Write Mode Register to MR2
10. Issue a Write Mode Register to MR3

Initialization Triggered and bypass

All initialization steps shown in Figure 3-1 on page 34 can be triggered using the PHY Initialization Register (PIR) as described in "PHY Initialization Register (PIR)" on page 47. Writing a '1' to PIR[INIT] register bit will start initialization, with the routines to be run being selected by the corresponding PIR register bits. If multiple routines are selected, they are run in the order shown in Figure 3-1 on page 34. This is also the order of the select bits in PIR register. The completion of the routines is indicated in the PHY General Status Register (PGSR) with the corresponding done status bits (see "PHY General Status Register (PGSR)" on page 52). The PGSR[IDONE] bit indicates the overall completion of the initialization sequence. An initialization done status register bit is cleared (reset to '0') when the corresponding routine is re-triggered.

The de-assertion of reset will automatically trigger the PHYCTL to perform DLL initialization (locking) and impedance calibration. Once the DLL has locked and impedance calibration has completed, the SDRAM initialization and DQS gating may be triggered or performed by software or memory controller.

Since the PHYCTL allows the selection of individual routines to be run when initialization is triggered using PIR register, only those routines that automatically trigger on reset de-assertion have individual bypass capability. This means that DLL locking and/or impedance calibration may be bypassed any time by writing a '1' to the corresponding bypass register bit in the PIR register. Once a routine is bypassed, it is internally registered as completed and the corresponding done status register bit is set in the PGSR register.

It is up to the user to re-trigger or perform the bypassed routine at a later time before the PHY can be used. The PIR[INITBYP] register bit provides the option to bypass the whole initialization sequence.

5.7.3 MDLL and MSDLL Reset Requirements

Reset issued to the MDLL and MSDLL must always meet the following requirements:

1. Reset must always be asserted for a minimum of 50ns to ensure proper reset of the DLL.
2. On power-up, reset must be held for a minimum of 50ns after MVDD has been raised to its full value.
3. After reset has been asserted and then de-asserted, a number of clock cycles must pass for the DLL to achieve lock.
4. The input clock to the DLL must be stable for a minimum of 50ns before DLL reset is de-asserted.

The following additional requirements apply when transitioning to/from bypass mode:

1. There must be at least 50ns between reset de-assertion and DLL bypass mode entry.
2. The DLL bypass pin must be asserted for at least 1000ns.
3. Reset must always be issued after the DLL mode has changed from bypass to normal mode.
4. A minimum of 100ns is required between bypass de-assertion and reset assertion.
5. Reset must be issued whenever DLL control/trim/option input bits are modified, with the exception of:

- a. Analog/digital test controls
- b. Slave DLL phase trim (if applicable).

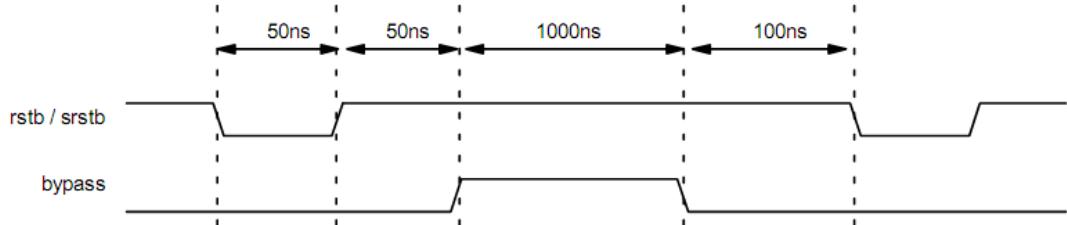


Fig. 5-11 DLL reset requirements

5.7.4 Data Training

Built-in DQS Gate Training

The PHYCTL has a built-in DQS gate training routine that may be triggered by software or memory controller using the PIR register.

DQS gate training returns a number of status, including the done and error status. There are two types of errors. The first type is when no valid window was found for the byte. This is indicated by DTERR register bit in DXnGSR and PGSR registers. This is usually an indication of bad configuration. The second type is when some passing configurations were found but these were interspersed by failures. This is not expected in a working system. A typical window is signified by consecutive passes followed by consecutive failures, e.g. FPPPPP and not FPPFPP. This type of error is called an intermittent error and is indicated by the DTIERR register bit in DXnGSR and PGSR registers. Provided for debug purpose is the status of how many passing configurations were found for each byte on each rank. This is indicated by DTPASS field in the DXnGSR register.

Software DQS Gate Training

DQS gate training may also be executed in software using the controller and/or the PUB DCU. Figure 13-16 shows the DQS gate training software algorithm. This is followed by a description of the main phases of the training.

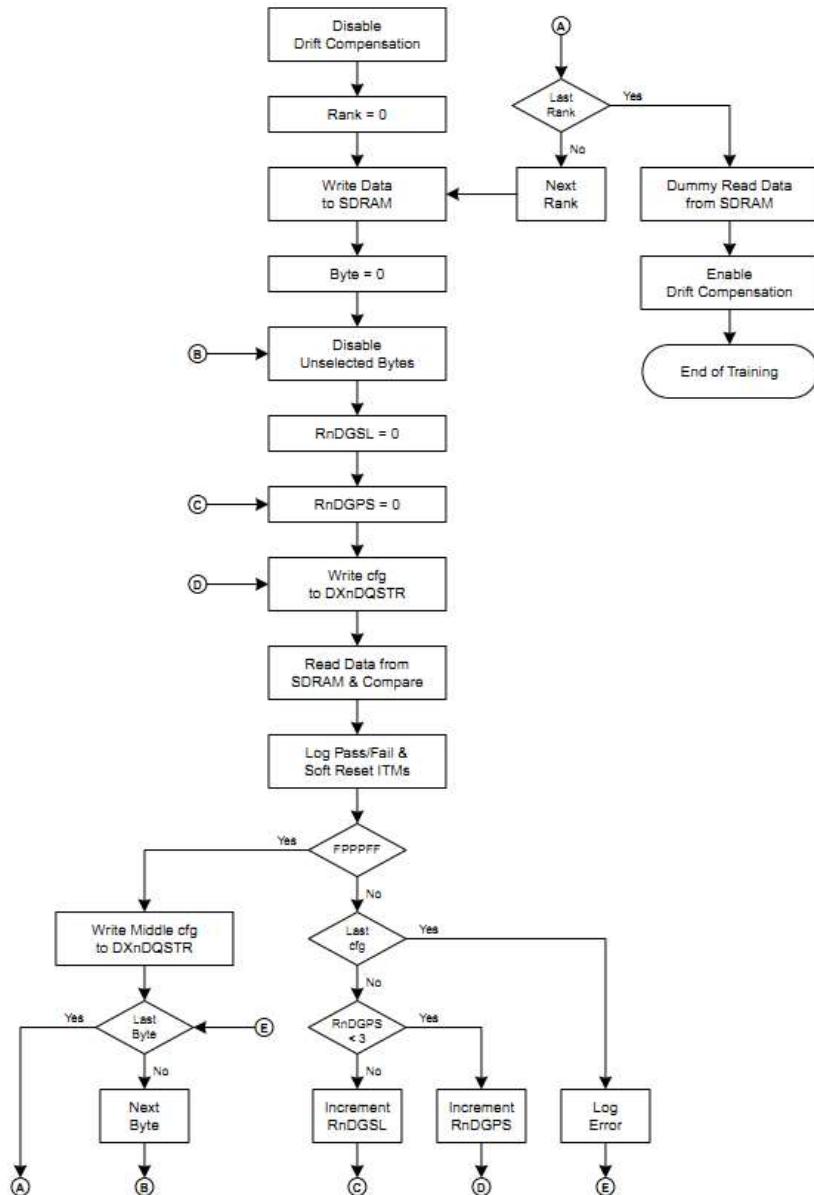


Fig. 5-12 DLL reset requirements

The software DQS gate training phases are as follows:

1. Disable drift compensation by writing '0' to PGCR.DFTCMP register.
2. Start with rank 0, i.e. rank 0 is selected for training.
3. Execute a minimum of two writes to the SDRAM. Any type of data and any SDRAM address can be used for DQS gate training. It is however not recommended to use data that is all zeroes since this may mask read data comparison. The data mask must be set to 0 to enable writing of all bytes. The number of writes must be chosen such that it results in a minimum of eight data beats at the SDRAM. This means at least two write commands when using SDRAM burst length of 4.
4. Start with byte 0 (i.e. byte 0 is selected for training).
5. Disable all the other bytes except the byte that has been selected for training. Bytes are enabled/disabled by writing 1/0 to DXnDGCR.DXEN.
6. Start with the selected rank byte DQS gating system latency (DXnDQSTR.RnDGSL) of 0.
7. Start with the selected rank byte DQS gating phase select (DXnDQSTR.RnDGPS) of 0.
8. Write the selected DQS gating configurations (RnDGSL and RnDGPS) to DXnDQSTR register of the selected byte, making sure the fields for the unselected ranks remain unchanged.
9. Execute reads from the SDRAM locations previously written. The number of reads must be equal to the number of writes used in Step 3. Compare the read data with the expected (written) data and log the pass/fail status as a sequence or history of flags for each trained

RnDGSL/RnDGPS configuration (e.g. FFPPPPFF). A fail is either when there is a data miscompare or when fewer data than expected is returned. Note that a controller that is designed to always wait for the correct number of read data may need a time-out in case the trained configuration results in fewer data than expected. This is not an issue when using the PUB DCU because it does not wait for the expected number of reads; rather the read count status will indicate if fewer reads were returned.

10. Once the read data has been compared and the pass/fail status logged, issue an ITM soft reset to clear the status of the read data logic in the PHY. This is important because the ITM read data FIFO pointers may be in the wrong state at the end of training an RnDGSL/RnDGPS configuration that resulted in wrong DQS gating window.

11. If two consecutive fails and some passes exist, then this is the end of the training for this rank byte. In this case, do the following:

Select the middle of the passes and write the values to the corresponding fields of DXnDQSTR register, making sure the fields for the unselected ranks remain unchanged
If this is not the last byte, then select the next byte and go to Step 5
If this is the last byte but not the last rank, then select the next rank and go to Step 3
If this is the last byte and the last rank, then go to Step 12 to do final clean-up before the end of the DQS gate training.

If the condition of two consecutive fails and some passes does not exist, then this signals that more RnDGSL/RnDGPS configurations need to be trained for this rank byte. If this is the case, do the following:

if RnDGPS is less than 3, then increment RnDGPS and go to Step 8
if RnDGPS is equal to 3 but RnDGSL is less than 7, then increment RnDGSL and go to Step 7
if RnDGPS is equal to 3 and RnDGSL is equal to 7, then log an error because this is a signal that something in the system is very wrong such that no passing configuration is possible for this rank byte. With such an error condition, you can either terminate the whole training to investigate the system or you can go to train the next byte.

12. Once the training of all ranks and all bytes is finished, issue one or more dummy reads to the same SDRAM locations. This will flush out the DQS drift compensation logic in the PHY and therefore avoid reporting any false drift events caused by previous DQS gating settings.

13. Once the dummy reads have completed, re-enable drift compensation by writing 1 to PGCR.DFTCMP register. This is the end of DQS gate training. Regular memory operations can now commence.

5.7.5 Impedance Calibration

The impedance calibration circuit, which controls the impedance values for ODT and driver output impedance, consists of the following components:

- ZQ calibration cell - PZQ
- External RZQ precision resistor
- Impedance control logic - zctrl
- VREF cell (for code encoding and level shifting)
- Functional I/O cells

The connectivity of these components is shown as follow figure:

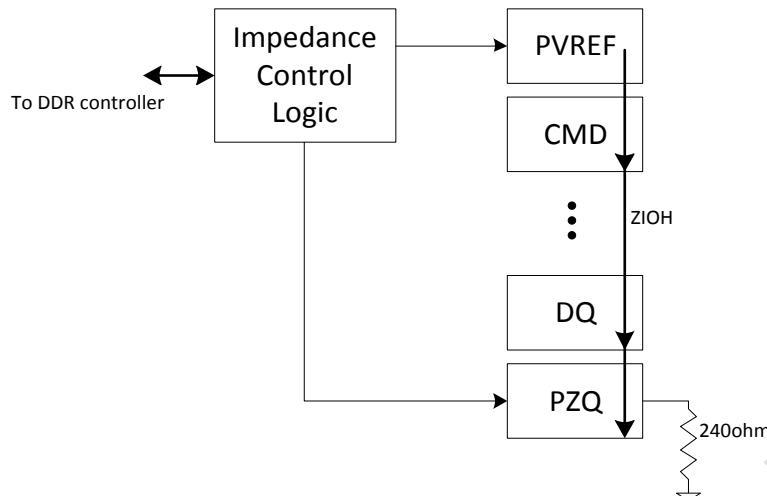


Fig. 5-13 Impedance Calibration Circuit

A single calibration cell (PZQ) is used for the interface. The user connects the PZQ pin through an external $240\text{ohm}\pm1\%$ resistor to ground. One or multiple VREF cells exist in the interface, depending on the total data width of the interface. The ZCTRL bus from the impedance control logic is connected to all VREF cells in the interface. It is not permitted to have a VREF cell in the interface that is not connected to the impedance control logic.

The impedance control logic sends an impedance code through the ZCTRL bus to the VREF cells. The VREF cells encode this data, level shifts it to the VDDQ power domain, and sends it to both the functional I/O cells and the PZQ cell through the ZIOH bus embedded within the SSTL cells. The PZQ cell also receives the desired divide ratios from the Memory Controller or the user logic. The PZQ cell compares the impedance control code received from the PVREF cell with the external resistor, taking into account the selected divide ratio. The PZQ cell then sends ZCOMP back to the impedance control logic to relay information about impedance matching. The impedance control logic then sends a new impedance code to the PVREF cells. This results in a closed-loop system.

The four impedance elements are calibrated sequentially:

- Pull-up termination impedance
- Pull-down termination impedance
- Pull-up output impedance
- Pull-down output impedance

The ZPROG bus is used to signal which element is being calibrated. The state machine is implemented on the Impedance Controller RTL block.

The impedance control logic connects to the Memory Controller or customer logic to allow full controllability and observability of the loop operation.

The impedance control loop operates with a low bandwidth as compared to the memory system, thus the impedance control logic contains a clock divider to permit operation at a reduced clock frequency.

There are three basic modes of operation:

- Direct Calibration - uses ZPROG settings.
- Override Setting - uses ctrl_ovrd_data settings.
- Custom Calibration - extends calibration beyond the values available on ZPROG

Direct Calibration

In this mode, the user is setting independently the value for ODT (ZPROG[7:4]) and Output Impedance (ZPROG[3:0]) and runs the calibration sequence:

1. Output impedance pulldown
2. Output impedance pull-up
3. On-Die termination (ODT) pull-down
4. ODT pull-up

Override Setting

In this mode, the user is not using the calibration loop, and instead directly controls the impedance control using zctrl_ovrd_data[19:0] bus, which is parsed in four nibbles that independently control driver pull-down/up and ODT pull-down/up impedance in 31 steps. For example, assuming one step is associated to current I and the calibration voltage is VREF, the programmed impedance for index N is:

$$Z_{PROG} = K * VREF / (N * I)$$

K is correction factor, which is approximately equal to 1. Based on the formula, it can be concluded that if index N is increased, then the impedance is decreased.

Custom Calibration

This mode is a two-step procedure combining the previous two modes.

1. The user provides a Direct Calibration using a convenient value and records the Impedance control results from status register.

2. The user applies the correction factor that provides the custom impedance.

The following example assumes that it is required to program Driver Output Impedance to 18 ohms.

1. The user performs a Direct Calibration for driver $Z_o=36$ ohms. For example, assume the result shows that Driver pull-up index is 12, and Driver pull-down index is 13.

2. Calculate and apply the Override Data for 18 ohm impedance adjustment as follows:

$$(<\text{cal_value}>/<\text{req_value}>) * <\text{cal_index}>$$

$$\text{Driver pull-down } (36/18) * 13 = 26$$

$$\text{Driver pull-up } (36/18) * 12 = 24$$

5.7.6 Retention Functional

The purpose of the retention function is to retain a known state on the signals to the SDRAMs while the system is placed in a low power mode, specifically when the core VDD supply is powered down. The general concept is that an external input signal (RET_EN) is driven low to put the SSTL I/O cells into retention mode shortly before the core VDD supply is powered down. The user must set the SSTL I/O outputs in the state required during power down before asserting RET_EN. This ensures that the output state of all SSTL I/Os are held static in the desired state while core VDD is power down. After core VDD is restored, the user must re-initialize the core logic to a known state before de-asserting the RET_EN signal. Following figure provides the I/O cell arrangement with retention.

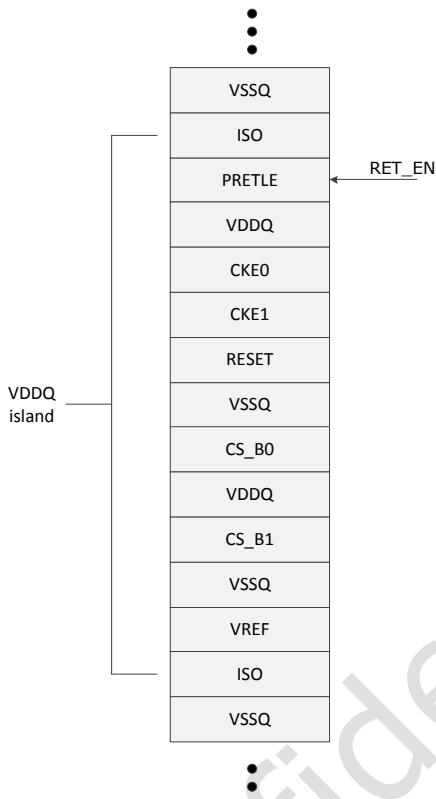


Fig. 5-14 I/O cell arrangement with retention

IOs between two ISO is a VDDQ island, they will maintain power on when other IOs are powered down by RET_EN active.

Following figure provides a sequence of events to enter and exit retention.

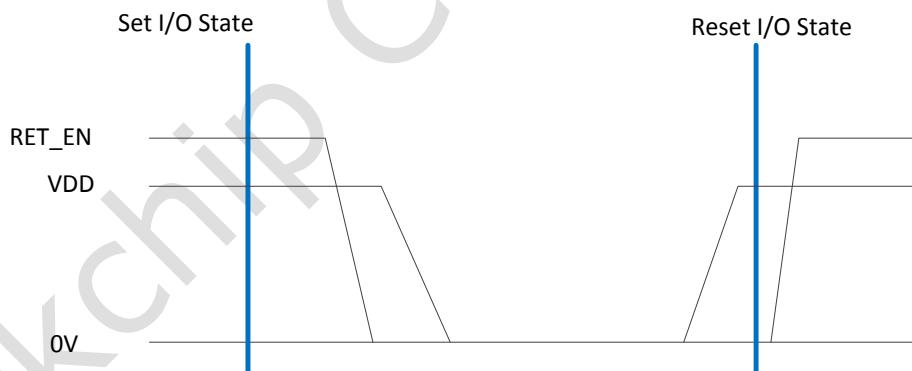


Fig. 5-15 Sequence of Events to Enter and Exit Retention

CKE Retention Mode

An alternative CKE retention mode is supported. This scheme works by placing the SDRAMs into self-refresh mode and then driving the CKE signal low. Core VDD and VDDQ can then both be powered down except for a small VDDQ island supplying the CKE output cell. Two of the special 5um spacer cells ISO are used to break the VDDQ rail in order to create a separate CKE VDDQ island, which is kept powered while core VDD and the main VDDQ are powered down. The sequence of events is as follows:

1. Enter self-refresh mode using the Self-Refresh Command
2. Set CKE low
3. Stop CK/CKB
4. Assert RET_EN (low)
5. Power-Off
6. Power-On
7. After reset is released, execute initialization

8. De-assert RET_EN (high)
9. Start CK/CKB
10. Set CKE high
11. Exit self-refresh mode

5.7.7 Low Power Operation

Low_power state can be entered/exited via following ways:

- Software control of PCTL State machine (highest priority)
- Hardware Low Power Interface (middle priority)
- Auto Self Refresh feature (lowest priority)

Note the priority of requests from Access to Low_power is highlighted above. The STAT.ip_trig register field reports which of the 3 requests caused the entry to Low_power state.

Software control of PCTL State

The application can request via software to enter the memories into Self Refresh state by issuing the SLEEP command by programming SCTL.PCTL responds to the software request by moving into the Low_power operational state and issuing the SRE command to the memories. Note that the Low_power state can only be reached from the Access state.

In a similar fashion, the application requests to exit the memories from Self Refresh by issuing a WAKEUP command by programming SCTL.. PCTL responds to the WAKEUP command issuing SRX and restoring normal NIF address channel operation.

Hardware Low Power Interface

The hardware low power interface can also be used to enter/exit Self Refresh. The functionality is enabled by setting SCFG.hw_low_power_en=1. Once that bit is set, the input c_sysreq has the ability to trigger entry into the Low Power configuration state just like the software methodology (SCTL.state_cmd = SLEEP). A hardware Low Power entry trigger will be ignored/denied if the input c_active_in=1 or n_valid=1. It may be accepted if c_active_in=0 and n_valid=0, depending on the current state of the PCTL. When SCFG.hw_low_power_en=1, the outputs c_sysack and c_active provide feedback as required by the AXI low power interface specification (this interface's operation is defined by the AXI specification). c_sysack acknowledges the request to go into the Low_power state, and c_active indicates when the PCTL is actually in the Low_power state.

The c_active output could also be used by an external Low Power controller to decide when to request a transition to low power. When MCFG1.hw_idle > 0, c_active = 1'b0 indicates that the NIF has been idle for at least MCFG1.hw_idle * 32 * n_clk cycles while in the Access state. When in low power the c_active output can be used by an external Low Power controller to trigger a low power exit. c_active will be driven high when either c_active_in or n_valid are high. The path from c_active_in and n_valid to c_active is asynchronous so even if the clocks have been removed c_active will assert. The Low Power controller should re-enable the clocks when c_active is driven high while in the Low_power state.

Auto Clock Stop/Power Down/Self Refresh

The Clock Stop and/or Power Down and/or Self Refresh sequence is automatically started by PCTL when the NIF address channel is idle for a number of cycles, depending on the programmed value in MCFG.mddr_lpddr2_clkstop_idle and MCFG.pd_idle and MCFG1.sr_idle. Following table outlines the effect of these settings in conjunction with NIF being idle.

mddr_lpddr2_clkstop_idle	pd_idle	sr_idle	Memory modes	Memory Type
0	0	0	none	All
>0	0	0	Clock Stop	mDDR/LPDDR2 only
0	>0	0	Power Down	All
>0	>0	0	Clock Stop -> Power Down®	mDDR/LPDDR2 only
0	0	>0	Self Refresh	All

mddr_lpddr2_clkstop_idle	pd_idle	sr_idle	Memory modes	Memory Type
>0	0	>0	Clock Stop -> Self Refresh ^②	mDDR/LPDDR2 only
0	>0	>0	Power Down -> Self Refresh ^③	All
>0	>0	>0	Clock Stop -> Power Down -> Self Refresh ^④	mDDR/LPDDR2 only

Note:

①: Clock Stop is entered if NIF is idle for mddr_lpddr2_clkstop_idle. Following on from that, if NIF continues to be idle for a further pd_idle cycles, Clock Stop is exited and Power Down is entered.

②: Clock Stop is entered if NIF is idle for mddr_lpddr2_clkstop_idle. Following on from that, if NIF continues to be idle for a further sr_idle*32 cycles, Clock Stop is exited and Self Refresh is entered.

③: Power Down is entered if NIF is idle for pd_idle. Following on from that, if NIF continues to be idle for a further sr_idle*32 cycles, Power Down is exited and Self Refresh is entered.

④: Clock Stop is entered if NIF is idle for mddr_lpddr2_clkstop_idle. Following on from that, if NIF continues to be idle for a further pd_idle cycles, Clock Stop is exited and Power Down is entered. Following on from that, if NIF continues to be idle for a further sr_idle*32 cycles, Power Down is exited and Self Refresh is entered.

Removing PCTL's n_clk

In LPDDR2 and DDR3, the relationship between SRE/SRX and stopping/starting the memory clock (CK) are formalized and are accounted for automatically by PCTL. With LPDDR2 and DDR3, CK should only be stopped after PCTL has reached the Low_power state. The current operational state can be verified by reading STAT.ctl_stat. The CK must be started and stable before the Software or Hardware Low Power Interface attempts to take the memory out of Self Refresh.

PCTL's n_clk can be safely removed when PCTL is in Low Power state. The sequences outlined in following table should be followed for safe operation:

Step	Application	PCTL
1	Write SLEEP to SCTL.state_cmd and poll STAT.ctl_stat = LOW_POWER.	Tells PCTL to move memories into Self Refresh and waits until this completes.
2	Write TREFI=0. Also, write DFITCRLUPDI=0 and DFIREFMSKI=0, if they are not already 0.	Stops any MC-driven DFI updates occurring internally with PCTL
3	Wait a minimum interval which is equivalent to the PCTL's Refresh Interval (previous value of TREFI*TOGCNT100N*internal timers clock period;	Ensures any already scheduled PHY/PVT updates have completed successfully.
4	Stop toggling n_clk to PCTL.	n_clk logic inside PCTL is stopped.
end		

Step	Application	PCTL
1	Drive c_active_in low	Confirms that system external to PCTL can accept a Low-power request
2	Drive c_sysreq low	System Low-power request
3	Wait for PCTL to drive c_sysack low	PCTL Low-power request acknowledgement
4	Check value of c_active when Step 3 occurs. - if c_active=1, request denied. Cannot remove n_clk. Go to END. - if c_active=0, request accepted.	PCTL low-power request status response
5	Stop toggling n_clk to PCTL	n_clk logic inside PCTL is stopped

end		
-----	--	--

Deep Power-Down

Compared with DDR2/DDR3, mDDR and LPDDR2 has an additional low power mode (Deep Power Down) :

Software-driven Deep Power Down Entry – on reception of DPDE from the application, PCTL drives CKE low for TDPD.t_dpd. After TDPD, MCMD.start_cmd will be cleared to 1'b0. The following are recommended values for TDPD:

mDDR: TDPD=0

LPDDR2: dependent on if the system wants to immediately power off the PCTL after Deep Power down is entered:

If PCTL not Powered off: TDPD=500μs

Else if PCTL is Powered off: TDPD=0 - up to higher level system to meet tDPD requirement.

To Exit Deep Power Mode, full initialization of the memories must be performed.

5.7.8 PHY Power Down

The PHYCTL includes several registers for putting certain components of the PHY in power down mode. The PHTCTL also supports DFI-initiated power-down of its components using the DFI low-power protocol.

Several components of the PHY can be powered down using PHYCTL registers. There are separate power-down register bits for the address/command lane and for each byte lane. Also there are separate controls for powering down the I/Os versus powering down the DLL. Following table describes the registers that are used to power down various components of the PHY.

Register Name	Bit Field	Description
PIR	DLLBYP	Bypasses, and hence disables or powers down all PHY DLLs.
ACDLLCR	DLLDIS	Disables (powers down) the address/command lane DLL
ACIOCR	ACPDD	Powers down the output drivers for address/command lane signal I/Os. Different groups of signals have dedicated driver power-down control registers to allow finer selection of signals to power down, especially that some signals, such as CKE and RST#, are required to remain powered up when the SDRAM is in self-refresh mode. Each rank CS# signal and each CK/CK# pair has dedicated driver power down control registers, with the other rank-specific signals (CKE and ODT) of each rank being controlled by separate power down control registers in a separate PUB register (DSGCR). There is also a dedicated driver power down control register for SDRAM reset signal. However, the rest of the signals going to the SDRAM (address, bank address, RAS#, CAS#, WE#, and PAR_IN) share a common driver power down register just dedicated for this group. The LPDDR TPD signal has a dedicated output driver power down control register in a separate PUB register (DSGCR).
ACIOCR	ACPDR	Powers down the input receivers for address/command lane signal I/Os. Different groups of signals have dedicated receiver power-down control registers to allow finer selection of signals to power down. Each rank and each CK/CK# pair has dedicated receiver power down control register, with all rank-specific signals (CKE, ODT, and CS#) of each rank sharing a common, but rank-specific, receiver power down control register. There is also a dedicated receiver power down control register for SDRAM reset pins. However, the rest of the signals going to the SDRAM (address, bank address, RAS#, CAS#, WE#, PAR_IN, TPD) share a common receiver power down register just dedicated for this group.
DXCCR	DXPDD	Powers down the output drivers for DQ, DM, and DQS/DQS# signal I/Os of all byte lanes. This is a convenient way of powering down the output drivers of all byte lane I/Os with just a single register write. In addition to this, each byte has a dedicated output driver power-down register control to allow only selected bytes to be powered down.
DXCCR	DXPDR	Powers down the input receivers for DQ, DM, and DQS/DQS# signal I/Os of all byte lanes. It also powers down the PDQSR cells of all bytes.

Register Name	Bit Field	Description
		This is a convenient way of powering down the input receivers of all byte lane I/Os with just a single register write. In addition to this, each byte has a dedicated input receiver power-down register control to allow only selected bytes to be powered down.
DSGCR	CKEPDD	Powers down the output drivers for CKE I/Os. Each rank CKE has a dedicated driver power down control register to allow finer control of CKE I/O driver power-down, especially that the CKE I/O driver of an SDRAM that is in self refresh is required to remain powered up.
DSGCR	ODTPDD	Powers down the output drivers for ODT I/Os. Each rank ODT has a dedicated driver power down control register to allow finer control of ODT I/O driver power-down, especially that the ODT I/O driver of an SDRAM that is in self refresh or power down mode may be required in certain DDR modes to remain powered up.
DSGCR	TPDPD	Powers down the output driver for the optional LPDDR TPD signal I/O.
DSGCR	NL2PD	Powers down the output driver and the input receiver on the I/O for non-LPDDR2 signals (ODT, RAS#, CAS#, WE#, and BA). This may be used when a chip that is designed for both LPDDR2 and other DDR modes is being used in LPDDR2 mode, in which case one may want to power down the unused I/Os. This power down control register is in addition to (ORed with) the individual ACIOCR power down control registers for these signals.
ZQnCRO	ZQPD	Powers down the PZQ cell. Each PZQ has a dedicated power down control register.
DXnDLLCR	DLLDIS	Disables (powers down) the byte lane DLL. Each byte lane has a dedicated DLL power down control register.
DXnGCR	DXPDD	Powers down the output drivers for DQ, DM, and DQS/DQS# signal I/Os of the byte lane. Each byte lane has a dedicated output driver power down control register, in conjunction with the global output driver power down control register DXCCR.DXPDD.
DXnGCR	DXPDR	Powers down the input receivers for DQ, DM, and DQS/DQS# signal I/Os of the byte lane. Each byte lane has a dedicated input receiver power down control register, in conjunction with the global input receiver power down control register DXCCR.DXPDR
DXnGCR	DQSRPD	Powers down the PDQSR cells of the byte lane. Each byte lane has a dedicated PDQSR power down control register, in conjunction with the global PDQSR power down control register DXCCR.DXPDR.
PGCR	PDDISDX	Selects whether the I/Os and DLL of a disabled byte should automatically be powered down by the PUB. A byte can be disabled by writing a '0' to the DXnGCR.DXEN register or by using the DFI data byte disable (dfi_data_byte_disable) signal.
DSGCR	LPIOPD	Specifies whether the PHY should respond to the controller-initiated DFI low power opportunity request and power down the I/Os of the PHY.
DSGCR	LPDLLPD	Specifies whether the PHY should respond to the controller-initiated DFI low power opportunity request and power down the DLL of the PHY if the requested wakeup time is greater than 2048 clock cycles

DFI-Initiated Power-Down

There are two ways how the controller can initiate PHY power down through the DFI interface. The first method is when the controller asserts the DFI data byte disable (dfi_data_byte_disable) signal during initialization when the DFI initialization start (dfi_init_start) signal is high. In this state, the PHY will power down the DLL and I/Os of the selected bytes if it is configured through DSGCR.BDISEN to respond to DFI data byte disable and if disabled bytes are configured through PGCR.PDDISDX to be powered down. The DFI data byte disable feature is normally used as a static configuration to disable bytes that are not being used.

The controller can also initiate PHY power down by using the DFI low power control interface. This is a dynamic low power request-acknowledge protocol that the controller may use to put the PHY into low power mode when it is not being used for a prolonged time. The PHY will acknowledge a low power request from the controller and power down I/Os and DLLs if it is configured to do so through DSGCR.LPIOPD and DSGCR.LPDLLPD. If the low power wakeup time requested by the controller is less than 2048 clock cycles, then only the I/Os will be

powered down. Otherwise if the wakeup time is equal to or more than 2048 cycles, then the DLLs and the I/Os are all powered down. If the DLLs are powered down, then on low power wakeup the PUB will soft reset the DLLs and wait for them to lock before acknowledging the low power wakeup request to the controller.

5.7.9 Dynamic ODT for I/Os

By default the DFI turns on the ODT for the PHY I/Os for DQ/DQS# only when there is read data coming back. This is called dynamic ODT control and is used to reduce power consumed by the termination resistors. The DFI uses the timing of the DQS gating to accurately place the PHY I/O ODT enable signal around the read data. Typically, the DFI turns on the byte ODT enable signal 2 clocks before the pre-amble and turns it off one clock after the post-amble. This guarantees correct setup and hold on the I/Os.

The PHY ODT signal does not go through the ITMs and therefore has to fan out to the DQ/DQS from RTL logic in the PHYCTL. This may result in different timing on these signals depending on the routing. For this reason various programmable features are provided on the ODT control signals to help mitigate some of the timing issues that may result from different implementations. These are described in the DXnGCR register. In summary, both the starting position and the width of the enable signal can be adjusted relative to the default position and lengths.

Chapter 6 Nand Flash Controller(NandC)

6.1 Overview

Nand Flash Controller (NandC) is used to control data transmission from host to flash device or from flash device to host. NandC is connected to AHB BUS through an AHB Master and an AHB Slave. The data transmission between host and external memory can be done through AHB Master interface or AHB Slave interface.

NandC supports the following features:

- NandC AHB bus clock (hclk) is asynchronous to NandC working clock (nclk)
- Software Interface Type
 - Support directly mode
 - Support LLP(Linked List Pointer) mode
- Flash Interface Type
 - Support Asynchronous Flash Interface with 8bits datawidth ("Asyn8x" for short)
 - Support Asynchronous Flash Interface with 16bits data width ("Asyn16x" for short)
 - Support ONFI Synchronous Flash Interface ("ONFI Syn" for short)
 - Support Toggle Flash Interface ("Toggle" for short)
 - Support 8 flash devices at most
- Flash Type
 - Support Managed NAND Flash(LBA) and Raw NAND Flash(NO-LBA)
 - Support SLC/MLC/TLC Flash
- Flash Interface Timing
 - Asyn8x: configurable timing, one byte per two Nandc working clocks at the fastest speed
 - Asyn16x: configurable timing, two bytes per two Nandc working clocks at the fastest speed
 - ONFI Syn: configurable timing, two bytes per two Nandc working clocks at the fastest speed
 - Toggle: configurable timing, two byte per two Nandc working clocks at the fastest speed
- Randomizer Ability
 - Support three randomizer mode with different polynomial
 - Support two randomizer width, 8bit and 16bit parallel
- BCH/ECC Ability
 - 16bit/1KB BCH/ECC: support 16bitBCH/ECC, which can detect and correct up to 16 error bits in every 1K bytes data
 - 24bit/1KB BCH/ECC: support 24bitBCH/ECC, which can detect and correct up to 24 error bits in every 1K bytes data
 - 40bit/1KB BCH/ECC: support 40bitBCH/ECC, which can detect and correct up to 40 error bits in every 1K bytes data
 - 60bit/1KB BCH/ECC: support 60bitBCH/ECC, which can detect and correct up to 60 error bits in every 1K bytes data
 - 8bit/512B BCH/ECC: support 8bitBCH/ECC, which can detect and correct up to 8 error bits in every 512 bytes data
 - 12bit/512B BCH/ECC: support 12bitBCH/ECC, which can detect and correct up to 12 error bits in every 512 bytes data
 - 20bit/512B BCH/ECC: support 20bitBCH/ECC, which can detect and correct up to 20 error bits in every 512 bytes data
 - 30bit/512B BCH/ECC: support 30bitBCH/ECC, which can detect and correct up to 30 error bits in every 512 bytes data
 - 16bit/512B BCH/ECC: support 16bitBCH/ECC, which can detect and correct up to 16 error bits in every 512 bytes data
 - 24bit/512B BCH/ECC: support 24bitBCH/ECC, which can detect and correct up to 24

- error bits in every 512 bytes data
- 40bit/512B BCH/ECC: support 40bitBCH/ECC, which can detect and correct up to 40 error bits in every 512 bytes data
- 60bit/512B BCH/ECC: support 60bitBCH/ECC, which can detect and correct up to 60 error bits in every 512 bytes data
- Transmission Ability
 - Support 32K bytes data transmission at a time at most
 - Support two transfer working modes: Bypass or DMA
 - Support two transfer codeword size for Managed NAND Flash: 1024 bytes/codeword or 512 bytes/codeword
- Internal Memory
 - 2 built-in srams, and the size is 1k bytes respectively
 - Can be accessed by other masters
 - Can be operated in pingpong mode by other masters

6.2 Block Diagram

NandC comprises with:

- MIF: AHB Master Interface
- SIF : AHB Slave Interface
- SRIF : Sram Interface
- TRANSC : Transfer Controller
- LLPC : LLP Controller
- BCHENC : BCH Encoder
- BCHDEC : BCH Decoder
- RANDMZ : Randomizer
- FIF_GEN : Flash Interface Generation
- DLC : Delay Line Controller

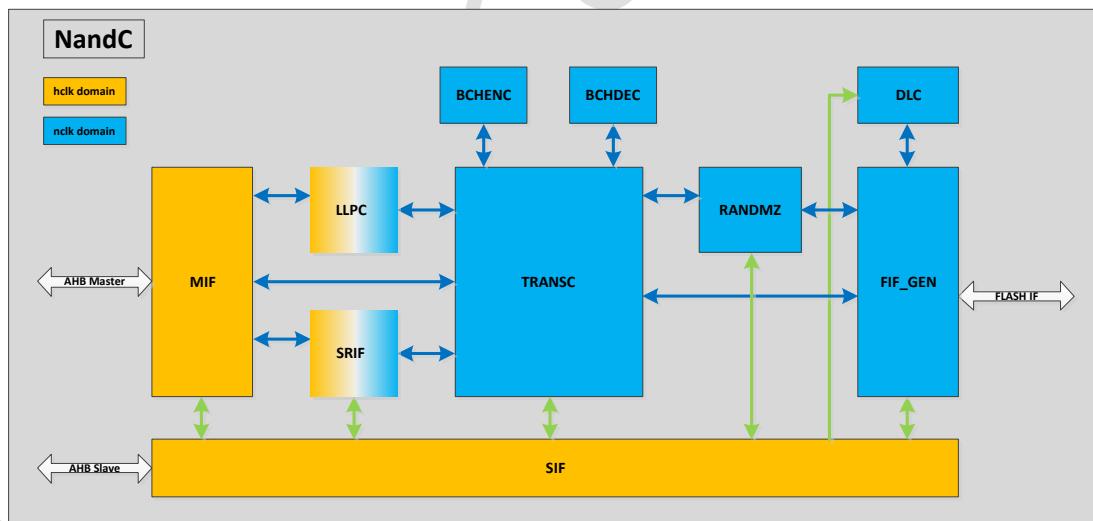


Fig. 6-1 NandC Block Diagram

6.3 Function Description

6.3.1 AHB Interface

There is an AHB master interface in NandC, which is selectable and configurable. It is responsible for transferring data from external memory to internal memory when flash program, or inverse when flash read; and transferring LLP data from external memory to internal register file when LLP is active.

There is an AHB slave interface in NandC. It is responsible for accessing registers and internal

memories. The addresses of these registers and memories are listed in "Internal Address Mapping" section.

6.3.2 Flash Type/Flash Interface

Flash device with different types of interfaces is supported. These interfaces include: asynchronous 8bits flash interface, asynchronous 16bits flash interface, ONFI synchronous flash interface, toggle flash interface, and so on. You can select one of them by software (configure FMCTL) to suit for these devices. Also you can configure their timing parameters by software (configure FMWAIT_ASYN/FMWAIT_SYN) to have your desired rate.

6.3.3 Linked List Pointer Mode (LLP)

To save the software resource and improve the performance, a LLP is add, which is selectable. When LLP is selected, the flash operation instructions stored in external memory with specific format should be loaded for flash working. The detailed format and working flow are referred to "LLP Application" section.

6.3.4 BCH Encoder/BCH Decoder

The BCH Encoder is responsible for encoding data to be written into flash device. The max encoded length is 1133bytes, in which the data length is 1024bytes, system information is 4bytes, BCH code is 105bytes.

The BCH Decoder is responsible for decoding data read from flash device. The max decoded length is 1133bytes, in which the data length is 1024bytes, spare length is 109bytes.

6.3.5 Randomizer

To improve device lifetime, a randomizer is added in NandC. It includes two parts: Scrambler and Descrambler, which is responsible for scrambling data to be written into flash after bch encoding, and descrambling data read from flash before bch decoding.

6.3.6 Delay Line Controller

For ONFI Synchronous Flash or Toggle Flash, the data read from flash follows with a strobe signal: DQS, where a skew between them exists. To remove the skew and improve the timing between data and DQS, a Delay Line Controller is needed. It is responsible for detecting the phase of the signal similar to DQS, determining the element number to be shifted, and then shifting the DQS with the determined number.

6.4 Register Description

6.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

Table 6-1 NandC Address Mapping

Base Address[12:8]	Device	Address Length	Offset Address Range
5'b00_00x(x=0, 1)	FLR	512 BYTE	0x0000 ~ 0x01ff
5'b00_01x(x=0, 1)	SPR	512 BYTE	0x0200 ~ 0x03ff
5'b00_10x(x=0, 1)	FLR1	512 BYTE	0x0400 ~ 0x05ff
5'b00_11x(x=0,1)	FLR2	512 BYTE	0x0600 ~ 0x07ff
5'b01_000	Flash0	256 BYTE	0x0800 ~ 0x08ff
5'b01_001	Flash1	256 BYTE	0x0900 ~ 0x09ff

Base Address[12:8]	Device	Address Length	Offset Address Range
5'b01_010	Flash2	256 BYTE	0x0a00 ~ 0x0aff
5'b01_011	Flash3	256 BYTE	0x0b00 ~ 0xbfff
5'b01_100	Flash4	256 BYTE	0x0c00 ~ 0xcfff
5'b01_101	Flash5	256 BYTE	0x0d00 ~ 0xdfff
5'b01_110	Flash6	256 BYTE	0x0e00 ~ 0xefff
5'b01_111	Flash7	256 BYTE	0x0f00 ~ 0xffff
5'b10_0xx(x=0, 1)	Sram0	1K BYTE	0x1000 ~ 0x13ff
5'b10_1xx(x=0, 1)	Sram1	1K BYTE	0x1400 ~ 0x17ff

6.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
NANDC_FMCTL	0x0000	W	0x000000200	Flash Interface Control Register
NANDC_FMWAIT_ASYN	0x0004	W	0x3f03f7ff	Flash Timing Control Register For Asynchronous Timing
NANDC_FLCTL	0x0008	W	0x00100000	Internal Transfer Control Register
NANDC_BCHCTL	0x000c	W	0x00000008	BCH Control Register
NANDC_MTRANS_CFG	0x0010	W	0x0000001d0	Bus Transfer Configuration Register
NANDC_MTRANS_SAD_DR0	0x0014	W	0x000000000	Start Address Register For Page Data Transmission
NANDC_MTRANS_SAD_DR1	0x0018	W	0x000000000	Start Address Register For Spare Data Transmission
NANDC_MTRANS_STAT	0x001c	W	0x000000000	Bus Transfer Status Register
NANDC_BCHST0	0x0020	W	0x040000000	BCH Status Register For Codeword 0~1
NANDC_BCHST1	0x0024	W	0x000000000	BCH Status Register For Codeword 2~3
NANDC_BCHST2	0x0028	W	0x000000000	BCH Status Register For Codeword 4~5
NANDC_BCHST3	0x002c	W	0x000000000	BCH Status Register For Codeword 6~7
NANDC_BCHST4	0x0030	W	0x000000000	BCH Status Register For Codeword 8~9
NANDC_BCHST5	0x0034	W	0x000000000	BCH Status Register For Codeword 10~11
NANDC_BCHST6	0x0038	W	0x000000000	BCH Status Register For Codeword 12~13
NANDC_BCHST7	0x003c	W	0x000000000	BCH Status Register For Codeword 14~15
NANDC_BCHLOC0	0x0040	W	0x000000000	BCH Error Bit Location Number Register For Codeword 0~5
NANDC_BCHLOC1	0x0044	W	0x000000000	BCH Error Bit Location Number Register For Codeword 6~11
NANDC_BCHLOC2	0x0048	W	0x000000000	BCH Error Bit Location Number Register For Codeword 12~17
NANDC_BCHLOC3	0x004c	W	0x000000000	BCH Error Bit Location Number Register For Codeword 24~29
NANDC_BCHLOC4	0x0050	W	0x000000000	BCH Error Bit Location Number Register For Codeword 24~29

Name	Offset	Size	Reset Value	Description
NANDC_BCHLOC5	0x0054	W	0x00000000	BCH Error Bit Location Number Register For Codeword 30~31
NANDC_BCHLOC6	0x0058	W	0x00000000	Highest Bit For BCH Error Bit Location Number Register
NANDC_BCHDE0_0	0x0070	W	0x00000000	BCH decode result of 0th error bit for codeword 0
NANDC_BCHDE0_1	0x0074	W	0x00000000	BCH decode result of 1th error bit for codeword 0
NANDC_BCHDE0_2	0x0078	W	0x00000000	BCH decode result of 2th error bit for codeword 0
NANDC_BCHDE0_3	0x007c	W	0x00000000	BCH decode result of 3th error bit for codeword 0
NANDC_BCHDE0_4	0x0080	W	0x00000000	BCH decode result of 4th error bit for codeword 0
NANDC_BCHDE0_5	0x0084	W	0x00000000	BCH decode result of 5th error bit for codeword 0
NANDC_BCHDE0_6	0x0088	W	0x00000000	BCH decode result of 6th error bit for codeword 0
NANDC_BCHDE0_7	0x008c	W	0x00000000	BCH decode result of 7th error bit for codeword 0
NANDC_BCHDE0_8	0x0090	W	0x00000000	BCH decode result of 8th error bit for codeword 0
NANDC_BCHDE0_9	0x0094	W	0x00000000	BCH decode result of 9th error bit for codeword 0
NANDC_BCHDE0_10	0x0098	W	0x00000000	BCH decode result of 10th error bit for codeword 0
NANDC_BCHDE0_11	0x009c	W	0x00000000	BCH decode result of 11th error bit for codeword 0
NANDC_BCHDE0_12	0x00a0	W	0x00000000	BCH decode result of 12th error bit for codeword 0
NANDC_BCHDE0_13	0x00a4	W	0x00000000	BCH decode result of 13th error bit for codeword 0
NANDC_BCHDE0_14	0x00a8	W	0x00000000	BCH decode result of 14th error bit for codeword 0
NANDC_BCHDE0_15	0x00ac	W	0x00000000	BCH decode result of 15th error bit for codeword 0
NANDC_BCHDE0_16	0x00b0	W	0x00000000	BCH decode result of 16th error bit for codeword 0
NANDC_BCHDE0_17	0x00b4	W	0x00000000	BCH decode result of 17th error bit for codeword 0
NANDC_BCHDE0_18	0x00b8	W	0x00000000	BCH decode result of 18th error bit for codeword 0

Name	Offset	Size	Reset Value	Description
NANDC_BCHDE0_19	0x00bc	W	0x00000000	BCH decode result of 19th error bit for codeword 0
NANDC_BCHDE0_20	0x00c0	W	0x00000000	BCH decode result of 20th error bit for codeword 0
NANDC_BCHDE0_21	0x00c4	W	0x00000000	BCH decode result of 21th error bit for codeword 0
NANDC_BCHDE0_22	0x00c8	W	0x00000000	BCH decode result of 22th error bit for codeword 0
NANDC_BCHDE0_23	0x00cc	W	0x00000000	BCH decode result of 23th error bit for codeword 0
NANDC_BCHDE1_0	0x00d0	W	0x00000000	BCH decode result of 0th error bit for codeword 1
NANDC_BCHDE1_1	0x00d4	W	0x00000000	BCH decode result of 1th error bit for codeword 1
NANDC_BCHDE1_2	0x00d8	W	0x00000000	BCH decode result of 2th error bit for codeword 1
NANDC_BCHDE1_3	0x00dc	W	0x00000000	BCH decode result of 3th error bit for codeword 1
NANDC_BCHDE1_4	0x00e0	W	0x00000000	BCH decode result of 4th error bit for codeword 1
NANDC_BCHDE1_5	0x00e4	W	0x00000000	BCH decode result of 5th error bit for codeword 1
NANDC_BCHDE1_6	0x00e8	W	0x00000000	BCH decode result of 6th error bit for codeword 1
NANDC_BCHDE1_7	0x00ec	W	0x00000000	BCH decode result of 7th error bit for codeword 1
NANDC_BCHDE1_8	0x00f0	W	0x00000000	BCH decode result of 8th error bit for codeword 1
NANDC_BCHDE1_9	0x00f4	W	0x00000000	BCH decode result of 9th error bit for codeword 1
NANDC_BCHDE1_10	0x00f8	W	0x00000000	BCH decode result of 10th error bit for codeword 1
NANDC_BCHDE1_11	0x00fc	W	0x00000000	BCH decode result of 11th error bit for codeword 1
NANDC_BCHDE1_12	0x0100	W	0x00000000	BCH decode result of 12th error bit for codeword 1
NANDC_BCHDE1_13	0x0104	W	0x00000000	BCH decode result of 13th error bit for codeword 1
NANDC_BCHDE1_14	0x0108	W	0x00000000	BCH decode result of 14th error bit for codeword 1
NANDC_BCHDE1_15	0x010c	W	0x00000000	BCH decode result of 15th error bit for codeword 1

Name	Offset	Size	Reset Value	Description
NANDC_BCHDE1_16	0x0110	W	0x00000000	BCH decode result of 16th error bit for codeword 1
NANDC_BCHDE1_17	0x0114	W	0x00000000	BCH decode result of 17th error bit for codeword 1
NANDC_BCHDE1_18	0x0118	W	0x00000000	BCH decode result of 1th error bit for codeword 1
NANDC_BCHDE1_19	0x011c	W	0x00000000	BCH decode result of 19th error bit for codeword 1
NANDC_BCHDE1_20	0x0120	W	0x00000000	BCH decode result of 20th error bit for codeword 1
NANDC_BCHDE1_21	0x0124	W	0x00000000	BCH decode result of 21th error bit for codeword 1
NANDC_BCHDE1_22	0x0128	W	0x00000000	BCH decode result of 22th error bit for codeword 1
NANDC_BCHDE1_23	0x012c	W	0x00000000	BCH decode result of 23th error bit for codeword 1
NANDC_DLL_CTL_REG_0	0x0130	W	0x007f7f05	DLL Control Register 0
NANDC_DLL_CTL_REG_1	0x0134	W	0x00000022	DLL Control Register 1
NANDC_DLL_OBS_REG_0	0x0138	W	0x00000200	DLL Status Register
NANDC_RANDMZ_CFG	0x0150	W	0x00000000	Randomizer Configure Register
NANDC_FMWAIT_SYN	0x0158	W	0x00000000	Flash Timing Control Register For Synchronous Timing
NANDC_MTRANS_STAT_2	0x015c	W	0x00000000	Bus Transfer Status Register2
NANDC_NANDC_VER	0x0160	W	0x56363232	Nandc Version Register
NANDC_LLP_CTL	0x0164	W	0x00000000	LLP Control Register
NANDC_LLP_STAT	0x0168	W	0x00000001	LLP Status Register
NANDC_INTEN	0x016c	W	0x00000000	NandC Interrupt Enable Register
NANDC_INTCLR	0x0170	W	0x00000000	NandC Interrupt Clear Register
NANDC_INTST	0x0174	W	0x00000000	NandC Interrupt Status Register
NANDC_SPARE0_0	0x0200	W	0xffffffff	System Information for codeword 0
NANDC_SPARE0_1	0x0204	W	0x00000000	Spare Data and BCH Encode Information for codeword 0
NANDC_SPARE0_2	0x0208	W	0x00000000	Spare Data and BCH Encode Information for codeword 0
NANDC_SPARE0_3	0x020c	W	0x00000000	Spare Data and BCH Encode Information for codeword 0
NANDC_SPARE0_4	0x0210	W	0x00000000	Spare Data and BCH Encode Information for codeword 0

Name	Offset	Size	Reset Value	Description
NANDC_SPARE0_5	0x0214	W	0x00000000	Spare Data and BCH Encode Information for codeword 0
NANDC_SPARE0_6	0x0218	W	0x00000000	Spare Data and BCH Encode Information for codeword 0
NANDC_SPARE0_7	0x021c	W	0x00000000	Spare Data and BCH Encode Information for codeword 0
NANDC_SPARE0_8	0x0220	W	0x00000000	Spare Data and BCH Encode Information for codeword 0
NANDC_SPARE0_9	0x0224	W	0x00000000	Spare Data and BCH Encode Information for codeword 0
NANDC_SPARE0_10	0x0228	W	0x00000000	Spare Data and BCH Encode Information for codeword 0
NANDC_SPARE0_11	0x022c	W	0x00000000	Spare Data and BCH Encode Information for codeword 0
NANDC_SPARE1_0	0x0230	W	0xffffffff	System Information for codeword 1
NANDC_SPARE1_1	0x0234	W	0x00000000	Spare Data and BCH Encode Information for codeword 1
NANDC_SPARE1_2	0x0238	W	0x00000000	Spare Data and BCH Encode Information for codeword 1
NANDC_SPARE1_3	0x023c	W	0x00000000	Spare Data and BCH Encode Information for codeword 1
NANDC_SPARE1_4	0x0240	W	0x00000000	Spare Data and BCH Encode Information for codeword 1
NANDC_SPARE1_5	0x0244	W	0x00000000	Spare Data and BCH Encode Information for codeword 1
NANDC_SPARE1_6	0x0248	W	0x00000000	Spare Data and BCH Encode Information for codeword 1
NANDC_SPARE1_7	0x024c	W	0x00000000	Spare Data and BCH Encode Information for codeword 1
NANDC_SPARE1_8	0x0250	W	0x00000000	Spare Data and BCH Encode Information for codeword 1
NANDC_SPARE1_9	0x0254	W	0x00000000	Spare Data and BCH Encode Information for codeword 1
NANDC_SPARE1_10	0x0258	W	0x00000000	Spare Data and BCH Encode Information for codeword 1
NANDC_SPARE1_11	0x025c	W	0x00000000	Spare Data and BCH Encode Information for codeword 1
NANDC_SPARE0_12	0x0260	W	0x00000000	Spare Data and BCH Encode Information for codeword 0
NANDC_SPARE0_13	0x0264	W	0x00000000	Spare Data and BCH Encode Information for codeword 0
NANDC_SPARE0_14	0x0268	W	0x00000000	Spare Data and BCH Encode Information for codeword 0

Name	Offset	Size	Reset Value	Description
NANDC_SPARE0_15	0x026c	W	0x00000000	Spare Data and BCH Encode Information for codeword 0
NANDC_SPARE0_16	0x0270	W	0x00000000	Spare Data and BCH Encode Information for codeword 0
NANDC_SPARE0_17	0x0274	W	0x00000000	Spare Data and BCH Encode Information for codeword 0
NANDC_SPARE0_18	0x0278	W	0x00000000	Spare Data and BCH Encode Information for codeword 0
NANDC_SPARE0_19	0x027c	W	0x00000000	Spare Data and BCH Encode Information for codeword 0
NANDC_SPARE0_20	0x0280	W	0x00000000	Spare Data and BCH Encode Information for codeword 0
NANDC_SPARE0_21	0x0284	W	0x00000000	Spare Data and BCH Encode Information for codeword 0
NANDC_SPARE0_22	0x0288	W	0x00000000	Spare Data and BCH Encode Information for codeword 0
NANDC_SPARE0_23	0x028c	W	0x00000000	Spare Data and BCH Encode Information for codeword 0
NANDC_SPARE0_24	0x0290	W	0x00000000	Spare Data and BCH Encode Information for codeword 0
NANDC_SPARE0_25	0x0294	W	0x00000000	Spare Data and BCH Encode Information for codeword 0
NANDC_SPARE0_26	0x0298	W	0x00000000	Spare Data and BCH Encode Information for codeword 0
NANDC_SPARE0_27	0x029c	W	0x00000000	Spare Data and BCH Encode Information for codeword 0
NANDC_SPARE1_12	0x02a0	W	0x00000000	Spare Data and BCH Encode Information for codeword 1
NANDC_SPARE1_13	0x02a4	W	0x00000000	Spare Data and BCH Encode Information for codeword 1
NANDC_SPARE1_14	0x02a8	W	0x00000000	Spare Data and BCH Encode Information for codeword 1
NANDC_SPARE1_15	0x02ac	W	0x00000000	Spare Data and BCH Encode Information for codeword 1
NANDC_SPARE1_16	0x02b0	W	0x00000000	Spare Data and BCH Encode Information for codeword 1
NANDC_SPARE1_17	0x02b4	W	0x00000000	Spare Data and BCH Encode Information for codeword 1
NANDC_SPARE1_18	0x02b8	W	0x00000000	Spare Data and BCH Encode Information for codeword 1
NANDC_SPARE1_19	0x02bc	W	0x00000000	Spare Data and BCH Encode Information for codeword 1

Name	Offset	Size	Reset Value	Description
NANDC_SPARE1_20	0x02c0	W	0x00000000	Spare Data and BCH Encode Information for codeword 1
NANDC_SPARE1_21	0x02c4	W	0x00000000	Spare Data and BCH Encode Information for codeword 1
NANDC_SPARE1_22	0x02c8	W	0x00000000	Spare Data and BCH Encode Information for codeword 1
NANDC_SPARE1_23	0x02cc	W	0x00000000	Spare Data and BCH Encode Information for codeword 1
NANDC_SPARE1_24	0x02d0	W	0x00000000	Spare Data and BCH Encode Information for codeword 1
NANDC_SPARE1_25	0x02d4	W	0x00000000	Spare Data and BCH Encode Information for codeword 1
NANDC_SPARE1_26	0x02d8	W	0x00000000	Spare Data and BCH Encode Information for codeword 1
NANDC_SPARE1_27	0x02dc	W	0x00000000	Spare Data and BCH Encode Information for codeword 1
NANDC_BCHDE0_24	0x0400	W	0x00000000	BCH decode result of 24th error bit for codeword 0
NANDC_BCHDE0_25	0x0404	W	0x00000000	BCH decode result of 25th error bit for codeword 0
NANDC_BCHDE0_26	0x0408	W	0x00000000	BCH decode result of 26th error bit for codeword 0
NANDC_BCHDE0_27	0x040c	W	0x00000000	BCH decode result of 27th error bit for codeword 0
NANDC_BCHDE0_28	0x0410	W	0x00000000	BCH decode result of 28th error bit for codeword 0
NANDC_BCHDE0_29	0x0414	W	0x00000000	BCH decode result of 29th error bit for codeword 0
NANDC_BCHDE0_30	0x0418	W	0x00000000	BCH decode result of 30th error bit for codeword 0
NANDC_BCHDE0_31	0x041c	W	0x00000000	BCH decode result of 31th error bit for codeword 0
NANDC_BCHDE0_32	0x0420	W	0x00000000	BCH decode result of 32th error bit for codeword 0
NANDC_BCHDE0_33	0x0424	W	0x00000000	BCH decode result of 33th error bit for codeword 0
NANDC_BCHDE0_34	0x0428	W	0x00000000	BCH decode result of 34th error bit for codeword 0
NANDC_BCHDE0_35	0x042c	W	0x00000000	BCH decode result of 35th error bit for codeword 0
NANDC_BCHDE0_36	0x0430	W	0x00000000	BCH decode result of 36th error bit for codeword 0

Name	Offset	Size	Reset Value	Description
NANDC_BCHDE0_37	0x0434	W	0x00000000	BCH decode result of 37th error bit for codeword 0
NANDC_BCHDE0_38	0x0438	W	0x00000000	BCH decode result of 38th error bit for codeword 0
NANDC_BCHDE0_39	0x043c	W	0x00000000	BCH decode result of 39th error bit for codeword 0
NANDC_BCHDE0_40	0x0440	W	0x00000000	BCH decode result of 40th error bit for codeword 0
NANDC_BCHDE0_41	0x0444	W	0x00000000	BCH decode result of 41th error bit for codeword 0
NANDC_BCHDE0_42	0x0448	W	0x00000000	BCH decode result of 42th error bit for codeword 0
NANDC_BCHDE0_43	0x044c	W	0x00000000	BCH decode result of 43th error bit for codeword 0
NANDC_BCHDE0_44	0x0450	W	0x00000000	BCH decode result of 44th error bit for codeword 0
NANDC_BCHDE0_45	0x0454	W	0x00000000	BCH decode result of 45th error bit for codeword 0
NANDC_BCHDE0_46	0x0458	W	0x00000000	BCH decode result of 46th error bit for codeword 0
NANDC_BCHDE0_47	0x045c	W	0x00000000	BCH decode result of 47th error bit for codeword 0
NANDC_BCHDE0_48	0x0460	W	0x00000000	BCH decode result of 48th error bit for codeword 0
NANDC_BCHDE0_49	0x0464	W	0x00000000	BCH decode result of 49th error bit for codeword 0
NANDC_BCHDE0_50	0x0468	W	0x00000000	BCH decode result of 50th error bit for codeword 0
NANDC_BCHDE0_51	0x046c	W	0x00000000	BCH decode result of 51th error bit for codeword 0
NANDC_BCHDE0_52	0x0470	W	0x00000000	BCH decode result of 52th error bit for codeword 0
NANDC_BCHDE0_53	0x0474	W	0x00000000	BCH decode result of 53th error bit for codeword 0
NANDC_BCHDE0_54	0x0478	W	0x00000000	BCH decode result of 54th error bit for codeword 0
NANDC_BCHDE0_55	0x047c	W	0x00000000	BCH decode result of 55th error bit for codeword 0
NANDC_BCHDE0_56	0x0480	W	0x00000000	BCH decode result of 56th error bit for codeword 0
NANDC_BCHDE0_57	0x0484	W	0x00000000	BCH decode result of 57th error bit for codeword 0

Name	Offset	Size	Reset Value	Description
NANDC_BCHDE0_58	0x0488	W	0x00000000	BCH decode result of 58th error bit for codeword 0
NANDC_BCHDE0_59	0x048c	W	0x00000000	BCH decode result of 59th error bit for codeword 0
NANDC_BCHDE1_24	0x0490	W	0x00000000	BCH decode result of 24th error bit for codeword 1
NANDC_BCHDE1_25	0x0494	W	0x00000000	BCH decode result of 25th error bit for codeword 1
NANDC_BCHDE1_26	0x0498	W	0x00000000	BCH decode result of 26th error bit for codeword 1
NANDC_BCHDE1_27	0x049c	W	0x00000000	BCH decode result of 27th error bit for codeword 1
NANDC_BCHDE1_28	0x04a0	W	0x00000000	BCH decode result of 28th error bit for codeword 1
NANDC_BCHDE1_29	0x04a4	W	0x00000000	BCH decode result of 29th error bit for codeword 1
NANDC_BCHDE1_30	0x04a8	W	0x00000000	BCH decode result of 30th error bit for codeword 1
NANDC_BCHDE1_31	0x04ac	W	0x00000000	BCH decode result of 31th error bit for codeword 1
NANDC_BCHDE1_32	0x04b0	W	0x00000000	BCH decode result of 32th error bit for codeword 1
NANDC_BCHDE1_33	0x04b4	W	0x00000000	BCH decode result of 33th error bit for codeword 1
NANDC_BCHDE1_34	0x04b8	W	0x00000000	BCH decode result of 34th error bit for codeword 1
NANDC_BCHDE1_35	0x04bc	W	0x00000000	BCH decode result of 35th error bit for codeword 1
NANDC_BCHDE1_36	0x04c0	W	0x00000000	BCH decode result of 36th error bit for codeword 1
NANDC_BCHDE1_37	0x04c4	W	0x00000000	BCH decode result of 37th error bit for codeword 1
NANDC_BCHDE1_38	0x04c8	W	0x00000000	BCH decode result of 38th error bit for codeword 1
NANDC_BCHDE1_39	0x04cc	W	0x00000000	BCH decode result of 39th error bit for codeword 1
NANDC_BCHDE1_40	0x04d0	W	0x00000000	BCH decode result of 40th error bit for codeword 1
NANDC_BCHDE1_41	0x04d4	W	0x00000000	BCH decode result of 41th error bit for codeword 1
NANDC_BCHDE1_42	0x04d8	W	0x00000000	BCH decode result of 42th error bit for codeword 1

Name	Offset	Size	Reset Value	Description
NANDC_BCHDE1_43	0x04dc	W	0x00000000	BCH decode result of 43th error bit for codeword 1
NANDC_BCHDE1_44	0x04e0	W	0x00000000	BCH decode result of 44th error bit for codeword 1
NANDC_BCHDE1_45	0x04e4	W	0x00000000	BCH decode result of 45th error bit for codeword 1
NANDC_BCHDE1_46	0x04e8	W	0x00000000	BCH decode result of 46th error bit for codeword 1
NANDC_BCHDE1_47	0x04ec	W	0x00000000	BCH decode result of 47th error bit for codeword 1
NANDC_BCHDE1_48	0x04f0	W	0x00000000	BCH decode result of 48th error bit for codeword 1
NANDC_BCHDE1_49	0x04f4	W	0x00000000	BCH decode result of 49th error bit for codeword 1
NANDC_BCHDE1_50	0x04f8	W	0x00000000	BCH decode result of 50th error bit for codeword 1
NANDC_BCHDE1_51	0x04fc	W	0x00000000	BCH decode result of 51th error bit for codeword 1
NANDC_BCHDE1_52	0x0500	W	0x00000000	BCH decode result of 52th error bit for codeword 1
NANDC_BCHDE1_53	0x0504	W	0x00000000	BCH decode result of 53th error bit for codeword 1
NANDC_BCHDE1_54	0x0508	W	0x00000000	BCH decode result of 54th error bit for codeword 1
NANDC_BCHDE1_55	0x050c	W	0x00000000	BCH decode result of 55th error bit for codeword 1
NANDC_BCHDE1_56	0x0510	W	0x00000000	BCH decode result of 56th error bit for codeword 1
NANDC_BCHDE1_57	0x0514	W	0x00000000	BCH decode result of 57th error bit for codeword 1
NANDC_BCHDE1_58	0x0518	W	0x00000000	BCH decode result of 58th error bit for codeword 1
NANDC_BCHDE1_59	0x051c	W	0x00000000	BCH decode result of 59th error bit for codeword 1
NANDC_BCHST8	0x0520	W	0x00000000	BCH Status Register For Codeword 16~17
NANDC_BCHST9	0x0524	W	0x00000000	BCH Status Register For Codeword 18~19
NANDC_BCHST10	0x0528	W	0x00000000	BCH Status Register For Codeword 20~21
NANDC_BCHST11	0x052c	W	0x00000000	BCH Status Register For Codeword 22~23

Name	Offset	Size	Reset Value	Description
NANDC_BCHST12	0x0530	W	0x00000000	BCH Status Register For Codeword 24~25
NANDC_BCHST13	0x0534	W	0x00000000	BCH Status Register For Codeword 26~27
NANDC_BCHST14	0x0538	W	0x00000000	BCH Status Register For Codeword 28~29
NANDC_BCHST15	0x053c	W	0x00000000	BCH Status Register For Codeword 30~31
NANDC_RANDMZ_SEE_D13_0	0x0600	W	0x00000000	Seed 0 for Toshiba 13 Power Polynomial Randomizer
NANDC_RANDMZ_SEE_D13_1	0x0604	W	0x00000000	Seed 1 for Toshiba 13 Power Polynomial Randomizer
NANDC_RANDMZ_SEE_D13_2	0x0608	W	0x00000000	Seed 2 for Toshiba 13 Power Polynomial Randomizer
NANDC_RANDMZ_SEE_D13_3	0x060c	W	0x00000000	Seed 3 for Toshiba 13 Power Polynomial Randomizer
NANDC_RANDMZ_SEE_D13_4	0x0610	W	0x00000000	Seed 4 for Toshiba 13 Power Polynomial Randomizer
NANDC_RANDMZ_SEE_D13_5	0x0614	W	0x00000000	Seed 5 for Toshiba 13 Power Polynomial Randomizer
NANDC_RANDMZ_SEE_D13_6	0x0618	W	0x00000000	Seed 6 for Toshiba 13 Power Polynomial Randomizer
NANDC_RANDMZ_SEE_D13_7	0x061c	W	0x00000000	Seed 7 for Toshiba 13 Power Polynomial Randomizer
NANDC_RANDMZ_SEE_D13_8	0x0620	W	0x00000000	Seed 8 for Toshiba 13 Power Polynomial Randomizer
NANDC_RANDMZ_SEE_D13_9	0x0624	W	0x00000000	Seed 9 for Toshiba 13 Power Polynomial Randomizer
NANDC_RANDMZ_SEE_D13_10	0x0628	W	0x00000000	Seed 10 for Toshiba 13 Power Polynomial Randomizer
NANDC_RANDMZ_SEE_D13_11	0x062c	W	0x00000000	Seed 11 for Toshiba 13 Power Polynomial Randomizer
NANDC_RANDMZ_SEE_D13_12	0x0630	W	0x00000000	Seed 12 for Toshiba 13 Power Polynomial Randomizer
NANDC_RANDMZ_SEE_D13_13	0x0634	W	0x00000000	Seed 13 for Toshiba 13 Power Polynomial Randomizer
NANDC_RANDMZ_SEE_D13_14	0x0638	W	0x00000000	Seed 14 for Toshiba 13 Power Polynomial Randomizer
NANDC_RANDMZ_SEE_D13_15	0x063c	W	0x00000000	Seed 15 for Toshiba 13 Power Polynomial Randomizer
NANDC_RANDMZ_SEE_D17_0	0x0640	W	0x00000000	Seed 0 for Toshiba 17 Power Polynomial Randomizer

Name	Offset	Size	Reset Value	Description
NANDC_RANDMZ_SEE_D17_1	0x0644	W	0x00000000	Seed 1 for Toshiba 17 Power Polynomial Randomizer
NANDC_RANDMZ_SEE_D17_2	0x0648	W	0x00000000	Seed 2 for Toshiba 17 Power Polynomial Randomizer
NANDC_RANDMZ_SEE_D17_3	0x064c	W	0x00000000	Seed 3 for Toshiba 17 Power Polynomial Randomizer
NANDC_RANDMZ_SEE_D17_4	0x0650	W	0x00000000	Seed 4 for Toshiba 17 Power Polynomial Randomizer
NANDC_RANDMZ_SEE_D17_5	0x0654	W	0x00000000	Seed 5 for Toshiba 17 Power Polynomial Randomizer
NANDC_RANDMZ_SEE_D17_6	0x0658	W	0x00000000	Seed 6 for Toshiba 17 Power Polynomial Randomizer
NANDC_RANDMZ_SEE_D17_7	0x065c	W	0x00000000	Seed 7 for Toshiba 17 Power Polynomial Randomizer
NANDC_RANDMZ_SEE_D17_8	0x0660	W	0x00000000	Seed 8 for Toshiba 17 Power Polynomial Randomizer
NANDC_RANDMZ_SEE_D17_9	0x0664	W	0x00000000	Seed 9 for Toshiba 17 Power Polynomial Randomizer
NANDC_RANDMZ_SEE_D17_10	0x0668	W	0x00000000	Seed 10 for Toshiba 17 Power Polynomial Randomizer
NANDC_RANDMZ_SEE_D17_11	0x066c	W	0x00000000	Seed 11 for Toshiba 17 Power Polynomial Randomizer
NANDC_RANDMZ_SEE_D17_12	0x0670	W	0x00000000	Seed 12 for Toshiba 17 Power Polynomial Randomizer
NANDC_RANDMZ_SEE_D17_13	0x0674	W	0x00000000	Seed 13 for Toshiba 17 Power Polynomial Randomizer
NANDC_RANDMZ_SEE_D17_14	0x0678	W	0x00000000	Seed 14 for Toshiba 17 Power Polynomial Randomizer
NANDC_RANDMZ_SEE_D17_15	0x067c	W	0x00000000	Seed 15 for Toshiba 17 Power Polynomial Randomizer
NANDC_RANDMZ_SEE_D19_0	0x0680	W	0x00000000	Seed 0 for Toshiba 19 Power Polynomial Randomizer
NANDC_RANDMZ_SEE_D19_1	0x0684	W	0x00000000	Seed 1 for Toshiba 19 Power Polynomial Randomizer
NANDC_RANDMZ_SEE_D19_2	0x0688	W	0x00000000	Seed 2 for Toshiba 19 Power Polynomial Randomizer
NANDC_RANDMZ_SEE_D19_3	0x068c	W	0x00000000	Seed 3 for Toshiba 19 Power Polynomial Randomizer
NANDC_RANDMZ_SEE_D19_4	0x0690	W	0x00000000	Seed 4 for Toshiba 19 Power Polynomial Randomizer
NANDC_RANDMZ_SEE_D19_5	0x0694	W	0x00000000	Seed 5 for Toshiba 19 Power Polynomial Randomizer

Name	Offset	Size	Reset Value	Description
NANDC_RANDMZ_SEE_D19_6	0x0698	W	0x00000000	Seed 6 for Toshiba 19 Power Polynomial Randomizer
NANDC_RANDMZ_SEE_D19_7	0x069c	W	0x00000000	Seed 7 for Toshiba 19 Power Polynomial Randomizer
NANDC_RANDMZ_SEE_D19_8	0x06a0	W	0x00000000	Seed 8 for Toshiba 19 Power Polynomial Randomizer
NANDC_RANDMZ_SEE_D19_9	0x06a4	W	0x00000000	Seed 9 for Toshiba 19 Power Polynomial Randomizer
NANDC_RANDMZ_SEE_D19_10	0x06a8	W	0x00000000	Seed 10 for Toshiba 19 Power Polynomial Randomizer
NANDC_RANDMZ_SEE_D19_11	0x06ac	W	0x00000000	Seed 11 for Toshiba 19 Power Polynomial Randomizer
NANDC_RANDMZ_SEE_D19_12	0x06b0	W	0x00000000	Seed 12 for Toshiba 19 Power Polynomial Randomizer
NANDC_RANDMZ_SEE_D19_13	0x06b4	W	0x00000000	Seed 13 for Toshiba 19 Power Polynomial Randomizer
NANDC_RANDMZ_SEE_D19_14	0x06b8	W	0x00000000	Seed 14 for Toshiba 19 Power Polynomial Randomizer
NANDC_RANDMZ_SEE_D19_15	0x06bc	W	0x00000000	Seed 15 for Toshiba 19 Power Polynomial Randomizer
NANDC_RANDMZ_SEE_D23_0	0x06c0	W	0x00000000	Seed 0 for Toshiba 23 Power Polynomial Randomizer
NANDC_RANDMZ_SEE_D23_1	0x06c4	W	0x00000000	Seed 1 for Toshiba 23 Power Polynomial Randomizer
NANDC_RANDMZ_SEE_D23_2	0x06c8	W	0x00000000	Seed 2 for Toshiba 23 Power Polynomial Randomizer
NANDC_RANDMZ_SEE_D23_3	0x06cc	W	0x00000000	Seed 3 for Toshiba 23 Power Polynomial Randomizer
NANDC_RANDMZ_SEE_D23_4	0x06d0	W	0x00000000	Seed 4 for Toshiba 23 Power Polynomial Randomizer
NANDC_RANDMZ_SEE_D23_5	0x06d4	W	0x00000000	Seed 5 for Toshiba 23 Power Polynomial Randomizer
NANDC_RANDMZ_SEE_D23_6	0x06d8	W	0x00000000	Seed 6 for Toshiba 23 Power Polynomial Randomizer
NANDC_RANDMZ_SEE_D23_7	0x06dc	W	0x00000000	Seed 7 for Toshiba 23 Power Polynomial Randomizer
NANDC_RANDMZ_SEE_D23_8	0x06e0	W	0x00000000	Seed 8 for Toshiba 23 Power Polynomial Randomizer
NANDC_RANDMZ_SEE_D23_9	0x06e4	W	0x00000000	Seed 9 for Toshiba 23 Power Polynomial Randomizer
NANDC_RANDMZ_SEE_D23_10	0x06e8	W	0x00000000	Seed 10 for Toshiba 23 Power Polynomial Randomizer

Name	Offset	Size	Reset Value	Description
NANDC_RANDMZ_SEE_D23_11	0x06ec	W	0x00000000	Seed 11 for Toshiba 23 Power Polynomial Randomizer
NANDC_RANDMZ_SEE_D23_12	0x06f0	W	0x00000000	Seed 12 for Toshiba 23 Power Polynomial Randomizer
NANDC_RANDMZ_SEE_D23_13	0x06f4	W	0x00000000	Seed 13 for Toshiba 23 Power Polynomial Randomizer
NANDC_RANDMZ_SEE_D23_14	0x06f8	W	0x00000000	Seed 14 for Toshiba 23 Power Polynomial Randomizer
NANDC_RANDMZ_SEE_D23_15	0x06fc	W	0x00000000	Seed 15 for Toshiba 23 Power Polynomial Randomizer

Notes: Size : **B** - Byte (8 bits) access, **HW** - Half WORD (16 bits) access, **W** -WORD (32 bits) access

6.4.3 Detail Register Description

NANDC_FMCTL

Address: Operational Base + offset (0x0000)

Flash Interface Control Register

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15	RW	0x0	syn_mode Toggle enable signal, 1 active. 0: ONFI synchronous flash. 1: Toggle synchronous flash.
14	RW	0x0	syn_clken Synchronous flash clock enable signal, 1 active. Only available in Synchronous Mode. 0: flash clock is disabled. 1: flash clock is enabled.
13	RW	0x0	tm Timing mode indication. 0: Asynchronous Mode. 1: Synchronous Mode (Toggle or ONFI Synchronous).
12	RW	0x0	dwidth Flash data bus width indication. 0: 8bits, active in both Asynchronous Mode flash and Synchronous Mode flash. 1: 16bits, active only in Asynchronous Mode flash.
11:10	RO	0x0	reserved

Bit	Attr	Reset Value	Description
9	RO	0x1	frdy Flash ready/busy indicate signal. 0: flash is busy. 1: flash is ready. This bit is the sample of the pin of R/Bn.
8	RW	0x0	wp Flash write protect. 0: flash program/erase disabled. 1: flash program/erase enabled. This bit is output to the pin of WPn.
7	RW	0x0	fcs7 Flash memory chip 7 select control. 1: hold flash memory chip select activity. 0: flash memory chip select activity free.
6	RW	0x0	fcs6 Flash memory chip 6 select control. 1: hold flash memory chip select activity. 0: flash memory chip select activity free.
5	RW	0x0	fcs5 Flash memory chip 5 select control. 1: hold flash memory chip select activity. 0: flash memory chip select activity free.
4	RW	0x0	fcs4 Flash memory chip 4 select control. 1: hold flash memory chip select activity. 0: flash memory chip select activity free.
3	RW	0x0	fcs3 Flash memory chip 3 select control. 1: hold flash memory chip select activity. 0: flash memory chip select activity free.
2	RW	0x0	fcs2 Flash memory chip 2 select control. 1: hold flash memory chip select activity. 0: flash memory chip select activity free.
1	RW	0x0	fcs1 Flash memory chip 1 select control. 1: hold flash memory chip select activity. 0: flash memory chip select activity free.
0	RW	0x0	fcs0 Flash memory chip 0 select control. 1: hold flash memory chip select activity. 0: flash memory chip select activity free.

NANDC_FMWAIT_ASYNC

Address: Operational Base + offset (0x0004)

Flash Timing Control Register For Asynchronous Timing

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30	RW	0x0	fmw_dly_en fmw_dly enable signal, 1 active.
29:24	RW	0x3f	fmw_dly The number of delay cycle between two codeword transmission.
23:18	RO	0x0	reserved
17:12	RW	0x3f	csrw When in Asynchronous mode or Toggle address/command mode, this field specifies the number of processor clock cycles from the falling edge of CSn to the falling edge of RDn or WRn. The min value of csrw is 0.
11	RO	0x0	reserved
10:5	RW	0x3f	rwpw When in Asynchronous mode or Toggle address/command mode, this field specifies the width of RDn or WRn in processor clock cycles, $0x0 \leq rwpw \leq 0x3f$.
4:0	RW	0x1f	rwcs When in Asynchronous mode or Toggle address/command mode, this field specifies the number of processor clock cycles from the rising edge of RDn or WRn to the rising edge of CSn, $0x0 \leq rwcs \leq 0x1f$.

NANDC_FLCTL

Address: Operational Base + offset (0x0008)

Internal Transfer Control Register

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28	RW	0x0	low_power Nandc low power control 0: normal mode 1: low power mode
27:22	RW	0x00	page_num Transmission codeword number in internal DMA mode when bus-mode is master-mode 1~32: 1~32 codeword. default: not support. Notes: a. Only active in internal DMA mode b. Only active when bus-mode is master-mode

Bit	Attr	Reset Value	Description
21	RW	0x0	<p>page_size Transmission codeword size in internal DMA mode 0: 1024bytes/codeword 1: 512bytes/codeword</p>
20	RO	0x1	<p>tr_rdy Internal DMA transmission ready indication. 0: internal DMA transmission is busy 1: internal DMA transmission is ready When reading flash, tr_rdy should not be set to 1 until all data transmission and correct finished. When programing flash, tr_rdy should not be set to 1 until all data transmission finished. Notes: Only active in internal DMA mode.</p>
19	RO	0x0	reserved
18:12	RW	0x00	<p>spare_size Spare byte number when lba_en=1. $0 \leq \text{spare_size} \leq 109$. When $\text{spare_size} \geq 109$, it is treated as 0. Notes: The spare_size must be even number when flash is ONFI Synchronous Flash or Asynchronous Flash with 16bits data width.</p>
11	RW	0x0	<p>lba_en LBA mode indication, 1 active. 0: NO-LBA mode, NandC should transfer both page data and spare data in every codeword, and the page size is 1024 bytes or 512 bytes determined by BCHCTL[16](bchpage), spare size is 32/46/74 bytes or 109 bytes determined by BCHCTL[4] and BCHCTL[18]. 1: LBA mode, NandC should transfer both page data and spare data in every codeword, and the page size is 1024 bytes or 512 bytes determined by FLCTL[21](page_size), spare size is determined by FLCTL[17:12](spare_size). Notes: a. When lba_en is active, BCH CODEC should be disabled, spare_size and page_size are configurable. b. When lba_en is active, cor_able is inactive.</p>

Bit	Attr	Reset Value	Description
10	RW	0x0	<p>cor_able Auto correct enable indication, 1 active. 0: auto correct disable 1: auto correct enable Notes: a. Only active in internal DMA mode. b. lba_en is prior to cor_able. When lba_en=1, cor_able is ignored.</p>
9:8	RO	0x0	reserved
7	RW	0x0	<p>flash_st_mod Mode for NandC to start internal data transmission in internal DMA mode. 0: busy mode: hardware should not start internal data transmission until flash is ready even flash_st is asserted. 1: ready mode: hardware should start internal data transmission directly when flash_st is asserted. Notes: Only active in internal DMA mode.</p>
6:5	RW	0x0	<p>tr_count Transmission codeword number in internal DMA mode when bus-mode is slave-mode 00: 0 codeword need transferred 01: 1 codeword need transferred 10: 2 codeword need transferred 11: not supported Notes: a. Only active in internal DMA mode. b. Only active when bus-mode is slave-mode.</p>
4	RW	0x0	<p>st_addr Start buffer address. 0: start transfer from sram0 1: start transfer from sram1 Notes: Only active in internal DMA mode.</p>
3	RW	0x0	<p>bypass NandC internal DMA bypass indication. 0: bypass the internal DMA, data are transferred to/from flash by direct path. 1: internal DMA active, data are transferred to/from flash by internal DMA.</p>

Bit	Attr	Reset Value	Description
2	RW	0x0	<p>flash_st Start signal for NandC to transfer data between flash and internal buffer in internal DMA mode. When asserted, it will auto cleared.</p> <p>0: not start transmission 1: start transmission</p> <p>Notes: Only active in internal DMA mode</p>
1	RW	0x0	<p>flash_rdn Indicate data flow direction. 0: NandC read data from flash. 1: NandC write data to flash</p>
0	RW	0x0	<p>flash_RST NandC software reset indication. When asserted, it will auto cleared. 0: not software reset 1: software reset</p> <p>Notes: flash_RST is prior to flash_st</p>

NANDC_BCHCTL

Address: Operational Base + offset (0x000c)

BCH Control Register

Bit	Attr	Reset Value	Description
31:27	RO	0x0	reserved
26:19	RW	0x00	bchthres BCH error number threshold
18	RW	0x0	bchmode1 High bit of BCH mode selection for 40bitBCH or 60bitBCH. BchMode=bchmode1, bchmode0: 00: 16bitBCH 01: 24bitBCH 10: 40bitBCH 11: 60bitBCH
17	RO	0x0	reserved

Bit	Attr	Reset Value	Description
16	RW	0x0	<p>bchpage The data size indication when BCH is active. 0: 1024 bytes, all the 1024 bytes data in codeword are valid data to be transferred. 1: 512 bytes, higher 512bytes are valid, and lower 512bytes are invalid and stuffed with 0xff.</p> <p>Notes:</p> <ul style="list-style-type: none"> a. Only active when data transferred in internal DMA mode. b. Only active for asynchronous flash.
15:8	RW	0x00	<p>addr BCH active range selection. BCH should be active when access in range address.</p>
7:5	RW	0x0	<p>region BCH active region selection indication. 000: Flash memory 0 region (flash 0) 001: Flash memory 1 region (flash 1) 010: Flash memory 2 region (flash 2) 011: Flash memory 3 region (flash 3) 100: Flash memory 4 region (flash 4) 101: Flash memory 5 region (flash 5) 110: Flash memory 6 region (flash 6) 111: Flash memory 7 region (flash 7)</p>
4	RW	0x0	<p>bchmode0 BCH mode selection indication. BCH mode is determined by both bchmode0 and bchmode1,detailed information is showed in BCHCTL[18].</p>
3	RW	0x1	<p>bchepd BCH encoder/decoder power down indication. 0: BCH encoder/decoder working. 1: BCH encoder/decoder not working.</p>
2	RW	0x0	<p>mode_addrare BCH address care mode selection indication. 0: address care. 1: address not care.</p> <p>Notes: This bit is just active for data transmission in bypass mode, but not for command and address transmission.</p>
1	RO	0x0	reserved

Bit	Attr	Reset Value	Description
0	RW	0x0	<p>bchrst BCH software reset indication, When asserted, it will auto cleared. 0: not software reset 1: software reset Notes: a. BCH Decoder should be software reset before decode begin. b. bch software reset should be used with nandc software reset at the same time.</p>

NANDC_MTRANS_CFG

Address: Operational Base + offset (0x0010)

Bus Transfer Configuration Register

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15	W1C	0x0	<p>ahb_rst ahb master interface software reset, auto cleared</p>
14	RW	0x0	<p>fl_pwd Flash power down indication, 1 active. 0: Flash power on, data transferred through master interface is data that to be written into or read from flash. 1: Flash power down, data transferred through master interface is not data that to be written into or read from flash. NandC is just used as DMA for external memory and internal memory.</p>
13:9	RW	0x00	<p>incr_num AHB Master incr num indication. incr_num=1~16. When burst=001, software should configure incr_num. Notes: Only active for master-mode.</p>
8:6	RW	0x7	<p>burst AHB Master burst type indication: 000 : Single transfer 011 : 4-beat burst 101 : 8-beat Burst 111 : 16-beat burst default : not supported Notes: Only active for master-mode.</p>

Bit	Attr	Reset Value	Description
5:3	RW	0x2	<p>hsize AHB Master data size indication: 000 : 8 bits 001 : 16 bits 010 : 32 bits default : not supported Notes: Only active for master-mode.</p>
2	RW	0x0	<p>bus_mode Bus interface selection. 0: Slave interface, flash data is transferred through slave interface 1: Master interface, flash data is transferred through master interface</p>
1	RW	0x0	<p>ahb_wr Data transfer direction through master interface. 0: read direction(internal memory ->external memory) 1: write direction (internal memory->external memory) Notes: a. Only active for master-mode. b. When read flash(flash_rdn=0), ahb_wr=1; when program flash(flash_rdn=1), ahb_wr=0.</p>
0	W1C	0x0	<p>ahb_wr_st Start indication for loading data from external memory to internal memory or storing data from internal memory to external memory through master. When asserted, it will auto cleared. Notes: a. Only active for master-mode and fl_pwd=1. b. When fl_pwd=0, flash is active, NandC start to transfer data through master interface if flash_st=1 c. When fl_pwd=1, flash is not active, NandC start to transfer data through master interface if ahb_wr_st=1</p>

NANDC_MTRANS_SADDR0

Address: Operational Base + offset (0x0014)

Start Address Register For Page Data Transmission

Bit	Attr	Reset Value	Description
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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	saddr0 Start address for page data transmission. Notes: a. Only active for master-mode. b. Should be aligned with hsize in MTRANS_CFG[5:3].

NANDC_MTRANS_SADDR1

Address: Operational Base + offset (0x0018)

Start Address Register For Spare Data Transmission

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	saddr1 Start address for spare data. Notes: a. Only active for master-mode. b. Should be aligned with hsize in MTRANS_CFG[5:3].

NANDC_MTRANS_STAT

Address: Operational Base + offset (0x001c)

Bus Transfer Status Register

Bit	Attr	Reset Value	Description
31:22	RO	0x0	reserved
21:16	RO	0x00	mtrans_cnt finished counter for codeword transmission through Master interface Notes: Only active for master-mode.
15:0	RO	0x0000	bus_err Bus error indication for codeword0~15. [0] : bus error for codeword 0 [15] : bus error for codeword 15 Notes: Only active for master-mode.

NANDC_BCHST0

Address: Operational Base + offset (0x0020)

BCH Status Register For Codeword 0~1

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30	RO	0x0	err_hnum1_h1 Highest bit of err_hnum1
29	RO	0x0	err_tnum1_h1 Highest bit of err_tnum1

Bit	Attr	Reset Value	Description
28	RO	0x0	err_hnum0_h1 Highest bit of err_hnum0
27	RO	0x0	err_tnum0_h1 Highest bit of err_tnum0
26	RO	0x1	bchrdy Ready indication for bch encoder/decoder, 1 active. 0: bch encoder/decoder is busy 1: bch encoder/decoder is ready
25:21	RO	0x00	err_hnum1_l5 Lower 5 bits of number of error bits found in first 512bytes of 1st backup codeword
20:16	RO	0x00	err_tnum1_l5 Lower 5 bits of number of error bits found in 1st backup codeword
15	RO	0x0	fail1 Indication for the 1st backup codeword decoded failed or not. 0: decode successfully 1: decode fail
14	RO	0x0	done1 Indication for finishing decoding the 1st backup codeword 0: not finished 1: finished
13	RO	0x0	errf1 Indication for error found in 1st backup codeword. 0: no error 1: error found
12:8	RO	0x00	err_hnum0_l5 Lower 5 bits of number of error bits found in first 512bytes of current backup codeword
7:3	RO	0x00	err_tnum0_l5 Lower 5 bits of number of error bits found in current backup codeword
2	RO	0x0	fail0 Indication for current backup codeword decode failed or not 0: decode successfully 1: decode fail

Bit	Attr	Reset Value	Description
1	RO	0x0	done0 Indication for finishing decoding the current backup codeword. 0: not finished 1: finished
0	RO	0x0	errf0 Indication for error found in current backup codeword. 0: no error 1: error found

NANDC_BCHST1

Address: Operational Base + offset (0x0024)

BCH Status Register For Codeword 2~3

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30	RO	0x0	err_hnum3_h1 Highest bit of err_hnum3
29	RO	0x0	err_tnum3_h1 Highest bit of err_tnum3
28	RO	0x0	err_hnum2_h1 Highest bit of err_hnum2
27	RO	0x0	err_tnum2_h1 Highest bit of err_tnum2
26	RO	0x0	reserved
25:21	RO	0x00	err_hnum3_l5 Lower 5 bits of number of error bits found in first 512bytes of 3th backup codeword
20:16	RO	0x00	err_tnum3_l5 Lower 5 bits of number of error bits found in 3th backup codeword
15	RO	0x0	fail3 Indication for the 3th backup codeword decoded failed or not. 0: decode successfully 1: decode fail
14	RO	0x0	done3 Indication for finishing decoding the 3th backup codeword 0: not finished 1: finished

Bit	Attr	Reset Value	Description
13	RO	0x0	errf3 Indication for error found in 3th backup codeword. 0: no error 1: error found
12:8	RO	0x00	err_hnum2_l5 Lower 5 bits of number of error bits found in first 512bytes of 2th backup codeword
7:3	RO	0x00	err_tnum2_l5 Lower 5 bits of number of error bits found in 2th backup codeword
2	RO	0x0	fail2 Indication for 2th backup codeword decode failed or not 0: decode successfully 1: decode fail
1	RO	0x0	done2 Indication for finishing decoding the 2th backup codeword. 0: not finished 1: finished
0	RO	0x0	errf2 Indication for error found in 2th backup codeword. 0: no error 1: error found

NANDC_BCHST2

Address: Operational Base + offset (0x0028)

BCH Status Register For Codeword 4~5

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	bchst_cwd4_cwd5 BCHST information for 4th and 5th backup codeword. Bit assignment is similar to BCHST1 register. For more description, please refer to BCHST1 register.

NANDC_BCHST3

Address: Operational Base + offset (0x002c)

BCH Status Register For Codeword 6~7

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	bchst_cwd6_cwd7 BCHST information for 6th and 7th backup codeword. Bit assignment is similar to BCHST1 register. For more description, please refer to BCHST1 register.

NANDC_BCHST4

Address: Operational Base + offset (0x0030)

BCH Status Register For Codeword 8~9

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	bchst_cwd8_cwd9 BCHST information for 8th and 9th backup codeword. Bit assignment is similar to BCHST1 register. For more description, please refer to BCHST1 register.

NANDC_BCHST5

Address: Operational Base + offset (0x0034)

BCH Status Register For Codeword 10~11

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	bchst_cwd10_cwd11 BCHST information for 10th and 11th backup codeword. Bit assignment is similar to BCHST1 register. For more description, please refer to BCHST1 register.

NANDC_BCHST6

Address: Operational Base + offset (0x0038)

BCH Status Register For Codeword 12~13

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	bchst_cwd12_cwd13 BCHST information for 12th and 13th backup codeword. Bit assignment is similar to BCHST1 register. For more description, please refer to BCHST1 register.

NANDC_BCHST7

Address: Operational Base + offset (0x003c)

BCH Status Register For Codeword 14~15

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	bchst_cwd14_cwd15 BCHST information for 14th and 15th backup codeword. Bit assignment is similar to BCHST1 register. For more description, please refer to BCHST1 register.

NANDC_BCHLOC0

Address: Operational Base + offset (0x0040)

BCH Error Bit Location Number Register For Codeword 0~5

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:25	RO	0x00	err_loc5_I5 Lower 5 bits of number of 8bit error location in 5th backup codeword
24:20	RO	0x00	err_loc4_I5 Lower 5 bits of number of 8bit error location in 4th backup codeword
19:15	RO	0x00	err_loc3_I5 Lower 5 bits of number of 8bit error location in 3rd backup codeword
14:10	RO	0x00	err_loc2_I5 Lower 5 bits of number of 8bit error location in 2nd backup codeword
9:5	RO	0x00	err_loc1_I5 Lower 5 bits of number of 8bit error location in 1st backup codeword
4:0	RO	0x00	err_loc0_I5 Lower 5 bits of number of 8bit error location in current backup codeword

NANDC_BCHLOC1

Address: Operational Base + offset (0x0044)

BCH Error Bit Location Number Register For Codeword 6~11

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:25	RO	0x00	err_loc11_I5 Lower 5 bits of number of 8bit error location in 11th backup codeword
24:20	RO	0x00	err_loc10_I5 Lower 5 bits of number of 8bit error location in 10th backup codeword
19:15	RO	0x00	err_loc9_I5 Lower 5 bits of number of 8bit error location in 9th backup codeword

Bit	Attr	Reset Value	Description
14:10	RO	0x00	err_loc8_I5 Lower 5 bits of number of 8bit error location in 8th backup codeword
9:5	RO	0x00	err_loc7_I5 Lower 5 bits of number of 8bit error location in 7th backup codeword
4:0	RO	0x00	err_loc6_I5 Lower 5 bits of number of 8bit error location in 6th backup codeword

NANDC_BCHLOC2

Address: Operational Base + offset (0x0048)

BCH Error Bit Location Number Register For Codeword 12~17

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:25	RO	0x00	err_loc17_I5 Lower 5 bits of number of 8bit error location in 17th backup codeword
24:20	RO	0x00	err_loc16_I5 Lower 5 bits of number of 8bit error location in 16th backup codeword
19:15	RO	0x00	err_loc15_I5 Lower 5 bits of number of 8bit error location in 15th backup codeword
14:10	RO	0x00	err_loc14_I5 Lower 5 bits of number of 8bit error location in 14th backup codeword
9:5	RO	0x00	err_loc13_I5 Lower 5 bits of number of 8bit error location in 13th backup codeword
4:0	RO	0x00	err_loc12_I5 Lower 5 bits of number of 8bit error location in 12th backup codeword

NANDC_BCHLOC3

Address: Operational Base + offset (0x004c)

BCH Error Bit Location Number Register For Codeword 24~29

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:25	RO	0x00	err_loc23_I5 Lower 5 bits of number of 8bit error location in 23th backup codeword

Bit	Attr	Reset Value	Description
24:20	RO	0x00	err_loc22_I5 Lower 5 bits of number of 8bit error location in 22th backup codeword
19:15	RO	0x00	err_loc21_I5 Lower 5 bits of number of 8bit error location in 21th backup codeword
14:10	RO	0x00	err_loc20_I5 Lower 5 bits of number of 8bit error location in 20th backup codeword
9:5	RO	0x00	err_loc19_I5 Lower 5 bits of number of 8bit error location in 19th backup codeword
4:0	RO	0x00	err_loc18_I5 Lower 5 bits of number of 8bit error location in 18th backup codeword

NANDC_BCHLOC4

Address: Operational Base + offset (0x0050)

BCH Error Bit Location Number Register For Codeword 24~29

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:25	RO	0x00	err_loc29_I5 Lower 5 bits of number of 8bit error location in 23th backup codeword
24:20	RO	0x00	err_loc28_I5 Lower 5 bits of number of 8bit error location in 22th backup codeword
19:15	RO	0x00	err_loc27_I5 Lower 5 bits of number of 8bit error location in 21th backup codeword
14:10	RO	0x00	err_loc26_I5 Lower 5 bits of number of 8bit error location in 20th backup codeword
9:5	RO	0x00	err_loc25_I5 Lower 5 bits of number of 8bit error location in 19th backup codeword
4:0	RO	0x00	err_loc24_I5 Lower 5 bits of number of 8bit error location in 18th backup codeword

NANDC_BCHLOC5

Address: Operational Base + offset (0x0054)

BCH Error Bit Location Number Register For Codeword 30~31

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:10	RO	0x0	reserved
9:5	RO	0x00	err_loc31_l5 Lower 5 bits of number of 8bit error location in 31th backup codeword
4:0	RO	0x00	err_loc30_l5 Lower 5 bits of number of 8bit error location in 30th backup codeword

NANDC_BCHLOC6

Address: Operational Base + offset (0x0058)

Highest Bit For BCH Error Bit Location Number Register

Bit	Attr	Reset Value	Description
31	RO	0x0	err_loc31_h1 High bit for numbers of 8bit error location in 31th codeword
30	RO	0x0	err_loc30_h1 High bit for numbers of 8bit error location in 30th codeword
29	RO	0x0	err_loc29_h1 High bit for numbers of 8bit error location in 29th codeword
28	RO	0x0	err_loc28_h1 High bit for numbers of 8bit error location in 28th codeword
27	RO	0x0	err_loc27_h1 High bit for numbers of 8bit error location in 27th codeword
26	RO	0x0	err_loc26_h1 High bit for numbers of 8bit error location in 26th codeword
25	RO	0x0	err_loc25_h1 High bit for numbers of 8bit error location in 25th codeword
24	RO	0x0	err_loc24_h1 High bit for numbers of 8bit error location in 24th codeword
23	RO	0x0	err_loc23_h1 High bit for numbers of 8bit error location in 23th codeword
22	RO	0x0	err_loc22_h1 High bit for numbers of 8bit error location in 22th codeword
21	RO	0x0	err_loc21_h1 High bit for numbers of 8bit error location in 21th codeword

Bit	Attr	Reset Value	Description
20	RO	0x0	err_loc20_h1 High bit for numbers of 8bit error location in 20th codeword
19	RO	0x0	err_loc19_h1 High bit for numbers of 8bit error location in 19th codeword
18	RO	0x0	err_loc18_h1 High bit for numbers of 8bit error location in 18th codeword
17	RO	0x0	err_loc17_h1 High bit for numbers of 8bit error location in 17th codeword
16	RO	0x0	err_loc16_h1 High bit for numbers of 8bit error location in 16th codeword
15	RO	0x0	err_loc15_h1 High bit for numbers of 8bit error location in 15th codeword
14	RO	0x0	err_loc14_h1 High bit for numbers of 8bit error location in 14th codeword
13	RO	0x0	err_loc13_h1 High bit for numbers of 8bit error location in 13th codeword
12	RO	0x0	err_loc12_h1 High bit for numbers of 8bit error location in 12th codeword
11	RO	0x0	err_loc11_h1 High bit for numbers of 8bit error location in 11th codeword
10	RO	0x0	err_loc10_h1 High bit for numbers of 8bit error location in 10th codeword
9	RO	0x0	err_loc9_h1 High bit for numbers of 8bit error location in 9th codeword
8	RO	0x0	err_loc8_h1 High bit for numbers of 8bit error location in 8th codeword
7	RO	0x0	err_loc7_h1 High bit for numbers of 8bit error location in 7th codeword
6	RO	0x0	err_loc6_h1 High bit for numbers of 8bit error location in 6th codeword

Bit	Attr	Reset Value	Description
5	RO	0x0	err_loc5_h1 High bit for numbers of 8bit error location in 5th codeword
4	RO	0x0	err_loc4_h1 High bit for numbers of 8bit error location in 4th codeword
3	RO	0x0	err_loc3_h1 High bit for numbers of 8bit error location in 3th codeword
2	RO	0x0	err_loc2_h1 High bit for numbers of 8bit error location in 2th codeword
1	RO	0x0	err_loc1_h1 High bit for numbers of 8bit error location in 1th codeword
0	RO	0x0	err_loc0_h1 High bit for numbers of 8bit error location in 0th codeword

NANDC_BCHDE0_0

Address: Operational Base + offset (0x0070)

BCH decode result of 0th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:8	RO	0x000	offset The offset byte address of the error bit. The value is 11bit, which is the byte offset address in the codeword. The address can be divided into different part for different use, showed as follows. 0 ~1023: page data 1024~1027: system information 1028~1055: bch information for 16bitBCH 1028~1069: bch information for 24bitBCH 1028~1097: bch information for 40bitBCH 1028~1132: bch information for 60bitBCH
7:0	RO	0x00	err_val The error value of corresponding error byte

NANDC_BCHDE0_1

Address: Operational Base + offset (0x0074)

BCH decode result of 1th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved

Bit	Attr	Reset Value	Description
18:0	RO	0x00000	bchde0_1 decode result of 1th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_2

Address: Operational Base + offset (0x0078)

BCH decode result of 2th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_2 decode result of 2th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_3

Address: Operational Base + offset (0x007c)

BCH decode result of 3th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_3 decode result of 3th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_4

Address: Operational Base + offset (0x0080)

BCH decode result of 4th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_4 decode result of 4th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_5

Address: Operational Base + offset (0x0084)
 BCH decode result of 5th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_5 decode result of 5th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_6

Address: Operational Base + offset (0x0088)
 BCH decode result of 6th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_6 decode result of 6th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_7

Address: Operational Base + offset (0x008c)
 BCH decode result of 7th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_7 decode result of 7th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_8

Address: Operational Base + offset (0x0090)
 BCH decode result of 8th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_8 decode result of 8th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_9

Address: Operational Base + offset (0x0094)

BCH decode result of 9th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_9 decode result of 9th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_10

Address: Operational Base + offset (0x0098)

BCH decode result of 10th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_10 decode result of 10th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_11

Address: Operational Base + offset (0x009c)

BCH decode result of 11th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_11 decode result of 11th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_12

Address: Operational Base + offset (0x00a0)

BCH decode result of 12th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved

Bit	Attr	Reset Value	Description
18:0	RO	0x00000	bchde0_12 decode result of 12th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_13

Address: Operational Base + offset (0x00a4)

BCH decode result of 13th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_13 decode result of 13th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_14

Address: Operational Base + offset (0x00a8)

BCH decode result of 14th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_14 decode result of 14th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_15

Address: Operational Base + offset (0x00ac)

BCH decode result of 15th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_15 decode result of 15th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_16

Address: Operational Base + offset (0x00b0)
 BCH decode result of 16th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_16 decode result of 16th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_17

Address: Operational Base + offset (0x00b4)
 BCH decode result of 17th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_17 decode result of 17th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_18

Address: Operational Base + offset (0x00b8)
 BCH decode result of 18th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_18 decode result of 18th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_19

Address: Operational Base + offset (0x00bc)
 BCH decode result of 19th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_19 decode result of 1th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_20

Address: Operational Base + offset (0x00c0)

BCH decode result of 20th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_20 decode result of 20th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_21

Address: Operational Base + offset (0x00c4)

BCH decode result of 21th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_21 decode result of 21th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_22

Address: Operational Base + offset (0x00c8)

BCH decode result of 22th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_22 decode result of 22th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_23

Address: Operational Base + offset (0x00cc)

BCH decode result of 23th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved

Bit	Attr	Reset Value	Description
18:0	RO	0x00000	bchde0_23 decode result of 23th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE1_0

Address: Operational Base + offset (0x00d0)

BCH decode result of 0th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:8	RO	0x000	offset The offset byte address of the error bit. The value is 11bit, which is the byte offset address in the codeword. The address can be divided into different part for different use, showed as follows. 0 ~1023: page data 1024~1027: system information 1028~1055: bch information for 16bitBCH 1028~1069: bch information for 24bitBCH 1028~1097: bch information for 40bitBCH 1028~1132: bch information for 60bitBCH
7:0	RO	0x00	err_val The error value of corresponding error byte

NANDC_BCHDE1_1

Address: Operational Base + offset (0x00d4)

BCH decode result of 1th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_1 decode result of 1th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_2

Address: Operational Base + offset (0x00d8)

BCH decode result of 2th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved

Bit	Attr	Reset Value	Description
18:0	RO	0x00000	bchde1_2 decode result of 2th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_3

Address: Operational Base + offset (0x00dc)

BCH decode result of 3th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_3 decode result of 3th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_4

Address: Operational Base + offset (0x00e0)

BCH decode result of 4th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_4 decode result of 4th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_5

Address: Operational Base + offset (0x00e4)

BCH decode result of 5th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_5 decode result of 5th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_6

Address: Operational Base + offset (0x00e8)
 BCH decode result of 6th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_6 decode result of 6th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_7

Address: Operational Base + offset (0x00ec)
 BCH decode result of 7th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_7 decode result of 7th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_8

Address: Operational Base + offset (0x00f0)
 BCH decode result of 8th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_8 decode result of 8th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_9

Address: Operational Base + offset (0x00f4)
 BCH decode result of 9th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_9 decode result of 9th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_10

Address: Operational Base + offset (0x00f8)

BCH decode result of 10th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_10 decode result of 10th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_11

Address: Operational Base + offset (0x00fc)

BCH decode result of 11th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_11 decode result of 11th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_12

Address: Operational Base + offset (0x0100)

BCH decode result of 12th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_12 decode result of 12th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_13

Address: Operational Base + offset (0x0104)

BCH decode result of 13th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved

Bit	Attr	Reset Value	Description
18:0	RO	0x00000	bchde1_13 decode result of 13th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_14

Address: Operational Base + offset (0x0108)

BCH decode result of 14th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_14 decode result of 14th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_15

Address: Operational Base + offset (0x010c)

BCH decode result of 15th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_15 decode result of 15th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_16

Address: Operational Base + offset (0x0110)

BCH decode result of 16th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_16 decode result of 16th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_17

Address: Operational Base + offset (0x0114)
 BCH decode result of 17th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_17 decode result of 17th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_18

Address: Operational Base + offset (0x0118)
 BCH decode result of 1th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_18 decode result of 18th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_19

Address: Operational Base + offset (0x011c)
 BCH decode result of 19th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_19 decode result of 19th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_20

Address: Operational Base + offset (0x0120)
 BCH decode result of 20th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_20 decode result of 20th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_21

Address: Operational Base + offset (0x0124)

BCH decode result of 21th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_21 decode result of 21th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_22

Address: Operational Base + offset (0x0128)

BCH decode result of 22th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_22 decode result of 22th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_23

Address: Operational Base + offset (0x012c)

BCH decode result of 23th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_23 decode result of 23th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_DLL_CTL_REG0

Address: Operational Base + offset (0x0130)

DLL Control Register 0

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23:16	RW	0x7f	dll_dqs_dly_bypass Holds the read DQS delay setting when the DLL is operating in bypass mode.

Bit	Attr	Reset Value	Description
15:8	RW	0x7f	dll_dqs_dly Holds the read DQS delay setting when the DLL is operating in normal mode. Typically, this value is 1/4 of a clock cycle. Each increment of this field represents 1/128th of a clock cycle.
7:0	RW	0x05	dll_start_point DLL Start Point Control. This value is loaded into the DLL at initialization and is the value at which the DLL will begin searching for a lock. Each increment of this field represents 1/128th of a clock cycle.

NANDC_DLL_CTL_REG1

Address: Operational Base + offset (0x0134)

DLL Control Register 1

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:4	RW	0x02	dll_incr DLL Increment Value. This sets the increment used by the DLL when searching for a lock. It is recommended keeping this field small (around 0x4) to keep the steps gradual
3:2	RW	0x0	dll_qtren Quarter flag of DLL, active in no-bypass mode. 01:1/4 fclk, dqs_dly=128. 10:1/8 fclk, dqs_dly=64. Default: dqs_dly=dll_dqs_dly(DLL_CTL_REG0[15:8]). When dll_qtr='b01 or 'b10, software not need to configure dll_dqs_dly , and hardware should delay the input signal for 1/4 or 1/8 fclk cycle time; When dll_qtr=0, software need to configure dll_dqs_dly.
1	RW	0x1	dll_bypass DLL Bypass Control, 1active 0: dll not bypass, dll_dqs_dleay= dqs_dly 1: dll bypass, dll_dqs_dleay= dll_dqs_dly_bypass
0	RW	0x0	dll_start Start signal for DLL, 1 active. Notes: It will keep high until dll disabled.

NANDC_DLL_OBS_REG0

Address: Operational Base + offset (0x0138)

DLL Status Register

Bit	Attr	Reset Value	Description
31:17	RO	0x0	reserved
16:9	RO	0x01	dll_dqs_delay_value Report the delay value for the read DQS signal
8:1	RO	0x00	dll_lock_value Reports the DLL encoder value from the master DLL to the slave DLL's. The slaves use this value to set up their delays for the clk_wr and read DQS signals.
0	RO	0x0	dll_lock DLL Lock indication: 0: DLL has not locked 1: DLL is locked.

NANDC_RANDMZ_CFG

Address: Operational Base + offset (0x0150)

Randomizer Configure Register

Bit	Attr	Reset Value	Description
31	RW	0x0	randmz_en Randomizer enable indication, 1 active. 0: Randomizer active 1: Randomizer not active Notes: a. Not active when data transmission in bypass mode. b. Just active for data, but not for address and command. c. Not active when BchPage=1.
30:29	RW	0x0	randmz_mode Randomizer mode: 00- Samsung randomizer Polynomial= $1+x+x^{15}$ 10- Samsung randomizer Polynomial= $1+x^{14}+x^{15}$ 01-TOSHIBA randomizer
28:24	RW	0x00	page_offset basic seed rotation bits for every 16page
23:20	RW	0x0	cwd_offset basic seed start point for every page

Bit	Attr	Reset Value	Description
19:0	RW	0x00000	randmz_seed when Samsung randomizer: The seed for randomizer(initial value); when Toshiba randomizer: Seed Agitation Register.

NANDC_FMWAIT_SYN

Address: Operational Base + offset (0x0158)

Flash Timing Control Register For Synchronous Timing

Bit	Attr	Reset Value	Description
31:15	RO	0x0	reserved
14:9	RW	0x00	pst Write/Read Postamble time for ONFI synchronous mode or Toggle data mode. This field specifies the number of processor clock cycle for Postamb- le time.
8:3	RW	0x00	pre Write/Read Preamble time for ONFI synchronous mode or Toggle data mode. This field specifies the number of processor clock cycle for preamble time.
2:0	RW	0x0	fclk Half hclk cycle number for flash clock for ONFI synchronous mode or Toggle data mode

NANDC_MTRANS_STAT2

Address: Operational Base + offset (0x015c)

Bus Transfer Status Register2

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:0	RO	0x0000	bus_err2 Bus error indication for codeword16~31. [0] : bus error for codeword 16 [15] : bus error for codeword 31 Notes: Only active for master-mode.

NANDC_NANDC_VER

Address: Operational Base + offset (0x0160)

Nandc Version Register

Bit	Attr	Reset Value	Description
31:0	RO	0x56363232	version Version indication for NANDC

NANDC_LLPC_CTL

Address: Operational Base + offset (0x0164)

LLP Control Register

Bit	Attr	Reset Value	Description
31:6	RW	0x0000000	llp_loc Starting address for LLI0, 64byte align
5	RW	0x0	llp_frdy Working time for FOP_WAIT_FRDY for all FOP in first LLP group: 0: FOP_WAIT_FRDY begin working when started 1: FOP_WAIT_FRDY not begin working until 16 cycles later after started
4:3	RO	0x0	reserved
2	RW	0x0	llp_RST Reset signal for LLP. When asserted, it will auto cleared.
1	RW	0x0	llp_mode 0- current LLI only has FOP 1-current LLI has both CFG and FOP
0	RW	0x0	llp_en Enable signal for LLP 0-LLP disable 1-LLP enable

NANDC_LLPC_STAT

Address: Operational Base + offset (0x0168)

LLP Status Register

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	llp_stat latest LLI_LOC finished, 64byte align
5:2	RO	0x0	reserved
1	RO	0x0	llp_err error status for llp load or execute 0-llp is correct 1-llp is error
0	RO	0x1	llp_rdy ready status for all llp load 0-llp load is busy 1-llp load is ready

NANDC_INTEN

Address: Operational Base + offset (0x016c)

NandC Interrupt Enable Register

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:5	RO	0x0	reserved
4	RW	0x0	llp_int_en Enable for LLP finished interrupt. 0: interrupt disable 1: interrupt enable When llp_en_en is active, an interrupt is generated if LLP operation is finished
3	RW	0x0	bchfail_int_en Enable for bch fail interrupt. 0-interrupt disable 1-interrupt enable When bchfail_int_en is active, an interrupt is generated if bch decode failed
2	RW	0x0	bcherr_int_en Enable for bch error interrupt. 0-interrupt disable 1-interrupt enable When bcherr_int_en is active, an interrupt is generated if bch decode error bit is larger than bchthres(BCHCTL[26:19])
1	RW	0x0	frdy_int_en Enable for flash_rdy interrupt 0-interrupt disable 1-interrupt enable When frdy_int_en is active, an interrupt is generated if flash R/B# changes from 0 to 1
0	RW	0x0	dma_int_en Enable for internal DMA transfer finished interrupt 0-interrupt disable 1-interrupt enable When dma_int_en is active, an interrupt is generated if page_num(FLCTL[27:22]) of flash data transfer in DMA mode is finished

NANDC_INTCLR

Address: Operational Base + offset (0x0170)

NandC Interrupt Clear Register

Bit	Attr	Reset Value	Description
31:5	RO	0x0	reserved
4	RW	0x0	llp_int_clr Clear for LLP finished interrupt. When asserted, this bit will be auto cleared. 0: interrupt not cleared 1: interrupt cleared

Bit	Attr	Reset Value	Description
3	RW	0x0	bchfail_int_clr Clear for bch decode fail interrupt. When asserted, this bit will be auto cleared. 0-interrupt cleared 1-interrupt not cleared
2	RW	0x0	bcherr_int_clr Clear for bch error interrupt. When asserted, this bit will be auto cleared. 0-interrupt cleared 1-interrupt not cleared
1	RW	0x0	frdy_int_clr Clear for flash_rdy interrupt. When asserted, this bit will be auto cleared. 0-interrupt cleared 1-interrupt not cleared
0	RW	0x0	dma_int_clr Clear for internal DMA transfer finished interrupt. When asserted, this bit will be auto cleared. 0-interrupt cleared 1-interrupt not cleared

NANDC_INTST

Address: Operational Base + offset (0x0174)

NandC Interrupt Status Register

Bit	Attr	Reset Value	Description
31:5	RO	0x0	reserved
4	RO	0x0	llp_int_stat Status for LLP finished interrupt, high active
3	RO	0x0	bchfail_int_stat Status for bch decode fail interrupt, high active
2	RO	0x0	bcherr_int_stat Status for bch error interrupt, high active
1	RO	0x0	frdy_int_stat Status for flash_rdy interrupt, high active
0	RO	0x0	dma_int_stat Status for internal DMA transfer finished interrupt, high active

NANDC_SPARE0_0

Address: Operational Base + offset (0x0200)

System Information for codeword 0

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:24	RW	0xff	system_3 the 4th system byte of codeword 0
23:16	RW	0xff	system_2 the 3rd system byte of codeword 0
15:8	RW	0xff	system_1 the 2nd system byte of codeword 0
7:0	RW	0xff	system_0 the 1st system byte of codeword 0

NANDC_SPARE0_1

Address: Operational Base + offset (0x0204)

Spare Data and BCH Encode Information for codeword 0

Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH0_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH0_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
15:8	RW	0x00	BCH0_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH0_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE0_2

Address: Operational Base + offset (0x0208)

Spare Data and BCH Encode Information for codeword 0

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH0_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH0_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
15:8	RW	0x00	BCH0_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH0_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE0_3

Address: Operational Base + offset (0x020c)

Spare Data and BCH Encode Information for codeword 0

Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH0_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH0_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25

Bit	Attr	Reset Value	Description
15:8	RW	0x00	BCH0_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH0_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE0_4

Address: Operational Base + offset (0x0210)

Spare Data and BCH Encode Information for codeword 0

Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH0_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH0_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
15:8	RW	0x00	BCH0_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH0_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE0_5

Address: Operational Base + offset (0x0214)

Spare Data and BCH Encode Information for codeword 0

Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH0_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH0_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
15:8	RW	0x00	BCH0_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH0_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE0_6

Address: Operational Base + offset (0x0218)

Spare Data and BCH Encode Information for codeword 0

Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH0_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH0_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25

Bit	Attr	Reset Value	Description
15:8	RW	0x00	BCH0_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH0_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE0_7

Address: Operational Base + offset (0x021c)

Spare Data and BCH Encode Information for codeword 0

Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH0_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH0_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
15:8	RW	0x00	BCH0_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH0_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE0_8

Address: Operational Base + offset (0x0220)

Spare Data and BCH Encode Information for codeword 0

Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH0_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH0_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
15:8	RW	0x00	BCH0_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH0_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE0_9

Address: Operational Base + offset (0x0224)

Spare Data and BCH Encode Information for codeword 0

Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH0_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH0_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25

Bit	Attr	Reset Value	Description
15:8	RW	0x00	BCH0_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH0_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE0_10

Address: Operational Base + offset (0x0228)

Spare Data and BCH Encode Information for codeword 0

Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH0_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH0_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
15:8	RW	0x00	BCH0_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH0_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE0_11

Address: Operational Base + offset (0x022c)

Spare Data and BCH Encode Information for codeword 0

Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH0_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH0_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
15:8	RW	0x00	BCH0_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH0_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE1_0

Address: Operational Base + offset (0x0230)

System Information for codeword 1

Bit	Attr	Reset Value	Description
31:24	RW	0xff	system_3 the 4th system byte of codeword 1
23:16	RW	0xff	system_2 the 3rd system byte of codeword 1
15:8	RW	0xff	system_1 the 2nd system byte of codeword 1
7:0	RW	0xff	system_0 the 1st system byte of codeword 1

NANDC_SPARE1_1

Address: Operational Base + offset (0x0234)

Spare Data and BCH Encode Information for codeword 1

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH1_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH1_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
15:8	RW	0x00	BCH1_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH1_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE1_2

Address: Operational Base + offset (0x0238)

Spare Data and BCH Encode Information for codeword 1

Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH1_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH1_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25

Bit	Attr	Reset Value	Description
15:8	RW	0x00	BCH1_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH1_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE1_3

Address: Operational Base + offset (0x023c)

Spare Data and BCH Encode Information for codeword 1

Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH1_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH1_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
15:8	RW	0x00	BCH1_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH1_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE1_4

Address: Operational Base + offset (0x0240)

Spare Data and BCH Encode Information for codeword 1

Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH1_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH1_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
15:8	RW	0x00	BCH1_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH1_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE1_5

Address: Operational Base + offset (0x0244)

Spare Data and BCH Encode Information for codeword 1

Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH1_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH1_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25

Bit	Attr	Reset Value	Description
15:8	RW	0x00	BCH1_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH1_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE1_6

Address: Operational Base + offset (0x0248)

Spare Data and BCH Encode Information for codeword 1

Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH1_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH1_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
15:8	RW	0x00	BCH1_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH1_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE1_7

Address: Operational Base + offset (0x024c)

Spare Data and BCH Encode Information for codeword 1

Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH1_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH1_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
15:8	RW	0x00	BCH1_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH1_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE1_8

Address: Operational Base + offset (0x0250)

Spare Data and BCH Encode Information for codeword 1

Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH1_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH1_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25

Bit	Attr	Reset Value	Description
15:8	RW	0x00	BCH1_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH1_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE1_9

Address: Operational Base + offset (0x0254)

Spare Data and BCH Encode Information for codeword 1

Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH1_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH1_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
15:8	RW	0x00	BCH1_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH1_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE1_10

Address: Operational Base + offset (0x0258)

Spare Data and BCH Encode Information for codeword 1

Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH1_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH1_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
15:8	RW	0x00	BCH1_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH1_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE1_11

Address: Operational Base + offset (0x025c)

Spare Data and BCH Encode Information for codeword 1

Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH1_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH1_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25

Bit	Attr	Reset Value	Description
15:8	RW	0x00	BCH1_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH1_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE0_12

Address: Operational Base + offset (0x0260)

Spare Data and BCH Encode Information for codeword 0

Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH0_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH0_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
15:8	RW	0x00	BCH0_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH0_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE0_13

Address: Operational Base + offset (0x0264)

Spare Data and BCH Encode Information for codeword 0

Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH0_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH0_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
15:8	RW	0x00	BCH0_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH0_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE0_14

Address: Operational Base + offset (0x0268)

Spare Data and BCH Encode Information for codeword 0

Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH0_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH0_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25

Bit	Attr	Reset Value	Description
15:8	RW	0x00	BCH0_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH0_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE0_15

Address: Operational Base + offset (0x026c)

Spare Data and BCH Encode Information for codeword 0

Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH0_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH0_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
15:8	RW	0x00	BCH0_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH0_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE0_16

Address: Operational Base + offset (0x0270)

Spare Data and BCH Encode Information for codeword 0

Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH0_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH0_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
15:8	RW	0x00	BCH0_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH0_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE0_17

Address: Operational Base + offset (0x0274)

Spare Data and BCH Encode Information for codeword 0

Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH0_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH0_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25

Bit	Attr	Reset Value	Description
15:8	RW	0x00	BCH0_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH0_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE0_18

Address: Operational Base + offset (0x0278)

Spare Data and BCH Encode Information for codeword 0

Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH0_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH0_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
15:8	RW	0x00	BCH0_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH0_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE0_19

Address: Operational Base + offset (0x027c)

Spare Data and BCH Encode Information for codeword 0

Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH0_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH0_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
15:8	RW	0x00	BCH0_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH0_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE0_20

Address: Operational Base + offset (0x0280)

Spare Data and BCH Encode Information for codeword 0

Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH0_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH0_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25

Bit	Attr	Reset Value	Description
15:8	RW	0x00	BCH0_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH0_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE0_21

Address: Operational Base + offset (0x0284)

Spare Data and BCH Encode Information for codeword 0

Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH0_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH0_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
15:8	RW	0x00	BCH0_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH0_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE0_22

Address: Operational Base + offset (0x0288)

Spare Data and BCH Encode Information for codeword 0

Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH0_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH0_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
15:8	RW	0x00	BCH0_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH0_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE0_23

Address: Operational Base + offset (0x028c)

Spare Data and BCH Encode Information for codeword 0

Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH0_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH0_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25

Bit	Attr	Reset Value	Description
15:8	RW	0x00	BCH0_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH0_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE0_24

Address: Operational Base + offset (0x0290)

Spare Data and BCH Encode Information for codeword 0

Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH0_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH0_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
15:8	RW	0x00	BCH0_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH0_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE0_25

Address: Operational Base + offset (0x0294)

Spare Data and BCH Encode Information for codeword 0

Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH0_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH0_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
15:8	RW	0x00	BCH0_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH0_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE0_26

Address: Operational Base + offset (0x0298)

Spare Data and BCH Encode Information for codeword 0

Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH0_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH0_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25

Bit	Attr	Reset Value	Description
15:8	RW	0x00	BCH0_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH0_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE0_27

Address: Operational Base + offset (0x029c)

Spare Data and BCH Encode Information for codeword 0

Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH0_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH0_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
15:8	RW	0x00	BCH0_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH0_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE1_12

Address: Operational Base + offset (0x02a0)

Spare Data and BCH Encode Information for codeword 1

Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH1_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH1_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
15:8	RW	0x00	BCH1_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH1_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE1_13

Address: Operational Base + offset (0x02a4)

Spare Data and BCH Encode Information for codeword 1

Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH1_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH1_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25

Bit	Attr	Reset Value	Description
15:8	RW	0x00	BCH1_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH1_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE1_14

Address: Operational Base + offset (0x02a8)

Spare Data and BCH Encode Information for codeword 1

Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH1_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH1_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
15:8	RW	0x00	BCH1_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH1_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE1_15

Address: Operational Base + offset (0x02ac)

Spare Data and BCH Encode Information for codeword 1

Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH1_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH1_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
15:8	RW	0x00	BCH1_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH1_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE1_16

Address: Operational Base + offset (0x02b0)

Spare Data and BCH Encode Information for codeword 1

Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH1_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH1_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25

Bit	Attr	Reset Value	Description
15:8	RW	0x00	BCH1_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH1_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE1_17

Address: Operational Base + offset (0x02b4)

Spare Data and BCH Encode Information for codeword 1

Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH1_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH1_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
15:8	RW	0x00	BCH1_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH1_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE1_18

Address: Operational Base + offset (0x02b8)

Spare Data and BCH Encode Information for codeword 1

Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH1_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH1_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
15:8	RW	0x00	BCH1_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH1_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE1_19

Address: Operational Base + offset (0x02bc)

Spare Data and BCH Encode Information for codeword 1

Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH1_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH1_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25

Bit	Attr	Reset Value	Description
15:8	RW	0x00	BCH1_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH1_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE1_20

Address: Operational Base + offset (0x02c0)

Spare Data and BCH Encode Information for codeword 1

Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH1_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH1_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
15:8	RW	0x00	BCH1_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH1_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE1_21

Address: Operational Base + offset (0x02c4)

Spare Data and BCH Encode Information for codeword 1

Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH1_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH1_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
15:8	RW	0x00	BCH1_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH1_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE1_22

Address: Operational Base + offset (0x02c8)

Spare Data and BCH Encode Information for codeword 1

Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH1_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH1_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25

Bit	Attr	Reset Value	Description
15:8	RW	0x00	BCH1_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH1_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE1_23

Address: Operational Base + offset (0x02cc)

Spare Data and BCH Encode Information for codeword 1

Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH1_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH1_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
15:8	RW	0x00	BCH1_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH1_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE1_24

Address: Operational Base + offset (0x02d0)

Spare Data and BCH Encode Information for codeword 1

Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH1_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH1_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
15:8	RW	0x00	BCH1_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH1_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE1_25

Address: Operational Base + offset (0x02d4)

Spare Data and BCH Encode Information for codeword 1

Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH1_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH1_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25

Bit	Attr	Reset Value	Description
15:8	RW	0x00	BCH1_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH1_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE1_26

Address: Operational Base + offset (0x02d8)

Spare Data and BCH Encode Information for codeword 1

Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH1_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH1_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
15:8	RW	0x00	BCH1_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH1_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE1_27

Address: Operational Base + offset (0x02dc)

Spare Data and BCH Encode Information for codeword 1

Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH1_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH1_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
15:8	RW	0x00	BCH1_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH1_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_BCHDE0_24

Address: Operational Base + offset (0x0400)

BCH decode result of 24th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_24 decode result of 24th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_25

Address: Operational Base + offset (0x0404)

BCH decode result of 25th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved

Bit	Attr	Reset Value	Description
18:0	RO	0x00000	bchde0_25 decode result of 25th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_26

Address: Operational Base + offset (0x0408)

BCH decode result of 26th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_26 decode result of 26th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_27

Address: Operational Base + offset (0x040c)

BCH decode result of 27th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_27 decode result of 27th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_28

Address: Operational Base + offset (0x0410)

BCH decode result of 28th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_28 decode result of 28th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_29

Address: Operational Base + offset (0x0414)
 BCH decode result of 29th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_29 decode result of 29th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_30

Address: Operational Base + offset (0x0418)
 BCH decode result of 30th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_30 decode result of 30th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_31

Address: Operational Base + offset (0x041c)
 BCH decode result of 31th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_31 decode result of 31th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_32

Address: Operational Base + offset (0x0420)
 BCH decode result of 32th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_3 decode result of 3th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_33

Address: Operational Base + offset (0x0424)

BCH decode result of 33th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_33 decode result of 33th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_34

Address: Operational Base + offset (0x0428)

BCH decode result of 34th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_34 decode result of 34th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_35

Address: Operational Base + offset (0x042c)

BCH decode result of 35th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_35 decode result of 35th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_36

Address: Operational Base + offset (0x0430)

BCH decode result of 36th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved

Bit	Attr	Reset Value	Description
18:0	RO	0x00000	bchde0_36 decode result of 36th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_37

Address: Operational Base + offset (0x0434)

BCH decode result of 37th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_37 decode result of 37th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_38

Address: Operational Base + offset (0x0438)

BCH decode result of 38th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_38 decode result of 38th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_39

Address: Operational Base + offset (0x043c)

BCH decode result of 39th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_39 decode result of 39th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_40

Address: Operational Base + offset (0x0440)
 BCH decode result of 40th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_40 decode result of 40th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_41

Address: Operational Base + offset (0x0444)
 BCH decode result of 41th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_41 decode result of 41th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_42

Address: Operational Base + offset (0x0448)
 BCH decode result of 42th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_42 decode result of 4th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_43

Address: Operational Base + offset (0x044c)
 BCH decode result of 43th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_43 decode result of 43th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_44

Address: Operational Base + offset (0x0450)

BCH decode result of 44th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_44 decode result of 44th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_45

Address: Operational Base + offset (0x0454)

BCH decode result of 45th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_45 decode result of 45th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_46

Address: Operational Base + offset (0x0458)

BCH decode result of 46th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_46 decode result of 46th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_47

Address: Operational Base + offset (0x045c)

BCH decode result of 47th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved

Bit	Attr	Reset Value	Description
18:0	RO	0x00000	bchde0_47 decode result of 47th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_48

Address: Operational Base + offset (0x0460)

BCH decode result of 48th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_48 decode result of 48th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_49

Address: Operational Base + offset (0x0464)

BCH decode result of 49th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_49 decode result of 49th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_50

Address: Operational Base + offset (0x0468)

BCH decode result of 50th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_50 decode result of 50th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_51

Address: Operational Base + offset (0x046c)
 BCH decode result of 51th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_51 decode result of 51th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_52

Address: Operational Base + offset (0x0470)
 BCH decode result of 52th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_52 decode result of 52th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_53

Address: Operational Base + offset (0x0474)
 BCH decode result of 53th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_53 decode result of 53th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_54

Address: Operational Base + offset (0x0478)
 BCH decode result of 54th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_54 decode result of 54th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_55

Address: Operational Base + offset (0x047c)

BCH decode result of 55th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_55 decode result of 55th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_56

Address: Operational Base + offset (0x0480)

BCH decode result of 56th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_56 decode result of 56th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_57

Address: Operational Base + offset (0x0484)

BCH decode result of 57th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_57 decode result of 57th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_58

Address: Operational Base + offset (0x0488)

BCH decode result of 58th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved

Bit	Attr	Reset Value	Description
18:0	RO	0x00000	bchde0_58 decode result of 58th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_59

Address: Operational Base + offset (0x048c)

BCH decode result of 59th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_59 decode result of 59th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE1_24

Address: Operational Base + offset (0x0490)

BCH decode result of 24th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_24 decode result of 24th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_25

Address: Operational Base + offset (0x0494)

BCH decode result of 25th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_25 decode result of 25th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_26

Address: Operational Base + offset (0x0498)
 BCH decode result of 26th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_26 decode result of 26th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_27

Address: Operational Base + offset (0x049c)
 BCH decode result of 27th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_27 decode result of 27th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_28

Address: Operational Base + offset (0x04a0)
 BCH decode result of 28th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_28 decode result of 28th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_29

Address: Operational Base + offset (0x04a4)
 BCH decode result of 29th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_29 decode result of 2th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_30

Address: Operational Base + offset (0x04a8)

BCH decode result of 30th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_30 decode result of 30th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_31

Address: Operational Base + offset (0x04ac)

BCH decode result of 31th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_31 decode result of 31th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_32

Address: Operational Base + offset (0x04b0)

BCH decode result of 32th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_32 decode result of 32th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_33

Address: Operational Base + offset (0x04b4)

BCH decode result of 33th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved

Bit	Attr	Reset Value	Description
18:0	RO	0x00000	bchde1_33 decode result of 33th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_34

Address: Operational Base + offset (0x04b8)

BCH decode result of 34th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_34 decode result of 34th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_35

Address: Operational Base + offset (0x04bc)

BCH decode result of 35th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_35 decode result of 35th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_36

Address: Operational Base + offset (0x04c0)

BCH decode result of 36th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_36 decode result of 36th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_37

Address: Operational Base + offset (0x04c4)
 BCH decode result of 37th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_37 decode result of 37th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_38

Address: Operational Base + offset (0x04c8)
 BCH decode result of 38th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_38 decode result of 38th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_39

Address: Operational Base + offset (0x04cc)
 BCH decode result of 39th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_39 decode result of 39th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_40

Address: Operational Base + offset (0x04d0)
 BCH decode result of 40th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_40 decode result of 40th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_41

Address: Operational Base + offset (0x04d4)

BCH decode result of 41th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_41 decode result of 41th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_42

Address: Operational Base + offset (0x04d8)

BCH decode result of 42th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_42 decode result of 42th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_43

Address: Operational Base + offset (0x04dc)

BCH decode result of 43th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_43 decode result of 43th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_44

Address: Operational Base + offset (0x04e0)

BCH decode result of 44th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved

Bit	Attr	Reset Value	Description
18:0	RO	0x00000	bchde1_44 decode result of 44th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_45

Address: Operational Base + offset (0x04e4)

BCH decode result of 45th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_45 decode result of 45th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_46

Address: Operational Base + offset (0x04e8)

BCH decode result of 46th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_46 decode result of 46th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_47

Address: Operational Base + offset (0x04ec)

BCH decode result of 47th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_47 decode result of 47th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_48

Address: Operational Base + offset (0x04f0)
 BCH decode result of 48th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_48 decode result of 48th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_49

Address: Operational Base + offset (0x04f4)
 BCH decode result of 49th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_49 decode result of 49th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_50

Address: Operational Base + offset (0x04f8)
 BCH decode result of 50th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_50 decode result of 50th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_51

Address: Operational Base + offset (0x04fc)
 BCH decode result of 51th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_51 decode result of 51th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_52

Address: Operational Base + offset (0x0500)

BCH decode result of 52th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_52 decode result of 52th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_53

Address: Operational Base + offset (0x0504)

BCH decode result of 53th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_53 decode result of 53th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_54

Address: Operational Base + offset (0x0508)

BCH decode result of 54th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_54 decode result of 54th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_55

Address: Operational Base + offset (0x050c)

BCH decode result of 55th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved

Bit	Attr	Reset Value	Description
18:0	RO	0x00000	bchde1_55 decode result of 55th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_56

Address: Operational Base + offset (0x0510)

BCH decode result of 56th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_56 decode result of 56th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_57

Address: Operational Base + offset (0x0514)

BCH decode result of 57th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_57 decode result of 57th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_58

Address: Operational Base + offset (0x0518)

BCH decode result of 58th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_58 decode result of 58th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_59

Address: Operational Base + offset (0x051c)
 BCH decode result of 59th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_59 decode result of 59th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHST8

Address: Operational Base + offset (0x0520)

BCH Status Register For Codeword 16~17

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	bchst_cwd16_cwd17 BCHST information for 16th and 17th backup codeword. Bit assignment is similar to BCHST1 register. For more description, please refer to BCHST1 register.

NANDC_BCHST9

Address: Operational Base + offset (0x0524)

BCH Status Register For Codeword 18~19

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	bchst_cwd18_cwd19 BCHST information for 18th and 19th backup codeword. Bit assignment is similar to BCHST1 register. For more description, please refer to BCHST1 register.

NANDC_BCHST10

Address: Operational Base + offset (0x0528)

BCH Status Register For Codeword 20~21

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	bchst_cwd20_cwd21 BCHST information for 20th and 21th backup codeword. Bit assignment is similar to BCHST1 register. For more description, please refer to BCHST1 register.

NANDC_BCHST11

Address: Operational Base + offset (0x052c)

BCH Status Register For Codeword 22~23

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	bchst_cwd22_cwd23 BCHST information for 22th and 23th backup codeword. Bit assignment is similar to BCHST1 register. For more description, please refer to BCHST1 register.

NANDC_BCHST12

Address: Operational Base + offset (0x0530)

BCH Status Register For Codeword 24~25

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	bchst_cwd24_cwd25 BCHST information for 24th and 25th backup codeword. Bit assignment is similar to BCHST1 register. For more description, please refer to BCHST1 register.

NANDC_BCHST13

Address: Operational Base + offset (0x0534)

BCH Status Register For Codeword 26~27

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	bchst_cwd26_cwd27 BCHST information for 26th and 27th backup codeword. Bit assignment is similar to BCHST1 register. For more description, please refer to BCHST1 register.

NANDC_BCHST14

Address: Operational Base + offset (0x0538)

BCH Status Register For Codeword 28~29

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	bchst_cwd28_cwd29 BCHST information for 28th and 29th backup codeword. Bit assignment is similar to BCHST1 register. For more description, please refer to BCHST1 register.

NANDC_BCHST15

Address: Operational Base + offset (0x053c)

BCH Status Register For Codeword 30~31

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	bchst_cwd30_cwd31 BCHST information for 30th and 31th backup codeword. Bit assignment is similar to BCHST1 register. For more description, please refer to BCHST1 register.

NANDC_RANDMZ_SEED13_0

Address: Operational Base + offset (0x0600)

Seed 0 for Toshiba 13 Power Polynomial Randomizer

Bit	Attr	Reset Value	Description
31:13	RO	0x0	reserved
12:0	RW	0x0000	randmz_seed13_0 The seed for randomizer(initial value);

NANDC_RANDMZ_SEED13_1

Address: Operational Base + offset (0x0604)

Seed 1 for Toshiba 13 Power Polynomial Randomizer

Bit	Attr	Reset Value	Description
31:13	RO	0x0	reserved
12:0	RW	0x0000	randmz_seed13_1 The seed for randomizer(initial value);

NANDC_RANDMZ_SEED13_2

Address: Operational Base + offset (0x0608)

Seed 2 for Toshiba 13 Power Polynomial Randomizer

Bit	Attr	Reset Value	Description
31:13	RO	0x0	reserved
12:0	RW	0x0000	randmz_seed13_2 The seed for randomizer(initial value);

NANDC_RANDMZ_SEED13_3

Address: Operational Base + offset (0x060c)

Seed 3 for Toshiba 13 Power Polynomial Randomizer

Bit	Attr	Reset Value	Description
31:13	RO	0x0	reserved
12:0	RW	0x0000	randmz_seed13_3 The seed for randomizer(initial value);

NANDC_RANDMZ_SEED13_4

Address: Operational Base + offset (0x0610)

Seed 4 for Toshiba 13 Power Polynomial Randomizer

Bit	Attr	Reset Value	Description
31:13	RO	0x0	reserved

Bit	Attr	Reset Value	Description
12:0	RW	0x0000	randmz_seed13_4 The seed for randomizer(initial value);

NANDC_RANDMZ_SEED13_5

Address: Operational Base + offset (0x0614)

Seed 5 for Toshiba 13 Power Polynomial Randomizer

Bit	Attr	Reset Value	Description
31:13	RO	0x0	reserved
12:0	RW	0x0000	randmz_seed13_5 The seed for randomizer(initial value);

NANDC_RANDMZ_SEED13_6

Address: Operational Base + offset (0x0618)

Seed 6 for Toshiba 13 Power Polynomial Randomizer

Bit	Attr	Reset Value	Description
31:13	RO	0x0	reserved
12:0	RW	0x0000	randmz_seed13_6 The seed for randomizer(initial value);

NANDC_RANDMZ_SEED13_7

Address: Operational Base + offset (0x061c)

Seed 7 for Toshiba 13 Power Polynomial Randomizer

Bit	Attr	Reset Value	Description
31:13	RO	0x0	reserved
12:0	RW	0x0000	randmz_seed13_7 The seed for randomizer(initial value);

NANDC_RANDMZ_SEED13_8

Address: Operational Base + offset (0x0620)

Seed 8 for Toshiba 13 Power Polynomial Randomizer

Bit	Attr	Reset Value	Description
31:13	RO	0x0	reserved
12:0	RW	0x0000	randmz_seed13_8 The seed for randomizer(initial value);

NANDC_RANDMZ_SEED13_9

Address: Operational Base + offset (0x0624)

Seed 9 for Toshiba 13 Power Polynomial Randomizer

Bit	Attr	Reset Value	Description
31:13	RO	0x0	reserved
12:0	RW	0x0000	randmz_seed13_9 The seed for randomizer(initial value);

NANDC_RANDMZ_SEED13_10

Address: Operational Base + offset (0x0628)
Seed 10 for Toshiba 13 Power Polynomial Randomizer

Bit	Attr	Reset Value	Description
31:13	RO	0x0	reserved
12:0	RW	0x0000	randmz_seed13_10 The seed for randomizer(initial value);

NANDC_RANDMZ_SEED13_11

Address: Operational Base + offset (0x062c)
Seed 11 for Toshiba 13 Power Polynomial Randomizer

Bit	Attr	Reset Value	Description
31:13	RO	0x0	reserved
12:0	RW	0x0000	randmz_seed13_11 The seed for randomizer(initial value);

NANDC_RANDMZ_SEED13_12

Address: Operational Base + offset (0x0630)
Seed 12 for Toshiba 13 Power Polynomial Randomizer

Bit	Attr	Reset Value	Description
31:13	RO	0x0	reserved
12:0	RW	0x0000	randmz_seed13_12 The seed for randomizer(initial value);

NANDC_RANDMZ_SEED13_13

Address: Operational Base + offset (0x0634)
Seed 13 for Toshiba 13 Power Polynomial Randomizer

Bit	Attr	Reset Value	Description
31:13	RO	0x0	reserved
12:0	RW	0x0000	randmz_seed13_13 The seed for randomizer(initial value);

NANDC_RANDMZ_SEED13_14

Address: Operational Base + offset (0x0638)
Seed 14 for Toshiba 13 Power Polynomial Randomizer

Bit	Attr	Reset Value	Description
31:13	RO	0x0	reserved
12:0	RW	0x0000	randmz_seed13_14 The seed for randomizer(initial value);

NANDC_RANDMZ_SEED13_15

Address: Operational Base + offset (0x063c)
Seed 15 for Toshiba 13 Power Polynomial Randomizer

Bit	Attr	Reset Value	Description
31:13	RO	0x0	reserved

Bit	Attr	Reset Value	Description
12:0	RW	0x0000	randmz_seed13_15 The seed for randomizer(initial value);

NANDC_RANDMZ_SEED17_0

Address: Operational Base + offset (0x0640)

Seed 0 for Toshiba 17 Power Polynomial Randomizer

Bit	Attr	Reset Value	Description
31:17	RO	0x0	reserved
16:0	RW	0x00000	randmz_seed17_0 The seed for randomizer(initial value);

NANDC_RANDMZ_SEED17_1

Address: Operational Base + offset (0x0644)

Seed 1 for Toshiba 17 Power Polynomial Randomizer

Bit	Attr	Reset Value	Description
31:17	RO	0x0	reserved
16:0	RW	0x00000	randmz_seed17_1 The seed for randomizer(initial value);

NANDC_RANDMZ_SEED17_2

Address: Operational Base + offset (0x0648)

Seed 2 for Toshiba 17 Power Polynomial Randomizer

Bit	Attr	Reset Value	Description
31:17	RO	0x0	reserved
16:0	RW	0x00000	randmz_seed17_2 The seed for randomizer(initial value);

NANDC_RANDMZ_SEED17_3

Address: Operational Base + offset (0x064c)

Seed 3 for Toshiba 17 Power Polynomial Randomizer

Bit	Attr	Reset Value	Description
31:17	RO	0x0	reserved
16:0	RW	0x00000	randmz_seed17_3 The seed for randomizer(initial value);

NANDC_RANDMZ_SEED17_4

Address: Operational Base + offset (0x0650)

Seed 4 for Toshiba 17 Power Polynomial Randomizer

Bit	Attr	Reset Value	Description
31:17	RO	0x0	reserved
16:0	RW	0x00000	randmz_seed17_4 The seed for randomizer(initial value);

NANDC_RANDMZ_SEED17_5

Address: Operational Base + offset (0x0654)
 Seed 5 for Toshiba 17 Power Polynomial Randomizer

Bit	Attr	Reset Value	Description
31:17	RO	0x0	reserved
16:0	RW	0x00000	randmz_seed17_5 The seed for randomizer(initial value);

NANDC_RANDMZ_SEED17_6

Address: Operational Base + offset (0x0658)
 Seed 6 for Toshiba 17 Power Polynomial Randomizer

Bit	Attr	Reset Value	Description
31:17	RO	0x0	reserved
16:0	RW	0x00000	randmz_seed17_6 The seed for randomizer(initial value);

NANDC_RANDMZ_SEED17_7

Address: Operational Base + offset (0x065c)
 Seed 7 for Toshiba 17 Power Polynomial Randomizer

Bit	Attr	Reset Value	Description
31:17	RO	0x0	reserved
16:0	RW	0x00000	randmz_seed17_7 The seed for randomizer(initial value);

NANDC_RANDMZ_SEED17_8

Address: Operational Base + offset (0x0660)
 Seed 8 for Toshiba 17 Power Polynomial Randomizer

Bit	Attr	Reset Value	Description
31:17	RO	0x0	reserved
16:0	RW	0x00000	randmz_seed17_8 The seed for randomizer(initial value);

NANDC_RANDMZ_SEED17_9

Address: Operational Base + offset (0x0664)
 Seed 9 for Toshiba 17 Power Polynomial Randomizer

Bit	Attr	Reset Value	Description
31:17	RO	0x0	reserved
16:0	RW	0x00000	randmz_seed17_9 The seed for randomizer(initial value);

NANDC_RANDMZ_SEED17_10

Address: Operational Base + offset (0x0668)
 Seed 10 for Toshiba 17 Power Polynomial Randomizer

Bit	Attr	Reset Value	Description
31:17	RO	0x0	reserved

Bit	Attr	Reset Value	Description
16:0	RW	0x00000	randmz_seed17_10 The seed for randomizer(initial value);

NANDC_RANDMZ_SEED17_11

Address: Operational Base + offset (0x066c)

Seed 11 for Toshiba 17 Power Polynomial Randomizer

Bit	Attr	Reset Value	Description
31:17	RO	0x0	reserved
16:0	RW	0x00000	randmz_seed17_11 The seed for randomizer(initial value);

NANDC_RANDMZ_SEED17_12

Address: Operational Base + offset (0x0670)

Seed 12 for Toshiba 17 Power Polynomial Randomizer

Bit	Attr	Reset Value	Description
31:17	RO	0x0	reserved
16:0	RW	0x00000	randmz_seed17_12 The seed for randomizer(initial value);

NANDC_RANDMZ_SEED17_13

Address: Operational Base + offset (0x0674)

Seed 13 for Toshiba 17 Power Polynomial Randomizer

Bit	Attr	Reset Value	Description
31:17	RO	0x0	reserved
16:0	RW	0x00000	randmz_seed17_13 The seed for randomizer(initial value);

NANDC_RANDMZ_SEED17_14

Address: Operational Base + offset (0x0678)

Seed 14 for Toshiba 17 Power Polynomial Randomizer

Bit	Attr	Reset Value	Description
31:17	RO	0x0	reserved
16:0	RW	0x00000	randmz_seed17_14 The seed for randomizer(initial value);

NANDC_RANDMZ_SEED17_15

Address: Operational Base + offset (0x067c)

Seed 15 for Toshiba 17 Power Polynomial Randomizer

Bit	Attr	Reset Value	Description
31:17	RO	0x0	reserved
16:0	RW	0x00000	randmz_seed17_15 The seed for randomizer(initial value);

NANDC_RANDMZ_SEED19_0

Address: Operational Base + offset (0x0680)
 Seed 0 for Toshiba 19 Power Polynomial Randomizer

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RW	0x00000	randmz_seed19_0 The seed for randomizer(initial value);

NANDC_RANDMZ_SEED19_1

Address: Operational Base + offset (0x0684)
 Seed 1 for Toshiba 19 Power Polynomial Randomizer

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RW	0x00000	randmz_seed19_1 The seed for randomizer(initial value);

NANDC_RANDMZ_SEED19_2

Address: Operational Base + offset (0x0688)
 Seed 2 for Toshiba 19 Power Polynomial Randomizer

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RW	0x00000	randmz_seed19_2 The seed for randomizer(initial value);

NANDC_RANDMZ_SEED19_3

Address: Operational Base + offset (0x068c)
 Seed 3 for Toshiba 19 Power Polynomial Randomizer

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RW	0x00000	randmz_seed19_3 The seed for randomizer(initial value);

NANDC_RANDMZ_SEED19_4

Address: Operational Base + offset (0x0690)
 Seed 4 for Toshiba 19 Power Polynomial Randomizer

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RW	0x00000	randmz_seed19_4 The seed for randomizer(initial value);

NANDC_RANDMZ_SEED19_5

Address: Operational Base + offset (0x0694)
 Seed 5 for Toshiba 19 Power Polynomial Randomizer

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved

Bit	Attr	Reset Value	Description
18:0	RW	0x00000	randmz_seed19_5 The seed for randomizer(initial value);

NANDC_RANDMZ_SEED19_6

Address: Operational Base + offset (0x0698)

Seed 6 for Toshiba 19 Power Polynomial Randomizer

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RW	0x00000	randmz_seed19_6 The seed for randomizer(initial value);

NANDC_RANDMZ_SEED19_7

Address: Operational Base + offset (0x069c)

Seed 7 for Toshiba 19 Power Polynomial Randomizer

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RW	0x00000	randmz_seed19_7 The seed for randomizer(initial value);

NANDC_RANDMZ_SEED19_8

Address: Operational Base + offset (0x06a0)

Seed 8 for Toshiba 19 Power Polynomial Randomizer

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RW	0x00000	randmz_seed19_8 The seed for randomizer(initial value);

NANDC_RANDMZ_SEED19_9

Address: Operational Base + offset (0x06a4)

Seed 9 for Toshiba 19 Power Polynomial Randomizer

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RW	0x00000	randmz_seed19_9 The seed for randomizer(initial value);

NANDC_RANDMZ_SEED19_10

Address: Operational Base + offset (0x06a8)

Seed 10 for Toshiba 19 Power Polynomial Randomizer

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RW	0x00000	randmz_seed19_10 The seed for randomizer(initial value);

NANDC_RANDMZ_SEED19_11

Address: Operational Base + offset (0x06ac)
 Seed 11 for Toshiba 19 Power Polynomial Randomizer

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RW	0x00000	randmz_seed19_11 The seed for randomizer(initial value);

NANDC_RANDMZ_SEED19_12

Address: Operational Base + offset (0x06b0)
 Seed 12 for Toshiba 19 Power Polynomial Randomizer

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RW	0x00000	randmz_seed19_12 The seed for randomizer(initial value);

NANDC_RANDMZ_SEED19_13

Address: Operational Base + offset (0x06b4)
 Seed 13 for Toshiba 19 Power Polynomial Randomizer

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RW	0x00000	randmz_seed19_13 The seed for randomizer(initial value);

NANDC_RANDMZ_SEED19_14

Address: Operational Base + offset (0x06b8)
 Seed 14 for Toshiba 19 Power Polynomial Randomizer

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RW	0x00000	randmz_seed19_14 The seed for randomizer(initial value);

NANDC_RANDMZ_SEED19_15

Address: Operational Base + offset (0x06bc)
 Seed 15 for Toshiba 19 Power Polynomial Randomizer

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RW	0x00000	randmz_seed19_15 The seed for randomizer(initial value);

NANDC_RANDMZ_SEED23_0

Address: Operational Base + offset (0x06c0)
 Seed 0 for Toshiba 23 Power Polynomial Randomizer

Bit	Attr	Reset Value	Description
31:23	RO	0x0	reserved

Bit	Attr	Reset Value	Description
22:0	RW	0x000000	randmz_seed23_0 The seed for randomizer(initial value);

NANDC_RANDMZ_SEED23_1

Address: Operational Base + offset (0x06c4)

Seed 1 for Toshiba 23 Power Polynomial Randomizer

Bit	Attr	Reset Value	Description
31:23	RO	0x0	reserved
22:0	RW	0x000000	randmz_seed23_1 The seed for randomizer(initial value);

NANDC_RANDMZ_SEED23_2

Address: Operational Base + offset (0x06c8)

Seed 2 for Toshiba 23 Power Polynomial Randomizer

Bit	Attr	Reset Value	Description
31:23	RO	0x0	reserved
22:0	RW	0x000000	randmz_seed23_2 The seed for randomizer(initial value);

NANDC_RANDMZ_SEED23_3

Address: Operational Base + offset (0x06cc)

Seed 3 for Toshiba 23 Power Polynomial Randomizer

Bit	Attr	Reset Value	Description
31:23	RO	0x0	reserved
22:0	RW	0x000000	randmz_seed23_3 The seed for randomizer(initial value);

NANDC_RANDMZ_SEED23_4

Address: Operational Base + offset (0x06d0)

Seed 4 for Toshiba 23 Power Polynomial Randomizer

Bit	Attr	Reset Value	Description
31:23	RO	0x0	reserved
22:0	RW	0x000000	randmz_seed23_4 The seed for randomizer(initial value);

NANDC_RANDMZ_SEED23_5

Address: Operational Base + offset (0x06d4)

Seed 5 for Toshiba 23 Power Polynomial Randomizer

Bit	Attr	Reset Value	Description
31:23	RO	0x0	reserved
22:0	RW	0x000000	randmz_seed23_5 The seed for randomizer(initial value);

NANDC_RANDMZ_SEED23_6

Address: Operational Base + offset (0x06d8)
 Seed 6 for Toshiba 23 Power Polynomial Randomizer

Bit	Attr	Reset Value	Description
31:23	RO	0x0	reserved
22:0	RW	0x000000	randmz_seed23_6 The seed for randomizer(initial value);

NANDC_RANDMZ_SEED23_7

Address: Operational Base + offset (0x06dc)
 Seed 7 for Toshiba 23 Power Polynomial Randomizer

Bit	Attr	Reset Value	Description
31:23	RO	0x0	reserved
22:0	RW	0x000000	randmz_seed23_7 The seed for randomizer(initial value);

NANDC_RANDMZ_SEED23_8

Address: Operational Base + offset (0x06e0)
 Seed 8 for Toshiba 23 Power Polynomial Randomizer

Bit	Attr	Reset Value	Description
31:23	RO	0x0	reserved
22:0	RW	0x000000	randmz_seed23_8 The seed for randomizer(initial value);

NANDC_RANDMZ_SEED23_9

Address: Operational Base + offset (0x06e4)
 Seed 9 for Toshiba 23 Power Polynomial Randomizer

Bit	Attr	Reset Value	Description
31:23	RO	0x0	reserved
22:0	RW	0x000000	randmz_seed23_9 The seed for randomizer(initial value);

NANDC_RANDMZ_SEED23_10

Address: Operational Base + offset (0x06e8)
 Seed 10 for Toshiba 23 Power Polynomial Randomizer

Bit	Attr	Reset Value	Description
31:23	RO	0x0	reserved
22:0	RW	0x000000	randmz_seed23_10 The seed for randomizer(initial value);

NANDC_RANDMZ_SEED23_11

Address: Operational Base + offset (0x06ec)
 Seed 11 for Toshiba 23 Power Polynomial Randomizer

Bit	Attr	Reset Value	Description
31:23	RO	0x0	reserved

Bit	Attr	Reset Value	Description
22:0	RW	0x000000	randmz_seed23_11 The seed for randomizer(initial value);

NANDC_RANDMZ_SEED23_12

Address: Operational Base + offset (0x06f0)

Seed 12 for Toshiba 23 Power Polynomial Randomizer

Bit	Attr	Reset Value	Description
31:23	RO	0x0	reserved
22:0	RW	0x000000	randmz_seed23_12 The seed for randomizer(initial value);

NANDC_RANDMZ_SEED23_13

Address: Operational Base + offset (0x06f4)

Seed 13 for Toshiba 23 Power Polynomial Randomizer

Bit	Attr	Reset Value	Description
31:23	RO	0x0	reserved
22:0	RW	0x000000	randmz_seed23_13 The seed for randomizer(initial value);

NANDC_RANDMZ_SEED23_14

Address: Operational Base + offset (0x06f8)

Seed 14 for Toshiba 23 Power Polynomial Randomizer

Bit	Attr	Reset Value	Description
31:23	RO	0x0	reserved
22:0	RW	0x000000	randmz_seed23_14 The seed for randomizer(initial value);

NANDC_RANDMZ_SEED23_15

Address: Operational Base + offset (0x06fc)

Seed 15 for Toshiba 23 Power Polynomial Randomizer

Bit	Attr	Reset Value	Description
31:23	RO	0x0	reserved
22:0	RW	0x000000	randmz_seed23_15 The seed for randomizer(initial value);

6.5 Interface Description

Table 6-2 NandC0 Interface Description

Module Pin	IO	Pad Name	IOMUX Setting
flash_wp	O	IO_FLASH0wp_EMMCpwen_FLASH 0gpio3b1	GPIO3B_IOMUX[3:2] = 2'b01
flash_ale	O	IO_FLASH0ale_FLASH0gpio3b3	GPIO3B_IOMUX[6]= 1'b1
flash_cle	O	IO_FLASH0cle_FLASH0gpio3b4	GPIO3B_IOMUX[8]= 1'b1

Module Pin	IO	Pad Name	IOMUX Setting
flash_wrn	O	IO_FLASH0wrn_FLASH0gpio3b5	GPIO3B_IOMUX[10]=1'b1
flash_rdn	O	IO_FLASH0rdn_FLASH0gpio3b2	GPIO3B_IOMUX[4]=1'b1
flash_dqs	I/O	IO_FLASH0dqs_EMMCclkout_FLASH0gpio3c2	GPIO3C_IOMUX[5:4]=2'b01
flash_rdy	I	IO_FLASH0rdy_FLASH0gpio3b0	GPIO3B_IOMUX[0]=1'b1
flash_csn0	O	IO_FLASH0csn0_FLASH0gpio3b6	GPIO3B_IOMUX[12]=1'b1
flash_csn1	O	IO_FLASH0csn1_FLASH0gpio3b7	GPIO3B_IOMUX[14]=1'b1
flash_csn2	O	IO_FLASH0csn2_EMMCCmd_FLASH0gpio3c0	GPIO3C_IOMUX[1:0]=2'b01
flash_csn3	O	IO_FLASH0csn3_EMMCrstnout_FLASH0gpio3c1	GPIO3C_IOMUX[3:2]=2'b01
flash_csn4	O	IO_FLASH1wp_HOSTckoutn_MACRxdv_FLASH0csn4_FLASH1gpio4a1	GPIO4AL_IOMUX[6:4]=3'b100
flash_csn5	O	IO_FLASH1rdn_HOSTdout8_MACRixer_FLASH0csn5_FLASH1gpio4a2	GPIO4AL_IOMUX[10:8]=3'b100
flash_csn6	O	IO_FLASH1ale_HOSTdout9_MACClk_FLASH0csn6_FLASH1gpio4a3	GPIO4AL_IOMUX[14:12]=3'b100
flash_csn7	O	IO_FLASH1cle_HOSTdout10_MACTxen_FLASH0csn7_FLASH1gpio4a4	GPIO4AH_IOMUX[2:0]=3'b100
flash_data0	I/O	IO_FLASH0data0_EMMCdata0_FLASH0gpio3a0	GPIO3A_IOMUX[1:0]=2'b01
flash_data1	I/O	IO_FLASH0data1_EMMCdata1_FLASH0gpio3a1	GPIO3A_IOMUX[3:2]=2'b01
flash_data2	I/O	IO_FLASH0data2_EMMCdata2_FLASH0gpio3a2	GPIO3A_IOMUX[5:4]=2'b01
flash_data3	I/O	IO_FLASH0data3_EMMCdata3_FLASH0gpio3a3	GPIO3A_IOMUX[7:6]=2'b01
flash_data4	I/O	IO_FLASH0data4_EMMCdata4_FLASH0gpio3a4	GPIO3A_IOMUX[9:8]=2'b01
flash_data5	I/O	IO_FLASH0data5_EMMCdata5_FLASH0gpio3a5	GPIO3A_IOMUX[11:10]=2'b01
flash_data6	I/O	IO_FLASH0data6_EMMCdata6_FLASH0gpio3a6	GPIO3A_IOMUX[13:12]=2'b01
flash_data7	I/O	IO_FLASH0data7_EMMCdata7_FLASH0gpio3a7	GPIO3A_IOMUX[15:14]=2'b01

Notes: I=input, O=output, I/O=input/output, bidirectional

Table 6-3 NandC1 Interface Description

Module Pin	IO	Pad Name	IOMUX Setting
flash_wp	O	IO_FLASH1wp_HOSTckoutn_MACRxdv_FLASH0csn4_FLASH1gpio4a1	GPIO4AL_IOMUX[2:0]=3'b001
flash_ale	O	IO_FLASH1ale_HOSTdout9_MACClk_FLASH0csn6_FLASH1gpio4a3	GPIO4AL_IOMUX[14:12]=3'b001
flash_cle	O	IO_FLASH1cle_HOSTdout10_MACTxen_FLASH0csn7_FLASH1gpio4a4	GPIO4AH_IOMUX[2:0]=3'b001
flash_wrn	O	IO_FLASH1wrn_HOSTdout11_MACmdio_FLASH1gpio4a5	GPIO4AH_IOMUX[5:4]=2'b01
flash_rdn	O	IO_FLASH1rdn_HOSTdout8_MACRixer_FLASH0csn5_FLASH1gpio4a2	GPIO4AL_IOMUX[10:8]=3'b001
flash_dqs	I/O	IO_FLASH1dqs_HOSTdout14_MAC	GPIO4BL_IOMUX[2:0]

Module Pin	IO	Pad Name	IOMUX Setting
		col_FLASH1csn3_FLASH1gpio4b0]= 3'b001
flash_rdy	I	IO_FLASH1rdy_HOSTckoutp_MAC mdc_FLASH1gpio4a0	GPIO4AL_IOMUX[1:0]]= 2'b01
flash_csn0	O	IO_FLASH1csn0_HOSTdout12_MA Crxclk_SDIO1cmd_FLASH1gpio4a6	GPIO4AH_IOMUX[10: 8]= 3'b001
flash_csn1	O	IO_FLASH1csn1_HOSTdout13_MA Ccrs_SDIO1clkout_FLASH1gpio4a7	GPIO4AH_IOMUX[14: 12]= 3'b001
flash_csn2	O	IO_FLASH1csn2_HOSTdout15_MA Ctxclk_SDIO1pwren_FLASH1gpio4 b1	GPIO4BL_IOMUX[6:4]]= 3'b001
flash_csn3	O	IO_FLASH1dqs_HOSTdout14_MAC col_FLASH1csn3_FLASH1gpio4b0	GPIO4BL_IOMUX[2:0]]= 3'b100
flash_data0	I/O	IO_FLASH1data0_HOSTdout0_MAC txd2_SDIO1data0_FLASH1gpio3d0	GPIO3DL_IOMUX[2:0]]= 3'b001
flash_data1	I/O	IO_FLASH1data1_HOSTdout1_MAC txd3_SDIO1data1_FLASH1gpio3d1	GPIO3DL_IOMUX[6:4]]= 3'b001
flash_data2	I/O	IO_FLASH1data2_HOSTdout2_MAC rx2_SDIO1data2_FLASH1gpio3d2	GPIO3DL_IOMUX[10: 8]= 3'b001
flash_data3	I/O	IO_FLASH1data3_HOSTdout3_MAC rx3_SDIO1data3_FLASH1gpio3d3	GPIO3DL_IOMUX[14: 12]= 3'b001
flash_data4	I/O	IO_FLASH1data4_HOSTdout4_MAC txd0_SDIO1detectn_FLASH1gpio3d 4	GPIO3DH_IOMUX[2:0]]= 3'b001
flash_data5	I/O	IO_FLASH1data5_HOSTdout5_MAC txd1_SDIO1wrprt_FLASH1gpio3d5	GPIO3DH_IOMUX[6:4]]= 3'b001
flash_data6	I/O	IO_FLASH1data6_HOSTdout6_MAC rx3_SDIO1bkpwr_FLASH1gpio3d6	GPIO3DH_IOMUX[10: 8]= 3'b001
flash_data7	I/O	IO_FLASH1data7_HOSTdout7_MAC rx3_SDIO1intn_FLASH1gpio3d7	GPIO3DH_IOMUX[14: 12]= 3'b001

Notes: I=input, O=output, I/O=input/output, bidirectional

Furthermore, different IOs are selected and connected to different flash interface, which is shown as follows.

Table 6-4 NandC Interface Connection

Module Pin	Direction	Flash Interface			
		Asyn8x	Asyn16x	ONFI	Toggle
flash_csn <i>i</i> (i=0~7)	O	✓	✓	✓	✓
flash_wp	O	✓	✓	✓	✓
flash_ale	O	✓	✓	✓	✓
flash_cle	O	✓	✓	✓	✓
flash_wrn	O	✓	✓	✓	✓
flash_rdn	O	✓	✓	✓	✓
flash_data[7:0]	I/O	✓	✓	✓	✓
flash_data[15:8]	I/O	-	✓	-	-
flash_dqs	I/O	-	-	✓	✓
flash_rdy	I	✓	✓	✓	✓

6.6 Application Notes

6.6.1 Clock Description

There are two clock domains in the NandC. One is hclk, and the other is nclk.

- AHB slave bus uses the hclk to configure the NandC registers.
- AHB master bus uses the hclk to transmit the data between the external memory and internal sram.
- NandC use nclk to transmit the data between the nand flash and internal sram.
- All the flash interface timing configuration is relative to the nclk.

6.6.2 BCHST/BCHLOC/BCHDE/SPARE Application

1. BCHST

There are 16 BCHST-registers in NandC to store 32 codeword's BCH decode status(bchst) information. Every register stores 2 codeword's bchst information except BCHST0, which not only includes bchst information, but also includes one bit for *bchrdy*.

Let *bchst_cwd0*~*bchst_cwd31* be the bchst information for 32 codewords. In BCHST-registers, the latest codeword's bchst is stored into *bchst_cwd0*, and the former is shifted into *bchst_cwd1*. That is, *bchst_cwd0*→*bchst_cwd1*→.....→*bchst_cwd31*. Therefore, for example, if 32 codewords are decoded, then *bchst_cwd0* is the bch decode status for codeword31, and *bchst_cwd31* is the bch decode status for codeword0.

```

bchst_cwd0 = {BCHST0[28],BCHST0[12:8],BCHST0[27],BCHST0[7:3],BCHST0[2:0]}
bchst_cwd1 = {BCHST0[30],BCHST0[25:21],BCHST0[29],BCHST0[20:16],BCHST0[15:13]}
bchst_cwd2 = {BCHST1[28],BCHST1[12:8],BCHST1[27],BCHST1[7:3],BCHST1[2:0]}
bchst_cwd3 = {BCHST1[30],BCHST1[25:21],BCHST1[29],BCHST1[20:16],BCHST1[15:13]}
bchst_cwd4 = {BCHST2[28],BCHST2[12:8] ,BCHST2[27],BCHST2[7:3],BCHST2[2:0]}
bchst_cwd5 = {BCHST2[30],BCHST2[25:21],BCHST2[29],BCHST2[20:16],BCHST2[15:13]}
bchst_cwd6 = {BCHST3[28],BCHST3[12:8] ,BCHST3[27],BCHST3[7:3],BCHST3[2:0]}
bchst_cwd7 = {BCHST3[30],BCHST3[25:21],BCHST3[29],BCHST3[20:16],BCHST3[15:13]}
bchst_cwd8 = {BCHST4[28],BCHST4[12:8] ,BCHST4[27],BCHST4[7:3],BCHST4[2:0]}
bchst_cwd9 = {BCHST4[30],BCHST4[25:21],BCHST4[29],BCHST4[20:16],BCHST4[15:13]}
bchst_cwd10 = {BCHST5[28],BCHST5[12:8] ,BCHST5[27],BCHST5[7:3],BCHST5[2:0]}
bchst_cwd11 = {BCHST5[30],BCHST5[25:21],BCHST5[29],BCHST5[20:16],BCHST5[15:13]}
bchst_cwd12 = {BCHST6[28],BCHST6[12:8] ,BCHST6[27],BCHST6[7:3],BCHST6[2:0]}
bchst_cwd13 = {BCHST6[30],BCHST6[25:21],BCHST6[29],BCHST6[20:16],BCHST6[15:13]}
bchst_cwd14 = {BCHST7[28],BCHST7[12:8] ,BCHST7[27],BCHST7[7:3],BCHST7[2:0]}
bchst_cwd15 = {BCHST7[30],BCHST7[25:21],BCHST7[29],BCHST7[20:16],BCHST7[15:13]}
bchst_cwd16 = {BCHST8[28],BCHST8[12:8],BCHST8[27],BCHST8[7:3],BCHST8[2:0]}
bchst_cwd17 = {BCHST8[30],BCHST8[25:21],BCHST8[29],BCHST8[20:16],BCHST8[15:13]}
bchst_cwd18 = {BCHST9[28],BCHST9[12:8],BCHST9[27],BCHST9[7:3],BCHST9[2:0]}
bchst_cwd19 = {BCHST9[30],BCHST9[25:21],BCHST9[29],BCHST9[20:16],BCHST9[15:13]}
bchst_cwd20 = {BCHST10[28],BCHST10[12:8] ,BCHST10[27],BCHST10[7:3],BCHST10[2:0]}
bchst_cwd21 = {BCHST10[30],BCHST10[25:21],BCHST10[29],BCHST10[20:16],BCHST10[15:13]}
bchst_cwd22 = {BCHST11[28],BCHST11[12:8] ,BCHST11[27],BCHST11[7:3],BCHST11[2:0]}
bchst_cwd23 = {BCHST11[30],BCHST11[25:21],BCHST11[29],BCHST11[20:16],BCHST11[15:13]}
bchst_cwd24 = {BCHST12[28],BCHST12[12:8] ,BCHST12[27],BCHST12[7:3],BCHST12[2:0]}
bchst_cwd25 = {BCHST12[30],BCHST12[25:21],BCHST12[29],BCHST12[20:16],BCHST12[15:13]}
bchst_cwd26 = {BCHST13[28],BCHST13[12:8] ,BCHST13[27],BCHST13[7:3],BCHST13[2:0]}
bchst_cwd27 = {BCHST13[30],BCHST13[25:21],BCHST13[29],BCHST13[20:16],BCHST13[15:13]}
bchst_cwd28 = {BCHST14[28],BCHST14[12:8] ,BCHST14[27],BCHST14[7:3],BCHST14[2:0]}

```

```
bchst_cwd29 =  
{BCHST14[30],BCHST14[25:21],BCHST14[29],BCHST14[20:16],BCHST14[15:13]}  
  
bchst_cwd30 = {BCHST15[28],BCHST15[12:8] ,BCHST15[27],BCHST15[7:3],BCHST15[2:0]}  
bchst_cwd31 =  
{BCHST15[30],BCHST15[25:21],BCHST15[29],BCHST15[20:16],BCHST15[15:13]}
```

2. BCHLOC

There are 7 BCHLOC-registers in NandC to store 32 codeword's bch decode location(bchloc) information.

Let bchloc_cwd0~bchloc_cwd31 be the bchloc information for the 32 codeword. In BCHLOC registers, the latest codeword's bchloc is stored into bchloc_cwd0, and the former is shifted into bchloc_cwd1. That is, bchloc_cwd0→bchloc_cwd1→.....→bchloc_cwd31. Therefore, for example, if 32 codeword are decoded, then bchloc_cwd0 is the bch decode status for codeword31, and bchloc_cwd31 is the bch decode status for codeword0.

```
bchloc_cwd0 = {BCHLOC6[0], BCHLOC0[4:0]}  
bchloc_cwd1 = {BCHLOC6[1], BCHLOC0[9:5]}  
bchloc_cwd2 = {BCHLOC6[2], BCHLOC0[14:10]}  
bchloc_cwd3 = {BCHLOC6[3], BCHLOC0[19:15]}  
bchloc_cwd4 = {BCHLOC6[4], BCHLOC0[24:20]}  
bchloc_cwd5 = {BCHLOC6[5], BCHLOC0[29:25]}  
bchloc_cwd6 = {BCHLOC6[6], BCHLOC1[4:0]}  
bchloc_cwd7 = {BCHLOC6[7], BCHLOC1[9:5]}  
bchloc_cwd8 = {BCHLOC6[8], BCHLOC1[14:10]}  
bchloc_cwd9 = {BCHLOC6[9], BCHLOC1[19:15]}  
bchloc_cwd10 = {BCHLOC6[10], BCHLOC1[24:20]}  
bchloc_cwd11 = {BCHLOC6[11], BCHLOC1[29:25]}  
bchloc_cwd12 = {BCHLOC6[12], BCHLOC2[4:0]}  
bchloc_cwd13 = {BCHLOC6[13], BCHLOC2[9:5]}  
bchloc_cwd14 = {BCHLOC6[14], BCHLOC2[14:10]}  
bchloc_cwd15 = {BCHLOC6[15], BCHLOC2[19:15]}  
bchloc_cwd16 = {BCHLOC6[16], BCHLOC2[24:20]}  
bchloc_cwd17 = {BCHLOC6[17], BCHLOC2[29:25]}  
bchloc_cwd18 = {BCHLOC6[18], BCHLOC3[4:0]}  
bchloc_cwd19 = {BCHLOC6[19], BCHLOC3[9:5]}  
bchloc_cwd20 = {BCHLOC6[20], BCHLOC3[14:10]}  
bchloc_cwd21 = {BCHLOC6[21], BCHLOC3[19:15]}  
bchloc_cwd22 = {BCHLOC6[22], BCHLOC3[24:20]}  
bchloc_cwd23 = {BCHLOC6[23], BCHLOC3[29:25]}  
bchloc_cwd24 = {BCHLOC6[24], BCHLOC4[4:0]}  
bchloc_cwd25 = {BCHLOC6[25], BCHLOC4[9:5]}
```

```
bchloc_cwd26 = {BCHLOC6[26], BCHLOC4[14:10]}\n\nbchloc_cwd27 = {BCHLOC6[27], BCHLOC4[19:15]}\n\nbchloc_cwd28 = {BCHLOC6[28], BCHLOC4[24:20]}\n\nbchloc_cwd29 = {BCHLOC6[29], BCHLOC4[29:25]}\n\nbchloc_cwd30 = {BCHLOC6[30], BCHLOC5[4:0]}\n\nbchloc_cwd31 = {BCHLOC6[31], BCHLOC5[9:5]}
```

3. BCHDE

BCHDE includes two register-groups, BCHDE0 and BCHDE1. Each group has 60 registers: BCHDE0_0~BCHDE0_59 and BCHDE1_0~BCHDE1_59. BCHDE0_n(n=0~59) is the decode information of the nth error bit for codeword in sram0, and BCHDE1_n(n=0~59) is the decode information of the nth error bit for codeword in sram1.

The needed number of BCHDE registers is determined by bchmode. That is:

- a. When 16bitBCH selected, BCHDEM_0 ~ BCHDEM_15 are available
- b. When 24bitBCH selected, BCHDEM_0 ~ BCHDEM_23 are available
- c. When 40bitBCH selected, BCHDEM_0 ~ BCHDEM_39 are available
- d. When 60bitBCH selected, BCHDEM_0 ~ BCHDEM_59 are available

4. SPARE

SPARE includes two register-groups, SPARE0 and SPARE1. Each group has 28 registers: SPARE0_0~SPARE0_27 and SPARE1_0~SPARE1_27.

When in bch encoding, SPARE0_0 stores system information for codeword in sram0, SPARE0_n(n=1~27) stores encode information for codeword in sram0; SPARE1_0 stores system information for codeword in sram1, SPARE1_n(n=1~27) stores encode information for codeword in sram1.

When in bch decoding, SPARE0_n(n=0~27) stores the spare data read from flash for codeword in sram0; SPARE1_n(n=0~27) stores the spare data read from flash for codeword in sram1.

The needed number of BCHDE registers is determined by bchmode. That is:

- a. When 16bitBCH selected, spare data=28bytes, SPAREm_0~SPAREm_7 are available
- b. When 24bitBCH selected, spare data=42bytes, SPAREm_0~SPAREm_10 and SPAREm_11[15:0] are available
- c. When 40bitBCH selected, spare data=70bytes, SPAREm_0~SPAREm_17 and SPAREm_18[15:0] are available
- d. When 60bitBCH selected, spare data=105bytes, SPAREm_0~SPAREm_26 and SPAREm_27[7:0] are available

6.6.3 Bus Mode Application

MTRANS_CFG[2] determines whether the data load/store between internal memory and external memory is through slave interface or master interface.

1. Slave Mode

When MTRANS_CFG[2]=0, slave is selected. i. e. , flash data load/store between internal memory and external memory is through slave interface by cpu or external DMA.

In this mode, software should store page data into internal memory and spare data into SPARE

registers before starting flash program operation; and should load page data from internal memory and spare data from SPARE registers after finishing flash read operation.

In this mode, MTRANS_CFG, MTRANS_SADDR0 and MTRANS_SADDR1 are unused. The transfer codeword number is determined by FLCTL[6:5], and the maximum number is 2.

The judgment condition for finishing data transfer is FLCTL[20]. When FLCTL[20] is high, it means that data transfer is finished.

2. Master Mode

When MTRANS_CFG[2]=1, master is selected. i. e. , flash data load/store between internal memory and external memory is through master interface.

In this mode, software should initialize page data and spare data into external memory, and set their addresses in MTRANS_SADDR0 and MTRANS_SADDR1 respectively before starting flash program operation. Similarly, software should configure MTRANS_SADDR0 and MTRANS_SADDR1 respectively before starting flash read operation and could read data from addresses in MTRANS_SADDR0 and MTRANS_SADDR1 after NandC transfer finish.

In this mode, MTRANS_CFG, MTRANS_SADDR0 and MTRANS_SADDR1 are used. The transfer codeword number is determined by FLCTL[26:22], and the maximum number is 16.

The judgment condition for finishing data transfer is FLCTL[20]. When FLCTL[20] is high, it means that data transmission is finished.

When MTRANS_CFG[2]=1, page data and spare data are stored in the continuous space of external memory respectively.

For page data, source address is named Saddr0, specified in MTRANS_SADDR0. The space can be divided into many continuous units, and the unit size(named PUnit) is 1024 bytes or 512 bytes determined by FLCTL[21] and FLCTL[11]:

- a. when FLCTL[11]=0, PUnit is always equal to 1024 bytes
- b. when FLCTL[11]=1 and FLCTL[21]=0, PUnit is equal to 1024 bytes
- c. when FLCTL[11]=1 and FLCTL[21]=1, PUnit is equal to 512 bytes

For spare data, source address is named Saddr1, specified in MTRANS_SADDR1. The space can be divided into many continuous units, and the unit size(named SUnit) is 64 bytes or 128 bytes determined by BCHCTL[18], FLCTL[11] and FLCTL[21]:

- a. When FLCTL[11]=0 and BCHCTL[18]=0, SUnit is equal to 64 bytes
- b. When FLCTL[11]=0 and BCHCTL[18]=1, SUnit is equal to 128 bytes
- c. When FLCTL[11]=1 and FLCTL[21]=0, SUnit is equal to 128 bytes
- d. When FLCTL[11]=1 and FLCTL[21]=1, SUnit is equal to 64 bytes

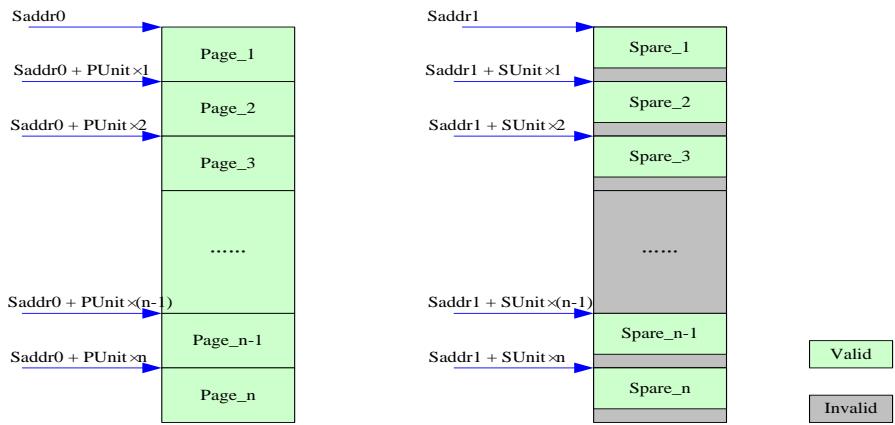


Fig. 6-2 NandC Address Assignment

The detailed format for page data and spare data in every unit is shown in following figures.

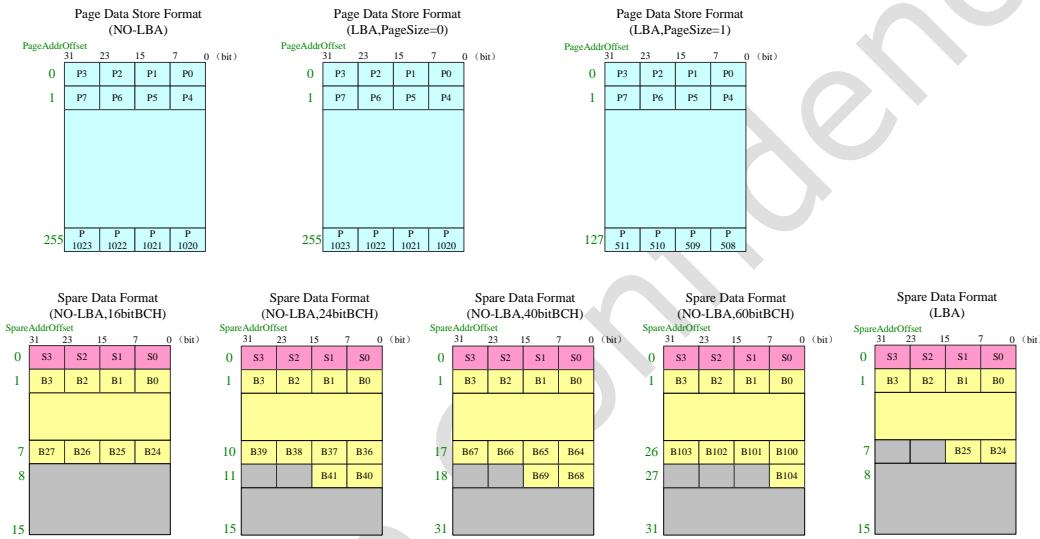


Fig. 6-3 NandC DataFormat

6.6.4 BchPage Application

BCHCTL[16] determines whether codeword size for page data is 1024 bytes or 512 bytes when FLCTL[11] is 0.

1. 1024bytes

When BCHCTL[16]=0, BchPage=0, hardware needs to write 1024 bytes page data and spare data into flash or read 1024 bytes page data and spare data from flash. All the 1024 bytes page data and spare data are encoded when writing or decoded when reading.

2. 512bytes

When BCHCTL[16]=1, BchPage=1, hardware needs to write 512 bytes page data and spare data into flash or read 512 bytes page data and spare data from flash.

In this mode, the page data unit size for BCH encoder and BCH decoder still is 1024byte. So to support BCH encoder and decoder, software should configure page data as follows: 1th~512th bytes are invalid data which must be stuffed with 0xff, 513th~1024th bytes are valid page data.

However, Randomizer function is not supported under this condition.

6.6.5 PageSize/SpareSize Application

FLCTL[21] determines whether the codeword size is 1024 bytes or 512 bytes when FLCTL[11]

is 1.

1. Big Page

When FLCTL[11]=0(LbaEn=0), the flash to be operated is Raw NAND Flash. Every codeword size is 1024 bytes and FLCTL[21] should always be set to 0, and the PageStep in external memory is 1024 bytes if bus mode is master mode.

At this mode, the spare size and SpareStep in external memory are determined by BCH Mode as follows:

BCH Mode=16bitBCH: spare size=(28+4)bytes , SpareStep=64bytes

BCH Mode=24bitBCH: spare size=(42+4)bytes , SpareStep=64bytes

BCH Mode=40bitBCH: spare size=(70+4)bytes , SpareStep=128bytes

BCH Mode=60bitBCH: spare size=(105+4)bytes, SpareStep=128bytes

2. Small Page

When FLCTL[11]=1, LbaEn=1, the flash to be operated is Managed NAND Flash. Every codeword size could be 1024 bytes or 512 bytes according to FLCTL[21]. If FLCTL[21]=0, codeword size is 1024 bytes, PageStep in external memory is 1024 bytes, and SpareStep is 128bytes. If FLCTL[21]=1, codeword size is 512 bytes, PageStep in external memory is 512 bytes, and SpareStep is 64 bytes.

At this mode, the spare size is configured in FLCTL[18:12], and the max available number is 109.

In the summary, the total data size in every codeword for flash or for software including page data and spare data, is determined by BCHCTL[16], FLCTL[11], FLCTL[21], BCHCTL[4], BCHCTL[18]. Their relationship is shown as follows.

Table 6-5 NandC Page/Spare size for flash

	page/spare size for software	page size /codeword	spare size /codeword
FLCTL[11]=0	16bitECC	1024 byte	(4+28)byte
	24bitECC	1024 byte	(4+42)byte
	40bitECC	1024 byte	(4+70)byte
	60bitECC	1024 byte	(4+105)byte
FLCTL[11]=1	FLCTL[21]=0	1024 byte	FLCTL[18:12]
	FLCTL[21]=1	512 byte	FLCTL[18:12]

Notes: that "page/spare size for flash" means that hardware should transfer these numbers of bytes in every codeword to or from flash.

6.6.6 Randomizer Application

RANDMZ_CFG[31] determines whether randomizer is enable or not. When RANDMZ_CFG[31] equals to 1, randomizer is active. Data should be scrambled before written into flash, and descrambled after read from flash.

RANDMZ_CFG[30:29] determines the randomizer polynomial.

When RANDMZ_CFG[30:29]=2'b00, Samsung randomizer, Polynomial = $1+x+x^{15}$. RANDMZ_CFG[14:0] is the seed for randomizer.

When RANDMZ_CFG[30:29]=2'b01, TOSHIBA randomizer. RANDMZ_CFG[19:0] is the seed agitation register for randomizer. RANDMZ_CFG[23:20] is the basic seed start point for every page. RANDMZ_CFG[28:24] is the basic seed rotation bits for every 16 page.

When RANDMZ_CFG[30:29]=2'b10, Samsung randomizer, Polynomial = $1+x^{14}+x^{15}$. RANDMZ_CFG[14:0] is the seed for randomizer.

The data unit for randomizer is one codeword(data+spare).

However, Randomizer is just available for data transfer by internal DMA mode, but not by forced bypass mode. Furthermore, it should not be enable if BCHCTL[16]=0 (BchPage=512bytes).

6.6.7 DLL Application

When Toggle Flash or ONFI Synchronous Flash interface is active, DLL should be used to adjust DQS input with DQ when reading flash.

There are 2 registers for DLL configuration(DLL_CFG_REG0 and DLL_CFG_REG1), and 1 register for DLL status(DLL_OBS_REG0).

The usage guide is as follows:

If bypass mode is used, you should set *dll_bypass* in DLL_CFG_REG1[1] to 1, and set *dll_dqs_dly_bypass* in DLL_CFG_REG0[23:16] to determine the dll element number needed. And then set *dll_start* in DLL_CFG_REG1[0] to 1 to start the DLL.

If auto adjusting is used, you should set *dll_bypass* in DLL_CFG_REG1[1] to 0, and set the *dll_start_point* in DLL_CFG_REG0[7:0] and *dll_incr* in DLL_CFG_REG1[11:4]. You also should set the adjusting mode *dll_qtren* in DLL_CFG_REG1[3:2] to compute the dll element number needed. If *dll_qtren*=2'b00, the dll element number is determined by *dll_dqs_dly* in DLL_CFG_REG0[15:8]; otherwise, it is 1/4 or 1/8 of the total number of dll elements used for *dll_qtren*=2'b01 or *dll_qtren*=2'b10 separately. The last step is to set *dll_start* in DLL_CFG_REG1[0] to 1 to start the DLL.

If you want to monitor the dll working status, you could read DLL_OBS_REG0. If DLL_OBS_REG0[0]=0, it means that DLL is not locked, and still in detecting status. Otherwise, it means that DLL is locked, and *dll_lock_value* in DLL_OBS_REG0[8:1] is the total number of dll elements used, *dll_dqs_delay_value* in DLL_OBS_REG0[16:9] is the total number of DQS delay used.

6.6.8 NandC Interrupt Application

NandC has 1 interrupt output signal and 4 interrupt sources: dma finish interrupt source, flash ready interrupt source, bch error interrupt source, bchfail interrupt source. When one or more of these interrupt source are enabled, NandC interrupt is asserted if one or more interrupt source is high. Software can determine the interrupt source by reading INTST and clear interrupt by writing corresponding bit in INTCLR.

6.6.9 LLP Application

LLP is used in NandC to store and execute instruction groups configured in external memory by software. When LLPCTL[0]=1, LLP is active, NandC will load instruction groups stored in {LLPCTL[31:6], 6'h0} and execute them. Next instruction groups should not be loaded until current instruction execution finished.

1. LLP Structure

The structure of LLP is shown as follows:

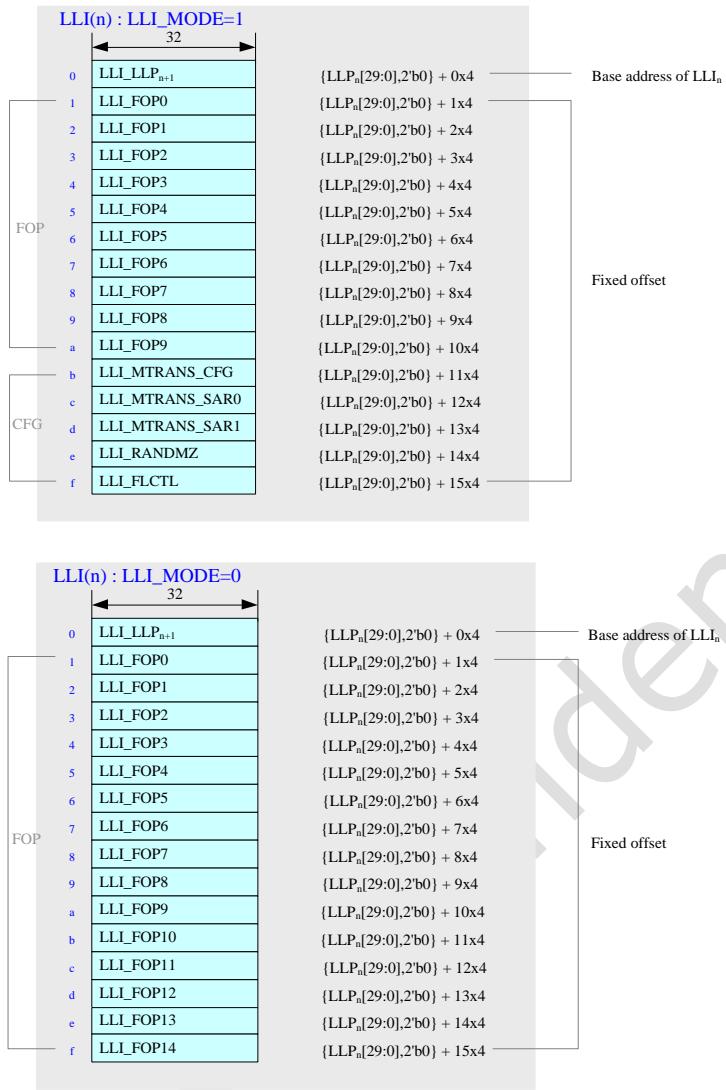


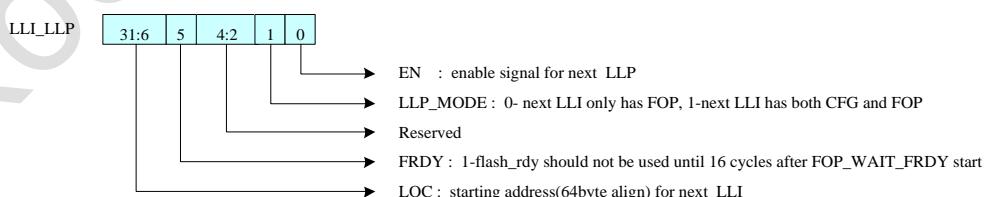
Fig. 6-4 NandC LLP Data Format

LLI_MODE is determined by LLPCTL[1]. If current operation is flash program or flash read, then LLI_MODE=1 is need; otherwise, LLI_MODE=0 is workable.

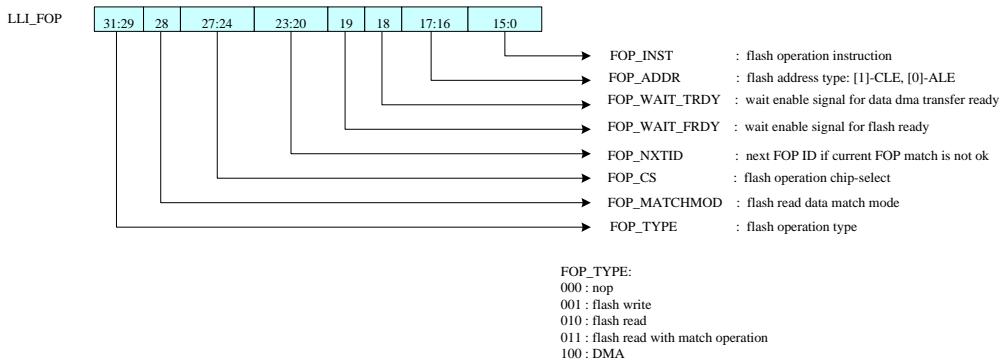
In addition, you could do more than one flash operation in one LLP group, but you should not separate one flash operation into two LLI groups.

2. LLI Format

a. LLI_LL_Pn+1 stores the address for next LLI group data



b. LLI_FOP0~LLI_FOP14 store the flash operation instruction



When FOP_TYPE=3'b011, match operation is active, and the PATTERN is LLI_FOP[15:0]. It is matched when "RDATA|PATTERN=PATTERN" with FOP_MATCHMOD=0, or when "RDATA&PATTERN=PATTERN" with FOP_MATCHMOD=1.

c. LLI_MTRANS_CFG/LLI_MTRANS_SADDR0/LLI_MTRANS_SADDR1/ LLI_RANDMZ/ LLI_FLCTL store the configuration for MTRANS_CFG/
MTRANS_SADDR0/MTRANS_SADDR1/RANDMZ/FLCTL.

3. LLP Working Mode

There are two working modes for LLP:

- Normal mode: LLPCTL[0] is kept to 1 until all LLP loading and executing finished. Software can monitor the progress by LLPSTAT[31:6], LLPSTAT[0].
- Pause mode: LLPCTL[0] is changed from 1 to 0 during LLP loading or LLP executing. NandC should not stop working until current LLP executing finished. Software can monitor the progress by LLPSTAT[31:6], LLPSTAT[0].

Chapter 7 Interconnect

7.1 Overview

The chip-level interconnect consists of main interconnect and peri interconnects. It enables communication among the modules and subsystems in the device.

The main interconnect supports the following features:

- Cross-bar exchange network
- A special internal slave for accessing the configuration register
- Little-endian platform
- Embedded memory scheduler for ddr transaction generation
- QoS management for optimizing the transaction flow
- Transaction statistics for analyzing the transaction flow
- Security protection mechanism to compatible with the TrustZone technology
- The peri interconnect belong to peripheral system which is responsible for peripheral devices control such as usb device, flash device, uart, spi etc.

7.2 Block Diagram

The interconnect comprises with:

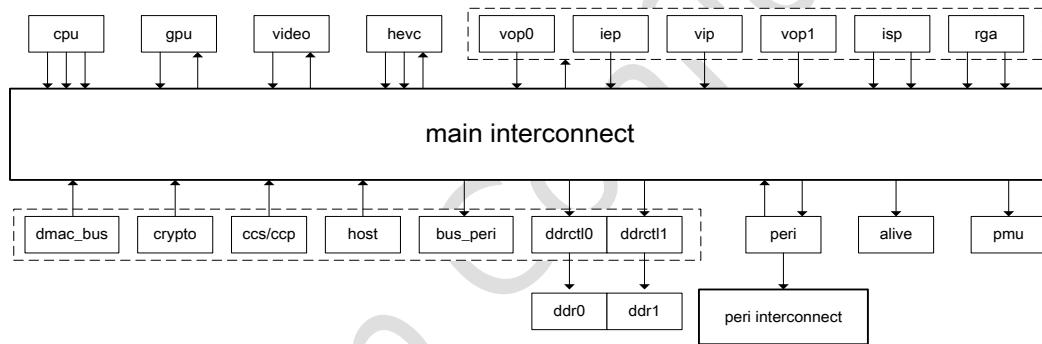


Fig. 7-1 Block Diagram

7.3 Function Description(main interconnect)

7.3.1 Master & Slave

The main interconnect is connected with all the related IPs of the system, the interface between the IP and the interconnect is called as NIU(native interface unit). All the connected NIU are list as bellowing:

Table 7-1 Master NIU

Master NIU	Description
cpup	Cortex-A17 AXI P port, access to any peripheral device
cpum	Cortex-A17 AXI M port , access to main memory
dbg	Jtag Debug master , access to any peripheral
bus_dmac	DMAC in pd_bus power domain
crypto	Crypto , used in trustzone technolgy

ccs	CCS, used in trustzone technology
ccp	CCP, used in trustzone technology
gpu	Mali-T760 of pd_gpu power domain
hevc	HEVC of pd_hevc power domain
video	Video codec of pd_video power domain
vop_big	Lcdc full function of pd_vio power domain
iep	IEP of pd_vio power domain
vip	VIP of pd_vio power domain
vop_lit	Lcdc lite of pd_vio power domain
isp	ISP of pd_vio power domain
rga	RGA of pd_vio power domain
peri	Peri-bus of pd_peri power domain

Table 7-2 slave NIU

Slave NIU	Description
msch0	Memory scheduler channel-0 in pd_bus power domain
msch1	Memory scheduler channel-1 in pd_bus power domain
bus_ahb	Ahb slave in pd_bus power domain
imem	Internal memory in pd_bus power domain
bus_apb	Apb slave in pd_bus power domain
pmu_apb	Pmu apb slave in pd_pmu power domain
alive_apb	Alive apb slave in pd_alive power domain
vio_ahb	Vio ahb slave in pd_vio power domain
gevc_ahb	Hevc ahb slave in pd_hevc power domain
video_ahb	Video ahb slave in pd_video power domain
gpu_axi	Gpu axi slave in pd_gpu power domain
service_bus	Service module inside the interconnect in pd_bus power domain, used as register configuration
service_core	Service module in pd_core power domain
service_dmac	Service module in pd_bus power domain
service_gpu	Service module in pd_gpu power domain
service_hevc	Service module in pd_hevc power domain

service_peri	Service module in pd_peri power domain
service_vio	Service module in pd_vio power domain
service_video	Service module in pd_video power domain

7.3.2 Clock & Power domain

The interconnect is divided to several clock domain and power domain. Each domain contain different IPs.

The clock/power domain and IP combination is list as bellowing:

Table 7-3 Clock and Power domain

Clock domain	Clock	Power domain	IP
alive_clk_dm	alive_pclk	alive_pwr	CRU/PLL/GRF/GPIO/TIMER/WDT
bus_clk_dm	bus_aclk	bus_pwr	IMEM
	bus_hclk		I2S/SPDIF/CRYPTO
	bus_pclk		TIMER/PWM/I2C/UART/DMAC/PCTL
core_clk_dm	cpum_aclk/ cpup_aclk	core_pwr	Cortex-A17
gpu_clk_dm	gpu_aclk	gpu_pwr	Mali-T760
hevc_aclk_dm	hevc_aclk	hevc_pwr	HEVC
hevc_hclk_dm	hevc_hclk		
msch0_clk_dm	msch0_clk	bus_pwr	Memory scheduler 0
msch1_clk_dm	msch1_clk		Memory scheduler 1
peri_clk_dm	peri_aclk	peri_pwr	Peri-BUS
pmu_clk_dm	pmu_pclk	pmu_pwr	PMU/PMU_IMEM/SGRF/GPIO
video_aclk_dm	video_aclk	video_pwr	VCODEC
video_hclk_dm	video_hclk		
vio0_clk_dm	vio0_aclk	vio_pwr	VOP_BIG/IEP/VIP
vio01_clk_dm	vio1_aclk		ISP/VOP_LIT
vio2_clk_dm	vio2_aclk		RGA
vio_hclk_dm	vio_hclk		

7.3.3 QoS management

The interconnect offers 4 modes of qos management:

- None: QoSGenerator is disabled, and priority information are stuck at 0.
- Fixed: QoSGenerator drives applies a fixed urgency to read transactions, and a (possibly different) urgency to write transactions.
- Limiter: QoSGenerator behaves as in fixed mode, but limits the traffic bandwidth coming from that socket, possibly stalling requests if the initiator attempts to exceed its budget.

- Regulator: QoSGenerator promotes are demotes hurry, depending the bandwidth obtained by the initiator is below or beyond a bandwidth budget. As transactions exceeding the bandwidth limit are sent (even though demoted), the regulator mode may be considered as a softer version of the limiter mode.

Limiter Behavior

When configured in bandwidth limiter, the unit uses a 23 bit counter to measure the average bandwidth. This counter has a 1/256 byte resolution and works as follows:

- Adds the number of byte rounded up to 16 (1 -> 16) and then multiplied by 256 to the current value, each time a request is sent.
- Subtracts the Bandwidth register value every cycle. If the Counter becomes negative, force it to 0.
- If the Counter value is greater than the Saturation register value multiplied by 16*256, any incoming request is stalled until this condition disappears. Note that the Counter cannot wrap-around because the maximum value it can reach is: $\text{SaturationMax} \times 16 \times 256 + \text{BurstMax} \times 256 = 1023 \times 4K + 4K \times 256 = 5116K$ or $223 = 8192K$.

The following example will show the Counter behavior: 32 byte bursts, F=400MHz, BW=200MB/s, T=0.32us. The Bandwidth register will be set to $256 \times 200 / 400 = 128$, and the Saturation register to $128 \times 0.32 \times 400 / 4096 = 4$ (which corresponds to 64 bytes).

Regulator Behavior

When configured in bandwidth regulator, the unit uses a 23 bit counter to measure the average bandwidth. This counter has a 1/256 byte resolution and works as follows:

- Adds the number of byte rounded up to 16 and then multiplied by 256 to the current value, each time a response is received. If the result is greater than the Saturation register value multiplied by 16*256, saturation to this value is applied.
- Subtracts the Bandwidth register value every cycle. If the Counter becomes negative, force it to 0.
- If the Counter value is less than or equal to the Saturation register value multiplied by $16 \times 256 / 2$, the SocketMst Hurry signal will be set to the HurryHigh register, and HurryLow otherwise. Note that Urgency and Press will be also set to the same value.

The following example will show the Counter behavior: 1Kbyte bursts, F=500MHz, BW=2GB/s, T=2.048us. The Bandwidth register will be set to $256 \times 2000 / 500 = 1024$, and the Saturation register to $1024 \times 2.048 \times 500 / 4096 = 256$ (which corresponds to 4 Kbytes).

QoS Generator Programming

Bandwidth: This $\log_2(\text{socket.wData}/8)+8$ bits register defines the bandwidth in 1/256th byte per cycle unit. This allows a 2 MByte/s resolution at 500MHz. When the bandwidth is given in MByte/s, the value of this register will be equal to $256 \times \text{BWMB/s} / \text{FMHz}$.

Saturation: This 10 bits register defines the number of bytes used for bandwidth measurement. It is expressed in 16bytes unit (up to 16 Kbyte). Usually the integration window is given in us or in cycle: the value of this register will be equal to $\text{Bandwidth} \times \text{Tus} \times \text{FMHz} / (256 \times 16)$ or $\text{Bandwidth} \times \text{Ncycle} / (256 \times 16)$.

7.3.4 Memory Scheduler

Memory scheduler is a special NIU of the interconnect, it mainly deal with the transaction inside the interconnect and convert it to the transaction which the ddr protocol controller can

recognize.

There are two memory schedulers in the interconnect, each is in different clock domain. These two memory schedulers are totally equal in function .

Following table shows the software configurable setting for the memory scheduler when the system connected to different size of ddr device.

The DDRCONF[3:0] is a configurable register inside the interconnect.

R: indicates Row bits

B: indicates Bank bits

C: indicates Column bits

D: indicates Chip selects bits

Table 7-4 DDR configuration

DDR CONF[3:0]	
0	R DBBB RRRR RRRR RRRC CCCC CCCC C---
1	C RRRD RRRR RRRR RRRR RBBC CCCC CCCC C---
2	C RRDR RRRR RRRR RRRR RBBC CCCC CCCC C---
3	C RDRR RRRR RRRR RRRR RBBC CCCC CCCC C---
4	C DRDR RRRR RRRR RRRR RBBC CCCC CCCC C---
5	R RRDR RRRR RRRR RRRR BBBC CCCC CCCC C---
6	R RDRR RRRR RRRR RRRR BBBC CCCC CCCC C---
7	R DRRR RRRR RRRR RRRR BBBC CCCC CCCC C---
8	C CRRR DRRR RRRR RRRR RRBB BCCC CCCC C---
9	C CRRD RRRR RRRR RRRR RRBB BCCC CCCC C---
10	C CRDR RRRR RRRR RRRR RRBB BCCC CCCC C---
11	C CBRR DRRR RRRR RRRR RRRB BCCC CCCC C---
12	C RBRR DRRR RRRR RRRR RRBB CCCC CCCC C---
13	B RRRR DRRR RRRR RRRR RBBC CCCC CCCC C---
14	C DRBB BRDR RRRR RRRR RRRR CCCC CCCC C---
15	D RRRR RRRR RRRR RRRR BBBC CCCC CCCC C---

When access to the two memory schedulers, the interconnect supports different stride between the two memory schedulers. Because of this function, the transaction can be interleaved send to the two channel ddr devices.

The stride can be 0Bytes,128Bytes,256Bytes,512Bytes,4kBytes.

It support the following configuration:

Table 7-5 DDR Stride

DDR STRIDE[4:0]	Channel 0 Address range	Channel 1 Address range	Stride size	Total size
5'b0_0000	0x0--0x0fff_ffff	0x1000_0000--0x1fff_ffff	256MB	512MB
5'b0_0001	0x0--0x1ffff_ffff	0x2000_0000--0x3fff_ffff	512MB	1GB
5'b0_0010	0x0--0x3fff_ffff	0x4000_0000--0x7fff_ffff	1GB	2GB
5'b0_0011	0x0--0x7fff_ffff	0x8000_0000--0xffff_ffff	2GB	4GB
5'b0_0100	0x0--0x3fff_ffff	0x0--0x3fff_ffff	128B	1GB
5'b0_0101	0x0--0x3fff_ffff	0x0--0x3fff_ffff	256B	1GB
5'b0_0110	0x0--0x3fff_ffff	0x0--0x3fff_ffff	512B	1GB
5'b0_0111	0x0--0x3fff_ffff	0x0--0x3fff_ffff	4KB	1GB

DDR STRIDE[4:0]	Channel 0 Address range	Channel 1 Address range	Stride size	Total size
5'b0_1000	0x0--0x7fff_ffff	0x0--0x7fff_ffff	128B	2GB
5'b0_1001	0x0--0x7fff_ffff	0x0--0x7fff_ffff	256B	2GB
5'b0_1010	0x0--0x7fff_ffff	0x0--0x7fff_ffff	512B	2GB
5'b0_1011	0x0--0x7fff_ffff	0x0--0x7fff_ffff	4KB	2GB
5'b0_1100	0x0--0xffff_ffff	0x0--0xffff_ffff	128B	4GB
5'b0_1101	0x0--0xffff_ffff	0x0--0xffff_ffff	256B	4GB
5'b0_1110	0x0--0xffff_ffff	0x0--0xffff_ffff	512B	4GB
5'b0_1111	0x0--0xffff_ffff	0x0--0xffff_ffff	4KB	4GB
5'b1_0000	0x0-- 0x7fff_ffff	0x0-- 0x7fff_ffff	128B	3GB
	0x8000_0000-- 0xbfff_ffff	0x8000_0000-- 0xbfff_ffff	128B	
5'b1_0001	0x0-- 0x7fff_ffff	0x0-- 0x7fff_ffff	256B	3GB
	0x8000_0000-- 0xbfff_ffff	0x8000_0000-- 0xbfff_ffff	256B	
5'b1_0010	0x0-- 0x7fff_ffff	0x0-- 0x7fff_ffff	512B	3GB
	0x8000_0000-- 0xbfff_ffff	0x8000_0000-- 0xbfff_ffff	512B	
5'b1_0011	0x0-- 0x7fff_ffff	0x0-- 0x7fff_ffff	4KB	3GB
	0x8000_0000-- 0xbfff_ffff	0x8000_0000-- 0xbfff_ffff	4KB	
5'b1_0100	0x0-- 0x0fff_ffff	0x1000_0000-- 0x1fff_ffff	256MB	1GB
	0x2000_0000-- 0x3fff_ffff	0x2000_0000-- 0x3fff_ffff	128B	
5'b1_0101	0x0-- 0x1fff_ffff	0x2000_0000-- 0x3fff_ffff	512MB	2GB
	0x4000_0000-- 0x7fff_ffff	0x4000_0000-- 0x7fff_ffff	128B	
5'b1_0110	0x0--0xffff_ffff		4GB	4GB
5'b1_0111		0x0000_0000--0xffff_ffff	4GB	4GB
5'b1_1010	0x0-0xffff_ffff	0x1_0000_0000--0x1_ffff_ffff	4GB	8GB
5'b1_1011	0x0-0x1_ffff_ffff	0x0-0x1_ffff_ffff	128B	8GB

The following picture shows the address mapping from soc system to ddr device space, when configure the ddrstride=5'b01000 ,interleaved size as 128Bytes.

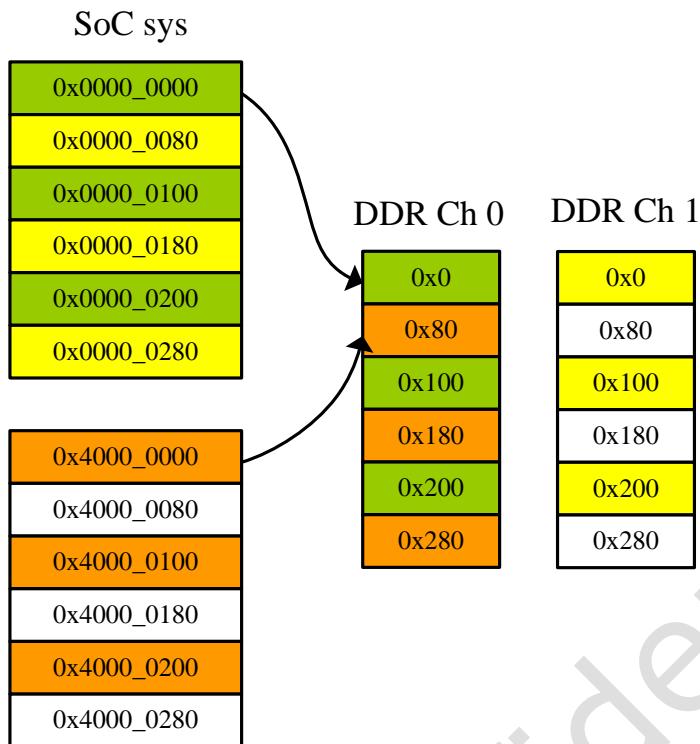


Fig. 7-2 DDR interleaved example

7.4 Register Description(main interconnect)

7.4.1 Internal Address Mapping

Table 7-6 Service module

Service Module	Base address
service_bus	0xffac_0000
service_core	0xffa8_0000
service_dmac	0xffa9_0000
service_gpu	0xffaa_0000
service_hevc	0xffaf_0000
service_peri	0xffab_0000
service_vio	0xffad_0000
service_video	0xffae_0000

Table 7-7 Service_bus block

Register block inside service_bus	Internal offset
msch0	0x0
msch0_cpum_probe	0x400
msch0_gpu_probe	0x800
msch0_obsrv	0x180
msch0_peri_probe	0xc00
msch0_video_probe	0x1000
msch0_vio0_probe	0x1400
msch0_vio1_probe	0x1800
msch0_vio2_probe	0x1c00
msch1	0x80
msch1_cpum_probe	0x2000
msch1_gpu_probe	0x2400
msch1_obsrv	0x200
msch1_peri_probe	0x2800
msch1_video_probe	0x2c00

Register block inside service_bus	Internal offset
msch1_vio0_probe	0x3000
msch1_vio1_probe	0x3400
msch1_vio2_probe	0x3800

Table 7-8 Service_core block

Register block inside service_core	Internal offset
cpum_r_qos	0x80
cpum_w_qos	0x100
cpup_qos	0x0

Table 7-9 Service_dmac block

Register block inside service_dmac	Internal offset
bus_dmac_qos	0x0
ccp_qos	0x180
crypto_qos	0x100
ccs_qos	0x200
host_qos	0x80

Table 7-10 Service_gpu block

Register block inside service_gpu	Internal offset
gpu_r_qos	0x0
gpu_w_qos	0x80

Table 7-11 Service_hevc block

Register block inside service_hevc	Internal offset
hevc_r_qos	0x0
hevc_w_qos	0x100

Table 7-12 Service_peri block

Register block inside service_peri	Internal offset
peri_qos	0x0

Table 7-13 Service_vio block

Register block inside service_vio	Internal offset
vio0_iep_qos	0x500
vio0_vip_qos	0x480
vio0_vop_qos	0x400
vio1_isp_r_qos	0x900
vio1_isp_w0_qos	0x100
vio1_isp_w1_qos	0x180
vio1_vop_qos	0x0
vio2_rga_r_qos	0x800
vio2_rga_w_qos	0x880

7.4.2 Registers Summary

service_bus: memory scheduler channel-0 register summary

Name	Offset	Size	Reset Value	Description
coreid	0x0000	W	0x21501602	core id of memory scheduler 0
revisionid	0x0004	W	0x0126f200	revisionid
ddrconf	0x0008	W	0x00000000	ddr configuration register
ddrtiming	0x000c	W	0x2475931c	ddr timing register
ddrmode	0x0010	W	0x00000000	ddr mode register

Name	Offset	Size	Reset Value	Description
readlatency	0x0014	W	0x00000032	read latency register
activate	0x0038	W	0x00000400	activate register
devtodev	0x003c	W	0x00000000	devtodev register

service_core: cpup_qos register summary

Name	Offset	Size	Reset Value	Description
priority	0x0008	W	0x00000101	priority register
mode	0x000c	W	0x00000003	qos mode register
bandwidth	0x0010	W	0x00000005	qos bandwidth register
saturation	0x0014	W	0x00000040	qos saturation register
extcontrol	0x0018	W	0x00000000	qos extcontrol register

Notes:**S**ize:**B**- Byte (8 bits) access, **H**W- Half WORD (16 bits) access, **W**-WORD (32 bits) access

service_bus:msch1's register is same with msch0

other master's qos register is same with service_core:cpup_qos

7.4.3 Detail Register Description

service_bus: memory scheduler channel-0 coreid

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:0	RO	0x21501602	msch0' core id

service_bus: memory scheduler channel-0 revisionid

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:0	RO	0x0126f200	msch0' revision id

service_bus: memory scheduler channel-0 ddrconf

Address: Operational Base + offset (0x0008)

Memory scheduler configuration register

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved
3:0	RW	0x0	DdrConf select the ddr rank,row,bank,col sequence

service_bus: memory scheduler channel-0 ddrtiming

Address: Operational Base + offset (0x000c)

Memory scheduler timing register

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31	RW	0x0	BwRatio Bandwidth determines , in conjunction with field BwRatioExtended of register ddrmode, the number of DRAM data bus cycles required to process a scheduler data bus word. When BwRatio and BwRatioExtended are set to 0, the bandwidth ratio is 1:1, that is one DRAM cycles per scheduler word. When BwRatio is set to 1, and BwRatioExtended is set to 0, the bandwidth ratio is 2:1, that is ,two DRAM cycles per scheduler word.
30:26	RW	0x00	WrToRd Minimum time between the last DRAM Write command and a Read command.
25:21	RW	0x00	RdToWr Minimum time between the last DRAM Read command and a Write command.
20:18	RW	0x0	BurstLen DRAM burst duration on the DRAM data bus. Also equal to minimum time between two DRAM commands.
17:12	RW	0x00	WrToMiss Minimum time between the last DRAM Write command and a new Read or Write command in another page of the same bank.
11:6	RW	0x00	RdToMiss Minimum time between the last DRAM Read command and a new Read or Write command in another page of the same bank.
5:0	RW	0x00	ActToAct Minimum time between two consecutive DRAM Activate commands on the same bank.

service_bus: memory scheduler channel-0 ddrmode

Address: Operational Base + offset (0x0010)

Memory scheduler mode register

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	RW	0x0	BwRatioExtended When 0, bandwidth ratio is determined by BwRatio. When 1, the bandwidth ratio is 4:1, that is four DRAM cycles per scheduler word, and BwRatio must be set to 0.

Bit	Attr	Reset Value	Description
0	RW	0x0	AutoPrecharge When set to 1, pages are automatically closed after each access(no page hit). When set to 0, pages are left open until an access in a different page occurs.

service_bus: memory scheduler channel-0 readlatency

Address: Operational Base + offset (0x0014)

Memory scheduler read latency register

Bit	Attr	Reset Value	Description
31:6	RO	0x0	reserved
7:0	RW	0x32	ReadLatency Stores a user-defined read response latency ceiling, expressed in scheduler clock cycles. When the scheduler determines that the latency of a read transaction to the controller exceeded this value, the scheduler stalls further transactions to reduce the number of commands in the memory controller queue.

service_bus: memory scheduler channel-0 activate

Address: Operational Base + offset (0x0038)

Memory scheduler activate register

Bit	Attr	Reset Value	Description
31:11	RO	0x0	reserved
10	RW	0x01	Fawbank Indicates the number of banks of a given device involved in the FAW period during which four banks can be activate.
9:4	RW	0x00	Faw The length of the FAW period, in cycles.
3:0	RW	0x00	Rrd The minimum number of scheduler clock cycles between two consecutive DRAM activate commands on different banks on the same device.

service_bus: memory scheduler channel-0 devtodev

Address: Operational Base + offset (0x003c)

Memory scheduler devtodev register

Bit	Attr	Reset Value	Description
31:6	RO	0x0	reserved
5:4	RW	0x00	Buswrtord The time delay, expressed in cycles, between a write and a read operation on different devices.

Bit	Attr	Reset Value	Description
3:2	RW	0x00	Busrdtown The time delay, expressed in cycles, between a read and a write operation on different devices.
1:0	RW	0x00	Busrdtord The time delay, expressed in cycles, between a read and a read operation on different devices.

Following is cpup port's QoS register detail description. Other ports have the same register. The only different is the base address's offset. The offset information is described in Table1-6 ~ Table1-13.

service_core: cpup_qos Priority

Address: Operational Base + offset (0x0008)

CPU master0 priority register

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved
3:2	RW	0x2	P1 sets the high hurry level (i.e. when the measured bandwidth does not exceed the setting) when in Regulator mode, or read urgency level when in fixed or limiter mode.
1:0	RW	0x0	P0 sets the low hurry level, that is, when the measured bandwidth exceeds the setting, when in regulator mode, or write urgency level when in fixed or limiter mode.

service_core: cpup_qos Mode

Address: Operational Base + offset (0x000c)

CPU master0 QoS mode register

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1:0	RW	0x3	Mode determines which of the following modes the QoSGenerator will adopt at reset: 0 : None 1 : Fixed 2 : Limiter 3 : Regulator

service_core: cpup_qos Bandwidth

Address: Operational Base + offset (0x0010)

CPU master0 QoS bandwidth register

Bit	Attr	Reset Value	Description
31:11	RO	0x0	reserved

Bit	Attr	Reset Value	Description
10:0	RW	0x007	Bandwidth Parameter bandwidth determines the bandwidth triggering of the limiter or the regulator. It is expressed in bytes per second. This parameter becomes available when limiter or regulator hardware is implemented.

service_core: cpup_qos Saturation

Address: Operational Base + offset (0x0014)

CPU master0 QoS saturation register

Bit	Attr	Reset Value	Description
31:10	RO	0x0	reserved
9:0	RW	0x3ff	Saturation Parameter saturation determines the excursion of the payload counter, used to estimate the bandwidth, expressed in bytes. This parameter becomes available when limiter or regulator hardware is implemented.

service_core: cpup_qos ExtControl

Address: Operational Base + offset (0x0014)

CPU master0 QoS saturation register

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
2	RW	0x0	Replace the External reference by the local clock.
1	RW	0x0	ExtThr input controls Low/High priority instead of bandwidth threshold.
0	W	0x0	Combines the Socket QoS with Regulator QoS

7.5 Function Description(peri interconnect)

The peri interconnect contain the following master:

peri,gps,dmac,usb,nandc,mac,tsp,sdmmc.

A Global Programmers View (GPV) module exists to configure some properties of the interconnect. The arbitration scheme of this interconnect is configurable through GPV.

The priority from high to low is as follow:

- peri/gps
- dmac
- usb
- nandc/mac

Customers can configure the Qos value through the GPV to change this priority. If you config them to same priority, then the interconnect uses a Least Recently Used (LRU) algorithm

7.6 Register Description(peri interconnect)

7.6.1 Registers Summary

Name	Offset	Size	Reset Value	Description
PERI_RQos_M0	0x42100	4bits	0x0003	peri AXI Port Read channel QoS value.

Name	Offset	Size	Reset Value	Description
PERI_WQos_M0	0x42104	4bits	0x0003	peri AXI Port Write channel quality value.
PERI_RQos_M1	0x43100	4bits	0x0002	dmac Port Read channel QoS value.
PERI_WQos_M1	0x43104	4bits	0x0002	dmac Port Write channel quality value.
PERI_RQos_M2	0x44100	4bits	0x0001	nandc Port Read channel QoS value.
PERI_WQos_M2	0x44104	4bits	0x0001	nandc Port Write channel quality value.
PERI_RQos_M3	0x45100	4bits	0x0000	usb Port Read channel QoS value.
PERI_WQos_M3	0x45104	4bits	0x0000	usb Port Write channel quality value.
PERI_RQos_M4	0x46100	4bits	0x0000	gps Port Read channel QoS value.
PERI_WQos_M4	0x46104	4bits	0x0000	gps Port Write channel quality value.

Notes: **S**ize: **B** – Byte (8 bits) access, **H**W – Half WORD (16 bits) access, **W** – WORD (32 bits) access

7.6.2 Detail Register Description

PERI_RQos_M0

Address: Operational Base+0x42100

PERI_AXI Port Read Qos register

Bit	Attr	Reset Value	Description
3:0	RW	0x1	Read channel QoS value.Higher value indicates higher priority.

PERI_WQos_M0

Address: Operational Base+0x42104

PERI_AXI Port Write Qos register

Bit	Attr	Reset Value	Description
3:0	RW	0x1	Write channel QoS value.Higher value indicates higher priority.

PERI_RQos_M1

Address: Operational Base+0x43100

DMAC Port Read Qos register

Bit	Attr	Reset Value	Description
3:0	RW	0x0	Read channel QoS value.Higher value indicates higher priority.

PERI_WQos_M1

Address: Operational Base+0x43104

DMAC Port Write Qos register

Bit	Attr	Reset Value	Description
3:0	RW	0x0	Write channel QoS value.Higher value indicates higher priority.

PERI_RQos_M2

Address: Operational Base+0x44100

NANDC Port Read Qos register

Bit	Attr	Reset Value	Description
3:0	RW	0x0	Read channel QoS value.Higher value indicates

		higher priority.
--	--	------------------

PERI_WQos_M2

Address: Operational Base+0x44104

NANDC Port Write Qos register

Bit	Attr	Reset Value	Description
3:0	RW	0x0	Write channel QoS value.Higher value indicates higher priority.

PERI_RQos_M3

Address: Operational Base+0x45100

USB Port Read Qos register

Bit	Attr	Reset Value	Description
3:0	RW	0x0	Read channel QoS value.Higher value indicates higher priority.

PERI_WQos_M3

Address: Operational Base+0x45104

USB Port Write Qos register

Bit	Attr	Reset Value	Description
3:0	RW	0x0	Write channel QoS value.Higher value indicates higher priority.

PERI_RQos_M4

Address: Operational Base+0x46100

GPS Port Read Qos register

Bit	Attr	Reset Value	Description
3:0	RW	0x0	Read channel QoS value.Higher value indicates higher priority.

PERI_WQos_M4

Address: Operational Base+0x46104

GPS Port Write Qos register

Bit	Attr	Reset Value	Description
3:0	RW	0x0	Write channel QoS value.Higher value indicates higher priority.

7.7 Application Notes

7.7.1 QoS setting

The cpum read channel, vop read channel , gpu write channel have the external QoS control. After reset each master port both have priority setting as 1. It's recommended that field 0 of qos.ExtControl set to 1 to enable the external qos control. And priority setting of each master kept at 1.

7.7.2 Idle request

The main interconnect supports flushing the ongoing transaction when the software needed to do so.

If the GPU power domain need to disconnect from the main interconnect, Idle request has to be sent to GPU NIU, the NIU will respond a ack, and when it's ready to be disconnect, one Idle signal will be send out . Then, if GPU still have transaction to be sent to the memory scheduler, it will be stalled by the NIU.

If the GPU system power domain is disconnected as the above flow, then CPU want to access to the GPU system, it will response error to CPU.

The sequence is like following figure shows:

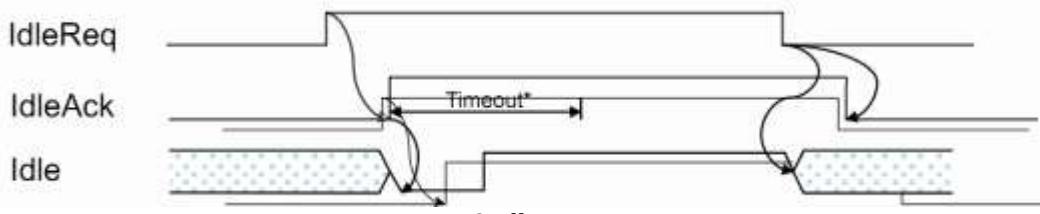


Fig. 7-3 Idle request

The idle request is set by PMU register.

7.7.3 DDR timing examples

The following picture provides examples of DDR timing values, in clock cycles for register values, and nanoseconds for parameter values.

DDR type	DDR2-3E		DDR2-25E		DDR3-187E		DDR3-125E	
DDR frequency	333 MHz		400 MHz		533 MHz		800 MHz	
Scheduler frequency	333 MHz		400 MHz		533 MHz		400 MHz	
Burst length	4		8		8		8	
Register field	cycles	ns	cycles	ns	cycles	ns	cycles	ns
ActToAct	18	54	22	55	27	50.6	19	47.5
RdToMiss	9	27	9	22.5	15	28.1	11	27.5
WrToMiss	16	48	20	50	29	54.3	20	50
BurstLen	2	6	4	10	4	7.5	2	5
RdToWr	2	6	2	5	3	5.6	2	5
WrToRd	2	6	7	17.5	10	18.7	7	17.5
Rrd	4	12	4	10	6	11.2	3	7.5
Faw	17	51	18	45	27	50.6	16	24
BusRdToRd	1	3	1	2.5	1	1.8	1	2.5
BusRdToWr	2	6	2	5	2	3.7	2	5
BusWrToRd	2	6	2	5	2	3.7	2	5

Fig. 7-4 DDR timing example

Chapter 8 Visual Output Processor (VOP)

8.1 Overview

VOP is the display interface from memory frame buffer to display device (LCD panel, LVDS, MIPI, eDP, HDMI and TV set). VOP is connected to an AHB bus through an AHB slave and AXI bus through an AXI master. The register setting is configured through the AHB slave interface and the display frame data is read through the AXI master interface. Furthermore, there is a data path between IEP and VOP, which can provide frame data from IEP to VOP.

8.1.1 Features

- Display interface
 - Parallel RGB LCD Interface
 - ◆ RGB101010,RGB888,RGB666,RGB565
 - Serial RGB LCD Interface
 - ◆ 2x12-bit,3x8-bit(RGB delta supported),3x8-bit+dummy
 - Parallel MCU LCD Interface
 - ◆ 24-bit(RGB888),18-bit(RGB666),16-bit(RGB565)
 - ◆ hold/auto/bypass mode
 - Serial MCU LCD Interface
 - ◆ 2x12-bit, 3x8-bit with hold mode
 - TV Interface
 - ◆ ITU-R BT.656(8-bit, 480i/576i/1080i)
 - ◆ 3 output mode: valid data in lower 8bit, middle 8bit and higher 8bit
 - ◆ TV encoder
 - Support SDR(single data rate) interface
 - Support DDR(dual data rate) interface for LVDS/PARALLEL RGB
 - ◆ parallel RGB and 2x12-bit serial RGB
 - ◆ Single or dual clock out
 - Max output resolution
 - ◆ VOP_BIG: 3840x2160
 - ◆ VOP_LITTLE: 2560x1600
 - Scaning timing 8192x4096
 - Support configurable polarity of DCLK/HSYNC/VSYNC/DEN
 - 4 groups of scanning output for PARALLEL RGB,LVDS,LVDS,HDMI,eDP
 - MIPI control
 - ◆ MIPI dual channel,overlay scan(overlapped pixels=2~16 pix)
 - ◆ MIPI flow control(edpihalt)
 - ◆ MIPI DCS command mode
- Display process
 - CABC
 - BCSH,8bit
 - ◆ Brightness,Contrast,Saturation,Hue adjustment
 - ◆ YUV-10bit, RGB-10bit
 - Dither down
 - ◆ pre dither down for RGB-10bit to RGB-8bit
 - ◆ allegro for RGB565 and RGB666
 - ◆ FRC with configurable pattern for RGB666
 - Gamma
 - ◆ LUT(lookup table) for R/G/B respectively
 - ◆ 8bit/10bit RGB look up table
 - ◆ gamma after dither
 - Support display data swap
 - ◆ BG swap, RB swap, RG swap, dummy swap, delta swap

- Support three YUV2RGB transition modes:
 - ◆ 8bit-YUV: rec601-mpeg/rec601-jpeg/rec709
 - ◆ 10bit-YUV: BT2020
- blank display
- black display
- standby mode
- auto dynamic power control
- X-MIRROR,Y-MIRROR for win0/win1/win2/win3/hwc?
- scale down for TV overscan
 - ◆ after overlay
 - ◆ arbitrary non-integer scaling ratio
 - ◆ horizontal scale down using bilinear, 0.5~1.0
 - ◆ vertical scale down using bilinear, 0.5~1.0
- Layer process
 - Background layer
 - ◆ programmable 24-bit color
 - Win0/Win1 layer
 - ◆ Support data format
 - ✧ RGB888, ARGB888, RGB565,
 - ✧ YCbCr420SP, YCbCr422SP, YCbCr444SP
 - ✧ YUV-8bit,YUV-10bit
 - ◆ YUV clip
 - ✧ Y-10bit:64~940;UV-10bit: 64~960
 - ✧ Y-8bit: 16~235;UV-8bit: 16~240
 - ◆ Support max input resolution 4096x8192
 - ◆ Support max output resolution 3840x2160
 - ◆ Support virtual display
 - ◆ Support 1/8 to 8 scaling-down and scaling-up engine
 - ✧ scale up using bicubic and bilinear
 - Arbitrary non-integer scaling ratio
 - 4 bicubic table for scale up using precise,spline,catrom,Mitchell
 - ✧ scale down using bilinear and average
 - Arbitrary non-integer scaling ratio
 - ✧ per-pix alpha + scale
 - ◆ Support data swap
 - ✧ RGB/BPP: alpha_swap,rb_swap
 - ✧ YUV: mid_swap,uv_swap
 - ◆ transparency color key,prior to alpha blending and fading
 - ◆ Support fading,prior to alpha blending
 - ◆ Support alpha blending
 - ◆ Support interlace and de-flicker for interlace output
 - ◆ Support IEP direct path input
 - Win2/Win3 layer
 - ◆ Support data format
 - ✧ RGB888, ARGB888, RGB565
 - ✧ 1BPP,2BPP,4BPP,8BPP
 - ✧ little endian and big endian for BPP
 - ✧ BYPASS and LUT mode(25bit LUT, 1bit AA+8bit-RGB) for BPP
 - ◆ 4 display regions
 - ✧ only one region at one scanning line
 - ◆ Support data swap
 - ✧ RGB/BPP:rb_swap,alpha_swap
 - ◆ Support transparency color key,prior to alpha blending and fading
 - ◆ Support fading,prior to alpha blending
 - ◆ Support alpha blending
 - ◆ Support interlace read and interlace output

- ◆ Support IEP direct path input
- Hardware Cursor layer(HWC for short)
 - ◆ Support data format
 - ◊ RGB888, ARGB888, RGB565
 - ◊ 1BPP,2BPP,4BPP,8BPP
 - ◊ little endian and big endian for BPP
 - ◊ BYPASS and LUT mode(25bit LUT, 1bit AA+8bit-RGB)for BPP
 - ◆ Support four hwc size: 32x32,64x64,96x96,128x128
 - ◆ Support 2 color modes: normal and reversed color
 - ◆ Support fading,prior to alpha blending
 - ◆ Support alpha blending
 - ◆ Support displaying out of panel,right or bottom
 - ◆ Support NORMAL color and REVERSE color mode
 - ◆ Support interlace read and interlace output
- Overlay
 - ◆ Support 6 layers,background/win0/win1/win2/win3/hwc
 - ◆ Win0/Win1/Win2/Win3 overlay position exchangeable
 - ◆ Alpha blending
 - ◊ Support 12 alpha blending modes
 - ◊ Support pre-multiplied alpha
 - ◊ Support global alpha and per_pix alpha
 - ◊ Support 256 level alpha
 - ◊ layer1/layer2/layer3/hwc support alpha
- Bus interface
 - Support AMBA 2.0 AHB slave interface for accessing internal registers and LUT memories, 32bit data bus width
 - Support AMBA 3.0 AXI master read interface for loading frame data
 - ◆ 128bit data bus width
 - Support MMU
 - Support two transfer modes
 - ◆ auto outstanding transfer
 - ◆ configurable outstanding transfer(gather transfer)
 - DMA line mode for YUV
 - Support QoS request for higher bus priority for win2/win3
 - Support NOC hurry for higher bus priority for win0/win1
 - Support DMA stop mode
 - max read outstanding number
 - ◆ 32 when MMU disable
 - ◆ 31 when MMU enable
- Interrupt
 - One combined interrupt
 - ◆ high active
 - ◆ raw status
 - ◆ combinational with 12 interrupt sources
 - ◊ frame start interrupt
 - ◊ line flag interrupt
 - ◊ bus error interrupt
 - ◊ win0 empty interrupt
 - ◊ win1 empty interrupt
 - ◊ win2 empty interrupt
 - ◊ win3 empty interrupt
 - ◊ hwc empty interrupt
 - ◊ post empty interrupt
 - ◊ pwm gen interrupt

✧ irq_mmu

8.2 Block Diagram

The architecture is shown in the following figure.

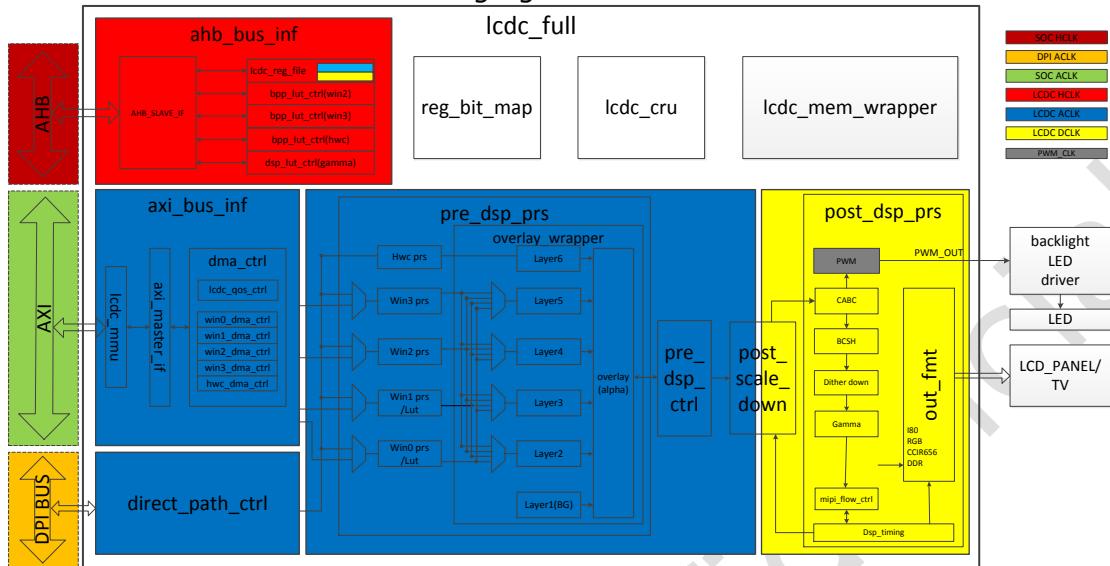


Fig. 8-1 VOP Block Diagram

8.3 Function Description

8.3.1 Pixel format

1.RGB

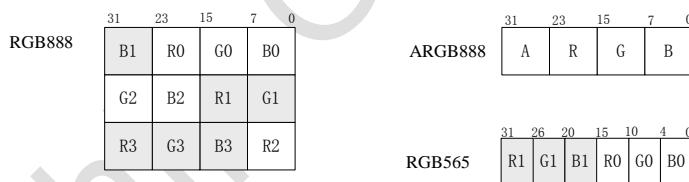


Fig. 8-2 RGB data format

2.YCbCr/YUV(8bit/10bit)

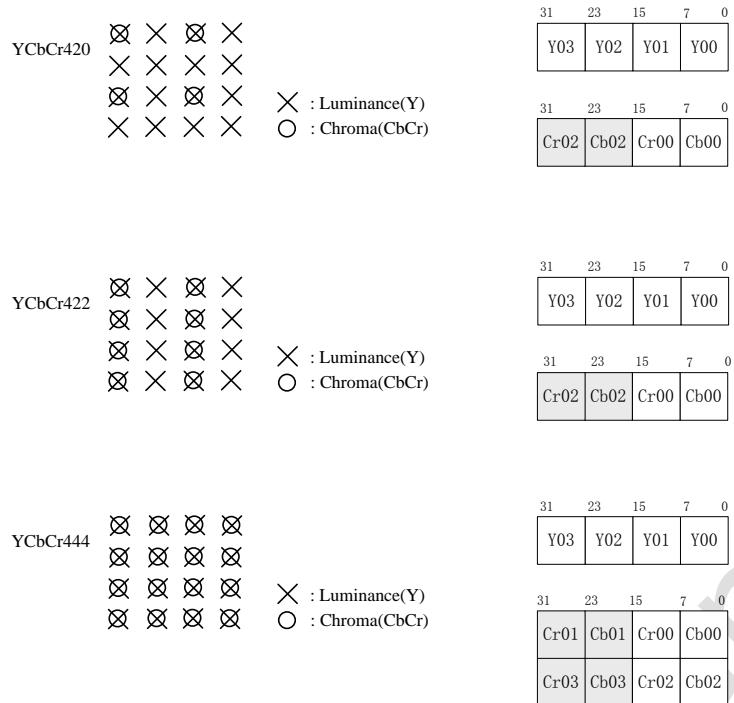


Fig. 8-3 YUV data format

YUV just support SP
YUV-8bit 32bit align
YUV-10bit 128bit align

3.BPP

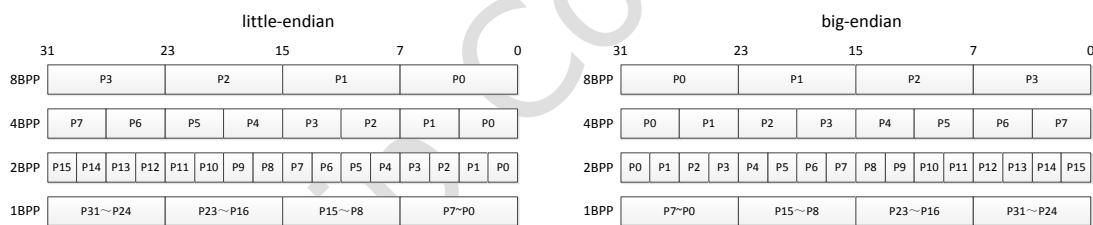


Fig. 8-4 BPP little/big endian data format

8.3.2 Pixel Data Path

There are two data input path for VOP to get display layers' pixel data. One is internal DMA; the other is direction path interface.

1.Internal DMA

Internal DMA can fetch the pixel data through AXI bus from system memory (DDR) for all the display layers. Data fetching is driven by display output requirement.

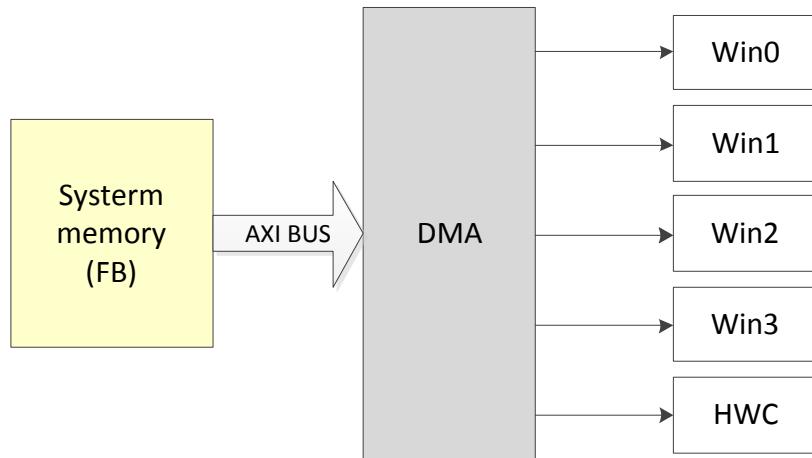


Fig. 8-5 LCDC Internal DMA

2.Direct Path Interface

Direct path interface (DPI) is used for direct image display of external image processing IP. There is a local bus between VOP and external image processing IP for the data transfer.

DPI is connected to WIN0/WIN1/WIN2/WIN3 but can only be configured for One layer use (Win0 or Win1 or Win2 or Win3) in each frame.

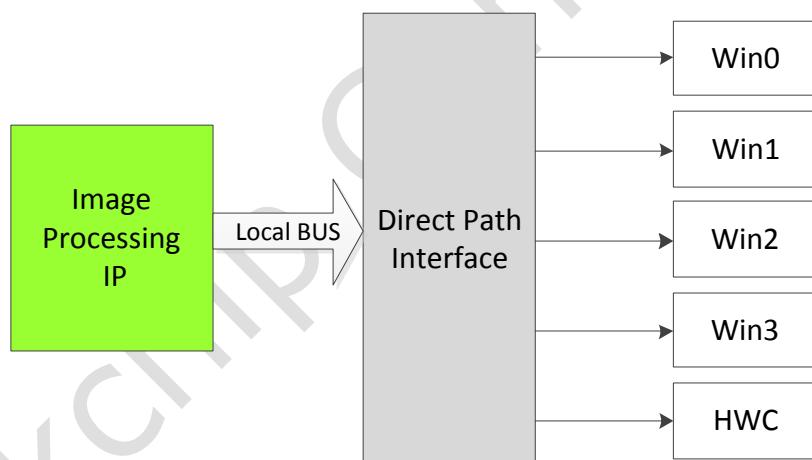


Fig. 8-6 VOP Direct Path Interface

8.3.3 Win Scaling

The scaling operation is the image resizing process by scaling-up or scaling-down the source image from active window size to display window size for displaying on LCD panel or TV set. Horizontal scaling and vertical scaling are realized independently.

1. Scaling factor

Pseudo Code:

```

void calc_win_scl_factor(LCDC_WIN_PARAMETERS *p_win_para)
{
    u16 srcW;
    u16 srcH;
    u16 dstW;
    u16 dstH;
    u8  is_3d_mix;
  
```

```

u16 yrgb_srcW;
u16 yrgb_srcH;
u16 yrgb_dstW;
u16 yrgb_dstH;
u32 yrgb_vScaleDnMult;
u32 yrgb_xscl_factor;
u32 yrgb_yscl_factor;
u8 yrgb_vsd_bil_gt2;
u8 yrgb_vsd_bil_gt4;
u8 yrgb_vsd_bil_extra;

u16 cbcr_srcW;
u16 cbcr_srcH;
u16 cbcr_dstW;
u16 cbcr_dstH;
u32 cbcr_vScaleDnMult;
u32 cbcr_xscl_factor;
u32 cbcr_yscl_factor;
u8 cbcr_vsd_bil_gt2;
u8 cbcr_vsd_bil_gt4;
u8 cbcr_vsd_bil_extra;

//-----
//width and height, 3D enable
is_3d_mix = (p_win_para->win_3d_en == ENABLE) && ((p_win_para->win_3d_mode == MIX_R_GB) ||
(p_win_para->win_3d_mode == MIX_G_RB) || (p_win_para->win_3d_mode == MIX_B_RG));

srcW = p_win_para->win_act_width;
if((p_win_para->win_3d_en == ENABLE)&&(p_win_para->win_3d_mode ==
INTERLEAVE_HORIZONTAL)) {
    dstW = p_win_para->dsp_win_width >> 1;
} else {
    dstW = p_win_para->dsp_win_width;
}
srcH = p_win_para->win_act_height;

if((p_win_para->win_3d_en == ENABLE)&&(p_win_para->win_3d_mode == INTERLEAVE_VERTICAL)) {
    dstH = p_win_para->dsp_win_height >> 1;
} else {
    dstH = p_win_para->dsp_win_height;
}

dstH = p_win_para->dsp_win_height;

if(p_win_para->win_3d_en == ENABLE) {
    if(p_win_para->win_3d_mode == INTERLEAVE_HORIZONTAL) {
        dstW = dstW/2;
    }
    else if(p_win_para->win_3d_mode == INTERLEAVE_VERTICAL) {
        dstH = dstH/2;
    }
}

//-----
//SCALE MODE(YGRB)
yrgb_srcW = srcW;
yrgb_dstW = dstW;
yrgb_srcH = srcH;
yrgb_dstH = dstH;

printf("[hxxy_dbg] yrgb_srcW=%d; yrgb_dstW=%d; yrgb_srcH=%d;
yrgb_dstH=%d;\n",yrgb_srcW,yrgb_dstW,yrgb_srcH,yrgb_dstH);

if (yrgb_srcW < yrgb_dstW) {
    p_win_para->yrgb_hor_scl_mode = SCALE_UP;
} else if (yrgb_srcW > yrgb_dstW) {
    p_win_para->yrgb_hor_scl_mode = SCALE_DOWN;
}

```

```

} else {
    p_win_para->yrgb_hor_scl_mode = SCALE_NONE;
}

if (yrgb_srcH < yrgb_dstH) {
    p_win_para->yrgb_ver_scl_mode = SCALE_UP;
} else if (yrgb_srcH > yrgb_dstH) {
    p_win_para->yrgb_ver_scl_mode = SCALE_DOWN;
} else {
    p_win_para->yrgb_ver_scl_mode = SCALE_NONE;
}

//SCALE MODE(CBCR)
if(p_win_para->win_lcdc_format == LCDC_FMT_YUV422) {
    cbcr_srcW = srcW/2;
    cbcr_dstW = dstW;
    cbcr_srcH = srcH;
    cbcr_dstH = dstH;

    if (cbcr_srcW < cbcr_dstW) {
        p_win_para->cbr_hor_scl_mode = SCALE_UP;
    } else if (cbcr_srcW > cbcr_dstW) {
        p_win_para->cbr_hor_scl_mode = SCALE_DOWN;
    } else {
        p_win_para->cbr_hor_scl_mode = SCALE_NONE;
    }

    if (cbcr_srcH < cbcr_dstH) {
        p_win_para->cbr_ver_scl_mode = SCALE_UP;
    } else if (cbcr_srcH > cbcr_dstH) {
        p_win_para->cbr_ver_scl_mode = SCALE_DOWN;
    } else {
        p_win_para->cbr_ver_scl_mode = SCALE_NONE;
    }
}
else if(p_win_para->win_lcdc_format == LCDC_FMT_YUV420) {
    cbcr_srcW = srcW/2;
    cbcr_dstW = dstW;
    cbcr_srcH = srcH/2;
    cbcr_dstH = dstH;

    if (cbcr_srcW < cbcr_dstW) {
        p_win_para->cbr_hor_scl_mode = SCALE_UP;
    } else if (cbcr_srcW > cbcr_dstW) {
        p_win_para->cbr_hor_scl_mode = SCALE_DOWN;
    } else {
        p_win_para->cbr_hor_scl_mode = SCALE_NONE;
    }

    if (cbcr_srcH < cbcr_dstH) {
        p_win_para->cbr_ver_scl_mode = SCALE_UP;
    } else if (cbcr_srcH > cbcr_dstH) {
        p_win_para->cbr_ver_scl_mode = SCALE_DOWN;
    } else {
        p_win_para->cbr_ver_scl_mode = SCALE_NONE;
    }
}
else if(p_win_para->win_lcdc_format == LCDC_FMT_YUV444) {
    cbcr_srcW = srcW;
    cbcr_dstW = dstW;
    cbcr_srcH = srcH;
    cbcr_dstH = dstH;

    if (cbcr_srcW < cbcr_dstW) {
        p_win_para->cbr_hor_scl_mode = SCALE_UP;
    } else if (cbcr_srcW > cbcr_dstW) {
        p_win_para->cbr_hor_scl_mode = SCALE_DOWN;
    }
}

```

```

    } else {
        p_win_para->cbr_hor_scl_mode = SCALE_NONE;
    }

    if (cbcr_srcH < cbcr_dstH) {
        p_win_para->cbr_ver_scl_mode = SCALE_UP;
    } else if (cbcr_srcH > cbcr_dstH) {
        p_win_para->cbr_ver_scl_mode = SCALE_DOWN;
    } else {
        p_win_para->cbr_ver_scl_mode = SCALE_NONE;
    }
} else {
    cbcr_srcW = 0;
    cbcr_dstW = 0;
    cbcr_srcH = 0;
    cbcr_dstH = 0;

    p_win_para->cbr_hor_scl_mode = SCALE_NONE;
    p_win_para->cbr_ver_scl_mode = SCALE_NONE;
}

printf("[hx debug] cbcr_srcW=%d; cbcr_dstW=%d; cbcr_srcH=%d;
cbcr_dstH=%d;\n", cbcr_srcW, cbcr_dstW, cbcr_srcH, cbcr_dstH);

//-----
//SCALE ALGORITHM
if( (p_win_para->win_lcdc_format == LCDC_FMT_YUV422) || (p_win_para->win_lcdc_format ==
LCDC_FMT_YUV420 ) ) {
    if(p_win_para->cbr_hor_scl_mode == SCALE_DOWN) {
        if(cbcr_dstW > 3840) {
            printf("ERROR cbcr_dst_width exceeds 3840\n");
            exit (-1);
        } else if(cbcr_dstW > 2560) {
            p_win_para->win_lb_mode = LB_RGB_3840X2;
        } else if(cbcr_dstW > 1920) {
            if(p_win_para->yrgb_hor_scl_mode == SCALE_DOWN) {
                if(yrgb_dstW > 3840) {
                    printf("ERROR yrgb_dst_width exceeds 3840\n");
                    exit (-1);
                } else if(yrgb_dstW > 2560) {
                    p_win_para->win_lb_mode = LB_RGB_3840X2;
                } else if(yrgb_dstW > 1920) {
                    p_win_para->win_lb_mode = LB_RGB_2560X4;
                } else {
                    printf("ERROR never run here!yrgb_dstW<1920 ==> cbcr_dstW<1920");
                    exit (-1);
                }
            }
        } else if(cbcr_dstW > 1280) {
            p_win_para->win_lb_mode = LB_YUV_3840X5;
        } else {
            p_win_para->win_lb_mode = LB_YUV_2560X8;
        }
    } else { //SCALE_UP or SCALE_NONE
        if(cbcr_srcW > 3840) {
            printf("ERROR cbcr_act_width exceeds 3840\n");
            exit (-1);
        } else if(cbcr_srcW > 2560) {
            p_win_para->win_lb_mode = LB_RGB_3840X2;
        } else if(cbcr_srcW > 1920) {
            if(p_win_para->yrgb_hor_scl_mode == SCALE_DOWN) {
                if(yrgb_dstW > 3840) {
                    printf("ERROR yrgb_dst_width exceeds 3840\n");
                    exit (-1);
                } else if(yrgb_dstW > 2560) {
                    p_win_para->win_lb_mode = LB_RGB_3840X2;
                }
            }
        }
    }
}

```

```

        } else if(yrgb_dstW > 1920) {
            p_win_para->win_lb_mode = LB_RGB_2560X4;
        } else {
            printf("ERROR never run here!yrgb_dstW<1920 ==> cbcr_dstW<1920 ==>
cbcr_srcW<=1920\n");
            exit (-1);
        }
    }
} else {
    if(p_win_para->yrgb_hor_scl_mode == SCALE_DOWN) {
        if(yrgb_dstW > 3840) {
            printf("ERROR yrgb_dsp_width exceeds 3840\n");
            exit (-1);
        } else if(yrgb_dstW > 2560) {
            p_win_para->win_lb_mode = LB_RGB_3840X2;
        } else if(yrgb_dstW > 1920) {
            p_win_para->win_lb_mode = LB_RGB_2560X4;
        } else if(yrgb_dstW > 1280){
            p_win_para->win_lb_mode = LB_RGB_1920X5;
        } else {
            p_win_para->win_lb_mode = LB_RGB_1280X8;
        }
    } else { //SCALE_UP or SCALE_NONE
        if(yrgb_srcW > 3840) {
            printf("ERROR yrgb_act_width exceeds 3840\n");
            exit (-1);
        } else if(yrgb_srcW > 2560) {
            p_win_para->win_lb_mode = LB_RGB_3840X2;
        } else if(yrgb_srcW > 1920) {
            p_win_para->win_lb_mode = LB_RGB_2560X4;
        } else if(yrgb_srcW > 1280){
            p_win_para->win_lb_mode = LB_RGB_1920X5;
        } else {
            p_win_para->win_lb_mode = LB_RGB_1280X8;
        }
    }
}

printf("[hxdbg] p_win_para->win_lb_mode = %d;\n",p_win_para->win_lb_mode);

//vsd/vsu scale ALGORITHM
switch(p_win_para->win_lb_mode) {
    case LB_YUV_3840X5:
        p_win_para->yrgb_vsu_mode = SCALE_UP_BIC ;
        //p_win_para->yrgb_vsd_mode = SCALE_DOWN_BIL; //not to specify
        p_win_para->cbr_vsu_mode = SCALE_UP_BIC ;
        //p_win_para->cbr_vsd_mode = SCALE_DOWN_BIL; //not to specify
        break;
    case LB_YUV_2560X8:
        p_win_para->yrgb_vsu_mode = SCALE_UP_BIC ;
        //p_win_para->yrgb_vsd_mode = SCALE_DOWN_BIL; //not to specify
        p_win_para->cbr_vsu_mode = SCALE_UP_BIC ;
        //p_win_para->cbr_vsd_mode = SCALE_DOWN_BIL; //not to specify
        break;
    case LB_RGB_3840X2:
        if(p_win_para->yrgb_ver_scl_mode != SCALE_NONE) {
            printf("ERROR : not allow yrgb ver scale\n");
            exit(-1);
        }
}

```

```

if(p_win_para->cbr_ver_scl_mode != SCALE_NONE) {
    printf("ERROR : not allow cbcr ver scale\n");
    exit(-1);
}

//p_win_para->yrgb_vsu_mode = SCALE_UP_BIC ;
//p_win_para->yrgb_vsd_mode = SCALE_DOWN_BIL;
//p_win_para->cbcr_vsu_mode = SCALE_UP_BIC ;
//p_win_para->cbcr_vsd_mode = SCALE_DOWN_BIL;
break;

case LB_RGB_2560X4:
    p_win_para->yrgb_vsu_mode = SCALE_UP_BIL ; //<2
    //p_win_para->yrgb_vsd_mode = SCALE_DOWN_BIL; //<2 //not to specify
    p_win_para->cbcr_vsu_mode = SCALE_UP_BIL ; //<2
    //p_win_para->cbcr_vsd_mode = SCALE_DOWN_BIL; //<2 //not to specify
    break;
case LB_RGB_1920X5:
    p_win_para->yrgb_vsu_mode = SCALE_UP_BIC ;
    //p_win_para->yrgb_vsd_mode = SCALE_DOWN_BIL; //not to specify
    p_win_para->cbcr_vsu_mode = SCALE_UP_BIC ;
    //p_win_para->cbcr_vsd_mode = SCALE_DOWN_BIL; //not to specify
    break;
case LB_RGB_1280X8:
    p_win_para->yrgb_vsu_mode = SCALE_UP_BIC ;
    //p_win_para->yrgb_vsd_mode = SCALE_DOWN_BIL; //not to specify
    p_win_para->cbcr_vsu_mode = SCALE_UP_BIC ;
    //p_win_para->cbcr_vsd_mode = SCALE_DOWN_BIL; //not to specify
    break;
default :
    break;
}

//-----
//SCALE FACTOR
yrgb_vsd_bil_gt4 = 0;
yrgb_vsd_bil_gt2 = 0;
cbcr_vsd_bil_gt4 = 0;
cbcr_vsd_bil_gt2 = 0;

//(1.1)YRGB HOR SCALE FACTOR
switch(p_win_para->yrgb_hor_scl_mode) {
    case SCALE_NONE:
        yrgb_xscl_factor = (1<<SCALE_FACTOR_DEFAULT_FIXPOINT_SHIFT);
        break;

    case SCALE_UP :
        yrgb_xscl_factor = GET_SCALE_FACTOR_BIC(yrgb_srcW, yrgb_dstW);
        break;

    case SCALE_DOWN:
        switch(p_win_para->yrgb_hsd_mode)
        {
            case SCALE_DOWN_BIL:
                yrgb_xscl_factor = GET_SCALE_FACTOR_BILI_DN(yrgb_srcW, yrgb_dstW);
                break;
            case SCALE_DOWN_AVG:
                yrgb_xscl_factor = GET_SCALE_FACTOR_AVRG(yrgb_srcW, yrgb_dstW);
                break;
            default :
                break;
        } //p_win_para->yrgb_vsd_mode
        break;

    default :
        break;
} //p_win_para->yrgb_hor_scl_mode

//(1.2)YRGB VER SCALE FACTOR

```

```

switch(p_win_para->yrgb_ver_scl_mode)
{
    case SCALE_NONE:
        yrgb_yscl_factor = (1<<SCALE_FACTOR_DEFAULT_FIXPOINT_SHIFT);
        break;

    case SCALE_UP :
        switch(p_win_para->yrgb_vsu_mode)
        {
            case SCALE_UP_BIL:
                yrgb_yscl_factor = GET_SCALE_FACTOR_BILI_UP(yrgb_srcH, yrgb_dstH);
                break;
            case SCALE_UP_BIC:
                if(yrgb_srcH < 3) {
                    printf("[hxx_dbg] yrgb_srcH should be greater than 3 !!!\n");
                    exit (-1);
                }
                yrgb_yscl_factor = GET_SCALE_FACTOR_BIC(yrgb_srcH, yrgb_dstH);
                break;
            default :
                break;
        } //p_win_para->yrgb_vsu_mode
        break;

    case SCALE_DOWN:
        switch(p_win_para->yrgb_vsd_mode)
        {
            case SCALE_DOWN_BIL:
                yrgb_vScaleDnMult = getHardWareVSkipLines(yrgb_srcH, yrgb_dstH);
                yrgb_yscl_factor = GET_SCALE_FACTOR_BILI_DN_VSKIP(yrgb_srcH, yrgb_dstH,
yrgb_vScaleDnMult);
                //printf("[hxx_dbg] yrgb_vScaleDnMult=%d;
yrgb_yscl_factor=%04x;\n",yrgb_vScaleDnMult,yrgb_yscl_factor);
                if(yrgb_vScaleDnMult == 4) {
                    yrgb_vsd_bil_gt4 = 1;
                    yrgb_vsd_bil_gt2 = 0;
                } else if(yrgb_vScaleDnMult == 2) {
                    yrgb_vsd_bil_gt4 = 0;
                    yrgb_vsd_bil_gt2 = 1;
                } else {
                    yrgb_vsd_bil_gt4 = 0;
                    yrgb_vsd_bil_gt2 = 0;
                }
                break;
            case SCALE_DOWN_AVG:
                yrgb_yscl_factor = GET_SCALE_FACTOR_AVRG(yrgb_srcH, yrgb_dstH);
                break;
            default :
                break;
        } //p_win_para->yrgb_vsd_mode
        break;

    default :
        break;
} //p_win_para->yrgb_hor_scl_mode

p_win_para->win_h_YRGB_factor = yrgb_xscl_factor;
p_win_para->win_v_YRGB_factor = yrgb_yscl_factor;
p_win_para->vsd_yrgb_gt4      = yrgb_vsd_bil_gt4;
p_win_para->vsd_yrgb_gt2      = yrgb_vsd_bil_gt2;

//(2.1)CBR HOR SCALE FACTOR
switch(p_win_para->cbr_hor_scl_mode)
{
    case SCALE_NONE:
        cbr_xscl_factor = (1<<SCALE_FACTOR_DEFAULT_FIXPOINT_SHIFT);
        break;
}

```

```

case SCALE_UP :
    cbcr_xscl_factor = GET_SCALE_FACTOR_BIC(cbcr_srcW, cbcr_dstW);
    break;

case SCALE_DOWN:
    switch(p_win_para->cbr_hsd_mode)
    {
        case SCALE_DOWN_BIL:
            cbcr_xscl_factor = GET_SCALE_FACTOR_BILI_DN(cbcr_srcW, cbcr_dstW);
            break;
        case SCALE_DOWN_AVG:
            cbcr_xscl_factor = GET_SCALE_FACTOR_AVRG(cbcr_srcW, cbcr_dstW);
            break;
        default :
            break;
    } //p_win_para->cbr_vsd_mode
    break;

default :
    break;
} //p_win_para->cbr_hor_scl_mode

//(2.2)CBCR VER SCALE FACTOR
switch(p_win_para->cbr_ver_scl_mode)
{
    case SCALE_NONE:
        cbcr_yscl_factor = (1<<SCALE_FACTOR_DEFAULT_FIXPOINT_SHIFT);
        break;

    case SCALE_UP :
        switch(p_win_para->cbr_vsu_mode)
        {
            case SCALE_UP_BIL:
                cbcr_yscl_factor = GET_SCALE_FACTOR_BILI_UP(cbcr_srcH, cbcr_dstH);
                break;
            case SCALE_UP_BIC:
                if(cbcr_srcH < 3) {
                    printf("[hxx_dbg] cbcr_srcH should be greater than 3 !!!\n");
                    exit (-1);
                }
                cbcr_yscl_factor = GET_SCALE_FACTOR_BIC(cbcr_srcH, cbcr_dstH);
                break;
            default :
                break;
        } //p_win_para->cbr_vsu_mode
        break;

    case SCALE_DOWN:
        switch(p_win_para->cbr_vsd_mode)
        {
            case SCALE_DOWN_BIL:
                cbcr_vScaleDnMult = getHardWareVSkipLines(cbcr_srcH, cbcr_dstH);
                cbcr_yscl_factor = GET_SCALE_FACTOR_BILI_DN_VSKIP(cbcr_srcH, cbcr_dstH,
cbcr_vScaleDnMult);
                //printf("[hxx_dbg] cbcr_vScaleDnMult=%d;\n",cbcr_vScaleDnMult);
                if(cbcr_vScaleDnMult == 4) {
                    cbcr_vsd_bil_gt4 = 1;
                    cbcr_vsd_bil_gt2 = 0;
                } else if(cbcr_vScaleDnMult == 2) {
                    cbcr_vsd_bil_gt4 = 0;
                    cbcr_vsd_bil_gt2 = 1;
                } else {
                    cbcr_vsd_bil_gt4 = 0;
                    cbcr_vsd_bil_gt2 = 0;
                }
                break;
        }
}

```

```

        case SCALE_DOWN_AVG:
            cbcr_y scl_factor = GET_SCALE_FACTOR_AVRG(cbcr_srcH, cbcr_dstH);
            break;
        default :
            break;
    } //p_win_para->cbr_vsd_mode
    break;

    default :
        break;
} //p_win_para->cbr_hor_scl_mode

p_win_para->vsd_cbr_gt4      = cbcr_vsd_bil_gt4;
p_win_para->vsd_cbr_gt2      = cbcr_vsd_bil_gt2;
p_win_para->win_h_Cbr_factor = cbcr_xscl_factor;
p_win_para->win_v_Cbr_factor = cbcr_yscl_factor;

//-----
switch(p_win_para->yrgb_hor_scl_mode) {
    case SCALE_NONE :
        printf("[hxx_dbg] X YRGB SCALE_NONE\n");
        break;
    case SCALE_UP :
        printf("[hxx_dbg] X YRGB SCALE_UP_BICUBIC; yrgb_xscl_factor=%04x;\n",yrgb_xscl_factor);
        //switch(p_win_para->yrgb_hsu_mode) {
        //    case SCALE_UP_BIL :
        //        printf("[hxx_dbg] X YRGB SCALE_UP_BILINEAR;[ERROR] yrgb_xscl_factor=%04x;\n
",yrgb_xscl_factor);
        //        break;
        //    case SCALE_UP_BIC :
        //        printf("[hxx_dbg] X YRGB SCALE_UP_BICUBIC; yrgb_xscl_factor=%04x;\n
",yrgb_xscl_factor);
        //        break;
        //    default :
        //}
        break;
    case SCALE_DOWN :
        switch(p_win_para->yrgb_hsd_mode) {
            case SCALE_DOWN_BIL :
                printf("[hxx_dbg] X YRGB SCALE_DOWN_BILINEAR;
yrgb_xscl_factor=%04x;\n",yrgb_xscl_factor);
                break;
            case SCALE_DOWN_AVG :
                printf("[hxx_dbg] X YRGB SCALE_DOWN_AVERAGE;
yrgb_xscl_factor=%04x;\n",yrgb_xscl_factor);
                break;
            default:
                break;
        }
        break;
    default:
        break;
}

switch(p_win_para->yrgb_ver_scl_mode) {
    case SCALE_NONE :
        printf("[hxx_dbg] Y YRGB SCALE_NONE\n");
        break;
    case SCALE_UP :
        switch(p_win_para->yrgb_vsu_mode) {
            case SCALE_UP_BIL :
                printf("[hxx_dbg] Y YRGB SCALE_UP_BILINEAR;
yrgb_yscl_factor=%04x;\n",yrgb_yscl_factor);
                break;
            case SCALE_UP_BIC :
                printf("[hxx_dbg] Y YRGB SCALE_UP_BICUBIC;
yrgb_yscl_factor=%04x;\n",yrgb_yscl_factor);

```

```

        break;
    default :
        break;
    }
    break;
case SCALE_DOWN :
    switch(p_win_para->yrgb_vsd_mode) {
        case SCALE_DOWN_BIL :
            printf("[hxx_dbg] Y YRGB SCALE_DOWN_BILINEAR;
yrgb_yscl_factor=%04x;\n",yrgb_yscl_factor);
            break;
        case SCALE_DOWN_AVG :
            printf("[hxx_dbg] Y YRGB SCALE_DOWN_AVERAGE;
yrgb_yscl_factor=%04x;\n",yrgb_yscl_factor);
            break;
        default:
            break;
    }
    break;
default:
    break;
}
//-----
switch(p_win_para->cbr_hor_scl_mode) {
    case SCALE_NONE :
        printf("[hxx_dbg] X CBCR SCALE_NONE\n");
        break;
    case SCALE_UP :
        printf("[hxx_dbg] X CBCR SCALE_UP_BICUBIC; cbcr_xscl_factor=%04x;\n",cbcr_xscl_factor);
        //switch(p_win_para->cbr_hsu_mode) {
        //    printf("[hxx_dbg] X CBCR SCALE_UP_BICUBIC; cbcr_xscl_factor=%04x;\n
",cbcr_xscl_factor);
        //    case SCALE_UP_BIL :
        //        printf("[hxx_dbg] X CBCR SCALE_UP_BILINEAR;[ERROR] cbcr_xscl_factor=%04x;\n
",cbcr_xscl_factor);
        //        break;
        //    case SCALE_UP_BIC :
        //        printf("[hxx_dbg] X CBCR SCALE_UP_BICUBIC; cbcr_xscl_factor=%04x;\n
",cbcr_xscl_factor);
        //        break;
        //    default :
        //}
        break;
    case SCALE_DOWN :
        switch(p_win_para->cbr_hsd_mode) {
            case SCALE_DOWN_BIL :
                printf("[hxx_dbg] X CBCR SCALE_DOWN_BILINEAR;
cbcr_xscl_factor=%04x;\n",cbcr_xscl_factor);
                break;
            case SCALE_DOWN_AVG :
                printf("[hxx_dbg] X CBCR SCALE_DOWN_AVERAGE;
cbcr_xscl_factor=%04x;\n",cbcr_xscl_factor);
                break;
            default:
                break;
        }
        break;
    default:
        break;
}

switch(p_win_para->cbr_ver_scl_mode) {
    case SCALE_NONE :
        printf("[hxx_dbg] Y CBCR SCALE_NONE\n");
        break;
    case SCALE_UP :
        switch(p_win_para->cbr_vsu_mode) {

```

```

        case SCALE_UP_BIL :
            printf("[hxx_dbg] Y CBCR SCALE_UP_BILINEAR;
cbcr_yscl_factor=%04x;\n",cbcr_yscl_factor);
            break;
        case SCALE_UP_BIC :
            printf("[hxx_dbg] Y CBCR SCALE_UP_BICUBIC;
cbcr_yscl_factor=%04x;\n",cbcr_yscl_factor);
            break;
        default :
            break;
    }
    break;
case SCALE_DOWN :
    switch(p_win_para->cbr_vsd_mode) {
        case SCALE_DOWN_BIL :
            printf("[hxx_dbg] Y CBCR SCALE_DOWN_BILINEAR;
cbcr_yscl_factor=%04x;\n",cbcr_yscl_factor);
            break;
        case SCALE_DOWN_AVG :
            printf("[hxx_dbg] Y CBCR SCALE_DOWN_AVERAGE;
cbcr_yscl_factor=%04x;\n",cbcr_yscl_factor);
            break;
        default:
            break;
    }
    break;
default:
    break;
}

//-----
//printf("[hxx_dbg] p_win_para->yrgb_hor_scl_mode=%d;\n",p_win_para->yrgb_hor_scl_mode);
//printf("[hxx_dbg] p_win_para->yrgb_ver_scl_mode=%d;\n",p_win_para->yrgb_ver_scl_mode);
//printf("[hxx_dbg] p_win_para->cbcr_hor_scl_mode=%d;\n",p_win_para->cbcr_hor_scl_mode );
//printf("[hxx_dbg] p_win_para->cbcr_ver_scl_mode=%d;\n",p_win_para->cbcr_ver_scl_mode );

//printf("[hxx_dbg] p_win_para->yrgb_hsd_mode= %d;\n",p_win_para->yrgb_hsd_mode);
//printf("[hxx_dbg] p_win_para->cbr_hsd_mode = %d;\n",p_win_para->cbr_hsd_mode );

//printf("[hxx_dbg] p_win_para->yrgb_vsu_mode= %d;\n",p_win_para->yrgb_vsu_mode);
//printf("[hxx_dbg] p_win_para->yrgb_vsd_mode= %d;\n",p_win_para->yrgb_vsd_mode);
//printf("[hxx_dbg] p_win_para->cbr_vsu_mode = %d;\n",p_win_para->cbr_vsu_mode );
//printf("[hxx_dbg] p_win_para->cbr_vsd_mode = %d;\n",p_win_para->cbr_vsd_mode );

//printf("[hxx_dbg] yrgb_xscl_factor= %04x\n", yrgb_xscl_factor);
//printf("[hxx_dbg] yrgb_yscl_factor= %04x\n", yrgb_yscl_factor);
//
//printf("[hxx_dbg] cbcr_xscl_factor= %04x\n", cbcr_xscl_factor);
//printf("[hxx_dbg] cbcr_yscl_factor= %04x\n", cbcr_yscl_factor);

} //end calc_win_scl_factor

```

2.Limitation of YUV scaling down(3840 < width < 4096)

Limitation of 3840~4096 horizontal scale down for YUV422/420:

YUV422

- (1) not support vertical scale up/down if width(>3840) scale down to width(>2560);
- (2) support vertical down but only support vertical bilinear scale up if width(>3840) scale down to width(>1920 and <2560);
- (3) no limitation if width(>3840) scale down to width(<=1920);

YUV420

- (1) not support width(>3840) scale down to width(>2560);

(2) support vertical down but only support vertical bilinear scale up if width(>3840) scale down to width(>1920 and <2560);

(3) no limitation if width(>3840) scale down to width(<=1920);

Since the sampling rate is different for lumina data and chroma data with the format of YCbCr422 and YCbCr420, the scaling factors for lumina data and chroma data are calculated and configured in VOP_WIN0_SCL_FACTOR_Y/ VOP_WIN0_SCL_FACTOR_CBR respectively.

8.3.4 De-flicker

It is necessary to display a non-interlaced video signal on an interlaced display panel (such as TV set). Thus "non-interlaced-to-interlaced conversion" is required.

The easiest approach is to throw away every other active scan line in each non-interlaced frame. Although the cost is minimal, there are problems with this approach. If there is a sharp vertical transition of color or intensity, it will flicker at one-half the refresh rate.

A better solution is to use two lines of non-interlaced data to generate one line of interlace data. Fast vertical transition is smoothed out over several interlace lines.

The vertical filtering of two non-interlaced lines can be done by enabling the vertical scaling offset updated dynamically in different fields, i.e, even field and odd field. The dynamic updated value of scaling offset is half of the scaling factor.

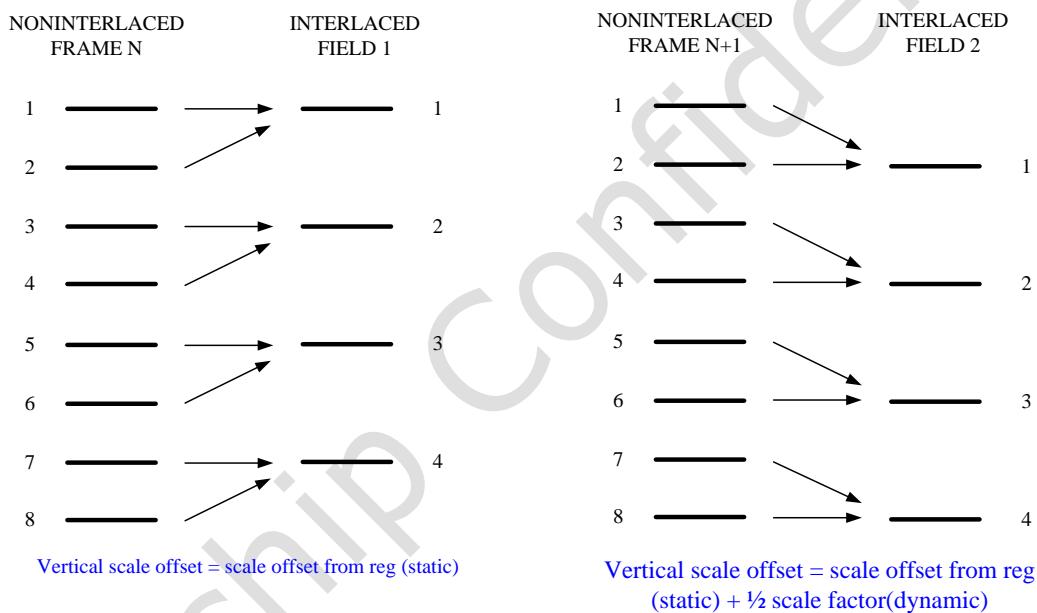


Fig. 8-7 De-flicker

8.3.5 Virtual display

When in virtual display, the active image is part of the virtual (original) image in frame buffer memory.

The virtual width is indicated by setting VIR_STRIDE and VIR_STRIDE for different data format. Note that RGB/BPP has one stride—yrgb_vir_stride; YUV has two virtual stride—yrgb_vir_stride and cbcr_vir_stride.

For RGB-8bit and YUV-8bit, the stride should be multiples of word (32-bit), with dummy bytes in the end of virtual line if the original width is not 32-bit aligned.

For YUV-10bit, the stride should be multiples of word (-bit), with dummy bytes in the end of virtual line if the original width is not 128-bit aligned.

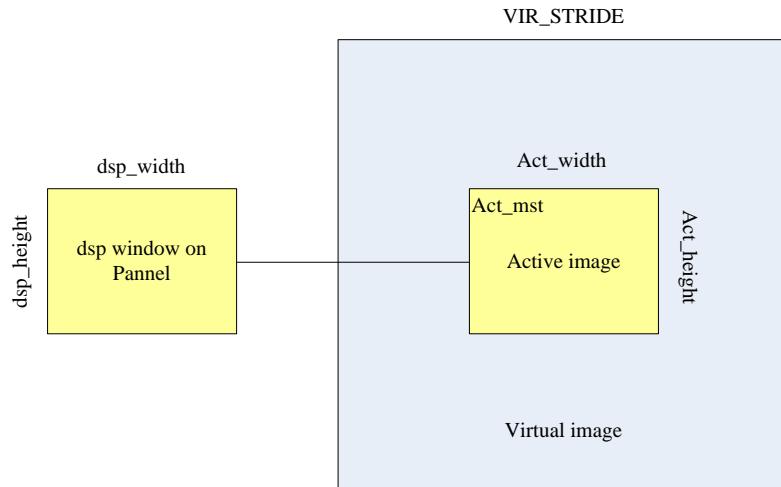


Fig. 8-8 Virtual display

8.3.6 MIRROR display

Mirror display is necessary for the panel with mirror timing interface. There are two types of mirror mode: horizontal mirror(X-Mirror) and vertical mirror(Y-mirror).

The default display order is from left to right(L2R) in horizontal direction and from top to bottom(T2B) in vertical direction. However, when X-Mirror is enable, the horizontal display order is from right to left(R2L); when Y-MIRROR is enable, the vertical display order is from bottom to top(B2T).

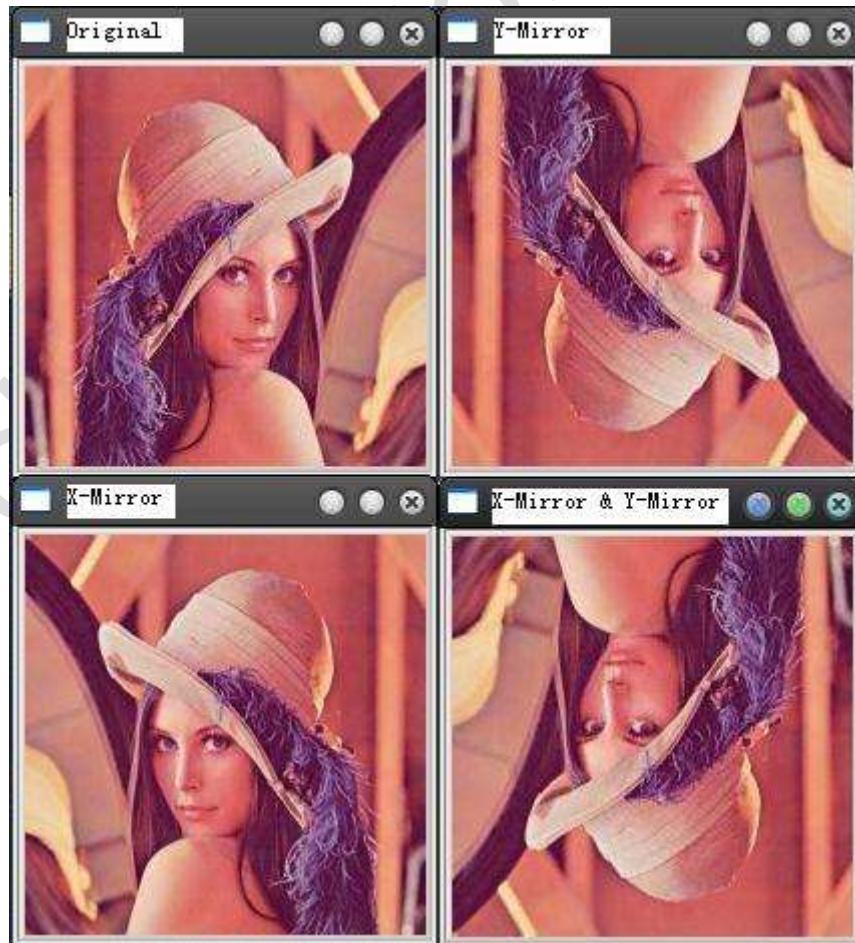
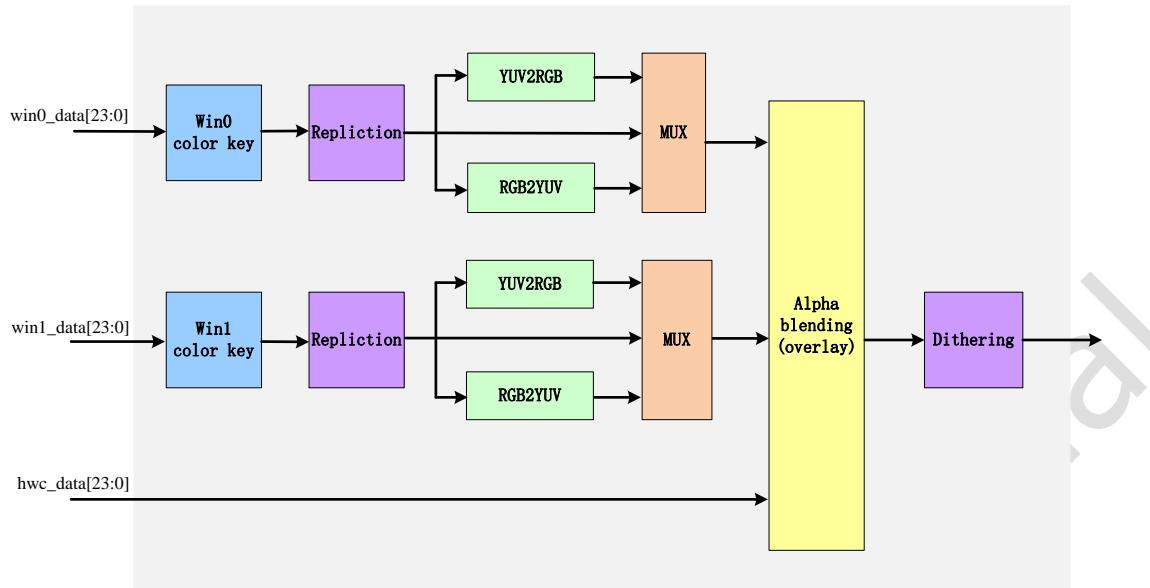


Fig. 8-9 X-Mirror and Y-Mirror

8.3.7 Display process



1. Overlay display

There are totally 4 layers for overlay display: Background, win0 layer, win1 layer and hardware cursor layer(HWC).

Background is a programmable solid color layer, which is always in the bottom of the display screen.

HWC is a 32x32 or 64x64 3-LUT-colors layer, which is always on the top of the display screen.

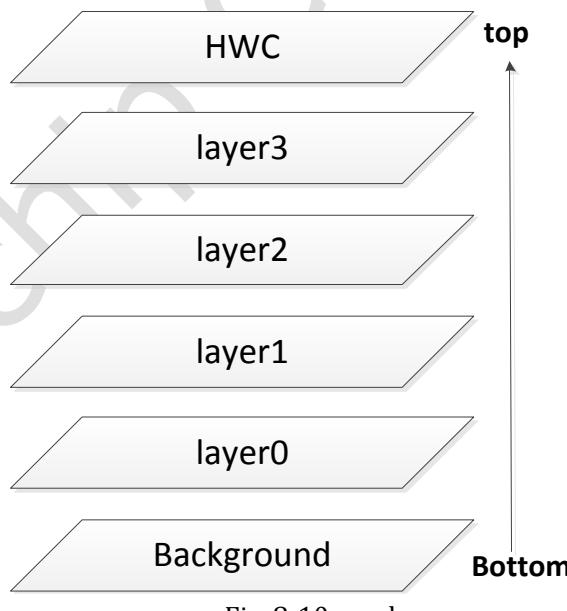
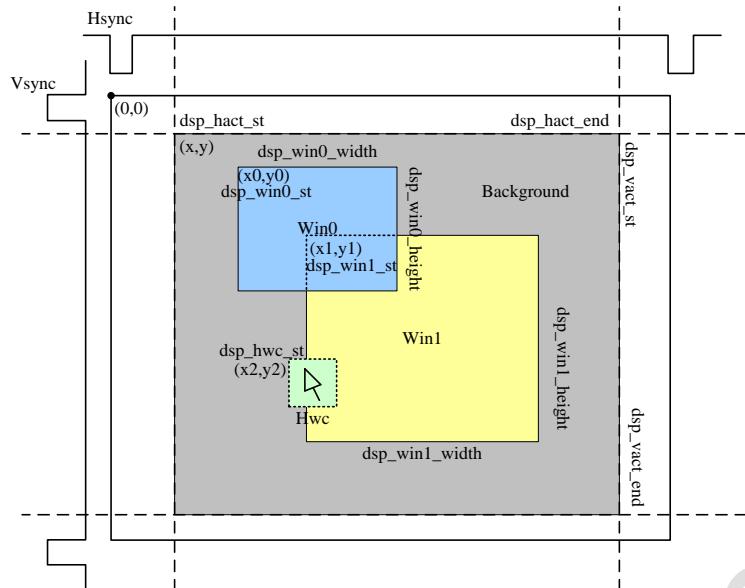


Fig. 8-10 overlay

Following figure is an example of overlay display for `win0`,`win1` and `hwc`.



2.Post scale down

Post scale down after overlay is supported to fix overscan, that draws the borders of the image beyond the normally visible area on the screen.

The scale ratio of post scale down is 0.5~1.

Post timing setting

The post scale parameter ,such as,post_dsp_hact_st,post_dsp_hact_end, post_dsp_vact_st,post_dsp_vact_end can be configured.

When post scaling equal "1" ,the post scaler parameter are the same as dsp timing parameter.

eg:

```
post_dsp_hact_st = dsp_hact_st
post_dsp_hact_end = dap_hact_end
post_dsp_vact_st = dsp_vact_st
post_dsp_vact_end = dsp_vact_end
```

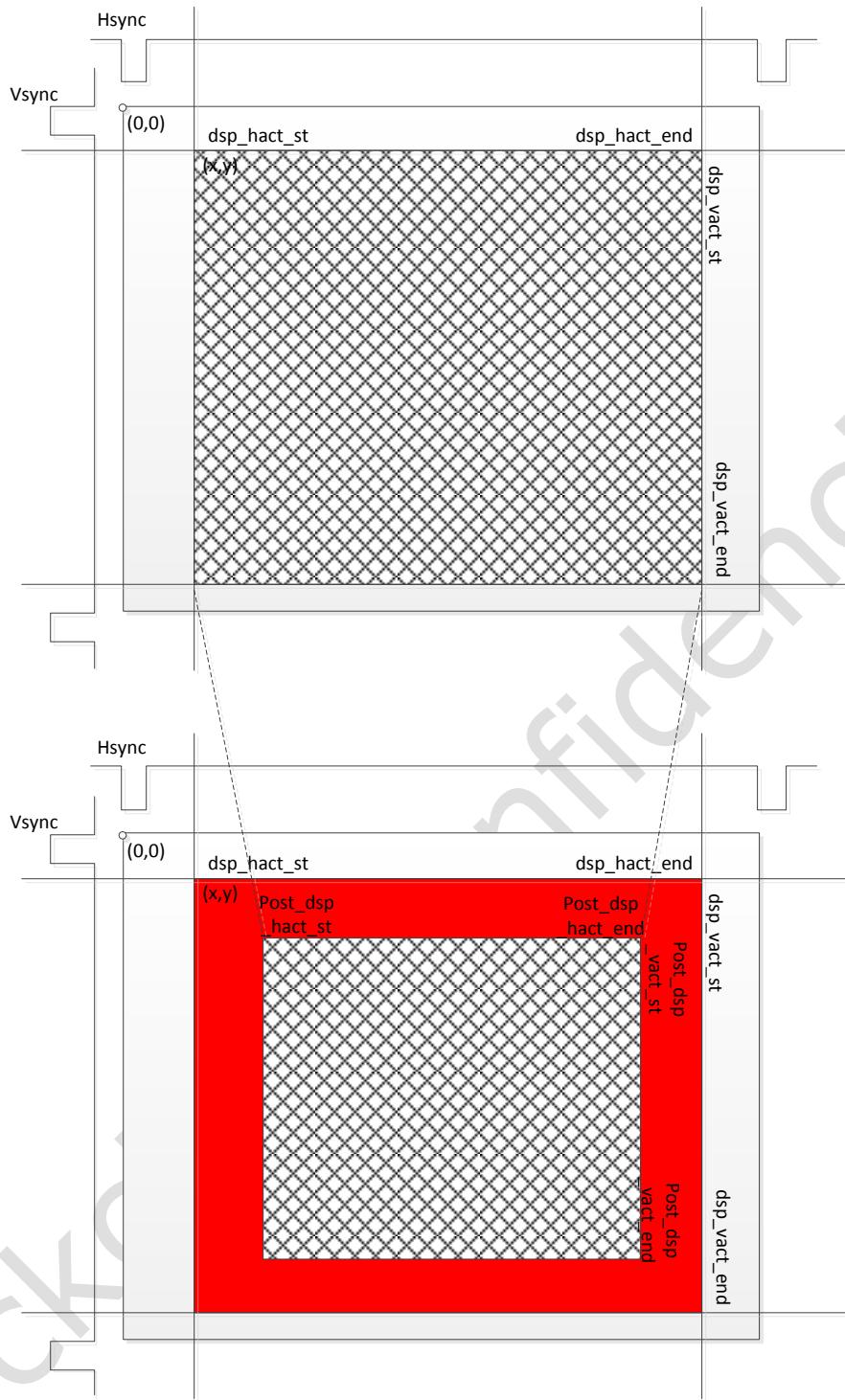


Fig. 8-11 post scaling timing

Post scale down factor

For horizontal scale down,factor = $((src_width*2/3)<<16)/(dst_width-1)$.

For vertical scale down,factor = $((src_width*2/3)<<16)/(dst_width-1)$.

3.Transparency color key

The transparency color key value defines the pixel treated as transparent pixel. The pixel whose value is equal to the color key value could not be visible on the screen, instead of the pixel in the under layer or solid background color.

There are two transparency color key for win0 layer and win1 layer respectively. When color

key is enable, the transparency process is done after scaling but before YUV2RGB color space converter.

Moreover, transparency color key is just available for non-scaling mode.

Following figure is an example of transparency color key for win0 and win1.

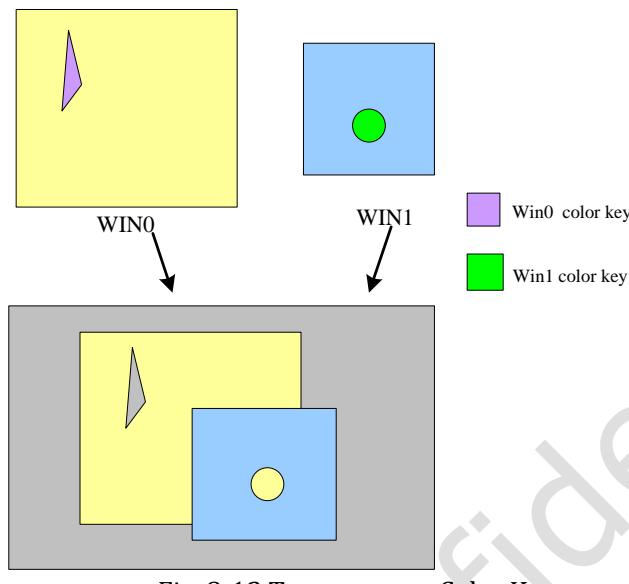
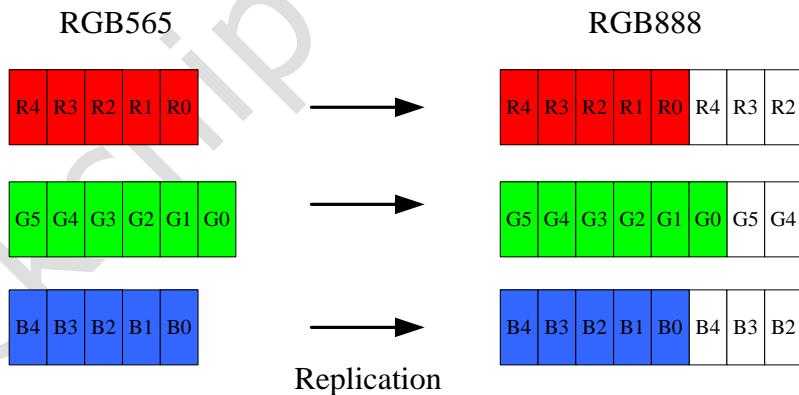


Fig. 8-12 Transparency Color Key

4.Replication(dither up)

If the size of panel data bus is larger than the size of source pixel data, i.e., the source input format is RGB565 and display output format is RGB888, you could do bit replication by replicating MSBs to LSBs if replication is enable (VOP_DSP_CTRL0[9]=1) or filling with "0" to LSBs if replication is disable (VOP_DSP_CTRL0[9]=0).



5.Alpha blending

There are 12 alpha blending mode between two overlay layers for layer1/layer2/layer3/hwc. Layer0 does not support alpha blending with background.

When in per-pixel mode, the alpha value for every pixel is following with the pixel data. i.e., aRGB, and can be scaled like RGB data. Therefore it is just suitable for win0/win1/win2/win3/hwc layer with ARGB data format.

The alpha blending architecture is shown as follows.

Table 8-1 alpha blending mode settings

Blending Mode	C_s'	F_s	C_d'	F_d
---------------	--------	-------	--------	-------

AA_USER_DEFINED	X	User defined	Cd	User defined
AA_CLEAR	X	0	Cd	0
AA_SRC	X	0	Cd	1
AA_DST	X	1	Cd	1
AA_SRC_OVER	Cs	1	Cd	1-As''
AA_DST_OVER	Cs	1-As''	Cd	1
AA_SRC_IN	Cs	As''	Cd	0
AA_DST_IN	X	0	Cd	As''
AA_SRC_OUT	Cs	1-As''	Cd	0
AA_DST_OUT	X	0	Cd	1-As''
AA_SRC_ATOP	Cs	As''	Cd	1-As''
AA_DST_ATOP	Cs	1-As''	Cd	As''
AA_XOR	Cs	1-As''	Cd	1-As''
AA_SRC_OVER_GLOBAL	Cs*As''	Ags''	Cd	1-As''

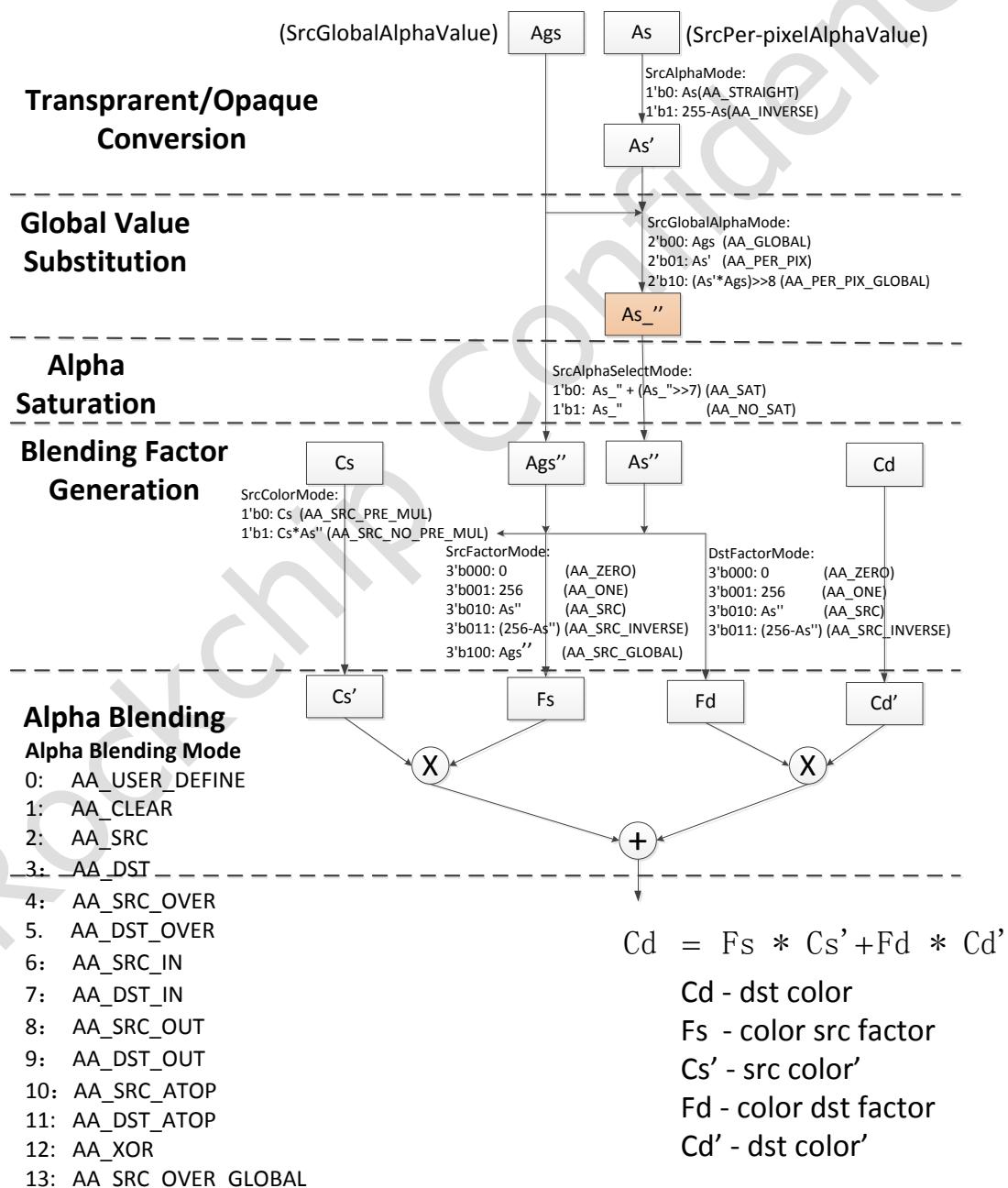


Fig. 8-13 alpha configuration flow

Pseudo Code:

```
switch(alpha_config->alpha_blending_mode)
{
    case AA_USER_DEFINE:
        break;
    case AA_CLEAR:
        alpha_config->src_factor_mode=AA_ZERO;
        alpha_config->dst_factor_mode=AA_ZERO;
        break;
    case AA_SRC:
        alpha_config->src_factor_mode=AA_ONE;
        alpha_config->dst_factor_mode=AA_ZERO;
        break;
    case AA_DST:
        alpha_config->src_factor_mode=AA_ZERO;
        alpha_config->dst_factor_mode=AA_ONE;
        break;
    case AA_SRC_OVER:
        alpha_config->src_color_mode=AA_SRC_PRE_MUL;
        alpha_config->src_factor_mode=AA_ONE;
        alpha_config->dst_factor_mode=AA_SRC_INVERSE;
        break;
    case AA_DST_OVER:
        alpha_config->src_color_mode=AA_SRC_PRE_MUL;
        alpha_config->src_factor_mode=AA_SRC_INVERSE;
        alpha_config->dst_factor_mode=AA_ONE;
        break;
    case AA_SRC_IN:
        alpha_config->src_color_mode=AA_SRC_PRE_MUL;
        alpha_config->src_factor_mode=AA_SRC;
        alpha_config->dst_factor_mode=AA_ZERO;
        break;
    case AA_DST_IN:
        alpha_config->src_factor_mode=AA_ZERO;
        alpha_config->dst_factor_mode=AA_SRC;
        break;
    case AA_SRC_OUT:
        alpha_config->src_color_mode=AA_SRC_PRE_MUL;
        alpha_config->src_factor_mode=AA_SRC_INVERSE;
        alpha_config->dst_factor_mode=AA_ZERO;
        break;
    case AA_DST_OUT:
        alpha_config->src_factor_mode=AA_ZERO;
        alpha_config->dst_factor_mode=AA_SRC_INVERSE;
        break;
    case AA_SRC_ATOP:
        alpha_config->src_color_mode=AA_SRC_PRE_MUL;
        alpha_config->src_factor_mode=AA_SRC;
        alpha_config->dst_factor_mode=AA_SRC_INVERSE;
        break;
    case AA_DST_ATOP:
        alpha_config->src_color_mode=AA_SRC_PRE_MUL;
        alpha_config->src_factor_mode=AA_SRC_INVERSE;
        alpha_config->dst_factor_mode=AA_SRC;
        break;
    case AA_XOR:
        alpha_config->src_color_mode=AA_SRC_PRE_MUL;
```

```

alpha_config->src_factor_mode=AA_SRC_INVERSE;
alpha_config->dst_factor_mode=AA_SRC_INVERSE;
break;
case AA_SRC_OVER_GLOBAL:
alpha_config->src_global_alpha_mode=AA_PER_PIX_GLOBAL;
alpha_config->src_color_mode=AA_SRC_NO_PRE_MUL;
alpha_config->src_factor_mode=AA_SRC_GLOBAL;
alpha_config->dst_factor_mode=AA_SRC_INVERSE;
break;
default:
    printf("alpha mode error\n");
    break;
}

```

6.CABC

CABC(Content Adaptive Backlight Control) is used to increase the contrast of such LCD-screens the backlight can be (globally) dimmed when the image to be displayed is dark (i.e. not comprising high intensity image data) while the image data is numerically corrected and adapted to the reduced backlight intensity.

Config the panel total pixel num to reg 0x1c4 ,and config the calc pixel num to regfile 0x1c0 (typical calc_pixel_num / total_pixel_num \approx 80% ~90%).

Config the stage up and stage down to ensure the luminance difference will not be too big in each two adjacent frames. Typical value is 0x20~0x40.

There are 3x7 Gaussian filter tables in reg 0x1c8~0x1dc.

default value as follow:

0x1c8 : 0x15110903
 0x1cc : 0x00030911
 0x1d0 : 0x1a150b04
 0x1d4 : 0x00040b15
 0x1d8 : 0x15110903
 0x1dc : 0x00030911

7.BCSH

BCSH is used to adjust "Brightness,Contrast,Saturation,Hue,like IEP BCSH-8bit. For details,please refer to IEP chapter.

- Extend yuv data from 8bits(IEP) to 10bits.
- The brightness adjust support (-128,127).
- The yuv data of color bar are 10bits.

8.Color space conversion

There are three standards for YUV2RGB-8bit, and BT2020 standard for YUV2RGB-10bit.

- YUV2RGB-8bit

1. yuv to rgb (REC-601) range 0 (Y[16:235], UV[16:240], RGB[0:255])

$$R = 1.164(Y-16) + 1.596(V-128)$$

$$G = 1.164(Y-16) - 0.391(U-128) - 0.813(V-128)$$

$$B = 1.164(Y-16) + 2.018(U-128)$$

2. yuv to rgb (REC-601) range 1 (YUV[0:255], RGB[0:255])

$$R = (Y-16) + 1.402(V-128)$$

$$G = (Y-16) - 0.344(U-128) - 0.714(V-128)$$

$$B = (Y-16) + 1.772(U-128)$$

3. yuv to rgb (REC-709) range 0 (Y[16:235], UV[16:240], RGB[0:255])

$$R = 1.164(Y-16) + 1.793(V-128)$$

$$G = 1.164(Y-16) - 0.213(U-128) - 0.534(V-128)$$

$$B = 1.164(Y-16) + 2.115(U-128)$$

- RGB2YUV-8bit

ccir601

$$Y = 0.257R + 0.504G + 0.098B + 16$$

$$Cb = -0.148R - 0.291G + 0.439B + 128$$

$$Cr = 0.439R - 0.368G - 0.071B + 128$$

- YUV2RGB-10bit

$$Y = (230R+595G+52B+65536)/1024$$

$$U = (-125R-323G+449B+524288)/1024$$

$$V = (449R-412G-36B+524288)/1024$$

- RGB2YUV-10bit

$$R = 1.1636Y + 1.6778V - 933.504$$

$$G = 1.1636Y - 0.1872U - 0.6501V + 351.9232$$

$$B = 1.1636Y + 2.1406U - 1170.4576$$

9.Dither Down

Dither down directly

The invalid lower bits will be replaced by "0" after dither operation, if disable dither down. eg:
10'b10_1011_00XX → 10'b10_1011_0000.

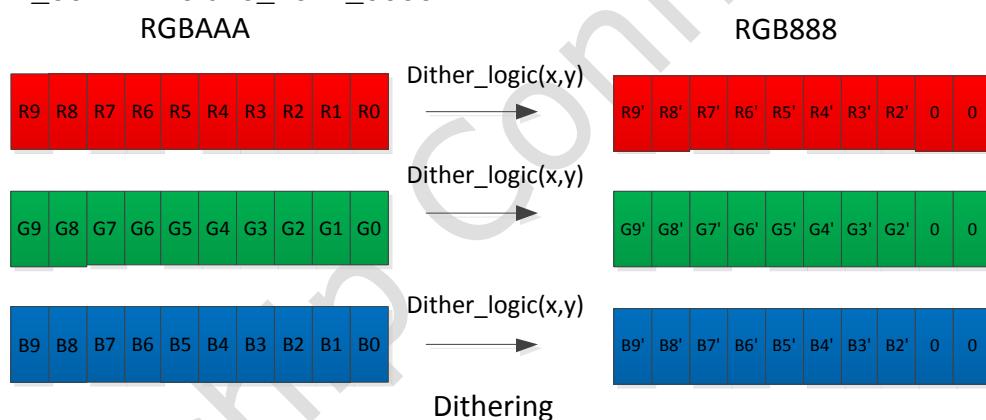


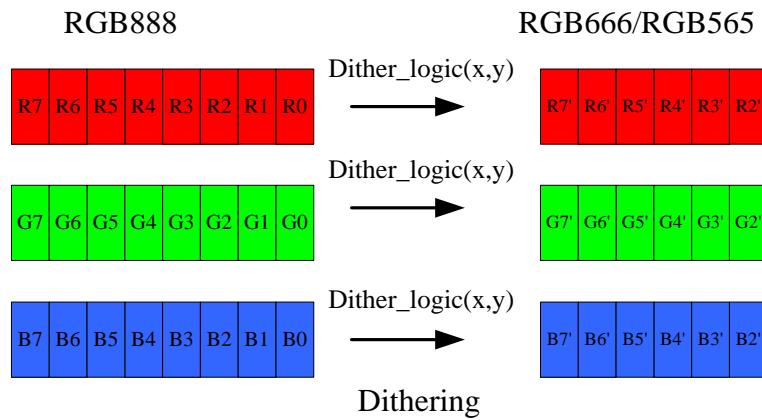
Fig. 8-14 Dither down directly

Allegro Dither Down

Dithering is an intentional applied form of noise, using to randomize quantization error, and thereby preventing large-scaling patterns such as "banding".

The pixel value is used by dithering process to display the data in a lower color depth on the LCD panel, i.e, the source input format is RGB888 and display output format is RGB565 or RGB666. When dithering is enable(VOP_DSP_CTRL0[11]=1), the output data is generated by dithering algorithm based on the pixel position and the value of removed bits. Otherwise, the MSBs of the pixel color components are output as display data.

There are two dither modes: "RGB888 to RGB666" and "RGB888 to RGB565", which is defined by VOP_DSP_CTRL0[10]. When VOP_DSP_CTRL0[10] is 1, dithering with "RGB888 to RGB666" is available; otherwise, "RGB888 to RGB565" is used.



FRC Dither Down

The pattern of dither frc was configured by vop regfile vop_base+0x1e0~0x1f4.

The following fig is the default pattern picture in vop, you can config different value of regfile 0x1e0~0x1f4, to change the pattern picture.

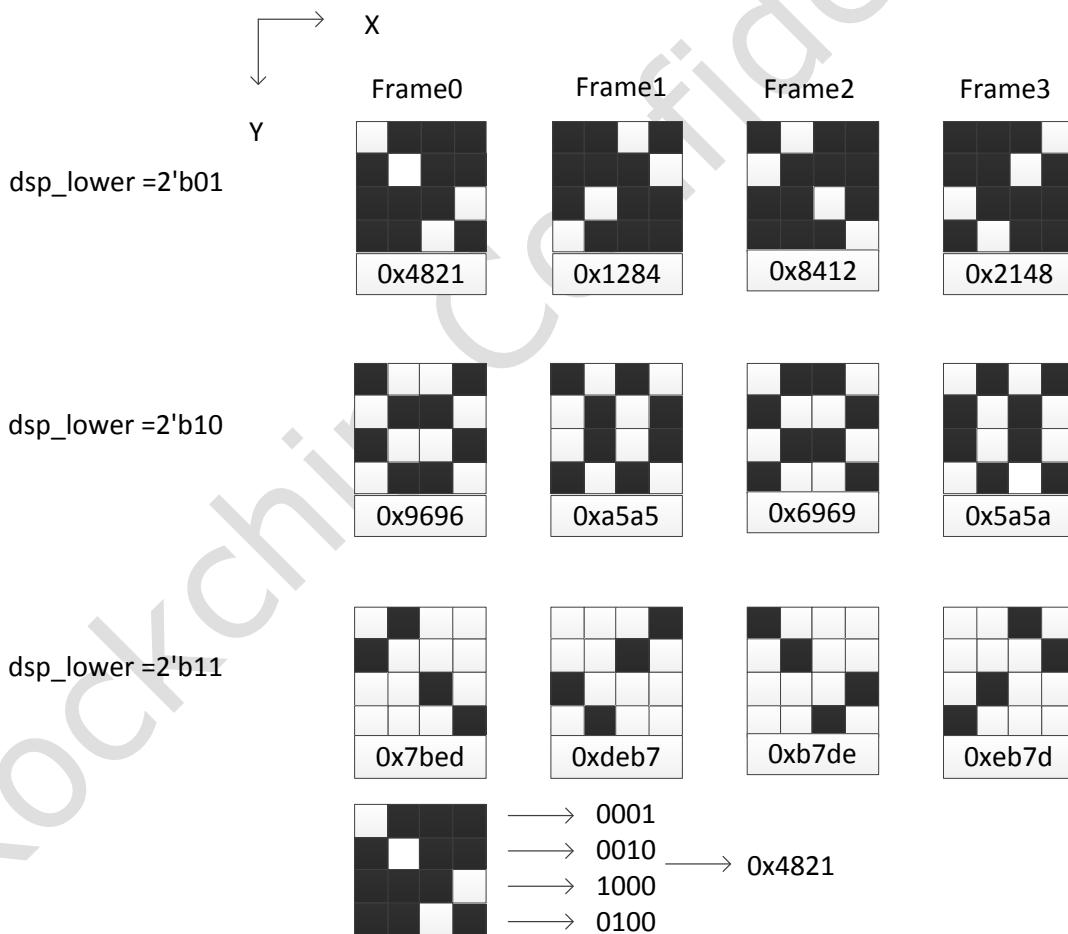


Fig. 8-15 frc pattern diagram

There are four typical pattern as follow :

default pattern:
 0x1e0 : 0x12844821
 0x1e4 : 0x21488412
 0x1e8 : 0xa55a9696
 0x1ec : 0x5aa56969

```

0x1f0 : 0xdeb77bed
0x1f4 : 0xed7bb7de
    for column inversion panel:
0x1e0 : 0x50a00a05
0x1e4 : 0xa050050a
0x1e8 : 0x5a5aa5a5
0x1ec : 0x5a5aa5a5
0x1f0 : 0xaf5ff5fa
0x1f4 : 0x5faffaf5
    for 1+2dot panel
0x1e0 : 0x0c308421
0x1e4 : 0x124803c0
0x1e8 : 0xcc339669
0x1ec : 0x33cc9669
0x1f0 : 0xf3cf7bde
0x1f4 : 0xedb7fc3f
    default enhance pattern
0x1e0 : 0x12844821
0x1e4 : 0x21488412
0x1e8 : 0x55aaaa55
0x1ec : 0x55aaaa55
0x1f0 : 0xdeb77bed
0x1f4 : 0xed7bb7de

```

10.Gamma Correction

Gamma Correction is necessary because most monitors don't have a linear relationship between the voltage and the brightness, which results in your scene looking like it has too much contrast and the light falling off from the source outward, happens too quickly. The result can also be problematic if you are going into a composition program.

You can correct this by "Gamma Correction", which allows you to display the images and textures on your computer in an accurate manner.

Your screen is not linear, in that it displays the brightness unevenly. As a result, the image looks to be more high contrast than it should, you end up adding more lights or turning up the intensity, or you don't use the lighting in a realistic way that matches well with live action scenes. It also creates problems for you if you use compositing software.

There are three 1024x10bits line buffers separately for 10bit-R/G/B gamma correction. For 8bit-RGB, it only consumes 256x8bit for each channel. You can write gamma correction LUT through register "GAMMA_LUT_ADDR" one by one.

11.Output format

Config `dsp_out_mode` register to adapt a variety of panel interface. As follow:



Fig. 8-16 `dsp_out_mode` description

8.4 Register Description

8.4.1 Registers Summary

Name	Offset	Size	Reset Value	Description
VOP_REG_CFG_DONE	0x0000	W	0x00000000	Register config done flag
VOP_VERSION_INFO	0x0004	W	0x00000000	
VOP_SYS_CTRL	0x0008	W	0x00801000	System control register0
VOP_SYS_CTRL1	0x000c	W	0x00000000	
VOP_DSP_CTRL0	0x0010	W	0x00000000	Display control register0
VOP_DSP_CTRL1	0x0014	W	0x0000e400	Display control register1
VOP_DSP_BG	0x0018	W	0x00000000	background color
VOP MCU CTRL	0x001c	W	0x00711c08	MCU mode control register
VOP_INTR_CTRL0	0x0020	W	0x00000000	Interrupt ctrl register0
VOP_INTR_CTRL1	0x0024	W	0x00000000	Interrupt ctrl register1
VOP_INTR_RESERVED0	0x0028	W	0x00000000	
VOP_INTR_RESERVED1	0x002c	W	0x00000000	
VOP_WIN0_CTRL0	0x0030	W	0x00000040	win0 ctrl register0
VOP_WIN0_CTRL1	0x0034	W	0x00000000	win1 ctrl register1
VOP_WIN0_COLOR_KEY	0x0038	W	0x00000000	Win0 color key register
VOP_WIN0_VIR	0x003c	W	0x00000140	Win0 virtual stride
VOP_WIN0_YRGB_MST	0x0040	W	0x00000000	Win0 YRGB memory start address
VOP_WIN0_CBR_MST	0x0044	W	0x00000000	Win0 Cbr memory start address
VOP_WIN0_ACT_INFO	0x0048	W	0x00ef013f	Win0 active window width/height
VOP_WIN0_DSP_INFO	0x004c	W	0x00ef013f	Win0 display width/height on panel
VOP_WIN0_DSP_ST	0x0050	W	0x000a000a	Win0 display start point on panel
VOP_WIN0_SCL_FACTOR_YRGB	0x0054	W	0x10001000	Win0 YRGB scaling factor
VOP_WIN0_SCL_FACTOR_CBR	0x0058	W	0x10001000	Win0 Cbr scaling factor
VOP_WIN0_SCL_OFFSET	0x005c	W	0x00000000	Win0 scaling start point offset
VOP_WIN0_SRC_ALPHA_CTRL	0x0060	W	0x00000000	
VOP_WIN0_DST_ALPHA_CTRL	0x0064	W	0x00000000	
VOP_WIN0_FADING_CTRL	0x0068	W	0x00000000	
VOP_WIN0_RESERVED0	0x006c	W	0x00000000	
VOP_WIN1_CTRL0	0x0070	W	0x00000040	win1 ctrl register0
VOP_WIN1_CTRL1	0x0074	W	0x00000000	win1 ctrl register1
VOP_WIN1_COLOR_KEY	0x0078	W	0x00000000	Win1 color key register
VOP_WIN1_VIR	0x007c	W	0x00000140	win1 virtual stride
VOP_WIN1_YRGB_MST	0x0080	W	0x00000000	Win1 YRGB memory start address

Name	Offset	Size	Reset Value	Description
VOP_WIN1_CBR_MST	0x0084	W	0x00000000	Win1 Cbr memory start address
VOP_WIN1_ACT_INFO	0x0088	W	0x00ef013f	Win1 active window width/height
VOP_WIN1_DSP_INFO	0x008c	W	0x00ef013f	Win1 display width/height on panel
VOP_WIN1_DSP_ST	0x0090	W	0x000a000a	Win1 display start point on panel
VOP_WIN1_SCL_FACTOR_YRGB	0x0094	W	0x10001000	Win1 YRGB scaling factor
VOP_WIN1_SCL_FACTOR_CBR	0x0098	W	0x10001000	Win1 Cbr scaling factor
VOP_WIN1_SCL_OFFSET	0x009c	W	0x00000000	Win1 scaling start point offset
VOP_WIN1_SRC_ALPHA_CTRL	0x00a0	W	0x00000000	
VOP_WIN1_DST_ALPHA_CTRL	0x00a4	W	0x00000000	
VOP_WIN1_FADED_CTRL	0x00a8	W	0x00000000	
VOP_WIN1_RESERVED0	0x00ac	W	0x00000000	
VOP_WIN2_CTRL0	0x00b0	W	0x00000000	win2 ctrl register0
VOP_WIN2_CTRL1	0x00b4	W	0x00000000	win2 ctrl register0
VOP_WIN2_VIRO_1	0x00b8	W	0x01400140	Win2 virtual stride0 and virtaul stride1
VOP_WIN2_VIR2_3	0x00bc	W	0x01400140	Win2 virtual stride2 and virtaul stride3
VOP_WIN2_MST0	0x00c0	W	0x00000000	Win2 memory start address0
VOP_WIN2_DSP_INFO0	0x00c4	W	0x00ef013f	Win2 display width0/height0 on panel
VOP_WIN2_DSP_ST0	0x00c8	W	0x000a000a	Win2 display start point0 on panel
VOP_WIN2_COLOR_KEY	0x00cc	W	0x00000000	Win2 color key register
VOP_WIN2_MST1	0x00d0	W	0x00000000	Win2 memory start address1
VOP_WIN2_DSP_INFO1	0x00d4	W	0x00ef013f	Win2 display width1/height1 on panel
VOP_WIN2_DSP_ST1	0x00d8	W	0x000a000a	Win2 display start point1 on panel
VOP_WIN2_SRC_ALPHA_CTRL	0x00dc	W	0x00000000	
VOP_WIN2_MST2	0x00e0	W	0x00000000	Win2 memory start address2
VOP_WIN2_DSP_INFO2	0x00e4	W	0x00ef013f	Win2 display width2/height2 on panel
VOP_WIN2_DSP_ST2	0x00e8	W	0x000a000a	Win2 display start point2 on panel
VOP_WIN2_DST_ALPHA_CTRL	0x00ec	W	0x00000000	

Name	Offset	Size	Reset Value	Description
VOP_WIN2_MST3	0x00f0	W	0x00000000	Win2 memory start address3
VOP_WIN2_DSP_INFO3	0x00f4	W	0x00ef013f	Win2 display width3/height3 on panel
VOP_WIN2_DSP_ST3	0x00f8	W	0x000a000a	Win2 display start point3 on panel
VOP_WIN2_FADING_CTRL	0x00fc	W	0x00000000	
VOP_WIN3_CTRL0	0x0100	W	0x00000000	win0 ctrl register0
VOP_WIN3_CTRL1	0x0104	W	0x00000000	win0 ctrl register1
VOP_WIN3_VIRO_1	0x0108	W	0x01400140	Win3 virtual stride0 and virtaul stride1
VOP_WIN3_VIR2_3	0x010c	W	0x01400140	Win3 virtual stride2 and virtaul stride3
VOP_WIN3_MST0	0x0110	W	0x00000000	Win3 memory start address0
VOP_WIN3_DSP_INFO0	0x0114	W	0x00ef013f	Win3 display width0/height0 on panel
VOP_WIN3_DSP_ST0	0x0118	W	0x000a000a	Win3 display start point0 on panel
VOP_WIN3_COLOR_KEY	0x011c	W	0x00000000	Win3 color key register
VOP_WIN3_MST1	0x0120	W	0x00000000	Win3 memory start address1
VOP_WIN3_DSP_INFO1	0x0124	W	0x00ef013f	Win3 display width1/height1 on panel
VOP_WIN3_DSP_ST1	0x0128	W	0x000a000a	Win3 display start point1 on panel
VOP_WIN3_SRC_ALPHA_CTRL	0x012c	W	0x00000000	
VOP_WIN3_MST2	0x0130	W	0x00000000	Win3 memory start address2
VOP_WIN3_DSP_INFO2	0x0134	W	0x00ef013f	Win3 display width2/height2 on panel
VOP_WIN3_DSP_ST2	0x0138	W	0x000a000a	Win3 display start point2 on panel
VOP_WIN3_DST_ALPHA_CTRL	0x013c	W	0x00000000	
VOP_WIN3_MST3	0x0140	W	0x00000000	Win3 memory start address3
VOP_WIN3_DSP_INFO3	0x0144	W	0x00ef013f	Win3 display width3/height3 on panel
VOP_WIN3_DSP_ST3	0x0148	W	0x000a000a	Win3 display start point3 on panel
VOP_WIN3_FADING_CTRL	0x014c	W	0x00000000	
VOP_HWC_CTRL0	0x0150	W	0x00000000	Hwc ctrl register0
VOP_HWC_CTRL1	0x0154	W	0x00000000	Hwc ctrl register1

Name	Offset	Size	Reset Value	Description
VOP_HWC_MST	0x0158	W	0x00000000	Hwc memory start address
VOP_HWC_DSP_ST	0x015c	W	0x000a000a	Hwc display start point on panel
VOP_HWC_SRC_ALPHA_CTRL	0x0160	W	0x00000000	
VOP_HWC_DST_ALPHA_CTRL	0x0164	W	0x00000000	
VOP_HWC_FADED_CTRL	0x0168	W	0x00000000	
VOP_HWC_RESERVED1	0x016c	W	0x00000000	
VOP_POST_DSP_HACT_INFO	0x0170	W	0x000a014a	post scaler down horizontal start and end
VOP_POST_DSP_VACT_INFO	0x0174	W	0x000a00fa	Panel active horizontal scanning start point and end point
VOP_POST_SCL_FACTOR_YRGB	0x0178	W	0x10001000	post yrgb scaling factor
VOP_POST_RESERVED	0x017c	W	0x00001000	
VOP_POST_SCL_CTRL	0x0180	W	0x00000000	post scaling start point offset
VOP_POST_DSP_VACT_INFO_F1	0x0184	W	0x000a00fa	Panel active horizontal scanning start point and end point F1
VOP_DSP_HTOTAL_HS_END	0x0188	W	0x014a000a	Panel scanning horizontal width and hsync pulse end point
VOP_DSP_HACT_ST_END	0x018c	W	0x000a014a	Panel active horizontal scanning start point and end point
VOP_DSP_VTOTAL_VS_END	0x0190	W	0x00fa000a	Panel scanning vertical height and vsync pulse end point
VOP_DSP_VACT_ST_END	0x0194	W	0x000a00fa	Panel active vertical scanning start point and end point
VOP_DSP_VS_ST_END_F1	0x0198	W	0x00000000	Vertical scanning start point and vsync pulse end point of even filed in interlace mode
VOP_DSP_VACT_ST_END_F1	0x019c	W	0x00000000	Vertical scanning active start point and end point of even filed in interlace mode
VOP_PWM_CTRL	0x01a0	W	0x0000200a	PWM Control Register
VOP_PWM_PERIOD_HPR	0x01a4	W	0x00000000	PWM Period Register/High Polarity Capture Register

Name	Offset	Size	Reset Value	Description
VOP_PWM_DUTY_LPR	0x01a8	W	0x00000000	PWM Duty Register/Low Polarity Capture Register
VOP_PWM_CNT	0x01ac	W	0x00000000	PWM Counter Register
VOP_BCSH_COLOR_BAR	0x01b0	W	0x00000000	color bar config register
VOP_BCSH_BCS	0x01b4	W	0xd0010000	brightness contrast saturation*contrast config register
VOP_BCSH_H	0x01b8	W	0x01000000	sin hue and cos hue config register
VOP_BCSH_RESERVED	0x01bc	W	0x00000000	
VOP_CABC_CTRL0	0x01c0	W	0x00000000	
VOP_CABC_CTRL1	0x01c4	W	0x00000000	
VOP_CABC_GAUSS_LINE0_0	0x01c8	W	0x15110903	Register0000 Abstract
VOP_CABC_GAUSS_LINE0_1	0x01cc	W	0x00030911	Register0001 Abstract
VOP_CABC_GAUSS_LINE1_0	0x01d0	W	0x1a150b04	Register0002 Abstract
VOP_CABC_GAUSS_LINE1_1	0x01d4	W	0x00040b15	Register0003 Abstract
VOP_CABC_GAUSS_LINE2_0	0x01d8	W	0x15110903	Register0004 Abstract
VOP_CABC_GAUSS_LINE2_1	0x01dc	W	0x00030911	Register0005 Abstract
VOP_FRC_LOWER01_0	0x01e0	W	0x12844821	
VOP_FRC_LOWER01_1	0x01e4	W	0x21488412	
VOP_FRC_LOWER10_0	0x01e8	W	0xa55a9696	
VOP_FRC_LOWER10_1	0x01ec	W	0x5aa56969	
VOP_FRC_LOWER11_0	0x01f0	W	0xdeb77bed	
VOP_FRC_LOWER11_1	0x01f4	W	0xed7bb7de	
VOP_FRC_RESERVED0	0x01f8	W	0x00000000	
VOP_FRC_RESERVED1	0x01fc	W	0x00000000	
VOP_MMU_DTE_ADDR	0x0300	W	0x00000000	MMU current page Table address
VOP_MMU_STATUS	0x0304	W	0x00000000	MMU status register
VOP_MMU_COMMAND	0x0308	W	0x00000000	MMU command register
VOP_MMU_PAGE_FAULT_ADDR	0x030c	W	0x00000000	MMU logical address of last page fault
VOP_MMU_ZAP_ONE_LINE	0x0310	W	0x00000000	MMU Zap cache line register
VOP_MMU_INT_RAWSTAT	0x0314	W	0x00000000	MMU raw interrupt status register
VOP_MMU_INT_CLEAR	0x0318	W	0x00000000	MMU raw interrupt status register
VOP_MMU_INT_MASK	0x031c	W	0x00000000	MMU raw interrupt status register
VOP_MMU_INT_STATUS	0x0320	W	0x00000000	MMU raw interrupt status register
VOP_MMU_AUTO_GATING	0x0324	W	0x00000000	mmu auto gating
VOP_WIN2_LUT_ADDR	0x0400	W	0x00000000	

Name	Offset	Size	Reset Value	Description
VOP_WIN3_LUT_ADDR	0x0800	W	0x00000000	
VOP_HWC_LUT_ADDR	0x0c00	W	0x00000000	
VOP_GAMMA_LUT_ADDR	0x1000	W	0x00000000	
VOP MCU_BYPASS_WPORT	0x2200	W	0x00000000	Register0000 Abstract
VOP MCU_BYPASS_RPORT	0x2300	W	0x00000000	Register0001 Abstract

Notes: *Size* : **B** - Byte (8 bits) access, **HW** - Half WORD (16 bits) access, **W** -WORD (32 bits) access

8.4.2 Detail Register Description

VOP_REG_CFG_DONE

Address: Operational Base + offset (0x0000)

Register config done flag

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	WO	0x0	reg_load_en Lcdc register config done flag In the first setting of the register, the new value was saved into the mirror register. When all the register config finish, writing this register to enable the copyright of the mirror register to real register. Then register would be updated at the start of every frame.

VOP_VERSION_INFO

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	fpga_version
15:0	RW	0x0000	rtl_version

VOP_SYS_CTRL

Address: Operational Base + offset (0x0008)

System control register0

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23	RW	0x1	auto_gating_en LCDC layer axi-clk auto gating enable 1'b0 : disable auto gating 1'b1 : enable auto gating default auto gating enable

Bit	Attr	Reset Value	Description
22	RW	0x0	<p>vop_standby_en LCDC standby mode Writing "1" to turn LCDC into standby mode, All the layer would disable and the data transfer from frame buffer memory would stop at the end of current frame.</p> <p>The output would be blank. When writing "0" to this bit, standby mode would disable and the LCDC go back to work immediately.</p> <p>1'b0 : disable 1'b1 : enable * Black display is recommended before setting standby mode enable.</p>
21	RW	0x0	<p>vop_dma_stop LCDC DMA stop mode 1'b0 : disable 1'b1 : enable * If DMA is working, the stop mode would not be active until current bus transfer is finished.</p>
20	RW	0x0	<p>vop_mmu_en vop mmu enable signal 1'b0 : bypass mmu 1'b1 : enable mmu</p>
19:18	RW	0x0	<p>dma_burst_length DMA read Burst length 2'b00 : burst16 (burst 15 in rgb888 pack mode) 2'b01 : burst8 (burst 12 in rgb888 pack mode) 2'b10 : burst4 (burst 6 in rgb888 pack mode)</p>
17:16	RO	0x0	reserved
15	RW	0x0	<p>mipi_out_en 1'b0 : gating output clk ,data and control signal 1'b1 : mipi interface enable</p>
14	RW	0x0	<p>edp_out_en 1'b0 : gating output clk ,data and control signal 1'b1 : edp interface enable</p>
13	RW	0x0	<p>hdmi_out_en 1'b0 : gating output clk ,data and control signal 1'b1 : hdmi interface enable</p>
12	RW	0x1	<p>rgb_out_en 1'b0 : gating output clk ,data and control signal 1'b1 : rgb/lvds interface enable</p>
11	RO	0x0	reserved

Bit	Attr	Reset Value	Description
10	RW	0x0	edpi_wms_fs edpi wms mode , rame st signal write: edpi_wms_mode frame start (when other register is config done) read : wms mode hold status
9	RW	0x0	edpi_wms_mode 1'b1: mipi command mode
8	RW	0x0	edpi_halt_en mipi flow ctrl enable
7:4	RW	0x0	doub_ch_overlap_num 4'h0: overlap num 0 4'h1: overlap num 2 4'h2: overlap num 4 4'h3: overlap num 6 4'h4: overlap num 8 4'h5: overlap num 10 4'h6: overlap num 12 4'h7: overlap num 14 4'h8: overlap num 16
3	RW	0x0	doub_channel_en mipi double channel enable
2:1	RW	0x0	direct_path_layer_sel direct path layer select 2'b00 : select win0 2'b01 : select win1 2'b10 : select win2 2'b11 : select win3
0	RW	0x0	direct_path_en iep direct path enable signal 1'b0 : disable iep direct path 1'b1 : enable iep direct path

VOP_SYS_CTRL1

Address: Operational Base + offset (0x000c)

Bit	Attr	Reset Value	Description
31:18	RO	0x0	reserved
17:13	RW	0x00	axi_outstanding_max_num
12	RW	0x0	axi_max_outstanding_en
11:10	RW	0x0	noc_win_qos
9	RW	0x0	noc_qos_en
8:3	RW	0x00	noc_hurry_threshold
2:1	RW	0x0	noc_hurry_value
0	RW	0x0	noc_hurry_en

VOP_DSP_CTRL0

Address: Operational Base + offset (0x0010)

Display control register0

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23	RW	0x0	dsp_y_mir_en 1'b0 : no y_mirror 1'b1 : y_mirror
22	RW	0x0	dsp_x_mir_en 1'b0 : no x_mirror 1'b1 : x_mirror
21	RW	0x0	dsp_yuv_clip YCrCb clip 1'b0 : disable, YCbCr no clip 1'b1 : enable, YCbCr clip before YCbCr2RGB10bit *Y clip: 64~940, CbCr clip: 64~960
20	RW	0x0	dsp_ccir656_avg Cb-Cr filter in CCIR656 mode 1'b0 : drop mode 1'b1 : average mode
19	RW	0x0	dsp_black_en Black display mode When this bit enable, the pixel data output is all black (0x000000)
18	RW	0x0	dsp_blank_en Blank display mode When this bit enable, the Hsync/Vsync/Den output is blank
17	RW	0x0	dsp_out_zero Hsync/Vsync/Den output software ctrl 1'b0 : normal output 1'b1 : all output '0'
16	RW	0x0	dsp_dummy_swap Display dummy swap enable 1'b0 : B+G+R+dummy 1'b1 : dummy+B+G+R
15	RW	0x0	dsp_delta_swap Display delta swap enable 1'b0 : disable 1'b1 : enable *See detail description in Delta display chapter.
14	RW	0x0	dsp_rg_swap Display output red and green swap enable 1'b0 : RGB 1'b1 : GRB

Bit	Attr	Reset Value	Description
13	RW	0x0	dsp_rb_swap Display output red and blue swap enable 1'b0 : RGB 1'b1 : BGR
12	RW	0x0	dsp_bg_swap Display output blue and green swap enable 1'b0 : RGB 1'b1 : RBG
11	RW	0x0	dsp_field_pol field polarity when interlace dsp 1'b0 : normal 1'b1 : invert
10	RW	0x0	dsp_interlace Interlace display enable 1'b0 : disable 1'b1 : enable *This mode is related to the ITU-R656 output, the display timing of odd field must be set correctly. (lcdc_dsp_vs_st_end_f1/lcdc_dsp_vact_end_f1)
9	RW	0x0	dsp_ddr_phase dclk phase lock 1'b0 : no lock 1'b1 : lock every line
8	RW	0x0	dsp_dclk_ddr dclk output mode 1'b0 : SDR 1'b1 : DDR
7	RW	0x0	dsp_dclk_pol DCLK invert enable 1'b0 : normal 1'b1 : invert default dclk invert
6	RW	0x0	dsp_den_pol DEN polarity 1'b0 : positive 1'b1 : negative
5	RW	0x0	dsp_vsync_pol VSYNC polarity 1'b0 : negative 1'b1 : positive
4	RW	0x0	dsp_hsync_pol HSYNC polarity 1'b0 : negative 1'b1 : positive

Bit	Attr	Reset Value	Description
3:0	RW	0x0	dsp_out_mode Display output format 4'b0000: Parallel 24-bit RGB888 output R[7:0],G[7:0],B[7:0] 4'b0001: Parallel 18-bit RGB666 output 6'b0,R[5:0],G[5:0],B[5:0] 4'b0010: Parallel 16-bit RGB565 output 8'b0,R[4:0],G[5:0],B[4:0] 4'b0011: Parallel 24-bit RGB888 double pixel mix out phase0:G1[3:0],B1[7:0],G0[3:0],B0[7:0] phase1:R1[7:0],G1[7:4],R0[7:0],G0[7:4] 4'b0100: Serial 2x12-bit 12'b0,G[3:0],B[7:0] + 12'b0,R[7:0],G[7:4] 4'b0101: ITU-656 output mode0 16'b0,pixel_data[7:0] 4'b0110: ITU-656 output mode1 8'b0,pixel_data[7:0],8'b0 4'b0111: ITU-656 output mode2 9'b0,pixel_data[7:0],7'b0 4'b1000: Serial 3x8-bit RGB888 16'b0, B[7:0]+16'b0,G[7:0]+16'b0,R[7:0] 4'b1100: Serial 3x8-bit RGB888 + dummy 16'b0, B[7:0]+16'b0,G[7:0]+16'b0,R[7:0] + dummy 4'b1111: Parallel 30-bit RGBaaa output R[9:0],G[9:0],B[9:0] Others: Reserved.

VOP_DSP_CTRL1

Address: Operational Base + offset (0x0014)

Display control register1

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:14	RW	0x3	dsp_layer3_sel
13:12	RW	0x2	dsp_layer2_sel
11:10	RW	0x1	dsp_layer1_sel
9:8	RW	0x0	dsp_layer0_sel
7	RO	0x0	reserved
6	RW	0x0	dither_up_en
5	RO	0x0	reserved
4	RW	0x0	dither_down_sel dither down mode select 2'b0 : allegro 2'b1 : FRC

Bit	Attr	Reset Value	Description
3	RW	0x0	dither_down_mode Dither-down mode 1'b0 : RGB888 to RGB565 1'b1 : RGB888 to RGB666
2	RW	0x0	dither_down_en Dither-down enable 1'b0 : disable 1'b1 : enable
1	RW	0x0	pre_dither_down_en 10bit -> 8bit (allegro)
0	RW	0x0	dsp_lut_en Display LUT ram enable 1'b0 : disable 1'b1 : enable *This bit should be "0" when CPU updates the LUT, and should be "1" when Display LUT mode enable.

VOP_DSP_BG

Address: Operational Base + offset (0x0018)

background color

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x000	dsp_bg_red Background Red color
19:10	RW	0x000	dsp_bg_green Background Green color
9:0	RW	0x000	dsp_bg_blue Background Blue color

VOP MCU CTRL

Address: Operational Base + offset (0x001c)

MCU mode control register

Bit	Attr	Reset Value	Description
31	RW	0x0	mcu_type MCU LCD output SELECT
30	RW	0x0	mcu_bypass MCU LCD BYPASS MODE Select
29	RW	0x0	mcu_rs MCU LCD RS Select
28	RW	0x0	muc_frame_st Write"1" : MCU HOLD Mode Frame Start Read : MCU/LCDC standby HOLD status
27	RW	0x0	mcu_hold_mode MCU HOLD Mode Select

Bit	Attr	Reset Value	Description
26	RW	0x0	mcu_clk_sel MCU_CLK_SEL for MCU bypass 1'b1 : MCU BYPASS sync with DCLK 1'b0 : MCU BYPASS sync with HCLK
25:20	RW	0x07	mcu_rw_pend MCU_RW signal end point (0-63)
19:16	RW	0x1	mcu_rw_pst MCU_RW signal start point (0-15)
15:10	RW	0x07	mcu_cs_pend MCU_CS signal end point (0-63)
9:6	RW	0x0	mcu_cs_pst MCU_CS signal start point (0-15)
5:0	RW	0x08	mcu_pix_total MCU LCD Interface writing period (1-63)

VOP_INTR_CTRL0

Address: Operational Base + offset (0x0020)

Interrupt ctrl register0

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24:12	RW	0x0000	dsp_line_frag_num Line number of the Line flag interrupt The display line number when the flag interrupt occur, the range is (0~ DSP_VTOTAL-1).
11	WO	0x0	bus_error_intr_clr Bus error Interrupt clear (Auto clear)
10	WO	0x0	line_frag_intr_clr Line flag Interrupt clear (Auto clear)
9	WO	0x0	fs_intr_clr Frame start interrupt clear (Auto clear)
8	WO	0x0	dsp_hold_valid_intr_clr display hold valid interrupt clear (Auto clear)
7	RW	0x0	bus_error_intr_en Bus error interrupt enable 1'b0 : disable 1'b1 : enable
6	RW	0x0	line_frag_intr_en Line flag Interrupt enable 1'b0 : disable 1'b1 : enable
5	RW	0x0	fs_intr_en Frame start interrupt enable 1'b0 : disable 1'b1 : enable

Bit	Attr	Reset Value	Description
4	RW	0x0	dsp_hold_valid_intr_en display hold valid interrupt enable 1'b0 : disable 1'b1 : enable
3	RO	0x0	bus_error_intr_sts Bus error Interrupt status
2	RO	0x0	line_frag_intr_sts Line flag Interrupt status
1	RO	0x0	fs_intr_sts Frame start interrupt status
0	RO	0x0	dsp_hold_valid_intr_sts display hold valid interrupt status

VOP_INTR_CTRL1

Address: Operational Base + offset (0x0024)

Interrupt ctrl register1

Bit	Attr	Reset Value	Description
31:23	RO	0x0	reserved
22	RW	0x0	pwm_gen_intr_clr
21	RW	0x0	post_buf_empty_intr_clr post line buffer empty interrupt clear(auto clear)
20	RW	0x0	hwc_empty_intr_clr hwc data empty interrupt clear(auto clear)
19	RW	0x0	win3_empty_intr_clr win3 data empty interrupt clear(auto clear)
18	RW	0x0	win2_empty_intr_clr win2 data empty interrupt clear(auto clear)
17	RW	0x0	win1_empty_intr_clr win1 data empty interrupt clear(auto clear)
16	W1C	0x0	win0_empty_intr_clr win0 data empty interrupt clear(auto clear)
15	RO	0x0	reserved
14	RW	0x0	pwm_gen_intr_en
13	RW	0x0	post_buf_empty_intr_en post line buffer empty interrupt enable signal 1'b0 : disable 1'b1 : enable
12	RW	0x0	hwc_empty_intr_en hwc data empty interrupt enable signal 1'b0 : disable 1'b1 : enable

Bit	Attr	Reset Value	Description
11	RW	0x0	win3_empty_intr_en win3 data empty interrupt enable signal 1'b0 : disable 1'b1 : enable
10	RW	0x0	win2_empty_intr_en win2 data empty interrupt enable signal 1'b0 : disable 1'b1 : enable
9	RW	0x0	win1_empty_intr_en win1 data empty interrupt enable signal 1'b0 : disable 1'b1 : enable
8	RW	0x0	win0_empty_intr_en win0 data empty interrupt enable signal 1'b0 : disable 1'b1 : enable
7	RO	0x0	reserved
6	RW	0x0	pwm_gen_intr_sts pwm generated interrupt 0: Channel 0 Interrupt not generated 1: Channel 0 Interrupt generated
5	RW	0x0	post_buf_empty_intr_sts post buffer empty interrupt status
4	RW	0x0	hwc_empty_intr_sts hwc data empty interrupt status
3	RW	0x0	win3_empty_intr_sts win3 data empty interrupt status
2	RW	0x0	win2_empty_intr_sts win2 data empty interrupt status
1	RW	0x0	win1_empty_intr_sts win1 data empty interrupt status
0	RO	0x0	win0_empty_intr_sts win0 data empty interrupt status

VOP_INTR_RESERVED0

Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	reserved

VOP_INTR_RESERVED1

Address: Operational Base + offset (0x002c)

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	reserved

VOP_WIN0_CTRL0

Address: Operational Base + offset (0x0030)

win0 ctrl register0

Bit	Attr	Reset Value	Description
31:21	RO	0x0	reserved
20	RW	0x0	win0_yuv_clip YCrCb clip 1'b0 : disable, YCbCr no clip 1'b1 : enable, YCbCr clip before YCbCr2RGB *Y clip: 16~235, CbCr clip: 16~239
19	RW	0x0	win0_cbr_deflick Win0 Cbr deflick mode 1'b0 : disable 1'b1 : enable
18	RW	0x0	win0_yrgb_deflick win0 YRGB deflick mode 1'b0 : disable 1'b1 : enable
17	RO	0x0	reserved
16	RW	0x0	win0_ppas_zero_en 0:per_pix_alpha+scale,pix not change; 1:per_pix_alpha_scale,pix=0 when alpha=0;
15	RW	0x0	win0_uv_swap Win0 CbCr swap 1'b0 : CrCb 1'b1 : CbCr
14	RW	0x0	win0_mid_swap Win0 Y middle swap 1'b0 : Y3Y2Y1Y0 1'b1 : Y3Y1Y2Y0
13	RW	0x0	win0_alpha_swap win0 alpha swap 1'b0 : ARGB 1'b1 : RGBA
12	RW	0x0	win0_rb_swap win0 RGB RED and BLUE swap 1'b0 : RGB 1'b1 : BGR

Bit	Attr	Reset Value	Description
11:10	RW	0x0	win0_csc_mode Win0 YUV2RGB Color space conversion: 2'b00/01 : mpeg 2'b10 : jpeg 2'b11 : hd
9	RW	0x0	win0_no_outstanding win0 AXI master read outstanding 1'b0 : enable 1'b1 : disable
8	RW	0x0	win0_interlace_read Win0 interlace read mode 1'b0 : disable 1'b1 : enable
7:5	RW	0x2	win0_lb_mode
4	RW	0x0	win0_fmt_10 0: yuv 8bit fmt mode 1: yuv 10bit fmt mode
3:1	RW	0x0	win0_data_fmt 3'b000 : ARGB888 3'b001 : RGB888 3'b010 : RGB565 3'b100 : YcbCr420 3'b101 : YcbCr422 3'b110 : YcbCr444
0	RW	0x0	win0_en

VOP_WIN0_CTRL1

Address: Operational Base + offset (0x0034)

win1 ctrl register1

Bit	Attr	Reset Value	Description
31	RW	0x0	win0_cbr_vsd_mode win0 vertical scaler down mode select 1'b0 : bilinear 1'b1 : average
30	RW	0x0	win0_cbr_vsu_mode win0 vertical scaler down mode select 1'b0 : bilinear 1'b1 : bicubic
29:28	RW	0x0	win0_cbr_hsd_mode win0 horizontal scaler down mode select 2'b00 : bilinear 2'b01 : bicubic 2'b10 : average
27:26	RW	0x0	win0_cbr_ver_scl_mode

Bit	Attr	Reset Value	Description
25:24	RW	0x0	win0_cbr_hor_scl_mode 2'b00 : no scale 2'b01 : scale up 2'b10 : scale down 2'b11 : no scale
23	RW	0x0	win0_yrgb_vsd_mode win0 vertical scaler down mode select 1'b0 : bilinear 1'b1 : average
22	RW	0x0	win0_yrgb_vsu_mode win0 vertical scaler down mode select 1'b0 : bilinear 1'b1 : bicubic
21:20	RW	0x0	win0_yrgb_hsd_mode win0 horizontal scaler down mode select 2'b00 : bilinear 2'b01 : average
19:18	RW	0x0	win0_yrgb_ver_scl_mode 2'b00 : no scale 2'b01 : scale up 2'b10 : scale down 2'b11 : no scale
17:16	RW	0x0	win0_yrgb_hor_scl_mode 2'b00 : no scale 2'b01 : scale up 2'b10 : scale down 2'b11 : no scale
15	RW	0x0	win0_line_load_mode when yuv fmt,if 1'b0: load data by axi trans 1'b1: load data by lines
14:12	RW	0x0	win0_cbr_axi_gather_num
11:8	RW	0x0	win0_yrgb_axi_gather_num
7	RW	0x0	win0_vsd_cbr_gt2
6	RW	0x0	win0_vsd_cbr_gt4
5	RW	0x0	win0_vsd_yrgb_gt2
4	RW	0x0	win0_vsd_yrgb_gt4
3:2	RW	0x0	win0_bic_coe_sel 2'b00 : PRECISE 2'b01 : SPLINE 2'b10 : CATROM 2'b11 : MITCHELL
1	RW	0x0	win0_cbr_axi_gather_en
0	RW	0x0	win0_yrgb_axi_gather_en

VOP_WIN0_COLOR_KEY

Address: Operational Base + offset (0x0038)

Win0 color key register

Bit	Attr	Reset Value	Description
31	RW	0x0	win0_key_en Win0 transparency color key enable 1'b0 : disable; 1'b1 : enable;
30	RO	0x0	reserved
29:0	RW	0x00000000	win0_key_color Win0 key color

VOP_WIN0_VIR

Address: Operational Base + offset (0x003c)

Win0 virtual stride

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	win0_vir_stride_uv
15:14	RO	0x0	reserved
13:0	RW	0x0140	win0_vir_stride Win0 Virtual stride Number of words of Win0 Virtual width ARGB888 : win0_vir_width RGB888 : (win0_vir_width*3/4) + (win0_vir_width%3) RGB565 : ceil(win0_vir_width/2) YUV : ceil(win0_vir_width/4)

VOP_WIN0_YRGB_MST

Address: Operational Base + offset (0x0040)

Win0 YRGB memory start address

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	win0_yrgb_mst win0 YRGB frame buffer memory start address

VOP_WIN0_CBR_MST

Address: Operational Base + offset (0x0044)

Win0 Cbr memory start address

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	win0_cbr_mst win0 CBR frame buffer memory start address

VOP_WIN0_ACT_INFO

Address: Operational Base + offset (0x0048)

Win0 active window width/height

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x00ef	win0_act_height Win0 active(original) window height win_act_height = (win0 vertical size -1)
15:13	RO	0x0	reserved
12:0	RW	0x013f	win0_act_width Win0 active(original) window width win_act_width = (win0 horizontal size -1)

VOP_WIN0_DSP_INFO

Address: Operational Base + offset (0x004c)

Win0 display width/height on panel

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x0ef	win0_dsp_height Win0 display window height win0_dsp_height = (win0 vertical size -1)
15:12	RO	0x0	reserved
11:0	RW	0x13f	win0_dsp_width Win0 display window width win0_dsp_width = (win0 horizontal size -1)

VOP_WIN0_DSP_ST

Address: Operational Base + offset (0x0050)

Win0 display start point on panel

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x000a	win0_dsp_yst Win0 vertical start point(y) of the Panel scanning
15:13	RO	0x0	reserved
12:0	RW	0x000a	win0_dsp_xst Win0 horizontal start point(x) of the Panel scanning

VOP_WIN0_SCL_FACTOR_YRGB

Address: Operational Base + offset (0x0054)

Win0 YRGB scaling factor

Bit	Attr	Reset Value	Description
31:16	RW	0x1000	win0_vs_factor_yrgb Win0 YRGB vertical scaling factor: factor=((LCDC_WIN0_ACT_INFO[31:16]) /(LCDC_WIN0_DSP_INFO[31:16]))*2^12

Bit	Attr	Reset Value	Description
15:0	RW	0x1000	win0_hs_factor_yrgb Win0 YRGB horizontal scaling factor: factor=((LCDC_WIN0_ACT_INFO[15:0]) /(LCDC_WIN0_DSP_INFO[15:0]))*2^12

VOP_WIN0_SCL_FACTOR_CBR

Address: Operational Base + offset (0x0058)

Win0 Cbr scaling factor

Bit	Attr	Reset Value	Description
31:16	RW	0x1000	win0_vs_factor_cbr Win0 CBR vertical scaling factor: YCbCr420: factor=((LCDC_WIN0_ACT_INFO[31:16]/ 2) /(LCDC_WIN0_DSP_INFO[31:16]))*2^12 YCbCr422,YCbCr444: factor=((LCDC_WIN0_ACT_INFO[31:16]) /(LCDC_WIN0_DSP_INFO[31:16]))*2^12
15:0	RW	0x1000	win0_hs_factor_cbr Win0 CBR horizontal scaling factor: YCbCr422,YCbCr420: factor=((LCDC_WIN0_ACT_INFO[15:0]/2) /(LCDC_WIN0_DSP_INFO[15:0]))*2^12 YCbCr444: factor=((LCDC_WIN0_ACT_INFO[15:0]) /(LCDC_WIN0_DSP_INFO[15:0]))*2^12

VOP_WIN0_SCL_OFFSET

Address: Operational Base + offset (0x005c)

Win0 scaling start point offset

Bit	Attr	Reset Value	Description
31:24	RW	0x00	win0_vs_offset_cbr Cbr Vertical scaling start point offset (0x00~0xff)/0x100 = 0~0.99
23:16	RW	0x00	win0_vs_offset_yrgb Y Vertical scaling start point offset (0x00~0xff)/0x100 = 0~0.99
15:8	RW	0x00	win0_hs_offset_cbr Cbr Horizontal scaling start point offset (0x00~0xff)/0x100 = 0~0.99
7:0	RW	0x00	win0_hs_offset_yrgb Y Horizontal scaling start point offset (0x00~0xff)/0x100 = 0~0.99

VOP_WIN0_SRC_ALPHA_CTRL

Address: Operational Base + offset (0x0060)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	win0_fading_value
23:16	RW	0x00	win0_src_global_alpha layer0 src global alpha (eused by fading value)
15:9	RO	0x0	reserved
8:6	RW	0x0	win0_src_factor_m0
5	RW	0x0	win0_src_alpha_cal_m0
4:3	RW	0x0	win0_src_blend_m0
2	RW	0x0	win0_src_alpha_m0
1	RW	0x0	win0_src_color_m0
0	RW	0x0	win0_src_alpha_en

VOP_WIN0_DST_ALPHA_CTRL

Address: Operational Base + offset (0x0064)

Bit	Attr	Reset Value	Description
31:9	RO	0x0	reserved
8:6	RW	0x0	win0_dst_factor_m0
5:0	RW	0x00	win0_dst_m0_reserved

VOP_WIN0_FADING_CTRL

Address: Operational Base + offset (0x0068)

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24	RW	0x0	layer0_fading_en
23:16	RW	0x00	layer0_fading_offset_b
15:8	RW	0x00	layer0_fading_offset_g
7:0	RW	0x00	layer0_fading_offset_r

VOP_WIN0_RESERVED0

Address: Operational Base + offset (0x006c)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	reserved

VOP_WIN1_CTRL0

Address: Operational Base + offset (0x0070)

win1 ctrl register0

Bit	Attr	Reset Value	Description
31:21	RO	0x0	reserved

Bit	Attr	Reset Value	Description
20	RW	0x0	win1_yuv_clip YCrCb clip 1'b0 : disable, YCbCr no clip 1'b1 : enable, YCbCr clip before YCbCr2RGB *Y clip: 16~235, CbCr clip: 16~239
19	RW	0x0	win1_cbr_deflick Win1 Cbr deflick mode 1'b0 : disable 1'b1 : enable
18	RW	0x0	win1_yrgb_deflick win1 YRGB deflick mode 1'b0 : disable 1'b1 : enable
17	RO	0x0	reserved
16	RW	0x0	win1_ppas_zero_en 0:per_pix_alpha+scale,pix not change; 1:per_pix_alpha_scale,pix=0 when alpha=0;
15	RW	0x0	win1_uv_swap Win1 CbCr swap 1'b0 : CrCb 1'b1 : CbCr
14	RW	0x0	win1_mid_swap Win1 Y middle 8-bit swap 1'b0 : Y3Y2Y1Y0 1'b1 : Y3Y1Y2Y0
13	RW	0x0	win1_alpha_swap win1 alpha swap 1'b0 : ARGB 1'b1 : RGBA
12	RW	0x0	win1_rb_swap win1 RGB RED and BLUE swap 1'b0 : RGB 1'b1 : BGR
11:10	RW	0x0	win1_csc_mode Win1 YUV2RGB Color space conversion: 2'b00/01 : mpeg 2'b10 : jpeg 2'b11 : hd
9	RW	0x0	win1_no_outstanding win1 AXI master read outstanding 1'b0 : enable 1'b1 : disable

Bit	Attr	Reset Value	Description
8	RW	0x0	win1_interlace_read Win1 interlace read mode 1'b0 : disable 1'b1 : enable
7:5	RW	0x2	win1_lb_mode
4	RW	0x0	win1_fmt_10 0: yuv 8bit fmt mode 1: yuv 10bit fmt mode
3:1	RW	0x0	win1_data_fmt 3'b000 : ARGB888 3'b001 : RGB888 3'b010 : RGB565 3'b100 : YcbCr420 3'b101 : YcbCr422 3'b110 : YcbCr444
0	RW	0x0	win1_en

VOP_WIN1_CTRL1

Address: Operational Base + offset (0x0074)

win1 ctrl register1

Bit	Attr	Reset Value	Description
31	RW	0x0	win1_cbr_vsd_mode win1 vertical scaler down mode select 1'b0 : bilinear 1'b1 : average
30	RW	0x0	win1_cbr_vsu_mode win1 vertical scaler up mode select 1'b0 : bilinear 1'b1 : bicubic
29:28	RW	0x0	win1_cbr_hsd_mode win1 horizontal scaler down mode select 2'b00 : bilinear 2'b01 : bicubic 2'b10 : average
27:26	RW	0x0	win1_cbr_ver_scl_mode 2'b00 : no scale 2'b01 : scale up 2'b10 : scale down 2'b11 : no scale
25:24	RW	0x0	win1_cbr_hor_scl_mode 2'b00 : no scale 2'b01 : scale up 2'b10 : scale down 2'b11 : no scale

Bit	Attr	Reset Value	Description
23	RW	0x0	win1_yrgb_vsd_mode win1 vertical scaler down mode select 1'b0 : bilinear 1'b1 : average
22	RW	0x0	win1_yrgb_vsu_mode win1 vertical scaler up mode select 1'b0 : bilinear 1'b1 : bicubic
21:20	RW	0x0	win1_yrgb_hsd_mode win1 horizontal scaler down mode select 2'b00 : bilinear 2'b01 : average
19:18	RW	0x0	win1_yrgb_ver_scl_mode 2'b00 : no scale 2'b01 : scale up 2'b10 : scale down 2'b11 : no scale
17:16	RW	0x0	win1_yrgb_hor_scl_mode 2'b00 : no scale 2'b01 : scale up 2'b10 : scale down 2'b11 : no scale
15	RW	0x0	win1_line_load_mode when yuv fmt,if 1'b0: load data by pixels 1'b1: load data by lines
14:12	RW	0x0	win1_cbr_axi_gather_num
11:8	RW	0x0	win1_yrgb_axi_gather_num
7	RW	0x0	win1_vsd_cbr_gt2
6	RW	0x0	win1_vsd_cbr_gt4
5	RW	0x0	win1_vsd_yrgb_gt2
4	RW	0x0	win1_vsd_yrgb_gt4
3:2	RW	0x0	win1_bic_coe_sel 2'b00 : PRECISE 2'b01 : SPLINE 2'b10 : CATROM 2'b11 : MITCHELL
1	RW	0x0	win1_cbr_axi_gather_en
0	RW	0x0	win1_yrgb_axi_gather_en

VOP_WIN1_COLOR_KEY

Address: Operational Base + offset (0x0078)

Win1 color key register

Bit	Attr	Reset Value	Description
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Bit	Attr	Reset Value	Description
31	RW	0x0	win1_key_en Win1 transparency color key enable 1'b0 : disable; 1'b1 : enable;
30	RO	0x0	reserved
29:0	RW	0x00000000	win1_key_color Win1 key color

VOP_WIN1_VIR

Address: Operational Base + offset (0x007c)

Win1 virtual stride

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	win1_vir_stride_uv
15:14	RO	0x0	reserved
13:0	RW	0x0140	win1_vir_stride Win1 Virtual stride Number of words of Win1 Virtual width ARGB888 : win1_vir_width RGB888 : (win1_vir_width*3/4) + (win1_vir_width%3) RGB565 : ceil(win1_vir_width/2) YUV : ceil(win1_vir_width/4)

VOP_WIN1_YRGB_MST

Address: Operational Base + offset (0x0080)

Win1 YRGB memory start address

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	win1_yrgb_mst win1 YRGB frame buffer memory start address

VOP_WIN1_CBR_MST

Address: Operational Base + offset (0x0084)

Win1 Cbr memory start address

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	win1_cbr_mst win1 CBR frame buffer memory start address

VOP_WIN1_ACT_INFO

Address: Operational Base + offset (0x0088)

Win1 active window width/height

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved

Bit	Attr	Reset Value	Description
28:16	RW	0x00ef	win1_act_height Win1 active(original) window height win_act_height = (win1 vertical size -1)
15:13	RO	0x0	reserved
12:0	RW	0x013f	win1_act_width Win1 active(original) window width win_act_width = (win1 horizontal size -1)

VOP_WIN1_DSP_INFO

Address: Operational Base + offset (0x008c)

Win1 display width/height on panel

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x0ef	win1_dsp_height Win1 display window height win1_dsp_height = (win1 vertical size -1)
15:12	RO	0x0	reserved
11:0	RW	0x13f	win1_dsp_width Win1 display window width win1_dsp_width = (win1 horizontal size -1)

VOP_WIN1_DSP_ST

Address: Operational Base + offset (0x0090)

Win1 display start point on panel

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x000a	win1_dsp_yst Win1 vertical start point(y) of the Panel scanning
15:13	RO	0x0	reserved
12:0	RW	0x000a	win1_dsp_xst Win1 horizontal start point(x) of the Panel scanning

VOP_WIN1_SCL_FACTOR_YRGB

Address: Operational Base + offset (0x0094)

Win1 YRGB scaling factor

Bit	Attr	Reset Value	Description
31:16	RW	0x1000	win1_vs_factor_yrgb Win1 YRGB vertical scaling factor: factor=((LCDC_WIN1_ACT_INFO[31:16]) /(LCDC_WIN1_DSP_INFO[31:16]))*2^12
15:0	RW	0x1000	win1_hs_factor_yrgb Win1 YRGB horizontal scaling factor: factor=((LCDC_WIN1_ACT_INFO[15:0]) /(LCDC_WIN1_DSP_INFO[15:0]))*2^12

VOP_WIN1_SCL_FACTOR_CBR

Address: Operational Base + offset (0x0098)

Win1 Cbr scaling factor

Bit	Attr	Reset Value	Description
31:16	RW	0x1000	win1_vs_factor_cbr Win1 Cbr vertical scaling factor: YCbCr420: factor=((LCDC_WIN1_ACT_INFO[31:16]/ 2) /(LCDC_WIN1_DSP_INFO[31:16]))*2^12 YCbCr422,YCbCr444: factor=((LCDC_WIN1_ACT_INFO[31:16]) /(LCDC_WIN1_DSP_INFO[31:16]))*2^12
15:0	RW	0x1000	win1_hs_factor_cbr Win1 Cbr horizontal scaling factor: YCbCr422,YCbCr420: factor=((LCDC_WIN1_ACT_INFO[15:0]/2) /(LCDC_WIN1_DSP_INFO[15:0]))*2^12 YCbCr444: factor=((LCDC_WIN1_ACT_INFO[15:0]) /(LCDC_WIN1_DSP_INFO[15:0]))*2^12

VOP_WIN1_SCL_OFFSET

Address: Operational Base + offset (0x009c)

Win1 scaling start point offset

Bit	Attr	Reset Value	Description
31:24	RW	0x00	win1_vs_offset_cbr Cbr Vertical scaling start point offset (0x00~0xff)/0x100 = 0~0.99
23:16	RW	0x00	win1_vs_offset_yrgb Y Vertical scaling start point offset (0x00~0xff)/0x100 = 0~0.99
15:8	RW	0x00	win1_hs_offset_cbr Cbr Horizontal scaling start point offset (0x00~0xff)/0x100 = 0~0.99
7:0	RW	0x00	win1_hs_offset_yrgb Y Horizontal scaling start point offset (0x00~0xff)/0x100 = 0~0.99

VOP_WIN1_SRC_ALPHA_CTRL

Address: Operational Base + offset (0x00a0)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	win1_fading_value

Bit	Attr	Reset Value	Description
23:16	RW	0x00	win1_src_global_alpha layer0 src global alpha (eused by fading value)
15:9	RO	0x0	reserved
8:6	RW	0x0	win1_src_factor_m0
5	RW	0x0	win1_src_alpha_cal_m0
4:3	RW	0x0	win1_src_blend_m0
2	RW	0x0	win1_src_alpha_m0
1	RW	0x0	win1_src_color_m0
0	RW	0x0	win1_src_alpha_en

VOP_WIN1_DST_ALPHA_CTRL

Address: Operational Base + offset (0x00a4)

Bit	Attr	Reset Value	Description
31:9	RO	0x0	reserved
8:6	RW	0x0	win1_dst_factor_m0
5:0	RW	0x00	win1_dsp_m0_reserved

VOP_WIN1_FADING_CTRL

Address: Operational Base + offset (0x00a8)

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24	RW	0x0	win1_fading_en
23:16	RW	0x00	win1_fading_offset_b
15:8	RW	0x00	win1_fading_offset_g
7:0	RW	0x00	win1_fading_offset_r

VOP_WIN1_RESERVED0

Address: Operational Base + offset (0x00ac)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	reserved

VOP_WIN2_CTRL0

Address: Operational Base + offset (0x00b0)

win2 ctrl register0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved

Bit	Attr	Reset Value	Description
18	RW	0x0	<p>win2_lut_en Win2 LUT ram enable 1'b0 : disable 1'b1 : enable *This bit should be "0" when CPU updates the LUT, and should be "1" when Win1 LUT mode enable.</p>
17:15	RO	0x0	reserved
14	RW	0x0	<p>win2_endian_swap Win2 8pp palette data Big-endian/ Little-endian select 1'b0 : Big-endian 1'b1 : Little-endian</p>
13	RW	0x0	<p>win2_alpha_swap Win2 RGB alpha swap 1'b0 : ARGB 1'b1 : RGBA</p>
12	RW	0x0	<p>win2_rb_swap Win2 RGB Red and Blue swap 1'b0 : RGB 1'b1 : BGR</p>
11	RO	0x0	reserved
10	RW	0x0	<p>win2_csc_mode Win2 RGB2YUV Color space conversion: 1'b0 : no CSC 1'b1 : RGB2YUV</p>
9	RW	0x0	<p>win2_no_outstanding Win2 AXI master read outstanding 1'b0 : enable 1'b1 : disable</p>
8	RW	0x0	<p>win2_interlace_read Win2 interlace read mode 1'b0 : disable 1'b1 : enable</p>
7	RW	0x0	<p>win2_mst3_en win2 master3 enable</p>
6	RW	0x0	<p>win2_mst2_en win2 master2 enable</p>
5	RW	0x0	<p>win2_mst1_en win2 master1 enable</p>
4	RW	0x0	<p>win2_mst0_en win2 master0 enable</p>

Bit	Attr	Reset Value	Description
3:1	RW	0x0	win2_data_fmt 3'b000 : ARGB888 3'b001 : RGB888 3'b010 : RGB565 3'b100: 8bpp 3'b101: 4bpp 3'b110: 2bpp 3'b111: 1bpp
0	RW	0x0	win2_en

VOP_WIN2_CTRL1

Address: Operational Base + offset (0x00b4)

win2 ctrl register0

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:4	RW	0x0	win2_axi_gather_num
3:1	RO	0x0	reserved
0	RW	0x0	win2_axi_gather_en

VOP_WIN2_VIRO_1

Address: Operational Base + offset (0x00b8)

Win2 virtual stride0 and virtaul stride1

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0140	win2_vir_stride1 Win2 Virtual stride1 Number of words of Win2 Virtual1 width ARGB888 : win2_vir_width1 RGB888 : (win2_vir_width1 * 3/4) + (win2_vir_width1 % 3) RGB565 : ceil(win2_vir_width1 / 2) 8BPP : ceil(win2_vir_width1 / 4) 4BPP : ceil(win2_vir_width1 / 8) 2BPP : ceil(win2_vir_width1 / 16) 1BPP : ceil(win2_vir_width1 / 32)
15:13	RO	0x0	reserved

Bit	Attr	Reset Value	Description
12:0	RW	0x0140	win2_vir_stride0 Win2 Virtual stride0 Number of words of Win2 Virtual0 width ARGB888 : win2_vir_width0 RGB888 : (win2_vir_width0 * 3/4) + (win2_vir_width0 % 3) RGB565 : ceil(win2_vir_width0 / 2) 8BPP : ceil(win2_vir_width0 / 4) 4BPP : ceil(win2_vir_width0 / 8) 2BPP : ceil(win2_vir_width0 / 16) 1BPP : ceil(win2_vir_width0 / 32)

VOP_WIN2_VIR2_3

Address: Operational Base + offset (0x00bc)

Win2 virtual stride2 and virtaul stride3

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0140	win2_vir_stride3 Win2 Virtual stride3 Number of words of Win2 Virtual3 width ARGB888 : win2_vir_width3 RGB888 : (win2_vir_width3 * 3/4) + (win2_vir_width3 % 3) RGB565 : ceil(win2_vir_width3 / 2) 8BPP : ceil(win2_vir_width3 / 4) 4BPP : ceil(win2_vir_width3 / 8) 2BPP : ceil(win2_vir_width3 / 16) 1BPP : ceil(win1_vir_width3 / 32)
15:13	RO	0x0	reserved
12:0	RW	0x0140	win2_vir_stride2 Win2 Virtual stride2 Number of words of Win2 Virtual2 width ARGB888 : win2_vir_width2 RGB888 : (win2_vir_width2 * 3/4) + (win2_vir_width2 % 3) RGB565 : ceil(win2_vir_width2 / 2) 8BPP : ceil(win2_vir_width2 / 4) 4BPP : ceil(win2_vir_width2 / 8) 2BPP : ceil(win2_vir_width2 / 16) 1BPP : ceil(win1_vir_width2 / 32)

VOP_WIN2_MST0

Address: Operational Base + offset (0x00c0)

Win2 memory start address0

Bit	Attr	Reset Value	Description
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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	win2_mst0 Win2 frame buffer memory start address0 *must be aliased to 8byte address

VOP_WIN2_DSP_INFO0

Address: Operational Base + offset (0x00c4)

Win2 display width0/height0 on panel

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x0ef	win2_dsp_height0 Win2 display window height0 win2_dsp_height0 = size -1
15:12	RO	0x0	reserved
11:0	RW	0x13f	win2_dsp_width0 Win2 display window width0 win2_dsp_width = size -1

VOP_WIN2_DSP_ST0

Address: Operational Base + offset (0x00c8)

Win2 display start point0 on panel

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x000a	win2_dsp_yst0 Win2 vertical start point(y) of the Panel scanning
15:13	RO	0x0	reserved
12:0	RW	0x000a	win2_dsp_xst0 Win2 horizontal start point(x) of the Panel scanning

VOP_WIN2_COLOR_KEY

Address: Operational Base + offset (0x00cc)

Win2 color key register

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24	RW	0x0	win2_key_en Win2 transparency color key enable 1'b0 : disable; 1'b1 : enable;
23:0	RW	0x000000	win2_key_color Win2 key color

VOP_WIN2_MST1

Address: Operational Base + offset (0x00d0)

Win2 memory start address1

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	win2_mst1 Win2 frame buffer memory start address1 *must be aliased to 8byte address

VOP_WIN2_DSP_INFO1

Address: Operational Base + offset (0x00d4)

Win2 display width1/height1 on panel

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x0ef	win2_dsp_height1 Win2 display window height1 win2_dsp_height0 = size -1
15:12	RO	0x0	reserved
11:0	RW	0x13f	win2_dsp_width1 Win2 display window width1 win2_dsp_width = size -1

VOP_WIN2_DSP_ST1

Address: Operational Base + offset (0x00d8)

Win2 display start point1 on panel

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x000a	win2_dsp_yst1 Win2 vertical start point(y) of the Panel scanning
15:13	RO	0x0	reserved
12:0	RW	0x000a	win2_dsp_xst1 Win2 horizontal start point(x) of the Panel scanning

VOP_WIN2_SRC_ALPHA_CTRL

Address: Operational Base + offset (0x00dc)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	win2_fading_value
23:16	RW	0x00	win2_src_global_alpha layer0 src global alpha (reused by fading value)
15:9	RO	0x0	reserved
8:6	RW	0x0	win2_src_factor_m0
5	RW	0x0	win2_src_alpha_cal_m0
4:3	RW	0x0	win2_src_blend_m0
2	RW	0x0	win2_src_alpha_m0
1	RW	0x0	win2_src_color_m0
0	RW	0x0	win2_src_alpha_en

VOP_WIN2_MST2

Address: Operational Base + offset (0x00e0)

Win2 memory start address2

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	win2_mst2 Win2 frame buffer memory start address2 *must be aliased to 8byte address

VOP_WIN2_DSP_INFO2

Address: Operational Base + offset (0x00e4)

Win2 display width2/height2 on panel

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x0ef	win2_dsp_height2 Win2 display window height2 win2_dsp_height0 = size -1
15:12	RO	0x0	reserved
11:0	RW	0x13f	win2_dsp_width2 Win2 display window width2 win2_dsp_width = size -1

VOP_WIN2_DSP_ST2

Address: Operational Base + offset (0x00e8)

Win2 display start point2 on panel

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x000a	win2_dsp_yst2 Win2 vertical start point(y) of the Panel scanning
15:13	RO	0x0	reserved
12:0	RW	0x000a	win2_dsp_xst2 Win2 horizontal start point(x) of the Panel scanning

VOP_WIN2_DST_ALPHA_CTRL

Address: Operational Base + offset (0x00ec)

Bit	Attr	Reset Value	Description
31:9	RO	0x0	reserved
8:6	RW	0x0	win2_dst_factor_m0
5:0	RW	0x00	win2_dst_m0_reserved

VOP_WIN2_MST3

Address: Operational Base + offset (0x00f0)

Win2 memory start address3

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	win2_mst3 Win2 frame buffer memory start address3 *must be aliased to 8byte address

VOP_WIN2_DSP_INFO3

Address: Operational Base + offset (0x00f4)

Win2 display width3/height3 on panel

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x0ef	win2_dsp_height3 Win2 display window height3 win2_dsp_height0 = size -1
15:12	RO	0x0	reserved
11:0	RW	0x13f	win2_dsp_width3 Win2 display window width3 win2_dsp_width = size -1

VOP_WIN2_DSP_ST3

Address: Operational Base + offset (0x00f8)

Win2 display start point3 on panel

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x000a	win2_dsp_yst3 Win2 vertical start point(y) of the Panel scanning
15:13	RO	0x0	reserved
12:0	RW	0x000a	win2_dsp_xst3 Win2 horizontal start point(x) of the Panel scanning

VOP_WIN2_FADING_CTRL

Address: Operational Base + offset (0x00fc)

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24	RW	0x0	win2_fading_en
23:16	RW	0x00	win2_fading_offset_b
15:8	RW	0x00	win2_fading_offset_g
7:0	RW	0x00	win2_fading_offset_r

VOP_WIN3_CTRL0

Address: Operational Base + offset (0x0100)

win0 ctrl register0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved

Bit	Attr	Reset Value	Description
18	RW	0x0	<p>win3_lut_en Win3 LUT ram enable 1'b0 : disable 1'b1 : enable *This bit should be "0" when CPU updates the LUT, and should be "1" when Win1 LUT mode enable.</p>
17:15	RO	0x0	reserved
14	RW	0x0	<p>win3_endian_swap Win3 8pp palette data Big-endian/ Little-endian select 1'b0 : Big-endian 1'b1 : Little-endian</p>
13	RW	0x0	<p>win3_alpha_swap Win3 RGB alpha swap 1'b0 : ARGB 1'b1 : RGBA</p>
12	RW	0x0	<p>win3_rb_swap Win3 RGB Red and Blue swap 1'b0 : RGB 1'b1 : BGR</p>
11	RO	0x0	reserved
10	RW	0x0	<p>win3_csc_mode Win3 RGB2YUV Color space conversion: 1'b0 : no CSC 1'b1 : RGB2YUV</p>
9	RW	0x0	<p>win3_no_outstanding Win3 AXI master read outstanding 1'b0 : enable 1'b1 : disable</p>
8	RW	0x0	<p>win3_interlace_read Win3 interlace read mode 1'b0 : disable 1'b1 : enable</p>
7	RW	0x0	<p>win3_mst3_en win3 master3 enable</p>
6	RW	0x0	<p>win3_mst2_en win3 master2 enable</p>
5	RW	0x0	<p>win3_mst1_en win3 master1 enable</p>
4	RW	0x0	<p>win3_mst0_en win3 master0 enable</p>

Bit	Attr	Reset Value	Description
3:1	RW	0x0	win3_data_fmt 3'b000 : ARGB888 3'b001 : RGB888 3'b010 : RGB565 3'b100: 8bpp 3'b101: 4bpp 3'b110: 2bpp 3'b111: 1bpp
0	RW	0x0	win3_en

VOP_WIN3_CTRL1

Address: Operational Base + offset (0x0104)

win0 ctrl register1

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:4	RW	0x0	win3_axi_gather_num
3:1	RO	0x0	reserved
0	RW	0x0	win3_axi_gather_en

VOP_WIN3_VIRO_1

Address: Operational Base + offset (0x0108)

Win3 virtual stride0 and virtaul stride1

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0140	win3_vir_stride1 Win3 Virtual stride1 Number of words of Win3 Virtual1 width ARGB888 : win3_vir_width1 RGB888 : (win3_vir_width1 * 3/4) + (win3_vir_width1 % 3) RGB565 : ceil(win3_vir_width1 / 2) 8BPP : ceil(win3_vir_width1 / 4) 4BPP : ceil(win3_vir_width1 / 8) 2BPP : ceil(win3_vir_width1 / 16) 1BPP : ceil(win3_vir_width1 / 32)
15:13	RO	0x0	reserved

Bit	Attr	Reset Value	Description
12:0	RW	0x0140	win3_vir_stride0 Win3 Virtual stride0 Number of words of Win3 Virtual1 width ARGB888 : win3_vir_width1 RGB888 : (win3_vir_width1 * 3/4) + (win3_vir_width1 % 3) RGB565 : ceil(win3_vir_width1 / 2) 8BPP : ceil(win3_vir_width1 / 4) 4BPP : ceil(win3_vir_width1 / 8) 2BPP : ceil(win3_vir_width1 / 16) 1BPP : ceil(win3_vir_width1 / 32)

VOP_WIN3_VIR2_3

Address: Operational Base + offset (0x010c)

Win3 virtual stride2 and virtaul stride3

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0140	win3_vir_stride3 Win3 Virtual stride3 Number of words of Win3 Virtual1 width ARGB888 : win3_vir_width1 RGB888 : (win3_vir_width1 * 3/4) + (win3_vir_width1 % 3) RGB565 : ceil(win3_vir_width1 / 2) 8BPP : ceil(win3_vir_width1 / 4) 4BPP : ceil(win3_vir_width1 / 8) 2BPP : ceil(win3_vir_width1 / 16) 1BPP : ceil(win3_vir_width1 / 32)
15:13	RO	0x0	reserved
12:0	RW	0x0140	win3_vir_stride2 Win3 Virtual stride2 Number of words of Win3 Virtual1 width ARGB888 : win3_vir_width1 RGB888 : (win3_vir_width1 * 3/4) + (win3_vir_width1 % 3) RGB565 : ceil(win3_vir_width1 / 2) 8BPP : ceil(win3_vir_width1 / 4) 4BPP : ceil(win3_vir_width1 / 8) 2BPP : ceil(win3_vir_width1 / 16) 1BPP : ceil(win3_vir_width1 / 32)

VOP_WIN3_MST0

Address: Operational Base + offset (0x0110)

Win3 memory start address0

Bit	Attr	Reset Value	Description
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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	win3_mst0 Win3 frame buffer memory start address0 *must be aliased to 8byte address

VOP_WIN3_DSP_INFO0

Address: Operational Base + offset (0x0114)

Win3 display width0/height0 on panel

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x0ef	win3_dsp_height0 Win3 display window height0 win3_dsp_height0 = size -1
15:12	RO	0x0	reserved
11:0	RW	0x13f	win3_dsp_width0 Win3 display window width0 win3_dsp_width = size -1

VOP_WIN3_DSP_ST0

Address: Operational Base + offset (0x0118)

Win3 display start point0 on panel

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x000a	win3_dsp_yst0 Win3 vertical start point(y) of the Panel scanning
15:13	RO	0x0	reserved
12:0	RW	0x000a	win3_dsp_xst0 Win3 horizontal start point(x) of the Panel scanning

VOP_WIN3_COLOR_KEY

Address: Operational Base + offset (0x011c)

Win3 color key register

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24	RW	0x0	win3_key_en Win3 transparency color key enable 1'b0 : disable; 1'b1 : enable;
23:0	RW	0x000000	win3_key_color Win3 key color

VOP_WIN3_MST1

Address: Operational Base + offset (0x0120)

Win3 memory start address1

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	win3_mst1 Win3 frame buffer memory start address1 *must be aliased to 8byte address

VOP_WIN3_DSP_INFO1

Address: Operational Base + offset (0x0124)

Win3 display width1/height1 on panel

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x0ef	win3_dsp_height1 Win3 display window height1 win3_dsp_height0 = size -1
15:12	RO	0x0	reserved
11:0	RW	0x13f	win3_dsp_width1 Win3 display window width1 win3_dsp_width = size -1

VOP_WIN3_DSP_ST1

Address: Operational Base + offset (0x0128)

Win3 display start point1 on panel

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x000a	win3_dsp_yst1 Win3 vertical start point(y) of the Panel scanning
15:13	RO	0x0	reserved
12:0	RW	0x000a	win3_dsp_xst1 Win3 horizontal start point(x) of the Panel scanning

VOP_WIN3_SRC_ALPHA_CTRL

Address: Operational Base + offset (0x012c)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	win3_fading_value
23:16	RW	0x00	win3_src_global_alpha layer0 src global alpha (reused by fading value)
15:9	RO	0x0	reserved
8:6	RW	0x0	win3_src_factor_m0
5	RW	0x0	win3_src_alpha_cal_m0
4:3	RW	0x0	win3_src_blend_m0
2	RW	0x0	win3_src_alpha_m0
1	RW	0x0	win3_src_color_m0
0	RW	0x0	win3_src_alpha_en

VOP_WIN3_MST2

Address: Operational Base + offset (0x0130)

Win3 memory start address2

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	win3_mst2 Win3 frame buffer memory start address2 *must be aliased to 8byte address

VOP_WIN3_DSP_INFO2

Address: Operational Base + offset (0x0134)

Win3 display width2/height2 on panel

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x0ef	win3_dsp_height2 Win3 display window height2 win3_dsp_height0 = size -1
15:12	RO	0x0	reserved
11:0	RW	0x13f	win3_dsp_width2 Win3 display window width2 win3_dsp_width = size -1

VOP_WIN3_DSP_ST2

Address: Operational Base + offset (0x0138)

Win3 display start point2 on panel

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x000a	win3_dsp_yst2 Win3 vertical start point(y) of the Panel scanning
15:13	RO	0x0	reserved
12:0	RW	0x000a	win3_dsp_xst2 Win3 horizontal start point(x) of the Panel scanning

VOP_WIN3_DST_ALPHA_CTRL

Address: Operational Base + offset (0x013c)

Bit	Attr	Reset Value	Description
31:9	RO	0x0	reserved
8:6	RW	0x0	win3_dst_factor_m0
5:0	RW	0x00	win3_dst_factor_reserved

VOP_WIN3_MST3

Address: Operational Base + offset (0x0140)

Win3 memory start address3

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	win3_mst3 Win3 frame buffer memory start address3 *must be aliased to 8byte address

VOP_WIN3_DSP_INFO3

Address: Operational Base + offset (0x0144)

Win3 display width3/height3 on panel

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x0ef	win3_dsp_height3 Win3 display window height3 win3_dsp_height0 = size -1
15:12	RO	0x0	reserved
11:0	RW	0x13f	win3_dsp_width3 Win3 display window width3 win3_dsp_width = size -1

VOP_WIN3_DSP_ST3

Address: Operational Base + offset (0x0148)

Win3 display start point3 on panel

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x000a	win3_dsp_yst3 Win3 vertical start point(y) of the Panel scanning
15:13	RO	0x0	reserved
12:0	RW	0x000a	win3_dsp_xst3 Win3 horizontal start point(x) of the Panel scanning

VOP_WIN3_FADING_CTRL

Address: Operational Base + offset (0x014c)

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24	RW	0x0	win3_fading_en
23:16	RW	0x00	win3_fading_offset_b
15:8	RW	0x00	win3_fading_offset_g
7:0	RW	0x00	win3_fading_offset_r

VOP_HWC_CTRL0

Address: Operational Base + offset (0x0150)

Hwc ctrl register0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18	RW	0x0	hwc_lut_en

Bit	Attr	Reset Value	Description
17:15	RO	0x0	reserved
14	RW	0x0	hwc_endian_swap hwc 8pp palette data Big-endian/ Little-endian select 1'b0 : Big-endian 1'b1 : Little-endian
13	RW	0x0	hwc_alpha_swap hwc RGB alpha swap 1'b0 : ARGB 1'b1 : RGBA
12	RW	0x0	hwc_rb_swap hwc RGB Red and Blue swap 1'b0 : RGB 1'b1 : BGR
11	RO	0x0	reserved
10	RW	0x0	hwc_csc_mode hwc RGB2YUV Color space conversion: 1'b0 : no CSC 1'b1 : RGB2YUV
9	RW	0x0	hwc_no_outstanding hwc AXI master read outstanding 1'b0 : enable 1'b1 : disable
8	RW	0x0	hwc_interlace_read hwc interlace read mode 1'b0 : disable 1'b1 : enable
7	RO	0x0	reserved
6:5	RW	0x0	hwc_size 2'b00 : 32x32 2'b01 : 64x64 2'b10 : 96x96 2'b11 : 128x128
4	RW	0x0	hwc_mode hwc color mode 1'b0 : normal color mode 1'b1 : reversed color mode
3:1	RW	0x0	hwc_data_fmt
0	RW	0x0	hwc_en

VOP_HWC_CTRL1

Address: Operational Base + offset (0x0154)

Hwc ctrl register1

Bit	Attr	Reset Value	Description
31:7	RO	0x0	reserved

Bit	Attr	Reset Value	Description
6:4	RW	0x0	win3_axi_gather_num
3:1	RO	0x0	reserved
0	RW	0x0	win3_axi_gather_en

VOP_HWC_MST

Address: Operational Base + offset (0x0158)

Hwc memory start address

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	hwc_mst HWC data memory start address

VOP_HWC_DSP_ST

Address: Operational Base + offset (0x015c)

Hwc display start point on panel

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x000a	hwc_dsp_yst HWC vertical start point(y) of the Panel scanning
15:13	RO	0x0	reserved
12:0	RW	0x000a	hwc_dsp_xst HWC horizontal start point(x) of the Panel scanning

VOP_HWC_SRC_ALPHA_CTRL

Address: Operational Base + offset (0x0160)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	hwc_fading_value
23:16	RW	0x00	hwc_src_global_alpha layer0 src global alpha (eused by fading value)
15:9	RO	0x0	reserved
8:6	RW	0x0	hwc_src_factor_m0
5	RW	0x0	hwc_src_alpha_cal_m0
4:3	RW	0x0	hwc_src_blend_m0
2	RW	0x0	hwc_src_alpha_m0
1	RW	0x0	hwc_src_color_m0
0	RW	0x0	hwc_src_alpha_en

VOP_HWC_DST_ALPHA_CTRL

Address: Operational Base + offset (0x0164)

Bit	Attr	Reset Value	Description
31:9	RO	0x0	reserved
8:6	RW	0x0	hwc_dst_factor_m0

Bit	Attr	Reset Value	Description
5:0	RW	0x00	hwc_dst_m0_reserved

VOP_HWC_FADING_CTRL

Address: Operational Base + offset (0x0168)

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24	RW	0x0	hwc_fading_en
23:16	RW	0x00	hwc_fading_offset_b
15:8	RW	0x00	hwc_fading_offset_g
7:0	RW	0x00	hwc_fading_offset_r

VOP_HWC_RESERVED1

Address: Operational Base + offset (0x016c)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	reserved

VOP_POST_DSP_HACT_INFO

Address: Operational Base + offset (0x0170)

post scaler down horizontal start and end

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x000a	dsp_hact_st_post Panel display scanning horizontal active start point
15:13	RO	0x0	reserved
12:0	RW	0x014a	dsp_hact_end_post Panel display scanning horizontal active end point

VOP_POST_DSP_VACT_INFO

Address: Operational Base + offset (0x0174)

Panel active horizontal scanning start point and end point

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x000a	dsp_vact_st_post Panel display scanning horizontal active start point
15:13	RO	0x0	reserved
12:0	RW	0x00fa	dsp_vact_end_post Panel display scanning horizontal active end point

VOP_POST_SCL_FACTOR_YRGB

Address: Operational Base + offset (0x0178)

post yrgb scaling factor

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	RW	0x1000	post_vs_factor_yrgb post YRGB vertical scaling factor: factor=((src_height[31:16]) /(dst_height[31:16]))*2^12
15:0	RW	0x1000	post_hs_factor_yrgb Post YRGB horizontal scaling factor: factor=((src_width[15:0]) /(dst_width[15:0]))*2^12

VOP_POST_RESERVED

Address: Operational Base + offset (0x017c)

Bit	Attr	Reset Value	Description
31:0	RW	0x00001000	post_reserved

VOP_POST_SCL_CTRL

Address: Operational Base + offset (0x0180)

post scaling start point offset

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	RW	0x0	post_ver_sd_en 1'b0 : post ver scl down disable 1'b1 : post ver scl down enable
0	RW	0x0	post_hor_sd_en 1'b0 : post hor scl down disable 1'b1 : post hor scl down enable

VOP_POST_DSP_VACT_INFO_F1

Address: Operational Base + offset (0x0184)

Panel active horizontal scanning start point and end point F1

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x000a	dsp_vact_st_post Panel display scanning horizontal active start point
15:13	RO	0x0	reserved
12:0	RW	0x00fa	dsp_vact_end_post Panel display scanning horizontal active end point

VOP_DSP_HTOTAL_HS_END

Address: Operational Base + offset (0x0188)

Panel scanning horizontal width and hsync pulse end point

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved

Bit	Attr	Reset Value	Description
28:16	RW	0x014a	dsp_htotal Panel display scanning horizontal period
15:13	RO	0x0	reserved
12:0	RW	0x000a	dsp_hs_end Panel display scanning hsync pulse width

VOP_DSP_HACT_ST_END

Address: Operational Base + offset (0x018c)

Panel active horizontal scanning start point and end point

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x000a	dsp_hact_st Panel display scanning horizontal active start point
15:13	RO	0x0	reserved
12:0	RW	0x014a	dsp_hact_end Panel display scanning horizontal active end point

VOP_DSP_VTOTAL_VS_END

Address: Operational Base + offset (0x0190)

Panel scanning vertical height and vsync pulse end point

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x00fa	dsp_vtotal Panel display scanning vertical period.
15:13	RO	0x0	reserved
12:0	RW	0x000a	dsp_vs_end Panel display scanning vsync pulse width

VOP_DSP_VACT_ST_END

Address: Operational Base + offset (0x0194)

Panel active vertical scanning start point and end point

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x000a	dsp_vact_st Panel display scanning vertical active start point
15:13	RO	0x0	reserved
12:0	RW	0x00fa	dsp_vact_end Panel display scanning vertical active end point

VOP_DSP_VS_ST_END_F1

Address: Operational Base + offset (0x0198)

Vertical scanning start point and vsync pulse end point of even field in interlace mode

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved

Bit	Attr	Reset Value	Description
28:16	RW	0x0000	dsp_vs_st_f1 Panel display scanning vertical vsync start point of 2nd field (interlace display mode)
15:13	RO	0x0	reserved
12:0	RW	0x0000	dsp_vs_end_f1 Panel display scanning vertical vsync end point of 2nd field (interlace display mode)

VOP_DSP_VACT_ST_END_F1

Address: Operational Base + offset (0x019c)

Vertical scanning active start point and end point of even filed in interlace mode

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	dsp_vact_st_f1 Panel display scanning vertical active start point of 2nd field (interlace display mode)
15:13	RO	0x0	reserved
12:0	RW	0x0000	dsp_vact_end_f1 Panel display scanning vertical active end point of 2nd field (interlace display mode)

VOP_PWM_CTRL

Address: Operational Base + offset (0x01a0)

PWM Control Register

Bit	Attr	Reset Value	Description
31:24	RW	0x00	rpt Repeat Counter This field defines the repeated effective periods of output waveform in one-shot mode. The value N means N+1 repeated effective periods.
23:16	RW	0x00	scale Scale Factor This fields defines the scale factor applied to prescaled clock. The value N means the clock is divided by 2*N. If N is 0, it means that the clock is divided by 512(2*256).
15	RO	0x0	reserved
14:12	RW	0x2	prescale Prescale Factor This field defines the prescale factor applied to input clock. The value N means that the input clock is divided by 2^N.
11:10	RO	0x0	reserved

Bit	Attr	Reset Value	Description
9	RW	0x0	<p>clk_sel Clock Source Select 0: non-scaled clock is selected as PWM clock source. It means that the prescale clock is directly used as the PWM clock source 1: scaled clock is selected as PWM clock source</p>
8	RW	0x0	<p>lp_en Low Power Mode Enable 0: disabled 1: enabled When PWM channel is inactive state and Low Power Mode is enabled, the path to PWM Clock prescale module is blocked to reduce power consumption.</p>
7:6	RO	0x0	reserved
5	RW	0x0	<p>output_mode PWM Output mode 0: left aligned mode 1: center aligned mode</p>
4	RW	0x0	<p>inactive_pol Inactive State Output Polarity This defines the output waveform polarity when PWM channel is in inactive state. The inactive state means that PWM finishes the complete waveform in one-shot mode or PWM channel is disabled. 0: negative 1: positive</p>
3	RW	0x1	<p>duty_pol Duty Cycle Output Polarity This defines the polarity for duty cycle. PWM starts the output waveform with duty cycle. 0: negative 1: positive</p>
2:1	RW	0x1	<p>pwm_mode PWM Operation Mode 00: One shot mode. PWM produces the waveform within the repeated times defined by PWMx_CTRL_rpt . 01: Continuous mode. PWM produces the waveform continuously 10: Capture mode. PWM measures the cycles of high/low polarity of input waveform. 11: reserved</p>

Bit	Attr	Reset Value	Description
0	RW	0x0	pwm_en PWM channel enable 0: disabled 1: enabled. If the PWM is worked the one-shot mode, this bit will be cleared at the end of operation

VOP_PWM_PERIOD_HPR

Address: Operational Base + offset (0x01a4)

PWM Period Register/High Polarity Capture Register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pwm_period Output Waveform Period/Input Waveform High Polarity Cycle If PWM is operated at the continuous mode or one-shot mode, this value defines the period of the output waveform. Note that, if the PWM is operated at the center-aligned mode, the period should be an even one, and therefore only the bit [31:1] is taken into account and bit [0] always considered as 0. If PWM is operated at the capture mode, this value indicates the effective high polarity cycles of input waveform. This value is based on the PWM clock. The value ranges from 0 to (2^32-1).

VOP_PWM_DUTY_LPR

Address: Operational Base + offset (0x01a8)

PWM Duty Register/Low Polarity Capture Register

Bit	Attr	Reset Value	Description
------------	-------------	--------------------	--------------------

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	<p>pwm_duty Output Waveform Duty Cycle/Input Waveform Low Polarity Cycle If PWM is operated at the continuous mode or one-shot mode, this value defines the duty cycle of the output waveform. The PWM starts the output waveform with duty cycle. Note that, if the PWM is operated at the center-aligned mode, the period should be an even one, and therefore only the [31:1] is taken into account.</p> <p>If PWM is operated at the capture mode, this value indicates the effective low polarity cycles of input waveform.</p> <p>This value is based on the PWM clock. The value ranges from 0 to ($2^{32}-1$).</p>

VOP_PWM_CNT

Address: Operational Base + offset (0x01ac)

PWM Counter Register

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	<p>pwm_cnt Timer Counter The 32-bit indicates current value of PWM Channel 0 counter. The counter runs at the rate of PWM clock. The value ranges from 0 to ($2^{32}-1$).</p>

VOP_BCSH_COLOR_BAR

Address: Operational Base + offset (0x01b0)

color bar config register

Bit	Attr	Reset Value	Description
31:22	RW	0x000	color_bar_v v color value
21:12	RW	0x000	color_bar_u u color value
11:2	RW	0x000	color_bar_y y color value
1	RO	0x0	reserved
0	RW	0x0	bcs_sh_en 1'b0 : bcs bypass 1'b1 : bcs enable

VOP_BCSH_BCS

Address: Operational Base + offset (0x01b4)
 brightness contrast saturation*contrast config register

Bit	Attr	Reset Value	Description
31:30	RW	0x3	out_mode video out mode config register 2'b00 : black 2'b01 : blue 2'b10 : color bar 2'b11 : normal video
29:20	RW	0x100	sat_con Saturation*Contrast*256 : 0,1.992*1.992
19:17	RO	0x0	reserved
16:8	RW	0x100	contrast Contrast*256 : 0,1.992
7:0	RW	0x00	brightness Brightness : -128,127

VOP_BCSH_H

Address: Operational Base + offset (0x01b8)
 sin hue and cos hue config register

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24:16	RW	0x100	cos_hue cos hue value
15:9	RO	0x0	reserved
8:0	RW	0x000	sin_hue sin hue value

VOP_BCSH_RESERVED

Address: Operational Base + offset (0x01bc)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	reserved

VOP_CABC_CTRL0

Address: Operational Base + offset (0x01c0)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	cabc_stage_up
23:1	RW	0x000000	cabc_calc_pixel_num Field0000 Abstract Field0000 Description
0	RW	0x0	cabc_en 1'b0 : cabc disable 1'b1 : cabc enable

VOP_CABC_CTRL1

Address: Operational Base + offset (0x01c4)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	cabc_stage_down Field0000 Abstract Field0000 Description
23:1	RW	0x000000	cabc_total_num
0	RO	0x0	reserved

VOP_CABC_GAUSS_LINE0_0

Address: Operational Base + offset (0x01c8)

Register0000 Abstract

Bit	Attr	Reset Value	Description
31:24	RW	0x15	t_line0_3
23:16	RW	0x11	t_line0_2
15:8	RW	0x09	t_line0_1
7:0	RW	0x03	t_line0_0

VOP_CABC_GAUSS_LINE0_1

Address: Operational Base + offset (0x01cc)

Register0001 Abstract

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23:16	RW	0x03	t_line0_6
15:8	RW	0x09	t_line0_5
7:0	RW	0x11	t_line0_4

VOP_CABC_GAUSS_LINE1_0

Address: Operational Base + offset (0x01d0)

Register0002 Abstract

Bit	Attr	Reset Value	Description
31:24	RW	0x1a	t_line1_3
23:16	RW	0x15	t_line1_2
15:8	RW	0x0b	t_line1_1
7:0	RW	0x04	t_line1_0

VOP_CABC_GAUSS_LINE1_1

Address: Operational Base + offset (0x01d4)

Register0003 Abstract

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23:16	RW	0x04	t_line1_6
15:8	RW	0x0b	t_line1_5
7:0	RW	0x15	t_line1_4

VOP_CABC_GAUSS_LINE2_0

Address: Operational Base + offset (0x01d8)

Register0004 Abstract

Bit	Attr	Reset Value	Description
31:24	RW	0x15	t_line2_3
23:16	RW	0x11	t_line2_2
15:8	RW	0x09	t_line2_1
7:0	RW	0x03	t_line2_0

VOP_CABC_GAUSS_LINE2_1

Address: Operational Base + offset (0x01dc)

Register0005 Abstract

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23:16	RW	0x03	t_line2_6
15:8	RW	0x09	t_line2_5
7:0	RW	0x11	t_line2_4

VOP_FRC_LOWER01_0

Address: Operational Base + offset (0x01e0)

Bit	Attr	Reset Value	Description
31:16	RW	0x1284	lower01_frm1
15:0	RW	0x4821	lower01_frm0

VOP_FRC_LOWER01_1

Address: Operational Base + offset (0x01e4)

Bit	Attr	Reset Value	Description
31:16	RW	0x2148	lower01_frm3
15:0	RW	0x8412	lower01_frm2

VOP_FRC_LOWER10_0

Address: Operational Base + offset (0x01e8)

Bit	Attr	Reset Value	Description
31:16	RW	0xa55a	lower10_frm1
15:0	RW	0x9696	lower10_frm0

VOP_FRC_LOWER10_1

Address: Operational Base + offset (0x01ec)

Bit	Attr	Reset Value	Description
31:16	RW	0x5aa5	lower10_frm3

Bit	Attr	Reset Value	Description
15:0	RW	0x6969	lower10_frm2

VOP_FRC_LOWER11_0

Address: Operational Base + offset (0x01f0)

Bit	Attr	Reset Value	Description
31:16	RW	0xdeb7	lower11_frm1
15:0	RW	0x7bed	lower11_frm0

VOP_FRC_LOWER11_1

Address: Operational Base + offset (0x01f4)

Bit	Attr	Reset Value	Description
31:16	RW	0xed7b	lower11_frm3
15:0	RW	0xb7de	lower11_frm2

VOP_FRC_RESERVED0

Address: Operational Base + offset (0x01f8)

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	Field0000 Abstract Field0000 Description

VOP_FRC_RESERVED1

Address: Operational Base + offset (0x01fc)

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	Field0000 Abstract Field0000 Description

VOP_MMU_DTE_ADDR

Address: Operational Base + offset (0x0300)

MMU current page Table address

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	MMU_DTE_ADDR Field0000 Abstract Field0000 Description

VOP_MMU_STATUS

Address: Operational Base + offset (0x0304)

MMU status register

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:11	RO	0x0	reserved
10:6	RO	0x00	PAGE_FAULT_BUS_ID Field0000 Abstract Index of master responsible for last page fault
5	RO	0x0	PAGE_FAULT_IS_WRITE Field0000 Abstract The direction of access for last page fault: 0 = Read 1 = Write
4	RO	0x0	REPLAY_BUFFER_EMPTY Field0000 Abstract The MMU replay buffer is empty
3	RO	0x0	MMU_IDLE Field0000 Abstract The MMU is idle when accesses are being translated and there are no unfinished translated accesses.
2	RO	0x0	STAIL_ACTIVE Field0001 Abstract MMU stall mode currently enabled. The mode is enabled by command
1	RO	0x0	PAGE_FAULT_ACTIVE Field0000 Abstract MMU page fault mode currently enabled . The mode is enabled by command.
0	RO	0x0	PAGING_ENABLED Field0000 Abstract Paging is enabled

VOP_MMU_COMMAND

Address: Operational Base + offset (0x0308)

MMU command register

Bit	Attr	Reset Value	Description
31:3	RO	0x0	reserved
2:0	WO	0x0	MMU_CMD Field0000 Abstract MMU_CMD. This can be: 0: MMU_ENABLE_PAGING 1: MMU_DISABLE_PAGING 2: MMU_ENABLE_STALL 3: MMU_DISABLE_STALL 4: MMU_ZAP_CACHE 5: MMU_PAGEFAULT_DONE 6: MMU_FORCE_RESET

VOP_MMU_PAGE_FAULT_ADDR

Address: Operational Base + offset (0x030c)

MMU logical address of last page fault

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	PAGE_FAULT_ADDR Field0000 Abstract address of last page fault

VOP_MMU_ZAP_ONE_LINE

Address: Operational Base + offset (0x0310)

MMU Zap cache line register

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	MMU_ZAP_ONE_LINE Field0000 Abstract address to be invalidated from the page table cache

VOP_MMU_INT_RAWSTAT

Address: Operational Base + offset (0x0314)

MMU raw interrupt status register

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	RW	0x0	READ_BUS_ERROR Field0000 Abstract read bus error
0	RW	0x0	PAGEFAULT Field0000 Abstract page fault

VOP_MMU_INT_CLEAR

Address: Operational Base + offset (0x0318)

MMU raw interrupt status register

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	WO	0x0	READ_BUS_ERROR Field0000 Abstract read bus error
0	WO	0x0	PAGEFAULT Field0000 Abstract page fault

VOP_MMU_INT_MASK

Address: Operational Base + offset (0x031c)

MMU raw interrupt status register

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved

Bit	Attr	Reset Value	Description
1	RW	0x0	READ_BUS_ERROR Field0000 Abstract read bus error
0	RW	0x0	PAGE_FAULT Field0000 Abstract page fault

VOP_MMU_INT_STATUS

Address: Operational Base + offset (0x0320)

MMU raw interrupt status register

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	RO	0x0	READ_BUS_ERROR Field0000 Abstract read bus error
0	RO	0x0	PAGE_FAULT Field0000 Abstract page fault

VOP_MMU_AUTO_GATING

Address: Operational Base + offset (0x0324)

mmu auto gating

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	mmu_auto_gating mmu auto gating when it is 1'b1, the mmu will auto gating it self

VOP_WIN2_LUT_ADDR

Address: Operational Base + offset (0x0400)

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	Field0000 Abstract Field0000 Description

VOP_WIN3_LUT_ADDR

Address: Operational Base + offset (0x0800)

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	Field0000 Abstract Field0000 Description

VOP_HWC_LUT_ADDR

Address: Operational Base + offset (0x0c00)

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	Field0000 Abstract Field0000 Description

VOP_GAMMA_LUT_ADDR

Address: Operational Base + offset (0x1000)

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	Field0000 Abstract Field0000 Description

VOP MCU BYPASS_WPORT

Address: Operational Base + offset (0x2200)

Register0000 Abstract

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	Field0000 Abstract Field0000 Description

VOP MCU BYPASS_RPORT

Address: Operational Base + offset (0x2300)

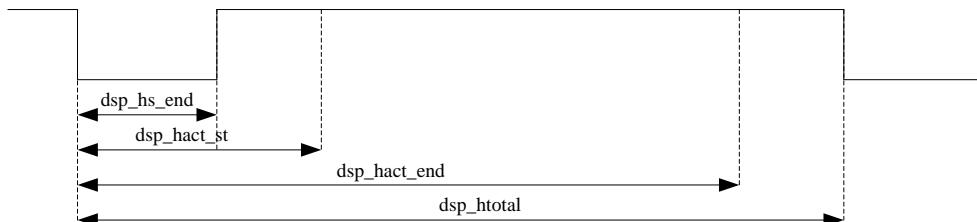
Register0001 Abstract

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	Field0000 Abstract Field0000 Description

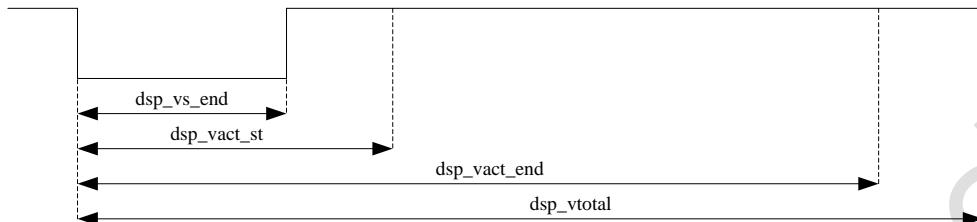
8.5 Timing Diagram

8.5.1 RGB LCD interface timing

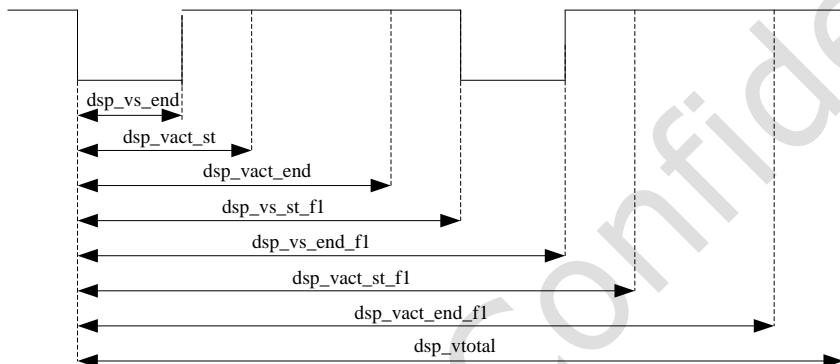
1.Timing parameter



Horizontal timing



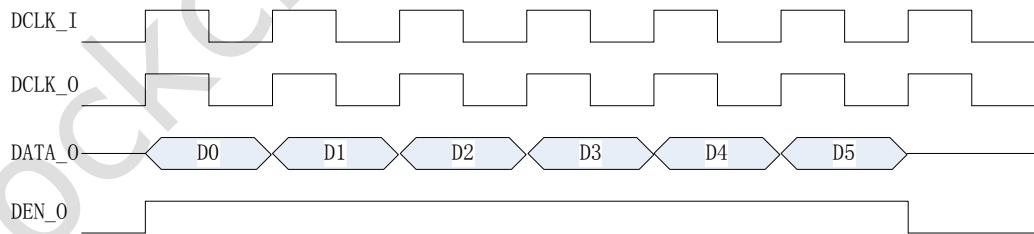
Vertical timing(Progressive mode)



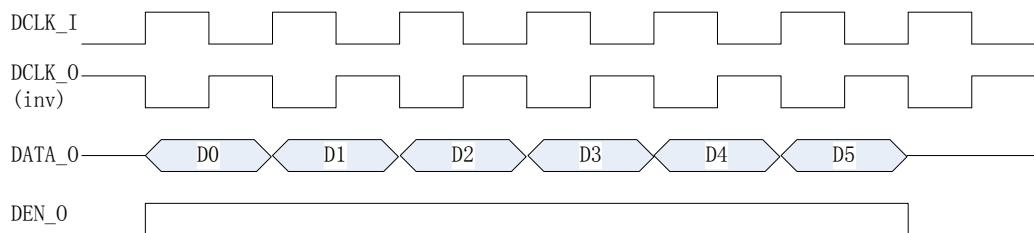
Vertical timing(Interlace mode)

2. Data timing for RGB LCD SDR interface

SDR:



SDR+INV:



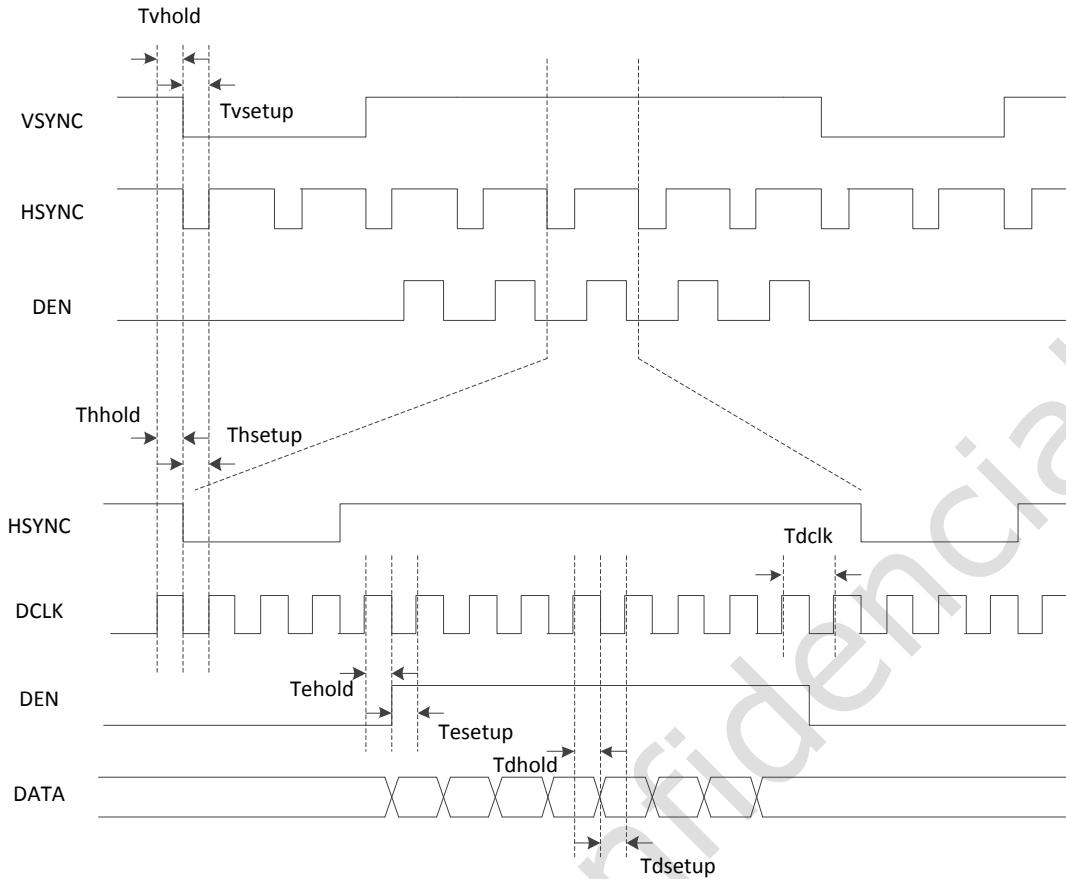


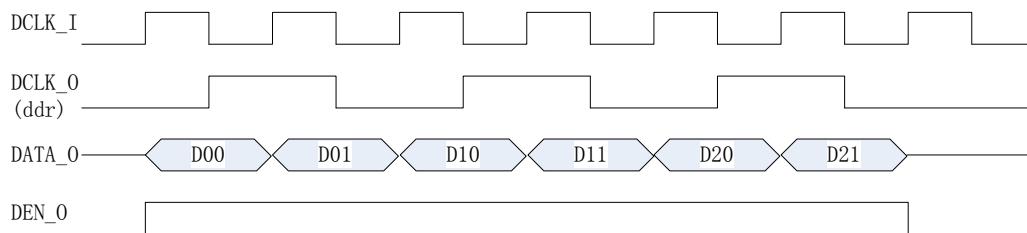
Fig. 8-17 LCDC RGB interface timing (SDR)

Table 8-2 LCDC0 RGB interface(SDR) signal timing constant
($VDD_{core} = 0.9V$ to $1.1V$, $VDD_{IO}=3.0V$ to $3.6V$, $TA = -40^{\circ}C$ ot $125^{\circ}C$)

Item	Symbol	Min	Typ	Max	Unit
Display clock period	Tdclk				ns
VSYNC setup to DCLK falling edge	Tvsetup				ns
VSYNC hold from DCLK falling edge	Tvhold				ns
HSYNC setup to DCLK falling edge	Thsetup				ns
HSYNC hold from DCLK falling edge	Thhold				ns
DEN setup to DCLK falling edge	Tesetup				ns
DEN hold from DCLK falling edge	Tehold				ns
DATA setup to DCLK falling edge	Tdsetup				ns
DATA hold from DCLK falling edge	Tdhold				ns

3.Data timing for RGB LCD DDR interface

DDR:



DDR+INV:

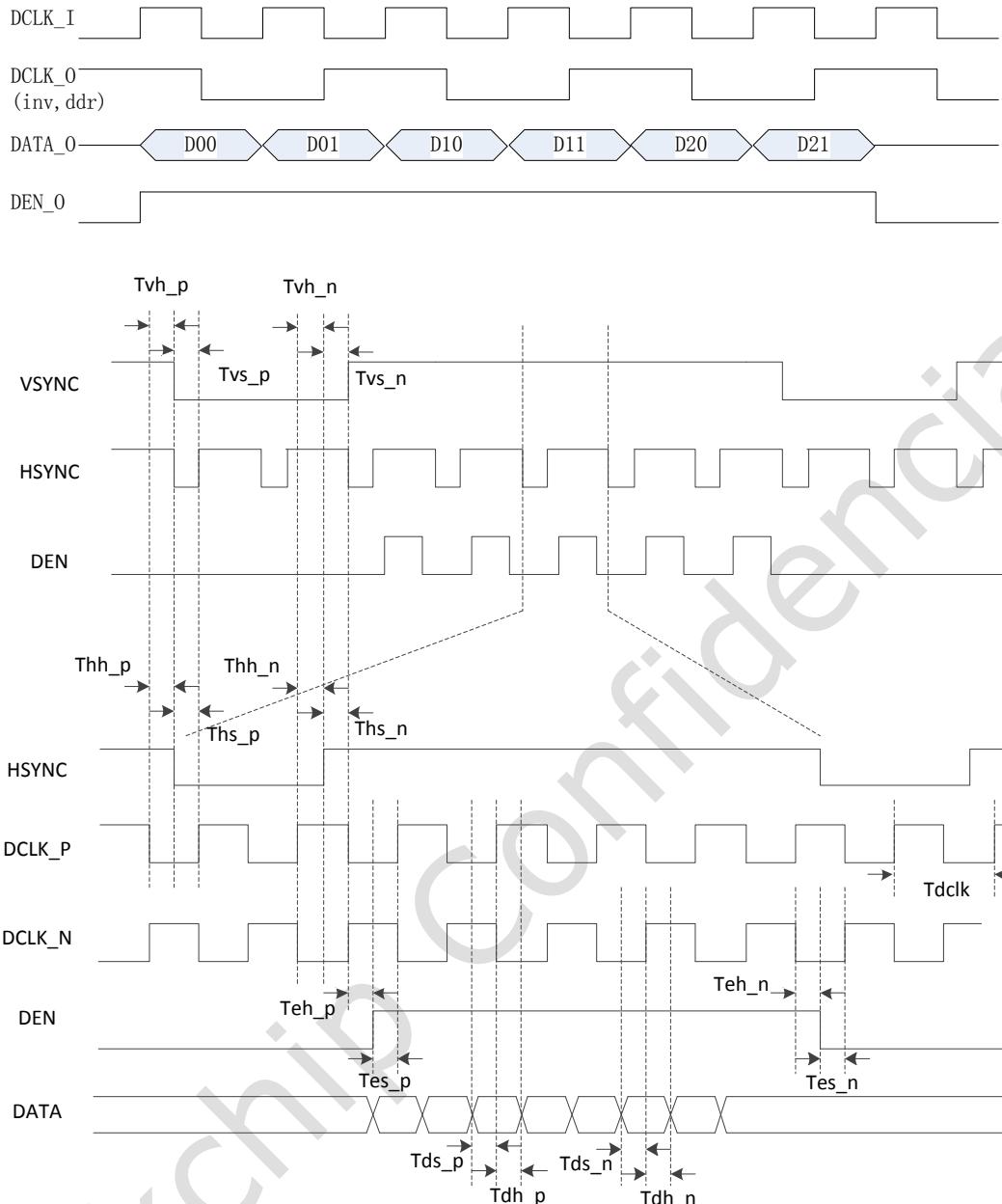


Fig. 8-18 LCDC RGB interface timing (DDR)

Table 8-3 LCDC0 RGB interface (DDR) signal timing constant
($VDD_{core} = 0.9V$ to $1.1V$, $VDD_{IO} = 3.0V$ to $3.6V$, $TA = -40^{\circ}C$ to $125^{\circ}C$)

Item	Symbol	Min	Typ	Max	Unit
Display clock period	$Tdclk$				ns
VSYNC setup to DCLK_N falling edge	Tvs_p				ns
VSYNC hold from DCLK_N falling edge	Tvh_p				ns
HSYNC setup to DCLK_N falling edge	Ths_p				ns
HSYNC hold from DCLK_N falling edge	Thh_p				ns
DEN setup to DCLK_N falling edge	Tes_p				ns
DEN hold from DCLK_N falling edge	The_p				ns
DATA setup to DCLK_N falling edge	Tds_p				ns
DATA hold from DCLK_N falling edge	Tdh_p				ns
VSYNC setup to DCLK_P falling edge	Tvs_p				ns
VSYNC hold from DCLK_P falling edge	Tvh_p				ns

HSYNC setup to DCLK_P falling edge	Ths_p				ns
HSYNC hold from DCLK_P falling edge	Thh_p				ns
DEN setup to DCLK_P falling edge	Tes_p				ns
DEN hold from DCLK_P falling edge	The_p				ns
DATA setup to DCLK_P falling edge	Tds_p				ns
DATA hold from DCLK_P falling edge	Tdh_p				ns

Table 8-4 LCDC1 RGB interface signal timing constant
(VDD_core = 0.9V to 1.1V, VDD_IO=3.0V to 3.6V , TA = -40°C ot 125°C)

Item	Symbol	Min	Typ	Max	Unit
Display clock period	Tdclk				ns
VSYNC setup to DCLK falling edge	Tvsetup				ns
VSYNC hold from DCLK falling edge	Tvhold				ns
HSYNC setup to DCLK falling edge	Thsetup				ns
HSYNC hold from DCLK falling edge	Thhold				ns
DEN setup to DCLK falling edge	Tesetup				ns
DEN hold from DCLK falling edge	Tehold				ns
DATA setup to DCLK falling edge	Tdsetup				ns
DATA hold from DCLK falling edge	Tdhold				ns

8.5.2 MCU LCD interface timing

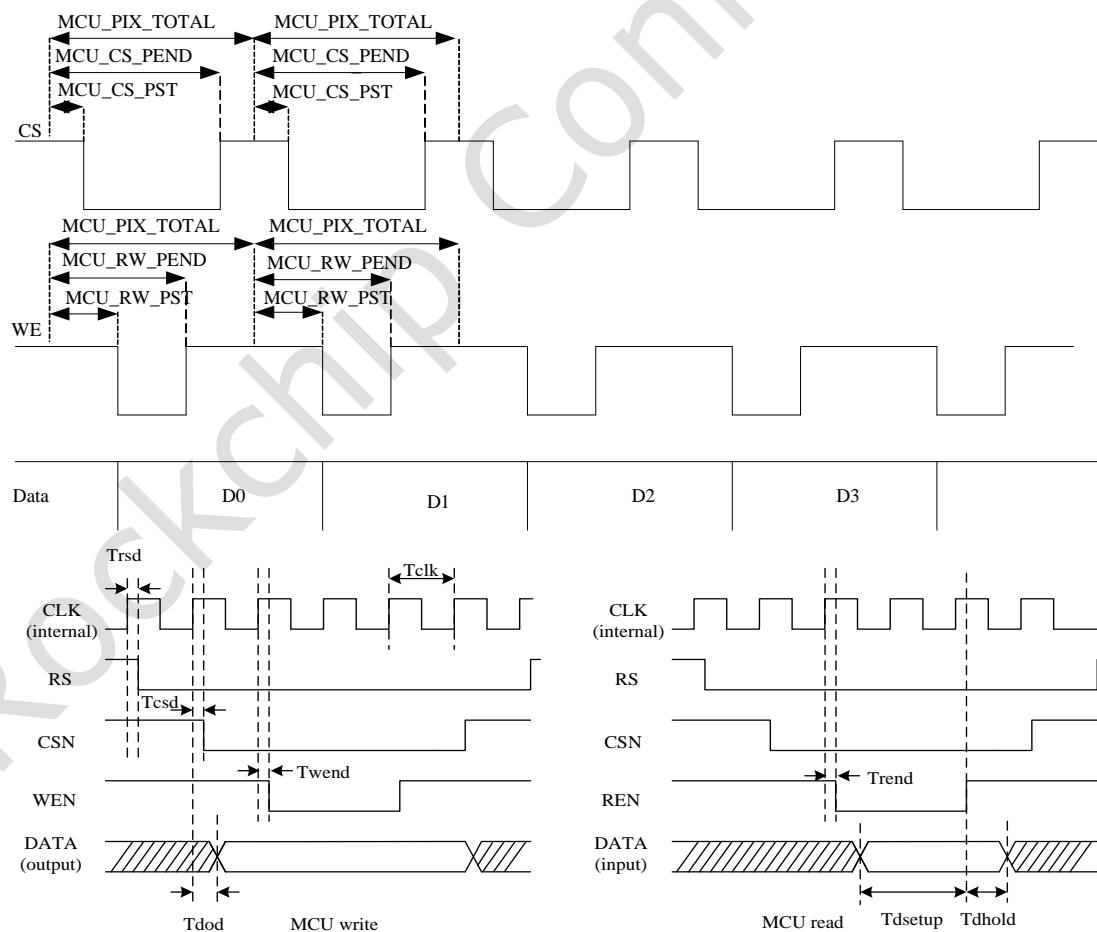


Fig. 8-19 LCDC MCU interface (i80) timing

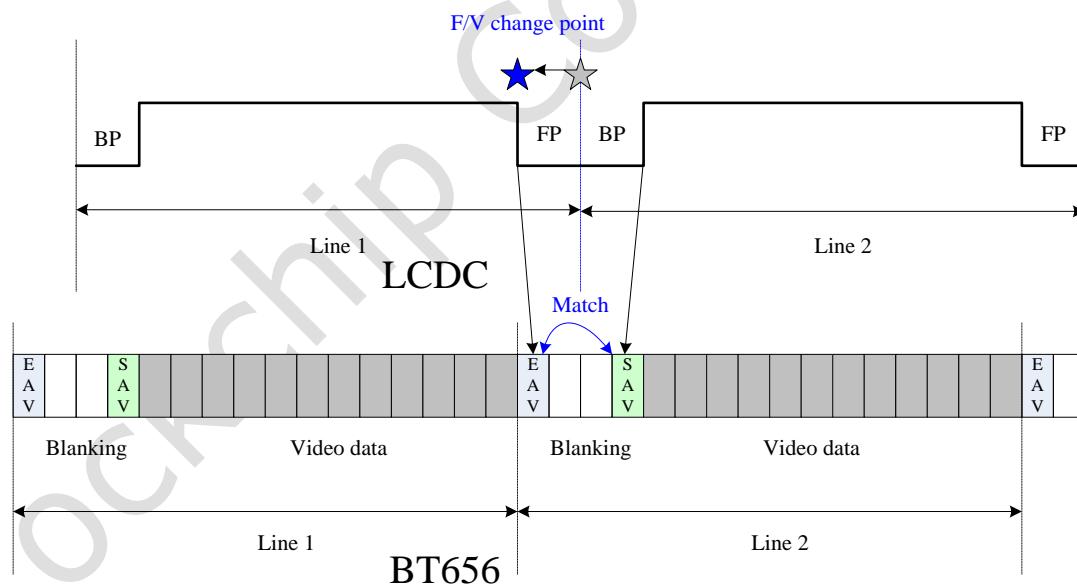
Table 8-5 LCDC0 RGB interface signal timing constant
(VDD_core = 0.9V to 1.1V, VDD_IO=3.0V to 3.6V , TA = -40°C ot 125°C)

Item	Symbol	Min	Typ	Max	Unit
Internal clock period	Tclk				ns
RS delay from CLK rising edge	Trsd				ns
CSN delay from CLK rising edge	Tcsd				ns
WEN delay from CLK rising edge	Twend				ns
REN delay from CLK rising edge	Trend				ns
D_out delay from CLK rising edge	Tdod				ns
D_in setup to REN rising edge	Tdsetup				ns
D_in hold from REN rising edge	Tdhold				ns

Table 8-6 LCDC1 RGB interface signal timing constant
(VDD_core = 0.9V to 1.1V, VDD_IO=3.0V to 3.6V , TA = -40°C ot 125°C)

Item	Symbol	Min	Typ	Max	Unit
Internal clock period	Tclk				ns
RS delay from CLK rising edge	Trsd				ns
CSN delay from CLK rising edge	Tcsd				ns
WEN delay from CLK rising edge	Twend				ns
REN delay from CLK rising edge	Trend				ns
D_out delay from CLK rising edge	Tdod				ns
D_in setup to REN rising edge	Tdsetup				ns
D_in hold from REN rising edge	Tdhold				ns

8.5.3 ITU656 interface timing



8.6 Interface Description

8.6.1 Display interface description

The VOP is suitable for different display mode by different usage, which is shown as follows.

Display mode	RGB Parallel	RGB Parallel	RGB Parallel	RGB Serial	RGB Serial	RGB Serial 3x8-bit

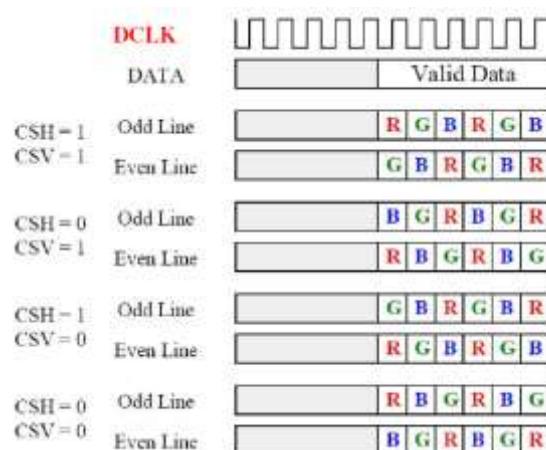
	24-bit	18-bit	16-bit	2x12-bit	3x8-bit	+ dummy
DCLK	DCLK	DCLK	DCLK	DCLK	DCLK	DCLK
VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC
Hsync	Hsync	Hsync	Hsync	Hsync	Hsync	Hsync
DEN	DEN	DEN	DEN	DEN	DEN	DEN
DATA	DATA[23:0]	DATA[17:0]	DATA[15:0]	DATA[11:0]	DATA[7:0]	DATA[7:0]

Display mode	MCU	MCU	MCU	MCU	MCU
	Parallel	Parallel	Parallel	Serial	Serial
	24-bit	18-bit	16-bit	2x12-bit	3x8-bit
DCLK	RS	RS	RS	RS	RS
VSYNC	CSN	CSN	CSN	CSN	CSN
Hsync	WEN	WEN	WEN	WEN	WEN
DEN	REN	REN	REN	REN	REN
DATA	DATA[23:0]	DATA[17:0]	DATA[15:0]	DATA[11:0]	DATA[7:0]

Display mode	ITU656	ITU656	ITU656
	Mode0	Mode1	Mode2
DCLK	DCLK	DCLK	DCLK
VSYNC	-	-	-
Hsync	-	-	-
DEN	-	-	-
DATA	DATA[7:0]	DATA[15:8]	DATA[23:16]

In the case of "RGB serial 3x8-bit", there are four scanning modes for the RGB delta data when delta swap is enable, shown as follows.

<i>RGB delta LCD scanning mode</i>	<i>delta_en</i>	<i>dsp_rg_swap</i>	<i>dsp_rb_swap</i>	<i>dsp_bg_swap</i>
CSH=1,CSV=1	1	0	1	0
CSH=0,CSV=1	1	0	0	0
CSH=1,CSV=0	1	0	0	1
CSH=0,CSV=0	1	0	1	1



8.6.2 IOMUX description

There are two VOPs in the chip, config GRF_SOC_CON6 register to select a VOP to IO/LVDS port.

programing flow as follow:

step1 : config GRF,iomux,io driver,lc当地 select

GRF_GPIO1H_SR and GRF_GPIO1D_E register are optional.

config GRF_BASE + GRF_SOC_CON6 = (0x8<<16) | (0x0) to select vop_big output to IO/LVDS.

config GRF_BASE + GRF_SOC_CON6 = (0x8<<16) | (0x1<<3) to select vop_lit output to IO/LVDS.

eg:

```
GRF_BASE + GRF_GPIO1D_IOMUX = ((0x55<<16)|(0x55<<0));
```

```
GRF_BASE + GRF_GPIO1H_SR = (0x0f000f00);
```

```
GRF_BASE + GRF_GPIO1D_E = (0x00ff00ff);
```

```
GRF_BASE + GRF_SOC_CON6 = (0x8<<16) | (0x0);
```

```
GRF_BASE + GRF_SOC_CON7 = (0x1fff<<16) | (0x1840);
```

step 2 : config LVDS PHY0 register to initial LVDS PHY0

eg:

```
LVDS_BASE + 0x00*4 = 0x7f;
```

```
LVDS_BASE + 0x01*4 = 0x40;
```

```
LVDS_BASE + 0x02*4 = 0x00;
```

```
LVDS_BASE + 0x03*4 = 0x46;
```

```
LVDS_BASE + 0x04*4 = 0x3f;
```

```
LVDS_BASE + 0x05*4 = 0x3f;
```

```
LVDS_BASE + 0x0d*4 = 0xa;
```

step 3 : config LVDS PHY1 register to initial LVDS PHY1

eg:

```
LVDS_BASE + 0x40*4 = 0x7f;
```

```
LVDS_BASE + 0x41*4 = 0x40;
```

```
LVDS_BASE + 0x42*4 = 0x00;
```

```
LVDS_BASE + 0x43*4 = 0x46;
```

```
LVDS_BASE + 0x44*4 = 0x3f;
```

```
LVDS_BASE + 0x45*4 = 0x3f;
```

```
LVDS_BASE + 0x4d*4 = 0xa;
```

8.7 Application Notes

8.7.1 DMA transfer mode

There are three DMA transfer modes for loading win0 or win1 frame data determined by following parameters(X=0,1,2,3):

dma_burst_length

winX_no_outstanding

winX_gather_en

winX_gather_thres

- **auto outstanding transfer mode(random transfer)**

When winX_no_outstanding is 0, multi-bursts transfer command could be sent out to AXI master interface continuously if the internal memory has enough space to store new data. The continuous random burst number is in the range of 1 to 4, mainly depending on the empty level of internal memory, dma_burst_length, data format and active image width.

- **configured outstanding transfer mode(fixed transfer)**

When winX_gather_en is 1, fixed-number of bursts transfer command should be sent out to

AXI master interface continuously if the internal memory has enough space to store new data. The fixed-number is determined by `winX_gather_thres`. Since the internal memory size is limited, there is some restriction for the `winX_gather_thres` as follows.

Table 8-7 Gather configuration for all format

Gather Threshold	dma_burst_length =2'b00(burst16)	dma_burst_length =2'b01(burst8)	dma_burst_length =2'b10(burst4)
YUV420	0	0,1,2	0,1,2,3
YUV422			
YUV444			
ARGB888	0,1,2,3	0,1,2,3	0,1,2,3
RGB888			
RGB565			
8BPP	0,1,2,3	0,1,2,3	0,1,2,3
4BPP			
2BPP			
1BPP			

8.7.2 Win0/Win1 dma load mode

If you want to improve the efficiency of accessing external memory for loading winX frame data, you could assert `winX_dma_load`. When `winX_dma_load` is high, winX frame data is loaded in the unit of line composing with one or more burst transfers; otherwise, loaded in the unit of burst transfer. However, it is not suitable for data format YUV420, no-scaling and active width less than 256.

8.7.3 IEP direct path

There are two data source for win0/win1/win2/win3: external memory and IEP internal memory. However, the IEP data is just active for one layer at one frame time when IEP data path is enable, determined by `dsp_layer0/1/2/3_sel`. Moreover, it is not suitable for win0/1 with scaling, reverse display.

Direct path interface (DPI) can be used for LCDC to display images from other image processing IPs, which also has DPI (slave).

There are programming flows for both DPI display on sequence and DPI display off sequence.

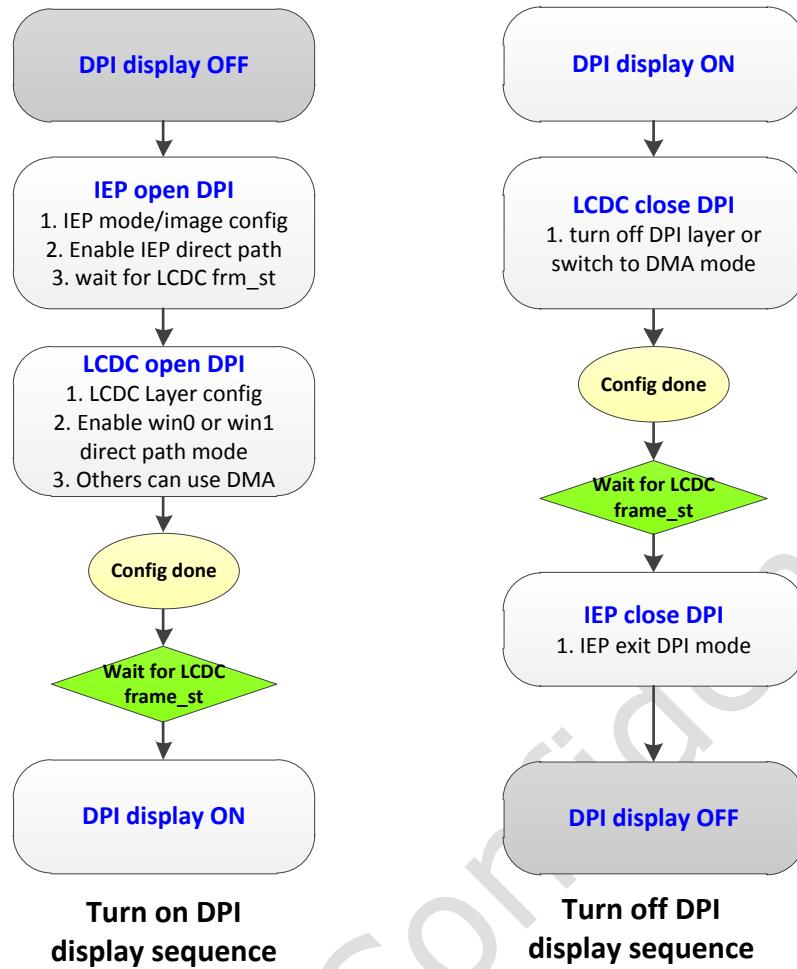


Fig. 8-20 LCDC DPI Programming flow

1.Turn on DPI display

First, configure IEP into DPI mode. After doing image information and image processing mode configuration, IEP DPI mode can be turn on for display. IEP is in idle mode only if LCDC's frame start input signal is valid.

Second, configure LCDC for DPI display. Note that only one layer (Win0 or Win1) can use DPI in same frame. Other layers still can use internal DMA.

Finally, set LCDC "config_done" to confirm all the new configuration and waiting frame sync to start DPI display actually.

2.Turn off DPI display

First, close LCDC layer's DPI mode by turning off DPI layer or switching it to DMA mode. Then set LCDC "config_done" to confirm new configuration.

Second, wait for LCDC's frame synchronization to close DPI display in LCDC.

Finally, turn off IEP's DPI mode.

8.7.4 WIN BPP LUT/GAMMA LUT

WIN1 LUT/DSP LUT should be configured before displaying if win2/3_lut_en/dsp_lut_en is high. You could only update these LUTs by software.

When win1_lut_load_en is 0, the WIN LUT data should be refreshed by software,i.e, writing win1 lut data to the internal memory with the start address WIN1_LUT_MST. The memory size is 256x25, i.e, lower 25bits valid, and the writing data number is determined by software, .

When dsp_lut_load_en is 0, the DSP LUT data should be refreshed by software,i.e, writing dsp lut data to the internal memory with the start address DSP_LUT_MST. The memory size is 256x24, i.e, lower 25bits valid, and the writing data number is determined by software.

8.7.5 DMA QoS request

If you want to get higher priority for VOP to access external memory when the frame data is urgent, a QoS request can be generated and sent out basing on the configured values:

noc_hurry_en
noc_hurry_value
noc_qos_en
noc_win_qos

If noc_qos_en is enable, a win0/1_qos_req is asserted when the empty level of win0/1's linebuffer is greater than the threshold configured in noc_win_qos. And it will be disserted when the empty level is smaller than the threshold or noc_qos_en is disable.

If noc_qos_en is enable, a win0/1_hurry_req is asserted when the empty level of win2/3's fifo is greater than the threshold configured in noc_win_qos. And it will be disserted when the empty level is smaller than the threshold or noc_qos_en is disable.

Either win0/1_qos_req or win2/3_hurry_req is high, a QoS request will be sent out for VOP.

8.7.6 Mirror display

If Y-Mirror display is enable, the frame data is loaded from last line to first line, where the start address of first pixel in last line is defined in

WIN0/1_YRGB0_MST/WIN0/1_CBR0_MST/WIN0/1_YRGB1_MST/WIN0/1_CBR_MST/WIN2/3_MST for win0/1/2/3 respectively.

Otherwise, the win's frame line data width and virtual stride should be 64bit-aligned for 8bit-RGB/YUV or 128bit-aligned for 10bit YUV if X-Mirror or Y-Mirror display is enable.

8.7.7 DDR interface

LCD DDR interface is just suitable for Parallel RGB LCD panel and Serial RGB LCD 2x12 panel.

If LCD DDR interface is enable, the timing parameters for LCD panel should be even.

Otherwise, you can synchronize output clock with VSYNC or HSYNC depending on dclk_ddr_sync.

8.7.8 Interrupt

VOP interrupt is comprised of 12 interrupt sources:

frame start interrupt
line flag interrupt
bus error interrupt
win0 empty interrupt
win1 empty interrupt
win2 empty interrupt
win3 empty interrupt
hwc empty interrupt
post empty interrupt
pwm gen interrupt
irq_mmu

Every interrupt has independent interrupt enable (VOP_INT_EN), interrupt clear (VOP_INT_CLR), interrupt status (VOP_INT_STATUS).

8.7.9 RGB display mode

RGB display mode is used for RGB panel display and CCIR656 output. It is a continuous frames display mode.

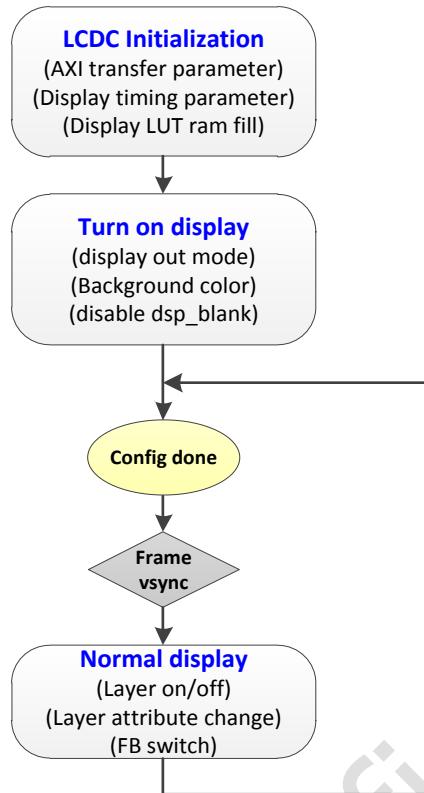


Fig. 8-21 LCDC RGB mode Programming flow

1. LCDC initialization

LCDC initialization should be done before turning display on.

First, AXI bus parameter (LCDC_SYS_CTRL) should be set for DMA transfer.

Second, display panel/interface timing should be set for display output. The registers are:

LCDC_DSP_HTOTAL_HS_END/ LCDC_DSP_HACT_ST_END/ LCDC_DSP_VTOTAL_HS_END/
LCDC_DSP_VACT_ST_END/ LCDC_DSP_VS_ST_END_F1/ LCDC_DSP_VACT_ST_END_F1

2. Background display

Before normal display, the background display could be turn on.

First, set display output mode (LCDC_DSP_CTRL0/1) according to display device.

Second, disable dsp_blank mode, which would not be enable until frame synchronization.

Finally, writing '1' to "LCDC_REG_CFG_DONE" register then all the frame-sync registers will be enable at the beginning of next frame.

3. Normal display

In normal display, all the display layers' attribute could be different according display scenario. So there is a programming loop in this mode.

First, configure all the display layers' attribute registers for the change of image format, location, size, scaling factor, alpha and overlay and so on. Those register would not be enable until frame synchronization.

Finally, write '1' to "LCDC_REG_CFG_DONE" register then all the frame-sync registers will be enable at the beginning of next frame.

8.7.10 MCU display mode

MCU display mode is used for MCU panel display or MCU I80 local bus. It is a single frame display mode.

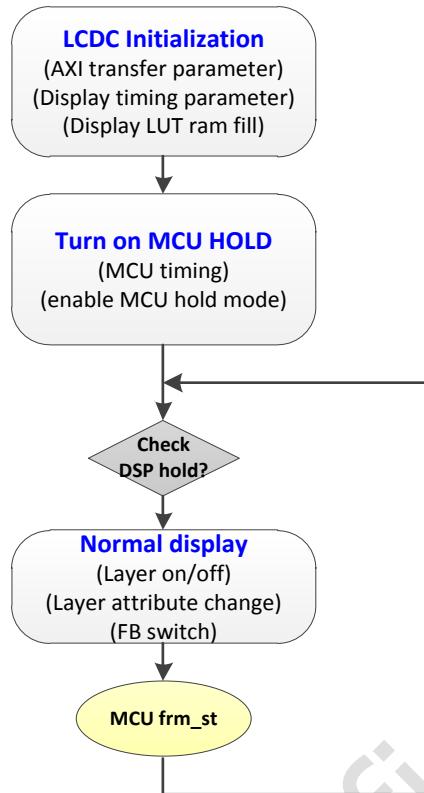


Fig. 8-22 LCDC RGB mode Programming flow

1.LCDC initialization

LCDC initialization should be done before turning display on.

First, AXI bus parameter (LCDC_SYS_CTRL) should be set for DMA transfer.

Second, display panel/interface timing should be set for display output. The registers are:

LCDC_DSP_HTOTAL_HS_END/ LCDC_DSP_HACT_ST_END/ LCDC_DSP_VTOTAL_HS_END/

LCDC_DSP_VACT_ST_END/ LCDC_DSP_VS_ST_END_F1/ LCDC_DSP_VACT_ST_END_F1

Finally, fill the display LUT ram if color LUT function enable.

2.Turn on MCU hold mode

First setting MCU timing parameter (LCDC_MCU_CTRL[26:0]).

Turn on MCU hold mode (LCDC_MCU_CTRL[31] and LCDC_MCU_CTRL[27]), then wait for MCU display hold (read LCDC_MCU_CTRL[28] if its value is '1', or set display hold valid interrupt)

3.Single display

If MCU display hold status is valid, single MCU display frame could be start by setting mcu_frame_st (LCDC_MCU_CTRL[28])

First, configure all the display layers' attribute registers for the change of image format, location, size, scaling factor, alpha and overlay and so on. Those register would not be enable until MCU frame start.

Second, write '1' to start one MCU frame.

Finally, wait for MCU display hold status.

8.7.11 MIPI control

1.double channel

MIPI double channel display is supported in the version(only left-right type).

Config doub_channel_en register in DSP_CTRL0 to adapt double channel display .

When doub_channel mode ,the vop will output two data bus to MIPI PHY,data0 is left panel data,data1 is right panel data.

Double channel overlap display is supported at the same time.

normal mode:

left panel data is from 0 to (width/2 -1).

right panel data is from width/2 to width-1.

overlap mode:

left panel data is from 0 to (width/2 -1+overlap number).

right panel data is from width/2-overlap number to width-1.

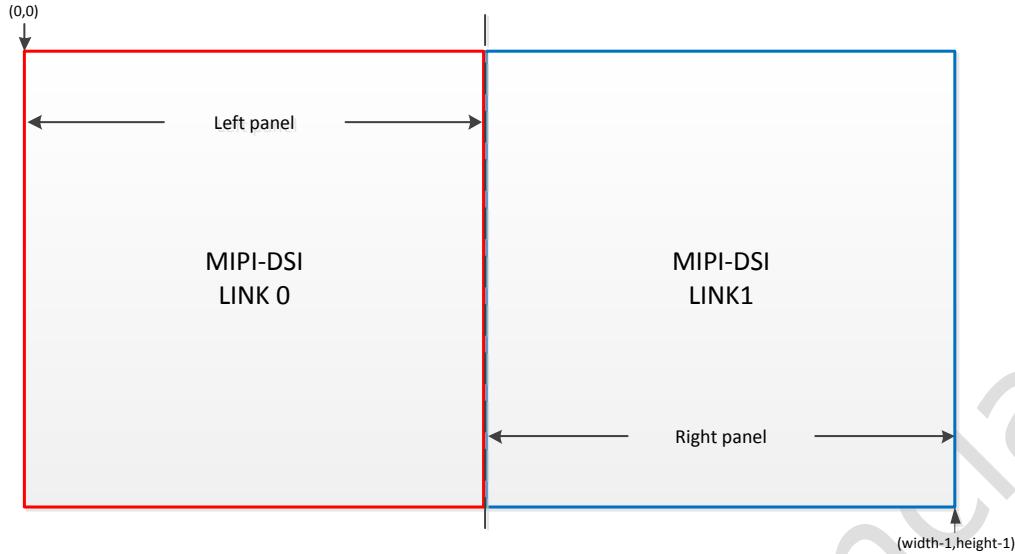


Fig. 8-23 normal mode left-right type display

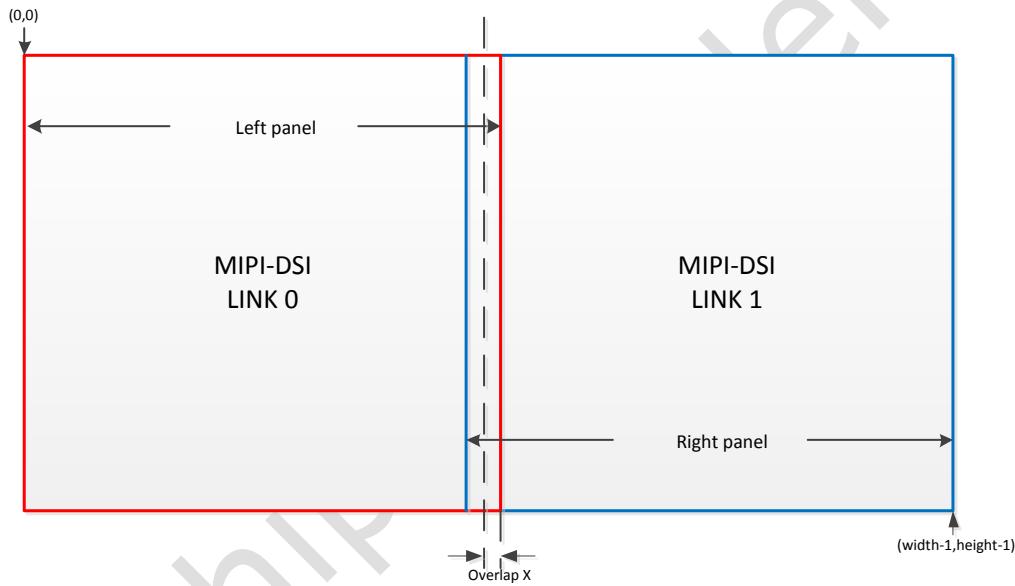


Fig. 8-24 overlap mode left-right type display

The overlap number equal double_ch_overlap_num value *2,in the range of 0~16.

2.halt mode

Mipi halt fuction is supported in this version, detail configuration reference MIPI-DSI chapter.

3.command mode flow

Mipi command mode is supported in this version .

There is programming flows for command mode .

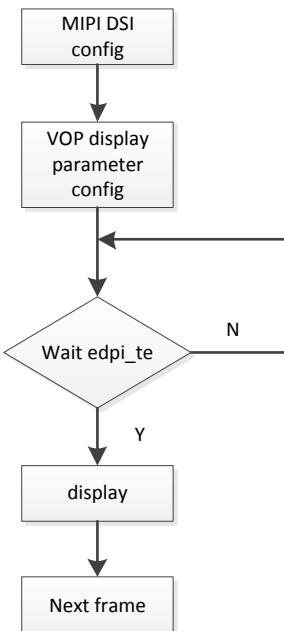


Fig. 8-25 command mode flow

8.7.12 Immediately control register

There are two type register in VOP , one type is effective immediately,the other is effective by frame sync.

Effective immediately registers list as follows,other registers are all effective by frame sync.

Table 8-8 effective immediately register table

register address	description
0x008[23:21],0x008[15:8]	some dsp ctrl function bit
0x00c	sys ctrl1 register
0x018	background color register
0x01c	mcu ctrl register
0x038	win0 color key register
0x078	win1 color key register
0x0cc	win2 color key register
0x11c	win3 color key register
0x188~0x19c	dsp_timing ctrl registers
0x1a0~0x1a8	pwm ctrl registers
0x1c8~0x1dc	cabc_gauss_parameter registers
0x1ec~0x1f4	frc pattern parameter registers

Chapter 9 HDMI Transmitter

9.1 Overview

HDMI TX is fully compliant with HDMI 1.4a and 2.0a specification. It offers a simple implementation for consumer electronics like DVD/player/recorder and camcorder. HDMI TX consists of one HDMI transmitter controller and one HDMI transmitter PHY.

It supports following features:

Video formats:

All CEA-861-E video formats up to 1080p at 60 Hz and 720p/1080i at 120 Hz

Optional HDMI 1.4b video formats

HDMI 2.0 video formats, All CEA-861-F video formats

Colorimetry, 24/30-bit RGB 4:4:4

Pixel clock from 13.5 MHz up to 600 MHz

Up to 192 kHz IEC60958 audio sampling rate

Flexible synchronous enable per clock domain to set functional power down modes

AMBA APB 3.0 register access

I2C DDC, EDID block read mode

SCDC I2C DDC access

TMDS Scrambler to enable support for 2160p@60Hz with RGB 4:4:4

Integrated CEC hardware engine

9.2 Block Diagram

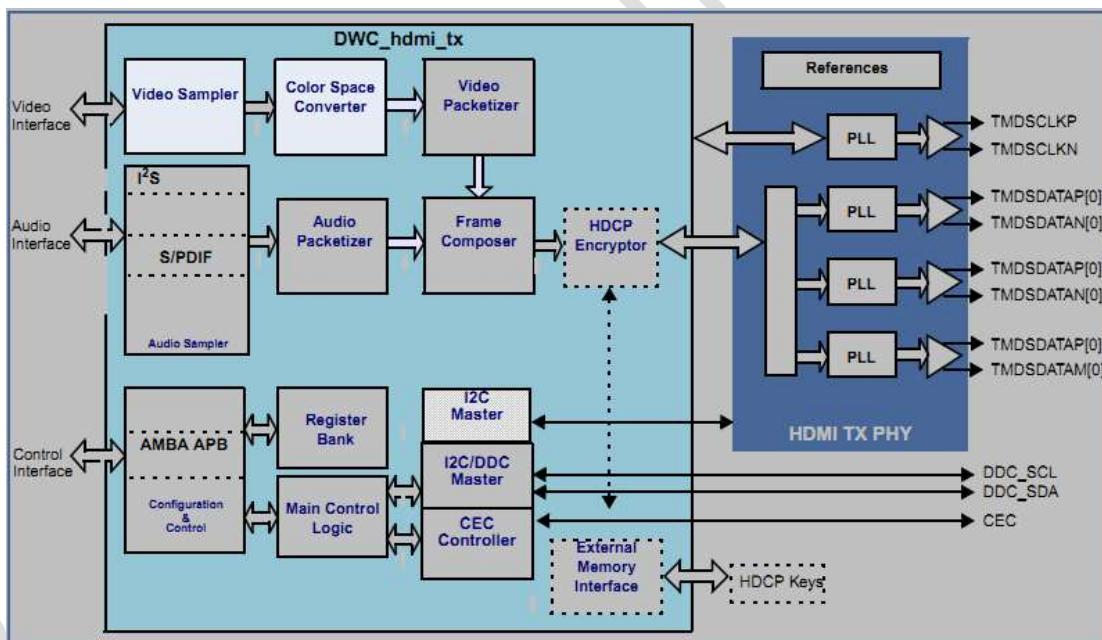


Fig. 9-1 HDMI TX Block Diagram

9.3 Function Description

9.3.1 Video Data Processing

The video processing contain video format timings, pixel encodings(RGB to YCbCr, or YCbCr to RGB), colorimetry and corresponding requirements. This function is implemented by some functional blocks, Video Capture block, Color Space Conversion block, and Deep Color block.

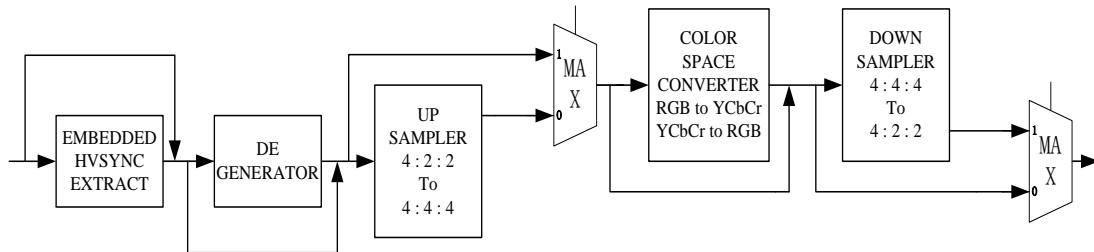


Fig. 9-2 HDMI Video Data Processing

The input video pixels can be encoded in either RGB, YCBCR 4:4:4 or YCBCR 4:2:2 formats by Color Space Conversion block.

The input Video data can have a pixel size of 24, 30bits. The deep color block is used to deal with different pixel size. Video at the default 24-bit color depth is carried at a TMDS clock rate equal to the pixel clock rate. Higher color depths are carried using a correspondingly higher TMDS clock rate. HDMI Transmitter support video formats with TMDS rates below 25MHz (e.g. 13.5MHz for 480i/NTSC) that can be transmitted using a pixel-repetition scheme by setting relative registers.

The following interface timing diagram outlines the Video interface signal format. 24 bit data (we also support 36 bit data for deep color) in RGB can be captured by the rising edge of VCLK with 1ns setup time and 1ns hold time requirements. Control signals such DE and VSync/HSync/FSync going with the same timing relationship.

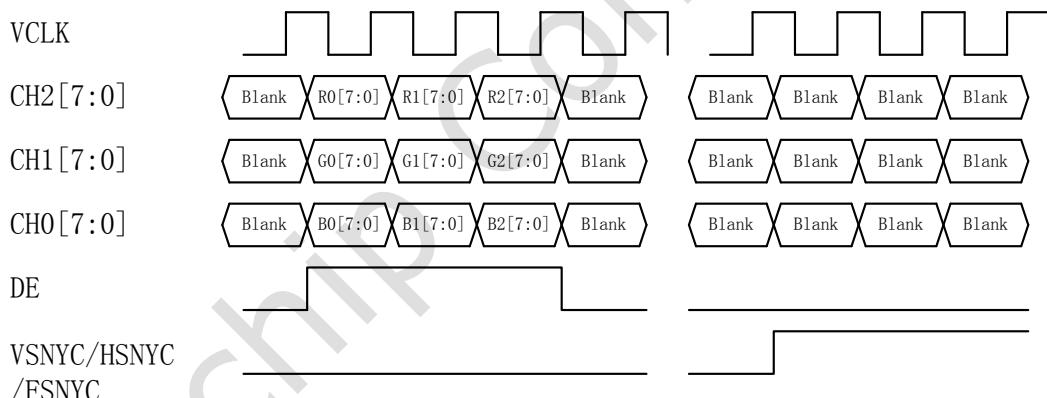


Fig. 9-3 HDMI Video Processing Timing

1. Video Data Capture Logic

HDMI TX support input video data related format table is listed below.

Table 9-1 HDMI Supported Input Video Formats

Color Space	Pixel Encoding	Sync	Channel Width	Pin Nums
RGB	4:4:4	Separate	8	24
RGB	4:4:4	Separate	10	30
RGB	4:4:4	Separate	12	36
YCbCr	4:4:4	Separate	8	24
YCbCr	4:4:4	Separate	10	30
YCbCr	4:4:4	Separate	12	36
YCbCr	4:2:2	Separate	8	16
YCbCr	4:2:2	Separate	10	20

Color Space	Pixel Encoding	Sync	Channel Width	Pin Nums
YCbCr	4:2:2	Separate	12	24
YCbCr	4:4:4	Embedded	8	24
YCbCr	4:4:4	Embedded	10	30
YCbCr	4:4:4	Embedded	12	36
YCbCr	4:2:2	Embedded	8	16
YCbCr	4:2:2	Embedded	10	20
YCbCr	4:2:2	Embedded	12	24

2. Embedded Sync Extraction Module

The module is used to extract Vsync and Hsync signals from input video data stream such as ITU656 format. With setting the relative registers, this functional module can extract correct video sync signals for later process block using.

3. Data Enable (DE) Generator

HDMI Transmitter has DE signal generator by incoming HSYNCs, VSYNCs and Video clock. External DE is optional and selected by appropriate register settings. This feature is particularly useful when interfacing to MPEG decoders that do not provide a specific DE output signal.

4. Color Space Conversion

HDMI Transmitter Color space conversion (CSC) is available to interface for several MPEG decoders like with YCbCr-only outputs, and to provide full DVI backwards compatibility.

The function of this module is to perform color space conversion functionality as listed below.

- (1). Convert RGB input Video data to YCbCr Video data.
- (2). Convert YCbCr input Video data to RGB Video data.
- (3). upsample for YCbCr 4:2:2 to YCbCr 4:4:4
- (4). downsample for YCbCr 4:4:4 to YCbCr 4:2:2

9.3.2 Audio Data Processing

The HDMI TX audio process contain audio clock regeneration, placement of audio samples within packets, packet timing control, audio sample rates setting, and channel/speaker assignments. This function is implemented by Audio Capture blocks

The Audio Capture support either SPDIF or four channel I2S input. SPDIF input supports audio sampling rates from 32 to 192 KHz. The I2S input supports from 2-channel to 8-channel audio up to 192 KHz.

The scheme of audio processing as shown in the figure below:

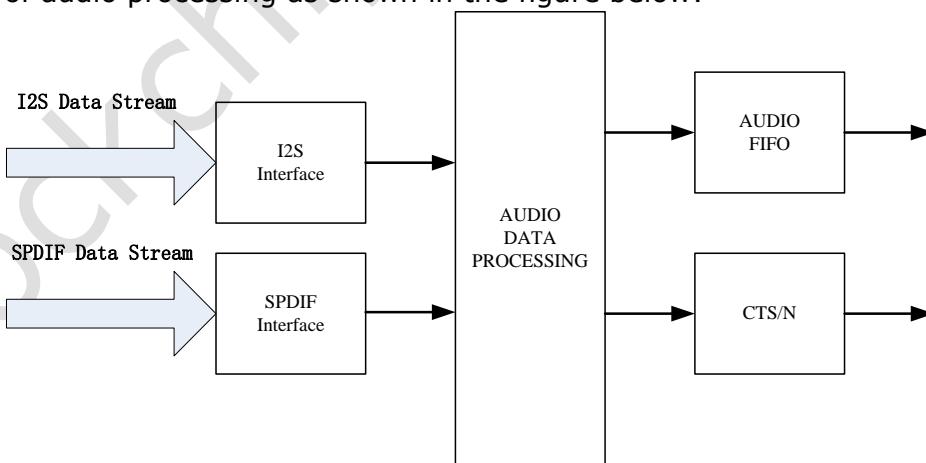


Fig. 9-4 HDMI Audio Data Processing Diagram

1.I2S

The function of this module is to implement I2S audio input feature. The incoming audio stream is captured, processed then transmitted into the TMDS link. Four I2S inputs also allow transmission of DVD-Audio and decoded Dolby Digital to A/V Receivers and high-end displays. The interface supports from 2-channel to 8-channel audio up to 192 kHz. The I2S pins must also be coherent with mclk. The appropriate registers must be configured to describe the

format of audio being input. This information is passed over the HDMI link in the CEA-861D Audio Info (AI) packets. Table shows the I2S 8 channel audio formats that are supported for each of the video formats.

Table 9-2 HDMI TX I2S 2 Channel Audio Sampling Frequency

Video Format	32kHz	44.1kHz	48kHz	88.2kHz	96kHz	176.4kHz	192kHz
720x480p /720x576p	Yes	Yes	Yes	Yes	Yes	Yes	Yes
1440x480i/ 1440x576i	Yes	Yes	Yes	Yes	Yes	Yes	Yes
720p	Yes	Yes	Yes	Yes	Yes	Yes	Yes
1080i	Yes	Yes	Yes	Yes	Yes	Yes	Yes
1080p	Yes	Yes	Yes	Yes	Yes	Yes	Yes

Table 9-3 HDMI TX I2S 8 Channel Audio Sampling Frequency

Video Format	32kHz	44.1kHz	48kHz	88.2kHz	96kHz	176.4kHz	192kHz
720x480p /720x576p	Yes	Yes	Yes	No	No	No	No
1440x480i/ 1440x576i	Yes	Yes	Yes	Yes	No	No	No
720p	Yes	Yes	Yes	Yes	Yes	Yes	Yes
1080i	Yes	Yes	Yes	Yes	Yes	Yes	Yes
1080p	Yes	Yes	Yes	Yes	Yes	Yes	Yes

2.SPDIF

The function of this module is to implement SPDIF audio input feature. The incoming audio stream is captured, processed then transmitted into the TMDS link. SPDIF stream can carry 2-channel uncompressed PCM data (IEC 60958) or a compressed bit stream for multi-channel (IEC 61937) formats. The audio data capture logic forms the audio data into packets in accordance with the HDMI specification. SPDIF input supports audio sampling rates from 32 to 192 KHz. The following shows the SPDIF audio formats that are supported for each of the video formats

Table 9-4 HDMI SPDIF Sampling Frequency at Each Video Format

Video Format	32kHz	44.1kHz	48kHz	88.2kHz	96kHz	176.4kHz	192kHz
720x480p /720x576p	Yes	Yes	Yes	Yes	Yes	No	No
1440x480i/ 1440x576i	Yes	Yes	Yes	Yes	Yes	No	No
720p	Yes	Yes	Yes	Yes	Yes	Yes	Yes
1080i	Yes	Yes	Yes	Yes	Yes	Yes	Yes
1080p	Yes	Yes	Yes	Yes	Yes	Yes	Yes

3.Audio Sample Clock Capture and Regeneration

Audio data being carried across the HDMI link, which is driven by a TMDS clock running at a rate corresponding to the video pixel rate, does not retain the original audio sample clock. The task of recreating this clock at the Sink is called Audio Clock Regeneration.

The HDMI Transmitter determine the fractional relationship between the TMDS clock and an audio reference clock (128 audio sample rate [fs]) and pass the numerator and denominator of that fraction to the HDMI Sink across the HDMI link. The Sink then re-create the audio clock from the TMDS clock by using a clock divider and a clock multiplier.

The exact relationship between the two clocks will be.

$$128 \cdot f_S = f_{TMDS_clock} \cdot N / CTS.$$

The scheme of the Audio Sample Clock Capture and Regeneration as shown below:

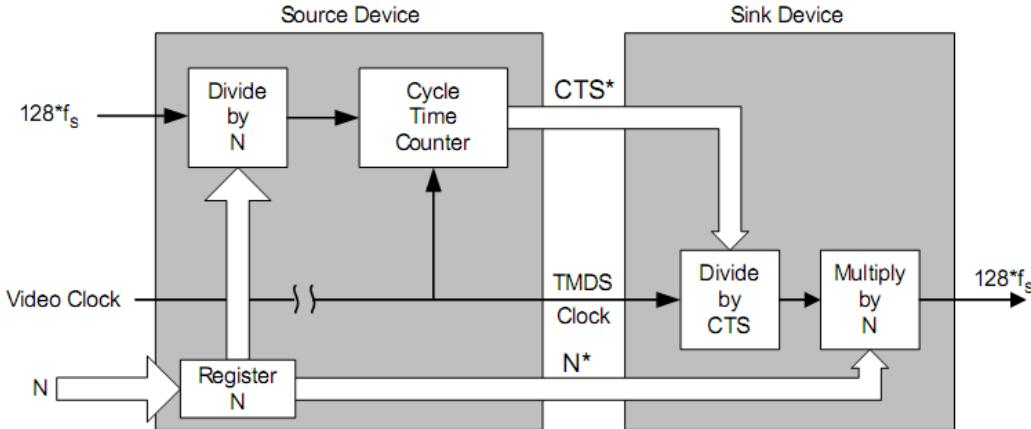


Fig. 9-5 HDMI Audio Clock Regeneration Model

Because there is no audio clock carried through the HDMI link, only the TMDS clock is used. Software sets the CTS/N with a value taken from the below table, which shows the CTS and N value for the supported standard. All other TMDS clocks are not supported; The TMDS clocks divided or multiplied by 1,001 coefficients are not supported.

Table 9-5 HDMI CTS and N table

f _s (kHz)	TMDS Clock (MHz)													
	25.2		27		54		74.25		148.5		297		597	
N	CTS	N	CTS	N	CTS	N	CTS	N	CTS	N	CTS	N	CTS	
32	4096	25200	4096	27000	4096	54000	4096	74250	4096	148500	3072	222750	3072	445500
44.1	6272	28000	6272	30000	6272	60000	6272	82500	6272	165000	4704	247500	9408	990000
48	6144	25200	6144	27000	6144	54000	6144	74250	6144	148500	5120	247500	6144	495000
88.2	12544	28000	12544	30000	12544	60000	12544	82500	12544	165000	9408	247500	18816	990000
96	12288	25200	12288	27000	12288	54000	12288	74250	12288	148500	10240	247500	12288	495000
176.4	25088	28000	25088	30000	25088	60000	25088	82500	25088	165000	18816	247500	37632	990000
192	24576	25200	24576	27000	24576	54000	24576	74250	24576	148500	20480	247500	24576	4950000

9.3.3 DDC

The DDC functional block is used for configuration and status exchange between the HDMI Source and HDMI Sink. HDMI Transmitter Controller has I2C Master Interface for DDC transactions. It enables for host controller to read EDID, HDCP authentication by issuing simple register access. The I2C bus speed is limited by DDC specification. DDC bus access frequency can be controlled.

9.3.4 EDID

Extended Display Identification Data (EDID) was created by VESA to enable plug and play capabilities of monitors. This data, which is stored in the sink device, describes video formats that the DTV Monitor is capable of receiving and rendering. The information is supplied to the source device, over the interface, upon the request of the source device. The source device then chooses its output format, taking into account the format of the original video stream and the formats supported by the DTV Monitor. The function of this module is to implement EDID feature.

9.3.5 HDCP

HDMI Transmitter has a capability for HDCP authentication by hardware. The function of this module is to implement HDCP encryption feature. This feature can be turned on or off depending on register setting.

9.3.6 Hot Plug Detect

HDMI Transmitter has a capability for detecting the Sink plug in or plug out, and launch an interrupt and registers state indicating for software controlling.

9.3.7 TMDS encoder

The TMDS encoder converts the 2/4/8 bits data into the 10 bit DC-balanced TMDS data. HDMI TX put the TMDS encoding on the audio /video /aux data received from the HDCP XOR mask. This data is output onto three TMDS differential data lines along with a TMDS differential clock.

9.3.8 CEC

The CEC functional block provides high-level control functions between all of the various audiovisual products in a user's environment through one line.

9.4 Register Description

The address offset of the HDMI TX is 0xff980000, it contains 16 address section. The offset of the table of Register Summary must multiple with 4 when software configure it. Like the Interrupt registers, its base address is 0x0100. If we want to configure it, its real address is 0xff980000+0x0100*4.

We can configure the HDMI PHY register through the internal I2C interface. The internal I2C register interface map with the address which from 0x3020. We just to configure the register which can trigger one i2c write or i2c read. For example, we configure the PLL through these register.

9.4.1 Register Summary

Name	Offset	Size	Reset Value	Description
Identification Registers	0x0000	B		Identification releted registers
Interrupt registers	0x0100	B		Interrupt releted registers
Video Sampler registers	0x0200	B		Video Sampler registers
Video Packetizer registers	0x0800	B		Video Packetizer registers
Frame Composer Registers	0x1000	B		Frame Composer Registers
HDMI Source PHY Registers	0x3000	B		HDMI Source PHY Registers
I2C Master PHY Registers	0x3020	B		I2C Master PHY Registers
Audio Sampler Registers	0x3100	B		Audio Sampler Registers
Main Controller Registers	0x4000	B		Main Controller Registers
Color Space Converter Registers	0x4100	B		Color Space Converter Registers
HDCP Encryption Engine Registers	0x5000	B		HDCP Encryption Engine Registers
HDCP BKSV Registers	0x7800	B		HDCP BKSV Registers
HDCP AN Registers	0x7805	B		HDCP AN Registers
Encrypted DPK Embedded Storage Registers	0x780E	B		Encrypted DPK Embedded Storage Registers
CEC Engine Registers	0x7D00	B		CEC Engine Registers
I2C Master Registers	0x7E00	B		I2C Master Registers for E-DDC/SCDC

Name	Offset	Size	Reset Value	Description
Identification Registers	0x0000	B		Identification releted registers
Interrupt registers	0x0100	B		Interrupt releted registers
Video Sampler registers	0x0200	B		Video Sampler registers
Video Packetizer registers	0x0800	B		Video Packetizer registers
Frame Composer Registers	0x1000	B		Frame Composer Registers
HDMI Source PHY Registers	0x3000	B		HDMI Source PHY Registers
I2C Master PHY Registers	0x3020	B		I2C Master PHY Registers
Audio Sampler Registers	0x3100	B		Audio Sampler Registers
Main Controller Registers	0x4000	B		Main Controller Registers
Color Space Converter Registers	0x4100	B		Color Space Converter Registers
HDCP Encryption Engine Registers	0x5000	B		HDCP Encryption Engine Registers
HDCP BKSV Registers	0x7800	B		HDCP BKSV Registers
HDCP AN Registers	0x7805	B		HDCP AN Registers
Encrypted DPK Embedded Storage Registers	0x780E	B		Encrypted DPK Embedded Storage Registers
CEC Engine Registers	0x7D00	B		CEC Engine Registers
I2C Master Registers	0x7E00	B		I2C Master Registers for E-DDC/SCDC

9.4.2 Registers Detail

Identification Registers

Identification Registers. Follow the link for the register to see a detailed description of the register.

Registers for Address Block: Identification

Register	Offset	Description
design_id	0x0	Design Identification Register
revision_id	0x1	Revision Identification Register
product_id0	0x2	Product Identification Register 0
product_id1	0x3	Product Identification Register 1
config0_id	0x4	Configuration Identification Register 0
config1_id	0x5	Configuration Identification Register 1
config2_id	0x6	Configuration Identification Register 2
config3_id	0x7	Configuration Identification Register 3

design_id

Description: Design Identification Register

Size: 8 bits

Offset: 0x0

Bits	Name	Attr	Description
7:0	design_id	R	Design ID code fixed by HDMI that Identifies the instantiated DWC_hdmi_tx controller. For example, DWC_hdmi_tx 2.11a, DESIGN_ID = 21 Value After Reset: 0x21

revision_id

Description: Revision Identification Register

Size: 8 bits

Offset: 0x1

Bits	Name	Attr	Description
7:0	revision_id	R	Revision ID code fixed by HDMI that Identifies the instantiated DWC_hdmi_tx controller. Value After Reset: 0x1a

product_id0

Description: Product Identification Register 0

Size: 8 bits

Offset: 0x2

Bits	Name	Attr	Description
7:0	product_id0	R	This one byte fixed code Identifies HDMI's product line ("A0h" for DWC_hdmi_tx products). Value After Reset: 0xa0

product_id1

Description: Product Identification Register 1

Size: 8 bits

Offset: 0x3

Bits	Name	Attr	Description
7:6	product_id1_hdcp	R	These bits identify a HDMI Controller with HDCP encryption according to HDMI product line. Value After Reset: "(HDCP== 1) ? 3 : 0"
5:2			Reserved for future use.
1	product_id1_rx	R	This bit Identifies HDMI's DWC_hdmi_rx Controller according to HDMI product line. Value After Reset: 0x0
0	product_id1_tx	R	This bit Identifies H Controller according to HDMI product line. Value After Reset: 0x1

config0_id

Description: Configuration Identification Register 0

Size: 8 bits

Offset: 0x4

Bits	Name	Attr	Description
7	prepen	R	Indicates if it is possible to use internal pixel repetition Value After Reset: "(HDMI_TX_INTPREPEN== 1) ? 1 : 0"
6			Reserved for future use.
5	audspdif	R	Indicates if the SPDIF audio interface is present Value After Reset: "(SPDIFPORTS== 1) ? 1 : 0"
4	audi2s	R	Indicates if I2S interface is present Value After Reset: "(I2SPORTS== 1) ? 1 : 0"
3	hdmi14	R	Indicates if HDMI 1.4 features are present Value After Reset: "(HDMI_TX_14== 1) ? 1 : 0"
2	csc	R	Indicates if Color Space Conversion block is present Value After Reset: "(CSC== 1) ? 1 : 0"
1	cec	R	Indicates if CEC is present Value After Reset: "(CEC== 1) ? 1 : 0"
0	hdcp	R	Indicates if HDCP is present Value After Reset: "(HDCP== 1) ? 1 : 0"

config1_id

Description: Configuration Identification Register 1

Size: 8 bits

Offset: 0x5

Bits	Name	Attr	Description
7	hdcp22_snps	R	Indicates if HDCP 2.2 SNPS solution is present Value After Reset: $(\text{HTX_HDCP22_SNPS} == 1) ? 1 : 0$
6	hdcp22_ext	R	Indicates if external HDCP 2.2 interface support is present Value After Reset: $"(\text{HTX_HDCP22_EXTERNAL} == 1) ? 1 : 0"$
5	hdmi20	R	Indicates if HDMI 2.0 features are present Value After Reset: $"(\text{HDMI_TX_20} == 1) ? 1 : 0"$
4:2			Reserved for future use.
1	confapb	R	Indicates that configuration interface is APB interface Value After Reset: 0x1
0			Reserved for future use.

config2_id

Description: Configuration Identification Register 2

Size: 8 bits

Offset: 0x6

Bits	Name	Attr	Description
7:0	phytype	R	Indicates the type of PHY interface selected: 0x00: Legacy PHY (HDMI Tx PHY) 0xF2: PHY GEN2 (HDMI 3D TX PHY) 0xE2: PHY GEN2 (HDMI 3D TX PHY) + HEAC PHY 0xC2: PHY MHL COMBO (MHL+HDMI 2.0 TX PHY) 0xB2: PHY MHL COMBO (MHL+HDMI 2.0 TX PHY) + HEAC PHY 0xF3: PHY HDMI 20 (HDMI 2.0 TX PHY) 0xE3: PHY HDMI 20 (HDMI 2.0 TX PHY) + HEAC PHY 0xFE: External PHY Value After Reset: $"(\text{PHY_HDMI20} == 1) ? ((\text{HDMI_HEAC_PHY_EN} == 1) ? 0xE3 : 0xF3) : ((\text{PHY_MHL_COMBO} == 1) ? ((\text{HDMI_HEAC_PHY_EN} == 1) ? 0xB2 : 0xC2) : (\text{PHY_GEN2} == 1) ? ((\text{HDMI_HEAC_PHY_EN} == 1) ? 0xE2 : 0xF2) : (\text{PHY_EXTERNAL} == 1) ? 0xFE : 0x00"$

config3_id

Description: Configuration Identification Register 3

Size: 8 bits

Offset: 0x7

Bits	Name	Attr	Description
7:2			Reserved for future use.
1	confahbaudma	R	Indicates that the audio interface is AHB AUD DMA Value After Reset: $"(\text{AHBAUDDMAIF} == 1) ? 1 : 0"$
0	cfgpaud	R	Indicates that the audio interface is Generic Parallel Audio (GPAUD) Value After Reset: $"(\text{GPAUDPORTS} == 1) ? 1 : 0"$

Interrupt Registers

Interrupt Registers. Follow the link for the register to see a detailed description of the register.
Registers for Address Block: Interrupt

Register	Offset	Description
ih_fc_stat0	0x100	Frame Composer Interrupt Status Register 0 (Packet Interrupts)
ih_fc_stat1	0x101	Frame Composer Interrupt Status Register 1 (Packet Interrupts)
ih_fc_stat2	0x102	Frame Composer Interrupt Status Register 2 (Packet Interrupts)
ih_as_stat0	0x103	Audio Sampler Interrupt Status Register (FIFO Threshold, Underflow and Overflow Interrupts)
ih_phy_stat0	0x104	PHY Interface Interrupt Status Register (RXSENSE, PLL Lock and HPD Interrupts)
ih_i2cm_stat0	0x105	E-DDC I2C Master Interrupt Status Register (Done and Error Interrupts)
ih_cec_stat0	0x106	CEC Interrupt Status Register (Functional Operation Interrupts)
ih_vp_stat0	0x107	Video Packetizer Interrupt Status Register (FIFO Full and Empty Interrupts)
ih_i2cmphy_stat0	0x108	PHY GEN2 I2C Master Interrupt Status Register (Done and Error Interrupts)
ih_ahbdmaaud_stat0	0x109	AHB Audio DMA Interrupt Status Register (Functional Operation, Buffer Full and Empty...)
ih_decode	0x170	Interruption Handler Decode Assist Register
ih_mute_fc_stat0	0x180	Frame Composer Interrupt Mute Control Register 0
ih_mute_fc_stat1	0x181	Frame Composer Interrupt Mute Control Register 1
ih_mute_fc_stat2	0x182	Frame Composer Interrupt Mute Control Register 2
ih_mute_as_stat0	0x183	Audio Sampler Interrupt Mute Control Register
ih_mute_phy_stat0	0x184	PHY Interface Interrupt Mute Control Register
ih_mute_i2cm_stat0	0x185	E-DDC I2C Master Interrupt Mute Control Register
ih_mute_cec_stat0	0x186	CEC Interrupt Mute Control Register
ih_mute_vp_stat0	0x187	Video Packetizer Interrupt Mute Control Register
ih_mute_i2cmphy_stat0	0x188	PHY GEN2 I2C Master Interrupt Mute Control Register
ih_mute_ahbdmaaud_stat0	0x189	AHB Audio DMA Interrupt Mute Control Register
ih_mute	0x1ff	Global Interrupt Mute Control Register

ih_fc_stat0

Description: Frame Composer Interrupt Status Register 0 (Packet Interrupts)

Size: 8 bits

Offset: 0x100

Bits	Name	Attr	Description
7	AUDI	R/W1C	Active after successful transmission of an Audio InfoFrame packet. Value After Reset: 0x0
6	ACP	R/W1C	Active after successful transmission of an Audio Content Protection packet. Value After Reset: 0x0
5	HBR	R/W1C	Active after successful transmission of an Audio HBR

			packet. Value After Reset: 0x0
4	MAS	R/W1C	Active after successful transmission of an MultiStream Audio packet Value After Reset: 0x0
3	NVBI	R/W1C	Active after successful transmission of an NTSC VBI packet Value After Reset: 0x0
2	AUDS	R/W1C	Active after successful transmission of an Audio Sample packet. Due to high number of audio sample packets transmitted, this interrupt is by default masked at frame composer. Value After Reset: 0x0
1	ACR	R/W1C	Active after successful transmission of an Audio Clock Regeneration (N/ CTS transmission) packet. Value After Reset: 0x0
0	NULL	R/W1C	Active after successful transmission of an Null packet. Due to high number of audio sample packets transmitted, this interrupt is by default masked at frame composer. Value After Reset: 0x0

ih_fc_stat1

Description: Frame Composer Interrupt Status Register 1 (Packet Interrupts)

Size: 8 bits

Offset: 0x101

Bits	Name	Attr	Description
7	GMD	R/W1C	Active after successful transmission of an Gamut metadata packet. Value After Reset: 0x0
6	ISCR1	R/W1C	Active after successful transmission of an International Standard Recording Code 1 packet. Value After Reset: 0x0
5	ISCR2	R/W1C	Active after successful transmission of an International Standard Recording Code 2 packet Value After Reset: 0x0
4	VSD	R/W1C	Active after successful transmission of an Vendor Specific Data InfoFrame packet. Value After Reset: 0x0
3	SPD	R/W1C	Active after successful transmission of an Source Product Descriptor InfoFrame packet. Value After Reset: 0x0
2	AMP	R/W1C	Active after successful transmission of an Audio Metadata packet Value After Reset: 0x0
1	AVI	R/W1C	Active after successful transmission of an AVI InfoFrame packet. Value After Reset: 0x0
0	GCP	R/W1C	Active after successful transmission of an General Control Packet. Value After Reset: 0x0

ih_fc_stat2

Description: Frame Composer Interrupt Status Register 2 (Packet Interrupts)

Size: 8 bits

Offset: 0x102

Bits	Name	Attr	Description
7:5			Reserved for future use.
4	DRM	R/W1C	Active after successful transmission of an DRM packet Value After Reset: 0x0
1	LowPriority_o verflow	R/W1C	Frame Composer low priority packet queue descriptor overflow indication Value After Reset: 0x0
0	HighPriority_ overflow	R/W1C	Frame Composer high priority packet queue descriptor overflow indication Value After Reset: 0x0

ih_as_stat0

Description: Audio Sampler Interrupt Status Register (FIFO Threshold, Underflow and Overflow Interrupts)

Size: 8 bits

Offset: 0x103

Bits	Name	Attr	Description
7:5			Reserved for future use.
4	fifo_underrun	R/W1C	Indicates an underrun on the audio FIFO Value After Reset: 0x0
3	fifo_overrun	R/W1C	Indicates an overrun on the audio FIFO. Value After Reset: 0x0
2	Aud_fifo_und erflow_thr	R/W1C	Audio Sampler audio FIFO empty threshold (four samples) indication for the legacy HBR audio interface. For AHB_DMA, this bit indicates that the number of samples in the FIFO is equal to (or less) than the number of active audio channels. This bit is not relevant for I2S, SPDIF, and GPA interfaces. Value After Reset: 0x0
1	Aud_fifo_und erflow	R/W1C	Audio Sampler audio FIFO empty indication. Value After Reset: 0x0
0	Aud_fifo_ove rflow	R/W1C	Audio Sampler audio FIFO full indication. Value After Reset: 0x0

ih_phy_stat0

Description: PHY Interface Interrupt Status Register (RXSENSE, PLL Lock and HPD Interrupts)

Size: 8 bits

Offset: 0x104

Bits	Name	Attr	Description
7:6			Reserved for future use.
5	RX_SENSE_3	R/W1C	TX PHY RX_SENSE indication for driver 3. You may need to mask or change polarity of this interrupt after it has become active. Value After Reset: 0x0
4	RX_SENSE_2	R/W1C	TX PHY RX_SENSE indication for driver 2. You may need to mask or change polarity of this interrupt after it has become active. Value After Reset: 0x0
3	RX_SENSE_1	R/W1C	TX PHY RX_SENSE indication for driver 1. You may need to mask or change polarity of this

			interrupt after it has become active. Value After Reset: 0x0
2	RX_SENSE_0	R/W1C	TX PHY RX_SENSE indication for driver 0. You may need to mask or change polarity of this interrupt after it has become active. Value After Reset: 0x0
1	TX_PHY_LOC_K	R/W1C	TX PHY PLL lock indication. Value After Reset: 0x0
0	HPD	R/W1C	HDMI Hot Plug Detect indication. You may need to mask or change polarity of this interrupt after it has become active. Value After Reset: 0x0

ih_i2cm_stat0

Description: E-DDC I2C Master Interrupt Status Register (Done and Error Interrupts)

Size: 8 bits

Offset: 0x105

Bits	Name	Attr	Description
7:3			Reserved for future use.
2	scdc_readreq	R/W1C	I2C Master SCDC read request indication. Value After Reset: 0x0
1	I2Cmasterdone	R/W1C	I2C Master done indication Value After Reset: 0x0
0	I2Cmastererr	R/W1C	I2C Master error indication Value After Reset: 0x0

ih_cec_stat0

Description: CEC Interrupt Status Register (Functional Operation Interrupts)

Size: 8 bits

Offset: 0x106

Bits	Name	Attr	Description
7			Reserved for future use.
6	WAKEUP	R/W1C	CEC Wake-up indication Value After Reset: 0x0
5	ERROR_FOLL_OW	R/W1C	CEC Error Follow indication Value After Reset: 0x0
4	ERROR_INIT_IATOR	R/W1C	CEC Error Initiator indication Value After Reset: 0x0
3	ARB_LOST	R/W1C	CEC Arbitration Lost indication Value After Reset: 0x0
2	NACK	R/W1C	CEC Not Acknowledge indication Value After Reset: 0x0
1	EOM	R/W1C	CEC End of Message Indication Value After Reset: 0x0
0	DONE	R/W1C	CEC Done Indication Value After Reset: 0x0

ih_vp_stat0

Description: Video Packetizer Interrupt Status Register (FIFO Full and Empty Interrupts)

Size: 8 bits

Offset: 0x107

Bits	Name	Attr	Description
7	fifofullrepet	R/W1C	Video Packetizer pixel repeater FIFO full interrupt Value After Reset: 0x0
6	fifoemptyrep	R/W1C	Video Packetizer pixel repeater FIFO empty interrupt Value After Reset: 0x0

5	fifofullpp	R/W1C	Video Packetizer pixel packing FIFO full interrupt Value After Reset: 0x0
4	fifoemptypp	R/W1C	Video Packetizer pixel packing FIFO empty interrupt Value After Reset: 0x0
3	fifofullremap	R/W1C	Video Packetizer pixel YCC 422 re-mapper FIFO full interrupt Value After Reset: 0x0
2	fifoemptyremap	R/W1C	Video Packetizer pixel YCC 422 re-mapper FIFO empty interrupt Value After Reset: 0x0
1:0		R/W1C	Reserved and read as zero

ih_i2cmphy_stat0

Description: PHY GEN2 I2C Master Interrupt Status Register (Done and Error Interrupts)

Size: 8 bits

Offset: 0x108

Bits	Name	Attr	Description
7:2			Reserved for future use.
1	I2Cmphydone	R/W1C	I2C Master PHY done indication Value After Reset: 0x0
0	I2Cmphyerror	R/W1C	I2C Master PHY error indication Value After Reset: 0x0

ih_ahbdmaaud_stat0

Description: AHB Audio DMA Interrupt Status Register (Functional Operation, Buffer Full and Empty Interrupts)

Size: 8 bits

Offset: 0x109

Bits	Name	Attr	Description
7			Reserved for future use.
6	ahbdmaaud_intbuffoverrun	R/W1C	AHB audio DMA Buffer overrun interruption Value After Reset: 0x0
5	ahbdmaaud_interror	R/W1C	AHB audio DMA error interrupt Value After Reset: 0x0
4	ahbdmaaud_intlostownership	R/W1C	AHB audio DMA lost ownership interrupt Value After Reset: 0x0
3	ahbdmaaud_intretrysplit	R/W1C	AHB audio DMA RETRY/SPLIT interrupt Value After Reset: 0x0
2	ahbdmaaud_intdone	R/W1C	AHB audio DMA done interrupt Value After Reset: 0x0
1	ahbdmaaud_intbufffull	R/W1C	AHB audio DMA Buffer full interrupt Value After Reset: 0x0
0	ahbdmaaud_intbuffempty	R/W1C	AHB audio DMA Buffer empty interrupt Value After Reset: 0x0

ih_decode

Description: Interruption Handler Decode Assist Register

Size: 8 bits

Offset: 0x170

Bits	Name	Attr	Description
7	ih_fc_stat0	R	Interruption active at the ih_fc_stat0 register Value After Reset: 0x0

Bits	Name	Attr	Description
6	ih_fc_stat1	R	Interruption active at the ih_fc_stat1 register Value After Reset: 0x0
5	ih_fc_stat2_vp	R	Interruption active at the ih_fc_stat2 or ih_vp_stat0 register Value After Reset: 0x0
4	ih_as_stat0	R	Interruption active at the ih_as_stat0 register Value After Reset: 0x0
3	ih_phy	R	Interruption active at the ih_phy_stat0 or ih_i2cmphy_stat0 register Value After Reset: 0x0
2	ih_i2cm_stat0	R	Interruption active at the ih_i2cm_stat0 register Value After Reset: 0x0
1	ih_cec_stat0	R	Interruption active at the ih_cec_stat0 register Value After Reset: 0x0
0	ih_ahbdmaaud_stat0	R	Interruption active at the ih_ahbdmaaud_stat0 register Value After Reset: 0x0

ih_mute_fc_stat0

Description: Frame Composer Interrupt Mute Control Register 0

Size: 8 bits

Offset: 0x180

Bits	Name	Attr	Description
7	AUDI	R/W	When set to 1, mutes ih_fc_stat0[7] Value After Reset: 0x0
6	ACP	R/W	When set to 1, mutes ih_fc_stat0[6] Value After Reset: 0x0
5	HBR	R/W	When set to 1, mutes ih_fc_stat0[5] Value After Reset: 0x0
4	MAS	R/W	When set to 1, mutes ih_fc_stat0[4]. Otherwise, this field is a "spare" bit with no associated functionality. Value After Reset: "(HDMI_TX_20== 1) ? 1 : 0"
3	NVBI	R/W	When set to 1, mutes ih_fc_stat0[3]. Otherwise, this field is a "spare" bit with no associated functionality. Value After Reset: "(HDMI_TX_20== 1) ? 1 : 0"
2	AUDS	R/W	When set to 1, mutes ih_fc_stat0[2] Value After Reset: 0x0
1	ACR	R/W	When set to 1, mutes ih_fc_stat0[1] Value After Reset: 0x0
0	NULL	R/W	When set to 1, mutes ih_fc_stat0[0] Value After Reset: 0x0

ih_mute_fc_stat1

Description: Frame Composer Interrupt Mute Control Register 1

Size: 8 bits

Offset: 0x181

Bits	Name	Attr	Description
7	GMD	R/W	When set to 1, mutes ih_fc_stat1[7] Value After Reset: 0x0
6	ISCR1	R/W	When set to 1, mutes ih_fc_stat1[6] Value After Reset: 0x0
5	ISCR2	R/W	When set to 1, mutes ih_fc_stat1[5] Value After Reset: 0x0
4	VSD	R/W	When set to 1, mutes ih_fc_stat1[4]

Bits	Name	Attr	Description
			Value After Reset: 0x0
3	SPD	R/W	When set to 1, mutes ih_fc_stat1[3] Value After Reset: 0x0
2	AMP	R/W	When set to 1, mutes ih_fc_stat1[2]. Otherwise, this field is a "spare" bit with no associated functionality. Value After Reset: "(HDMI_TX_20== 1) ? 1 : 0" Exists: HDMI_TX_20==1
1	AVI	R/W	When set to 1, mutes ih_fc_stat1[1] Value After Reset: 0x0
0	GCP	R/W	When set to 1, mutes ih_fc_stat1[0] Value After Reset: 0x0

ih_mute_fc_stat2

Description: Frame Composer Interrupt Mute Control Register 2

Size: 8 bits

Offset: 0x182

Bits	Name	Attr	Description
7:5			Reserved for future use.
4	DRM	R/W	When set to 1, mutes ih_fc_stat2[4]. Value After Reset: (HDMI_TX_20== 1) ? 1 : 0
3:2			Reserved for future use
1	LowPriority_overflow	R/W	When set to 1, mutes ih_fc_stat2[1] Value After Reset: 0x0
0	HighPriority_overflow	R/W	When set to 1, mutes ih_fc_stat2[0] Value After Reset: 0x0

ih_mute_as_stat0

Description: Audio Sampler Interrupt Mute Control Register

Size: 8 bits

Offset: 0x183

Bits	Name	Attr	Description
7:5			Reserved for future use.
4	fifo_underrun	R/W	When set to 1, mutes ih_as_stat0[4] Value After Reset: 0x1
3	fifo_overrun	R/W	When set to 1, mutes ih_as_stat0[3] Value After Reset: 0x1
2	Aud_fifo_underrflow_thr	R/W	When set to 1, mutes ih_as_stat0[2] Value After Reset: 0x0
1	Aud_fifo_underrflow	R/W	When set to 1, mutes ih_as_stat0[1] Value After Reset: 0x0
0	Aud_fifo_overflow	R/W	When set to 1, mutes ih_as_stat0[0] Value After Reset: 0x0

ih_mute_phy_stat0

Description: PHY Interface Interrupt Mute Control Register

Size: 8 bits

Offset: 0x184

Bits	Name	Attr	Description
7:6			Reserved for future use.
5	RX_SENSE_3	R/W	When set to 1, mutes ih_phy_stat0[5] Value After Reset: 0x0
4	RX_SENSE_2	R/W	When set to 1, mutes ih_phy_stat0[4] Value After Reset: 0x0

Bits	Name	Attr	Description
3	RX_SENSE_1	R/W	When set to 1, mutes ih_phy_stat0[3] Value After Reset: 0x0
2	RX_SENSE_0	R/W	When set to 1, mutes ih_phy_stat0[2] Value After Reset: 0x0
1	TX_PHY_LOC_K	R/W	When set to 1, mutes ih_phy_stat0[1] Value After Reset: 0x0
0	HPD	R/W	When set to 1, mutes ih_phy_stat0[0] Value After Reset: 0x0

ih_mute_i2cm_stat0

Description: E-DDC I2C Master Interrupt Mute Control Register

Size: 8 bits

Offset: 0x185

Bits	Name	Attr	Description
7:3			Reserved for future use.
2	scdc_readreq	R/W	When set to 1, mutes ih_i2cm_stat0[2] Value After Reset: 0x1
1	I2Cmasterdone	R/W	When set to 1, mutes ih_i2cm_stat0[1] Value After Reset: 0x0
0	I2Cmastererror	R/W	When set to 1, mutes ih_i2cm_stat0[0] Value After Reset: 0x0

ih_mute_cec_stat0

Description: CEC Interrupt Mute Control Register

Size: 8 bits

Offset: 0x186

Bits	Name	Attr	Description
7			Reserved for future use.
6	WAKEUP	R/W	When set to 1, mutes ih_cec_stat0[6] Value After Reset: 0x0
5	ERROR_FOLL_OV	R/W	When set to 1, mutes ih_cec_stat0[5] Value After Reset: 0x0
4	ERROR_INIT_IATOR	R/W	When set to 1, mutes ih_cec_stat0[4] Value After Reset: 0x0
3	ARB_LOST	R/W	When set to 1, mutes ih_cec_stat0[3] Value After Reset: 0x0
2	NACK	R/W	When set to 1, mutes ih_cec_stat0[2] Value After Reset: 0x0
1	EOM	R/W	When set to 1, mutes ih_cec_stat0[1] Value After Reset: 0x0
0	DONE	R/W	When set to 1, mutes ih_cec_stat0[0] Value After Reset: 0x0

ih_mute_vp_stat0

Description: Video Packetizer Interrupt Mute Control Register

Size: 8 bits

Offset: 0x187

Bits	Name	Attr	Description
7	fifofullrepet	R/W	When set to 1, mutes ih_vp_stat0[7] Value After Reset: 0x0
6	fifoemptyrep	R/W	When set to 1, mutes ih_vp_stat0[6] Value After Reset: 0x0
5	fifofullpp	R/W	When set to 1, mutes ih_vp_stat0[5] Value After Reset: 0x0
4	fifoemptypp	R/W	When set to 1, mutes ih_vp_stat0[4]

Bits	Name	Attr	Description
			Value After Reset: 0x0
3	fifofullremap	R/W	When set to 1, mutes ih_vp_stat0[3] Value After Reset: 0x0
2	fifoemptyremap	R/W	When set to 1, mutes ih_vp_stat0[2] Value After Reset: 0x0
1	spare_2	R/W	Reserved as "spare" bit with no associated functionality. Value After Reset: 0x0
0	spare_1	R/W	Reserved as "spare" bit with no associated functionality. Value After Reset: 0x0

ih_mute_i2cmphy_stat0

Description: PHY GEN2 I2C Master Interrupt Mute Control Register

Size: 8 bits

Offset: 0x188

Bits	Name	Attr	Description
7:2			Reserved for future use.
1	I2Cmphydone	R/W	When set to 1, mutes ih_i2cmphy_stat0[1] Value After Reset: 0x0
0	I2Cmphyerror	R/W	When set to 1, mutes ih_i2cmphy_stat0[0] Value After Reset: 0x0

ih_mute_ahbdmaaud_stat0

Description: AHB Audio DMA Interrupt Mute Control Register

Size: 8 bits

Offset: 0x189

Bits	Name	Attr	Description
7			Reserved for future use.
6	ahbdmaaud_intbuffoverrun	R/W	When set to 1, mutes ih_ahbdmaaud_stat0[6] Value After Reset: 0x1
5	ahbdmaaud_interror	R/W	When set to 1, mutes ih_ahbdmaaud_stat0[5] Value After Reset: 0x0
4	ahbdmaaud_intlostownership	R/W	When set to 1, mutes ih_ahbdmaaud_stat0[4] Value After Reset: 0x0
3	ahbdmaaud_intretrysplit	R/W	When set to 1, mutes ih_ahbdmaaud_stat0[3] Value After Reset: 0x0
2	ahbdmaaud_intdone	R/W	When set to 1, mutes ih_ahbdmaaud_stat0[2] Value After Reset: 0x0
1	ahbdmaaud_intbufffull	R/W	When set to 1, mutes ih_ahbdmaaud_stat0[1] Value After Reset: 0x0
0	ahbdmaaud_intbuffempty	R/W	When set to 1, mutes ih_ahbdmaaud_stat0[0] Value After Reset: 0x0

ih_mute

Description: Global Interrupt Mute Control Register

Size: 8 bits

Offset: 0x1ff

Bits	Name	Attr	Description
7:2			Reserved for future use.
1	mute_wakeup_interrupt	R/W	When set to 1, mutes the main interrupt output port. The sticky bit interrupts continue with their state accessible through the configuration bus, only the main interrupt line

			is muted. Value After Reset: 0x1
0	mute_all_int_errupt	R/W	When set to 1, mutes the main interrupt line (where all interrupts are ORed). The sticky bit interrupts continue with their state; only the main interrupt line is muted. Value After Reset: 0x1

VideoSampler Registers

Video Sampler Registers. Follow the link for the register to see a detailed description of the register.

Registers for Address Block: VideoSampler

Register	Offset	Description
tx_invid0	0x200	Video Input Mapping and Internal Data Enable Configuration Register
tx_instuffing	0x201	Video Input Stuffing Enable Register
tx_gydata0	0x202	Video Input gy Data Channel Stuffing Register 0
tx_gydata1	0x203	Video Input gy Data Channel Stuffing Register 1
tx_rcrdata0	0x204	Video Input rcr Data Channel Stuffing Register 0
tx_rcrdata1	0x205	Video Input rcr Data Channel Stuffing Register 1
tx_bcbdata0	0x206	Video Input bcb Data Channel Stuffing Register 0
tx_bcbdata1	0x207	Video Input bcb Data Channel Stuffing Register 1

tx_invid0

Description: Video Input Mapping and Internal Data Enable Configuration Register

Size: 8 bits

Offset: 0x200

Bits	Name	Attr	Description
7	internal_de_generator	R/W	<p>Internal data enable (DE) generator enable. If data enable is not available for the input video, set this bit to one to activate the internal data enable generator.</p> <p>Attention: This feature only works for input video modes that have native repetition (such as, all CEA videos). No desired pixel repetition can be used with this feature because these configurations only affect the Frame Composer and not this block.</p> <p>The DE Generator does not work for the following conditions:</p> <ul style="list-style-type: none"> Transmission of video with CEA VIC 39 Transmission of 3D video using the field alternative structure <p>Value After Reset: 0x0</p>
6:5			Reserved for future use.
4:0	video_mapping	R/W	<p>Video Input mapping (color space/color depth): 0x01: RGB 4:4:4/8 bits 0x03: RGB 4:4:4/10 bits 0x05: RGB 4:4:4/12 bits 0x07: RGB 4:4:4/16 bits</p>

Bits	Name	Attr	Description
			0x09: YCbCr 4:4:4 or 4:2:0/8 bits 0x0B: YCbCr 4:4:4 or 4:2:0/10 bits 0x0D: YCbCr 4:4:4 or 4:2:0/12 bits 0x0F: YCbCr 4:4:4 or 4:2:0/16 bits 0x16: YCbCr 4:2:2/8 bits 0x14: YCbCr 4:2:2/10 bits 0x12: YCbCr 4:2:2/12 bits 0x17: YCbCr 4:4:4 (IPI)/8 bits 0x18: YCbCr 4:4:4 (IPI)/10 bits 0x19: YCbCr 4:4:4 (IPI)/12 bits 0x1A: YCbCr 4:4:4 (IPI)/16 bits 0x1B: YCbCr 4:2:2 (IPI)/12 bits 0x1C: YCbCr 4:2:0 (IPI)/8 bits 0x1D: YCbCr 4:2:0 (IPI)/10 bits 0x1E: YCbCr 4:2:0 (IPI)/12 bits 0x1F: YCbCr 4:2:0 (IPI)/16 bits Value After Reset: 0x1

tx_instuffing

Description: Video Input Stuffing Enable Register

Size: 8 bits

Offset: 0x201

Bits	Name	Attr	Description
7:3			Reserved for future use.
2	bcbdata_stuffing	R/W	0b: When the dataen signal is low, the value in the bcbdata[15:0] output is the one sampled from the corresponding input data. 1b: When the dataen signal is low, the value in the bcbdata[15:0] output is given by the values in the TX_BCBDTA0 and TX_BCBDATA1 registers. Value After Reset: 0x0
1	rcrdata_stuffing	R/W	0b: When the dataen signal is low, the value in the rcrdata[15:0] output is the one sampled from the corresponding input data. 1b: When the dataen signal is low, the value in the rcrdata[15:0] output is given by the values in TX_RCRDTA0 and TX_RCRDATA1 registers. Value After Reset: 0x0
0	gydata_stuffing	R/W	0b: When the dataen signal is low, the value in the gydata[15:0] output is the one sampled from the corresponding input data. 1b: When the dataen signal is low, the value in the gydata[15:0] output is given by the values in TX_GYDTA0 and TX_GYDATA1 registers. Value After Reset: 0x0

tx_gydata0

Description: Video Input gy Data Channel Stuffing Register 0

Size: 8 bits

Offset: 0x202

Bits	Name	Attr	Description
7:0	gydata	R/W	This register defines the value of gydata[7:0] when TX_INSTUFFING[0] (gydata_stuffing) is set to 1b. Value After Reset: 0x0

tx_gydata1

Description: Video Input gy Data Channel Stuffing Register 1

Size: 8 bits

Offset: 0x203

Bits	Name	Attr	Description
7:0	gydata	R/W	This register defines the value of gydata[15:8] when TX_INSTUFFING[0] (gydata_stuffing) is set to 1b. Value After Reset: 0x0

tx_rcrdata0

Description: Video Input rcr Data Channel Stuffing Register 0

Size: 8 bits

Offset: 0x204

Bits	Name	Attr	Description
7:0	rcrdata	R/W	This register defines the value of rcrydata[7:0] when TX_INSTUFFING[1] (rcrdata_stuffing) is set to 1b. Value After Reset: 0x0

tx_rcrdata1

Description: Video Input rcr Data Channel Stuffing Register 1

Size: 8 bits

Offset: 0x205

Bits	Name	Attr	Description
7:0	rcrdata	R/W	This register defines the value of rcrydata[15:8] when TX_INSTUFFING[1] (rcrdata_stuffing) is set to 1b. Value After Reset: 0x0

tx_bcbdata0

Description: Video Input bcb Data Channel Stuffing Register 0

Size: 8 bits

Offset: 0x206

Bits	Name	Attr	Description
7:0	bcbdata	R/W	This register defines the value of bcbdata[7:0] when TX_INSTUFFING[2] (bcbdata_stuffing) is set to 1b. Value After Reset: 0x0

tx_bcbdata1

Description: Video Input bcb Data Channel Stuffing Register 1

Size: 8 bits

Offset: 0x207

Bits	Name	Attr	Description
7:0	bcbdata	R/W	This register defines the value of bcbdata[15:8] when TX_INSTUFFING[2] (bcbdata_stuffing) is set to 1b. Value After Reset: 0x0

VideoPacketizer Registers

Video Packetizer Registers. Follow the link for the register to see a detailed description of the register.

Register	Offset	Description
vp_status	0x800	Video Packetizer Packing Phase Status Register
vp_pr_cd	0x801	Video Packetizer Pixel Repetition and Color Depth Register
vp_stuff	0x802	Video Packetizer Stuffing and Default Packing Phase Register

vp_remap	0x803	Video Packetizer YCC422 Remapping Register
vp_conf	0x804	Video Packetizer Output and Enable Configuration Register
vp_mask	0x807	Video Packetizer Interrupt Mask Register

vp_status

Description: Video Packetizer Packing Phase Status Register

Size: 8 bits

Offset: 0x800

Bits	Name	Attr	Description
7:4			Reserved for future use.
3:0	packing_phase	R	Read only register that holds the "packing phase" output of the Video Packetizer block. Value After Reset: 0x0

vp_pr_cd

Description: Video Packetizer Pixel Repetition and Color Depth Register

Size: 8 bits

Offset: 0x801

Bits	Name	Attr	Description
7:4	color_depth	R/W	The Color depth configuration is described as the following, with the action stated corresponding to color_depth[3:0]: 0000b: 24 bits per pixel video (8 bits per component). 8-bit packing mode. 0001b-0011b: Reserved. Not used. 0100b: 24 bits per pixel video (8 bits per component). 8-bit packing mode. 0101b: 30 bits per pixel video (10 bits per component). 10-bit packing mode. 0110b: 36 bits per pixel video (12 bits per component). 12-bit packing mode. 0111b: 48 bits per pixel video (16 bits per component). 16-bit packing mode. Other: Reserved. Not used. Value After Reset: 0x0
3:0	desired_pr_factor	R/W	Desired pixel repetition factor configuration. The configured value sets H13T PHY PLL to multiply pixel clock by the factor in order to obtain the desired repetition clock. For the CEA modes some are already defined with pixel repetition in the input video. So for CEA modes this shall be always 0. Shall only be used if the user wants to do pixel repetition using H13TCTRL controller. The action is stated corresponding to desired_pr_factor[3:0]: 0000b: No pixel repetition (pixel sent only once) 0001b: Pixel sent two times (pixel repeated once) 0010b: Pixel sent three times 0011b: Pixel sent four times 0100b: Pixel sent five times 0101b: Pixel sent six times 0110b: Pixel sent seven times 0111b: Pixel sent eight times 1000b: Pixel sent nine times 1001b: Pixel sent 10 times Other: Reserved. Not used Value After Reset: 0x0

vp_stuff

Description: Video Packetizer Stuffing and Default Packing Phase Register

Size: 8 bits

Offset: 0x802

Bit S	Name	Attr	Description
7:6			Reserved for future use.
5	idefault_phase	R/W	Controls the default phase packing machine used according to HDMI 1.4b specification: "If the transmitted video format has timing such that the phase of the first pixel of every Video Data Period corresponds to pixel packing phase 0 (e.g. 10P0, 12P0, 16P0), the Source may set the Default_Phase bit in the GCP. The Sink may use this bit to optimize its filtering or handling of the PP field." This means that for 10-bit mode the Htotal must be dividable by 4; for 12-bit mode, the Htotal must be divisible by 2. Value After Reset: 0x0
4	ifix_pp_to_lastr	R/W	Reserved. Controls packing machine strategy Value After Reset: 0x0
3	icx_goto_p0_st	R/W	Reserved. Controls packing machine strategy Value After Reset: 0x0
2	ycc422_stuffing	R/W	YCC 422 remap stuffing control. For horizontal blanking, the action is stated corresponding to ycc422_stuffing: 0b: YCC 422 remap block in direct mode (input blanking data goes directly to output). 1b: YCC 422 remap block in stuffing mode. When "de" goes to low the outputs are fixed to 0x00. Value After Reset: 0x0
1	pp_stuffing	R/W	Pixel packing stuffing control. The action is stated corresponding to pp_stuffing: 0b: Pixel packing block in direct mode (input blanking data goes directly to output). 1b: Pixel packing block in stuffing mode. When "de_rep" goes to low the outputs are fixed to 0x00. Value After Reset: 0x0

Fields for Register: vp_stuff (Continued)

Bit S	Name	Attr	Description
0	pr_stuffing	R/W	Pixel repeater stuffing control. The action is stated corresponding to pp_stuffing: 0b: Pixel repeater block in direct mode (input blanking data goes directly to output). 1b: Pixel repeater block in stuffing mode. When "de" goes to low the outputs are fixed to 0x00. Value After Reset: 0x0

vp_remap

Description: Video Packetizer YCC422 Remapping Register

Size: 8 bits

Offset: 0x803

Bits	Name	Attr	Description
7:2			Reserved for future use.
1:0	ycc422_size	R/W	YCC 422 remap input video size ycc422_size[1:0] 00b: YCC 422 16-bit input video (8 bits per component) 01b: YCC 422 20-bit input video (10 bits per component) 10b: YCC 422 24-bit input video (12 bits per component) 11b: Reserved. Not used Value After Reset: 0x0

vp_conf

Description: Video Packetizer Output and Enable Configuration Register

Size: 8 bits

Offset: 0x804

Bits	Name	Attr	Description
7			Reserved for future use.
6	bypass_en	R/W	When set to 1'b1, Pixel packing enable. When set to 1b'0, the pixel packing block is controlled by pp_en. Value After Reset: 0x0
5	pp_en	R/W	Pixel packing enable. When set to 0, the pixel packing block is disabled if bypass_en is 1'b0. Value After Reset: 0x1
4	pr_en	R/W	Pixel repeater enable. When set to 0, the pixel repetition block is disabled. Value After Reset: 0x0
3	ycc422_en	R/W	YCC 422 select enable. Disabling forces bypass module to output always zeros. Value After Reset: 0x0
2	bypass_select	R/W	bypass_select 0b: Data from pixel repeater block 1b: Data from input of Video Packetizer block Value After Reset: 0x1
1	output_select	R/W	When set to 1'b1, Data from pixel packing block. Value After Reset: 0x0
0	output_select_0	R/W	Video Packetizer output selection 0b: Data from pixel packing block 1b: Data from YCC422 remap block Value After Reset: 0x0

vp_mask

Description: Video Packetizer Interrupt Mask Register

Size: 8 bits

Offset: 0x807

Bits	Name	Attr	Description
7	ointfullrep	R/W	Mask bit for Video Packetizer pixel repeater FIFO full Value After Reset: 0x0
6	ointemptyrep	R/W	Mask bit for Video Packetizer pixel repeater FIFO empty Value After Reset: 0x0
5	ointfullpp	R/W	Mask bit for Video Packetizer pixel packing FIFO full Value After Reset: 0x0

4	ointemptypp	R/W	Mask bit for Video Packetizer pixel packing FIFO empty Value After Reset: 0x0
3	ointfullremap	R/W	Mask bit for Video Packetizer pixel YCC 422 re-mapper FIFO full Value After Reset: 0x0
2	ointemptyremap	R/W	Mask bit for Video Packetizer pixel YCC 422 re-mapper FIFO empty Value After Reset: 0x0
1	spare_2	R/W	Reserved as "spare" bit with no associated functionality. Value After Reset: 0x0
0	spare_1	R/W	Reserved as "spare" bit with no associated functionality. Value After Reset: 0x0

FrameComposer Registers

Frame Composer Registers. Follow the link for the register to see a detailed description of the register.

Registers for Address Block: FrameComposer

Register	Offset	Description
fc_invidconf	0x1000	Frame Composer Input Video Configuration and HDCP Keepout Register
fc_inhactiv0	0x1001	Frame Composer Input Video HActive Pixels Register 0
fc_inhactiv1	0x1002	Frame Composer Input Video HActive Pixels Register 1
fc_inhblank0	0x1003	Frame Composer Input Video HBlank Pixels Register 0
fc_inhblank1	0x1004	Frame Composer Input Video HBlank Pixels Register 1
fc_invactiv0	0x1005	Frame Composer Input Video VActive Pixels Register 0
fc_invactiv1	0x1006	Frame Composer Input Video VActive Pixels Register 1
fc_invblank	0x1007	Frame Composer Input Video VBlank Pixels Register
fc_hsyncindelay0	0x1008	Frame Composer Input Video HSync Front Porch Register 0
fc_hsyncindelay1	0x1009	Frame Composer Input Video HSync Front Porch Register 1
fc_hsyncinwidth0	0x100a	Frame Composer Input Video HSync Width Register 0
fc_hsyncinwidth1	0x100b	Frame Composer Input Video HSync Width Register 1
fc_vsyncindelay	0x100c	Frame Composer Input Video VSync Front Porch Register
fc_vsyncinwidth	0x100d	Frame Composer Input Video VSync Width Register
fc_infreq0	0x100e	Frame Composer Input Video Refresh Rate Register 0
fc_infreq1	0x100f	Frame Composer Input Video Refresh Rate Register 1
fc_infreq2	0x1010	Frame Composer Input Video Refresh Rate Register 2
fc_ctrldur	0x1011	Frame Composer Control Period Duration Register
fc_exctrldur	0x1012	Frame Composer Extended Control Period Duration Register
fc_exctrlspac	0x1013	Frame Composer Extended Control Period Maximum Spacing Register
fc_ch0pream	0x1014	Frame Composer Channel 0 Non-Preamble Data Register
fc_ch1pream	0x1015	Frame Composer Channel 1 Non-Preamble Data Register
fc_ch2pream	0x1016	Frame Composer Channel 2 Non-Preamble Data Register
fc_aviconf3	0x1017	Frame Composer AVI Packet Configuration Register 3
fc_gcp	0x1018	Frame Composer GCP Packet Configuration Register
fc_aviconf0	0x1019	Frame Composer AVI Packet Configuration Register 0

fc_aviconf1	0x101a	Frame Composer AVI Packet Configuration Register 1
Registers for Address Block: FrameComposer (Continued)		
Register	Offset	Description
fc_aviconf2	0x101b	Frame Composer AVI Packet Configuration Register 2
fc_avivid	0x101c	Frame Composer AVI Packet VIC Register
fc_avietb[0:1]	0x101d + (i * 0x1)	Frame Composer AVI Packet End of Top Bar Register Array
fc_avisbb[0:1]	0x101f + (i * 0x1)	Frame Composer AVI Packet Start of Bottom Bar Register Array
fc_avielb[0:1]	0x1021 + (i * 0x1)	Frame Composer AVI Packet End of Left Bar Register Array
fc_avisrb[0:1]	0x1023 + (i * 0x1)	Frame Composer AVI Packet Start of Right Bar Register Array
fc_audiconf0	0x1025	Frame Composer AUD Packet Configuration Register 0
fc_audiconf1	0x1026	Frame Composer AUD Packet Configuration Register 1
fc_audiconf2	0x1027	Frame Composer AUD Packet Configuration Register 2
fc_audiconf3	0x1028	Frame Composer AUD Packet Configuration Register 3
fc_vsdieeeid2	0x1029	Frame Composer VSI Packet Data IEEE Register 2
fc_vsdsiz	0x102a	Frame Composer VSI Packet Data Size Register
fc_vsdieeeid1	0x1030	Frame Composer VSI Packet Data IEEE Register 1
fc_vsdieeeid0	0x1031	Frame Composer VSI Packet Data IEEE Register 0
fc_vsdpayload[0:23]	0x1032 + (i * 0x1)	Frame Composer VSI Packet Data Payload Register Array
fc_spdvendorname[0:7]	0x104a + (i * 0x1)	Frame Composer SPD Packet Data Vendor Name Register Array
fc_spdproductname[0:15]	0x1052 + (i * 0x1)	Frame Composer SPD packet Data Product Name Register Array
fc_spddeviceinf	0x1062	Frame Composer SPD Packet Data Source Product Descriptor Register
fc_audsconf	0x1063	Frame Composer Audio Sample Flat and Layout Configuration Register
fc_audsstat	0x1064	Frame Composer Audio Sample Flat and Layout Status Register
fc_audsval	0x1065	Frame Composer Audio Sample Validity Flag Register
fc_audsuser	0x1066	Frame Composer Audio Sample User Flag Register
fc_audschnl0	0x1067	Frame Composer Audio Sample Channel Status Configuration Register 0
fc_audschnl1	0x1068	Frame Composer Audio Sample Channel Status Configuration Register 1

Registers for Address Block: FrameComposer (Continued)

Register	Offset	Description
fc_audschnl2	0x1069	Frame Composer Audio Sample Channel Status Configuration Register 2
fc_audschnl3	0x106a	Frame Composer Audio Sample Channel Status Configuration Register 3
fc_audschnl4	0x106b	Frame Composer Audio Sample Channel Status Configuration Register 4
fc_audschnl5	0x106c	Frame Composer Audio Sample Channel Status Configuration Register 5
fc_audschnl6	0x106d	Frame Composer Audio Sample Channel Status

Register	Offset	Description
		Configuration Register 6
fc_audschnl7	0x106e	Frame Composer Audio Sample Channel Status Configuration Register 7
fc_audschnl8	0x106f	Frame Composer Audio Sample Channel Status Configuration Register 8
fc_ctrlqhigh	0x1073	Frame Composer Number of High Priority Packets Attended Configuration Register
fc_ctrlqlow	0x1074	Frame Composer Number of Low Priority Packets Attended Configuration Register
fc_acp0	0x1075	Frame Composer ACP Packet Type Configuration Register 0
fc_acp16	0x1082	Frame Composer ACP Packet Body Configuration Register 16
fc_acp15	0x1083	Frame Composer ACP Packet Body Configuration Register 15
fc_acp14	0x1084	Frame Composer ACP Packet Body Configuration Register 14
fc_acp13	0x1085	Frame Composer ACP Packet Body Configuration Register 13
fc_acp12	0x1086	Frame Composer ACP Packet Body Configuration Register 12
fc_acp11	0x1087	Frame Composer ACP Packet Body Configuration Register 11
fc_acp10	0x1088	Frame Composer ACP Packet Body Configuration Register 10
fc_acp9	0x1089	Frame Composer ACP Packet Body Configuration Register 9
fc_acp8	0x108a	Frame Composer ACP Packet Body Configuration Register 8
fc_acp7	0x108b	Frame Composer ACP Packet Body Configuration Register 7
fc_acp6	0x108c	Frame Composer ACP Packet Body Configuration Register 6

Registers for Address Block: FrameComposer (Continued)

Register	Offset	Description
fc_acp5	0x108d	Frame Composer ACP Packet Body Configuration Register 5
fc_acp4	0x108e	Frame Composer ACP Packet Body Configuration Register 4
fc_acp3	0x108f	Frame Composer ACP Packet Body Configuration Register 3
fc_acp2	0x1090	Frame Composer ACP Packet Body Configuration Register 2
fc_acp1	0x1091	Frame Composer ACP Packet Body Configuration Register 1
fc_iscr1_0	0x1092	Frame Composer ISRC1 Packet Status, Valid, and Continue Configuration Register
fc_iscr1_16	0x1093	Frame Composer ISRC1 Packet Body Register 16
fc_iscr1_15	0x1094	Frame Composer ISRC1 Packet Body Register 15
fc_iscr1_14	0x1095	Frame Composer ISRC1 Packet Body Register 14
fc_iscr1_13	0x1096	Frame Composer ISRC1 Packet Body Register 13
fc_iscr1_12	0x1097	Frame Composer ISRC1 Packet Body Register 12
fc_iscr1_11	0x1098	Frame Composer ISRC1 Packet Body Register 11
fc_iscr1_10	0x1099	Frame Composer ISRC1 Packet Body Register 10
fc_iscr1_9	0x109a	Frame Composer ISRC1 Packet Body Register 9

Register	Offset	Description
fc_iscr1_8	0x109b	Frame Composer ISRC1 Packet Body Register 8
fc_iscr1_7	0x109c	Frame Composer ISRC1 Packet Body Register 7
fc_iscr1_6	0x109d	Frame Composer ISRC1 Packet Body Register 6
fc_iscr1_5	0x109e	Frame Composer ISRC1 Packet Body Register 5
fc_iscr1_4	0x109f	Frame Composer ISRC1 Packet Body Register 4
fc_iscr1_3	0x10a0	Frame Composer ISRC1 Packet Body Register 3
fc_iscr1_2	0x10a1	Frame Composer ISRC1 Packet Body Register 2
fc_iscr1_1	0x10a2	Frame Composer ISRC1 Packet Body Register 1
fc_iscr2_15	0x10a3	Frame Composer ISRC2 Packet Body Register 15
fc_iscr2_14	0x10a4	Frame Composer ISRC2 Packet Body Register 14
fc_iscr2_13	0x10a5	Frame Composer ISRC2 Packet Body Register 13
fc_iscr2_12	0x10a6	Frame Composer ISRC2 Packet Body Register 12
fc_iscr2_11	0x10a7	Frame Composer ISRC2 Packet Body Register 11
fc_iscr2_10	0x10a8	Frame Composer ISRC2 Packet Body Register 10
fc_iscr2_9	0x10a9	Frame Composer ISRC2 Packet Body Register 9
fc_iscr2_8	0x10aa	Frame Composer ISRC2 Packet Body Register 8
fc_iscr2_7	0x10ab	Frame Composer ISRC2 Packet Body Register 7

Registers for Address Block: FrameComposer (Continued)

Register	Offset	Description
fc_iscr2_6	0x10ac	Frame Composer ISRC2 Packet Body Register 6
fc_iscr2_5	0x10ad	Frame Composer ISRC2 Packet Body Register 5
fc_iscr2_4	0x10ae	Frame Composer ISRC2 Packet Body Register 4
fc_iscr2_3	0x10af	Frame Composer ISRC2 Packet Body Register 3
fc_iscr2_2	0x10b0	Frame Composer ISRC2 Packet Body Register 2
fc_iscr2_1	0x10b1	Frame Composer ISRC2 Packet Body Register 1
fc_iscr2_0	0x10b2	Frame Composer ISRC2 Packet Body Register 0
fc_datauto0	0x10b3	Frame Composer Data Island Auto Packet Scheduling Register 0 Configures the Frame Composer RDRB(1)/ Manual(0)...
fc_datauto1	0x10b4	Frame Composer Data Island Auto Packet Scheduling Register 1 Configures the Frame Composer (FC)...
fc_datauto2	0x10b5	Frame Composer Data Island Auto packet scheduling Register 2 Configures the Frame Composer (FC)...
fc_datman	0x10b6	Frame Composer Data Island Manual Packet Request Register Requests to the Frame Composer the data...
fc_datauto3	0x10b7	Frame Composer Data Island Auto Packet Scheduling Register 3 Configures the Frame Composer Automatic(1)/ RDRB(0)...
fc_rdrb0	0x10b8	Frame Composer Round Robin ACR Packet Insertion Register 0 Configures the Frame Composer (FC) RDRB...
fc_rdrb1	0x10b9	Frame Composer Round Robin ACR Packet Insertion Register 1 Configures the Frame Composer (FC) RDRB...
fc_rdrb2	0x10ba	Frame Composer Round Robin AUDI Packet

Register	Offset	Description
	a	Insertion Register 2 Configures the Frame Composer (FC)...
fc_rdrb3	0x10b b	Frame Composer Round Robin AUDI Packet Insertion Register 3 Configures the Frame Composer (FC)...
fc_rdrb4	0x10bc	Frame Composer Round Robin GCP Packet Insertion Register 4 Configures the Frame Composer (FC) RDRB...
fc_rdrb5	0x10b d	Frame Composer Round Robin GCP Packet Insertion Register 5 Configures the Frame Composer (FC) RDRB...
fc_rdrb6	0x10b e	Frame Composer Round Robin AVI Packet Insertion Register 6 Configures the Frame Composer (FC) RDRB...
fc_rdrb7	0x10bf	Frame Composer Round Robin AVI Packet Insertion Register 7 Configures the Frame Composer (FC) RDRB...

Registers for Address Block: FrameComposer (Continued)

Register	Offset	Description
fc_mask0	0x10d 2	Frame Composer Packet Interrupt Mask Register 0
fc_mask1	0x10d 6	Frame Composer Packet Interrupt Mask Register 1
fc_mask2	0x10d a	Frame Composer High/Low Priority Overflow Interrupt Mask Register 2
fc_prconf	0x10e 0	Frame Composer Pixel Repetition Configuration Register
fc_scrambler_ctrl	0x10e 1	Frame Composer Scrambler Control
fc_gmd_stat	0x110 0	Frame Composer GMD Packet Status Register Gamut metadata packet status bit information for no_current_gmd,...
fc_gmd_en	0x110 1	Frame Composer GMD Packet Enable Register This register enables Gamut metadata (GMD) packet transmission....
fc_gmd_up	0x110 2	Frame Composer GMD Packet Update Register This register performs an GMD packet content update according...
fc_gmd_conf	0x110 3	Frame Composer GMD Packet Schedule Configuration Register This register configures the number of...
fc_gmd_hb	0x110 4	Frame Composer GMD Packet Profile and Gamut Sequence Configuration Register This register configures...
fc_gmd_pb[0:27]	0x110 5 + (i * 0x1)	Frame Composer GMD Packet Body Register Array Configures the GMD packet body of the GMD...

Registers for Address Block: FrameComposer (Continued)

Register	Offset	Description
fc_dbgforce	0x120 0	Frame Composer video/audio Force Enable Register This register allows to force the controller to...
fc_dbgaud0ch0	0x120	Frame Composer Audio Data Channel 0

Register	Offset	Description
	1	Register 0 Configures the audio fixed data to be used in channel...
fc_dbgaud1ch0	0x1202	Frame Composer Audio Data Channel 0 Register 1 Configures the audio fixed data to be used in channel...
fc_dbgaud2ch0	0x1203	Frame Composer Audio Data Channel 0 Register 2 Configures the audio fixed data to be used in channel...
fc_dbgaud0ch1	0x1204	Frame Composer Audio Data Channel 1 Register 0 Configures the audio fixed data to be used in channel...
fc_dbgaud1ch1	0x1205	Frame Composer Audio Data Channel 1 Register 1 Configures the audio fixed data to be used in channel...
fc_dbgaud2ch1	0x1206	Frame Composer Audio Data Channel 1 Register 2 Configures the audio fixed data to be used in channel...
fc_dbgaud0ch2	0x1207	Frame Composer Audio Data Channel 2 Register 0 Configures the audio fixed data to be used in channel...
fc_dbgaud1ch2	0x1208	Frame Composer Audio Data Channel 2 Register 1 Configures the audio fixed data to be used in channel...
fc_dbgaud2ch2	0x1209	Frame Composer Audio Data Channel 2 Register 2 Configures the audio fixed data to be used in channel...
fc_dbgaud0ch3	0x120a	Frame Composer Audio Data Channel 3 Register 0 Configures the audio fixed data to be used in channel...
fc_dbgaud1ch3	0x120b	Frame Composer Audio Data Channel 3 Register 1 Configures the audio fixed data to be used in channel...
fc_dbgaud2ch3	0x120c	Frame Composer Audio Data Channel 3 Register 2 Configures the audio fixed data to be used in channel...

Registers for Address Block: FrameComposer (Continued)

Register	Offset	Description
fc_dbgaud0ch4	0x120d	Frame Composer Audio Data Channel 4 Register 0 Configures the audio fixed data to be used in channel...
fc_dbgaud1ch4	0x120e	Frame Composer Audio Data Channel 4 Register 1 Configures the audio fixed data to be used in channel...
fc_dbgaud2ch4	0x120f	Frame Composer Audio Data Channel 4 Register 2 Configures the audio fixed data to be used in channel...
fc_dbgaud0ch5	0x1210	Frame Composer Audio Data Channel 5 Register 0 Configures the audio fixed data to be used in channel...
fc_dbgaud1ch5	0x1211	Frame Composer Audio Data Channel 5 Register 1 Configures the audio fixed data to be used in channel...
fc_dbgaud2ch5	0x1212	Frame Composer Audio Data Channel 5 Register 2 Configures the audio fixed data to be used in channel...
fc_dbgaud0ch6	0x1213	Frame Composer Audio Data Channel 6 Register 0 Configures the audio fixed data to be used in channel...
fc_dbgaud1ch6	0x1214	Frame Composer Audio Data Channel 6 Register 1 Configures the audio fixed data to be used in channel...
fc_dbgaud2ch6	0x1215	Frame Composer Audio Data Channel 6 Register 2 Configures the audio fixed data to be used in channel...

Register	Offset	Description
fc_dbgaud0ch7	0x1216	Frame Composer Audio Data Channel 7 Register 0 Configures the audio fixed data to be used in channel...
fc_dbgaud1ch7	0x1217	Frame Composer Audio Data Channel 7 Register 1 Configures the audio fixed data to be used in channel...
fc_dbgaud2ch7	0x1218	Frame Composer Audio Data Channel 7 Register 2 Configures the audio fixed data to be used in channel...
fc_dbgtmds[0:2]	0x1219 + (i * 0x1)	Frame Composer TMDS Data Channel Register Array Configures the video fixed data to be used in TMDS...

fc_invidconf

Description: Frame Composer Input Video Configuration and HDCP Keepout Register

Size: 8 bits

Offset: 0x1000

Bits	Name	Attr	Description
7	HDCP_keep_out	R/W	Start/stop HDCP keepout window generation 1b: Active Value After Reset: 0x0
6	vsync_in_polarity	R/W	Vsync input polarity 1b: Active high 0b: Active low Value After Reset: 0x1
5	hsync_in_polarity	R/W	Hsync input polarity 1b: Active high 0b: Active low Value After Reset: 0x1
4	de_in_polarity	R/W	Data enable input polarity 1b: Active high 0b: Active low Value After Reset: 0x1
3	DVI_modez	R/W	Active low 0b: DVI mode selected 1b: HDMI mode selected Value After Reset: 0x0
2			Reserved for future use.
1	r_v_blank_in_osc	R/W	Used for CEA861-D modes with fractional Vblank (for example, modes 5, 6, 7, 10, 11, 20, 21, and 22). For more modes, see the CEA861-D specification. Note: Set this field to 1 for video mode 39, although there is no Vblank oscillation. 1b: Active high Value After Reset: 0x0

Fields for Register: fc_invidconf (Continued)

Bits	Name	Attr	Description
0	in_I_P	R/W	Input video mode: 1b: Interlaced 0b: Progressive Value After Reset: 0x0

fc_inhactiv0

Description: Frame Composer Input Video HActive Pixels Register 0

Size: 8 bits

Offset: 0x1001

Bits	Name	Attr	Description
7:0	H_in_activ	R/W	Input video Horizontal active pixel region width. Number of Horizontal active pixels [0...8191]. Value After Reset: 0x0

fc_inhactiv1

Description: Frame Composer Input Video HActive Pixels Register 1

Size: 8 bits

Offset: 0x1002

Bits	Name	Attr	Description
7:6			Reserved for future use.
5	H_in_activ_13	R/W	Input video Horizontal active pixel region width (0 .. 16383) If the configuration parameter HDMI_TX_20 = True (1), this bit field holds bit 13. Value After Reset: 0x0

Fields for Register: fc_inhactiv1 (Continued)

Bits	Name	Attr	Description
4	H_in_activ_12	R/W	Input video Horizontal active pixel region width (0 .. 8191) If configuration parameter HDMI_TX_14 = True (1), this bit field holds bit 12. Value After Reset: 0x0
3:0	H_in_activ	R/W	Input video Horizontal active pixel region width Value After Reset: 0x0

fc_inhblank0

Description: Frame Composer Input Video HBlank Pixels Register 0

Size: 8 bits

Offset: 0x1003

Bits	Name	Attr	Description
7:0	H_in_blank	R/W	Input video Horizontal blanking pixel region width. Number of Horizontal blanking pixels [0...4095]. Value After Reset: 0x0

fc_inhblank1

Description: Frame Composer Input Video HBlank Pixels Register 1

Size: 8 bits

Offset: 0x1004

Bits	Name	Attr	Description
7:5			Reserved for future use.
4:2	H_in_blank_12	R/W	Input video Horizontal blanking pixel region width If configuration parameter HDMI_TX_14 = True (1), this bit field holds bit 12:10 of number of horizontal blanking pixels. Value After Reset: 0x0
1:0	H_in_blank	R/W	Input video Horizontal blanking pixel region width this bit field holds bits 9:8 of number of Horizontal blanking pixels. Value After Reset: 0x0

fc_invactiv0

Description: Frame Composer Input Video VActive Pixels Register 0

Size: 8 bits

Offset: 0x1005

Bits	Name	Attr	Description
7:0	V_in_activ	R/W	Input video Vertical active pixel region width. This bit field holds bits 7:0 of number of Vertical active pixels. Value After Reset: 0x0

fc_invactiv1

Description: Frame Composer Input Video VActive Pixels Register 1

Size: 8 bits

Offset: 0x1006

Bits	Name	Attr	Description
7:5			Reserved for future use.
4:3	V_in_activ_12_11	R/W	Input video Vertical active pixel region width. If the configuration parameter HDMI_TX_14 = True (1), this bit field holds bits 12:10 of number of Vertical active pixels. Value After Reset: 0x0
2:0	V_in_activ	R/W	Input video Vertical active pixel region width. This bit field holds bits 9:8 of number of Vertical active pixels. Value After Reset: 0x0

fc_invblank

Description: Frame Composer Input Video VBlank Pixels Register

Size: 8 bits

Offset: 0x1007

Bits	Name	Attr	Description
7:0	V_in_blank	R/W	Input video Vertical blanking pixel region width. Number of Vertical blanking lines [0...255]. Value After Reset: 0x0

fc_hsyncindelay0

Description: Frame Composer Input Video HSync Front Porch Register 0

Size: 8 bits

Offset: 0x1008

Bits	Name	Attr	Description
7:0	H_in_delay	R/W	Input video Hsync active edge delay. Integer number of pixel clock cycles from "de" non active edge of the last "de" valid period [0...4095]. Value After Reset: 0x0

fc_hsyncindelay1

Description: Frame Composer Input Video HSync Front Porch Register 1

Size: 8 bits

Offset: 0x1009

Bits	Name	Attr	Description
7:5			Reserved for future use.
4:3	H_in_delay_12	R/W	Input video Horizontal active edge delay. If configuration parameter HDMI_TX_14 = True (1), this bit field holds bit 12. Integer number of pixel clock cycles from "de" non-active edge of the last "de" valid period [0...8191]. Value After Reset: 0x0
2:0	H_in_delay	R/W	Input video Horizontal active edge delay. Value After Reset: 0x0

fc_hsyncinwidth0

Description: Frame Composer Input Video HSync Width Register 0

Size: 8 bits

Offset: 0x100a

Bits	Name	Attr	Description
7:0	H_in_width	R/W	Input video Hsync active pulse width. Integer

Bits	Name	Attr	Description
			number of pixel clock cycles [0...511]. Value After Reset: 0x0

fc_hsyncinwidth1

Description: Frame Composer Input Video HSync Width Register 1

Size: 8 bits

Offset: 0x100b

Bits	Name	Attr	Description
7:2			Reserved for future use.
1	H_in_width_9	R/W	Input video Hsync active pulse width. If configuration parameter HDMI_TX_14 = True (1), then this bit field holds bit 9. Number of Horizontal active pixels [0...1024]. Value After Reset: 0x0
0	H_in_width	R/W	Input video Hsync active pulse width. Value After Reset: 0x0

fc_vsyncindelay

Description: Frame Composer Input Video VSync Front Porch Register

Size: 8 bits

Offset: 0x100c

Bits	Name	Attr	Description
7:0	V_in_delay	R/W	Input video Vsync active edge delay. Integer number of Hsync pulses from "de" non active edge of the last "de" valid period. [0...255]. Value After Reset: 0x0

fc_vsyncinwidth

Description: Frame Composer Input Video VSync Width Register

Size: 8 bits

Offset: 0x100d

Bits	Name	Attr	Description
7:6			Reserved for future use.
5:0	V_in_width	R/W	Description: Input video Vsync active pulse width. Integer number of video lines [0...63]. Value After Reset: 0x0

fc_infreq0

Description: Frame Composer Input Video Refresh Rate Register 0

Size: 8 bits

Offset: 0x100e

Bits	Name	Attr	Description
7:0	infreq	R/W	Video refresh rate in Hz*1E3 format. This register is provided for debug and informative purposes. The Hdmi_tx does not write any data to this register; the data written by software is not used by the Hdmi_tx. Value After Reset: 0x0

fc_infreq1

Description: Frame Composer Input Video Refresh Rate Register 1

Size: 8 bits

Offset: 0x100f

Bits	Name	Attr	Description

Bits	Name	Attr	Description
7:0	infreq	R/W	<p>Video refresh rate in Hz*1E3 format. This register is provided for debug and informative purposes.</p> <p>The Hdmi_tx does not write any data to this register; the data written by software is not used by the Hdmi_tx.</p> <p>Value After Reset: 0x0</p>

fc_infreq2

Description: Frame Composer Input Video Refresh Rate Register 2

Size: 8 bits

Offset: 0x1010

Bits	Name	Attr	Description
7:4			Reserved for future use.
3:0	infreq	R/W	<p>Video refresh rate in Hz*1E3 format. This register is provided for debug and informative purposes.</p> <p>The Hdmi_tx does not write any data to this register; the data written by software is not used by the Hdmi_tx.</p> <p>Value After Reset: 0x0</p>

fc_ctrlldur

Description: Frame Composer Control Period Duration Register

Size: 8 bits

Offset: 0x1011

Bits	Name	Attr	Description
7:0	ctrlperiodduration	R/W	<p>Configuration of the control period minimum duration (minimum of 12 pixel clock cycles; refer to HDMI 1.4b specification). Integer number of pixel clocks cycles [0..223].</p> <p>Value After Reset: 0x0</p>

fc_exctrlldur

Description: Frame Composer Extended Control Period Duration Register

Size: 8 bits

Offset: 0x1012

Bits	Name	Attr	Description
7:0	exctrlperiodduration	R/W	<p>Configuration of the extended control period minimum duration (minimum of 32 pixel clock cycles; refer to HDMI 1.4b specification). Integer number of pixel clocks cycles [0..223].</p> <p>Value After Reset: 0x0</p>

fc_exctrlspac

Description: Frame Composer Extended Control Period Maximum Spacing Register

Size: 8 bits

Offset: 0x1013

Bits	Name	Attr	Description
7:0	exctrlperiodspacing	R/W	<p>Configuration of the maximum spacing between consecutive extended control periods (maximum of 50ms; refer to the applicable HDMI specification).</p> <p>When using the HDMI 2.0 supported features (HDMI_TX_20 = 1):</p>

Bits	Name	Attr	Description
			generated spacing = (1/freq tmds clock)*256*512*(extctrlperiodspacing +1) else generated spacing = (1/freq tmds clock)*256*256*(extctrlperiodspacing +1) Value After Reset: 0x0

fc_ch0pream

Description: Frame Composer Channel 0 Non-Preamble Data Register

Size: 8 bits

Offset: 0x1014

Bits	Name	Attr	Description
7:0	ch0_preamble_filter	R/W	When in control mode, configures 8 bits that fill the channel 0 data lines not used to transmit the preamble (for more clarification, refer to the HDMI 1.4b specification). Value After Reset: 0x0

fc_ch1pream

Description: Frame Composer Channel 1 Non-Preamble Data Register

Size: 8 bits

Offset: 0x1015

Bits	Name	Attr	Description
7:6			Reserved for future use.
5:0	ch1_preamble_filter	R/W	When in control mode, configures 6 bits that fill the channel 1 data lines not used to transmit the preamble (for more clarification, refer to the HDMI 1.4b specification). Value After Reset: 0x0

fc_ch2pream

Description: Frame Composer Channel 2 Non-Preamble Data Register

Size: 8 bits

Offset: 0x1016

Bits	Name	Attr	Description
7:6			Reserved for future use.
5:0	ch2_preamble_filter	R/W	When in control mode, configures 6 bits that fill the channel 2 data lines not used to transmit the preamble (for more clarification, refer to the HDMI 1.4b specification). Value After Reset: 0x0

fc_aviconf3

Description: Frame Composer AVI Packet Configuration Register 3

Size: 8 bits

Offset: 0x1017

Bits	Name	Attr	Description
7:4			Reserved for future use.
3:2	YQ	R/W	YCC Quantization range according to the CEA specification Value After Reset: 0x0
1:0	CN	R/W	IT content type according to CEA the specification Value After Reset: 0x0

fc_gcp

Description: Frame Composer GCP Packet Configuration Register

Size: 8 bits

Offset: 0x1018

Bits	Name	Attr	Description
7:3			Reserved for future use.
2	default_phase	R/W	Value of "default_phase" in the GCP packet. This data must be equal to the default phase used at Video Packetizer packing machine. Value After Reset: 0x0
1	set_avmute	R/W	Value of "set_avmute" in the GCP packet Once the AVmute is set, the frame composer schedules the GCP packet with AVmute set in the packet scheduler to be sent once (may only be transmitted between the active edge of VSYNC and 384 pixels following this edge). Value After Reset: 0x0
0	clear_avmute	R/W	Value of "clear_avmute" in the GCP packet Value After Reset: 0x0

fc_aviconf0

Description: Frame Composer AVI Packet Configuration Register 0

Size: 8 bits

Offset: 0x1019

Bits	Name	Attr	Description
7	rgc_ycc_indication_2	R/W	Y2, Bit 2 of rgc_ycc_indication Value After Reset: 0x0
6	active_format_present	R/W	Active format present Value After Reset: 0x0
5:4	scan_information	R/W	Scan information Value After Reset: 0x0
3:2	bar_information	R/W	Bar information data valid Value After Reset: 0x0
1:0	rgc_ycc_indication	R/W	Y1,Y0 RGB or YCC indicator Value After Reset: 0x0

fc_aviconf1

Description: Frame Composer AVI Packet Configuration Register 1

Size: 8 bits

Offset: 0x101a

Bits	Name	Attr	Description
7:6	Colorimetry	R/W	Colorimetry Value After Reset: 0x0
5:4	picture_aspect_ratio	R/W	Picture aspect ratio Value After Reset: 0x0
3:0	active_aspect_ratio	R/W	Active aspect ratio Value After Reset: 0x0

fc_aviconf2

Description: Frame Composer AVI Packet Configuration Register 2

Size: 8 bits

Offset: 0x101b

Bits	Name	Attr	Description
7	it_content	R/W	IT content Value After Reset: 0x0
6:4	extended_col	R/W	Extended colorimetry Value After Reset: 0x0

	orimetry		
3:2	quantization_range	R/W	Quantization range Value After Reset: 0x0
1:0	non_uniform_picture_scaling	R/W	Non-uniform picture scaling Value After Reset: 0x0

fc_avivid

Description: Frame Composer AVI Packet VIC Register

Size: 8 bits

Offset: 0x101c

Bits	Name	Attr	Description
7	fc_avivid_7	R/W	Bit 7 of fc_avivid register Value After Reset: 0x0
6:0	fc_avivid	R/W	Configures the AVI InfoFrame Video Identification code. For more information, refer to the CEA-861-E specification. Value After Reset: 0x0

fc_avietb[0:1]

Description: Frame Composer AVI Packet End of Top Bar Register Array

Size: 8 bits

Offset: 0x101d + (i * 0x1)

Bits	Name	Attr	Description
7:0	fc_avietb	R/W	Defines the AVI InfoFrame End of Top Bar value. For more information, refer to the CEA-861-E specification. Value After Reset: 0x0

fc_avisbb[0:1]

Description: Frame Composer AVI Packet Start of Bottom Bar Register Array

Size: 8 bits

Offset: 0x101f + (i * 0x1)

Bits	Name	Attr	Description
7:0	fc_avisbb	R/W	This register defines the AVI InfoFrame Start of Bottom Bar value. For more information, refer to the CEA-861-E specification. Value After Reset: 0x0

fc_avielb[0:1]

Description: Frame Composer AVI Packet End of Left Bar Register Array

Size: 8 bits

Offset: 0x1021 + (i * 0x1)

Bits	Name	Attr	Description
7:0	fc_avielb	R/W	This register defines the AVI InfoFrame End of Left Bar value. For more information, refer to the CEA-861-E specification. Value After Reset: 0x0

fc_avisrb[0:1]

Description: Frame Composer AVI Packet Start of Right Bar Register Array

Size: 8 bits

Offset: 0x1023 + (i * 0x1)

Bits	Name	Attr	Description
7:0	fc_avisrb	R/W	This register defines the AVI InfoFrame Start of Right Bar value. For more information, refer to the CEA-861-E specification.

		Value After Reset: 0x0
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fc_audiconf0

Description: Frame Composer AUD Packet Configuration Register 0

Size: 8 bits

Offset: 0x1025

Bits	Name	Attr	Description
7			Reserved for future use.
6:4	CC	R/W	Channel count Value After Reset: 0x0
3:0	CT	R/W	Coding Type Value After Reset: 0x0

fc_audiconf1

Description: Frame Composer AUD Packet Configuration Register 1

Size: 8 bits

Offset: 0x1026

Bits	Name	Attr	Description
7:6			Reserved for future use.
5:4	SS	R/W	Sampling size Value After Reset: 0x0
3			Reserved for future use.
2:0	SF	R/W	Sampling frequency Value After Reset: 0x0

fc_audiconf2

Description: Frame Composer AUD Packet Configuration Register 2

Size: 8 bits

Offset: 0x1027

Bits	Name	Attr	Description
7:0	CA	R/W	Channel allocation Value After Reset: 0x0

fc_audiconf3

Description: Frame Composer AUD Packet Configuration Register 3

Size: 8 bits

Offset: 0x1028

Bits	Name	Attr	Description
7			Reserved for future use.
6:5	LFEPBL	R/W	LFE playback information LFEPBL1, LFEPBL0 LFE playback level as compared to the other channels. Value After Reset: 0x0
4	DM_INH	R/W	Down mix enable Value After Reset: 0x0
3:0	LSV	R/W	Level shift value (for down mixing) Value After Reset: 0x0

fc_vsdieeid2

Description: Frame Composer VSI Packet Data IEEE Register 2

Size: 8 bits

Offset: 0x1029

Bits	Name	Attr	Description
7:0	IEEE	R/W	This register configures the Vendor Specific InfoFrame IEEE registration identifier. For more information, refer to the CEA- 861-E specification. Value After Reset: 0x0

fc_vsdsiz

Description: Frame Composer VSI Packet Data Size Register

Size: 8 bits

Offset: 0x102a

Bits	Name	Attr	Description
7:5			Reserved for future use.
4:0	VSDSIZE	R/W	Packet size as described in the HDMI Vendor Specific InfoFrame (from the HDMI specification). Value After Reset: 0x1b

fc_vsdieeid1

Description: Frame Composer VSI Packet Data IEEE Register 1

Size: 8 bits

Offset: 0x1030

Bits	Name	Attr	Description
7:0	IEEE	R/W	This register configures the Vendor Specific InfoFrame IEEE registration identifier. For more information, refer to the CEA-861-E specification. Value After Reset: 0x0

fc_vsdieeid0

Description: Frame Composer VSI Packet Data IEEE Register 0

Size: 8 bits

Offset: 0x1031

Bits	Name	Attr	Description
7:0	IEEE	R/W	This register configures the Vendor Specific InfoFrame IEEE registration identifier. For more information, refer to the CEA-861-E specification. Value After Reset: 0x0

fc_vsdpayload[0:23]

Description: Frame Composer VSI Packet Data Payload Register Array

Size: 8 bits

Offset: 0x1032 + (i * 0x1)

Bits	Name	Attr	Description
7:0	fc_vsdpayload	R/W	Frame Composer VSI Packet Data Payload Register Array Configures the Vendor Specific infoFrame 24 bytes specific payload. For more information, refer to the CEA-861-E specification. Value After Reset: 0x0

fc_spdvendorname[0:7]

Description: Frame Composer SPD Packet Data Vendor Name Register Array

Size: 8 bits

Offset: 0x104a + (i * 0x1)

Bits	Name	Attr	Description
7:0	fc_spdvendorname	R/W	Frame Composer SPD Packet Data Vendor Name Register Array Configures the Source Product Descriptor infoFrame 8 bytes Vendor name. For more information, refer to the CEA-861-E specification. Value After Reset: 0x0

fc_spdproductname[0:15]

Description: Frame Composer SPD packet Data Product Name Register Array

Size: 8 bits

Offset: 0x1052 + (i * 0x1)

Bit S	Name	Attr	Description
7:0	fc_spdproduct name	R/W	Frame Composer SPD packet Data Product Name Register Array Configures the Source Product Descriptor infoFrame 16 bytes Product name. For more information, refer to the CEA-861-E specification. Value After Reset: 0x0

fc_spddeviceinf

Description: Frame Composer SPD Packet Data Source Product Descriptor Register

Size: 8 bits

Offset: 0x1062

Bits	Name	Attr	Description
7:0	fc_spddeviceinf	R/W	Frame Composer SPD Packet Data Source Product Descriptor Register Value After Reset: 0x0

fc_audsconf

Description: Frame Composer Audio Sample Flat and Layout Configuration Register

Size: 8 bits

Offset: 0x1063

Bits	Name	Attr	Description
7:4	aud_packet_sampfilt	R/W	Set the audio packet sample flat value to be sent on the packet. Value After Reset: 0x0
3:1			Reserved for future use.
0	aud_packet_layout	R/W	Set the audio packet layout to be sent in the packet: 1b: layout 1 0b: layout 0 If HDMI_TX_20 is defined and register field fc_multistream_ctrl.fc_mas_packet_en is active, this bit has no effect. Value After Reset: 0x0

fc_audsstat

Description: Frame Composer Audio Sample Flat and Layout Status Register

Size: 8 bits

Offset: 0x1064

Bits	Name	Attr	Description
7:4			Reserved for future use.
3:0	packet_sampprs	R	Shows the data sample present indication of the last Audio sample packet sent by the HDMI Tx Controller. This register information is at TMDS clock rate. Value After Reset: 0x0

fc_audsv

Description: Frame Composer Audio Sample Validity Flag Register

Size: 8 bits

Offset: 0x1065

Bits	Name	Attr	Description
7	V3r	R/W	Set validity bit "V" for Channel 3, Right Value After Reset: 0x0
6	V2r	R/W	Set validity bit "V" for Channel 2, Right Value After Reset: 0x0
5	V1r	R/W	Set validity bit "V" for Channel 1, Right Value After Reset: 0x0
4	V0r	R/W	Set validity bit "V" for Channel 0, Right Value After Reset: 0x0
3	V3l	R/W	Set validity bit "V" for Channel 3, Left Value After Reset: 0x0
2	V2l	R/W	Set validity bit "V" for Channel 2, Left Value After Reset: 0x0
1	V1l	R/W	Set validity bit "V" for Channel 1, Left Value After Reset: 0x0
0	V0l	R/W	Set validity bit "V" for Channel 0, Left Value After Reset: 0x0

fc_audsu

Description: Frame Composer Audio Sample User Flag Register

Size: 8 bits

Offset: 0x1066

Bits	Name	Attr	Description
7	U3r	R/W	Set user bit "U" for Channel 3, Right Value After Reset: 0x0
6	U2r	R/W	Set user bit "U" for Channel 2, Right Value After Reset: 0x0
5	U1r	R/W	Set user bit "U" for Channel 1, Right Value After Reset: 0x0
4	U0r	R/W	Set user bit "U" for Channel 0, Right Value After Reset: 0x0
3	U3l	R/W	Set user bit "U" for Channel 3, Left Value After Reset: 0x0
2	U2l	R/W	Set user bit "U" for Channel 2, Left Value After Reset: 0x0
1	U1l	R/W	Set user bit "U" for Channel 1, Left Value After Reset: 0x0
0	U0l	R/W	Set user bit "U" for Channel 0, Left Value After Reset: 0x0

fc_audschnl0

Description: Frame Composer Audio Sample Channel Status Configuration Register 0

Size: 8 bits

Offset: 0x1067

Bits	Name	Attr	Description
7:6			Reserved for future use.
5:4	oiec_cgmsa	R/W	CGMS-A Value After Reset: 0x0
3:1			Reserved for future use.
0	oiec_copyright	R/W	IEC Copyright indication Value After Reset: 0x0

fc_audschnl1

Description: Frame Composer Audio Sample Channel Status Configuration Register 1

Size: 8 bits

Offset: 0x1068

Bits	Name	Attr	Description
7:0	oiec_categorycode	R/W	Category code Value After Reset: 0x0

fc_audschnl2

Description: Frame Composer Audio Sample Channel Status Configuration Register 2

Size: 8 bits

Offset: 0x1069

Bits	Name	Attr	Description
7			Reserved for future use.
6:4	oiec_pcmaudio mode	R/W	PCM audio mode Value After Reset: 0x0
3:0	oiec_sourcember	R/W	Source number Value After Reset: 0x0

fc_audschnl3

Description: Frame Composer Audio Sample Channel Status Configuration Register 3

Size: 8 bits

Offset: 0x106a

Bit s	Name	Attr	Description
7:4	oiec_channeln umcr1	R/W	Channel number for second right sample Value After Reset: 0x0
3:0	oiec_channeln umcr0	R/W	Channel number for first right sample Value After Reset: 0x0

fc_audschnl4

Description: Frame Composer Audio Sample Channel Status Configuration Register 4

Size: 8 bits

Offset: 0x106b

Bit s	Name	Attr	Description
7:4	oiec_channeln umcr3	R/W	Channel number for fourth right sample Value After Reset: 0x0
3:0	oiec_channeln umcr2	R/W	Channel number for third right sample Value After Reset: 0x0

fc_audschnl5

Description: Frame Composer Audio Sample Channel Status Configuration Register 5

Size: 8 bits

Offset: 0x106c

Bits	Name	Attr	Description
7:4	oiec_channeln umcl1	R/W	Channel number for second left sample Value After Reset: 0x0
3:0	oiec_channeln umcl0	R/W	Channel number for first left sample Value After Reset: 0x0

fc_audschnl6

Description: Frame Composer Audio Sample Channel Status Configuration Register 6

Size: 8 bits

Offset: 0x106d

Bits	Name	Attr	Description
7:4	oiec_channeln umcl3	R/W	Channel number for fourth left sample Value After Reset: 0x0

3:0	oiec_channeln umcl2	R/W	Channel number for third left sample Value After Reset: 0x0
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fc_audschnl7

Description: Frame Composer Audio Sample Channel Status Configuration Register 7

Size: 8 bits

Offset: 0x106e

Bits	Name	Attr	Description
7:6	oiec_sampfreq _ext	R/W	Sampling frequency (channel status bits 31 and 30) Value After Reset: 0x0
5:4	oiec_clkaccura cy	R/W	Clock accuracy Value After Reset: 0x0
3:0	oiec_sampfreq	R/W	Sampling frequency Value After Reset: 0x0

fc_audschnl8

Description: Frame Composer Audio Sample Channel Status Configuration Register 8

Size: 8 bits

Offset: 0x106f

Bit s	Name	Attr	Description
7:4	oiec_origsamp freq	R/W	Original sampling frequency Value After Reset: 0x0
3:0	oiec_wordleng th	R/W	Word length configuration Value After Reset: 0x0

fc_ctrlqhigh

Description: Frame Composer Number of High Priority Packets Attended Configuration Register

Size: 8 bits

Offset: 0x1073

Bits	Name	Attr	Description
7:5			Reserved for future use.
4:0	onhighattende d	R/W	Configures the number of high priority packets or audio sample packets consecutively attended before checking low priority queue status. Valid range is from 5'd1 to 5'd31. Value After Reset: 0xf

fc_ctrlqlow

Description: Frame Composer Number of Low Priority Packets Attended Configuration Register

Size: 8 bits

Offset: 0x1074

Bits	Name	Attr	Description
7:5			Reserved for future use.
4:0	onlowattended	R/W	Configures the number of low priority packets or null packets consecutively attended before checking high priority queue status or audio samples availability. Valid range is from 5'd1 to 5'd31. Value After Reset: 0x3

fc_acp0

Description: Frame Composer ACP Packet Type Configuration Register 0

Size: 8 bits

Offset: 0x1075

Bits	Name	Attr	Description
7:0	acptype	R/W	Configures the ACP packet type.

Bits	Name	Attr	Description
			Value After Reset: 0x0

fc_acp16

Description: Frame Composer ACP Packet Body Configuration Register 16

Size: 8 bits

Offset: 0x1082

Bits	Name	Attr	Description
7:0	fc_acp16	R/W	Frame Composer ACP Packet Body Configuration Register 16 Value After Reset: 0x0

fc_acp15

Description: Frame Composer ACP Packet Body Configuration Register 15

Size: 8 bits

Offset: 0x1083

Bits	Name	Attr	Description
7:0	fc_acp15	R/W	Frame Composer ACP Packet Body Configuration Register 15 Value After Reset: 0x0

fc_acp14

Description: Frame Composer ACP Packet Body Configuration Register 14

Size: 8 bits

Offset: 0x1084

Bits	Name	Attr	Description
7:0	fc_acp14	R/W	Frame Composer ACP Packet Body Configuration Register 14 Value After Reset: 0x0

fc_acp13

Description: Frame Composer ACP Packet Body Configuration Register 13

Size: 8 bits

Offset: 0x1085

Bits	Name	Attr	Description
7:0	fc_acp13	R/W	Frame Composer ACP Packet Body Configuration Register 13 Value After Reset: 0x0

fc_acp12

Description: Frame Composer ACP Packet Body Configuration Register 12

Size: 8 bits

Offset: 0x1086

Bits	Name	Attr	Description
7:0	fc_acp12	R/W	Frame Composer ACP Packet Body Configuration Register 12 Value After Reset: 0x0

fc_acp11

Description: Frame Composer ACP Packet Body Configuration Register 11

Size: 8 bits

Offset: 0x1087

Bits	Name	Attr	Description
7:0	fc_acp11	R/W	Frame Composer ACP Packet Body Configuration Register 11 Value After Reset: 0x0

fc_acp10

Description: Frame Composer ACP Packet Body Configuration Register 10

Size: 8 bits

Offset: 0x1088

Bits	Name	Attr	Description
7:0	fc_acp10	R/W	Frame Composer ACP Packet Body Configuration Register 10 Value After Reset: 0x0

fc_acp9

Description: Frame Composer ACP Packet Body Configuration Register 9

Size: 8 bits

Offset: 0x1089

Bits	Name	Attr	Description
7:0	fc_acp9	R/W	Frame Composer ACP Packet Body Configuration Register 9 Value After Reset: 0x0

fc_acp8

Description: Frame Composer ACP Packet Body Configuration Register 8

Size: 8 bits

Offset: 0x108a

Bits	Name	Attr	Description
7:0	fc_acp8	R/W	Frame Composer ACP Packet Body Configuration Register 8 Value After Reset: 0x0

fc_acp7

Description: Frame Composer ACP Packet Body Configuration Register 7

Size: 8 bits

Offset: 0x108b

Bits	Name	Attr	Description
7:0	fc_acp7	R/W	Frame Composer ACP Packet Body Configuration Register 7 Value After Reset: 0x0

fc_acp6

Description: Frame Composer ACP Packet Body Configuration Register 6

Size: 8 bits

Offset: 0x108c

Bits	Name	Attr	Description
7:0	fc_acp6	R/W	Frame Composer ACP Packet Body Configuration Register 6 Value After Reset: 0x0

fc_acp5

Description: Frame Composer ACP Packet Body Configuration Register 5

Size: 8 bits

Offset: 0x108d

Bits	Name	Attr	Description
7:0	fc_acp5	R/W	Frame Composer ACP Packet Body Configuration Register 5 Value After Reset: 0x0

fc_acp4

Description: Frame Composer ACP Packet Body Configuration Register 4

Size: 8 bits

Offset: 0x108e

Bits	Name	Attr	Description
7:0	fc_acp4	R/W	Frame Composer ACP Packet Body Configuration Register 4 Value After Reset: 0x0

fc_acp3

Description: Frame Composer ACP Packet Body Configuration Register 3

Size: 8 bits

Offset: 0x108f

Bits	Name	Attr	Description
7:0	fc_acp3	R/W	Frame Composer ACP Packet Body Configuration Register 3 Value After Reset: 0x0

fc_acp2

Description: Frame Composer ACP Packet Body Configuration Register 2

Size: 8 bits

Offset: 0x1090

Bits	Name	Attr	Description
7:0	fc_acp2	R/W	Frame Composer ACP Packet Body Configuration Register 2 Value After Reset: 0x0

fc_acp1

Description: Frame Composer ACP Packet Body Configuration Register 1

Size: 8 bits

Offset: 0x1091

Bits	Name	Attr	Description
7:0	fc_acp1	R/W	Frame Composer ACP Packet Body Configuration Register 1 Value After Reset: 0x0

fc_iscr1_0

Description: Frame Composer ISRC1 Packet Status, Valid, and Continue Configuration Register

Size: 8 bits

Offset: 0x1092

Bits	Name	Attr	Description
7:5			Reserved for future use.
4:2	isrc_status	R/W	ISRC1 Status signal Value After Reset: 0x0
1	isrc_valid	R/W	ISRC1 Valid control signal Value After Reset: 0x0
0	isrc_cont	R/W	ISRC1 Indication of packet continuation (ISRC2 will be transmitted) Value After Reset: 0x0

fc_iscr1_16

Description: Frame Composer ISRC1 Packet Body Register 16

Size: 8 bits

Offset: 0x1093

Bits	Name	Attr	Description
7:0	fc_iscr1_16	R/W	Frame Composer ISRC1 Packet Body Register 16; configures ISRC1 packet body of the ISRC1 packet Value After Reset: 0x0

fc_iscr1_15

Description: Frame Composer ISRC1 Packet Body Register 15

Size: 8 bits

Offset: 0x1094

Bits	Name	Attr	Description
7:0	fc_iscr1_15	R/W	Frame Composer ISRC1 Packet Body Register 15 Value After Reset: 0x0

fc_iscr1_14

Description: Frame Composer ISRC1 Packet Body Register 14

Size: 8 bits

Offset: 0x1095

Bits	Name	Attr	Description
7:0	fc_iscr1_14	R/W	Frame Composer ISRC1 Packet Body Register 14 Value After Reset: 0x0

fc_iscr1_13

Description: Frame Composer ISRC1 Packet Body Register 13

Size: 8 bits

Offset: 0x1096

Bits	Name	Attr	Description
7:0	fc_iscr1_13	R/W	Frame Composer ISRC1 Packet Body Register 13 Value After Reset: 0x0

fc_iscr1_12

Description: Frame Composer ISRC1 Packet Body Register 12

Size: 8 bits

Offset: 0x1097

Bits	Name	Attr	Description
7:0	fc_iscr1_12	R/W	Frame Composer ISRC1 Packet Body Register 12 Value After Reset: 0x0

fc_iscr1_11

Description: Frame Composer ISRC1 Packet Body Register 11

Size: 8 bits

Offset: 0x1098

Bits	Name	Attr	Description
7:0	fc_iscr1_11	R/W	Frame Composer ISRC1 Packet Body Register 11 Value After Reset: 0x0

fc_iscr1_10

Description: Frame Composer ISRC1 Packet Body Register 10

Size: 8 bits

Offset: 0x1099

Bits	Name	Attr	Description
7:0	fc_iscr1_10	R/W	Frame Composer ISRC1 Packet Body Register 10 Value After Reset: 0x0

fc_iscr1_9

Description: Frame Composer ISRC1 Packet Body Register 9

Size: 8 bits

Offset: 0x109a

Bits	Name	Attr	Description
7:0	fc_iscr1_9	R/W	Frame Composer ISRC1 Packet Body Register 9 Value After Reset: 0x0

fc_iscr1_8

Description: Frame Composer ISRC1 Packet Body Register 8

Size: 8 bits

Offset: 0x109b

Bits	Name	Attr	Description
7:0	fc_iscr1_8	R/W	Frame Composer ISRC1 Packet Body Register 8 Value After Reset: 0x0

fc_iscr1_7

Description: Frame Composer ISRC1 Packet Body Register 7

Size: 8 bits

Offset: 0x109c

Bits	Name	Attr	Description
7:0	fc_iscr1_7	R/W	Frame Composer ISRC1 Packet Body Register 7 Value After Reset: 0x0

fc_iscr1_6

Description: Frame Composer ISRC1 Packet Body Register 6

Size: 8 bits

Offset: 0x109d

Bits	Name	Attr	Description
7:0	fc_iscr1_6	R/W	Frame Composer ISRC1 Packet Body Register 6 Value After Reset: 0x0

fc_iscr1_5

Description: Frame Composer ISRC1 Packet Body Register 5

Size: 8 bits

Offset: 0x109e

Bits	Name	Attr	Description
7:0	fc_iscr1_5	R/W	Frame Composer ISRC1 Packet Body Register 5 Value After Reset: 0x0

fc_iscr1_4

Description: Frame Composer ISRC1 Packet Body Register 4

Size: 8 bits

Offset: 0x109f

Bits	Name	Attr	Description
7:0	fc_iscr1_4	R/W	Frame Composer ISRC1 Packet Body Register 4 Value After Reset: 0x0

fc_iscr1_3

Description: Frame Composer ISRC1 Packet Body Register 3

Size: 8 bits

Offset: 0x10a0

Bits	Name	Attr	Description
7:0	fc_iscr1_3	R/W	Frame Composer ISRC1 Packet Body Register 3 Value After Reset: 0x0

fc_iscr1_2

Description: Frame Composer ISRC1 Packet Body Register 2

Size: 8 bits

Offset: 0x10a1

Bits	Name	Attr	Description
7:0	fc_iscr1_2	R/W	Frame Composer ISRC1 Packet Body Register 2 Value After Reset: 0x0

fc_iscr1_1

Description: Frame Composer ISRC1 Packet Body Register 1

Size: 8 bits

Offset: 0x10a2

Bits	Name	Attr	Description
7:0	fc_iscr1_1	R/W	Frame Composer ISRC1 Packet Body Register 1 Value After Reset: 0x0

fc_iscr2_15

Description: Frame Composer ISRC2 Packet Body Register 15

Size: 8 bits

Offset: 0x10a3

Bits	Name	Attr	Description
7:0	fc_iscr2_15	R/W	Frame Composer ISRC2 Packet Body Register 15; configures the ISRC2 packet body of the ISRC2 packet Value After Reset: 0x0

fc_iscr2_14

Description: Frame Composer ISRC2 Packet Body Register 14

Size: 8 bits

Offset: 0x10a4

Bits	Name	Attr	Description
7:0	fc_iscr2_14	R/W	Frame Composer ISRC2 Packet Body Register 14 Value After Reset: 0x0

fc_iscr2_13

Description: Frame Composer ISRC2 Packet Body Register 13

Size: 8 bits

Offset: 0x10a5

Bits	Name	Attr	Description
7:0	fc_iscr2_13	R/W	Frame Composer ISRC2 Packet Body Register 13 Value After Reset: 0x0

fc_iscr2_12

Description: Frame Composer ISRC2 Packet Body Register 12

Size: 8 bits

Offset: 0x10a6

Bits	Name	Attr	Description
7:0			

7:0	fc_iscr2_12	R/W	Frame Composer ISRC2 Packet Body Register 12 Value After Reset: 0x0
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fc_iscr2_11

Description: Frame Composer ISRC2 Packet Body Register 11

Size: 8 bits

Offset: 0x10a7

Bits	Name	Attr	Description
7:0	fc_iscr2_11	R/W	Frame Composer ISRC2 Packet Body Register 11 Value After Reset: 0x0

fc_iscr2_10

Description: Frame Composer ISRC2 Packet Body Register 10

Size: 8 bits

Offset: 0x10a8

Bits	Name	Attr	Description
7:0	fc_iscr2_10	R/W	Frame Composer ISRC2 Packet Body Register 10 Value After Reset: 0x0

fc_iscr2_9

Description: Frame Composer ISRC2 Packet Body Register 9

Size: 8 bits

Offset: 0x10a9

Bits	Name	Attr	Description
7:0	fc_iscr2_9	R/W	Frame Composer ISRC2 Packet Body Register 9 Value After Reset: 0x0

fc_iscr2_8

Description: Frame Composer ISRC2 Packet Body Register 8

Size: 8 bits

Offset: 0x10aa

Bits	Name	Attr	Description
7:0	fc_iscr2_8	R/W	Frame Composer ISRC2 Packet Body Register 8 Value After Reset: 0x0

fc_iscr2_7

Description: Frame Composer ISRC2 Packet Body Register 7

Size: 8 bits

Offset: 0x10ab

Bits	Name	Attr	Description
7:0	fc_iscr2_7	R/W	Frame Composer ISRC2 Packet Body Register 7 Value After Reset: 0x0

fc_iscr2_6

Description: Frame Composer ISRC2 Packet Body Register 6

Size: 8 bits

Offset: 0x10ac

Bits	Name	Attr	Description
7:0	fc_iscr2_6	R/W	Frame Composer ISRC2 Packet Body Register 6

			Value After Reset: 0x0
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fc_iscr2_5

Description: Frame Composer ISRC2 Packet Body Register 5

Size: 8 bits

Offset: 0x10ad

Bits	Name	Attr	Description
7:0	fc_iscr2_5	R/W	Frame Composer ISRC2 Packet Body Register 5 Value After Reset: 0x0

fc_iscr2_4

Description: Frame Composer ISRC2 Packet Body Register 4

Size: 8 bits

Offset: 0x10ae

Bits	Name	Attr	Description
7:0	fc_iscr2_4	R/W	Frame Composer ISRC2 Packet Body Register 4 Value After Reset: 0x0

fc_iscr2_3

Description: Frame Composer ISRC2 Packet Body Register 3

Size: 8 bits

Offset: 0x10af

Bits	Name	Attr	Description
7:0	fc_iscr2_3	R/W	Frame Composer ISRC2 Packet Body Register 3 Value After Reset: 0x0

fc_iscr2_2

Description: Frame Composer ISRC2 Packet Body Register 2

Size: 8 bits

Offset: 0x10b0

Bits	Name	Attr	Description
7:0	fc_iscr2_2	R/W	Frame Composer ISRC2 Packet Body Register 2 Value After Reset: 0x0

fc_iscr2_1

Description: Frame Composer ISRC2 Packet Body Register 1

Size: 8 bits

Offset: 0x10b1

Bits	Name	Attr	Description
7:0	fc_iscr2_1	R/W	Frame Composer ISRC2 Packet Body Register 1 Value After Reset: 0x0

fc_iscr2_0

Description: Frame Composer ISRC2 Packet Body Register 0

Size: 8 bits

Offset: 0x10b2

Bits	Name	Attr	Description
7:0	fc_iscr2_0	R/W	Frame Composer ISRC2 Packet Body Register 0 Value After Reset: 0x0

fc_datauto0

Description: Frame Composer Data Island Auto Packet Scheduling Register 0

Configures the Frame Composer RDRB(1)/Manual(0) data island packet insertion for SPD, VSD, ISRC2, ISRC1 and ACP packets. On RDRB mode the described packet scheduling is controlled by registers FC_DATAUTO1 and FC_DATAUTO2, while in Manual mode register FC_DATMAN requests to FC the insertion of the requested packet.

Size: 8 bits

Offset: 0x10b3

Bits	Name	Attr	Description
7:5			Reserved for future use.
4	spd_auto	R/W	Enables SPD automatic packet scheduling Value After Reset: 0x0
3	vsd_auto	R/W	Enables VSD automatic packet scheduling Value After Reset: 0x0
2	isrc2_auto	R/W	Enables ISRC2 automatic packet scheduling Value After Reset: 0x0
1	isrc1_auto	R/W	Enables ISRC1 automatic packet scheduling Value After Reset: 0x0
0	acp_auto	R/W	Enables ACP automatic packet scheduling Value After Reset: 0x0

fc_datauto1

Description: Frame Composer Data Island Auto Packet Scheduling Register 1

Configures the Frame Composer (FC) RDRB frame interpolation for SPD, VSD, ISRC2, ISRC1 and ACP packet insertion on data island when FC is on RDRB mode for the listed packets.

Size: 8 bits

Offset: 0x10b4

Bits	Name	Attr	Description
7:4			Reserved for future use.
3:0	auto_frame_interpolation	R/W	Packet frame interpolation for automatic packet scheduling Value After Reset: 0x0

fc_datauto2

Description: Frame Composer Data Island Auto packet scheduling Register 2

Configures the Frame Composer (FC) RDRB line interpolation and number of packets in frame for SPD, VSD, ISRC2, ISRC1 and ACP packet insertion on data island when FC is on RDRB mode for the listed packets.

Size: 8 bits

Offset: 0x10b5

Bits	Name	Attr	Description
7:4	auto_frame_packets	R/W	Packets per frame, for automatic packet scheduling Value After Reset: 0x0
3:0	auto_line_spacing	R/W	Packets line spacing, for automatic packet scheduling Value After Reset: 0x0

fc_datman

Description: Frame Composer Data Island Manual Packet Request Register

Requests to the Frame Composer the data island packet insertion for NULL, SPD, VSD, ISRC2, ISRC1 and ACP packets when FC_DATAUTO0 bit is in manual mode for the packet requested.

Size: 8 bits

Offset: 0x10b6

Bits	Name	Attr	Description
7:6			Reserved for future use.

5	null_tx	W	Null packet Value After Reset: 0x0
4	spd_tx	W	SPD packet Value After Reset: 0x0
3	vsd_tx	W	VSD packet Value After Reset: 0x0
2	isrc2_tx	W	ISRC2 packet Value After Reset: 0x0
1	isrc1_tx	W	ISRC1 packet Value After Reset: 0x0
0	acp_tx	W	ACP packet Value After Reset: 0x0

fc_datauto3

Description: Frame Composer Data Island Auto Packet Scheduling Register 3

Configures the Frame Composer Automatic(1)/RDRB(0) data island packet insertion for AVI, GCP, AUDI and ACR packets. In Automatic mode, the packet is inserted on Vblanking when first line with active Vsync appears.

Size: 8 bits

Offset: 0x10b7

Bits	Name	Attr	Description
7:6			Reserved for future use.
5	nvbi_auto	R/W	Enables NTSC VBI packet insertion Value After Reset: 0x1
4	amp_auto	R/W	Enables AMP packet insertion Value After Reset: 0x1
3	avi_auto	R/W	Enables AVI packet insertion Value After Reset: 0x1
2	gcp_auto	R/W	Enables GCP packet insertion Value After Reset: 0x1
1	audi_auto	R/W	Enables AUDI packet insertion Value After Reset: 0x1
0	acr_auto	R/W	Enables ACR packet insertion Value After Reset: 0x1

fc_rdrb0

Description: Frame Composer Round Robin ACR Packet Insertion Register 0

Configures the Frame Composer (FC) RDRB frame interpolation for ACR packet insertion on data island when FC is on RDRB mode for this packet.

Size: 8 bits

Offset: 0x10b8

Bits	Name	Attr	Description
7:4			Reserved for future use.
3:0	ACRframeinterpolation	R/W	ACR Frame interpolation Value After Reset: 0x0

fc_rdrb1

Description: Frame Composer Round Robin ACR Packet Insertion Register 1

Configures the Frame Composer (FC) RDRB line interpolation and number of packets in frame for the ACR packet insertion on data island when FC is on RDRB mode this packet.

Size: 8 bits

Offset: 0x10b9

Bits	Name	Attr	Description
7:4	ACRpacketsinframe	R/W	ACR packets in frame Value After Reset: 0x0

3:0	ACRpacketline spacing	R/W	ACR packet line spacing Value After Reset: 0x0
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fc_rdrb2

Description: Frame Composer Round Robin AUDI Packet Insertion Register 2

Configures the Frame Composer (FC) RDRB frame interpolation for AUDI packet insertion on data island when FC is on RDRB mode for this packet.

Size: 8 bits

Offset: 0x10ba

Bits	Name	Attr	Description
7:4			Reserved for future use.
3:0	AUDIframeinterpolation	R/W	Audio frame interpolation Value After Reset: 0x0

fc_rdrb3

Description: Frame Composer Round Robin AUDI Packet Insertion Register 3

Configures the Frame Composer (FC) RDRB line interpolation and number of packets in frame for the AUDI packet insertion on data island when FC is on RDRB mode this packet.

Size: 8 bits

Offset: 0x10bb

Bits	Name	Attr	Description
7:4	AUDIpacketsinframe	R/W	Audio packets per frame Value After Reset: 0x0
3:0	AUDIpacketline spacing	R/W	Audio packets line spacing Value After Reset: 0x0

fc_rdrb4

Description: Frame Composer Round Robin GCP Packet Insertion Register 4

Configures the Frame Composer (FC) RDRB frame interpolation for GCP packet insertion on data island when FC is on RDRB mode for this packet.

Size: 8 bits

Offset: 0x10bc

Bits	Name	Attr	Description
7:4			Reserved for future use.
3:0	GCPframeinterpolation	R/W	Frames interpolated between GCP packets Value After Reset: 0x0

fc_rdrb5

Description: Frame Composer Round Robin GCP Packet Insertion Register 5

Configures the Frame Composer (FC) RDRB line interpolation and number of packets in frame for the GCP packet insertion on data island when FC is on RDRB mode this packet.

Size: 8 bits

Offset: 0x10bd

Bits	Name	Attr	Description
7:4	GCPpacketsinframe	R/W	GCP packets per frame Value After Reset: 0x0
3:0	GCPpacketline spacing	R/W	GCP packets line spacing Value After Reset: 0x0

fc_rdrb6

Description: Frame Composer Round Robin AVI Packet Insertion Register 6

Configures the Frame Composer (FC) RDRB frame interpolation for AVI packet insertion on data island when FC is on RDRB mode for this packet.

Size: 8 bits

Offset: 0x10be

Bits	Name	Attr	Description

7:4			Reserved for future use.
3:0	AVIframeinterpolation	R/W	Frames interpolated between AVI packets Value After Reset: 0x0

fc_rdrb7

Description: Frame Composer Round Robin AVI Packet Insertion Register 7

Configures the Frame Composer (FC) RDRB line interpolation and number of packets in frame for the AVI packet insertion on data island when FC is on RDRB mode this packet.

Size: 8 bits

Offset: 0x10bf

Bits	Name	Attr	Description
7:4	AVIpacketsinframe	R/W	AVI packets per frame Value After Reset: 0x0
3:0	AVIpacketlinespacing	R/W	AVI packets line spacing Value After Reset: 0x0

fc_mask0

Description: Frame Composer Packet Interrupt Mask Register 0

Size: 8 bits

Offset: 0x10d2

Bits	Name	Attr	Description
7	AUDI	R/W	Mask bit for FC_INT0.AUDI interrupt bit Value After Reset: 0x0
6	ACP	R/W	Mask bit for FC_INT0.ACPI interrupt bit Value After Reset: 0x0
5	HBR	R/W	Mask bit for FC_INT0.HBR interrupt bit Value After Reset: 0x1
4	MAS	R/W	Mask bit for FC_INT0.MAS interrupt bit. Otherwise, this field is a "spare" bit with no associated functionality. Value After Reset: "(HDMI_TX_20== 1) ? 1 : 0"
3	NVBI	R/W	Mask bit for FC_INT0.NVBI interrupt bit. Otherwise, this field is a "spare" bit with no associated functionality. Value After Reset: "(HDMI_TX_20== 1) ? 1 : 0"
2	AUDS	R/W	Mask bit for FC_INT0.AUDS interrupt bit Value After Reset: 0x1
1	ACR	R/W	Mask bit for FC_INT0.ACR interrupt bit Value After Reset: 0x0
0	NULL	R/W	Mask bit for FC_INT0.NULL interrupt bit Value After Reset: 0x1

fc_mask1

Description: Frame Composer Packet Interrupt Mask Register 1

Size: 8 bits

Offset: 0x10d6

Bits	Name	Attr	Description
7	GMD	R/W	Mask bit for FC_INT1.GMD interrupt bit Value After Reset: 0x0
6	ISCR1	R/W	Mask bit for FC_INT1.ISRC1 interrupt bit Value After Reset: 0x0
5	ISCR2	R/W	Mask bit for FC_INT1.ISRC2 interrupt bit Value After Reset: 0x0
4	VSD	R/W	Mask bit for FC_INT1.VSD interrupt bit

Bits	Name	Attr	Description
			Value After Reset: 0x0
3	SPD	R/W	Mask bit for FC_INT1.SPD interrupt bit Value After Reset: 0x0
2	AMP	R/W	Mask bit for FC_INT1.AMP interrupt bit. Otherwise, this field is a "spare" bit with no associated functionality. Value After Reset: "(HDMI_TX_20== 1) ? 1 : 0"
1	AVI	R/W	Mask bit for FC_INT1.AVI interrupt bit Value After Reset: 0x0
0	GCP	R/W	Mask bit for FC_INT1.GCP interrupt bit Value After Reset: 0x0

fc_mask2

Description: Frame Composer High/Low Priority Overflow and DRM Interrupt Mask Register 2

Size: 8 bits

Offset: 0x10da

Bits	Name	Attr	Description
7:5			Reserved for future use.
4	DRM	R/W	Mask bit for FC_INT2.DRM interrupt bit. Value After Reset: (HDMI_TX_20== 1) ? 1 : 0
3:2			Reserved for future use.
1	LowPriority_overflow	R/W	Mask bit for FC_INT2.LowPriority_overflow interrupt bit Value After Reset: 0x0
0	HighPriority_overflow	R/W	Mask bit for FC_INT2.HighPriority_overflow interrupt bit Value After Reset: 0x0

fc_prconf

Description: Frame Composer Pixel Repetition Configuration Register

Size: 8 bits

Offset: 0x10e0

Bits	Name	Attr	Description
7:4	incoming_pr_factor	R/W	Configures the input video pixel repetition. For CEA modes, this value must be extracted from the CEA specification for the video mode being input. incoming_pr_factor[3:0] 0000b: No action. Not used. 0001b: No pixel repetition (pixel sent only once) 0010b: Pixel sent two times (pixel repeated once) 0011b: Pixel sent three times 0100b: Pixel sent four times 0101b: Pixel sent five times 0110b: Pixel sent six times 0111b: Pixel sent seven times 1000b: Pixel sent eight times 1001b: Pixel sent nine times 1010b: Pixel sent 10 times Other: Reserved. Not used Value After Reset: 0x1
3:0	output_pr_factor	R/W	Configures the video pixel repetition ratio to be sent on the AVI InfoFrame. This value must be valid according to the HDMI specification. The output_pr_factor = incoming_pr_factor * (desired_pr_factor + 1) - 1. output_pr_factor[3:0] 0000b: No action. Not used. 0001b: Pixel sent two times (pixel repeated once) 0010b: Pixel sent three times 0011b: Pixel sent four times 0100b: Pixel sent five times 0101b: Pixel sent six times 0110b: Pixel sent

Bits	Name	Attr	Description
			<p>seven times 0111b: Pixel sent eight times 1000b: Pixel sent nine times 1001b: Pixel sent 10 times Other: Reserved. Not used</p> <p>Note: When working in YCC422 video, the actual repetition of the stream is Incoming_pr_factor * (desired_pr_factor + 1). This calculation is done internally in the H13TCTRL and no hardware overflow protection is available. Care must be taken to avoid this result passes the maximum number of 10 pixels repeated because no HDMI support is available for this in the specification and the H13TPHY does not support this higher repetition values.</p> <p>Value After Reset: 0x0</p>

fc_scrambler_ctrl

Description: Frame Composer Scrambler Control

Size: 8 bits

Offset: 0x10e1

Bits	Name	Attr	Description
7:5			Reserved for future use.
4	scrambler_ucp_line	R/W	<p>Debug register. When active (1'b1), the Unscrambled Control Period is generated after each active video line (non-compliant behavior). This is quasi-static field which requires a mc_swrtzreq.tmdsswrst_req reset request to be performed after the change of this configuration bit.</p> <p>Value After Reset: 0x0</p>
3:1			Reserved for future use.
0	scrambler_on	R/W	<p>When set (1'b1), this field activates the HDMI 2.0 scrambler feature. When disabled (1'b0) the scrambler feature is bypassed, placing Hdmi_tx in HDMI 1.4b compatible mode. To activate the scrambler feature, you must ensure that the quasi-static configuration bit fc_invidconf.HDCP_keepout is set (1'b1) at configuration time, before the required mc_swrtzreq.tmdsswrst_req reset request is issued. This is field can be changed in runtime.</p> <p>Value After Reset: 0x0</p>

fc_gmd_stat

Description: Frame Composer GMD Packet Status Register

Gamut metadata packet status bit information for no_current_gmd, next_gmd_field, gmd_packet_sequence and current_gamut_seq_num. For more information, refer to the HDMI 1.4b specification.

Size: 8 bits

Offset: 0x1100

Bits	Name	Attr	Description
7	igmdno_crnt_gbd	R	<p>Gamut scheduling: No current gamut data</p> <p>Value After Reset: 0x0</p>
6	igmddnext_field	R	<p>Gamut scheduling: Gamut Next field</p> <p>Value After Reset: 0x0</p>
5:4	igmdpacket_seq	R	<p>Gamut scheduling: Gamut packet sequence</p> <p>Value After Reset: 0x0</p>
3:0	igmdcurrent	R	<p>Gamut scheduling: Current Gamut packet</p>

Bits	Name	Attr	Description
	_gamut_seq_num		sequence number Value After Reset: 0x0

fc_gmd_en

Description: Frame Composer GMD Packet Enable Register

This register enables Gamut metadata (GMD) packet transmission. Packets are inserted in the incoming frame, starting in the line where active Vsync indication starts. After enable of GMD packets the outgoing packet is sent with no_current_gmd active indication until update GMD request is performed in the controller.

Size: 8 bits

Offset: 0x1101

Bits	Name	Attr	Description
7:1			Reserved for future use.
0	gmdenabletx	R/W	Gamut Metadata packet transmission enable (1b) Value After Reset: 0x0

fc_gmd_up

Description: Frame Composer GMD Packet Update Register

This register performs an GMD packet content update according to the configured packet body (FC_GMD_PB0 to FC_GMD_PB27) and packet header (FC_GMD_HB). This active high auto clear register reflects the body and header configurations on the GMD packets sent arbitrating the current_gamut_seq_num, gmd_packet_sequence and next_gmd_field bits on packet to correctly indicate to source the Gamut change to be performed. After enable GMD packets the first update request is also responsible for deactivating the no_current_gmd indication bit. Attention packet update request must only be done after correct configuration of GMD packet body and header registers. Correct affected_gamut_seq_num and gmd_profile configuration is user responsibility and must convey with HDMI 1.4b standard gamut rules.

Size: 8 bits

Offset: 0x1102

Bits	Name	Attr	Description
7:1			Reserved for future use.
0	gmdupdatepacket	W	Gamut Metadata packet update Value After Reset: 0x0

fc_gmd_conf

Description: Frame Composer GMD Packet Schedule Configuration Register

This register configures the number of GMD packets to be inserted per frame (starting always in the line where the active Vsync appears) and the line spacing between the transmitted GMD packets.

Note that for profile P0 (refer to the HDMI 1.4b specification) this register should only indicate one GMD packet to be inserted per video field.

Size: 8 bits

Offset: 0x1103

Bits	Name	Attr	Description
7:4	gmdpacketsinframe	R/W	Number of GMD packets per frame or video field (profile P0) Value After Reset: 0x1
3:0	gmdpacketlinespacing	R/W	Number of line spacing between the transmitted GMD packets Value After Reset: 0x0

fc_gmd_hb

Description: Frame Composer GMD Packet Profile and Gamut Sequence Configuration Register

This register configures the GMD packet header affected_gamut_seq_num and gmd_profile

bits. For more information, refer to the HDMI 1.4b specification.

Size: 8 bits

Offset: 0x1104

Bits	Name	Attr	Description
7			Reserved for future use.
6:4	gmdgbd_profile	R/W	GMD profile bits. Hdmi_tx only supports Profile 0 (P0) of the Gamut Boundary Description Metadata Profiles described in the HDMI 1.4 Specification (which defines four profiles, P0-P4). Value After Reset: 0x0
3:0	gmdaffected_gamut_seq_num	R/W	Affected gamut sequence number Value After Reset: 0x0

fc_gmd_pb[0:27]

Description: Frame Composer GMD Packet Body Register Array Configures the GMD packet body of the GMD packet.

Size: 8 bits

Offset: 0x1105 + (i * 0x1)

Bits	Name	Attr	Description
7:0	fc_gmd_pb	R/W	Frame Composer GMD Packet Body Register Array Value After Reset: 0x0

fc_dbgforce

Description: Frame Composer video/audio Force Enable Register

This register allows to force the controller to output audio and video data the values configured in the FC_DBGAUD and FC_DBGTMDS registers.

Size: 8 bits

Offset: 0x1200

Bits	Name	Attr	Description
7:5			Reserved for future use.
4	forceaudio	R/W	Force fixed audio output with FC_DBGAUDxCHx register contents. Value After Reset: 0x0
3:1			Reserved for future use.
0	forcevideo	R/W	Force fixed video output with FC_DBGTMDSx register contents. Value After Reset: 0x0

fc_dbgaud0cho

Description: Frame Composer Audio Data Channel 0 Register 0

Configures the audio fixed data to be used in channel 0 when in fixed audio selection.

Size: 8 bits

Offset: 0x1201

Bits	Name	Attr	Description
7:0	fc_dbgaud0ch0	R/W	Frame Composer Audio Data Channel 0 Register 0 Value After Reset: 0x0

fc_dbgaud1cho

Description: Frame Composer Audio Data Channel 0 Register 1

Configures the audio fixed data to be used in channel 0 when in fixed audio selection.

Size: 8 bits

Offset: 0x1202

Bits	Name	Attr	Description
7:0	fc_dbgaud1 ch0	R/W	Frame Composer Audio Data Channel 0 Register 1 Value After Reset: 0x0

fc_dbgaud2ch0

Description: Frame Composer Audio Data Channel 0 Register 2

Configures the audio fixed data to be used in channel 0 when in fixed audio selection.

Size: 8 bits

Offset: 0x1203

Bits	Name	Attr	Description
7:0	fc_dbgaud2 ch0	R/W	Frame Composer Audio Data Channel 0 Register 2 Value After Reset: 0x0

fc_dbgaud0ch1

Description: Frame Composer Audio Data Channel 1 Register 0

Configures the audio fixed data to be used in channel 1 when in fixed audio selection.

Size: 8 bits

Offset: 0x1204

Bits	Name	Attr	Description
7:0	fc_dbgaud0 ch1	R/W	Frame Composer Audio Data Channel 1 Register 0 Value After Reset: 0x0

fc_dbgaud1ch1

Description: Frame Composer Audio Data Channel 1 Register 1

Configures the audio fixed data to be used in channel 1 when in fixed audio selection.

Size: 8 bits

Offset: 0x1205

Bits	Name	Attr	Description
7:0	fc_dbgaud1 ch1	R/W	Frame Composer Audio Data Channel 1 Register 1 Value After Reset: 0x0

fc_dbgaud2ch1

Description: Frame Composer Audio Data Channel 1 Register 2

Configures the audio fixed data to be used in channel 1 when in fixed audio selection.

Size: 8 bits

Offset: 0x1206

Bits	Name	Attr	Description
7:0	fc_dbgaud2 ch1	R/W	Frame Composer Audio Data Channel 1 Register 2 Value After Reset: 0x0

fc_dbgaud0ch2

Description: Frame Composer Audio Data Channel 2 Register 0

Configures the audio fixed data to be used in channel 2 when in fixed audio selection.

Size: 8 bits

Offset: 0x1207

Bits	Name	Attr	Description
7:0	fc_dbgaud0 ch2	R/W	Frame Composer Audio Data Channel 2 Register 0 Value After Reset: 0x0

fc_dbgaud1ch2

Description: Frame Composer Audio Data Channel 2 Register 1

Configures the audio fixed data to be used in channel 2 when in fixed audio selection.

Size: 8 bits Offset: 0x1208

Bits	Name	Attr	Description
7:0	fc_dbgaud1c h2	R/W	Frame Composer Audio Data Channel 2 Register 1 Value After Reset: 0x0

fc_dbgaud2ch2

Description: Frame Composer Audio Data Channel 2 Register 2

Configures the audio fixed data to be used in channel 2 when in fixed audio selection.

Size: 8 bits

Offset: 0x1209

Bits	Name	Attr	Description
7:0	fc_dbgaud2 ch2	R/W	Frame Composer Audio Data Channel 2 Register 2 Value After Reset: 0x0

fc_dbgaud0ch3

Description: Frame Composer Audio Data Channel 3 Register 0

Configures the audio fixed data to be used in channel 3 when in fixed audio selection.

Size: 8 bits

Offset: 0x120a

Bits	Name	Attr	Description
7:0	fc_dbgaud0 ch3	R/W	Frame Composer Audio Data Channel 3 Register 0 Value After Reset: 0x0

fc_dbgaud1ch3

Description: Frame Composer Audio Data Channel 3 Register 1

Configures the audio fixed data to be used in channel 3 when in fixed audio selection.

Size: 8 bits

Offset: 0x120b

Bits	Name	Attr	Description
7:0	fc_dbgaud1c h3	R/W	Frame Composer Audio Data Channel 3 Register 1 Value After Reset: 0x0

fc_dbgaud2ch3

Description: Frame Composer Audio Data Channel 3 Register 2

Configures the audio fixed data to be used in channel 3 when in fixed audio selection.

Size: 8 bits

Offset: 0x120c

Bits	Name	Attr	Description
7:0	fc_dbgaud2 ch3	R/W	Frame Composer Audio Data Channel 3 Register 2 Value After Reset: 0x0

fc_dbgaud0ch4

Description: Frame Composer Audio Data Channel 4 Register 0

Configures the audio fixed data to be used in channel 4 when in fixed audio selection.

Size: 8 bits

Offset: 0x120d

Bits	Name	Attr	Description
7:0	fc_dbgaud0	R/W	Frame Composer Audio Data Channel 4

	ch4		Register 0 Value After Reset: 0x0
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fc_dbgaud1ch4

Description: Frame Composer Audio Data Channel 4 Register 1

Configures the audio fixed data to be used in channel 4 when in fixed audio selection.

Size: 8 bits

Offset: 0x120e

Bits	Name	Attr	Description
7:0	fc_dbgaud1ch4	R/W	Frame Composer Audio Data Channel 4 Register 1 Value After Reset: 0x0

fc_dbgaud2ch4

Description: Frame Composer Audio Data Channel 4 Register 2

Configures the audio fixed data to be used in channel 4 when in fixed audio selection.

Size: 8 bits

Offset: 0x120f

Bits	Name	Attr	Description
7:0	fc_dbgaud2ch4	R/W	Frame Composer Audio Data Channel 4 Register 2 Value After Reset: 0x0

fc_dbgaud0ch5

Description: Frame Composer Audio Data Channel 5 Register 0

Configures the audio fixed data to be used in channel 5 when in fixed audio selection.

Size: 8 bits

Offset: 0x1210

Bits	Name	Attr	Description
7:0	fc_dbgaud0ch5	R/W	Frame Composer Audio Data Channel 5 Register 0 Value After Reset: 0x0

fc_dbgaud1ch5

Description: Frame Composer Audio Data Channel 5 Register 1

Configures the audio fixed data to be used in channel 5 when in fixed audio selection.

Size: 8 bits

Offset: 0x1211

Bits	Name	Attr	Description
7:0	fc_dbgaud1ch5	R/W	Frame Composer Audio Data Channel 5 Register 1 Value After Reset: 0x0

fc_dbgaud2ch5

Description: Frame Composer Audio Data Channel 5 Register 2

Configures the audio fixed data to be used in channel 5 when in fixed audio selection.

Size: 8 bits

Offset: 0x1212

Bits	Name	Attr	Description
7:0	fc_dbgaud2ch5	R/W	Frame Composer Audio Data Channel 5 Register 2 Value After Reset: 0x0

fc_dbgaud0ch6

Description: Frame Composer Audio Data Channel 6 Register 0

Configures the audio fixed data to be used in channel 6 when in fixed audio selection.

Size: 8 bits

Offset: 0x1213

Bits	Name	Attr	Description
7:0	fc_dbgaud0 ch6	R/W	Frame Composer Audio Data Channel 6 Register 0 Value After Reset: 0x0

fc_dbgaud1ch6

Description: Frame Composer Audio Data Channel 6 Register 1

Configures the audio fixed data to be used in channel 6 when in fixed audio selection.

Size: 8 bits

Offset: 0x1214

Bits	Name	Attr	Description
7:0	fc_dbgaud1 ch6	R/W	Frame Composer Audio Data Channel 6 Register 1 Value After Reset: 0x0

fc_dbgaud2ch6

Description: Frame Composer Audio Data Channel 6 Register 2

Configures the audio fixed data to be used in channel 6 when in fixed audio selection.

Size: 8 bits

Offset: 0x1215

Bits	Name	Attr	Description
7:0	fc_dbgaud2 ch6	R/W	Frame Composer Audio Data Channel 6 Register 2 Value After Reset: 0x0

fc_dbgaud0ch7

Description: Frame Composer Audio Data Channel 7 Register 0

Configures the audio fixed data to be used in channel 7 when in fixed audio selection.

Size: 8 bits

Offset: 0x1216

Bits	Name	Attr	Description
7:0	fc_dbgaud0 ch7	R/W	Frame Composer Audio Data Channel 7 Register 0 Value After Reset: 0x0

fc_dbgaud1ch7

Description: Frame Composer Audio Data Channel 7 Register 1

Configures the audio fixed data to be used in channel 7 when in fixed audio selection.

Size: 8 bits

Offset: 0x1217

Bits	Name	Attr	Description
7:0	fc_dbgaud1c h7	R/W	Frame Composer Audio Data Channel 7 Register 1 Value After Reset: 0x0

fc_dbgaud2ch7

Description: Frame Composer Audio Data Channel 7 Register 2

Configures the audio fixed data to be used in channel 7 when in fixed audio selection.

Size: 8 bits

Offset: 0x1218

Bits	Name	Attr	Description
7:0	fc_dbgaud2c	R/W	Frame Composer Audio Data Channel 7

	h7		Register 2 Value After Reset: 0x0
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fc_dbgtdms[0:2]

Description: Frame Composer TMDS Data Channel Register Array

Configures the video fixed data to be used in TMDS channel x (where x is 0 to 2) when in fixed video selection.

For Channel 0, this equals to set B pixel component value in RGB video or Cb pixel component value in YCbCr.

For Channel 1, this equals set G pixel component value in RGB video or Y pixel component value in YCbCr.

For Channel 2, this equals to set R pixel component value in RGB video or Cr pixel component value in YCbCr.

Size: 8 bits

Offset: 0x1219 + (i * 0x1)

Bits	Name	Attr	Description
7:0	fc_dbgtdms	R/W	Frame Composer TMDS Data Channel 0 Register Value After Reset: 0x0

PHYConfiguration Registers

PHY Configuration Registers. Follow the link for the register to see a detailed description of the register.

Registers for Address Block: PHYConfiguration

Register	Offset	Description
phy_conf0	0x3000	PHY Configuration Register This register holds the power down, data enable polarity, and interface...
phy_tst0	0x3001	PHY Test Interface Register 0 PHY TX mapped test interface (control). For more information, refer...
phy_tst1	0x3002	PHY Test Interface Register 1 PHY TX mapped text interface (data in). For more information, refer...
phy_tst2	0x3003	PHY Test Interface Register 2 PHY TX mapped text interface (data out). For more information, refer...
phy_stat0	0x3004	PHY RXSENSE, PLL Lock, and HPD Status Register This register contains the following active high...
phy_int0	0x3005	PHY RXSENSE, PLL Lock, and HPD Interrupt Register This register contains the interrupt indication...
phy_mask0	0x3006	PHY RXSENSE, PLL Lock, and HPD Mask Register Mask register for generation of PHY_INT0...
phy_polo	0x3007	PHY RXSENSE, PLL Lock, and HPD Polarity Register Polarity register for generation of PHY_INT0...
PHY_PCLFREQ0	0x3008	PHY Test Interface Register 0
PHY_PCLFREQ1	0x3009	PHY Test Interface Register 1
PHY_PLLCFGFREQ0	0x300a	PHY PLL Test Interface Register 0
PHY_PLLCFGFREQ1	0x300b	PHY PLL Test Interface Register 1
PHY_PLLCFGFREQ2	0x300c	PHY PLL Test Interface Register 2
phy_i2cm_slave	0x3020	PHY I2C Slave Address Configuration

		Register
phy_i2cm_address	0x3021	PHY I2C Address Configuration Register This register writes the address for read and write...
phy_i2cm_datao_1	0x3022	PHY I2C Data Write Register 1
phy_i2cm_datao_0	0x3023	PHY I2C Data Write Register 0
phy_i2cm_datai_1	0x3024	PHY I2C Data Read Register 1
phy_i2cm_datai_0	0x3025	PHY I2C Data Read Register 0
phy_i2cm_operation	0x3026	PHY I2C RD/RD_EXT/WR Operation Register This register requests read and write operations from the...
phy_i2cm_int	0x3027	PHY I2C Done Interrupt Register This register contains and configures I2C master PHY done...

Registers for Address Block: PHYConfiguration (Continued)

Register	Offset	Description
phy_i2cm_ctlint	0x3028	PHY I2C error Interrupt Register This register contains and configures the I2C master PHY error...
phy_i2cm_div	0x3029	PHY I2C Speed control Register This register sets the I2C Master PHY to work in either Fast or...
phy_i2cm_softrstz	0x302a	PHY I2C SW reset control register This register sets the I2C Master PHY software reset.
phy_i2cm_ss_scl_hcnt_1_a_ddr	0x302b	PHY I2C Slow Speed SCL High Level Control Register 1
phy_i2cm_ss_scl_hcnt_0_a_ddr	0x302c	PHY I2C Slow Speed SCL High Level Control Register 0
phy_i2cm_ss_scl_lcnt_1_a_ddr	0x302d	PHY I2C Slow Speed SCL Low Level Control Register 1
phy_i2cm_ss_scl_lcnt_0_a_ddr	0x302e	PHY I2C Slow Speed SCL Low Level Control Register 0
phy_i2cm_fs_scl_hcnt_1_a_ddr	0x302f	PHY I2C Fast Speed SCL High Level Control Register 1
phy_i2cm_fs_scl_hcnt_0_a_ddr	0x3030	PHY I2C Fast Speed SCL High Level Control Register 0
phy_i2cm_fs_scl_lcnt_1_ad_dr	0x3031	PHY I2C Fast Speed SCL Low Level Control Register 1
phy_i2cm_fs_scl_lcnt_0_ad_dr	0x3032	PHY I2C Fast Speed SCL Low Level Control Register 0
phy_i2cm_sda_hold	0x3033	PHY I2C SDA HOLD Control Register

phy_conf0

Description: PHY Configuration Register

This register holds the power down, data enable polarity, and interface control of the HDMI Source PHY control.

Size: 8 bits

Offset: 0x3000

Bits	Name	Attr	description
7	PDZ	R/W	Power-down enable (active low 0b). Otherwise, this field is a "spare" bit with no associated functionality. Value After Reset: 0x0
6	ENTMDS	R/W	Enable TMDS drivers, bias, and TMDS digital logic. Otherwise, this field is a "spare" bit with no associated functionality. Value After Reset: 0x0
5	svsret	R/W	PHY SVSRET signal. Otherwise, this field is a

			"spare" bit with no associated functionality. Value After Reset: 0x0
4	pddq	R/W	PHY PDDQ signal. Otherwise, this field is a "spare" bit with no associated functionality. Value After Reset: "(PHY_MHL_COMBO== 1) ? 1 : 0"
3	txpwron	R/W	PHY TXPWRON signal. Otherwise, this field is a "spare" bit with no associated functionality. Value After Reset: 0x0
2	enhpdrrxsense	R/W	PHY ENHPDRXSENSE signal. Otherwise, this field is a "spare" bit with no associated functionality. Value After Reset: 0x1
1	seldataenpol	R/W	Select data enable polarity. Value After Reset: 0x1
0	seldipif	R/W	Select interface control. Value After Reset: 0x0

phy_tst0

Description: PHY Test Interface Register 0

PHY TX mapped test interface (control).

Size: 8 bits

Offset: 0x3001

Bits	Name	Attr	Description
7:6	spare_2	R/W	Reserved as "spare" bit with no associated functionality. Value After Reset: 0x0
5	testclr	R/W	Test Clear signal. Otherwise, this field is a "spare" bit with no associated functionality. Value After Reset: 0x0
4	testen	R/W	Test Enable signal. Otherwise, this field is a "spare" bit with no associated functionality. Value After Reset: 0x0
3:1	spare_1	R/W	Reserved as "spare" bit with no associated functionality. Value After Reset: 0x0
0	testclk	R/W	Test Clock signal. Otherwise, this field is a "spare" bit with no associated functionality. Value After Reset: 0x0

phy_tst1

Description: PHY Test Interface Register 1

PHY TX mapped text interface (data in).

Size: 8 bits

Offset: 0x3002

Bits	Name	Attr	Description
7:0	testdin	R/W	Test Data input. Otherwise, this field is a "spare" bit with no associated functionality. Value After Reset: 0x0

phy_tst2

Description: PHY Test Interface Register 2

PHY TX mapped text interface (data out).

Size: 8 bits

Offset: 0x3003

Bits	Name	Attr	Description
7:0	testdout	R	Test Data output. Otherwise, this field is a "spare" bit with no associated functionality. Value After Reset: 0x0

phy_stat0

Description: PHY RXSENSE, PLL Lock, and HPD Status Register

This register contains the following active high packet sent status indications.

Size: 8 bits

Offset: 0x3004

Bits	Name	Attr	Description
7	RX_SENSE_3	R	Status bit. TX PHY RX_SENSE indication for TMDS channel 3 driver. You may need to mask or change polarity of this interrupt after it has became active. Value After Reset: 0x0
6	RX_SENSE_2	R	Status bit. TX PHY RX_SENSE indication for TMDS channel 2 driver. You may need to mask or change polarity of this interrupt after it has became active. Value After Reset: 0x0
5	RX_SENSE_1	R	Status bit. TX PHY RX_SENSE indication for TMDS channel 1 driver. You may need to mask or change polarity of this interrupt after it has became active. Value After Reset: 0x0
4	RX_SENSE_0	R	Status bit. TX PHY RX_SENSE indication for TMDS channel 0 driver. You may need to mask or change polarity of this interrupt after it has became active. Value After Reset: 0x0
3:2			Reserved for future use.
1	HPD	R	Status bit. HDMI Hot Plug Detect indication. You may need to mask or change polarity of this interrupt after it has became active. Value After Reset: 0x0
0	TX_PHY_LO CK	R	Status bit. TX PHY PLL lock indication. You may need to mask or change polarity of this interrupt after it has became active. Value After Reset: 0x0

phy_int0

Description: PHY RXSENSE, PLL Lock, and HPD Interrupt Register

This register contains the interrupt indication of the PHY_STAT0 status interrupts. Interrupt generation is accomplished in the following way:

interrupt = (mask == 1'b0) && (polarity == status);

All these interrupts are forwarded to the Interrupt Handler sticky bit register ih_phy_stat0 and after ORed to a single main interrupt line to micro controller. Assertion of this interrupt implies that data related with the corresponding packet has been sent through the HDMI interface.

Size: 8 bits

Offset: 0x3005

Bits	Name	Attr	Description
7	RX_SENSE_3	R	Interrupt indication bit. TX PHY RX_SENSE indication interruption for TMDS CLK driver. Value After Reset: 0x0
6	RX_SENSE_2	R	Interrupt indication bit. TX PHY RX_SENSE indication interruption for TMDS channel 2 driver. Value After Reset: 0x0
5	RX_SENSE_1	R	Interrupt indication bit. TX PHY RX_SENSE indication interruption for TMDS channel 1 driver. Value After Reset: 0x0

4	RX_SENSE_0	R	Interrupt indication bit. TX PHY RX_SENSE indication interruption for TMDS channel 0 driver. Value After Reset: 0x0
3:2			Reserved for future use.
1	HPD	R	Interrupt indication bit. HDMI Hot Plug Detect indication interrupt. Value After Reset: 0x0
0	TX_PHY_LOCK	R	Interrupt indication bit. TX PHY PLL lock indication interrupt. Value After Reset: 0x0

phy_mask0

Description: PHY RXSENSE, PLL Lock, and HPD Mask Register Mask register for generation of PHY_INT0 interrupts.

Size: 8 bits

Offset: 0x3006

Bits	Name	Attr	Description
7	RX_SENSE_3	R/W	Mask bit for PHY_INT0.RX_SENSE[3] interrupt bit Value After Reset: 0x0
6	RX_SENSE_2	R/W	Mask bit for PHY_INT0.RX_SENSE[2] interrupt bit Value After Reset: 0x0
5	RX_SENSE_1	R/W	Mask bit for PHY_INT0.RX_SENSE[1] interrupt bit Value After Reset: 0x0
4	RX_SENSE_0	R/W	Mask bit for PHY_INT0.RX_SENSE[0] interrupt bit Value After Reset: 0x0
3:2			Reserved for future use.
1	HPD	R/W	Mask bit for PHY_INT0.HPD interrupt bit Value After Reset: 0x0
0	TX_PHY_LOCK	R/W	Mask bit for PHY_INT0.TX_PHY_LOCK interrupt bit Value After Reset: 0x0

phy_pol0

Description: PHY RXSENSE, PLL Lock, and HPD Polarity Register Polarity register for generation of PHY_INT0 interrupts.

Size: 8 bits

Offset: 0x3007

Bits	Name	Attr	Description
7	RX_SENSE_3	R/W	Polarity bit for PHY_INT0.RX_SENSE[3] interrupt bit Value After Reset: 0x1
6	RX_SENSE_2	R/W	Polarity bit for PHY_INT0.RX_SENSE[2] interrupt bit Value After Reset: 0x1
5	RX_SENSE_1	R/W	Polarity bit for PHY_INT0.RX_SENSE[1] interrupt bit Value After Reset: 0x1
4	RX_SENSE_0	R/W	Polarity bit for PHY_INT0.RX_SENSE[0] interrupt bit Value After Reset: 0x1
3:2			Reserved for future use.
1	HPD	R/W	Polarity bit for PHY_INT0.HPD interrupt bit

Bits	Name	Attr	Description
			Value After Reset: 0x1
0	TX_PHY_LO CK	R/W	Polarity bit for PHY_INT0.TX_PHY_LOCK interrupt bit Value After Reset: 0x1

PHY_PCLFREQ0

Description: PHY Test Interface Register 0

Size: 8 bits

Offset: 0x3008

Bits	Name	Attr	Description
7:0	pclk_freq	R/W	Pixel Clock Frequency (pclk_freq[7:0]). Value After Reset: 0x32

PHY_PCLFREQ1

Description: PHY Test Interface Register 1

Size: 8 bits

Offset: 0x3009

Bits	Name	Attr	Description
7:2			Reserved for future use.
1:0	pclk_freq	R/W	Pixel Clock Frequency (pclk_freq[9:8]). Value After Reset: 0x0

PHY_PLLCFGREQ0

Description: PHY PLL Test Interface Register 0

Size: 8 bits

Offset: 0x300a

Bits	Name	Attr	Description
7:0	pllcfgfreq	R/W	PLL Configuration Frequency (pllcfgfreq[7:0]). Value After Reset: 0x20

PHY_PLLCFGREQ1

Description: PHY PLL Test Interface Register 1

Size: 8 bits

Offset: 0x300b

Bits	Name	Attr	Description
7:0	pllcfgfreq	R/W	PLL Configuration Frequency (pllcfgfreq[15:8]). Value After Reset: 0x27

PHY_PLLCFGREQ2

Description: PHY PLL Test Interface Register 2

Size: 8 bits

Offset: 0x300c

Bits	Name	Attr	Description
7:0	pllcfgfreq	R/W	PLL Configuration Frequency (pllcfgfreq[23:16]). Value After Reset: 0x0

phy_i2cm_slave

Description: PHY I2C Slave Address Configuration Register

Size: 8 bits

Offset: 0x3020

Bits	Name	Attr	Description
7			Reserved for future use.
6:0	slaveaddr	R/W	Slave address to be sent during read and write operations.

			PHY Gen2 slave address: 7'h69 HEAC PHY slave address: 7'h49 Value After Reset: 0x0
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phy_i2cm_address

Description: PHY I2C Address Configuration Register

This register writes the address for read and write operations.

Size: 8 bits

Offset: 0x3021

Bits	Name	Attr	Description
7:0	address	R/W	Register address for read and write operations Value After Reset: 0x0

phy_i2cm_datao_1

Description: PHY I2C Data Write Register 1

Size: 8 bits

Offset: 0x3022

Bits	Name	Attr	Description
7:0	datao	R/W	Data MSB (datao[15:8]) to be written on register pointed by phy_i2cm_address [7:0]. Value After Reset: 0x0

phy_i2cm_datao_0

Description: PHY I2C Data Write Register 0

Size: 8 bits

Offset: 0x3023

Bits	Name	Attr	Description
7:0	datao	R/W	Data LSB (datao[7:0]) to be written on register pointed by phy_i2cm_address [7:0]. Value After Reset: 0x0

phy_i2cm_datai_1

Description: PHY I2C Data Read Register 1

Size: 8 bits

Offset: 0x3024

Bits	Name	Attr	Description
7:0	datai	R	Data MSB (datai[15:8]) read from register pointed by phy_i2cm_address[7:0]. Value After Reset: 0x0

phy_i2cm_datai_0

Description: PHY I2C Data Read Register 0

Size: 8 bits

Offset: 0x3025

Bits	Name	Attr	Description
7:0	datai	R	Data LSB (datai[7:0]) read from register pointed by phy_i2cm_address[7:0]. Value After Reset: 0x0

phy_i2cm_operation

Description: PHY I2C RD/RD_EXT/WR Operation Register

This register requests read and write operations from the I2C Master PHY. This register can only be written; reading this register always results in 00h. Writing 1'b1 simultaneously to read and write requests is considered a read request.

Size: 8 bits

Offset: 0x3026

Bits	Name	Attr	Description
7:5			Reserved for future use.
4	wr	W	Write operation request Value After Reset: 0x0
3:1			Reserved for future use.
0	rd	W	Read operation request Value After Reset: 0x0

phy_i2cm_int

Description: PHY I2C Done Interrupt Register

This register contains and configures I2C master PHY done interrupt.

Size: 8 bits

Offset: 0x3027

Bits	Name	Attr	Description
7:4			Reserved for future use.
3	done_pol	R/W	Done interrupt polarity configuration Value After Reset: 0x1
2	done_mask	R/W	Done interrupt mask signal Value After Reset: 0x0
1	done_interrupt	R	Operation done interrupt bit. Only lasts for 1 SFR clock cycle and is auto cleared after it. {done_interrupt = (done_mask==0b) && (done_status==done_pol)} Value After Reset: 0x0
0	done_status	R	Operation done status bit. Marks the end of a read or write operation. Value After Reset: 0x0

phy_i2cm_ctlint

Description: PHY I2C error Interrupt Register

This register contains and configures the I2C master PHY error interrupts.

Size: 8 bits

Offset: 0x3028

Bits	Name	Attr	Description
7	nack_pol	R/W	Not acknowledge error interrupt polarity configuration Value After Reset: 0x1
6	nack_mask	R/W	Not acknowledge error interrupt mask signal Value After Reset: 0x0
5	nack_interrupt	R	Not acknowledge error interrupt bit. Only lasts for one SFR clock cycle and is auto cleared after it. {nack_interrupt = (nack_mask==0b) && (nack_status==nack_pol)}. Note: This bit field is read by the sticky bits present on the ih_i2cmphy_stat0 register. Value After Reset: 0x0
4	nack_status	R	Not acknowledge error status bit. Error on I2C not acknowledge. Note: This bit field is read by the sticky bits present on the ih_i2cmphy_stat0 register. Value After Reset: 0x0
3	arbitration_p ol	R/W	Arbitration error interrupt polarity configuration. Value After Reset: 0x1
2	arbitration_ mask	R/W	Arbitration error interrupt mask signal. Value After Reset: 0x0
1	arbitration_in	R	Arbitration error interrupt bit

Bits	Name	Attr	Description
	terrupt		{arbitration_interrupt = (arbitration_mask==0b) && (arbitration_status==arbitration_pol)} Note: This bit field is read by the sticky bits present on the ih_i2cmphy_stat0 register. Value After Reset: 0x0

Table 9-6 Fields for Register: phy_i2cm_ctlint (Continued)

Bits	Name	Attr	Description
0	arbitration_status	R	Arbitration error status bit. Error on master I2C protocol arbitration. Only lasts for one SFR clock cycle and is auto cleared after it. Note: This bit field is read by the sticky bits present on the ih_i2cmphy_stat0 register. Value After Reset: 0x0

phy_i2cm_div

Description: PHY I2C Speed control Register

This register sets the I2C Master PHY to work in either Fast or Standard mode.

Size: 8 bits

Offset: 0x3029

Bits	Name	Attr	Description
7:4			Reserved for future use.
3	fast_std_mode	R/W	Sets the I2C Master to work in Fast Mode or Standard Mode: 1: Fast Mode 0: Standard Mode Value After Reset: 0x1
2:0	spare	R/W	Reserved as "spare" register with no associated functionality. Value After Reset: 0x3

phy_i2cm_softrstz

Description: PHY I2C SW reset control register

This register sets the I2C Master PHY software reset.

Size: 8 bits

Offset: 0x302a

Bits	Name	Attr	Description
7:1			Reserved for future use.
0	i2c_softrstz	R/W	I2C Master Software Reset. Active by writing a zero and auto cleared to one in the following cycle. Value After Reset: 0x1

phy_i2cm_ss_scl_hcnt_1_addr

Description: PHY I2C Slow Speed SCL High Level Control Register 1

Size: 8 bits

Offset: 0x302b

Bits	Name	Attr	Description
7:0	i2cmp_ss_scl_hcnt1	R/W	PHY I2C Slow Speed SCL High Level Control Register 1 Value After Reset: 0x0

phy_i2cm_ss_scl_hcnt_0_addr

Description: PHY I2C Slow Speed SCL High Level Control Register 0

Size: 8 bits

Offset: 0x302c

Bits	Name	Attr	Description
7:0	i2cmp_ss_scl_hcnt0	R/W	PHY I2C Slow Speed SCL High Level Control Register 0 Value After Reset: 0x6c

phy_i2cm_ss_scl_lcnt_1_addr

Description: PHY I2C Slow Speed SCL Low Level Control Register 1

Size: 8 bits

Offset: 0x302d

Bits	Name	Attr	Description
7:0	i2cmp_ss_scl_lcnt1	R/W	PHY I2C Slow Speed SCL Low Level Control Register 1 Value After Reset: 0x0

phy_i2cm_ss_scl_lcnt_0_addr

Description: PHY I2C Slow Speed SCL Low Level Control Register 0

Size: 8 bits

Offset: 0x302e

Bits	Name	Attr	Description
7:0	i2cmp_ss_scl_lcnt0	R/W	PHY I2C Slow Speed SCL Low Level Control Register 0 Value After Reset: 0x7f

phy_i2cm_fs_scl_hcnt_1_addr

Description: PHY I2C Fast Speed SCL High Level Control Register 1

Size: 8 bits

Offset: 0x302f

Bits	Name	Attr	Description
7:0	i2cmp_fs_scl_hcnt1	R/W	PHY I2C Fast Speed SCL High Level Control Register 1 Value After Reset: 0x0

phy_i2cm_fs_scl_hcnt_0_addr

Description: PHY I2C Fast Speed SCL High Level Control Register 0

Size: 8 bits

Offset: 0x3030

Bits	Name	Attr	Description
7:0	i2cmp_fs_scl_hcnt0	R/W	PHY I2C Fast Speed SCL High Level Control Register 0 Value After Reset: 0x11

phy_i2cm_fs_scl_lcnt_1_addr

Description: PHY I2C Fast Speed SCL Low Level Control Register 1

Size: 8 bits

Offset: 0x3031

Bits	Name	Attr	Description
7:0	i2cmp_fs_scl_lcnt1	R/W	PHY I2C Fast Speed SCL Low Level Control Register 1 Value After Reset: 0x0

phy_i2cm_fs_scl_lcnt_0_addr

Description: PHY I2C Fast Speed SCL Low Level Control Register 0

Size: 8 bits

Offset: 0x3032

Bits	Name	Attr	Description
7:0	i2cmp_fs_scl	R/W	PHY I2C Fast Speed SCL Low Level Control

	-lcnt0		Register 0 Value After Reset: 0x24
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phy_i2cm_sda_hold

Description: PHY I2C SDA HOLD Control Register

Size: 8 bits

Offset: 0x3033

Bits	Name	Attr	Description
7:0	osda_hold	R/W	Defines the number of SFR clock cycles to meet thD:DAT (300 ns) osda_hold = round_to_high_integer (300 ns / (1/ isfrclk_frequency)) Value After Reset: 0x9

AudioSample Registers

Audio Sample Registers. Follow the link for the register to see a detailed description of the register.

Registers for Address Block: AudioSample

Register	Offset	Description
aud_conf0	0x3100	Audio I2S Software FIFO Reset, Select, and Enable Control Register 0 This register configures the...
aud_conf1	0x3101	Audio I2S Width Configuration Register 1 This register configures the data width of the input...
aud_int	0x3102	I2S FIFO status and interrupts. This register configures the I2S FIFO status and interrupts.
aud_conf2	0x3103	Audio I2S PCUV, NLPCM and HBR configuration Register 2 This register configures the I2S Audio Data...
aud_int1	0x3104	I2S Mask Interrupt Register This register masks the interrupts present in the I2S module.

aud_conf0

Description: Audio I2S Software FIFO Reset, Select, and Enable Control Register 0

This register configures the I2S input enable that indicates which input I2S channels have valid data. It also allows the system processor to reset audio FIFOs upon underflow/overflow error detection.

Size: 8 bits

Offset: 0x3100

Bits	Name	Attr	Description
7	sw_audio_fifo_RST	R/W	Audio FIFOs software reset Writing 0b: no action taken Writing 1b: Resets all audio FIFOs Reading from this register always returns 0b. Note: If a FIFO reset request (via SFR command) lands in the middle of an I2S transaction, the samples become misaligned (left-right sequence lost). As a solution, for each FIFO reset, an associated I2S reset must be issued (writing 8'hF7 to MC_SWRSTZ register). Value After Reset: 0x0
6	spare_2	R/W	Reserved as "spare" bit with no associated functionality. Value After Reset: 0x0
5	i2s_select	R/W	1b: Selects I2S Audio Interface 0b: Selects the second (SPDIF/GPA) interface, in configurations with more than

Bits	Name	Attr	Description
			one audio interface (DOUBLE/GDOUBLE) Value After Reset: 0x1
4	spare_1	R/W	Reserved as "spare" bit with no associated functionality. Value After Reset: 0x0
3:0	I2S_in_en	R/W	Action I2S_in_en[0] - I2Sdata[0] enable I2S_in_en[1] - I2Sdata[1] enable I2S_in_en[2] - I2Sdata[2] enable I2S_in_en[3] - I2Sdata[3] enable Value After Reset: 0xf

aud_conf1

Description: Audio I2S Width Configuration Register 1 This register configures the data width of the input data.

Size: 8 bits

Offset: 0x3101

Bits	Name	Attr	Description
7:5			Reserved for future use.
4:0	I2S_width	R/W	I2S input data width I2S_width[4:0] Action 00000b-01111b Not used 10000b 16 bit data samples at input 10001b 17 bit data samples at input 10010b 18 bit data samples at input 10011b 19 bit data samples at input 10100b 20 bit data samples at input 10101b 21 bit data samples at input 10110b 22 bit data samples at input 10111b 23 bit data samples at input 11000b 24 bit data samples at input 11001b-11111b Not Used Value After Reset: 0x18

aud_int

Description: I2S FIFO status and interrupts.

This register configures the I2S FIFO status and interrupts.

Size: 8 bits

Offset: 0x3102

Bits	Name	Attr	Description
7:4			Reserved for future use.
3	fifo_empty_mask	R/W	FIFO empty mask. Value After Reset: 0x0
2	fifo_full_ma-sk	R/W	FIFO full mask. Value After Reset: 0x0
1:0			Reserved for future use.

aud_conf2

Description: Audio I2S PCUV, NLPCM and HBR configuration Register 2

This register configures the I2S Audio Data mapping. By default, audio data mapping is the standard I2S Linear PCM (L-PCM) mapping. You can choose to use the I2S interface to transport HBR or Non- Linear PCM (NL-PCM) audio, by setting the relevant bit in this register.

Size: 8 bits

Offset: 0x3103

Bits	Name	Attr	Description
7:3			Reserved for future use.
2	insert_pcuv	R/W	When set (1'b1), this bit enables the insertion of the PCUV (Parity, Channel Status, User bit and Validity) bits on the incoming audio stream (support limited to Linear

			PCM audio). If disabled, the incoming audio stream must contain the PCUV bits, mapped according to Databook. Value After Reset: 0x1
1	NLPCM	R/W	I2S NLPCM Mode Enable. When enabled, this bit assumes that PCUV data is included on the I2S audio stream according to the description located in the "I2S Interface" section of Chapter 2, "Functional Description." Value After Reset: 0x0
0	HBR	R/W	I2S HBR Mode Enable. When enabled, the I2S audio stream is transmitted using HBR packets. Value After Reset: 0x0

aud_int1

Description: I2S Mask Interrupt Register

This register masks the interrupts present in the I2S module.

Size: 8 bits

Offset: 0x3104

Bits	Name	Attr	Description
7:5			Reserved for future use.
4	fifo_overrun_mask	R/W	FIFO overrun mask Value After Reset: 0x1
3:0			Reserved for future use.

AudioPacketizer Registers

Audio Packetizer Registers. Follow the link for the register to see a detailed description of the register.

Registers for Address Block: AudioPacketizer

Register	Offset	Description
aud_n1	0x3200	Audio Clock Regenerator N Value Register 1 For N expected values, refer to the HDMI 1.4b...
aud_n2	0x3201	Audio Clock Regenerator N Value Register 2 For N expected values, refer to the HDMI 1.4b...
aud_n3	0x3202	Audio Clock Regenerator N Value Register 3 For N expected values, refer to the HDMI 1.4b...
aud_cts1	0x3203	Audio Clock Regenerator CTS Value Register 1 For CTS expected values, refer to the HDMI 1.4b...
aud_cts2	0x3204	Audio Clock Regenerator CTS Register 2 For CTS expected values, refer to the HDMI 1.4b...
aud_cts3	0x3205	Audio Clock Regenerator CTS value Register 3. For CTS expected values, refer to the HDMI 1.4b...
aud_inputclkfs	0x3206	Audio Input Clock FS Factor Register

aud_n1

Description: Audio Clock Regenerator N Value Register 1 For N expected values, refer to the HDMI 1.4b specification.

Size: 8 bits

Offset: 0x3200

Bits	Name	Attr	Description
7:0	AudN	R/W	HDMI Audio Clock Regenerator N value Value After Reset: 0x0

aud_n2

Description: Audio Clock Regenerator N Value Register 2 For N expected values, refer to the HDMI 1.4b specification.

Size: 8 bits

Offset: 0x3201

Bits	Name	Attr	Description
7:0	AudN	R/W	HDMI Audio Clock Regenerator N value Value After Reset: 0x0

aud_n3

Description: Audio Clock Regenerator N Value Register 3 For N expected values, refer to the HDMI 1.4b specification.

Size: 8 bits

Offset: 0x3202

Bits	Name	Attr	Description
7	ncts_atomic_write	R/W	When set, the new N and CTS values are only used when aud_n1 register is written. If clear, N and CTS data is updated each time a new N or CTS byte is written. The following write sequence is recommended: aud_n3 (set bit ncts_atomic_write if desired) aud_cts3 (set CTS_manual and CTS value if desired/enabled) aud_cts2 (required in CTS_manual) aud_cts1 (required in CTS_manual) aud_n3 (bit ncts_atomic_write with same value as in step 1.) aud_n2 aud_n1 For dynamic N/CTS changes, perform only steps from 2-7 or 5-7 depending on the state of CTS_manual. Value After Reset: 0x0
6:4			Reserved for future use.
3:0	AudN	R/W	HDMI Audio Clock Regenerator N value Value After Reset: 0x0

aud_cts1

Description: Audio Clock Regenerator CTS Value Register 1 For CTS expected values, refer to the HDMI 1.4b specification.

Size: 8 bits

Offset: 0x3203

Bits	Name	Attr	Description
7:0	AudCTS	R/W	HDMI Audio Clock Regenerator CTS calculated value. This value can be manually set using the CTS_manual (AUD_CTS3) mechanism. Value After Reset: 0x0

aud_cts2

Description: Audio Clock Regenerator CTS Register 2

For CTS expected values, refer to the HDMI 1.4b specification.

Size: 8 bits

Offset: 0x3204

Bits	Name	Attr	Description
7:0	AudCTS	R/W	HDMI Audio Clock Regenerator CTS calculated value. This value can be manually set using the CTS_manual (AUD_CTS3) mechanism.

		Value After Reset: 0x0
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aud_cts3

Description: Audio Clock Regenerator CTS value Register 3. For CTS expected values, refer to the HDMI 1.4b specification.

Size: 8 bits

Offset: 0x3205

Bits	Name	Attr	Description
7:5	Spare_bits	R/W	Reserved as "spare" bits with no associated functionality. Value After Reset: 0x0
4	CTS_manual	R/W	If the CTS_manual bit equals 0b, this register contains audCTS[19:0] generated by the Cycle time counter according to the specified timing. If the CTS_manual bit equals 1b, this register is configured with the audCTS[7:0] value that is output by the Audio Packetizer. Note: When the General Parallel Audio Interface (GPAUD) is enabled (AUDIO_IF = 6) or the AHB DMA Audio Interface is enabled (AUDIO_IF = 8), writing to these bits has no effect; reading these bits always return 0. Value After Reset: 0x0
3:0	AudCTS	R/W	HDMI Audio Clock Regenerator CTS calculated value. This value can be manually set using the CTS_manual (AUD_CTS3) mechanism. Value After Reset: 0x0

aud_inputclkfs

Description: Audio Input Clock FS Factor Register

Size: 8 bits

Offset: 0x3206

Bits	Name	Attr	Description
7:3			Reserved for future use.
2:0	ifsfactor	R/W	Fs factor configuration: ifsfactor[2:0] Audio Clock Action 0 128xFs If you select the Bypass SPDIF DRU unit in coreConsultant, the input audio clock (either I2S or SPDIF according to configuration) is used at the audio packetizer to calculate the CTS value and ACR packet insertion rate. 256xFs The input audio clock (I2S only) is divided by 2 and then used at audio packetizer to calculate the CTS value and ACR packet insertion rate. 512xFs The input audio clock (either I2S or SPDIF according to configuration) used divided by 4 and then used at the audio packetizer to calculate the CTS value and ACR packet insertion rate. Note: When the SPDIF interface is receiving an HBR audio stream ("Support for HBR over SDPFI" parameter must be enabled), it is required that the selected IFSFACTOR to be set at 512xFs in order to comply with the HDMI ACR requirements for HBR audio streams. Reserved 64xFs The input audio clock (I2S only) is multiplied by 2 and then used at the audio packetizer to calculate the CTS value and ACR packet insertion rate. others 128xFs If you select the Bypass SPDIF DRU unit in coreConsultant, the input audio clock (either

Bits	Name	Attr	Description
			I2S or SPDIF according to configuration) is used at the audio packetizer to calculate the CTS value and ACR packet insertion rate. The SPDIF interface, for non HBR audio, requires that the configured oversampling value to be 128xFs when HTX_SPDIFBYPDRU is enabled and 512xFs if not. When the SPDIF interface is receiving HBR audio (HBR_ON_SPDIF must be enabled), in order to comply with the HDMI ACR requirements for HBR audio streams. Value After Reset: 0x0

AudioSampleSPDIF Registers

Audio Sample SPDIF Registers. Follow the link for the register to see a detailed description of the register.

Registers for Address Block: AudioSampleSPDIF

Register	Offset	Description
aud_spdif0	0x3300	Audio SPDIF Software FIFO Reset Control Register 0 This register allows the system processor to...
aud_spdif1	0x3301	Audio SPDIF NLPCM and Width Configuration Register 1 This register configures the SPDIF data...
aud_spdifint	0x3302	Audio SPDIF FIFO Empty/Full Mask Register
aud_spdifint1	0x3303	Audio SPDIF Mask Interrupt Register 1 This register masks interrupts present in the SPDIF...

aud_spdif0

Description: Audio SPDIF Software FIFO Reset Control Register 0

This register allows the system processor to reset audio FIFOs upon underflow/overflow error detection.

Size: 8 bits

Offset: 0x3300

Bits	Name	Attr	Description
7	sw_audio_fifo_RST	R/W	Audio FIFOs software reset Writing 0b: no action taken Writing 1b: Resets all audio FIFOs Reading from this register always returns 0b. Note: If a FIFO reset request (via register write command) lands in the middle of an SPDIF audio transaction, the samples become misaligned (left-right sequence lost). As a solution, for each FIFO reset, an associated SPDIF reset must be issued (writing 8'hEF to MC_SWRSTZ register). Value After Reset: 0x0
6:0	spare	R/W	Reserved as "spare" bit with no associated functionality. Value After Reset: 0xf

aud_spdif1

Description: Audio SPDIF NLPCM and Width Configuration Register 1 This register configures the SPDIF data width.

Size: 8 bits

Offset: 0x3301

Bits	Name	Attr	Description
7	setnlpcm	R/W	Select Non-Linear (1b) / Linear (0b) PCM mode Value After Reset: 0x0
6	spdif_hbr_mode	R/W	When set to 1'b1, this bit field indicates that the input stream has a High Bit Rate (HBR) to be transmitted in HDMI HBR packets. When clear (1b'0), the audio is transmitted in HDMI AUDS packets. Note: < Otherwise, this field is a "spare" bit with no associated functionality.

aud_spdifint

Description: Audio SPDIF FIFO Empty/Full Mask Register

Size: 8 bits

Offset: 0x3302

Bits	Name	Attr	Description
7:4			Reserved for future use.
3	spdif_fifo_empty_mask	R/W	Description: SPDIF FIFO empty mask Value After Reset: 0x0
2	spdif_fifo_full_mask	R/W	Description: SPDIF FIFO full mask Value After Reset: 0x0
1:0			Reserved for future use.

aud_spdifint1

Description: Audio SPDIF Mask Interrupt Register 1

This register masks interrupts present in the SPDIF module.

Size: 8 bits

Offset: 0x3303

Bits	Name	Attr	Description
7:5			Reserved for future use.
4	fifo_overrun_mask	R/W	FIFO overrun mask Value After Reset: 0x1
3:0			Reserved for future use.

AudioSampleGP Registers

Audio Sample GP Registers. Follow the link for the register to see a detailed description of the register.

Register	Offset	Description
gp_conf0	0x3500	Audio GPA Software FIFO Reset Control Register 0
gp_conf1	0x3501	Audio GPA Channel Enable Configuration Register 1
gp_conf2	0x3502	Audio GPA HBR Enable Register 2
gp_mask	0x3506	Audio GPA FIFO Full and Empty Mask Interrupt Register

gp_conf0

Description: Audio GPA Software FIFO Reset Control Register 0

Size: 8 bits

Offset: 0x3500

Bits	Name	Attr	Description
7:1			Reserved for future use.
0	sw_audio_fifo_RST	R/W	Audio FIFOs software reset Writing 0b: no action taken Writing 1b: Resets all audio FIFOs Reading from this register always returns 0b.

Bits	Name	Attr	Description
			<p>Note: If a FIFO reset request (via register write command) lands in the middle of an GPAUD audio transaction, the samples become misaligned (left-right sequence lost). As a solution, for each FIFO reset, an associated SPDIF reset must be issued (writing 8'h7F to MC_SWRSTZ register).</p> <p>Value After Reset: 0x0</p>

gp_conf1

Description: Audio GPA Channel Enable Configuration Register 1

Size: 8 bits

Offset: 0x3501

Bits	Name	Attr	Description
7:0	ch_in_en	R/W	<p>Each bit controls the enabling of the respective audio channel. For instance, bit 1, when set (1'b1), the audio Channel 1 is enabled. When cleared, the referred channel is disabled.</p> <p>Value After Reset: 0x0</p>

gp_conf2

Description: Audio GPA HBR Enable Register 2

Size: 8 bits

Offset: 0x3502

Bits	Name	Attr	Description
7:2			Reserved for future use.
1	insert_pcu_v	R/W	<p>When set (1'b1), this bit enables the insertion of the PCUV (Parity, Channel Status, User bit and Validity) bits on the incoming audio stream (support limited to Linear PCM audio). If disabled, the incoming audio stream must contain the PCUV bits, mapped according to 2.6.4.2 Data Mapping Examples.</p> <p>Value After Reset: 0x0</p>
0	HBR	R/W	<p>HBR packets enable. The Hdmi_tx sends the HBR packets. This bit is enabled when the audio frequency is higher than 192 kHz. If this bit is enabled, the number of channels configured in GP_CONF1 must be set to 8'hFF.</p> <p>Value After Reset: 0x0</p>

gp_mask

Description: Audio GPA FIFO Full and Empty Mask Interrupt Register

Size: 8 bits

Offset: 0x3506

Bits	Name	Attr	Description
7:5			Reserved for future use.
4	fifo_overrun_mask	R/W	FIFO overrun mask Value After Reset: 0x1
3:2			Reserved for future use.
1	fifo_empty_mask	R/W	FIFO empty flag mask Value After Reset: 0x0
0	fifo_full_mask	R/W	FIFO full flag mask Value After Reset: 0x0

AudioDMA Registers

Audio DMA Registers. Follow the link for the register to see a detailed description of the register.

Register	Offset	Description
ahb_dma_conf0	0x3600	Audio DMA SW FIFO reset and DMA Configuration Register 0 This register contains the software reset...
ahb_dma_start	0x3601	Audio DMA Start Register The start_dma_transaction bit field signals the AHB audio DMA to start...
ahb_dma_stop	0x3602	Audio DMA Stop Register The stop_dma_transaction bit field signals the AHB audio DMA to stop current...
ahb_dma_thrsld	0x3603	Audio DMA FIFO Threshold Register This register defines the FIFO medium threshold occupation value....
ahb_dma_straddr_set0[0:3]	0x3604 + (i * 0x1)	Audio DMA Start Address Set0 Register Array Address offset: i = 0 to 3 These registers define...
ahb_dma_stpaddr_set0[0:3]	0x3608 + (i * 0x1)	Audio DMA Stop Address Set0 Register Array Address offset: i = 0 to 3 This registers define the...
ahb_dma_bstraddr[0:3]	0x360c + (i * 0x1)	Audio DMA Burst Start Address Register Array Address offset: i = 0 to 3 These read-only registers...
ahb_dma_mblength0	0x3610	Audio DMA Burst Length Register 0 This registers holds the length of the current burst operation....
ahb_dma_mblength	0x3611	Audio DMA Burst Length Register 1 This registers holds the length of the current burst operation....
ahb_dma_mask	0x3614	Audio DMA Mask Interrupt Register This register masks each of the interrupts present in the AHB...
ahb_dma_conf	0x3616	Audio DMA Channel Enable Configuration Register 1 In AUDS packet configuration with layout 0 selected,...
ahb_dma_buffmask	0x3619	Audio DMA Buffer Mask Interrupt Register
ahb_dma_mask1	0x361b	Audio DMA Mask Interrupt Register 1 This register masks interrupts present in the AHB audio DMA...
ahb_dma_status	0x361c	Audio DMA Status
ahb_dma_conf2	0x361d	Audio DMA Configuration Register 2
ahb_dma_straddr_set1[0:3]	0x3620 + (i * 0x1)	Audio DMA Start Address Set 1 Register Array Address offset: i = 0 to 3 These registers define...
ahb_dma_stpaddr_set1[0:3]	0x3624 + (i * 0x1)	Audio DMA Stop Address Set 1 Register Array Address offset: i = 0 to 3 These registers define...

ahb_dma_conf0

Description: Audio DMA SW FIFO reset and DMA Configuration Register 0

This register contains the software reset bit for the audio FIFOs. It also configures operating modes of the AHB master.

Size: 8 bits

Offset: 0x3600

Bit S	Name	Attr	Description
7	sw_fifo_RST	R/W	This is the software reset bit for the audio and FIFO clear. Writing 0'b does not result in any action. Writing 1'b to this register resets all audio FIFOs. Reading from this register always returns 0'b. Value After Reset: 0x0
6	insert_pcuV	R/W	Enables the insertion of PCUV data Value After Reset: 0x0
5			Reserved for future use.
4	hbr	R/W	HBR packet enable The Hdmi_tx sends the HBR packets. This bit must be enabled when transmitting non-linear audio of frequency higher than 192 kHz. If this bit is enabled, the number of channels configured in AHB_DMA_CONF1 is always 8. Value After Reset: 0x0
3	enable_hlock	R/W	Enable request of locked burst AHB mechanism. 1'b: Enables the usage of hlock for master request to arbiter of a locked complete burst. 0'b: Disables request of locked burst AHB mechanism Value After Reset: 0x0
2:1	incr_type	R/W	Selects the preferred burst length size 00'b: Corresponds to INCR4 fixed four beat, incremental AHB burst mode. Only valid when burst_mode is high. 01'b: Corresponds to INCR8 fixed eight beat incremental AHB burst mode. Only valid when burst_mode is high. 10'b: Corresponds to INCR16 fixed 16 beat incremental AHB burst mode. Only valid when burst_mode is high. 11'b: Corresponds to INCR16 fixed 16 beat incremental AHB burst mode. Only valid when burst_mode is high. Value After Reset: 0x0
0	burst_mode	R/W	1'b: Forces the burst mode to be fixed beat, incremental burst mode designated by the incr_type[1:0] signal. 0'b: Normal operation is unspecified length, incremental burst. It corresponds to INCR AHB burst mode. Value After Reset: 0x0

ahb_dma_start

Description: Audio DMA Start Register

The start_dma_transaction bit field signals the AHB audio DMA to start accessing system memory in order to fetch data samples to store in the FIFO. After the operation starts, a new request for a DMA start is ignored until the DMA is stopped or it reaches the end address. Only in one of these situations is a new start request acknowledged.

The first DMA burst request after start_dma_transaction configuration uses initial_addr[31:0]

as ohaddr[31:0] value; mburstlength[8:0] is set to the maximum admissible value. This maximum value is constrained by the size of buffer provided, the instantiated FIFO depth, or/and the number of words up to the next 1 Kbyte boundary.

Size: 8 bits

Offset: 0x3601

Bit s	Name	Attr	Description
7:1			Reserved for future use.
0	start_dma_transaction	R/W	Start DMA transaction This register is auto-cleared when the transfer operation is completed (done). Value After Reset: 0x0

ahb_dma_stop

Description: Audio DMA Stop Register

The stop_dma_transaction bit field signals the AHB audio DMA to stop current Attr. After it stops, if a new start DMA operation is requested, the DMA engine restarts the Attr using the initial_addr[31:0], which is programmed at ahb_dma_straddr0 to ahb_dma_straddr3.

Size: 8 bits

Offset: 0x3602

Bits	Name	Attr	Description
7:1			Reserved for future use.
0	stop_dma_transaction	R/W	Stop DMA transaction This register is auto-cleared when the transfer operation is stopped (done). Value After Reset: 0x0

ahb_dma_thrsld

Description: Audio DMA FIFO Threshold Register

This register defines the FIFO medium threshold occupation value.

After the AHB master completes a burst transaction successfully, the FIFO may remain full till the data fetch interface requests samples. Each data fetch operation reduces the number of samples stored in the FIFO by the number of channels enabled.

Therefore, the fifo_threshold[7:0] is the medium number of samples that should be available in the audio FIFO across the DMA operation.

As soon as the number of samples in the FIFO drops lower than the fifo_threshold[7:0], the DMA engine requests a new burst of samples for the AHB master. The length is constrained by the size of buffer provided, the instantiated FIFO depth minus fifo_threshold[7:0], and/or the number of words up to the next 1 kbyte boundary.

Size: 8 bits

Offset: 0x3603

Bits	Name	Attr	Description
7:0	fifo_threshold	R/W	FIFO medium threshold occupation value Value After Reset: 0x0

ahb_dma_straddr_set0[0:3]

Description: Audio DMA Start Address Set0 Register Array Address offset: i = 0 to 3

These registers define the initial_addr[31:0] used to initiate the DMA burst read transactions upon start_dma_transaction configuration.

Size: 8 bits

Offset: 0x3604 + (i * 0x1)

Bits	Name	Attr	Description
7:0	initial_addr	R/W	Defines init_addr[7:0] to initiate DMA burst transactions Value After Reset: 0x0

ahb_dma_stpaddr_set0[0:3]

Description: Audio DMA Stop Address Set0 Register Array Address offset: i = 0 to 3

This registers define the final_addr[31:0] used as the final point to the DMA burst read transactions.

Upon start_dma_transaction configuration, the DMA engine starts requesting burst reads from the external system memory. Each burst read can have a maximum theoretical length of 256 words (due to the AMBA AHB specification 1 Kbyte boundary burst limitation).

The DMA engine is responsible for incrementing the burst starting address and defining its corresponding burst length to reach the final_addr[31:0] address. The last burst request issued by the DMA engine takes into account that it should only request data until the final_addr[31:0] address (included) and for that should calculate the correct burst length.

After reaching the final_addr[31:0] address, the done interrupt is active to signal completion of DMA operation.

Size: 8 bits

Offset: 0x3608 + (i * 0x1)

Bits	Name	Attr	Description
7:0	final_addr	R/W	Defines final_addr[7:0] to end DMA burst transactions Value After Reset: 0x0

ahb_dma_bstraddr[0:3]

Description: Audio DMA Burst Start Address Register Array Address offset: i = 0 to 3

These read-only registers compose the start address of the current burst operation.

burst_start_addr[31:0] = haddr[31:0] = initial_addr[31:0] + 16.

Size: 8 bits

Offset: 0x360c + (i * 0x1)

Bits	Name	Attr	Description
7:0	burst_addr	R	Start address for the current burst operation Value After Reset: 0x0

ahb_dma_mblength0

Description: Audio DMA Burst Length Register 0

This registers holds the length of the current burst operation. As an example, if the first burst transaction of the AHB audio DMA is a length of 8, then the second burst should start at address ohaddr[31:0] = initial_addr[31:0] + 32.

Size: 8 bits

Offset: 0x3610

Bits	Name	Attr	Description
7:0	mburstlength	R	Requested burst length (mburstlength[7:0]) Value After Reset: 0x0

ahb_dma_mblength1

Description: Audio DMA Burst Length Register 1

This registers holds the length of the current burst operation. As an example, if the first burst transaction of the AHB audio DMA is a length of 8, then the second burst should start at address ohaddr[31:0] = initial_addr[31:0] + 32.

Size: 8 bits

Offset: 0x3611

Bits	Name	Attr	Description
7:1			Reserved for future use.
0	mburstlength	R	Requested burst length Value After Reset: 0x0

ahb_dma_mask

Description: Audio DMA Mask Interrupt Register

This register masks each of the interrupts present in the AHB audio DMA module.

Size: 8 bits

Offset: 0x3614

Bits	Name	Attr	Description
7	done_mask	R/W	DMA end of operation interrupt mask. Active when DMA engine reaches final_addr[15:0] or when stop DMA operation is activated. Value After Reset: 0x1
6	retrysplit_mask	R/W	Retry/split interrupt mask. Active when AHB master receives a RETRY or SPLIT response from slave. Value After Reset: 0x1
5	lostownership_mask	R/W	Master lost ownership interrupt mask when in burst transfer. Active when AHB master loses BUS ownership within the course of a burst transfer. Value After Reset: 0x1
4	error_mask	R/W	Error interrupt mask. Active when slave indicates error through the isresp[1:0]. Value After Reset: 0x1
3			Reserved for future use.
2	fifo_thremptry_mask	R/W	Audio FIFO empty interrupt mask when audio FIFO has less than the number of enabled audio channels. Value After Reset: 0x1
1	fifo_full_mask	R/W	Audio FIFO full interrupt mask. Value After Reset: 0x1
0	fifo_empty_mask	R/W	Audio FIFO empty interrupt mask. Value After Reset: 0x1

ahb_dma_conf1

Description: Audio DMA Channel Enable Configuration Register 1

In AUDS packet configuration with layout 0 selected, the maximum number of active channels is 2.

Size: 8 bits

Offset: 0x3616

Bits	Name	Attr	Description
7:0	ch_in_en	R/W	Each bit controls the enabling of the respective audio channel. For instance, when bit 1 is set (1'b1) the audio Channel 1 is enabled. When cleared, the referred channel is disabled. Value After Reset: 0x0

ahb_dma_buffmask

Description: Audio DMA Buffer Mask Interrupt Register

Size: 8 bits

Offset: 0x3619

Bit s	Name	Attr	Description
7:5			Reserved for future use.
4	mask_fifo_overrun	R/W	Buffer overrun flag mask Value After Reset: 0x1
3:2			Reserved for future use.
1	mask_buff_full	R/W	Buffer full flag mask Value After Reset: 0x1
0	mask_buff_empty	R/W	Buffer empty flag mask Value After Reset: 0x1

ahb_dma_mask1

Description: Audio DMA Mask Interrupt Register 1

This register masks interrupts present in the AHB audio DMA module.

Size: 8 bits

Offset: 0x361b

Bit s	Name	Attr	Description
7:2			Reserved for future use.
1	fifo_underrun_ _mask	R/W	AHB DMA FIFO underrun mask Value After Reset: 0x1
0	fifo_overrun_ _mask	R/W	AHB DMA FIFO overrun mask Value After Reset: 0x1

ahb_dma_status

Description: Audio DMA Status

Size: 8 bits

Offset: 0x361c

Bit s	Name	Attr	Description
7:1			Reserved for future use.
0	autostart_stau tus	R	Indicates the set of start and stop addresses currently used by the AHB audio DMA. If cleared (1'b0), the start and stop addresses configured in the address range 0x3604 to 0x360B are being used. When set (1'b1), the configurations at address range 0x3620 to 0x3627 are being used. This bit is always at zero when autostart_enable is cleared (1'b0). Value After Reset: 0x0

ahb_dma_conf2

Description: Audio DMA Configuration Register 2

Size: 8 bits

Offset: 0x361d

Bit s	Name	Attr	Description
7:2			Reserved for future use.
1	autostart_loo p	R/W	Enables the AHB audio DMA auto-start loop mode Value After Reset: 0x1
0	autostart_en able	R/W	Enables the AHB audio DMA auto-start feature Value After Reset: 0x0

ahb_dma_straddr_set1[0:3]

Description: Audio DMA Start Address Set 1 Register Array Address offset: i = 0 to 3

These registers define the initial_addr_1[31:0] used to initiate the DMA burst read transactions upon start_dma_transaction configuration.

Size: 8 bits

Offset: 0x3620 + (i * 0x1)

Bit s	Name	Attr	Description
7:0	initial_addr_1	R/W	Defines init_addr_1[7:0] to initiate DMA burst transactions Value After Reset: 0x0

ahb_dma_stpaddr_set1[0:3]

Description: Audio DMA Stop Address Set 1 Register Array Address offset: i = 0 to 3

These registers define the final_addr_1[31:0] used as the final point to the DMA burst read transactions. Upon start_dma_transaction configuration, the DMA engine starts requesting burst reads from the external system memory. Each burst read can have a maximum theoretical length of 256 words (due to the AMBA AHB specification 1 Kbyte boundary burst limitation).

The DMA engine is responsible for incrementing the burst starting address and defining its corresponding burst length to reach the final_addr[31:0] address. The last burst request issued by the DMA engine takes into account that it should only request data until the final_addr[31:0] address (included) and for that should calculate the correct burst length. After reaching the final_addr_1[31:0] address, the done interrupt is active to indicate completion of the DMA operation.

Size: 8 bits

Offset: 0x3624 + (i * 0x1)

Bit s	Name	Attr	Description
7:0	final_addr_1	R/W	Defines final_addr_1[7:0] to end DMA burst transactions Value After Reset: 0x0

MainController Registers

Main Controller Registers. Follow the link for the register to see a detailed description of the register.

Register	Offset	Description
mc_clkdis	0x4001	Main Controller Synchronous Clock Domain Disable Register
mc_swrtzreq	0x4002	Main Controller Software Reset Register Main controller software reset request per clock domain....
mc_opctrl	0x4003	Main Controller HDCP Bypass Control Register
mc_flowctrl	0x4004	Main Controller Feed Through Control Register
mc_phyrstz	0x4005	Main Controller PHY Reset Register
mc_lockonclock	0x4006	Main Controller Clock Present Register
mc_heacphy_rst	0x4007	Main Controller HEAC PHY Reset Register
mc_lockonclock_2	0x4009	Main Controller Clock Present Register 2
mc_swrtzreq_2	0x400a	Main Controller Software Reset Register 2 Main controller software reset request per clock domain....

mc_clkdis

Description: Main Controller Synchronous Clock Domain Disable Register

Size: 8 bits

Offset: 0x4001

Bits	Name	Attr	Description
7	h22sclk_disable	R/W	HDCP22 clock synchronous disable signal. When active (1b), simultaneously bypasses HDCP22. Value After Reset: 0x0
6	hdcpclk_disable	R/W	HDCP clock synchronous disable signal. When active (1b), simultaneously bypasses HDCP. Value After Reset: 0x0
5	cecclk_disable	R/W	CEC Engine clock synchronous disable signal. Value After Reset: 0x0

Bits	Name	Attr	Description
4	cscclk_disable	R/W	Color Space Converter clock synchronous disable signal. Value After Reset: 0x0
3	audclk_disable	R/W	Audio Sampler clock synchronous disable signal. Value After Reset: 0x0
2	prepclk_disable	R/W	Pixel Repetition clock synchronous disable signal. Value After Reset: 0x0
1	tmdsclk_disable	R/W	TMDS clock synchronous disable signal. It is required to perform a write action on one of the following registers: fc_invidconf, fc_inhactiv0, fc_inhactiv1, fc_inhblank0, fc_inhblank1, fc_invactiv0 fc_invactiv1, fc_invblank, fc_hsyncindelay0, fc_hsyncindelay1, fc_hsyncinwidth0 fc_hsyncinwidth1, fc_vsyncindelay, fc_vsyncinwidth, fc_ctrldur, fc_exctrldur, fc_exctrlspac Value After Reset: 0x0
0	pixelclk_disable	R/W	Pixel clock synchronous disable signal. Value After Reset: 0x0

mc_swrstreq

Description: Main Controller Software Reset Register

Main controller software reset request per clock domain. Writing zero to a bit of this register results in an NRZ signal toggle at sfrclk rate to an output signal that indicates a software reset request. This toggle must be used to generate a synchronized reset to de corresponding domain, with at least 1 clock cycle.

Size: 8 bits

Offset: 0x4002

Bits	Name	Attr	Description
7	igpaswrst_req	R/W	GPAUD interface soft reset request. This bit is enabled when the Generic Parallel Audio (GPAUD) interface is enabled (AUDIO_IF = 6). Otherwise, this bit returns zero. Value After Reset: 0x1
6	cecswrst_req	R/W	CEC software reset request. Defaults back to 1b after reset request. Note: After you configure cecswrst_req, set the value of the bit csc_clk_disable of the register mc_clkd to 1, 0, and then 1 again. Value After Reset: 0x1
5			Reserved for future use.
4	ispdifswrst_req	R/W	SPDIF audio software reset request. Value After Reset: 0x1
3	ii2sswrst_req	R/W	I2S audio software reset request. Value After Reset: 0x1
2	prepswrst_req	R/W	Pixel Repetition software reset request. Value After Reset: 0x1
1	tmdsswrst_req	R/W	TMDS software reset request. It is required to perform a write action on one of the following registers: fc_invidconf, fc_inhactiv0, fc_inhactiv1, fc_inhblank0, fc_inhblank1, fc_invactiv0 fc_invactiv1, fc_invblank, fc_hsyncindelay0, fc_hsyncindelay1, fc_hsyncinwidth0 fc_hsyncinwidth1, fc_vsyncindelay, fc_vsyncinwidth,

Bits	Name	Attr	Description
			fc_ctrldur, fc_exctrldur, fc_exctrlspac Value After Reset: 0x1
0	pixelswrst_req	R/W	Pixel software reset request. Value After Reset: 0x1

mc_opctrl

Description: Main Controller HDCP Bypass Control Register

Size: 8 bits

Offset: 0x4003

Bits	Name	Attr	Description
7:6			Reserved for future use.
5	h22s_ovr_val	R/W	HDCP SNPS 2.2 versus 1.4 switch override value 1'b0: The switch is routed to HDCP 1.4 signals when hdcp22snps_switch_lock is not set to 1'b1. 1'b1: The switch is routed to HDCP 2.2 SNPS signals when hdcp22snps_switch_lock is not set to 1'b1. Value After Reset: 0x1
4	h22s_switch_lck	R/W	HDCP 2.2 SNPS switch lock 1'b0: Enables you to change the direction of the HDCP 2.2 SNPS versus 1.4 switch by using the hdcp22snps_ovr_val. 1'b1: You can still write to hdcp22snps_ovr_val but has no effect over the HDCP 2.2 SNPS versus 1.4 switch, that keeps as it was configured by hdcp22snps_ovr_val at the time the 1'b1 was written to this bit field. Once you set the value to 1'b1, you can change the value back to 1'b0 only by issuing a master reset to the Hdmi_tx. Value After Reset: 0x0
3:1			Reserved for future use.
0	hdcp_block_byp	R/W	Block HDCP bypass mechanism 1'b0: This is the default value. You can write to the hdcp_clkdisable bit of the register mc_clkdis and bypass HDCP by acting on the register mc_clkdis bit 6 (hdcp_clkdisable) 1'b1: You can still write to the hdcp_clkdisable bit of the register mc_clkdis but this action disables the HDCP module and blocks the bypass mechanism. The output data is frozen and the HDMI Tx and RX fail authentication. Once you set the value to 1'b1, you can change the value back to 1'b0 only by issuing a master reset to the Hdmi_tx. Otherwise, this field is a "spare" bit with no associated functionality. Value After Reset: 0x0

mc_flowctrl

Description: Main Controller Feed Through Control Register

Size: 8 bits

Offset: 0x4004

Bits	Name	Attr	Description
7:1			Reserved for future use.
0	Feed_throu gh_off	R/W	Video path Feed Through enable bit: 1b: Color Space Converter is in the video data path.

Bits	Name	Attr	Description
			0b: Color Space Converter is bypassed (not in the video data path). Value After Reset: 0x0

mc_phyrstz

Description: Main Controller PHY Reset Register

Size: 8 bits

Offset: 0x4005

Bits	Name	Attr	Description
7:1			Reserved for future use.
0	phyrstz	R/W 1C	HDMI Source PHY active low reset control for PHY GEN1, active high reset control for PHY GEN2. Value After Reset: "(PHY_GEN2== 1) ? 1 : 0"

mc_lockonclock

Description: Main Controller Clock Present Register

Size: 8 bits

Offset: 0x4006

Bits	Name	Attr	Description
7	igpackl	R/W 1C	GPAUD interface clock status. This bit is enabled when the Generic Parallel Audio (GPAUD) interface is enabled (AUDIO_IF = 6). Otherwise, this bit returns zero. This bit indicates the clock is present in the system. It is cleared by writing 1 to this bit. Value After Reset: 0x0
6	pclk	R/W 1C	Pixel clock status. Indicates that the clock is present in the system. Cleared by WR 1 to this position. Value After Reset: 0x0
5	tclk	R/W 1C	TMDS clock status. Indicates that the clock is present in the system. Cleared by WR 1 to this position. Value After Reset: 0x0
4	prepclk	R/W 1C	Pixel Repetition clock status. Indicates that the clock is present in the system. Cleared by WR 1 to this position. Value After Reset: 0x0
3	i2sclk	R/W 1C	I2S clock status. Indicates that the clock is present in the system. Cleared by WR 1 to this position. Value After Reset: 0x0
2	audiospdifclk	R/W 1C	SPDIF clock status. Indicates that the clock is present in the system. Cleared by WR 1 to this position. Value After Reset: 0x0
1			Reserved for future use.
0	cecclk	R/W 1C	CEC clock status. Indicates that the clock is present in the system. Cleared by WR 1 to this position. Value After Reset: 0x0

mc_heacphy_rst

Description: Main Controller HEAC PHY Reset Register

Size: 8 bits

Offset: 0x4007

Bits	Name	Attr	Description
7:1			Reserved for future use.
0	heacphyrst	R/W	HEAC PHY reset (active high) Value After Reset: 0x1

mc_lockonclock_2

Description: Main Controller Clock Present Register 2

Size: 8 bits

Offset: 0x4009

Bits	Name	Attr	Description
7:1			Reserved for future use.
0	ahbdmaclk	R/W 1C	AHB audio DMA clock status. Indicates that the clock is present in the system. Cleared by WR 1 to this position. Value After Reset: 0x0

mc_swrtzreq_2

Description: Main Controller Software Reset Register 2

Main controller software reset request per clock domain. Writing zero to a bit of this register results in a signal toggle that indicates a software reset request. This toggle is used to generate a synchronized reset to the corresponding domain, with one or more clock cycles.

Size: 8 bits

Offset: 0x400a

Bits	Name	Attr	Description
7:1			Reserved for future use.
0	ahbdmaswr_st_req	R/W	AHB audio DMA software reset request. Writing 1'b1 does not result in any action. Writing 1'b0 to this register resets all AHB audio logic. Value After Reset: 0x0

ColorSpaceConverter Registers

Color Space Converter Registers Registers. Follow the link for the register to see a detailed description of the register.

Register	Offset	Description
csc_cfg	0x4100	Color Space Converter Interpolation and Decimation Configuration Register
csc_scale	0x4101	Color Space Converter Scale and Deep Color Configuration Register
csc_coef_a1_msb	0x4102	Color Space Converter Matrix A1 Coefficient Register MSB Notes: - The coefficients used in the...
csc_coef_a1_lsb	0x4103	Color Space Converter Matrix A1 Coefficient Register LSB Notes: - The coefficients used in the...
csc_coef_a2_msb	0x4104	Color Space Converter Matrix A2 Coefficient Register MSB Color Space Conversion A2...
csc_coef_a2_lsb	0x4105	Color Space Converter Matrix A2 Coefficient Register LSB Color Space Conversion A2...
csc_coef_a3_msb	0x4106	Color Space Converter Matrix A3 Coefficient Register MSB Color Space Conversion A3...
csc_coef_a3_lsb	0x4107	Color Space Converter Matrix A3 Coefficient Register LSB Color Space Conversion A3...
csc_coef_a4_msb	0x4108	Color Space Converter Matrix A4 Coefficient Register MSB Color Space Conversion A4...

Register	Offset	Description
csc_coef_a4_lsb	0x4109	Color Space Converter Matrix A4 Coefficient Register LSB Color Space Conversion A4...
csc_coef_b1_msb	0x410a	Color Space Converter Matrix B1 Coefficient Register MSB Color Space Conversion B1...
csc_coef_b1_lsb	0x410b	Color Space Converter Matrix B1 Coefficient Register LSB Color Space Conversion B1...
csc_coef_b2_msb	0x410c	Color Space Converter Matrix B2 Coefficient Register MSB Color Space Conversion B2...
csc_coef_b2_lsb	0x410d	Color Space Converter Matrix B2 Coefficient Register LSB Color Space Conversion B2...
csc_coef_b3_msb	0x410e	Color Space Converter Matrix B3 Coefficient Register MSB Color Space Conversion B3...
csc_coef_b3_lsb	0x410f	Color Space Converter Matrix B3 Coefficient Register LSB Color Space Conversion B3...
csc_coef_b4_msb	0x4110	Color Space Converter Matrix B4 Coefficient Register MSB Color Space Conversion B4...

Registers for Address Block: ColorSpaceConverter (Continued)

Register	Offset	Description
csc_coef_b4_lsb	0x4111	Color Space Converter Matrix B4 Coefficient Register LSB Color Space Conversion B4...
csc_coef_c1_msb	0x4112	Color Space Converter Matrix C1 Coefficient Register MSB Color Space Conversion C1...
csc_coef_c1_lsb	0x4113	Color Space Converter Matrix C1 Coefficient Register LSB Color Space Conversion C1...
csc_coef_c2_msb	0x4114	Color Space Converter Matrix C2 Coefficient Register MSB Color Space Conversion C2...
csc_coef_c2_lsb	0x4115	Color Space Converter Matrix C2 Coefficient Register LSB Color Space Conversion C2...
csc_coef_c3_msb	0x4116	Color Space Converter Matrix C3 Coefficient Register MSB Color Space Conversion C3...
csc_coef_c3_lsb	0x4117	Color Space Converter Matrix C3 Coefficient Register LSB Color Space Conversion C3...
csc_coef_c4_msb	0x4118	Color Space Converter Matrix C4 Coefficient Register MSB Color Space Conversion C4...
csc_coef_c4_lsb	0x4119	Color Space Converter Matrix C4 Coefficient Register LSB Color Space Conversion C4...
csc_spare_1	0x411a	Spare register with No associated functionality
csc_spare_2	0x411b	Spare register with No associated functionality

csc_cfg

Description: Color Space Converter Interpolation and Decimation Configuration Register

Size: 8 bits

Offset: 0x4100

Bits	Name	Attr	Description
7	csc_limit	R/W	When set (1'b1), the range limitation values defined in registers csc_mat_uplim and csc_mat_dnlim are applied to the output of the Color Space Conversion matrix. This feature ensures that the video output range is always respected, independently of the matrix coefficient configuration or of the video input stream. Value After Reset: 0x0
6	spare_2	R/W	Reserved as "spare" register with no associated functionality. Value After Reset: 0x0

5:4	intmode	R/W	Chroma interpolation configuration: intmode[1:0] Chroma Interpolation 00 interpolation disabled 01 $H_u(z) = 1 + z^{-1}$ 10 $H_u(z) = 1/2 + z^{-11} + 1/2 z^{-2}$ 11 interpolation disabled Value After Reset: 0x0
3:2	spare_1	R/W	Reserved as "spare" register with no associated functionality. Value After Reset: 0x0
1:0	decmode	R/W	Chroma decimation configuration: decmode[1:0] Chroma Decimation 00 decimation disabled 01 $H_d(z) = 1$ 10 $H_d(z) = 1/4 + 1/2z^{-1} + 1/4 z^{-2}$ 11 $H_d(z) \times 2^{11} = -5 + 12z^{-2} - 22z^{-4} + 39z^{-8} + 109z^{-10} - 204z^{-12} + 648z^{-14} + 1024z^{-15} + 648z^{-16} - 204z^{-18} + 109z^{-20} - 65z^{-22} + 39z^{-24} - 22z^{-26} + 12z^{-28} - 5z^{-30}$ Value After Reset: 0x0

csc_scale

Description: Color Space Converter Scale and Deep Color Configuration Register

Size: 8 bits

Offset: 0x4101

Bits	Name	Attr	Description
7:4	csc_color_depth	R/W	Color space converter color depth configuration: csc_colordepth[3:0] Action 0000 24 bit per pixel video (8 bit per component). 0001-0011 Reserved. Not used. 0100 24 bit per pixel video (8 bit per component). 0101 30 bit per pixel video (10 bit per component). 0110 36 bit per pixel video (12 bit per component). 0111 48 bit per pixel video (16 bit per component). other Reserved. Not used. Value After Reset: 0x0
3:2	spare	R/W	The is a Reserved as "spare" register with no associated functionality. Value After Reset: 0x0
1:0	cscscale	R/W	Defines the cscscale[1:0] scale factor to apply to all coefficients in Color Space Conversion. This scale factor is expressed in the number of left shifts to apply to each of the coefficients, ranging from 0 to 2. Value After Reset: 0x1

csc_coef_a1_msb

Description: Color Space Converter Matrix A1 Coefficient Register MSB Notes:

The coefficients used in the CSC matrix use only 15 bits for the internal computations.

Coefficients are represented in 2's complementary format and stored in two registers:

csc_coef_*_lsb[7:0]: coefficient bits 7 to 0

csc_coef_*_msb[7]: spare bit

csc_coef_*_msb[6:0]: coefficient bits 14 to 8

Examples for standard ITU601 and ITU709 RGB/YCC conversion CSC coefficients exist in the Video Datapath Application Note.

Size: 8 bits

Offset: 0x4102

Bits	Name	Attr	Description
7:0	csc_coef_a_1_msb	R/W	Color Space Converter Matrix A1 Coefficient Register MSB Value After Reset: 0x20

csc_coef_a1_lsb

Description: Color Space Converter Matrix A1 Coefficient Register LSB Notes:

The coefficients used in the CSC matrix use only 15 bits for the internal computations.

Coefficients are represented in 2's complementary format and stored in two registers:

csc_coef_*_lsb[7:0]: coefficient bits 7 to 0

csc_coef_*_msb[7]: spare bit

csc_coef_*_msb[6:0]: coefficient bits 14 to 8

Examples for standard ITU601 and ITU709 RGB/YCC conversion CSC coefficients exist in the Video Datapath Application Note.

Size: 8 bits

Offset: 0x4103

Bits	Name	Attr	Description
7:0	csc_coef_a_1_lsb	R/W	Color Space Converter Matrix A1 Coefficient Register LSB Value After Reset: 0x0

csc_coef_a2_msb

Description: Color Space Converter Matrix A2 Coefficient Register MSB Color Space Conversion A2 coefficient.

Size: 8 bits

Offset: 0x4104

Bits	Name	Attr	Description
7:0	csc_coef_a_2_msb	R/W	Color Space Converter Matrix A2 Coefficient Register MSB Value After Reset: 0x0

csc_coef_a2_lsb

Description: Color Space Converter Matrix A2 Coefficient Register LSB Color Space Conversion A2 coefficient.

Size: 8 bits

Offset: 0x4105

Bits	Name	Attr	Description
7:0	csc_coef_a_2_lsb	R/W	Color Space Converter Matrix A2 Coefficient Register LSB Value After Reset: 0x0

csc_coef_a3_msb

Description: Color Space Converter Matrix A3 Coefficient Register MSB Color Space Conversion A3 coefficient.

Size: 8 bits

Offset: 0x4106

Bits	Name	Attr	Description
7:0	csc_coef_a3_msb	R/W	Color Space Converter Matrix A3 Coefficient Register MSB Value After Reset: 0x0

csc_coef_a3_lsb

Description: Color Space Converter Matrix A3 Coefficient Register LSB Color Space Conversion A3 coefficient.

Size: 8 bits

Offset: 0x4107

Bits	Name	Attr	Description
7:0	csc_coef_a3_lsb	R/W	Color Space Converter Matrix A3 Coefficient Register LSB Value After Reset: 0x0

csc_coef_a4_msb

Description: Color Space Converter Matrix A4 Coefficient Register MSB Color Space Conversion A4 coefficient.

Size: 8 bits

Offset: 0x4108

Bits	Name	Attr	Description
7:0	csc_coef_a4_msb	R/W	Color Space Converter Matrix A4 Coefficient Register MSB Value After Reset: 0x0

csc_coef_a4_lsb

Description: Color Space Converter Matrix A4 Coefficient Register LSB Color Space Conversion A4 coefficient.

Size: 8 bits

Offset: 0x4109

Bits	Name	Attr	Description
7:0	csc_coef_a4_lsb	R/W	Color Space Converter Matrix A4 Coefficient Register LSB Value After Reset: 0x0

csc_coef_b1_msb

Description: Color Space Converter Matrix B1 Coefficient Register MSB Color Space Conversion B1 coefficient.

Size: 8 bits

Offset: 0x410a

Bits	Name	Attr	Description
7:0	csc_coef_b1_msb	R/W	Color Space Converter Matrix B1 Coefficient Register MSB Value After Reset: 0x0

csc_coef_b1_lsb

Description: Color Space Converter Matrix B1 Coefficient Register LSB Color Space Conversion B1 coefficient.

Size: 8 bits

Offset: 0x410b

Bits	Name	Attr	Description
7:0	csc_coef_b1_lsb	R/W	Color Space Converter Matrix B1 Coefficient Register LSB Value After Reset: 0x0

csc_coef_b2_msb

Description: Color Space Converter Matrix B2 Coefficient Register MSB Color Space Conversion B2 coefficient.

Size: 8 bits

Offset: 0x410c

Bits	Name	Attr	Description
7:0	csc_coef_b2_msb	R/W	Color Space Converter Matrix B2 Coefficient Register MSB Value After Reset: 0x20

csc_coef_b2_lsb

Description: Color Space Converter Matrix B2 Coefficient Register LSB Color Space Conversion B2 coefficient.

Size: 8 bits

Offset: 0x410d

Bits	Name	Attr	Description
7:0	csc_coef_b2_lsb	R/W	Color Space Converter Matrix B2 Coefficient Register LSB Value After Reset: 0x0

csc_coef_b3_msb

Description: Color Space Converter Matrix B3 Coefficient Register MSB Color Space Conversion B3 coefficient.

Size: 8 bits

Offset: 0x410e

Bits	Name	Attr	Description
7:0	csc_coef_b3_msb	R/W	Color Space Converter Matrix B3 Coefficient Register MSB Value After Reset: 0x0

csc_coef_b3_lsb

Description: Color Space Converter Matrix B3 Coefficient Register LSB Color Space Conversion B3 coefficient.

Size: 8 bits

Offset: 0x410f

Bits	Name	Attr	Description
7:0	csc_coef_b3_lsb	R/W	Color Space Converter Matrix B3 Coefficient Register LSB Value After Reset: 0x0

csc_coef_b4_msb

Description: Color Space Converter Matrix B4 Coefficient Register MSB Color Space Conversion B4 coefficient.

Size: 8 bits

Offset: 0x4110

Bits	Name	Attr	Description
7:0	csc_coef_b4_msb	R/W	Color Space Converter Matrix B4 Coefficient Register MSB Value After Reset: 0x0

csc_coef_b4_lsb

Description: Color Space Converter Matrix B4 Coefficient Register LSB Color Space Conversion B4 coefficient.

Size: 8 bits

Offset: 0x4111

Bits	Name	Attr	Description
7:0			

7:0	csc_coef_b4 _lsb	R/W	Color Space Converter Matrix B4 Coefficient Register LSB Value After Reset: 0x0
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csc_coef_c1_msb

Description: Color Space Converter Matrix C1 Coefficient Register MSB Color Space Conversion C1 coefficient.

Size: 8 bits

Offset: 0x4112

Bits	Name	Attr	Description
7:0	csc_coef_c1 _msb	R/W	Color Space Converter Matrix C1 Coefficient Register MSB Value After Reset: 0x0

csc_coef_c1_lsb

Description: Color Space Converter Matrix C1 Coefficient Register LSB Color Space Conversion C1 coefficient.

Size: 8 bits

Offset: 0x4113

Bits	Name	Attr	Description
7:0	csc_coef_c1 _lsb	R/W	Color Space Converter Matrix C1 Coefficient Register LSB Value After Reset: 0x0

csc_coef_c2_msb

Description: Color Space Converter Matrix C2 Coefficient Register MSB Color Space Conversion C2 coefficient.

Size: 8 bits

Offset: 0x4114

Bits	Name	Attr	Description
7:0	csc_coef_c2 _msb	R/W	Color Space Converter Matrix C2 Coefficient Register MSB Value After Reset: 0x0

csc_coef_c2_lsb

Description: Color Space Converter Matrix C2 Coefficient Register LSB Color Space Conversion C2 coefficient.

Size: 8 bits

Offset: 0x4115

Bits	Name	Attr	Description
7:0	csc_coef_c2 _lsb	R/W	Color Space Converter Matrix C2 Coefficient Register LSB Value After Reset: 0x0

csc_coef_c3_msb

Description: Color Space Converter Matrix C3 Coefficient Register MSB Color Space Conversion C3 coefficient.

Size: 8 bits

Offset: 0x4116

Bits	Name	Attr	Description
7:0	csc_coef_c3 _msb	R/W	Color Space Converter Matrix C3 Coefficient Register MSB Value After Reset: 0x20

csc_coef_c3_lsb

Description: Color Space Converter Matrix C3 Coefficient Register LSB Color Space Conversion

C3 coefficient.

Size: 8 bits

Offset: 0x4117

Bits	Name	Attr	Description
7:0	csc_coef_c3 _lsb	R/W	Color Space Converter Matrix C3 Coefficient Register LSB Value After Reset: 0x0

csc_coef_c4_msb

Description: Color Space Converter Matrix C4 Coefficient Register MSB Color Space Conversion C4 coefficient.

Size: 8 bits

Offset: 0x4118

Bits	Name	Attr	Description
7:0	csc_coef_c4 _msb	R/W	Description: Color Space Converter Matrix C4 Coefficient Register MSB Value After Reset: 0x0

csc_coef_c4_lsb

Description: Color Space Converter Matrix C4 Coefficient Register LSB Color Space Conversion C4 coefficient.

Size: 8 bits

Offset: 0x4119

Bits	Name	Attr	Description
7:0	csc_coef_c4 _lsb	R/W	Color Space Converter Matrix C4 Coefficient Register LSB Value After Reset: 0x0

csc_spare_1, csc_spare_1

Description: Spare Register with No Associated functionality

Value after Reset: 0x00, 0x00

Size: 8 bits

Offset: 0x411a, 0x411b

Bits	Name	Attr	Description
7:0	spare	R/W	This is a spare register with no associated functionality

csc_limit_up_lsb

Description: Color Space Converter Matrix output Up Limit Register LSB

For more details, refer to the HDMI 1.4 specification, paragraph 6.6 Video Quantization Ranges.

For an RGB output of 8 bits, the expected limit is 254 (valid range column of Table 6-3), and this register must be configured with 0xFE.

Size: 8 bits

Offset: 0x411b

Bits	Name	Attr	Description
7:0	csc_limit_u p_lsb	R/W	Color Space Converter Matrix Output Upper Limit Register LSB Value After Reset: 0xff

csc_limit_dn_msb

Description: Color Space Converter Matrix output Down Limit Register MSB

For more details, refer to the HDMI 1.4 specification, paragraph 6.6 Video Quantization Ranges.

For an RGB output of 8 bits, the expected limit is 1 (valid range column of Table 6-3), and this register must be configured with 0x00.

Size: 8 bits

Offset: 0x411c

Bits	Name	Attr	Description
7:0	csc_limit_dn_n_msb	R/W	Color Space Converter Matrix output Down Limit Register MSB Value After Reset: 0x0

csc_limit_dn_lsb

Description: Color Space Converter Matrix output Down Limit Register LSB

For more details, refer to the HDMI 1.4 specification, paragraph 6.6 Video Quantization Ranges. For an RGB output of 8 bits, the expected limit is 1 (valid range column of Table 6-3), and this register must be configured with 0x01.

Size: 8 bits

Offset: 0x411d

Bits	Name	Attr	Description
7:0	csc_limit_dn_lsb	R/W	Color Space Converter Matrix Output Down Limit Register LSB Value After Reset: 0x0

HDCP Registers

HDCP Registers. Follow the link for the register to see a detailed description of the register.

Register	Offset	Description
a_hdcpcfg0	0x5000	HDCP Enable and Functional Control Configuration Register 0
a_hdcpcfg1	0x5001	HDCP Software Reset and Functional Control Configuration Register 1
a_hdcpobs0	0x5002	HDCP Observation Register 0
a_hdcpobs1	0x5003	HDCP Observation Register 1
a_hdcpobs2	0x5004	HDCP Observation Register 2
a_hdcpobs3	0x5005	HDCP Observation Register 3
a_apiintclr	0x5006	HDCP Interrupt Clear Register Write only register, active high and auto cleared, cleans the respective...
a_apiintstat	0x5007	HDCP Interrupt Status Register Read only register, reports the interruption which caused the activation...
a_apiintmsk	0x5008	HDCP Interrupt Mask Register The configuration of this register mask a given setup of interruption,...
a_vidpolcfg	0x5009	HDCP Video Polarity Configuration Register
a_oesswcfg	0x500a	HDCP OESS WOO Configuration Register Pulse width of the encryption enable (CTL3) signal in the...
a_coreverlsb	0x5014	HDCP Controller Version Register LSB Design ID number.
a_corevermsb	0x5015	HDCP Controller Version Register MSB Revision ID number.
a_ksvmemctrl	0x5016	HDCP KSV Memory Control Register The KSVCTRLupd bit is a notification flag. This flag changes polarity...
hdcp_bstatus[0:1]	0x5020 + (i * 0x1)	HDCP BStatus Register Array
hdcp_m0[0:7]	0x5022 + (i * 0x1)	HDCP M0 Register Array
hdcp_ksv[0:634]	0x502a	HDCP KSV Registers

Register	Offset	Description
	+ (i * 0x1)	
hdcp_vh[0:19]	0x52a5 + (i * 0x1)	HDCP SHA-1 VH Registers
hdcp_revoc_size_0	0x52b9	HDCP Revocation KSV List Size Register 0
hdcp_revoc_size_1	0x52ba	HDCP Revocation KSV List Size Register 1
hdcp_revoc_list[0:5059]	0x52bb + (i * 0x1)	HDCP Revocation KSV Registers
hdcpreg_bksv0	0x7800	HDCP KSV Status Register 0

Registers for Address Block: HDCP (Continued)

Register	Offset	Description
hdcpreg_bksv1	0x7801	HDCP KSV Status Register 1
hdcpreg_bksv2	0x7802	HDCP KSV Status Register 2
hdcpreg_bksv3	0x7803	HDCP KSV Status Register 3
hdcpreg_bksv4	0x7804	HDCP KSV Status Register 4
hdcpreg_anconf	0x7805	HDCP AN Bypass Control Register
hdcpreg_an0	0x7806	HDCP Forced AN Register 0
hdcpreg_an1	0x7807	HDCP Forced AN Register 1
hdcpreg_an2	0x7808	HDCP forced AN Register 2
hdcpreg_an3	0x7809	HDCP Forced AN Register 3
hdcpreg_an4	0x780a	HDCP Forced AN Register 4
hdcpreg_an5	0x780b	HDCP Forced AN Register 5
hdcpreg_an6	0x780c	HDCP Forced AN Register 6
hdcpreg_an7	0x780d	HDCP Forced AN Register 7
hdcpreg_rmlctl	0x780e	HDCP Encrypted Device Private Keys Control Register This register is the control register for the...
hdcpreg_rmlsts	0x780f	HDCP Encrypted DPK Status Register The required software configuration sequence is documented in...
hdcpreg_seed0	0x7810	HDCP Encrypted DPK Seed Register 0 This register contains a byte of the HDCP Encrypted DPK seed...
hdcpreg_seed1	0x7811	HDCP Encrypted DPK Seed Register 1 This register contains a byte of the HDCP Encrypted DPK seed...
hdcpreg_dpk0	0x7812	HDCP Encrypted DPK Data Register 0 This register contains an HDCP DPK byte. The required software...
hdcpreg_dpk1	0x7813	HDCP Encrypted DPK Data Register 1 This register contains an HDCP DPK byte. The required software...
hdcpreg_dpk2	0x7814	HDCP Encrypted DPK Data Register 2 This register contains an HDCP DPK byte. The required software...
hdcpreg_dpk3	0x7815	HDCP Encrypted DPK Data Register 3 This register contains an HDCP DPK byte. The required software...
hdcpreg_dpk4	0x7816	HDCP Encrypted DPK Data Register 4 This register contains an HDCP DPK byte. The required software...
hdcpreg_dpk5	0x7817	HDCP Encrypted DPK Data Register 5 This register contains an HDCP DPK byte. The

Register	Offset	Description
		required software...
hdcpreg_dpk6	0x7818	HDCP Encrypted DPK Data Register 6 This register contains an HDCP DPK byte. The required software...

a_hdcpcfg0

Description: HDCP Enable and Functional Control Configuration Register 0

Size: 8 bits

Offset: 0x5000

Bits	Name	Attr	Description
7	ELVena	R/W	Enables the Enhanced Link Verification from the transmitter's side Value After Reset: 0x0
6	I2Cfastmode	R/W	Enable the I2C fast mode option from the transmitter's side. Value After Reset: 0x0
5	bypencryption	R/W	Bypasses all the data encryption stages Value After Reset: "(HDMI_HDCP_BYPASS== 1) ? 1 : 0"
4	syncricheck	R/W	Configures if the Ri check should be done at every 2s even or synchronously to every 128 encrypted frame. Value After Reset: 0x0
3	avmute	R	This register holds the current AVMUTE state of the Hdmi_tx controller, as expected to be perceived by the connected HDMI/HDCP sink device. Value After Reset: 0x0
2	rxdetect	R/W	Information that a sink device was detected connected to the HDMI port Value After Reset: 0x0
1	en11feature	R/W	Enable the use of features 1.1 from the transmitter's side Value After Reset: 0x0
0	hdmidvi	R/W	Configures the transmitter to operate with a HDMI capable device or with a DVI device. Value After Reset: 0x0

a_hdcpcfg1

Description: HDCP Software Reset and Functional Control Configuration Register 1

Size: 8 bits

Offset: 0x5001

Bits	Name	Attr	Description
7:5	spare	R/W	Reserved as "spare" register with no associated functionality. Value After Reset: 0x0
4	hdcp_lock	R/W	Lock the HDCP bypass and encryption disable mechanisms: 1'b0: The default 1'b0 value enables you to bypass HDCP through bit 5 (bypencryption) of the A_HDCPCFG0 register or to disable the encryption through bit 1 (encryptiondisable) of A_HDCPCFG1.

Bits	Name	Attr	Description
			1'b1: You can still write to the bit by encryption of A_HDCPCFG0 or encryption disable bit of A_HDCPCFG1 but you cannot enable the bypass. Once you set the value to 1'b1, you can change the value back to 1'b0 only by issuing a master reset to the Hdmi_tx. Value After Reset: 0x0
3	dissha1check	R/W	Disables the request to the API processor to verify the SHA1 message digest of a received KSV List Value After Reset: 0x0
2	ph2upshftenc	R/W	Enables the encoding of packet header in the tmdsch0 bit[0] with cipher[2] instead of the tmdsch0 bit[2] Note: This bit must always be set to 1 for all PHYs. Value After Reset: 0x0
1	encryptiondisable	R/W	Disable encryption without losing authentication Value After Reset: 0x0
0	swreset	R/W	Software reset signal, active by writing a zero and auto cleared to 1 in the following cycle. Value After Reset: 0x1

a_hdcpobs0

Description: HDCP Observation Register 0

Size: 8 bits

Offset: 0x5002

Bits	Name	Attr	Description
7:4	STATEA	R	Observability register informs in which state the authentication machine is on. Value After Reset: 0x0
3:1	SUBSTATEA	R	Observability register informs in which sub-state the authentication is on. Value After Reset: 0x0
0	hdcpengaged	R	Informs that the current HDMI link has the HDCP protocol fully engaged. Value After Reset: 0x0

a_hdcpobs1

Description: HDCP Observation Register 1

Size: 8 bits

Offset: 0x5003

Bits	Name	Attr	Description
7			Reserved for future use.
6:4	STATEOEG	R	Observability register informs in which state the OESS machine is on. Value After Reset: 0x0
3:0	STATER	R	Observability register informs in which state the revocation machine is on. Value After Reset: 0x0

a_hdcpobs2

Description: HDCP Observation Register 2

Size: 8 bits

Offset: 0x5004

Bits	Name	Attr	Description
7:6			Reserved for future use.
5:3	STATEE	R	Observability register informs in which state the cipher machine is on. Value After Reset: 0x0
2:0	STATEEEG	R	Observability register informs in which state the EESS machine is on. Value After Reset: 0x0

a_hdcpobs3

Description: HDCP Observation Register 3

Size: 8 bits

Offset: 0x5005

Bits	Name	Attr	Description
7	HDMI_RESERVED_1	R	Register read from attached sink device: Bcap(0x40) bit 7. Value After Reset: 0x0
6	REPEATER	R	Register read from attached sink device: Bcap(0x40) bit 6. Value After Reset: 0x0
5	KSV_FIFO_READY	R	Register read from attached sink device: Bcap(0x40) bit 5. Value After Reset: 0x0
4	FAST_I2C	R	Register read from attached sink device: Bcap(0x40) bit 4. Value After Reset: 0x0
3	HDMI_RESERVED_2	R	Register read from attached sink device: Bstatus(0x41) bit 13. Value After Reset: 0x0
2	HDMI_MODE	R	Register read from attached sink device: Bstatus(0x41) bit 12. Value After Reset: 0x0
1	FEATURES_1_1	R	Register read from attached sink device: Bcap(0x40) bit 1. Value After Reset: 0x0
0	FAST_REAUTHENTICATION	R	Register read from attached sink device: Bcap(0x40) bit 0. Value After Reset: 0x0

a_apiintclr

Description: HDCP Interrupt Clear Register

Write only register, active high and auto cleared, cleans the respective interruption in the interrupt status register.

Size: 8 bits

Offset: 0x5006

Bits	Name	Attr	Description
7	HDCP_engaged	W	Clears the interruption related to HDCP authentication process successful. Value After Reset: 0x0
6	HDCP_failed	W	Clears the interruption related to HDCP authentication process failed. Value After Reset: 0x0
5	KSVsha1calcdoneint	W	Clears the interruption related to SHA1 verification

			has been done Value After Reset: 0x0
4	I2Cnack	W	Clears the interruption related to I2C NACK reception. Value After Reset: 0x0
3	Lostarbitration	W	Clears the interruption related to I2C arbitration lost. Value After Reset: 0x0
2	Keepouterrorint	W	Clears the interruption related to keep out window error. Value After Reset: 0x0
1	KSVsha1calcint	W	Clears the interruption related to KSV list update in memory that needs to be SHA1 verified. Value After Reset: 0x0
0	KSVaccessint	W	Clears the interruption related to KSV Attr grant for Read-Write access. Value After Reset: 0x0

a_apiintstat

Description: HDCP Interrupt Status Register

Read only register, reports the interruption which caused the activation of the interruption output pin.

Size: 8 bits

Offset: 0x5007

Bits	Name	Attr	Description
7	HDCP_engaged	R	Notifies that the HDCP authentication process was successful Value After Reset: 0x0
6	HDCP_failed	R	Notifies that the HDCP authentication process was failed. Value After Reset: 0x0
5	KSVsha1calcdoneint	R	Notifies that the HDCP13TCTRL controller SHA1 verification has been done. The status ready to be read. Value After Reset: 0x0
4	I2Cnack	R	Notifies that the I2C received a NACK from slave device. Value After Reset: 0x0
3	Lostarbitration	R	Notifies that the I2C lost the arbitration to communicate. Another master gained arbitration. Value After Reset: 0x0
2	Keepouterrorint	R	Notifies that during the keep out window, the ctlout[3:0] bus was used besides control period. Value After Reset: 0x0
1	KSVsha1calcint	R	Notifies that the HDCP13TCTRL controller has updated a KSV list in memory that needs to be SHA1 verified. Value After Reset: 0x0
0	KSVaccessint	R	Notifies that the KSV Attr has been guaranteed for Read-Write access. Value After Reset: 0x0

a_apiintmsk

Description: HDCP Interrupt Mask Register

The configuration of this register mask a given setup of interruption, disabling them from generating interruption pulses in the interruption output pin.

Size: 8 bits

Offset: 0x5008

Bits	Name	Attr	Description
7	HDCP_engaged	R/W	Masks the interruption related to HDCP authentication process successful. Value After Reset: 0x0
6	HDCP_failed	R/W	Masks the interruption related to HDCP authentication process failed. Value After Reset: 0x0
5	KSVsha1calcdoneint	R/W	Masks the interruption related to SHA1 verification has been done Otherwise, this field is a "spare" bit with no associated functionality. Value After Reset: 0x0
4	I2Cnack	R/W	Masks the interruption related to I2C NACK reception. Value After Reset: 0x0
3	Lostarbitration	R/W	Masks the interruption related to I2C arbitration lost. Value After Reset: 0x0
2	Keepouterrorint	R/W	Masks the interruption related to keep out window error. Value After Reset: 0x0
1	KSVsha1calcint	R/W	Masks the interruption related to KSV list update in memory that needs to be SHA1 verified. Otherwise, this field is a "spare" bit with no associated functionality. Value After Reset: 0x0
0	KSVaccessint	R/W	Masks the interruption related to KSV Attr grant for Read-Write access. Value After Reset: 0x0

a_vidpolcfg

Description: HDCP Video Polarity Configuration Register

Size: 8 bits

Offset: 0x5009

Bits	Name	Attr	Description
7			Reserved for future use.
6:5	unencryptconf	R/W	Configuration of the color sent when sending unencrypted video data Value After Reset: 0x0
4	dataenpol	R/W	Configuration of the video data enable polarity Value After Reset: 0x0
3	vsyncpol	R/W	Configuration of the video Vertical synchronism polarity Value After Reset: 0x0
2	spare_2	R/W	Reserved as "spare" bit with no associated functionality. Value After Reset: 0x0
1	hsyncpol	R/W	Configuration of the video Horizontal synchronism polarity. Value After Reset: 0x0
0	spare_1	R/W	Reserved as "spare" bit with no associated functionality. Value After Reset: 0x0

a_oesswcfg

Description: HDCP OESS WOO Configuration Register

Pulse width of the encryption enable (CTL3) signal in the HDCP OESS mode. The window of opportunity for the Original Encryption Status Signaling starts at the active edge of the Vertical synchronism and stops after oesswindowoffset[7:0]*4 clock cycles of TMDS clock. According to the HDCP specification, the CTL3 signal must be asserted at least for eight TMDS clock cycles (oesswindowoffset[7:0] must be greater than 1), and it is recommended to transmit a larger pulse width for enhanced link reliability.

Size: 8 bits

Offset: 0x500a

Bits	Name	Attr	Description
7:0	a_oesswcfg	R/W	HDCP OESS WOO Configuration Register Value After Reset: 0x80

a_coreverlsb

Description: HDCP Controller Version Register LSB Design ID number.

Size: 8 bits

Offset: 0x5014

Bits	Name	Attr	Description
7:0	a_coreverlsb	R	HDCP Controller Version Register LSB Value After Reset: 0x2

a_corevermsb

Description: HDCP Controller Version Register MSB Revision ID number.

Size: 8 bits

Offset: 0x5015

Bits	Name	Attr	Description
7:0	a_corevermsb	R	HDCP Controller Version Register MSB Value After Reset: 0x3

a_ksvmemctrl

Description: HDCP KSV Memory Control Register

The KSVCTRLupd bit is a notification flag. This flag changes polarity whenever the register is written. This flag acts as a trigger to other blocks that processes this data. Upon reset the flag returns to low default value.

Size: 8 bits

Offset: 0x5016

Bits	Name	Attr	Description
7:5			Reserved for future use.
4	KSVsha1status	R	Notification whether the KSV list message digest is correct from the controller: 1'b1 if digest message verification failed 1'b0 if digest message verification succeeded Value After Reset: 0x0
3	SHA1fail	R/W	Notification whether the KSV list message digest is correct. Value After Reset: 0x0
2	KSVCTRLupd	R/W	Set to inform that the KSV list in memory has been analyzed and the response to the Message Digest has been updated if on configurations on software SHA-1 calculation. Value After Reset: 0x0
1	KSVMEMaccess	R	Notification that the KSV Attr as been guaranteed. Value After Reset: 0x0
0	KSVMEMrequest	R/W	Request access to the KSV memory; must be de-asserted after the access is completed by the

Bits	Name	Attr	Description
			system. Value After Reset: 0x0

hdcp_bstatus[0:1]

Description: HDCP BStatus Register Array

Size: 8 bits

Offset: 0x5020 + (i * 0x1)

Bits	Name	Attr	Description
7:0	bstatus	R/W	HDCP BSTATUS[15:0]. If Attr has not been granted (see register a_ksvmemctrl), the value read will be 8'hff. Value After Reset: 0xff

hdcp_m0[0:7]

Description: HDCP M0 Register Array

Size: 8 bits

Offset: 0x5022 + (i * 0x1)

Bits	Name	Attr	Description
7:0	M0	R/W	HDCP M0[32:0]. If Attr has not been granted (see register a_ksvmemctrl) , the value read will be 8'hff. These values are only available on a configuration that has the SHA1 calculation by software. Value After Reset: 0xff

hdcp_ksv[0:634]

Description: HDCP KSV Registers.

Size: 8 bits

Offset: 0x502a + (i * 0x1)

Bits	Name	Attr	Description
7:0	hdcp_ksv_byte	R/W	Sink KSV FIFO byte, ordered in little endian (byte at address 0x502a belongs to byte 0 of KSV0). If Attr has not been granted (see register a_ksvmemctrl), the value read is 8'hff. In this address space, 635 KSV FIFO bytes are mapped, which allow for 127 KSV values, each with 5 bytes (40 bits). Value After Reset: 0xff

hdcp_vh[0:19]

Description: HDCP SHA-1 VH Registers.

Size: 8 bits

Offset: 0x52a5 + (i * 0x1)

Bits	Name	Attr	Description
7:0	hdcp_vh_byte	R/W	Sink VH' byte, ordered in little endian (byte at address 0x525a belongs to byte 0 of VH0). If Attr has not been granted (see register a_ksvmemctrl), the value read is 8'hff. In this address space 20 VH bytes are mapped, which allow for 5 VH values, each with 4 bytes (32bits). Value After Reset: 0xff

hdcp_revoc_size_0

Description: HDCP Revocation KSV List Size Register 0

Size: 8 bits

Offset: 0x52b9

Bits	Name	Attr	Description
7:0	hdcp_revoc_size_0	R/W	Register containing the LSB of KSV list size (ksv_list_size[7:0]). If Attr has not been granted (see register a_ksvmemctrl), the value read is 8'hff. Value After Reset: 0xff

hdcp_revoc_size_1

Description: HDCP Revocation KSV List Size Register 1

Size: 8 bits

Offset: 0x52ba

Bits	Name	Attr	Description
7:0	hdcp_revoc_size_1	R/W	Register containing the MSB of KSV list size (ksv_list_size[15:8]). If Attr has not been granted (see register a_ksvmemctrl), the value read is 8'hff. Value After Reset: 0xff

hdcp_revoc_list[0:5059]

Description: HDCP Revocation KSV Registers.

Size: 8 bits

Offset: 0x52bb + (i * 0x1)

Bits	Name	Attr	Description
7:0	hdcp_revoc_list_ksv_byte	R/W	Revocation KSV byte, ordered in little endian (byte at address 0x52bb belongs to byte 0 of the first revoked KSV). If Attr has not been granted (see register a_ksvmemctrl), the value read is 8'hff. In this address space 5060 revoked KSV bytes are mapped, which allow for 1012 KSV values, each with 5 bytes (40 bits). Value After Reset: 0xff

hdcpreg_bksv0

Description: HDCP KSV Status Register 0

Size: 8 bits

Offset: 0x7800

Bits	Name	Attr	Description
7:0	hdcpreg_bksv0	R	Contains the value of BKS[7:0]. Value After Reset: 0x0

hdcpreg_bksv1

Description: HDCP KSV Status Register 1

Size: 8 bits

Offset: 0x7801

Bits	Name	Attr	Description
7:0	hdcpreg_bksv1	R	Description: Contains the value of BKS[15:8]. Value After Reset: 0x0

hdcpreg_bksv2

Description: HDCP KSV Status Register 2

Size: 8 bits

Offset: 0x7802

Bits	Name	Attr	Description
7:0	hdcpreg_bksv2	R	Contains the value of BKS[23:16]. Value After Reset: 0x0

hdcpreg_bksv3

Description: HDCP KSV Status Register 3

Size: 8 bits

Offset: 0x7803

Bits	Name	Attr	Description
7:0	hdcpreg_bksv3	R	Contains the value of BKS[31:24]. Value After Reset: 0x0

hdcpreg_bksv4

Description: HDCP KSV Status Register 4

Size: 8 bits

Offset: 0x7804

Bits	Name	Attr	Description
7:0	hdcpreg_bksv4	R	Contains the value of BKS[39:32]. Value After Reset: 0x0

hdcpreg_anconf

Description: HDCP AN Bypass Control Register

Size: 8 bits

Offset: 0x7805

Bits	Name	Attr	Description
7:1			Reserved for future use.
0	oanbypass	R/W	When oanbypass=1, the value of AN used in the HDCP engine comes from the hdcpreg_an0 to hdcpreg_an7 registers. When oanbypass=0, the value of AN used in the HDCP engine comes from the random number input. Value After Reset: 0x0

hdcpreg_an0

Description: HDCP Forced AN Register 0

Size: 8 bits

Offset: 0x7806

Bits	Name	Attr	Description
7:0	hdcpreg_an0	R/W	Contains the value of AN[7:0] Value After Reset: 0x0

hdcpreg_an1

Description: HDCP Forced AN Register 1

Size: 8 bits

Offset: 0x7807

Bits	Name	Attr	Description
7:0	hdcpreg_an1	R/W	Contains the value of AN[15:8] Value After Reset: 0x0

hdcpreg_an2

Description: HDCP forced AN Register 2

Size: 8 bits

Offset: 0x7808

Bits	Name	Attr	Description
7:0	hdcpreg_an2	R/W	Contains the value of AN[23:16] Value After Reset: 0x0

hdcpreg_an3

Description: HDCP Forced AN Register 3

Size: 8 bits

Offset: 0x7809

Bits	Name	Attr	Description
7:0	hdcpreg_an3	R/W	Contains the value of AN[31:24] Value After Reset: 0x0

hdcpreg_an4

Description: HDCP Forced AN Register 4

Size: 8 bits

Offset: 0x780a

Bits	Name	Attr	Description
7:0	hdcpreg_an4	R/W	Contains the value of AN[39:32] Value After Reset: 0x0

hdcpreg_an5

Description: HDCP Forced AN Register 5

Size: 8 bits

Offset: 0x780b

Bits	Name	Attr	Description
7:0	hdcpreg_an5	R/W	Contains the value of AN[47:40] Value After Reset: 0x0

hdcpreg_an6

Description: HDCP Forced AN Register 6

Size: 8 bits

Offset: 0x780c

Bits	Name	Attr	Description
7:0	hdcpreg_an6	R/W	Contains the value of AN[55:48] Value After Reset: 0x0

hdcpreg_an7

Description: HDCP Forced AN Register 7

Size: 8 bits

Offset: 0x780d

Bits	Name	Attr	Description
7:0	hdcpreg_an7	R/W	Contains the value of BKS[63:56] Value After Reset: 0x0

hdcpreg_rmlctl

Description: HDCP Encrypted Device Private Keys Control Register

This register is the control register for the software programmable encrypted DPK embedded storage feature. The required software configuration sequence is documented in the Cores HDMI Transmitter User Guide in the "Programming" chapter, Section 3.2.4, "Configure HDCP."

Size: 8 bits

Offset: 0x780e

Bits	Name	Attr	Description
7:1			Reserved for future use.
0	odpk_decrypt_enable	R/W	When set (1'b1), this bit activates the decryption of the Device Private keys. Value After Reset: 0x0

hdcpreg_rmlsts

Description: HDCP Encrypted DPK Status Register

The required software configuration sequence is documented in the Cores HDMI Transmitter User Guide in the "Programming" chapter, Section 3.2.4, "Configure HDCP."

Size: 8 bits

Offset: 0x780f

Bits	Name	Attr	Description
7			Reserved for future use.
6	idpk_wr_ok_sts	R	When high (1'b1), it indicates that a DPK write is allowed. Value After Reset: 0x0
5:0	idpk_data_index	R	Current Device Private Key being written plus one. Position 0 is occupied by the AKSV. Value After Reset: 0x0

hdcpreg_seed0

Description: HDCP Encrypted DPK Seed Register 0

This register contains a byte of the HDCP Encrypted DPK seed value used to encrypt the Device Private Keys. The required software configuration sequence is documented in the Cores HDMI Transmitter User Guide in the "Programming" chapter, Section 3.2.4, "Configure HDCP."

Size: 8 bits

Offset: 0x7810

Bits	Name	Attr	Description
7:0	hdcpreg_seed0	W	Least significant byte of the decryption seed value (dpk_decrypt_seed[7:0]). Value After Reset: 0x0

hdcpreg_seed1

Description: HDCP Encrypted DPK Seed Register 1

This register contains a byte of the HDCP Encrypted DPK seed value used to encrypt the Device Private Keys. The required software configuration sequence is documented in the Cores HDMI Transmitter User Guide in the "Programming" chapter, Section 3.2.4, "Configure HDCP."

Size: 8 bits

Offset: 0x7811

Bits	Name	Attr	Description
7:0	hdcpreg_seed1	W	Most significant byte of the decryption seed value (dpk_decrypt_seed[15:8]). Value After Reset: 0x0

hdcpreg_dpk0

Description: HDCP Encrypted DPK Data Register 0

This register contains an HDCP DPK byte. The required software configuration sequence is documented in the Cores HDMI Transmitter User Guide in the "Programming" chapter, Section 3.2.4, "Configure HDCP."

Size: 8 bits

Offset: 0x7812

Bits	Name	Attr	Description
7:0	dpk_data	W	Byte of the encrypted DPK value. dpk[7:0] When this byte is written, a strobe signal is generated that triggers the decryption and/or storage of the DPK word on the DPK internal RAM memory. Value After Reset: 0x0

hdcpreg_dpk1

Description: HDCP Encrypted DPK Data Register 1

This register contains an HDCP DPK byte. The required software configuration sequence is documented in the Cores HDMI Transmitter User Guide in the "Programming" chapter, Section 3.2.4, "Configure HDCP."

Size: 8 bits

Offset: 0x7813

Bits	Name	Attr	Description
7:0	dpk_data	W	Byte of the encrypted DPK value. dpk[15:8] Value After Reset: 0x0

hdcpreg_dpk2

Description: HDCP Encrypted DPK Data Register 2

This register contains an HDCP DPK byte. The required software configuration sequence is documented in the Cores HDMI Transmitter User Guide in the "Programming" chapter, Section 3.2.4, "Configure HDCP."

Size: 8 bits

Offset: 0x7814

Bits	Name	Attr	Description
7:0	dpk_data	W	Byte of the encrypted DPK value. dpk[23:16] Value After Reset: 0x0

hdcpreg_dpk3

Description: HDCP Encrypted DPK Data Register 3

This register contains an HDCP DPK byte. The required software configuration sequence is documented in the Cores HDMI Transmitter User Guide in the "Programming" chapter, Section 3.2.4, "Configure HDCP."

Size: 8 bits

Offset: 0x7815

Bits	Name	Attr	Description
7:0	dpk_data	W	Byte of the encrypted DPK value. dpk[31:24] Value After Reset: 0x0

hdcpreg_dpk4

Description: HDCP Encrypted DPK Data Register 4

This register contains an HDCP DPK byte.

Size: 8 bits

Offset: 0x7816

Bits	Name	Attr	Description
7:0	dpk_data	W	Byte of the encrypted DPK value. dpk[39:32] Value After Reset: 0x0

hdcpreg_dpk5

Description: HDCP Encrypted DPK Data Register 5

This register contains an HDCP DPK byte. The required software configuration sequence is documented in the Cores HDMI Transmitter User Guide in the "Programming" chapter, Section 3.2.4, "Configure HDCP."

Size: 8 bits

Offset: 0x7817

Bits	Name	Attr	Description
7:0	dpk_data	W	Contains the value of DPK[x][47:40] Value After Reset: 0x0

hdcpreg_dpk6

Description: HDCP Encrypted DPK Data Register 6

This register contains an HDCP DPK byte. The required software configuration sequence is documented in the Cores HDMI Transmitter User Guide in the "Programming" chapter, Section 3.2.4, "Configure HDCP."

Size: 8 bits

Offset: 0x7818

Bits	Name	Attr	Description
7:0	dpk_data	W	Contains the value of DPK[x][55:48] Value After Reset: 0x0

CEC Registers

CEC Registers. Follow the link for the register to see a detailed description of the register.

Register	Offset	Description
cec_ctrl	0x7d00	CEC Control Register This register handles the main control of the CEC initiator.
cec_mask	0x7d02	CEC Interrupt Mask Register This read/write register masks/unmasks the interrupt events. When the...
cec_addr_l	0x7d05	CEC Logical Address Register Low This register indicates the logical address(es) allocated to the...
cec_addr_h	0x7d06	CEC Logical Address Register High This register indicates the logical address(es) allocated to...
cec_tx_cnt	0x7d07	CEC TX Frame Size Register This register indicates the size of the frame in bytes (including header...)
cec_rx_cnt	0x7d08	CEC RX Frame Size Register This register indicates the size of the frame in bytes (including header...)
cec_tx_data[0:15]	0x7d10 + (i * 0x1)	CEC TX Data Register Array Address offset: i = 0 to 15 These registers (8 bits each) are the buffers...
cec_rx_data[0:15]	0x7d20 + (i * 0x1)	CEC RX Data Register Array Address offset: i = 0 to 15 These registers (8 bit each) are the buffers...
cec_lock	0x7d30	CEC Buffer Lock Register
cec_wakeupctrl	0x7d31	CEC Wake-up Control Register After receiving a message in the CEC_RX_DATA1 (OPCODE) registers,...

cec_ctrl

Description: CEC Control Register

This register handles the main control of the CEC initiator.

Size: 8 bits

Offset: 0x7d00

Bits	Name	Attr	Description
7:5			Reserved for future use.
4	standby	R/W	1: CEC controller responds with a NACK to all messages and generates a wakeup status for opcode. It only responds with a NACK when the EOM is received. This means only the last block of a frame responds with NACK. The follower sends an ACK to the message when there is only one head block pointed to the follower, if the follower is in the standby mode. 0: CEC controller responds the ACK to all messages. Value After Reset: 0x0
3	bc_nack	R/W	1'b1: Set by software to NACK the received broadcast message. This bit holds until software resets. The

Bits	Name	Attr	Description
			broadcasts is answered with 1'b0, indicating the follower reject the message. 1'b0: Reset by software to ACK the received broadcast message. Value After Reset: 0x0
2:1	frame_typ	R/W	2'b00: Signal Free Time = 3-bit periods. Previous attempt to send frame is unsuccessful. 2'b01: Signal Free Time = 5-bit periods. New initiator wants to send a frame. 2'b10: Signal Free Time = 7-bit periods. Present initiator wants to send another frame immediately after its previous frame. (specification CEC 9.1). 2'b11: Illegal value. If software writes this value, hardware sets the value to the default 2'b01. Value After Reset: 0x1
0	send	R/W	1'b1: Set by software to trigger CEC sending a frame as an initiator. This bit keeps at 1'b1 while the transmission is going on. 1'b0: Reset to 1'b0 by hardware when the CEC transmission is done (no matter successful or failed). It can also work as an indicator checked by software to see whether the transmission is finished. Value After Reset: 0x0

cec_mask

Description: CEC Interrupt Mask Register

This read/write register masks/unmasks the interrupt events. When the bit is set to 1 (masked), the corresponding event does not trigger an interrupt signal at the system interface. When the bit is reset to 0, the interrupt event is unmasked.

Size: 8 bits

Offset: 0x7d02

Bits	Name	Attr	Description
7			Reserved for future use.
6	wakeup	R/W	Follower wake-up signal mask Value After Reset: 0x0
5	error_flow	R/W	An error is notified by a follower. Abnormal logic data bit error (for follower) Value After Reset: 0x0
4	error_initiator	R/W	An error is detected on a CEC line (for initiator only). Value After Reset: 0x0
3	arb_lost	R/W	The initiator losses the CEC line arbitration to a second initiator. (specification CEC 9) Value After Reset: 0x0
2	nack	R/W	A frame is not acknowledged in a directly addressed message. Or a frame is negatively acknowledged in a broadcast message (for initiator only) Value After Reset: 0x0
1	eom	R/W	EOM is detected so that the received data is ready in the receiver data buffer (for follower only) Value After Reset: 0x0
0	done	R/W	The current transmission is successful (for initiator only)

Bits	Name	Attr	Description
			Value After Reset: 0x0

cec_addr_l

Description: CEC Logical Address Register Low

This register indicates the logical address(es) allocated to the CEC device.

This register is written by software when the logical allocation is finished. Bit value 1 means the corresponding logical address is allocated to this device. Bit value 0 means the corresponding logical address is not allocated to this device.

Size: 8 bits

Offset: 0x7d05

Bits	Name	Attr	Description
7	cec_addr_l_7	R/W	Logical address 7 - Tuner 3 Value After Reset: 0x0
6	cec_addr_l_6	R/W	Logical address 6 - Tuner 2 Value After Reset: 0x0
5	cec_addr_l_5	R/W	Logical address 5 - Audio System Value After Reset: 0x0
4	cec_addr_l_4	R/W	Logical address 4 - Playback Device 1 Value After Reset: 0x0
3	cec_addr_l_3	R/W	Logical address 3 - Tuner 1 Value After Reset: 0x0
2	cec_addr_l_2	R/W	Logical address 2 - Recording Device 2 Value After Reset: 0x0
1	cec_addr_l_1	R/W	Logical address 1 - Recording Device 1 Value After Reset: 0x0
0	cec_addr_l_0	R/W	Logical address 0 - Device TV Value After Reset: 0x0

cec_addr_h

Description: CEC Logical Address Register High

This register indicates the logical address(es) allocated to the CEC device.

This register is written by software when the logical allocation is finished. Bit value 1 means the corresponding logical address is allocated to this device. Bit value 0 means the corresponding logical address is not allocated to this device.

Size: 8 bits

Offset: 0x7d06

Bits	Name	Attr	Description
7	cec_addr_h_7	R/W	Logical address 15 - Unregistered (as initiator address), Broadcast (as destination address) Value After Reset: 0x1
6	cec_addr_h_6	R/W	Logical address 14 - Free use Value After Reset: 0x0
5	cec_addr_h_5	R/W	Logical address 13 - Reserved Value After Reset: 0x0
4	cec_addr_h_4	R/W	Logical address 12 - Reserved Value After Reset: 0x0
3	cec_addr_h_3	R/W	Logical address 11 - Playback Device 3 Value After Reset: 0x0
2	cec_addr_h_2	R/W	Logical address 10 - Tuner 4 Value After Reset: 0x0
1	cec_addr_h_1	R/W	Logical address 9 - Playback Device 3 Value After Reset: 0x0
0	cec_addr_h_0	R/W	Logical address 8 - Playback Device 2 Value After Reset: 0x0

cec_tx_cnt

Description: CEC TX Frame Size Register

This register indicates the size of the frame in bytes (including header and data blocks), which are available in the transmitter data buffer.

Note: When the value is zero, the CEC controller ignores the send command triggered by software. When the transmission is done (no matter success or not), the current value is held until it is overwritten by software.

Size: 8 bits

Offset: 0x7d07

Bits	Name	Attr	Description
7:5			Reserved for future use.
4:0	cec_tx_cnt	R/W	CEC Transmitter Counter register 5'd0: No data needs to be transmitted 5'd1: Frame size is 1 byte 5'd16: Frame size is 16 bytes Value After Reset: 0x0

cec_rx_cnt

Description: CEC RX Frame Size Register

This register indicates the size of the frame in bytes (including header and data blocks), which are available in the receiver data buffer.

Note: Only after the whole receiving process is finished successfully, the counter is refreshed to the value which indicates the total number of data bytes in the Receiver Data Register.

Size: 8 bits

Offset: 0x7d08

Bits	Name	Attr	Description
7:5			Reserved for future use.
4:0	cec_rx_cnt	R	CEC Receiver Counter register: 5'd0: No data received 5'd1: 1-byte data is received 5'd16: 16-byte data is received Value After Reset: 0x0

cec_tx_data[0:15]

Description: CEC TX Data Register Array Address offset: i = 0 to 15

These registers (8 bits each) are the buffers used for storing the data waiting for transmission (including header and data blocks).

Size: 8 bits

Offset: 0x7d10 + (i * 0x1)

Bits	Name	Attr	Description
7:0	databyte	R/W	Data byte[x], where x is 0 to 15 Value After Reset: 0x0

cec_rx_data[0:15]

Description: CEC RX Data Register Array Address offset: i =0 to 15

These registers (8 bit each) are the buffers used for storing the received data (including header and data blocks).

Size: 8 bits

Offset: 0x7d20 + (i * 0x1)

Bits	Name	Attr	Description
7:0	databyte	R	Data byte[x], where x is 0 to 15 Value After Reset: 0x0

cec_lock

Description: CEC Buffer Lock Register

Size: 8 bits

Offset: 0x7d30

Bits	Name	Attr	Description
7:1			Reserved for future use.
0	locked_buffer	R/W	When a frame is received, this bit would be active. The CEC controller answers to all the messages with NACK until the CPU writes it to '0'. Value After Reset: 0x0

cec_wakeupctrl

Description: CEC Wake-up Control Register

After receiving a message in the CEC_RX_DATA1 (OPCODE) registers, the CEC engine verifies the message opcode[7:0] against one of the previously defined values to generate the wake-up status:

Wakeupsstatus is 1 when:

received opcode is 0x04 and opcode0x04en is 1 or
 received opcode is 0x0D and opcode0x0Den is 1 or
 received opcode is 0x41 and opcode0x41en is 1 or
 received opcode is 0x42 and opcode0x42en is 1 or
 received opcode is 0x44 and opcode0x44en is 1 or
 received opcode is 0x70 and opcode0x70en is 1 or
 received opcode is 0x82 and opcode0x82en is 1 or
 received opcode is 0x86 and opcode0x86en is 1

Wakeupsstatus is 0 when none of the previous conditions are true.

This formula means that the wake-up status (on CEC_STAT[6] register) is only '1' if the opcode[7:0] received is equal to one of the defined values and the corresponding enable bit of that defined value is set to '1'.

Size: 8 bits

Offset: 0x7d31

Bits	Name	Attr	Description
7	opcode0x86 en	R/W	OPCODE 0x86 wake up enable Value After Reset: 0x1
6	opcode0x82 en	R/W	OPCODE 0x82 wake up enable Value After Reset: 0x1
5	opcode0x70 en	R/W	OPCODE 0x70 wake up enable Value After Reset: 0x1
4	opcode0x44 en	R/W	OPCODE 0x44 wake up enable Value After Reset: 0x1
3	opcode0x42 en	R/W	OPCODE 0x42 wake up enable Value After Reset: 0x1
2	opcode0x41 en	R/W	OPCODE 0x41 wake up enable Value After Reset: 0x1
1	opcode0x0D en	R/W	OPCODE 0x0D wake up enable Value After Reset: 0x1
0	opcode0x04 en	R/W	OPCODE 0x04 wake up enable Value After Reset: 0x1

EDDC Registers

E-DDC Registers. Follow the link for the register to see a detailed description of the register.

Register	Offset	Description
i2cm_slave	0x7e00	I2C DDC Slave address Configuration Register
i2cm_address	0x7e01	I2C DDC Address Configuration Register
i2cm_datao	0x7e02	I2C DDC Data Write Register
i2cm_datai	0x7e03	I2C DDC Data read Register
i2cm_operation	0x7e04	I2C DDC RD/RD_EXT/WR Operation Register Read and write operation request. This register can only...

Register	Offset	Description
i2cm_int	0x7e05	I2C DDC Done Interrupt Register This register configures the I2C master interrupts.
i2cm_ctlint	0x7e06	I2C DDC error Interrupt Register This register configures the I2C master arbitration lost and not...
i2cm_div	0x7e07	I2C DDC Speed Control Register This register configures the division relation between master and...
i2cm_segaddr	0x7e08	I2C DDC Segment Address Configuration Register This register configures the segment address for...
i2cm_softrstz	0x7e09	I2C DDC Software Reset Control Register This register resets the I2C master.
i2cm_segptr	0x7e0a	I2C DDC Segment Pointer Register This register configures the segment pointer for extended RD/WR...
i2cm_ss_scl_hcnt_1_addr	0x7e0b	I2C DDC Slow Speed SCL High Level Control Register 1
i2cm_ss_scl_hcnt_0_addr	0x7e0c	I2C DDC Slow Speed SCL High Level Control Register 0
i2cm_ss_scl_lcnt_1_addr	0x7e0d	I2C DDC Slow Speed SCL Low Level Control Register 1
i2cm_ss_scl_lcnt_0_addr	0x7e0e	I2C DDC Slow Speed SCL Low Level Control Register 0
i2cm_fs_scl_hcnt_1_addr	0x7e0f	I2C DDC Fast Speed SCL High Level Control Register 1
i2cm_fs_scl_hcnt_0_addr	0x7e10	I2C DDC Fast Speed SCL High Level Control Register 0
i2cm_fs_scl_lcnt_1_addr	0x7e11	I2C DDC Fast Speed SCL Low Level Control Register 1
i2cm_fs_scl_lcnt_0_addr	0x7e12	I2C DDC Fast Speed SCL Low Level Control Register 0
i2cm_sda_hold	0x7e13	I2C DDC SDA Hold Register
i2cm_read_buff0	0x7e20	I2C Master Sequential Read Buffer Register 0
i2cm_read_buff1	0x7e21	I2C Master Sequential Read Buffer Register 1

Registers for Address Block: EDDC (Continued)

Register	Offset	Description
i2cm_read_buff2	0x7e22	I2C Master Sequential Read Buffer Register 2
i2cm_read_buff3	0x7e23	I2C Master Sequential Read Buffer Register 3
i2cm_read_buff4	0x7e24	I2C Master Sequential Read Buffer Register 4
i2cm_read_buff5	0x7e25	I2C Master Sequential Read Buffer Register 5
i2cm_read_buff6	0x7e26	I2C Master Sequential Read Buffer Register 6
i2cm_read_buff7	0x7e27	I2C Master Sequential Read Buffer Register 7
i2cm_scdc_update0	0x7e30	I2C SCDC Read Update Register 0
i2cm_scdc_update1	0x7e31	I2C SCDC Read Update Register 1

i2cm_slave

Description: I2C DDC Slave address Configuration Register

Size: 8 bits

Offset: 0x7e00

Bits	Name	Attr	Description
7			Reserved for future use.
6:0	slaveaddr	R/W	Slave address to be sent during read and write normal operations. Value After Reset: 0x0

i2cm_address

Description: I2C DDC Address Configuration Register

Size: 8 bits

Offset: 0x7e01

Bits	Name	Attr	Description
7:0	address	R/W	Register address for read and write operations Value After Reset: 0x0

i2cm_datao

Description: I2C DDC Data Write Register

Size: 8 bits

Offset: 0x7e02

Bits	Name	Attr	Description
7:0	datao	R/W	Data to be written on register pointed by address[7:0]. Value After Reset: 0x0

i2cm_datai

Description: I2C DDC Data read Register

Size: 8 bits

Offset: 0x7e03

Bits	Name	Attr	Description
7:0	datai	R	Data read from register pointed by address[7:0]. Value After Reset: 0x0

i2cm_operation

Description: I2C DDC RD/RD_EXT/WR Operation Register

Read and write operation request. This register can only be written; reading this register always results in 00h. Writing 1'b1 simultaneously to rd, rd_ext and wr requests is considered as a read (rd) request.

Size: 8 bits

Offset: 0x7e04

Bits	Name	Attr	Description
7:6			Reserved for future use.
5	busclear	W	Bus clear operation request. Value After Reset: 0x0
4	wr	W	Single byte write operation request. Value After Reset: 0x0
3	rd8_ext	W	Extended sequential read operation request. Eight bytes are read starting at the address defined in register field i2cm_address.address and stored in registers i2cm_read_buffx. Value After Reset: 0x0
2	rd8	W	Sequential read operation request. Eight bytes are read starting at the address defined in the i2cm_address.address register field and stored in the i2cm_read_buffx registers. Value After Reset: 0x0
1	rd_ext	W	After writing 1'b1 to rd_ext bit a extended data read operation is started (E-DDC read operation). Value After Reset: 0x0
0	rd	W	Single byte read operation request Value After Reset: 0x0

i2cm_int

Description: I2C DDC Done Interrupt Register This register configures the I2C master interrupts.

Size: 8 bits

Offset: 0x7e05

Bits	Name	Attr	Description
7			Reserved for future use.
6	read_req_ma sk	R/W	Read request interruption mask signal. Value After Reset: 0x1
5:3			Reserved for future use.
2	done_mask	R/W	Done interrupt mask signal. Value After Reset: 0x0
1:0			Reserved for future use.

i2cm_ctlint

Description: I2C DDC error Interrupt Register

This register configures the I2C master arbitration lost and not acknowledge error interrupts.

Size: 8 bits

Offset: 0x7e06

Bits	Name	Attr	Description
7			Reserved for future use.
6	nack_mask	R/W	Not acknowledge error interrupt mask signal. Value After Reset: 0x0
5:3			Reserved for future use.
2	arbitration_ mask	R/W	Arbitration error interrupt mask signal. Value After Reset: 0x0
1:0			Reserved for future use.

i2cm_div

Description: I2C DDC Speed Control Register

This register configures the division relation between master and scl clock.

Size: 8 bits

Offset: 0x7e07

Bits	Name	Attr	Description
7:4			Reserved for future use.
3	fast_std_mo de	R/W	Sets the I2C Master to work in Fast Mode or Standard Mode: 1: Fast Mode 0: Standard Mode Value After Reset: 0x1
2:0	spare	R/W	Reserved as "spare" bit with no associated functionality. Value After Reset: 0x3

i2cm_segaddr

Description: I2C DDC Segment Address Configuration Register

This register configures the segment address for extended R/W destination and is used for EDID reading operations, particularly for the Extended Data Read Operation for Enhanced DDC.

Size: 8 bits

Offset: 0x7e08

Bits	Name	Attr	Description
7			Reserved for future use.
6:0	seg_addr	R/W	I2C DDC Segment Address Configuration Register Value After Reset: 0x0

i2cm_softrstz

Description: I2C DDC Software Reset Control Register This register resets the I2C master.

Size: 8 bits

Offset: 0x7e09

Bits	Name	Attr	Description
7:1			Reserved for future use.
0	i2c_softrstz	R/W	I2C Master Software Reset. Active by writing a zero and auto cleared to one in the following cycle. Value After Reset: 0x1

i2cm_segptr

Description: I2C DDC Segment Pointer Register

This register configures the segment pointer for extended RD/WR request.

Size: 8 bits

Offset: 0x7e0a

Bits	Name	Attr	Description
7:0	segptr	R/W	I2C DDC Segment Pointer Register Value After Reset: 0x0

i2cm_ss_scl_hcnt_1_addr

Description: I2C DDC Slow Speed SCL High Level Control Register 1

Size: 8 bits

Offset: 0x7e0b

Bits	Name	Attr	Description
7:0	i2cmp_ss_scl_hcnt1	R/W	I2C DDC Slow Speed SCL High Level Control Register 1 Value After Reset: 0x0

i2cm_ss_scl_hcnt_0_addr

Description: I2C DDC Slow Speed SCL High Level Control Register 0

Size: 8 bits

Offset: 0x7e0c

Bits	Name	Attr	Description
7:0	i2cmp_ss_scl_hcnt0	R/W	I2C DDC Slow Speed SCL High Level Control Register 0 Value After Reset: 0x6c

i2cm_ss_scl_lcnt_1_addr

Description: I2C DDC Slow Speed SCL Low Level Control Register 1

Size: 8 bits

Offset: 0x7e0d

Bits	Name	Attr	Description
7:0	i2cmp_ss_scl_lcnt1	R/W	I2C DDC Slow Speed SCL Low Level Control Register 1 Value After Reset: 0x0

i2cm_ss_scl_lcnt_0_addr

Description: I2C DDC Slow Speed SCL Low Level Control Register 0

Size: 8 bits

Offset: 0x7e0e

Bits	Name	Attr	Description
7:0	i2cmp_ss_scl_lcnt0	R/W	I2C DDC Slow Speed SCL Low Level Control Register 0 Value After Reset: 0x7f

i2cm_fs_scl_hcnt_1_addr

Description: I2C DDC Fast Speed SCL High Level Control Register 1

Size: 8 bits

Offset: 0x7e0f

Bits	Name	Attr	Description
7:0	i2cmp_fs_scl_hcnt1	R/W	I2C DDC Fast Speed SCL High Level Control Register 1 Value After Reset: 0x0

i2cm_fs_scl_hcnt_0_addr

Description: I2C DDC Fast Speed SCL High Level Control Register 0

Size: 8 bits

Offset: 0x7e10

Bits	Name	Attr	Description
7:0	i2cmp_fs_scl_hcnt0	R/W	I2C DDC Fast Speed SCL High Level Control Register 0 Value After Reset: 0x11

i2cm_fs_scl_lcnt_1_addr

Description: I2C DDC Fast Speed SCL Low Level Control Register 1

Size: 8 bits

Offset: 0x7e11

Bits	Name	Attr	Description
7:0	i2cmp_fs_scl_lcnt1	R/W	I2C DDC Fast Speed SCL Low Level Control Register 1 Value After Reset: 0x0

i2cm_fs_scl_lcnt_0_addr

Description: I2C DDC Fast Speed SCL Low Level Control Register 0

Size: 8 bits

Offset: 0x7e12

Bits	Name	Attr	Description
7:0	i2cmp_fs_scl_lcnt0	R/W	I2C DDC Fast Speed SCL Low Level Control Register 0 Value After Reset: 0x24

i2cm_sda_hold

Description: I2C DDC SDA Hold Register

Size: 8 bits

Offset: 0x7e13

Bits	Name	Attr	Description
7:0	osda_hold	R/W	Defines the number of SFR clock cycles to meet tHD;DAT (300 ns) osda_hold = round_to_high_integer (300 ns / (1 / isfrclk_frequency)) Value After Reset: 0x9

i2cm_read_buff0

Description: I2C Master Sequential Read Buffer Register 0

Size: 8 bits

Offset: 0x7e20

Bits	Name	Attr	Description
7:0	i2cm_read_b uff0	R	Byte 0 of a I2C read buffer sequential read (from address i2cm_address) Value After Reset: 0x0

i2cm_read_buff1

Description: I2C Master Sequential Read Buffer Register 1

Size: 8 bits

Offset: 0x7e21

Bits	Name	Attr	Description
7:0	i2cm_read_buff1	R	Byte 1 of a I2C read buffer sequential read (from address i2cm_address+1) Value After Reset: 0x0

i2cm_read_buff2

Description: I2C Master Sequential Read Buffer Register 2

Size: 8 bits

Offset: 0x7e22

Bits	Name	Attr	Description
7:0	i2cm_read_buff2	R	Byte 2 of a I2C read buffer sequential read (from address i2cm_address+2) Value After Reset: 0x0

i2cm_read_buff3

Description: I2C Master Sequential Read Buffer Register 3

Size: 8 bits

Offset: 0x7e23

Bits	Name	Attr	Description
7:0	i2cm_read_buff3	R	Byte 3 of a I2C read buffer sequential read (from address i2cm_address+3) Value After Reset: 0x0

i2cm_read_buff4

Description: I2C Master Sequential Read Buffer Register 4

Size: 8 bits

Offset: 0x7e24

Bits	Name	Attr	Description
7:0	i2cm_read_buff4	R	Byte 4 of a I2C read buffer sequential read (from address i2cm_address+4) Value After Reset: 0x0

i2cm_read_buff5

Description: I2C Master Sequential Read Buffer Register 5

Size: 8 bits

Offset: 0x7e25

Bits	Name	Attr	Description
7:0	i2cm_read_buff5	R	Byte 5 of a I2C read buffer sequential read (from address i2cm_address+5) Value After Reset: 0x0

i2cm_read_buff6

Description: I2C Master Sequential Read Buffer Register 6

Size: 8 bits

Offset: 0x7e26

Bits	Name	Attr	Description
7:0	i2cm_read_buff6	R	Byte 6 of a I2C read buffer sequential read (from address i2cm_address+6) Value After Reset: 0x0

i2cm_read_buff7

Description: I2C Master Sequential Read Buffer Register 7

Size: 8 bits

Offset: 0x7e27

Bits	Name	Attr	Description
7:0	i2cm_read_b	R	Byte 7 of a I2C read buffer sequential read

	uff7		(from address i2cm_address+7) Value After Reset: 0x0
--	------	--	---

i2cm_scdc_update0

Description: I2C SCDC Read Update Register 0

Size: 8 bits

Offset: 0x7e30

Bits	Name	Attr	Description
7:0	i2cm_scdc_update0	R	Byte 0 of a SCDC I2C update sequential read Value After Reset: 0x0

i2cm_scdc_update1

Description: I2C SCDC Read Update Register 1

Size: 8 bits

Offset: 0x7e31

Bits	Name	Attr	Description
7:0	i2cm_scdc_update1	R	Byte 1 of a SCDC I2C update sequential read Value After Reset: 0x0

9.5 Interface Description

9.5.1 Video Input Source

In RK3288, the HDMI TX video source comes from VOP_BIG and VOP_LIT.

9.5.2 Audio Input Source

In RK3288, the HDMI TX audio source comes from I2S_8CH or SPDIF_2CH.

9.6 Application Notes

This chapter describes how to bring up HDMI transmitter in your system. As shown few examples below, these introduce the basically HDMI transmitter application, likes, the Hot Plug Detect, EDID read back, multiple audio format input and different video resolution displaying. You can easily configure these functions with proper registers value setting by HDMI TX APB BUS.

9.6.1 Initial Operation

The default HDMI transmitter is configured to 24bit RGB 1080P resolution video with 8 channel 48K sample I2S format audio input. It is easily for customer to turn on HDMI transmitter without doing more complex operation. Just do the step, reset the HDMI TX.

9.6.2 Hot Plug Detection

Hot Plug Detect is a special feature for HDMI transmitter spying the state on the HDMI port. You can control this function by using the interrupt signal and proper registers from the HDMI transmitter with few operations. The following is a step by step instruction for detecting the hot plug in and out.

Hot Plug in Steps:

Step1: Write 1'b1 in the phy_conf0.enhpdrxsense bit field register..

Step2: Plug HDMI receiver in.

Step3: Check the interrupt from signal pin_int.

If the pin_int shows high, that means the HDMI transmitter interrupt have generated.

Step4: Check the interrupt.

Read the phy_stat0.HPD bit field register. If HPD=0, the Hot Plug signal is low(no Sink(Receiver) detected). If HPD=1, the Hot Plug signal is high(Sink(Receiver) detected).

Hot Plug out Steps:

Step1: HDMI transmitter at working state.

Step2: Plug HDMI receiver out.

Step3: Check the interrupt from signal pin_int.

If the pin_int shows high, that means the HDMI transmitter interrupt have generated.

Step4: Check the interrupt.

Read the phy_stat0.HPD bit field register. If HPD=0, the Hot Plug signal is low(no Sink(Receiver) detected). If HPD=1, the Hot Plug signal is high(Sink(Receiver) detected).

9.6.3 Reading EDID

Read EDID is a function that can make the HDMI transmitter to read the HDMI receiver's Extended Display Identification Data (EDID) in order to discover the HDMI receiver's configuration and capabilities. HDMI transmitter can choose the appropriate audio and video format for playing and displaying by the HDMI receiver through the use of the EDID. Besides, HDMI transmitter support the reading Enhanced Extended Display Identification Data (E-EDID) if HDMI receiver have this enhanced structure.

The following describes how to read E-EDID through HDMI transmitter. The total E-EDID is 512bytes data, which is divided into 2 segments. Each segment has 256bytes data. The Read E-EDID function is only read 64bytes data from HDMI receiver at each time. So, you must read 8 times that can read total 512bytes data back.

The related registers offset is 0x7E00.

Normal read E-EDID 512bytes Steps:

Step1: Set I2C slave address.

Write i2cm_slave.slaveaddr[6:0] bit field register.

Step2: Set I2C register address.

Write i2cm_slave.address[7:0] bit field register.

Step3: Activate Sequential Real operation.

Write "1" in the i2cm_operation.rd8 bit field register.

Step4: Wait for interruption

Wait for i2cmasterdone interrupt in the ih_i2cm_stat0 register

Step5: Read data result

Read data of registers i2cm_read_buff0[7:0] to i2cm_read_buff7[7:0]

Read E-EDID extended sequential read operation Steps:

Step1: Set I2C slave address.

Write i2cm_slave.slaveaddr[6:0] bit field register.

Step2: Set I2C segment address.

Write the i2cm_segaddr.seg_addr bit field register.

Step3: Set I2C segment pointer.

Write i2cm_segpdr.segpdr bit field register.

Step4: Activate Read operation.

Write "1" in the i2cm_operation.rd8_ext bit field register.

Step5: Wait for interruption.

Wait for i2cmasterdone interrupt in the ih_i2cm_stat0 register

Step6: Read data result.

Read data of registers i2cm_read_buff0[7:0] to i2cm_read_buff7[7:0].

9.6.4 Audio input configuration

HDMI transmitter audio support either SPDIF or four channel I2S input. SPDIF input supports audio sampling rates from 32 to 192 KHz. The I2S input supports from 2-channel to 8-channel audio up to 192 KHz. The default audio format is I2S input with 8 channels. The audio sample rate is 48K.

The following describes how to configure audio input format. The related register offset is from 0x3100.

Configure Audio Input Format with I2S Steps:

Step1: Select I2S input.

Write "1" in the aud_conf0.i2s_select bit field register.

Step2: Enable I2S inputs:

Write "1" in the aud_conf0.i2s_in_en[3:0] bit field register.

Step3: Set I2S Mode [Standard | Right-justified | Left-justified | Burst1 | Burst2]:

Write the aud_conf1.i2s_mode[2:0] bit field register.

Step4: Set I2S data width [16 bits up to 24 bits]:

Write the aud_conf1.i2s_width[4:0] bit field.

Configure Audio Input Format with SPDIF Steps:

Step1: Select SPDIF input.

Write "0" in the aud_conf0.i2s_select bit field register.

Step2: Set S/PDIF Linear-PCM or Non-Linear PCM audio samples:

Write the aud_spdif1.setnlpcm bit field register.

Step3: Set SPDIF data width [16 bits up to 24 bits]:

Write the aud_spdif1.spdif_width[4:0] bit field.

Configure Audio Parameters Steps:

Step1: Set Audio input frequency clock FS ratio factor [128 Fs | 256 Fs | 512 Fs]:

Write the aud_inputclkfs.lfsfactor bit field register.

Step2: Set Audio fixed N factor for Audio Clock Regeneration. This factor depends on the audio sampling rate and video mode.

Write the aud_n1.audN, aud_n2.audN, and aud_n3.audN bit field registers.

Step3: Set Audio CTS factor for Audio Clock Regeneration. This factor can be generated automatically or manually.

For Automatic CTS generation

Write "0" on the bit field "CTS_manual", Register 0x3205: AUD_CTS3

For Manual CTS setting

Write "1" in the aud_cts3.CTS_manual register bit field.

Write the aud_cts1.audCTS, aud_cts2.audCTS, aud_cts3.audCTS bit field registers.

Step4: Enable Audio sampler block:

Write "0" in the mc_clkdis.audclk_disable bit field register.

9.6.5 Video input configuration

HDMI transmitter support RGB/YCbCr 24/30bit video input with different resolution. The

default video format is RGB24bit input at resolution of 1080P@60. The following describes how to configure video input format into RGB24bit input at resolution of 480P@60, 720P@60 or 1080P@60.

HDMI pin_vclk cannot get invert.

Video input requirement:

24bit RGB 4:4:4 Source.

Resolution is 480P@60, 720P@60 or 1080P@60.

Configure Video Input Format Steps:

Step1: To select the Video Mapping input mode (RGB444, YCC444, YCC422).

Write the video code in the tx_invid0.video_mapping bit field register.

Step2: Set video timing information configuration:

Write the fc_invidconf.vsync_in_polarity register.

Write the fc_invidconf.hsync_in_polarity register.

Write the fc_invidconf.de_in_polarity register.

Write the fc_invidconf.r_v_blank_in_osc register.

Write the fc_invidconf.in_I_P register.

H active pixels

- Write the fc_inhactiv1.H_in_activ register.

- Write the fc_inhactiv0.H_in_activ register.

V active pixels

- Write the fc_invactiv1.V_in_activ register.

- Write the fc_invactiv0.V_in_activ register.

H blanking pixels

Write the fc_inhblank0.H_in_blank register.

V blanking pixels

Write the fc_invblank.V_in_blank register.

HSync offset

Write the fc_hsyncindelay0.H_in_delay register.

VSync offset

Write the fc_vsyncindelay0.V_in_delay register.

HSync pulse width

Write the fc_hsyncinwidth0.H_in_width register.

VSync pulse width

Write the fc_vsyncinwidth0.V_in_width register.

Step3: Select DVI or HDMI mode:

Write "0" for DVI in the fc_invidconf.DVI_modez bit field register.

Write "1" for HDMI in the fc_invidconf.DVI_modez bit field register.

The detail configuration for AVI information, please refer to the HDMI specification (8.2.1) and CEA-861-D (6.3).

9.6.6 HDMI MPLL CONFIGURE

HDMI transmitter have a PLL for generate the TMDS clock. Configuring the PLL related parameter use the i2c master interface.

Configure HDMI PLL Step:

Step1:Place the PHY in configuration mode by writing 8'h32 to the phy_conf0 register.

Step2:Reset the PHY by writing 0x01 in the mc_phyrstz register.

Step3:Write the desired color depth and the pixel repetition in the vp_pr_cd register.

Step4:After a PHY-dependent time, it is required to lift the reset by writing 0x00 to the mc_phyrstz register.

Step5:Set the PHY slave address by writing 0x69 in the phy_i2cm_slave register.

Step6:According to dwc_hdmi_tx_ew_6gbps-gf28slp18_databook_rockchip.pdf, (Appendix B:MPLL Configuration)you are required to look up the configuration for your intended video mode and write those values to the PHY I2C interface. The baseline flow to write to the

PHY through the I2C interface is as follows:

- i. Write the register address in the phy_i2cm_address register.
- ii. Write data in the phy_i2cm_datao_1 (MSB, [15:8]) and phy_i2cm_datao_0 (LSB, [7:0]) registers.
- iii. Initialize the write operation by writing 8'h10 in the phy_i2cm_operation register.
- iv. Wait for a done interruption from the I2C master.

Step7: After all of the required PHY I2C registers have been configured, you now need to place the PHY in power-on mode by setting the txpwron bit in the PHY_CONF0 register, writing 8'h2a to the phy_conf0 register.

The mc_phyrstz register controls the PHY reset.

Step8: At the end of the PHY configuration, it is recommended to check if the PHY PLL is locked.

Read the phy_stat0.tx_phy_lock bit field register.

If tx_phy_lock = 0, the PLL is not locked.

If tx_phy_lock = 1, the PLL is locked.

9.6.7 CEC OPERATION

The CEC line is used for high-level user control of HDMI-connected devices.The HDMI TX contain CEC TX operations and CEC RX operations.

You can control this function by using the interrupt signal and proper registers from the HDMI transmitter with few operations. The register offset is from 0x7D00.

Configure The CEC Step:

Step1:Write the CEC logical address to cec_addr_l,cec_addr_h register

Step2:Write the size of the frame in bytes which are available in the transmitter data buffer to cec_tx_cnt register

Step3:Write the desired CEC data(including header and data blocks) to cec_tx_data0 to cec_tx_data15

Step4:Write 1 to cec_ctrl.send register, to start the cec transmit.

9.6.8 HDCP OPERATION

HDCP is designed to protect the transmission of Audiovisual Content between an HDCP Transmitter and an HDCP Receiver. You can control this function by using the interrupt signal and proper registers from the HDMI transmitter with few operations.

The following is a step by step instruction for HDCP operation.

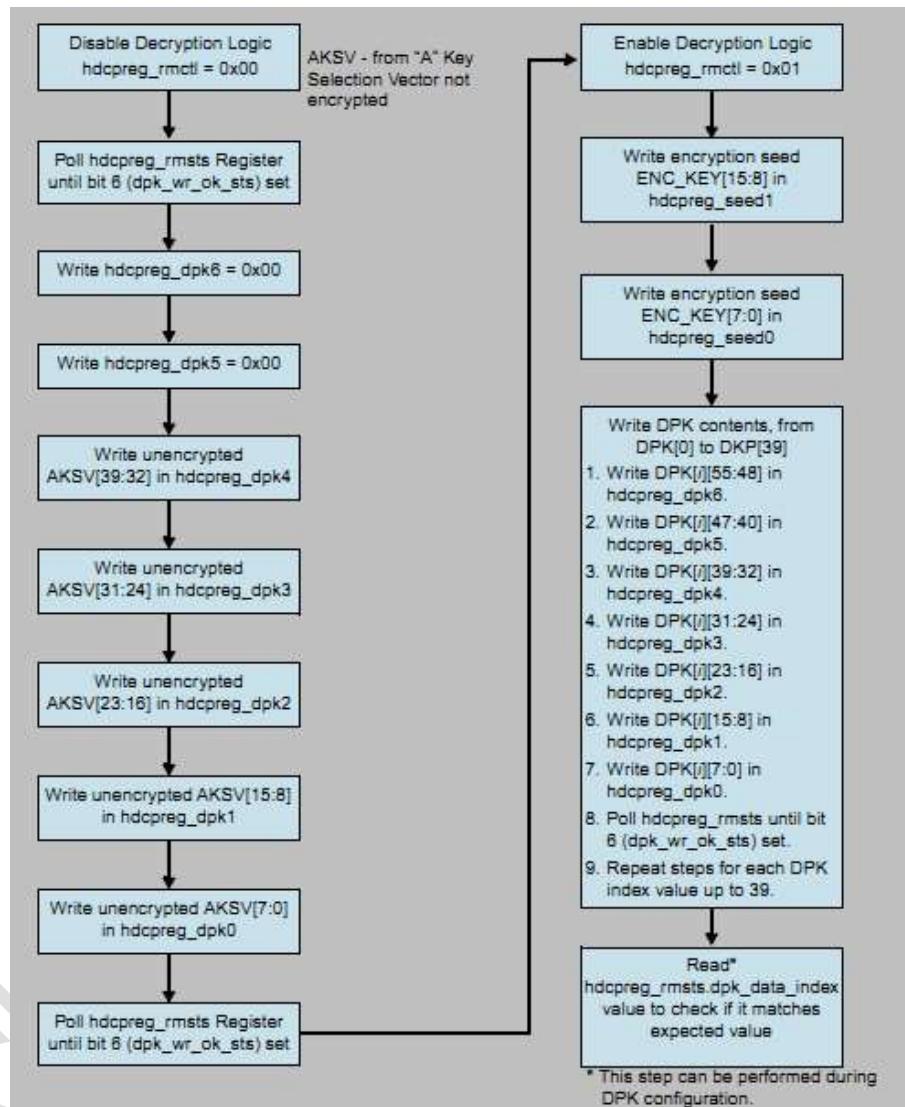
HDCP Access KSV Memory Step:

Step1: Request access to KSV memory through setting a_ksvmemctrl.KSVMEMrequest to 1'b1 and pool a_ksvmemctrl.KSVMEMaccess until this value is 1'b1 (access granted).

Step2: Read VH', M0, Bstatus, and the KSV FIFO.

The data is stored in the revocation memory, as provided in the "Address Mapping for Maximum Memory Allocation" table in the hdmi_databook.

HDCP Key Write Step:



Chapter 10 LVDS

10.1 Overview

LVDS transmitter converts a CMOS signal into a low-voltage differential signal. Using a differential signal reduces the system's susceptibility to noise and EMI emissions. In addition, using a differential signal can deliver high speeds. This results in a very cost-effective solution to some of the greatest bandwidth bottlenecks in many transmission applications.

LVDS supports following features:

- Comply with the TIA/EIA-644-A LVDS standard
- Combine LVTTL IO, support LVDS/LVTTL data output
- Support reference clock frequency range from 10Mhz to 148.5Mhz
- Support LVDS RGB 30/24/18bits color data transfer
- Support VESA/JEIDA LVDS data format transfer
- Support LVDS single channel and double channel data transfer, every channel include 5 data lanes and 1 clock lane
- Support MSB mode and LSB mode data transfer
- Support APB slave bus interface
- Support low power mode

10.2 Block Diagram

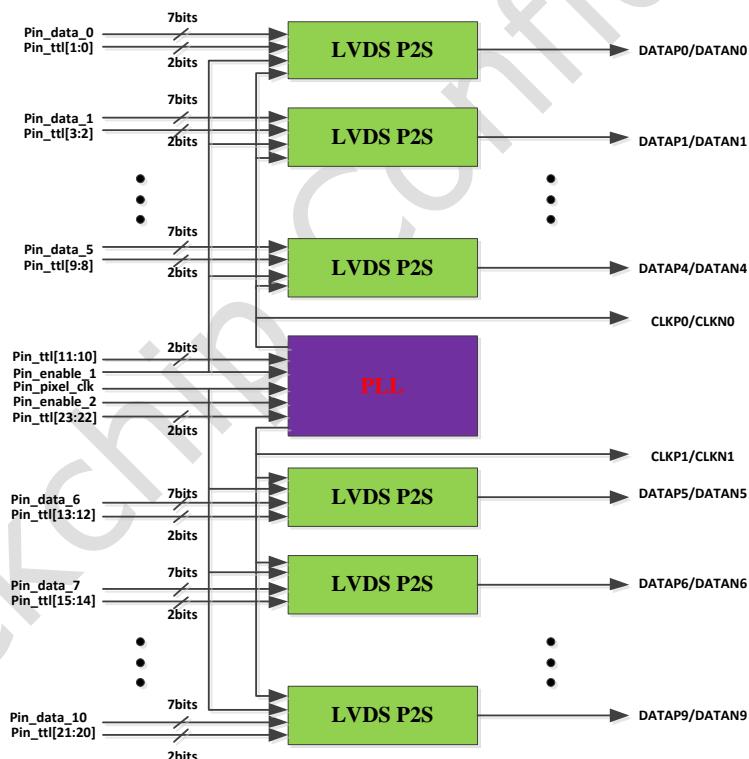


Fig. 10-1 LVDS Block Diagram

Fig.7-1 shows the brief block diagram of the innosilicon LVDS/TTL PHY, which includes ten LVDS P2S modules and one PLL module.

PLL is responsible for multiplying the pin_pixel_clk by 7, which generates a 7X clock used to deserialize the parallel data.

LVDS P2S module implements the parallel to serial function and transmits the TTL data directly.

10.3 Function Description

10.3.1 Transmitter with Two 35:5 Data Channels

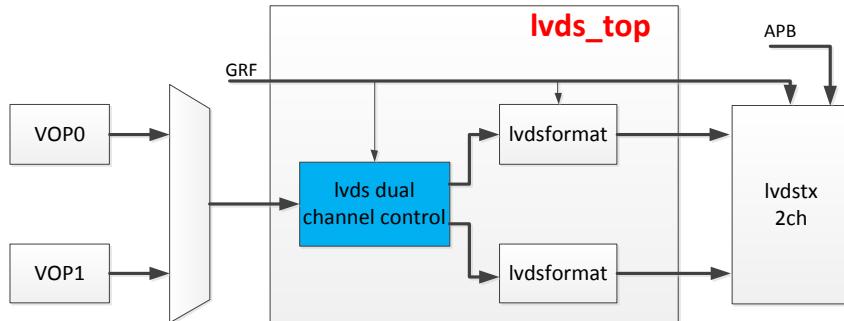


Fig. 10-2 LVDS in SoC

There are two transfer channels in LVDS, every channel include 4 data lanes and 1 clock lane. LVDS can work at single channel mode or double channel mode.

The LVDS output data timing is showed as the following figure,

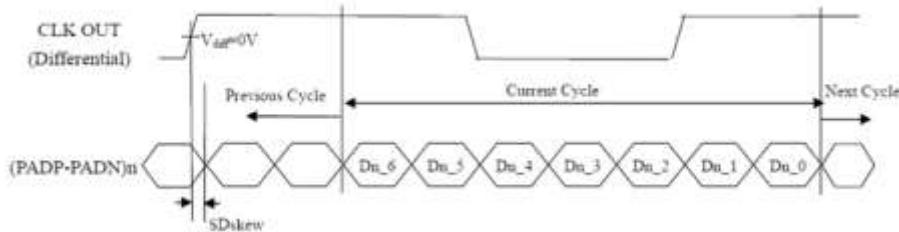


Fig. 10-3 LVDS output data timing

10.3.2 LVDS Format

Lvdsformat converts VOP RGB interface to LVDS format data. The lvdsformat support RGB 10/8/6bits color data input. There are two lvdsformat modules in the lvds_top.

When LVDS works at double channel mode, both the lvdsformat modules are necessary. One is for odd cycle RGB data format convert, and the other is for even cycle RGB data format convert. The frequency of LVDS output clock is half of the dclk.

When LVDS works at single channel mode, only one lvdsformat module is necessary. User can configure GRF register to select which lvdsformat converts the VOP RGB data. The frequency of LVDS output clock is equal to the dclk.

Table 10-1 is the MSB mapping relationship between the input data and output data of lvdsformat module (single channel mode). The LSB mapping relationship is opposite to MSB.

Table 10-1 MSB mapping relationship (single channel mode)

Lvds-format id	Serial Channel	Data Bits	RGB10 Bits		RGB8 Bits			RGB6 bits
			format -1	format -2	format -1	format -2	format -3	
lvds-format *	DATA0	DATA0[0]	R0	R4	R0	R2	R2	R0
		DATA0[1]	R1	R5	R1	R3	R3	R1
		DATA0[2]	R2	R6	R2	R4	R4	R2
		DATA0[3]	R3	R7	R3	R5	R5	R3

Lvds-format	Serial Channel	Data Bits	RGB10 Bits		RGB8 Bits			RGB6 bits
DATA0	DATA0	DATA0[4]	R4	R8	R4	R6	R6	R4
		DATA0[5]	R5	R9	R5	R7	R7	R5
		DATA0[6]	G0	G4	G0	G2	G2	G0
	DATA1	DATA1[0]	G1	G5	G1	G3	G3	G1
		DATA1[1]	G2	G6	G2	G4	G4	G2
		DATA1[2]	G3	G7	G3	G5	G5	G3
		DATA1[3]	G4	G8	G4	G6	G6	G4
		DATA1[4]	G5	G9	G5	G7	G7	G5
		DATA1[5]	B0	B4	B0	B2	B2	B0
		DATA1[6]	B1	B5	B1	B3	B3	B1
	DATA2	DATA2[0]	B2	B6	B2	B4	B4	B2
		DATA2[1]	B3	B7	B3	B5	B5	B3
		DATA2[2]	B4	B8	B4	B6	B6	B4
		DATA2[3]	B5	B9	B5	B7	B7	B5
		DATA2[4]	H SYNC	H SYNC	H SYNC	H SYNC	H SYNC	H SYNC
		DATA2[5]	V SYNC	V SYNC	V SYNC	V SYNC	V SYNC	V SYNC
		DATA2[6]	DEN	DEN	DEN	DEN	DEN	DEN
	DATA3	DATA3[0]	R6	R2	R6	R0	GND	GND
		DATA3[1]	R7	R3	R7	R1	GND	GND
		DATA3[2]	G6	G2	G6	G0	GND	GND
		DATA3[3]	G7	G3	G7	G1	GND	GND
		DATA3[4]	B6	B2	B6	B0	GND	GND
		DATA3[5]	B7	B3	B7	B1	GND	GND
		DATA3[6]	GND	GND	GND	GND	GND	GND
	DATA4	DATA4[0]	R8	R0	GND	GND	GND	GND
		DATA4[1]	R9	R1	GND	GND	GND	GND
		DATA4[2]	G8	G0	GND	GND	GND	GND
		DATA4[3]	G9	G1	GND	GND	GND	GND
		DATA4[4]	B8	B0	GND	GND	GND	GND
		DATA4[5]	B9	B1	GND	GND	GND	GND
		DATA4[6]	GND	GND	GND	GND	GND	GND
	CLKOUT	CLKOUT	DCLK	DCLK	DCLK	DCLK	DCLK	DCLK

Table 10-2 is the MSB mapping relationship between the input data and output data of Lvdsformat module (double channel mode). The LSB mapping relationship is opposite to MSB.

Table 10-2 MSB mapping relationship (double channel mode)

Lvds-format id	Serial Channel	Data Bits	RGB10 Bits		RGB8 Bits			RGB6 bits
			format -1	format -2	format -1	format -2	format -3	
Lvds-format 0	DATA0	DATA0[0]	OR0	OR4	OR0	OR2	OR2	OR0
		DATA0[1]	OR1	OR5	OR1	OR3	OR3	OR1
		DATA0[2]	OR2	OR6	OR2	OR4	OR4	OR2

Lvds-format	Serial Channel	Data Bits	RGB10 Bits		RGB8 Bits			RGB6 bits
Lvds-format 1	DATA0	DATA0[3]	OR3	OR7	OR3	OR5	OR5	OR3
		DATA0[4]	OR4	OR8	OR4	OR6	OR6	OR4
		DATA0[5]	OR5	OR9	OR5	OR7	OR7	OR5
		DATA0[6]	OG0	OG4	OG0	OG2	OG2	OG0
	DATA1	DATA1[0]	OG1	OG5	OG1	OG3	OG3	OG1
		DATA1[1]	OG2	OG6	OG2	OG4	OG4	OG2
		DATA1[2]	OG3	OG7	OG3	OG5	OG5	OG3
		DATA1[3]	OG4	OG8	OG4	OG6	OG6	OG4
		DATA1[4]	OG5	OG9	OG5	OG7	OG7	OG5
		DATA1[5]	OB0	OB4	OB0	OB2	OB2	OB0
		DATA1[6]	OB1	OB5	OB1	OB3	OB3	OB1
	DATA2	DATA2[0]	OB2	OB6	OB2	OB4	OB4	OB2
		DATA2[1]	OB3	OB7	OB3	OB5	OB5	OB3
		DATA2[2]	OB4	OB8	OB4	OB6	OB6	OB4
		DATA2[3]	OB5	OB9	OB5	OB7	OB7	OB5
		DATA2[4]	H SYNC	H SYNC	H SYNC	H SYNC	H SYNC	H SYNC
		DATA2[5]	V SYNC	V SYNC	V SYNC	V SYNC	V SYNC	V SYNC
		DATA2[6]	DEN	DEN	DEN	DEN	DEN	DEN
	DATA3	DATA3[0]	OR6	OR2	OR6	OR0	GND	GND
		DATA3[1]	OR7	OR3	OR7	OR1	GND	GND
		DATA3[2]	OG6	OG2	OG6	OG0	GND	GND
		DATA3[3]	OG7	OG3	OG7	OG1	GND	GND
		DATA3[4]	OB6	OB2	OB6	OB0	GND	GND
		DATA3[5]	OB7	OB3	OB7	OB1	GND	GND
		DATA3[6]	GND	GND	GND	GND	GND	GND
	DATA4	DATA4[0]	OR8	OR0	GND	GND	GND	GND
		DATA4[1]	OR9	OR1	GND	GND	GND	GND
		DATA4[2]	OG8	OG0	GND	GND	GND	GND
		DATA4[3]	OG9	OG1	GND	GND	GND	GND
		DATA4[4]	OB8	OB0	GND	GND	GND	GND
		DATA4[5]	OB9	OB1	GND	GND	GND	GND
		DATA4[6]	GND	GND	GND	GND	GND	GND
	CLKOUT	CLKOUT	DCLK/2	DCLK/2	DCLK/2	DCLK/2	DCLK/2	DCLK/2
Lvds-format 1	DATA0	DATA0[0]	ER0	ER4	ER0	ER2	ER2	ER0
		DATA0[1]	ER1	ER5	ER1	ER3	ER3	ER1
		DATA0[2]	ER2	ER6	ER2	ER4	ER4	ER2
		DATA0[3]	ER3	ER7	ER3	ER5	ER5	ER3
		DATA0[4]	ER4	ER8	ER4	ER6	ER6	ER4
		DATA0[5]	ER5	ER9	ER5	ER7	ER7	ER5
		DATA0[6]	EG0	EG4	EG0	EG2	EG2	EG0
	DATA1	DATA1[0]	EG1	EG5	EG1	EG3	EG3	EG1
		DATA1[1]	EG2	EG6	EG2	EG4	EG4	EG2

lvds-format	Serial Channel	Data Bits	RGB10 Bits		RGB8 Bits			RGB6 bits
DATA1		DATA1[2]	EG3	EG7	EG3	EG5	EG5	EG3
		DATA1[3]	EG4	EG8	EG4	EG6	EG6	EG4
		DATA1[4]	EG5	EG9	EG5	EG7	EG7	EG5
		DATA1[5]	EB0	EB4	EB0	EB2	EB2	EB0
		DATA1[6]	EB1	EB5	EB1	EB3	EB3	EB1
	DATA2	DATA2[0]	EB2	EB6	EB2	EB4	EB4	EB2
		DATA2[1]	EB3	EB7	EB3	EB5	EB5	EB3
		DATA2[2]	EB4	EB8	EB4	EB6	EB6	EB4
		DATA2[3]	EB5	EB9	EB5	EB7	EB7	EB5
		DATA2[4]	H SYNC	H SYNC	H SYNC	H SYNC	H SYNC	H SYNC
	DATA3	DATA2[5]	V SYNC	V SYNC	V SYNC	V SYNC	V SYNC	V SYNC
		DATA2[6]	DEN	DEN	DEN	DEN	DEN	DEN
		DATA3[0]	ER6	ER2	ER6	ER0	GND	GND
		DATA3[1]	ER7	ER3	ER7	ER1	GND	GND
		DATA3[2]	EG6	EG2	EG6	EG0	GND	GND
		DATA3[3]	EG7	EG3	EG7	EG1	GND	GND
		DATA3[4]	EB6	EB2	EB6	EB0	GND	GND
	DATA4	DATA3[5]	EB7	EB3	EB7	EB1	GND	GND
		DATA3[6]	GND	GND	GND	GND	GND	GND
		DATA4[0]	ER8	ER0	GND	GND	GND	GND
		DATA4[1]	ER9	ER1	GND	GND	GND	GND
		DATA4[2]	EG8	EG0	GND	GND	GND	GND
		DATA4[3]	EG9	EG1	GND	GND	GND	GND
		DATA4[4]	EB8	EB0	GND	GND	GND	GND
		DATA4[5]	EB9	EB1	GND	GND	GND	GND
		DATA4[6]	GND	GND	GND	GND	GND	GND

10.3.3 GRF Relative Register Description

GRF_SOC_CON6[3] (grf_con_lvds_lcdc_sel):

- 1'b0: lvds video source from vop0;
- 1'b1: lvds video source from vop1;

GRF_SOC_CON7[2:0] (grf_lvds_con_select):

- 3'b000: select RGB8 bits format-1;
- 3'b001: select RGB8 bits format-2;
- 3'b010: select RGB8 bits format-3;
- 3'b011: select RGB6 bits format;
- 3'b100: select RGB10 bits format-1;
- 3'b101: select RGB10 bits format-2;

GRF_SOC_CON7[3] (grf_lvds_con_msbsel):

- 1'b0: LSB for lvdsformat;
- 1'b1: MSB for lvds format;

GRF_SOC_CON7[4] (grf_lvds_con_chasel):

- 1'b0: single channel mode;
- 1'b1: double channel mode;

GRF_SOC_CON7[5] (grf_lvds_con_startsel):

- 1'b0: when lvds works at double channel mode, select lvdsformat 0 for odd pixel data convert and lvdsformat 1 for even pixel data convert;
- 1'b1: when lvds works at double channel mode, select lvdsformat 0 for even pixel data

convert and lvdsformat 1 for odd pixel data convert;
GRF_SOC_CON7[6] (grf_lvds_con_ttl_en):

- 1'b0: disable lvds ttl mode;
- 1'b1: enable lvds ttl mode;

GRF_SOC_CON7[7] (grf_lvds_con_startphase):

- 1'b0: dclk_div2 start phase reset to 0 at beginning of hs;
- 1'b1: dclk_div2 start phase reset to 1 at beginning of hs;

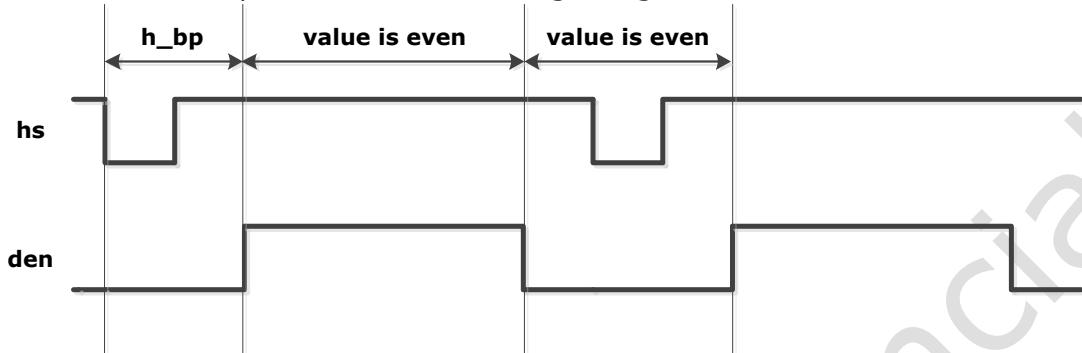


Fig. 10-4 LVDS h_bp timing diagram

when h_bp is odd, grf_lvds_con_startphase need be configured to 1'b1;
when h_bp is even, grf_lvds_con_startphase need be configured to 1'b0;

GRF_SOC_CON7[8] (grf_lvds_con_clkinv):

- 1'b0: not invert the clock to LVDS from lvds_top;
- 1'b1: invert the clock to LVDS from lvds_top;

GRF_SOC_CON7[9] (grf_lvds_con_hs_polarity):

- 1'b0: hsync polarity low active;
- 1'b1: hsync polarity high active;

GRF_SOC_CON7[10] (grf_lvds_con_den_polarity):

- 1'b0: den polarity high active;
- 1'b1: den polarity low active;

GRF_SOC_CON7[11] (grf_lvds_con_enable_1):

- 1'b0: LVDS channel 1 disable;
- 1'b1: LVDS channel 1 enable;

GRF_SOC_CON7[12] (grf_lvds_con_enable_2):

- 1'b0: LVDS channel 2 disable;
- 1'b1: LVDS channel 2 enable;

GRF_SOC_CON7[15] (grf_lvds_pwrdown):

- 1'b0: LVDS not power down;
- 1'b1: LVDS power down;

10.4 Register Description

This section describes the control/status registers of the design.

10.4.1 Registers Summary

Name	Offset	Size	Reset Value	Description
LVDS_channel0_reg00	0x0000	W	0x000000bf	LVDS register
LVDS_channel0_reg01	0x0004	W	0x0000003f	LVDS register
LVDS_channel0_reg02	0x0008	W	0x0000007e	LVDS register
LVDS_channel0_reg03	0x000c	W	0x00000046	LVDS register
LVDS_channel0_reg04	0x0010	W	0x00000000	LVDS register
LVDS_channel0_reg05	0x0014	W	0x00000000	LVDS register
LVDS_config_reg0c	0x0030	W	0x00000000	LVDS register
LVDS_channel0_reg0d	0x0034	W	0x0000000a	LVDS register
LVDS_channel0_reg20	0x0080	W	0x00000045	LVDS register

Name	Offset	Size	Reset Value	Description
LVDS_config_reg21	0x0084	W	0x00000000	LVDS register
LVDS_channel1_reg40	0x0100	W	0x000000bf	LVDS register
LVDS_channel1_reg41	0x0104	W	0x0000003f	LVDS register
LVDS_channel1_reg42	0x0108	W	0x0000007e	LVDS register
LVDS_channel1_reg43	0x010c	W	0x00000046	LVDS register
LVDS_channel1_reg44	0x0110	W	0x00000000	LVDS register
LVDS_channel1_reg45	0x0114	W	0x00000000	LVDS register
LVDS_channel1_reg4d	0x0134	W	0x0000000a	LVDS register
LVDS_channel1_reg60	0x0180	W	0x00000045	LVDS register

Notes: **Size** : **B** - Byte (8 bits) access, **HW** - Half WORD (16 bits) access, **W** - WORD (32 bits) access

10.4.2 Detail Register Description

LVDS_channel0_reg00

Address: Operational Base + offset (0x0000)

LVDS register

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7	RW	0x1	lvds_mode_en 1'b1: enable lvds mode; 1'b0: disable lvds mode;
6	RW	0x0	ttl_mode_en 1'b1: enable ttl mode; 1'b0: disable ttl mode;
5	RW	0x1	lane_en_ck 1'b1: enable lane_ck; 1'b0: disable lane_ck;
4	RW	0x1	lane_en_4 1'b1: enable lane_4; 1'b0: disable lane_4;
3	RW	0x1	lane_en_3 1'b1: enable lane_3; 1'b0: disable lane_3;
2	RW	0x1	lane_en_2 1'b1: enable lane_2; 1'b0: disable lane_2;
1	RW	0x1	lane_en_1 1'b1: enable lane_1; 1'b0: disable lane_1;
0	RW	0x1	lane_en_0 1'b1: enable lane_0; 1'b0: disable lane_0;

LVDS_channel0_reg01

Address: Operational Base + offset (0x0004)

LVDS register

Bit	Attr	Reset Value	Description
31:6	RO	0x0	reserved
5	RW	0x1	biasen_ck 1'b1: enable lane_ck bias; 1'b0: disable lane_ck bias;
4	RW	0x1	biasen_4 1'b1: enable lane_4 bias; 1'b0: disable lane_4 bias;
3	RW	0x1	biasen_3 1'b1: enable lane_3 bias; 1'b0: disable lane_3 bias;
2	RW	0x1	biasen_2 1'b1: enable lane_2 bias; 1'b0: disable lane_2 bias;
1	RW	0x1	biasen_1 1'b1: enable lane_1 bias; 1'b0: disable lane_1 bias;
0	RW	0x1	biasen_0 1'b1: enable lane_0 bias; 1'b0: disable lane_0 bias;

LVDS_channel0_reg02

Address: Operational Base + offset (0x0008)

LVDS register

Bit	Attr	Reset Value	Description
31:7	RO	0x0	reserved
6	RW	0x1	lane_lvds_en_ck 1'b1: enable lane_ck lvds mode; 1'b0: disable lane_ck lvds mode;
5	RW	0x1	lane_lvds_en_4 1'b1: enable lane_4 lvds mode; 1'b0: disable lane_4 lvds mode;
4	RW	0x1	lane_lvds_en_3 1'b1: enable lane_3 lvds mode; 1'b0: disable lane_3 lvds mode;
3	RW	0x1	lane_lvds_en_2 1'b1: enable lane_2 lvds mode; 1'b0: disable lane_2 lvds mode;
2	RW	0x1	lane_lvds_en_1 1'b1: enable lane_1 lvds mode; 1'b0: disable lane_1 lvds mode;
1	RW	0x1	lane_lvds_en_0 1'b1: enable lane_0 lvds mode; 1'b0: disable lane_0 lvds mode;

Bit	Attr	Reset Value	Description
0	RW	0x0	pll_fbdv_8 pll_fbdv[8];

LVDS_channel0_reg03

Address: Operational Base + offset (0x000c)

LVDS register

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RW	0x46	pll_fbdv_7_to_0 pll_fbdv[7:0];

LVDS_channel0_reg04

Address: Operational Base + offset (0x0010)

LVDS register

Bit	Attr	Reset Value	Description
31:6	RO	0x0	reserved
5	RW	0x0	lane_ttl_en_ck 1'b1: enable lane_ck ttl mode; 1'b0: disable lane_ck ttl mode;
4	RW	0x0	lane_ttl_en_4 1'b1: enable lane_4 ttl mode; 1'b0: disable lane_4 ttl mode;
3	RW	0x0	lane_ttl_en_3 1'b1: enable lane_3 ttl mode; 1'b0: disable lane_3 ttl mode;
2	RW	0x0	lane_ttl_en_2 1'b1: enable lane_2 ttl mode; 1'b0: disable lane_2 ttl mode;
1	RW	0x0	lane_ttl_en_1 1'b1: enable lane_1 ttl mode; 1'b0: disable lane_1 ttl mode;
0	RW	0x0	lane_ttl_en_0 1'b1: enable lane_0 ttl mode; 1'b0: disable lane_0 ttl mode;

LVDS_channel0_reg05

Address: Operational Base + offset (0x0014)

LVDS register

Bit	Attr	Reset Value	Description
31:6	RO	0x0	reserved
5	RW	0x0	lane_ttl_ctrl_ck 1'b1: enable lane_ck ttl data transmission; 1'b0: disable lane_ck ttl data transmission;

Bit	Attr	Reset Value	Description
4	RW	0x0	lane_ttl_ctr_4 1'b1: enable lane_4 ttl data transmission; 1'b0: disable lane_4 ttl data transmission;
3	RW	0x0	lane_ttl_ctr_3 1'b1: enable lane_3 ttl data transmission; 1'b0: disable lane_3 ttl data transmission;
2	RW	0x0	lane_ttl_ctr_2 1'b1: enable lane_2 ttl data transmission; 1'b0: disable lane_2 ttl data transmission;
1	RW	0x0	lane_ttl_ctr_1 1'b1: enable lane_1 ttl data transmission; 1'b0: disable lane_1 ttl data transmission;
0	RW	0x0	lane_ttl_ctr_0 1'b1: enable lane_0 ttl data transmission; 1'b0: disable lane_0 ttl data transmission;

LVDS_config_reg0c

Address: Operational Base + offset (0x0030)

LVDS register

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RW	0x00	enable_pll 8'h00: enable pll;

LVDS_channel0_reg0d

Address: Operational Base + offset (0x0034)

LVDS register

Bit	Attr	Reset Value	Description
31:5	RO	0x0	reserved
4:0	RW	0x0a	pll_prediv_4_to_0 pll_prediv[4:0];

LVDS_channel0_reg20

Address: Operational Base + offset (0x0080)

LVDS register

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RW	0x45	msb_lsb_sel 8'h45: MSB; 8'h44: LSB;

LVDS_config_reg21

Address: Operational Base + offset (0x0084)

LVDS register

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RW	0x00	enable_tx 8'h00: disable tx; 8'h92: enable tx;

LVDS_channel1_reg40

Address: Operational Base + offset (0x0100)

LVDS register

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7	RW	0x1	lvds_mode_en 1'b1: enable lvds mode; 1'b0: disable lvds mode;
6	RW	0x0	ttl_mode_en 1'b1: enable ttl mode; 1'b0: disable ttl mode;
5	RW	0x1	lane_en_ck 1'b1: enable lane_ck; 1'b0: disable lane_ck;
4	RW	0x1	lane_en_4 1'b1: enable lane_4; 1'b0: disable lane_4;
3	RW	0x1	lane_en_3 1'b1: enable lane_3; 1'b0: disable lane_3;
2	RW	0x1	lane_en_2 1'b1: enable lane_2; 1'b0: disable lane_2;
1	RW	0x1	lane_en_1 1'b1: enable lane_1; 1'b0: disable lane_1;
0	RW	0x1	lane_en_0 1'b1: enable lane_0; 1'b0: disable lane_0;

LVDS_channel1_reg41

Address: Operational Base + offset (0x0104)

LVDS register

Bit	Attr	Reset Value	Description
31:6	RO	0x0	reserved
5	RW	0x1	biasen_ck 1'b1: enable lane_ck bias; 1'b0: disable lane_ck bias;

Bit	Attr	Reset Value	Description
4	RW	0x1	biasen_4 1'b1: enable lane_4 bias; 1'b0: disable lane_4 bias;
3	RW	0x1	biasen_3 1'b1: enable lane_3 bias; 1'b0: disable lane_3 bias;
2	RW	0x1	biasen_2 1'b1: enable lane_2 bias; 1'b0: disable lane_2 bias;
1	RW	0x1	biasen_1 1'b1: enable lane_1 bias; 1'b0: disable lane_1 bias;
0	RW	0x1	biasen_0 1'b1: enable lane_0 bias; 1'b0: disable lane_0 bias;

LVDS_channel1_reg42

Address: Operational Base + offset (0x0108)

LVDS register

Bit	Attr	Reset Value	Description
31:7	RO	0x0	reserved
6	RW	0x1	lane_lvds_en_ck 1'b1: enable lane_ck lvds mode; 1'b0: disable lane_ck lvds mode;
5	RW	0x1	lane_lvds_en_4 1'b1: enable lane_4 lvds mode; 1'b0: disable lane_4 lvds mode;
4	RW	0x1	lane_lvds_en_3 1'b1: enable lane_3 lvds mode; 1'b0: disable lane_3 lvds mode;
3	RW	0x1	lane_lvds_en_2 1'b1: enable lane_2 lvds mode; 1'b0: disable lane_2 lvds mode;
2	RW	0x1	lane_lvds_en_1 1'b1: enable lane_1 lvds mode; 1'b0: disable lane_1 lvds mode;
1	RW	0x1	lane_lvds_en_0 1'b1: enable lane_0 lvds mode; 1'b0: disable lane_0 lvds mode;
0	RW	0x0	pll_fbdv_8 pll_fbdv[8];

LVDS_channel1_reg43

Address: Operational Base + offset (0x010c)

LVDS register

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RW	0x46	pll_fbdv_7_to_0 pll_fbdv[7:0];

LVDS_channel1_reg44

Address: Operational Base + offset (0x0110)

LVDS register

Bit	Attr	Reset Value	Description
31:6	RO	0x0	reserved
5	RW	0x0	lane_ttl_en_ck 1'b1: enable lane_ck ttl mode; 1'b0: disable lane_ck ttl mode;
4	RW	0x0	lane_ttl_en_4 1'b1: enable lane_4 ttl mode; 1'b0: disable lane_4 ttl mode;
3	RW	0x0	lane_ttl_en_3 1'b1: enable lane_3 ttl mode; 1'b0: disable lane_3 ttl mode;
2	RW	0x0	lane_ttl_en_2 1'b1: enable lane_2 ttl mode; 1'b0: disable lane_2 ttl mode;
1	RW	0x0	lane_ttl_en_1 1'b1: enable lane_1 ttl mode; 1'b0: disable lane_1 ttl mode;
0	RW	0x0	lane_ttl_en_0 1'b1: enable lane_0 ttl mode; 1'b0: disable lane_0 ttl mode;

LVDS_channel1_reg45

Address: Operational Base + offset (0x0114)

LVDS register

Bit	Attr	Reset Value	Description
31:6	RO	0x0	reserved
5	RW	0x0	lane_ttl_ctrl_ck 1'b1: enable lane_ck ttl data transmission; 1'b0: disable lane_ck ttl data transmission;
4	RW	0x0	lane_ttl_ctrl_4 1'b1: enable lane_4 ttl data transmission; 1'b0: disable lane_4 ttl data transmission;
3	RW	0x0	lane_ttl_ctrl_3 1'b1: enable lane_3 ttl data transmission; 1'b0: disable lane_3 ttl data transmission;

Bit	Attr	Reset Value	Description
2	RW	0x0	lane_ttl_ctr_2 1'b1: enable lane_2 ttl data transmission; 1'b0: disable lane_2 ttl data transmission;
1	RW	0x0	lane_ttl_ctr_1 1'b1: enable lane_1 ttl data transmission; 1'b0: disable lane_1 ttl data transmission;
0	RW	0x0	lane_ttl_ctr_0 1'b1: enable lane_0 ttl data transmission; 1'b0: disable lane_0 ttl data transmission;

LVDS_channel1_reg4d

Address: Operational Base + offset (0x0134)

LVDS register

Bit	Attr	Reset Value	Description
31:5	RO	0x0	reserved
4:0	RW	0xa	pll_prediv_4_to_0 pll_prediv[4:0];

LVDS_channel1_reg60

Address: Operational Base + offset (0x0180)

LVDS register

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RW	0x45	msb_lsb_sel 8'h45: MSB; 8'h44: LSB;

10.5 Interface Description

In RK3288, the LVDS video source comes from vop0 or vop1.

GRF_SOC_CON6[3] == 1'b0, video source from vop0.

GRF_SOC_CON6[3] == 1'b1, video source from vop1.

10.6 Application Notes

Following is the operation flow which describes how the software configures the registers to start lvds data transmission.

- Select the video source by GRF register;
- Select single channel mode or double channel mode by GRF register;
- Select data transfer format by GRF register;
- Enable lvds pll by LVDS registers;
- Enable lvds transfer by LVDS registers;

Chapter 11 eDP Controller

11.1 Overview

This eDP TX IP is compliant with DisplayPort standard 1.2a and eDP 1.3. DisplayPort is an industry standard to accommodate the growing broad adoption of digital display technology within the PC and consumer electronics (CE) industries. It consolidates the internal and external connection methods to reduce device complexity and cost, supports necessary features for key cross industry applications, and provides performance scalability to enable the next generation of displays featuring higher color depths, refresh rates, and display resolutions.

This DisplayPort 1.2 specification defines a scalable digital display interface with optional content protection capability for broad application within PC and CE devices. The interface is designed to support both internal chip-to-chip and external box-to-box digital display connections. Potential internal chip-to-chip applications include usage within a notebook PC for driving a panel from a graphics controller, and usage within a monitor or TV for driving the display component from a display controller. Examples of box-to-box applications for DisplayPort include display connections between PCs and monitors, projectors, and TV displays. DisplayPort is also suitable for display connections between consumer electronics devices such as high definition optical disc players, set top boxes, and TV displays.

It supports following features:

- Compliant with DisplayPort™ Specification, Version 1.2.
- Compliant with eDPTM Specification, Version 1.3.
- HDCP v1.3 amendment for DisplayPort™ Revision 1.0.
- Main link containing 4 physical lanes of 2.7/1.62 Gbps/lane
- TX PHY lanes, control pins and hot-plug pins are shared by the DisplayPort Source
- Bi-directional auxiliary link with up to 1Mbps speed.
- RGB, YCbCr 4:4:4, YCbCr 4:2:2 and 8/10/12 bit per component video format.
- Video and audio slave mode
- Support PSR
- I2S audio interface
- 2,4,6,8-ch PCM - IEC60958 compliant
- S/PDIF audio interface
- Encoded bit stream (Dolby Digital, or DTS) – IEC61937 compliant
- APB slave bus interface
- Hot plug and unplug detection and link status monitor.
- Support VESA DMT and CTV timing standards.
- Fully support EIA/CEA-861Dvideo timing and Info Frame structure.
- Supports reading of the display EDID whenever the display is connected to power, even an AC-trickle power.
- Up to 0.5% down-spreading support at high-speed link.
- Supports DDC/CI and MCCS command transmission when the monitor includes a display controller.
- Flexible output channel mapping and polarity setting.
- PRBS or programmable transmitter pattern for main link quality test.
- Integrated HDCP encryption engine for transmitting protected audio and video content
- SPSRAM interface to read external encrypted HDCP key
- 24 Mhz crystal clock input.
- Built-in video and audio BIST patterns.

- 28nm LP CMOS process with Core voltage 0.9V (min)/ 1.0V (typ)/ 1.08V (max) @ global corner.

11.2 Block Diagram

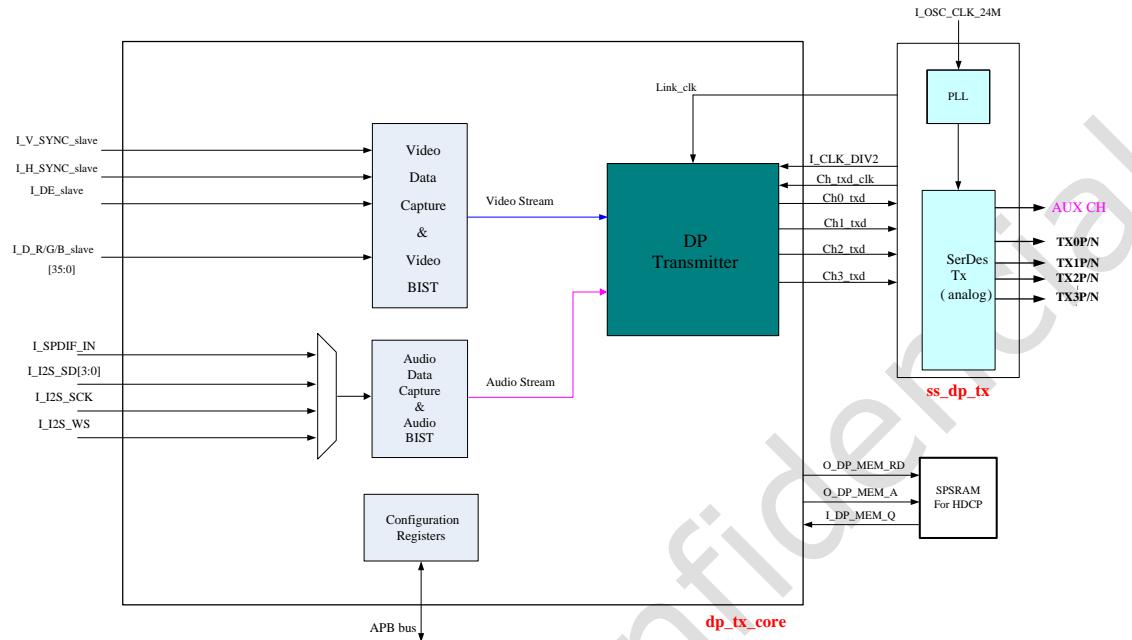


Fig. 11-1 eDP TX controller Block Diagram

Fig.8-1 shows the block diagram of eDP TX controller in top level. The video data and clock are sent directly from the VOP0 or VOP1.

The audio input has 2 interfaces, SPDIF and I2S.

The video data capture & video BIST block is separated as video_capture and display_bist module. The audio data capture & audio BIST block is separated as audio_capture and audio_bist. The block before SerDes is DP_TX main module. Following Table shows the brief function description of each sub-module.

Table 11-1 Brief function description of each module in top level

Module Name in Top Level	Brief Module Function Description
video_capture	Capture block of video data.
display_bist	Generation of arbitrary video format with three types of video data. The output of display_bist module will input to video_capture module directly if display BIST mode is active.
audio_capture	Capture block of audio data.
audio_bist	Generation of the audio BIST pattern.
dp_tx	DisplayPort transmitter block.
apb_slave_top	APB slave Bus interface

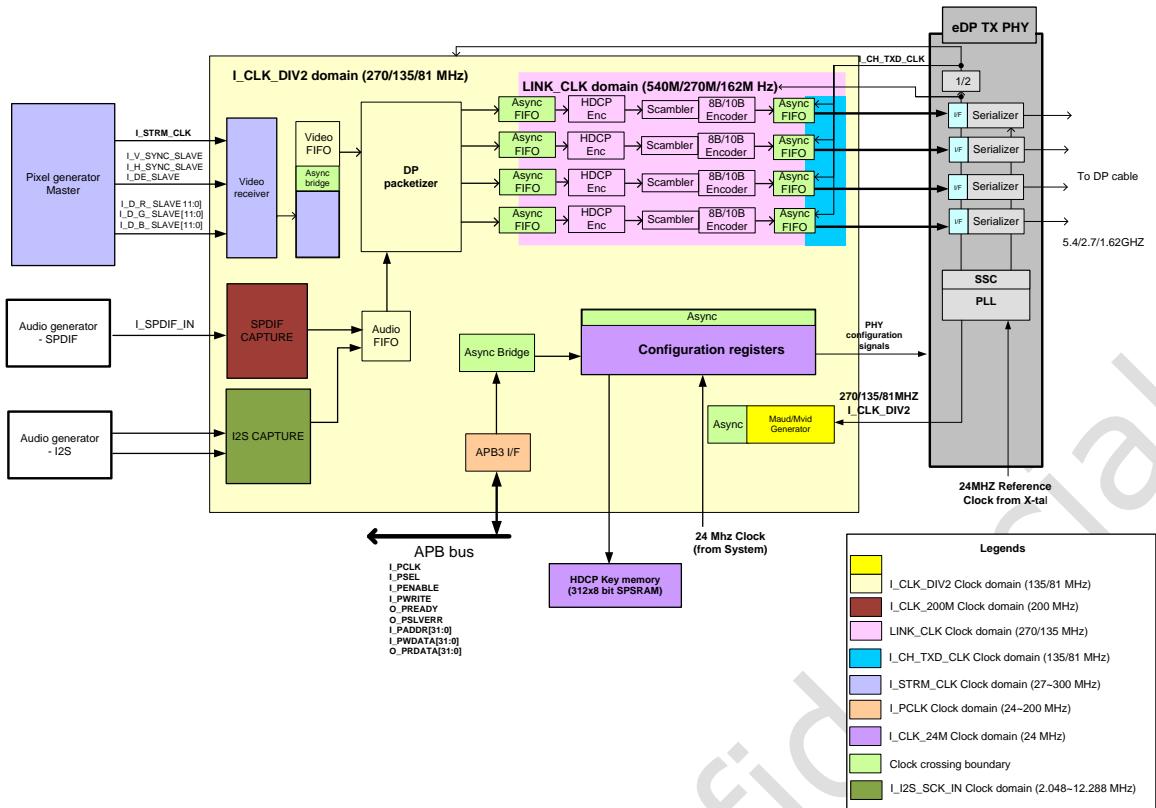


Fig. 11-2 DP_TX clock domain

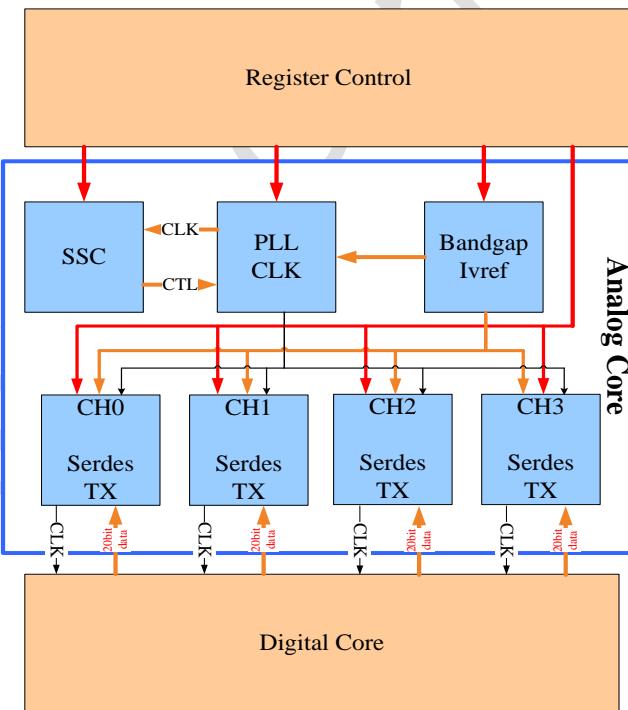


Fig. 11-3 eDP PHY block diagram

11.3 Function Description

11.3.1 eDP in SoC

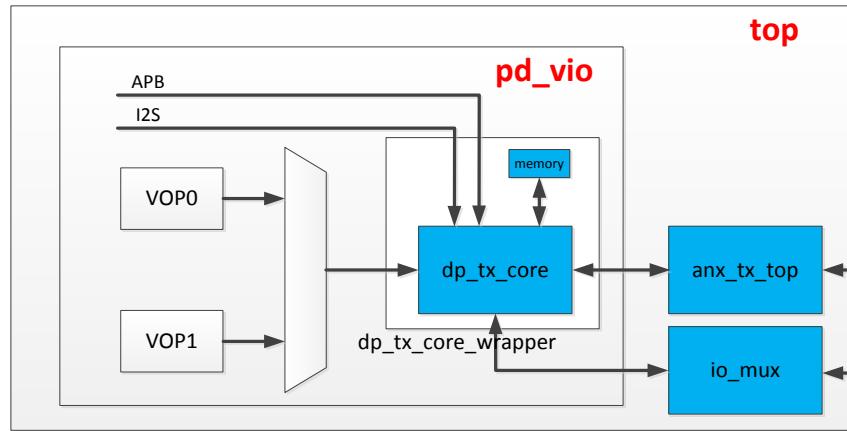


Fig. 11-4 eDP in SoC

There is a 512x8bits memory used to store the HDCP keys in the eDP controller. When **GRF_SOC_CON8[13]** (**grf_edp_mem_ctrl_sel**) = 1'b0, the memory is controlled by APB bus. When **GRF_SOC_CON8[13]** (**grf_edp_mem_ctrl_sel**) = 1'b1, the memory is controlled by eDP controller.

11.3.2 Video Capture

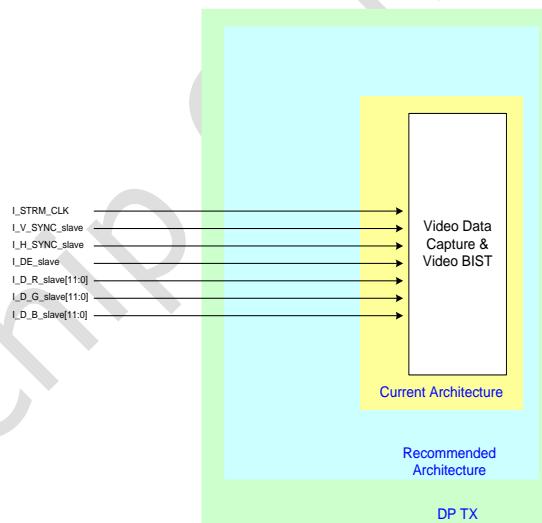


Fig. 11-5 Block diagram of Video Interface

11.3.3 Video slave mode interface

In this slave mode, all timing signals, video data and clock are provided to the DP_TX. All such signals are synchronous to the input clock (I_STRM_CLK) for slave mode. DP_TX receives such signals and stores the video signals into the buffer. Afterward, the video data packetizer which operates on LS_CLK clock (135/81MHz) reads from the buffer asynchronously.

The signals for slave mode are as follows.

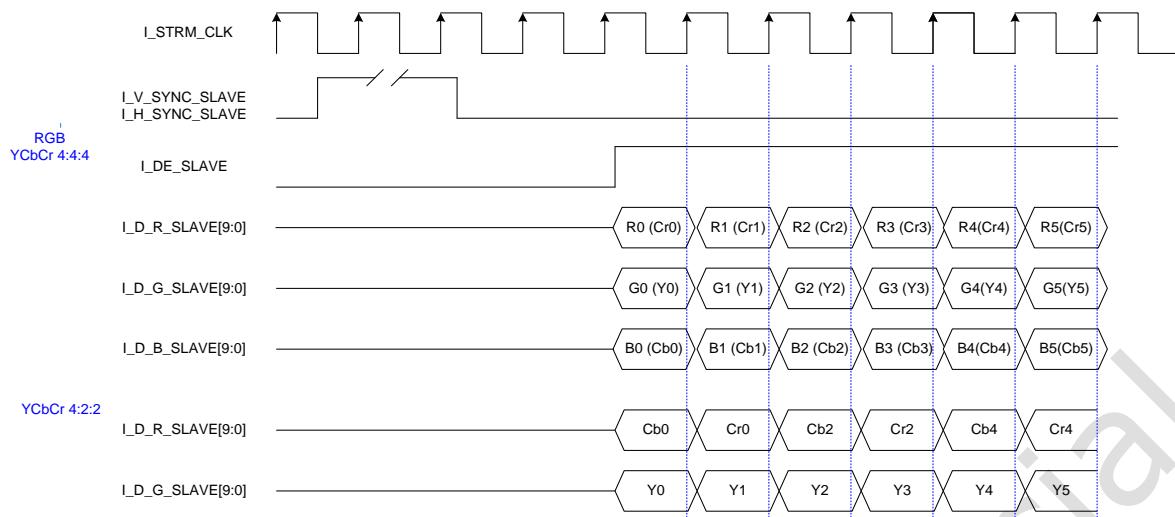


Fig. 11-6 Video interface signals for slave mode – YCbCr 4:4:4 and YCbCr 4:2:2 pixel bit format

Video pixel data is provided with the high state of **I_DE_slave** signal. The timing signals, **I_V_SYNC_slave**, **I_H_SYNC_slave** can be either active high or low by register setting.

11.3.4 Pixel Bit format

DP_TX supports 8/10/12 bit pixel input and supports RGB, YCbCr 4:4:4, and YCbCr 4:2:2. Such various pixel bit formats are shown in the following figures.

For the 10-bpc mode, the data should be left justified as shown in the following figure. Two unused bits should be stuffed as zeros.

I_PIX_DATA_R (I_D_R_SLAVE)	[11]	[10]	[9]	[8]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
RGB mode	R[9]	R[8]	R[7]	R[6]	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	1'b0	1'b0
YCbCr mode	Cr[9]	Cr[8]	Cr[7]	Cr[6]	Cr[5]	Cr[4]	Cr[3]	Cr[2]	Cr[1]	Cr[0]	1'b0	1'b0

I_PIX_DATA_G (I_D_G_SLAVE)	[11]	[10]	[9]	[8]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
RGB mode	G[9]	G[8]	G[7]	G[6]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	1'b0	1'b0
YCbCr mode	Y[9]	Y[8]	Y[7]	Y[6]	Y[5]	Y[4]	Y[3]	Y[2]	Y[1]	Y[0]	1'b0	1'b0

I_PIX_DATA_B (I_D_B_SLAVE)	[11]	[10]	[9]	[8]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
RGB mode	B[9]	B[8]	B[7]	B[6]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]	1'b0	1'b0
YCbCr mode	Cb[9]	Cb[8]	Cb[7]	Cb[6]	Cb[5]	Cb[4]	Cb[3]	Cb[2]	Cb[1]	Cb[0]	1'b0	1'b0

Fig. 11-7 10-bpc mode pixel bit format

For the 8-bpc mode, the data should be left justified as shown in the following figure and four unused bits should be stuffed as zeros

I_PIX_DATA_R (I_D_R_SLAVE)	[11]	[10]	[9]	[8]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
RGB mode	R[7]	R[6]	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	1'b0	1'b0	1'b0	1'b0
YCbCr mode	Cr[7]	Cr[6]	Cr[5]	Cr[4]	Cr[3]	Cr[2]	Cr[1]	Cr[0]	1'b0	1'b0	1'b0	1'b0
I_PIX_DATA_G (I_D_G_SLAVE)	[11]	[10]	[9]	[8]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
RGB mode	G[7]	G[6]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	1'b0	1'b0	1'b0	1'b0
YCbCr mode	Y[7]	Y[6]	Y[5]	Y[4]	Y[3]	Y[2]	Y[1]	Y[0]	1'b0	1'b0	1'b0	1'b0
I_PIX_DATA_B (I_D_B_SLAVE)	[11]	[10]	[9]	[8]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
RGB mode	B[7]	B[6]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]	1'b0	1'b0	1'b0	1'b0
YCbCr mode	Cb[7]	Cb[6]	Cb[5]	Cb[4]	Cb[3]	Cb[2]	Cb[1]	Cb[0]	1'b0	1'b0	1'b0	1'b0

Fig. 11-8 8-bpc pixel bit format

11.3.5 Video FIFO

The video data FIFO is used to buffer the input video stream in slave mode and send them out in the LS_CLK domain.

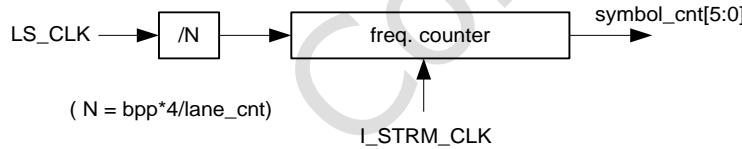


Fig. 11-9 Active symbol count implementation

The video FIFO is unsymmetrical FIFO, the input bus width can be variable and the output bus width is fixed. The video FIFO is divided into two parts. The first part unifies the variable input data bus width to 36 bits bus width, and the second part transfers data crossing clock domain and change bus width from 36 bits to 8 bits. The first part of video FIFO for one channel has $2 \cdot 36$ bit buffer, and which atom is 2 bit. The video pixel data is written to buffer and when the pointer crosses or matches the middle point of buffer, 36 bits data will be read out from buffer and be written to buffer of second part. The second part of video FIFO is a standard asynchronous unsymmetrical FIFO.

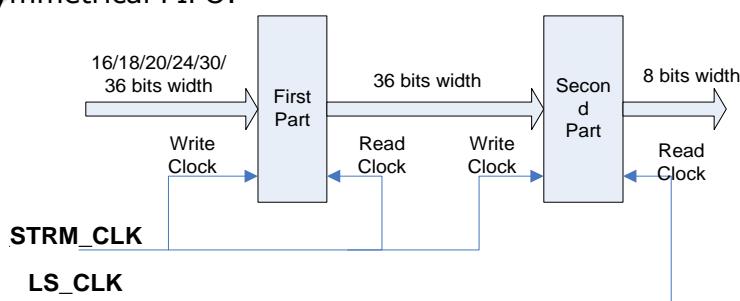


Fig. 11-10 The structure of video FIFO for video in slave mode

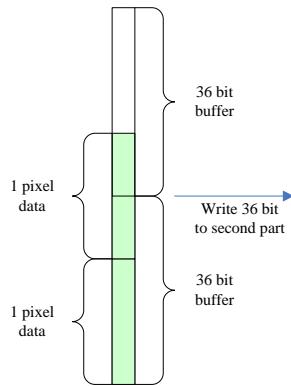


Fig. 11-11 First part structure of video FIFO

The buffer size of first part is $4 * 2 * 36$ bits, and that of second part is $4 * 72 * 16$ bits. The buffer for each channel is separated but uses same control pointer.

Whenever the video data FIFO fills up to pre-defined threshold, “read_en” signal asserts to “1” and it will assert to “0” till the end of a line, LS_CLK samples “read_en” and once it finds the rising edge of “read_en”, then it starts a TU (Transfer Unit) transfer and begins to read the symbols out of the FIFO. After active symbol of a TU is read out, which count is calculated by Active Symbol Generation module, reading of video FIFO is paused, until a whole TU (64 symbol) is completed. After the end of a line is written to video FIFO, “last pixel” signal will be asserted to “1”. When “last pixel” signal is “1” and all data in video FIFO is read out, a whole line transfer is completed. So if the video data of a line cannot reach the boundary of 16 bits, more dummy data should be written to video FIFO to fill up the last 8 bits.

The actual design read 2 symbols at one LS_CLK cycle. This is shown in following figure.

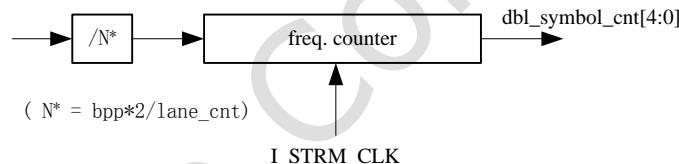


Fig. 11-12 Double byte active symbol count implementation

Here $N^* = N/2$. The symbols in the TU will be $2 * dbl_symbol_cnt$ and it's an even number. The dbl_symbol_cnt output would be 36, 36, 36, 36, 34, 36, 36, 36, 36, 34, 36, 36 ... et al.

11.3.6 Audio data interface

For audio, there are two interface; SDPIF slave and I2S slave. In SDPIF slave mode, the audio stream is sent from the SDPIF input. In I2S slave mode, the audio stream is sent from the I2S SDPIF input.

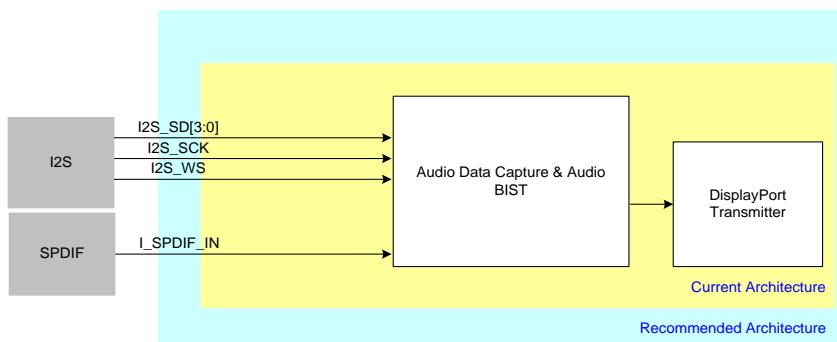


Fig. 11-13 Audio data interface block diagram

11.3.7 Audio Capture and Audio BIST

The audio capture block takes the audio stream either from SPDIF or from the I2S bus. The audio stream can carry up to 8-channel uncompressed PCM data (IEC 60958) or a compressed bit stream for multi-channel (IEC 61937) formats. The audio data capture logic forms the audio data into packets in accordance with the DisplayPort 1.2 specification. The audio capture block supports audio sampling rates from 32 to 192 kHz.

The appropriate registers must be configured to describe the format of audio being input into the DP TX. This information is passed over main link in the CEA-861D Audio Info packets. The audio BIST function in this block generates sin-wave with different amplitude and frequency. It is used to conveniently test the audio output of the DisplayPort receiver. The sin-wave amplitude and frequency are set by the configuration registers.

11.3.8 Audio FIFO

In order to send audio samples during video blanking period, the audio stream during each active video line period should first be stored. The audio samples stored for each line is calculated as follows:

$$\text{audio_samples/line} = \text{Fs} / (\text{Field_refresh_rate} * \text{lines_per_field})$$

e.g., for 2880 x 240p @60Hz video format, Fs = 192Khz,

Field_refresh_rate = Hz, lines_per_field = 262, then

$$\text{audio_samples/line} = 192000 / (60 * 262) \sim 13 \text{ samples}$$

Here, the audio_samples is composed by multiple audio channel data. For stereo audio, there are 2 audio channel data in each audio sample; while for 8 channels data, there are 8 channel data in each audio sample.

For 24-bits audio format, each channel data have 27-bits (24-bits PCM, 1-bit User data, 1-bit Channel Status and 1-bit Valid Bit).

eDP TX IP has 4 FIFO block for audio. Each FIFO width is 54-bits to fit 2 channel data, and depth is 16. When audio stream channel count is more than 2, 4 FIFO block will be used parallel to store audio channel data and dummy data. So for 3 ~ 8 channel audio case, the total depth is still 16.

But if audio stream is mono or stereo, 4 FIFO block are used serially. Then the total depth is 64.

11.3.9 Video and Audio M/N Value Generation

The transmitter needs to send video timing stamp to the receiver at the blanking period. The receiver recovers the video stream clock based on the M_VID and N_VID values. The relation between STRM_CLK and LS_CLK is:

$$M_{VID} = F_{STRM_CLK} * N_{VID} / (2 * F_{LS_CLK})$$

F_{LS_CLK} is 81M/135M.

Both M_VID and N_VID must be 24-bit values.

When the DP_TX and the stream source share the same reference clock, the N_VID and M_VID stay constant. This way of generating LS_CLK and STRM_CLK is called Synchronous Clock mode.

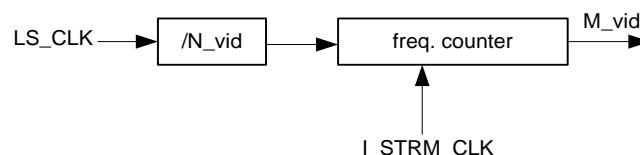


Fig. 11-14 M_VID Generation

If the STRM_CLK and LS_CLK are asynchronous with each other, the value of M_VID changes over time. This way of generating LS_CLK and I_STRM_CLK is called Asynchronous Clock mode. The value M_VID must change while the value N_VID stays constant. The value of N_VID in this Asynchronous Clock mode must be set to 2^{15} or 32,768. The maximum value of M_VID is 0xFFFF in Asynchronous Clock mode.

For DP SOC slave mode video stream, we have to use only asynchronous clock mode as long as the external video stream generator does not use the DP PLL output as a reference clock.

When in Asynchronous Clock mode, the DisplayPort transmitter must measure M using a counter running at the LS_CLK frequency as shown in Fig. 11-14 M_VID Generation shows some examples of the M_AUD for various audio sampling frequencies when audio clock and LS_CLK are synchronous.

Either when down-spreading of the link is enabled or audio clock is asynchronous to the link symbol clock, the value of M_AUD will change over time. As is the case with M_AUD measurement, the N_AUD must be set to 215 (32,768) for Maud measurement in asynchronous clock mode. The generation of M_AUD in these cases is same as generation of M_VID. The maximum value of M_AUD is 0xFFFF in Asynchronous Clock mode.

Table 11-2 Examples of M_AUD and N_AUD

$F_{LS_CLK} = 135MHz (2.7G bps)$	$F_{LS_CLK} = 81MHz (1.62G bps)$		
Regenerated clock = 512x 48kHz (Used when sample frequency = 48kHz)			
M_AUD	1024	M_AUD	1024
N_AUD	5625	N_AUD	3375
Regenerated clock = 512x 44.1kHz (Used when sample frequency = 44.1kHz)			
M_AUD	1486	M_AUD	1486
N_AUD	9375	N_AUD	5625
Regenerated clock = 512x 32kHz (Used when sample frequency = 32kHz)			
M_AUD	2048	M_AUD	2048
N_AUD	16875	N_AUD	10125

M_AUD[7:0] is transferred every horizontal line right after M_VID[7:0]. M_AUD[23:0] and N_AUD[23:0] are transferred as audio timestamp packet in a secondary packet, which is transferred every vertical blank time. Likewise, M_VID[7:0] is transferred every horizontal line right after VB-ID symbol. M_VID[23:0] and N_VID[23:0] are transferred, embedded in main stream attribute data packet, which is transferred every vertical blank time.

Note that N_AUD and N_VID are limited to the maximum 16 bit value, that is, 0xffff. N_VID is limited to the maximum 16 bit value, 0xffff, because too large N_VID is not a good idea due to the granularity of the adjustment of M/N value.

Hardware calculated M values may fluctuate frame by frame due to jitter of sampling between two different clock domains. To avoid and smooth out such variation, DP has filters for Video M value and Audio M value. Both of them use the same filtering algorithm. The M value is updated periodically (every N link clock cycles).

The filter is operated as following algorithm;

Let

i : frame index

M_raw(i) : M_value calculated by counter at i'th frame as shown in Fig. 11-14.

M_filtered(i) : Filtered out M value at i'th frame.

SumOfR(i) : Accumulated difference between M_raw(i) and M_filtered(i-1) then,

(1) SumOfR(0) = 0 & M_filtered(0) = 0; // initialization

```

(2) Get M_raw(i) for i'th frame by counter
(3) SumOfR(i) = SumOfR(i-1) + M_raw(i) - M_filtered(i-1)
Calculate M_filtered(i) and adjust of SumOfR(i)
if ( (SumOfR(i) > M_VID_GEN_FILTER_TH) or
(M_raw(i) > M_filtered(i-1) + M_VID_GEN_FILTER_TH) )
{
SumOfR(i) = SumOfR(i) - M_VID_GEN_FILTER_TH;
M_filtered(i) = M_filtered(i-1) + M_VID_GEN_FILTER_TH;
}
else if ( (SumOfR(i) < (-1 * M_VID_GEN_FILTER_TH)) or
(M_raw(i) < M_filtered(i-1) - M_VID_GEN_FILTER_TH) )
{
M_filtered(i) = M_filtered(i-1) - M_VID_GEN_FILTER_TH;
SumOfR(i) = SumOfR(i) + M_VID_GEN_FILTER_TH;
}
else M_filtered(i) = M_raw(i);

```

What hardware does for M value calculation:

Basically, as mentioned in DP specification, M/N value ratio must be the same to stream clock (FSTRM_CLK) / DP link symbol clock (FLS_CLK_O), where FLS_CLK_O is fixed as 270 MHz and 162MHz for high link rate and low link rate, respectively. However, actual hardware of DP Soc does not need to be implemented to run at such a high link symbol clock. In the case of this DP Tx Soc, DP link symbol clock (FLS_CLK) is 135 MHz for high link rate and 81 MHz for low link rate. So, we describe here what hardware does to calculate M value, which satisfies DP specification, with its own link clock, not 270Mhz. Note that here, even the stream clock (FSTRM_CLK) can be replaced to another available clock.

1. Audio M value (M_AUD) and N value (N_AUD)

Audio M value (M_AUD) and N value (N_AUD) are used for audio stream clock recovery by DP RX. DP SOC supports one ways to fetch audio data: slave mode.

Slave mode M_AUD value is counted by SPDIF biphase encoding clock (FS_BIPHASE), which is (32* FS_AUD_SLAVE * AudioChNum * 2). Here, 2 are for biphase encoding and 32 is for each sub frame. FS_AUD_SLAVE stands for slave mode audio sampling frequency. AudioChNum denotes the number of audio channels, so it is 2 for two channel SPDIF audio source.

In case two channel audio source is used, FS_BIPHASE are

$$\text{FS_BIPHASE} = 128 * \text{FS_AUD_SLAVE}$$

The following equation shows the relation of SPDIF biphase encoding clock and DP link symbol clock to meet DP specification.

$$\begin{aligned} M_{AUD} &= 512 * \text{FS_AUD_SLAVE} * N_{AUD} / \text{FLS_CLK}_O \\ &= 512 * \text{FS_AUD_SLAVE} * N_{AUD} / (2 * \text{FLS_CLK}) \\ &= 512 * (\text{FS_BIPHASE} / 128) * N_{AUD} / (2 * \text{FLS_CLK}) \\ &= 2 * \text{FS_BIPHASE} * N_{AUD} / \text{FLS_CLK}. \end{aligned}$$

implying that

$$M_{AUD} / (2 * N_{AUD}) = \text{FS_BIPHASE} / \text{FLS_CLK}.$$

This formula clearly explains what hardware does for M_AUD calculation at slave mode. It says that if a counter (M_AUD_COUNTER) increased by FS_BIPHASE is counted until the other counter (N_AUD_COUNTER) running on FLS_CLK reaches 2 * N_AUD, the value in M_AUD_COUNTER becomes a right M_AUD value for N_AUD at 270 MHz link symbol clock.

Therefore, as a M_AUD value, DP Tx tries to transfer M_AUD_COUNTER counted by FS_BIPHASE every 2 * N_AUD cycles counted by FLS_CLK. N_AUD are a fixed value. Usually, N_AUD is set to 215, especially for asynchronous mode. This means M_AUD is updated every 485 us (= 2 * 215 cycles at FLS_CLK) when FLS_CLK is 135 MHz

2. Video M value (M_VID) and N value (N_VID)

Video M value (M_VID) and N value (N_VID) are used for video stream clock recovery in DP RX. Video M/N value shows the ratio of video stream sampling frequency over DP link symbol clock. Video stream sampling frequency, that is, video stream clock shall be $V_{TOTAL} * H_{TOTAL} * \text{Refresh Rate}$, where H_TOTAL stands for the number of pixels in each line, V_TOTAL for the number of lines in each frame and Refresh Rate for the refresh rate of video frame. DP SOC supports one way to fetch video data: slave mode.

Let us denote slave mode video stream clock as FS_VID_SLAVE. DP link symbol clock (FLS_CLK) in this DP Tx is 135MHz for high link rate and 81 MHz for low link rate, while DP link symbol clock (LS_CLK_O) specified by DP Specification is 270 MHz and 162MHz, respectively.

The following equation shows how to calculate M_VID with DP link symbol clock, FLS_CLK, to meet DP specification.

$$\begin{aligned} M_{VID} &= FS_{VID_SLAVE} * N_{VID} / FLS_{CLK_O} \\ &= FS_{VID_SLAVE} * N_{VID} / (2 * FLS_{CLK}), \end{aligned}$$

leading to

$$M_{VID} / (N_{VID} / 2) = FS_{VID_SLAVE} / FLS_{CLK}.$$

By the formula above, DP Tx tries to transfer M_VID counted by FS_VID_SLAVE every $N_{VID} / 2$ cycles, which is counted by FLS_CLK.

That is, M_VID is counted by FS_VID_SLAVE until a counter running on FLS_CLK, N_VID_COUNTER, reaches $N_{VID} / 2$. When a counter running on FLS_CLK reaches $N_{VID} / 2$, M_VID is stored for the transmission to DP RX and restarts to count. Usually, N_VID is set to 215, especially for asynchronous mode. This means M_VID value is updated every 121 us (=215 / 2 cycles at FLS_CLK) when FLS_CLK is 135 MHz

11.3.10 DisplayPort Main Link

The DisplayPort transmitter includes 4 physical links: the main link and the auxiliary link. The main link is composed of 4 lanes link, where each is 2.7Gbps link or 1.62 Gbps used to transfer the video stream, audio stream, Info Frame packet as well as the related main link attributes.

11.3.11 Data Packing

The DP_TX gets the video data from the Video FIFO module. Then the video data will be packed into TU (Transfer Unit). The Info Frame is passed directly through the APB interface. Some main link attributes data come from APB interface, but the information of input video timing of main link attribute come from Video Capture module.

Video data is packed to byte ignoring the pixel boundary, such as following table.

Table 11-3 Video Data Mapping to Main Link
24-bpp RGB Mapping to 4-lane Main Link

Lane 0	Lane 1	Lane 2	Lane 3
R0-7:0	R1-7:0	R2-7:0	R3-7:0
G0-7:0	G1-7:0	G2-7:0	G3-7:0
B0-7:0	B1-7:0	B2-7:0	B3-7:0
R4-7:0	R5-7:0	R6-7:0	R7-7:0
G4-7:0	G5-7:0	G6-7:0	G7-7:0
B4-7:0	B5-7:0	B6-7:0	B7-7:0
R8-7:0	R9-7:0	R10-7:0	R11-7:0
G8-7:0	G9-7:0	G10-7:0	G11-7:0
B8-7:0	B9-7:0	B10-7:0	B11-7:0

Note: for YCbCr444, replace R with Cr, G with Y, and B with Cb

24-bpp RGB Mapping to 2-lane Main Link

Lane 0	Lane 1
R0-7:0	R1-7:0
G0-7:0	G1-7:0
B0-7:0	B1-7:0
R2-7:0	R3-7:0
G2-7:0	G3-7:0
B2-7:0	B3-7:0
R4-7:0	R5-7:0
G4-7:0	G5-7:0
B4-7:0	B5-7:0
R6-7:0	R7-7:0
G6-7:0	G7-7:0
B6-7:0	B7-7:0

Note: for YCbCr444, replace R with Cr, G with Y, and B with Cb

24-bpp RGB Mapping to 1-lane Main Link

Lane 0
R0-7:0
G0-7:0
B0-7:0
R1-7:0
G1-7:0
B1-7:0
R2-7:0
G2-7:0
B2-7:0
R3-7:0
G3-7:0
B3-7:0

Note: for YCbCr444, replace R with Cr, G with Y, and B with Cb

30-bpp RGB Mapping to 4-lane Main Link

Lane 0	Lane 1	Lane 2	Lane 3
R0-9:2	R1-9:2	R2-9:2	R3-9:2
R0-1:0 G0-9:4	R1-1:0 G1-9:4	R2-1:0 G2-9:4	R3-1:0 G3-9:4
G0-3:0 B0-9:6	G1-3:0 B1-9:6	G2-3:0 B2-9:6	G3-3:0 B3-9:6
B0-5:0 R4-9:8	B1-5:0 R5-9:8	B2-5:0 R6-9:8	B3-5:0 R7-9:8
R4-7:0	R5-7:0	R6-7:0	R7-7:0
G4-9:2	G5-9:2	G6-9:2	G7-9:2
G4-1:0 B4-9:4	G5-1:0 B5-9:4	R2-1:0 B6-9:4	R3-1:0 B7-9:4
B4-3:0 R8-9:6	B5-3:0 R9-9:6	B6-3:0 R10-9:6	B7-3:0 R11-9:6
R8-5:0 G8-9:8	R9-5:0 G9-9:8	R10-5:0 G10-9:8	R11-5:0 G11-9:8
G8-7:0	G9-7:0	G10-7:0	G11-7:0
B8-9:2	B9-9:2	B10-9:2	B11-9:2
B8-1:0 R12-9:4	B9-1:0 R13-9:4	B10-1:0 R14-9:4	B11-1:0 R15-9:4
R12-3:0 G12-9:6	R13-3:0 G13-9:6	R14-3:0 G14-9:6	G15-3:0 B15-9:6

G12-5:0 B12-9:8	G13-5:0 B13-9:8	G14-5:0 B14-9:8	B15-5:0 R15-9:8
B12-7:0	B13-7:0	B14-7:0	R15-7:0

Note: for YCbCr444, replace R with Cr, G with Y, and B with Cb

30-bpp RGB Mapping to 2-lane Main Link

Lane 0	Lane 1
R0-9:2	R1-9:2
R0-1:0 G0-9:4	R1-1:0 G1-9:4
G0-3:0 B0-9:6	G1-3:0 B1-9:6
B0-5:0 R2-9:8	B1-5:0 R3-9:8
R2-7:0	R3-7:0
G2-9:2	G3-9:2
G2-1:0 B2-9:4	G3-1:0 B3-9:4
B2-3:0 R3-9:6	B3-3:0 R4-9:6
R3-5:0 G4-9:8	R4-5:0 G5-9:8
G4-7:0	G5-7:0
B4-9:2	B5-9:2
B4-1:0 R6-9:4	B5-1:0 R7-9:4
R6-3:0 G6-9:6	R7-3:0 G7-9:6
G6-5:0 B6-9:8	G7-5:0 B7-9:8
B6-7:0	B7-7:0

Note: for YCbCr444, replace R with Cr, G with Y, and B with Cb

30-bpp RGB Mapping to 1-lane Main Link

Lane 0
R0-9:2
R0-1:0 G0-9:4
G0-3:0 B0-9:6
B0-5:0 R1-9:8
R1-7:0
G1-9:2
G1-1:0 B1-9:4
B1-3:0 R2-9:6
R2-5:0 G2-9:8
G2-7:0
B2-9:2
B2-1:0 R3-9:4
R3-3:0 G3-9:6
G3-5:0 B3-9:8
B3-7:0

Note: for YCbCr444, replace R with Cr, G with Y, and B with Cb

36-bpp RGB Mapping to 4-lane Main Link

Lane 0	Lane 1	Lane 2	Lane 3
R0-11:4	R1-11:4	R2-11:4	R3-11:4
R0-3:0 G0-11:8	R1-3:0 G1-11:8	R2-3:0 G2-11:8	R3-3:0 G3-11:8
G0-7:0	G1-7:0	G2-7:0	G3-7:0

B0-11:4	B1-11:4	B2-11:4	B3-11:4
B0-3:0 R4-11:8	B1-3:0 R5-11:8	B2-3:0 R6-11:8	B3-3:0 R7-11:8
R4-7:0	R5-7:0	R6-7:0	R7-7:0
G4-11:4	G5-11:4	G6-11:4	G7-11:4
G4-3:0 B4-11:8	G5-3:0 B5-11:8	G6-3:0 B6-11:8	G7-3:0 B7-11:8
B4-7:0	B5-7:0	B6-7:0	B7-7:0

36-bpp RGB Mapping to 2-lane Main Link

Lane 0	Lane 1
R0-11:4	R1-11:4
R0-3:0 G0-11:8	R1-3:0 G1-11:8
G0-7:0	G1-7:0
B0-11:4	B1-11:4
B0-3:0 R2-11:8	B1-3:0 R3-11:8
R2-7:0	R3-7:0
G2-11:4	G3-11:4
G2-3:0 B2-11:8	G3-3:0 B3-11:8
B2-7:0	B3-7:0

36-bpp RGB Mapping to 2-lane Main Link

Lane 0
R0-11:4
R0-3:0 G0-11:8
G0-7:0
B0-11:4
B0-3:0 R1-11:8
R1-7:0
G1-11:4
G1-3:0 B1-11:8
B1-7:0

Note: for YCbCr444, replace R with Cr, G with Y, and B with Cb

16-bpp YCbCr Mapping to 4-lane Main Link

Lane 0	Lane 1	Lane 2	Lane 3
Cb0-7:0	Cr0-7:0	Cb2-7:0	Cr0-7:0
Y0-7:0	Y1-7:0	Y2-7:0	Y3-7:0
Cb4-7:0	Cr4-7:0	Cb6-7:0	Cr6-7:0
Y4-7:0	Y5-7:0	Y6-7:0	Y7-7:0
Cb8-7:0	Cr8-7:0	Cb10-7:0	Cr10-7:0
Y8-7:0	Y9-7:0	Y10-7:0	Y11-7:0

16-bpp YCbCr Mapping to 2-lane Main Link

Lane 0	Lane 1
Cb0-7:0	Cr0-7:0
Y0-7:0	Y1-7:0
Cb2-7:0	Cr0-7:0

Y2-7:0	Y3-7:0
Cb4-7:0	Cr4-7:0
Y4-7:0	Y5-7:0
Cb6-7:0	Cr6-7:0
Y6-7:0	Y7-7:0
Cb8-7:0	Cr8-7:0
Y8-7:0	Y9-7:0
Cb10-7:0	Cr10-7:0
Y10-7:0	Y11-7:0

16-bpp YCbCr Mapping to 1-lane Main Link

Lane 0
Cb0-7:0
Y0-7:0
Cr0-7:0
Y1-7:0
Cb2-7:0
Y2-7:0
Cr0-7:0
Y3-7:0
Cb4-7:0
Y4-7:0
Cr4-7:0
Y5-7:0

20-bpp YcbCr422 mapping to 4-lane Main Link

Lane 0	Lane 1	Lane 2	Lane 3
Cb0-9:2	Cr0-9:2	Cb2-9:2	Cr2-9:2
Cb0-1:0 Y0-9:4	Cr0-1:0 Y1-9:4	Cb2-1:0 Y2-9:4	Cr2-1:0 Y3-9:4
Y0-3:0 Cb4-9:6	Y1-3:0 Cr4-9:6	Y2-3:0 Cb6-9:6	Y3-3:0 Cr6-9:6
Cb4-5:0 Y4-9:8	Cr4-5:0 Y5-9:8	Cb6-5:0 Y6-9:8	Cr6-5:0 Y7-9:8
Y4-7:0	Y5-7:0	Y6-7:0	Y7-7:0
Cb8-9:2	Cr8-9:2	Cb10-9:2	Cr10-9:2
Cb8-1:0 Y8-9:4	Cr8-1:0 Y9-9:4	Cb10-1:0 Y10-9:4	Cr10-1:0 Y11-9:4
Y8-3:0 Cb12-9:6	Y9-3:0 Cr12-9:6	Y10-3:0 Cb14-9:6	Y11-3:0 Cr14-9:6
Cb12-5:0 Y12-9:8	Cr12-5:0 Y13-9:8	Cb14-5:0 Y14-9:8	Cr14-5:0 Y15-9:8
Y12-7:0	Y13-7:0	Y14-7:0	Y15-7:0

20-bpp YCbCr422 Mapping to 2-lane Main Link

Lane 0	Lane 1
Cb0-9:2	Cr0-9:2
Cb0-1:0 Y0-9:4	Cr0-1:0 Y1-9:4
Y0-3:0 Cb2-9:6	Y1-3:0 Cr2-9:6
Cb2-5:0 Y2-9:8	Cr2-5:0 Y3-9:8
Y2-7:0	Y3-7:0
Cb4-9:2	Cr4-9:2

Lane 0	Lane 1
Cb4-1:0 Y4-9:4	Cr4-1:0 Y5-9:4
Y4-3:0 Cb6-9:6	Y5-3:0 Cr6-9:6
Cb6-5:0 Y6-9:8	Cr6-5:0 Y7-9:8
Y6-7:0	Y7-7:0

20-bpp YcbCr422 Mapping to 1-lane Main Link

Lane 0
Cb0-9:2
Cb0-1:0 Y0-9:4
Y0-3:0 Cr0-9:6
Cr0-5:0 Y1-9:8
Y1-7:0
Cb2-9:2
Cb2-1:0 Y2-9:4
Y2-3:0 Cr2-9:6
Cr2-5:0 Y3-9:8
Y3-7:0

24-bpp YcbCr422 mapping to 4-lane Main Link

Lane 0	Lane 1	Lane 2	Lane 3
Cb0-11:4	Cr0-11:4	Cb2-11:4	Cr2-11:4
Cb0-3:0 Y0-11:8	Cr0-3:0 Y1-11:8	Cb2-3:0 Y2-11:8	Cr2-3:0 Y3-11:8
Y0-7:0	Y1-7:0	Y2-7:0	Y3-7:0
Cb4-11:4	Cr4-11:4	Cb6-11:4	Cr6-11:4
Cb4-3:0 Y4-11:8	Cr4-3:0 Y4-11:8	Cb6-3:0 Y6-11:8	Cr6-3:0 Y6-11:8
Y4-7:0	Y5-7:0	Y6-7:0	Y7-7:0

24-bpp YcbCr422 mapping to 2-lane Main Link

Lane 0	Lane 1
Cb0-11:4	Cr0-11:4
Cb0-3:0 Y0-11:8	Cr0-3:0 Y1-11:8
Y0-7:0	Y1-7:0
Cb2-11:4	Cr2-11:4
Cb2-3:0 Y2-11:8	Cr2-3:0 Y3-11:8
Y2-7:0	Y3-7:0

24-bpp YcbCr422 mapping to 1-lane Main Link

Lane 0
Cb0-11:4
Cb0-3:0 Y0-11:8
Y0-7:0
Cr0-11:4
Cr0-3:0 Y1-11:8
Y1-7:0

Table 11-4 Control Symbols for Framing

Name	Symbol	Special Character	
		Normal Mode	Enhanced Mode
Blank Start	BS	K28.5	K28.5 + K28.3 + K28.3 + K28.5
Scrambler Reset	SR	K28.0	K28.0 + K28.3 + K28.3 + K28.0
Content Protection BS	CPBS	K28.1	K28.5 + K28.1+ K28.1 + K28.5
Content Protection SR	CPSR	K28.3	K28.0 + K28.1+ K28.1 + K28.0
Blank End	BE	K27.7	K27.7
Secondary-data Start	SS	K28.2	K28.2
Secondary-data End	SE	K29.7	K29.7
Fill Start	FS	K30.7	K30.7
Fill End	FE	K23.7	K23.7

To avoid the oversubscription of the link bandwidth, the packed data rate must be equal to or lower than the link symbol rate. When the packed data rate is lower than the link symbol rate, the link layer must perform symbol stuffing. During the active video period, stuffing symbols must be framed with control symbols FS & FE within Transfer Unit (TU) as shown in Fig. 8-12.

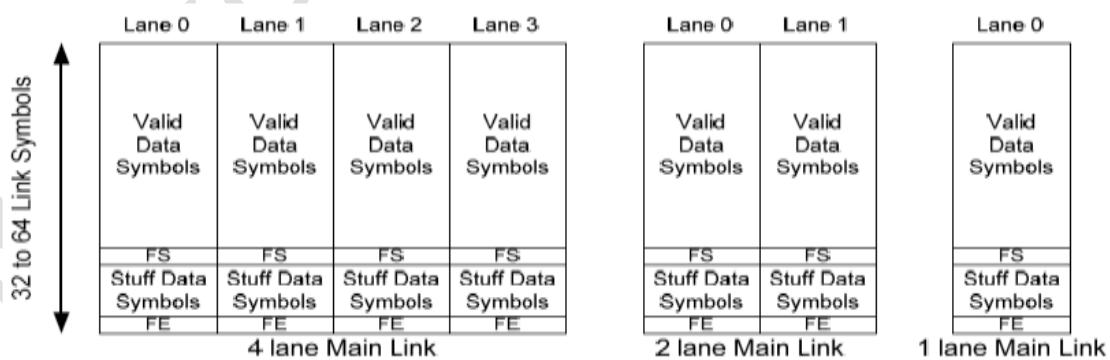


Fig. 11-15 Transfer unit

The transfer unit (TU) size must be in the range of 32 to 64 link symbols per lane. The DisplayPort Source Device must fix the TU size for a given video timing format. The first pixel data of the horizontal active display line, immediately after BE, must be placed as the first valid data symbols of the first TU of a line. The partial pixel data of Pixel 0 must always be placed on Lane 0.

The dummy stuffing data symbols during the video blanking periods (both vertical and horizontal) may be substituted either with main stream attributes data or a secondary data packet. Both must be framed with SS and SE control symbols as shown in following figure.

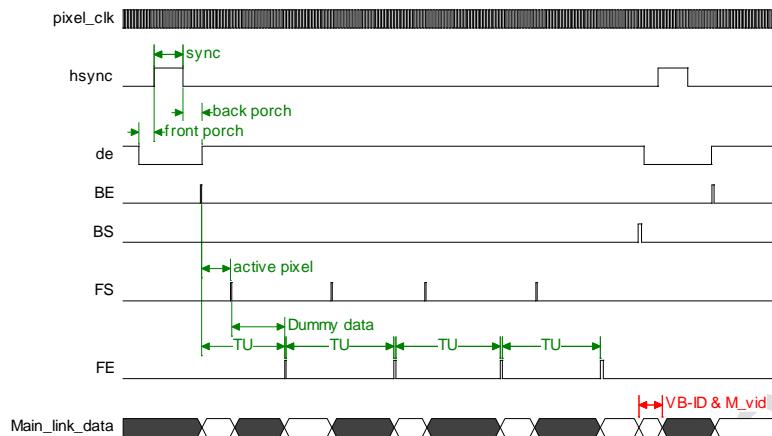


Fig. 11-16 TU in Main Link vs. Video Stream

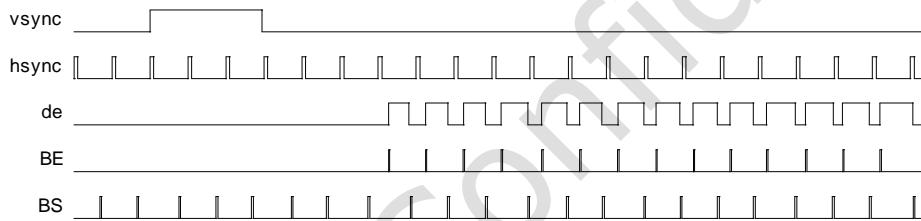


Fig. 11-17 Symbol BE and BS vs. Video Stream

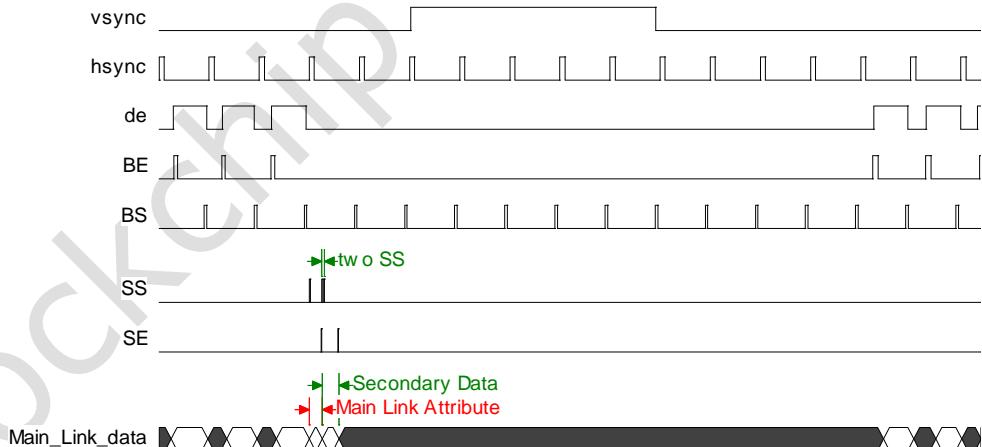


Fig. 11-18 Main Link Attribute Insertion in Main Link

After inserting the Main Link attributes data (and optionally, secondary data packet), the DisplayPort transmitter must insert a skew of two LS_CLK cycles between adjacent lanes. The following figure shows how the symbols must be transported after this inter-lane skewing. All the symbols, both those transmitted during video display period and those transmitted during video blanking period, are skewed by two LS_CLK period between adjacent lanes.

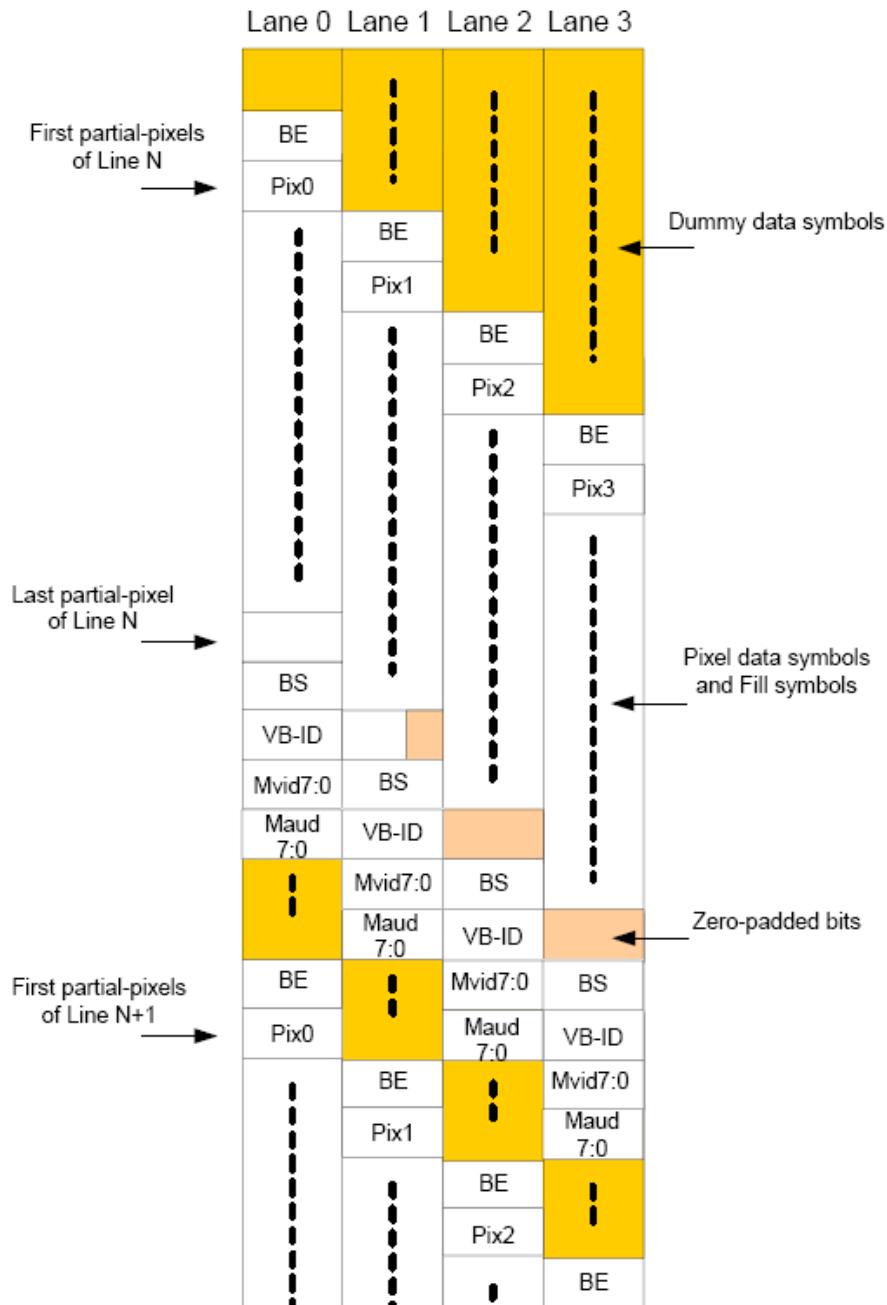


Fig. 11-19 Inter-lane Skewing

Audio sent to sink device is separated to three parts:

- ✓ AVI Info Frame
- ✓ Audio_TimeStamp Packet
- ✓ Audio_Stream Packet

All of these packets are sent as secondary data.

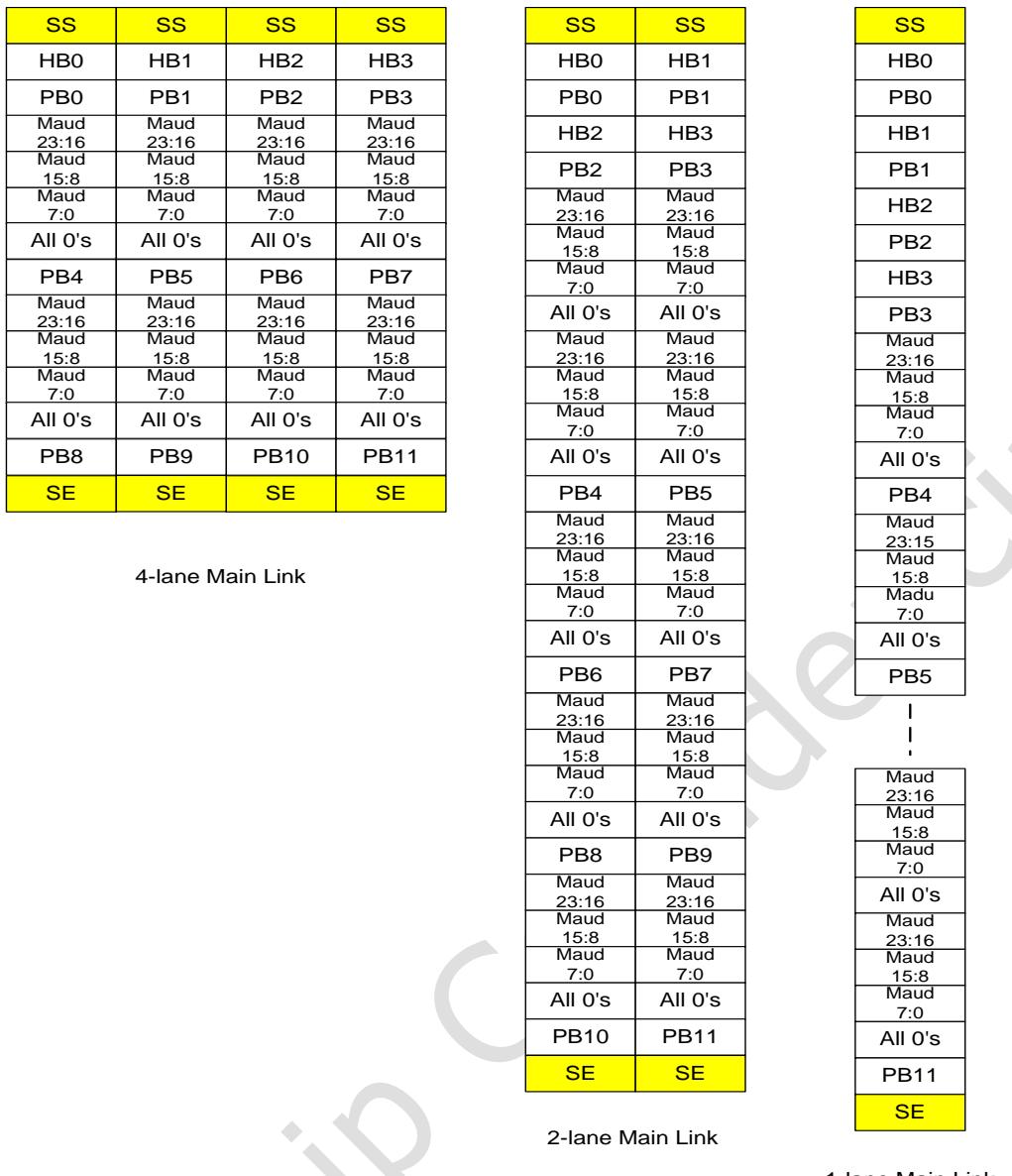


Fig. 11-20 Audio_TimeStamp Packet

Table 11-5 Header Bytes of Audio_Stream Packet

BYTE	Content
Header BYTE 0	Secondary-data Packet ID Info Frame packet, Audio Time Stamp packet, and Audio Stream packet must have the same Packet ID when they are associated with the same audio stream.
Header BYTE 1	0x02
Header BYTE 2	Reserved 0
Header BYTE 3	Bits 2:0 = ChannelCount, Actual channel count – 1 Bit 3 = Reserved (= 0) Bits 7:4 = Coding Type, 0000 = IEC60958-like coding All other values are reserved for DisplayPort

Table 11-6 Audio_Stream Packet over the Main Link for One or Two or Four Channel Audio

Four Lane ^④				Two Lane ^④		One Lane ^④
Lane 0 ^④	Lane 1 ^④	Lane 2 ^④	Lane 3 ^④	Lane 0 ^④	Lane 1 ^④	Lane 0 ^④
S ^④	SS ^④	SS ^④	SS ^④	SS ^④	SS ^④	SS ^④
HB0 ^④	HB1 ^④	HB2 ^④	HB3 ^④	HB0 ^④	HB1 ^④	HB0 ^④
PB0 ^④	PB1 ^④	PB2 ^④	PB3 ^④	PB0 ^④	PB1 ^④	PB0 ^④
S0_Ch1_B0 ^④	S0_Ch2_B0 ^④	S1_Ch1_B0 ^④	S1_Ch2_B0 ^④	HB2 ^④	HB3 ^④	HB1 ^④
S0_Ch1_B1 ^④	S0_Ch2_B1 ^④	S1_Ch1_B1 ^④	S1_Ch2_B1 ^④	PB2 ^④	PB3 ^④	PB1 ^④
S0_Ch1_B2 ^④	S0_Ch2_B2 ^④	S1_Ch1_B2 ^④	S1_Ch2_B2 ^④	S0_Ch1_B0 ^④	S0_Ch2_B0 ^④	HB2 ^④
S0_Ch1_B3 ^④	S0_Ch2_B3 ^④	S1_Ch1_B3 ^④	S1_Ch2_B3 ^④	S0_Ch1_B1 ^④	S0_Ch2_B1 ^④	PB2 ^④
PB4 ^④	PB5 ^④	PB6 ^④	PB7 ^④	S0_Ch1_B2 ^④	S0_Ch2_B2 ^④	HB3 ^④
S2_Ch1_B0 ^④	S2_Ch2_B0 ^④	S3_Ch1_B0 ^④	S3_Ch2_B0 ^④	S0_Ch1_B3 ^④	S0_Ch2_B3 ^④	PB3 ^④
S2_Ch1_B1 ^④	S2_Ch2_B1 ^④	S3_Ch1_B1 ^④	S3_Ch2_B1 ^④	PB4 ^④	PB5 ^④	S0_Ch1_B0 ^④
S2_Ch1_B2 ^④	S2_Ch2_B2 ^④	S3_Ch1_B2 ^④	S3_Ch2_B2 ^④	S1_Ch1_B0 ^④	S1_Ch2_B0 ^④	S0_Ch1_B1 ^④
S2_Ch1_B3 ^④	S2_Ch2_B3 ^④	S3_Ch1_B3 ^④	S3_Ch2_B3 ^④	S1_Ch1_B1 ^④	S1_Ch2_B1 ^④	S0_Ch1_B2 ^④
PB8 ^④	PB9 ^④	PB10 ^④	PB11 ^④	S1_Ch1_B2 ^④	S1_Ch2_B2 ^④	S0_Ch1_B3 ^④
“S” stands for Sample, “B” for Byte, and “Ch” for Channel. For example, S0_Ch1_B0 means Byte 0 of Channel1 of Sample0. ^④				S1_Ch1_B3 ^④	S1_Ch2_B3 ^④	PB4 ^④
				PB6 ^④	PB7 ^④	S0_Ch2_B0 ^④
				S2_Ch1_B0 ^④	S2_Ch2_B0 ^④	S0_Ch2_B1 ^④
				S2_Ch1_B1 ^④	S2_Ch2_B1 ^④	S0_Ch2_B2 ^④
				S2_Ch1_B2 ^④	S2_Ch2_B2 ^④	S0_Ch2_B3 ^④
				S2_Ch1_B3 ^④	S2_Ch2_B3 ^④	PB5 ^④

Table 11-7 Audio Stream Packet over the Main Link for Three to Eight Channel Audio

Four Lane ^④				Two Lane ^④		One Lane ^④
Lane 0 ^④	Lane 1 ^④	Lane 2 ^④	Lane 3 ^④	Lane 0 ^④	Lane 1 ^④	Lane 0 ^④
SS ^④	SS ^④	SS ^④	SS ^④	SS ^④	SS ^④	SS ^④
HB0 ^④	HB1 ^④	HB2 ^④	HB3 ^④	HB0 ^④	HB1 ^④	HB0 ^④
PB0 ^④	PB1 ^④	PB2 ^④	PB3 ^④	PB0 ^④	PB1 ^④	PB0 ^④
S0_Ch1_B0 ^④	S0_Ch2_B0 ^④	S0_Ch3_B0 ^④	S0_Ch4_B0 ^④	HB2 ^④	HB3 ^④	HB1 ^④
S0_Ch1_B1 ^④	S0_Ch2_B1 ^④	S0_Ch3_B1 ^④	S0_Ch4_B1 ^④	PB2 ^④	PB3 ^④	PB1 ^④
S0_Ch1_B2 ^④	S0_Ch2_B2 ^④	S0_Ch3_B2 ^④	S0_Ch4_B2 ^④	S0_Ch1_B0 ^④	S0_Ch2_B0 ^④	HB2 ^④
S0_Ch1_B3 ^④	S0_Ch2_B3 ^④	S0_Ch3_B3 ^④	S0_Ch4_B3 ^④	S0_Ch1_B1 ^④	S0_Ch2_B1 ^④	PB2 ^④
PB4 ^④	PB5 ^④	PB6 ^④	PB7 ^④	S0_Ch1_B2 ^④	S0_Ch2_B2 ^④	HB3 ^④
S0_Ch5_B0 ^④	S0_Ch6_B0 ^④	S0_Ch7_B0 ^④	S0_Ch8_B0 ^④	S0_Ch1_B3 ^④	S0_Ch2_B3 ^④	PB3 ^④
S0_Ch5_B1 ^④	S0_Ch6_B1 ^④	S0_Ch7_B1 ^④	S0_Ch8_B1 ^④	PB4 ^④	PB5 ^④	S0_Ch1_B0 ^④
S0_Ch5_B2 ^④	S0_Ch6_B2 ^④	S0_Ch7_B2 ^④	S0_Ch8_B2 ^④	S0_Ch3_B0 ^④	S0_Ch4_B0 ^④	S0_Ch1_B1 ^④
S0_Ch5_B3 ^④	S0_Ch6_B3 ^④	S0_Ch7_B3 ^④	S0_Ch8_B3 ^④	S0_Ch3_B1 ^④	S0_Ch4_B1 ^④	S0_Ch1_B2 ^④
PB8 ^④	PB9 ^④	PB10 ^④	PB11 ^④	S0_Ch3_B2 ^④	S0_Ch4_B2 ^④	S0_Ch1_B3 ^④
“S” stands for Sample, “B” for Byte, and “Ch” for Channel. For example, S0_Ch1_B0 means Byte 0 of Channel1 of Sample0. ^④				S0_Ch3_B3 ^④	S0_Ch4_B3 ^④	PB4 ^④
				PB6 ^④	PB7 ^④	S0_Ch2_B0 ^④
				S0_Ch5_B0 ^④	S0_Ch6_B0 ^④	S0_Ch2_B1 ^④
				S0_Ch5_B1 ^④	S0_Ch6_B1 ^④	S0_Ch2_B2 ^④
				S0_Ch5_B2 ^④	S0_Ch6_B2 ^④	S0_Ch2_B3 ^④
				S0_Ch5_B3 ^④	S0_Ch6_B3 ^④	PB5 ^④

“S” stands for Sample, “B” for Byte, and “Ch” for Channel. For example, S0_Ch1_B0 means Byte 0 of Channel1 of Sample0.^④

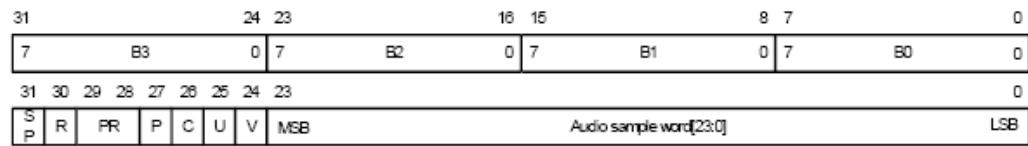


Fig. 11-21 Data Mapping within the Four Byte Payload of an Audio_Stream Packet

Table 11-8 Bit Definition of the Payload of an Audio_Stream Packet with IEC60958-like Coding

Bit Name	Description
Audio sample word	Audio data. Content of this data depends on the audio coding type. In case of LPCM audio, the most significant bit of the audio is placed in byte 2, bit 7. If the audio data size is less than 24 bits then unused least significant bits must be zero-padded.
V	Validity flag
U	User bit
C	Channel status
P	Parity bit
PR	Preamble code and its correspondence with IEC-60958 preamble: 00 – Subframe 1 and start of the audio block (11101000 preamble) 01 – Subframe 1 (1110010 preamble) 10 – Subframe 2 (1110100 preamble)
R	Reserved bit. It must be 0
SP	Sample present bit: 1 – Sample information is present and can be processed. 0 – Sample information is not present. All channels of one sample, whether used or unused, must have the same value for the sample present bit. This bit is especially useful when two channel audio is transported over a four lane Main Link. In this operation, Main Link lanes two and three may or may not have the audio sample data. This bit indicates whether the audio sample is present or not.

When the audio is input from I²S or Super Audio interface, user bit, channel status and preamble code will be generated by DP_TX.

11.3.12 RS Encode

All of the secondary-data packets must be protected via ECC based on RS (15, 13). The generator polynomial for the RS encoder is:

$$G(x) = x^2 + g_1 \cdot x + g_0$$

Where $g_1 = a_4$ and $g_0 = a$

With encoding of the base field GF (2⁴), "a" is equal to (0, 0, 1, 0) which gives $a_4 = (0, 0, 1, 1)$. The logic equations for implementing g_1 and g_0 multiplications are listed below (where $c [3:0]$ is a 4-bit nibble being multiplied by g_1 or g_0):

$$\begin{aligned} g_1 \cdot c[3:0] &= \{c[3]^2, c[2]^2, c[1]^2, c[0]^2\} \\ g_0 \cdot c[3:0] &= \{c[3], c[2], c[1], c[0]\} \end{aligned}$$

11.3.13 HDCP Authentication and Encryption

The HDCP encryption engine contains all the necessary logic to encrypt the data in main link except K-code. The HDCP Authentication and Encryption can be performed by hardware HDCP module. Pre-programmed HDCP keys and Key Selector Value (KSV) stored in SPSRAM are used in HDCP process. A resulting calculated value is applied to an XOR mask during each clock cycle to encrypt the data.

The HDCP authentication can also be performed by software. In this mode the KSV vector is first exchanged through AUX channel and this is controlled by software. After that the software starts the HDCP calculation and reads out the Ri values from the receiver side and compares the result. The software authentication is enabled by setting 'HW_AUTH_EN' bit to 0.

The data packing is working at half link clock frequency, while HDCP module is working at full link clock frequency. There is a HDCP FIFO to change the clock domain.

11.3.14 Scramble

Scrambling of the Main Link data is performed for EMI reduction prior to ANSI 8B/10B encoding on the transmitter. De-scrambling of the data symbols is performed subsequent to ANSI 8B/10B decoding at the receiver. Utilization of scrambling should result in approximately 7dB reduction in peak spectrum. Each of the Main Link lanes is scrambled and de-scrambled independently, each with a 16 bit LFSR as follows:

$$G(X) = X^{16} + X^5 + X^4 + X^3 + 1$$

BS symbol will be replaced with a SR symbol every 512th BS symbol. The SR symbol is used to reset the LFSR to FFFFh. The data scrambling rules must be as follows:

The LFSR advances on all symbols, both data and special symbols.

Special symbols are not scrambled.

Data symbols, including "fill data" are scrambled.

Scrambling must be disabled during Link Training and Recovered Link Clock Quality Measurement.

11.3.15 8B/10B Encode

The following 8B/10B encoder encodes each symbol (8bit data + 1bit control) to 10 bit DC balanced and transition maximized data. It is then mux'ed with the link training or PRBS BIST data and goes through a Serdes FIFO.

11.3.16 Serdes FIFO

Each Serdes has a dedicated clock; the four lanes data of main link should be distributed to each of the Serdes_TX analog cores through a DDR FIFO in order to change the data bus from 20 bits to 10 bits.

11.3.17 DisplayPort AUX CH

The auxiliary link is a low speed (1Mbps) half-duplex bi-directional link used to get state/attributes, such as link capabilities, link status and the EDID, from the receiver. The transmitter will also initiate the link training through the AUX link.

It is used to perform the native AUX CH link service and device services, such as DPCD reading/writing, link initialization, training and monitoring. It is also used to bridge the APB transactions (such as the EDID read) between the GPU and the display devices.

The DisplayPort Source Device must weakly pull up the AUX CH lines between the AC-coupling capacitors and the Source Connector to assist source detection by the Sink Device.

Source detection capable Sink Device must have ac-coupling capacitors. The Sink Device must pull down the AUX CH lines with $1\text{M}\Omega$ resistors between the sink connector and the ac-coupling capacitors, and monitor the DC voltage of AUX CH line.

The AUX CH uses the Manchester-II code for the self-coded transmission of signals as shown below in follows.

The data format of request transaction is shown as Fig. 11-22 AUX CH Request Transaction Data Format



Fig. 11-22 AUX CH Request Transaction Data Format

The reply transaction is shown as Fig. 11-23 AUX CH Reply Transaction Data Format

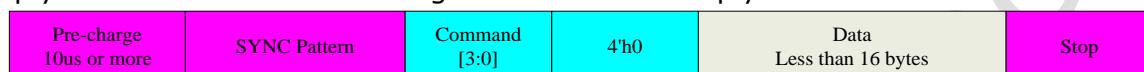


Fig. 11-23 AUX CH Reply Transaction Data Format

Pre-charge: 10 to 16 consecutive 0's in Manchester II code to pre-charge the AUX-CH+ and AUX-CH- to a common mode voltage.

Sync Pattern: Start with 16 consecutive 0's in Manchester II code, end with the AUX-CH+ driven to high for a two bit period and low for a two bit period, which is illegal in Manchester II code. The AUX-CH- must be driven to the opposite polarity.

Request Command:

COMM[3]	COMM[2]	COMM[1]	COMM[0]
1: DisplayPort transaction	000: Request type is write 001: Request type is read Others: Reserved		
0: I2C transaction	1: MOT (Middle-of-Transaction) = 1 0: MOT (Middle-of-Transaction) = 0	00 : write 01 : read 00 : write_status_request 01 : Reserved	

Reply Command:

COMM[3]	COMM[2]	COMM[1]	COMM[0]
I ² C-over-AUX Reply field: 00: I ² C_ACK. 01: I ² C_NACK. 10: I ² C_DEFER. 11: Reserved.		Native AUX CH Reply field: 00: AUX_ACK. 01: AUX_NACK. 10: AUX_DEFER. 11: Reserved.	

Stop: AUX-CH+ driven to high for a two bit period and low for a two bit period, which is illegal in Manchester II code. The AUX-CH- must be driven to the opposite polarity.

The request of AUX CH transaction comes from several sources: I²C interface (for native AUX CH access or I²C over AUX CH mapping), hardware link training module, hardware HDCP module, register control AUX CH module. All of these requests are translated to a uniform internal control interface that composed with following signals:

- ✓ aux_read: enable AUX CH read transaction.
- ✓ aux_write: enable AUX CH write transaction.
- ✓ aux_address: the address of current AUX CH read transaction.
- ✓ aux_length: the length data of current AUX CH read transaction.
- ✓ aux_mot: the MOT data of current AUX CH read transaction.
- ✓ aux_operation_done: indicate current AUX CH read transaction is finished.
- ✓ aux_operation_error: indicate current AUX CH read transaction is error.

The data that should be sent to sink device via AUX CH and the data that is received from sink device via AUX CH is stored to a buffer. In write transaction, after the write transaction is enabled, AUX CH transfer module will read data from buffer automatically and send these data to AUX CH link. Diagram of the AUX CH module is shown as Fig. 8-21.

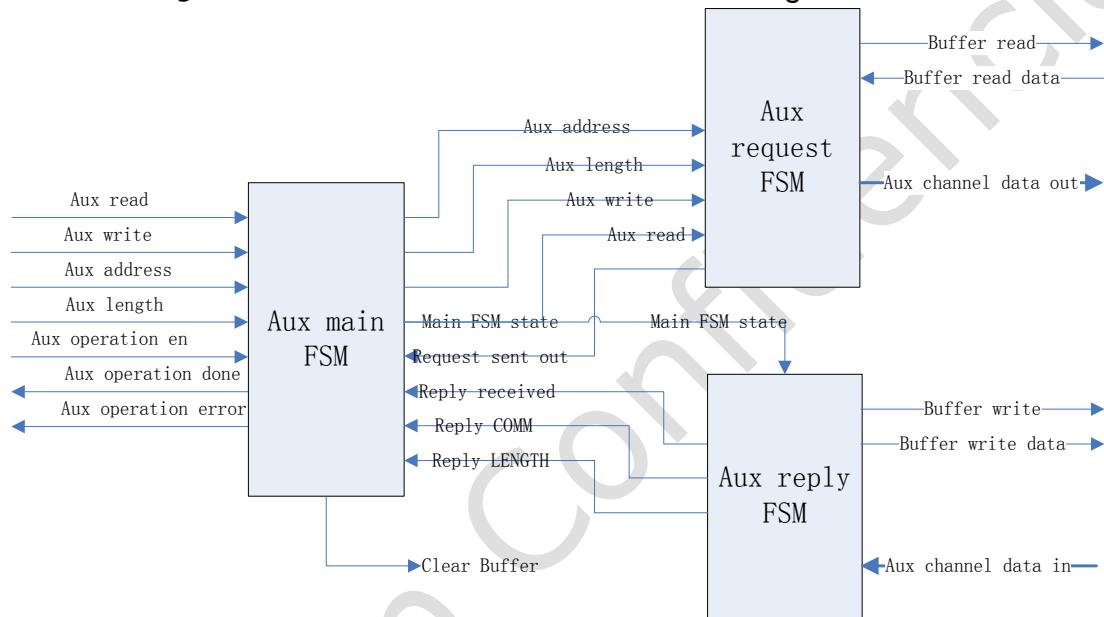


Fig. 11-24 Diagram of AUX CH Module

The typical action flow of the Source Device and the Sink Device upon a Hot Plug Detect event is shown in the following figure.

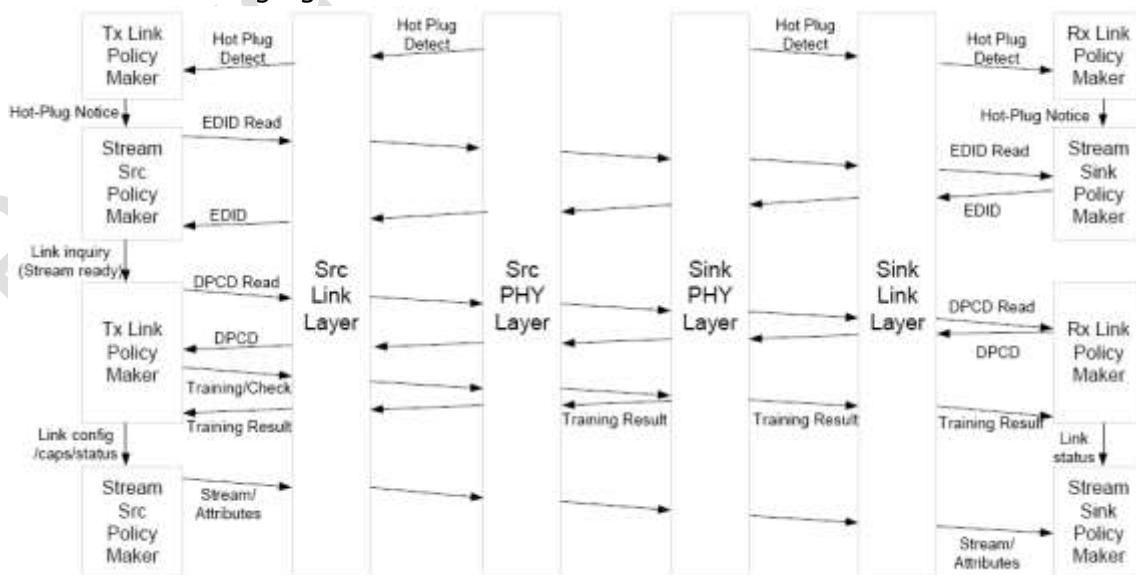


Fig. 11-25 Action Flow Sequences of the Source upon Hot Plug Detect Event

The link training flow chart is shown as in the following two figures.

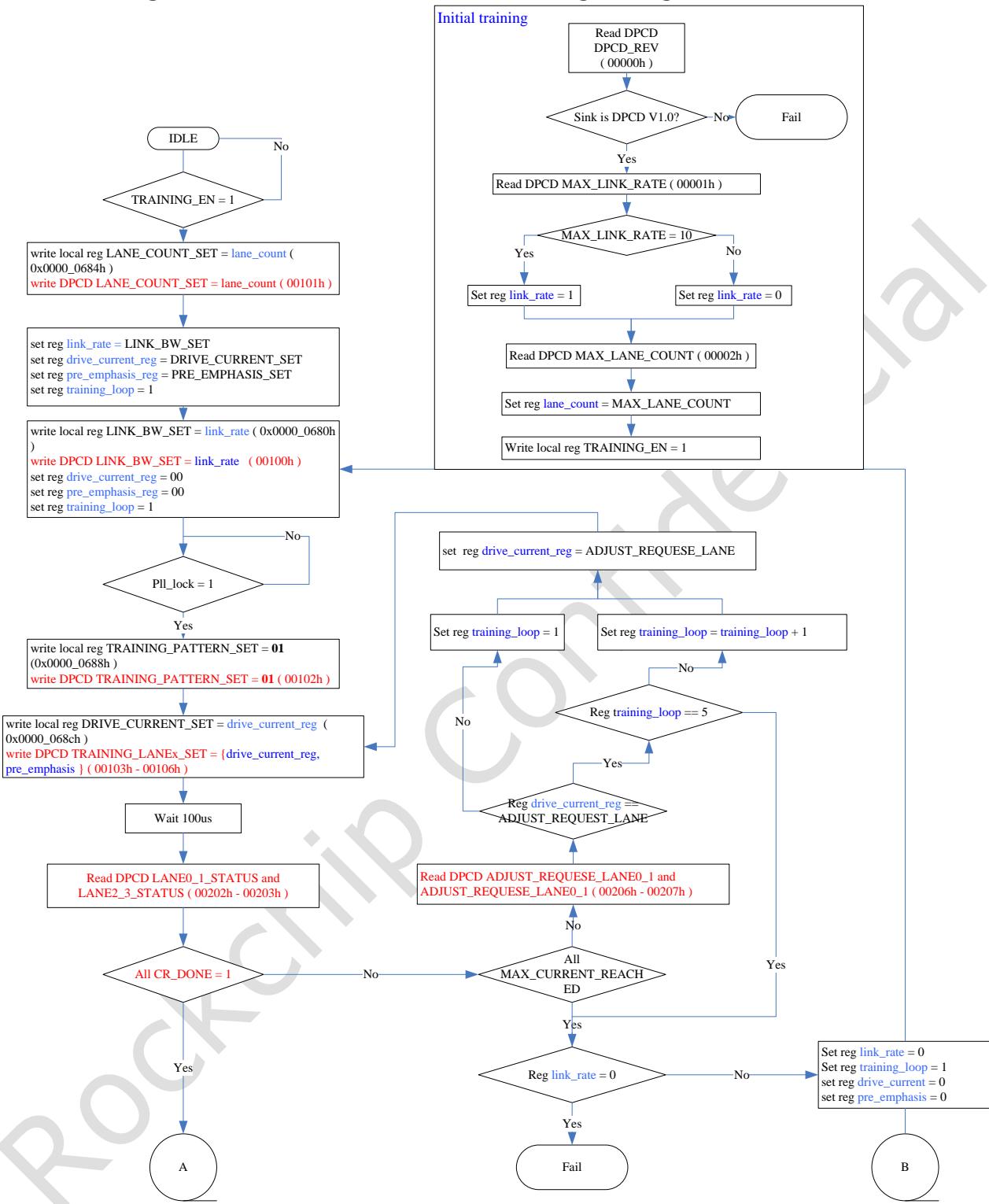
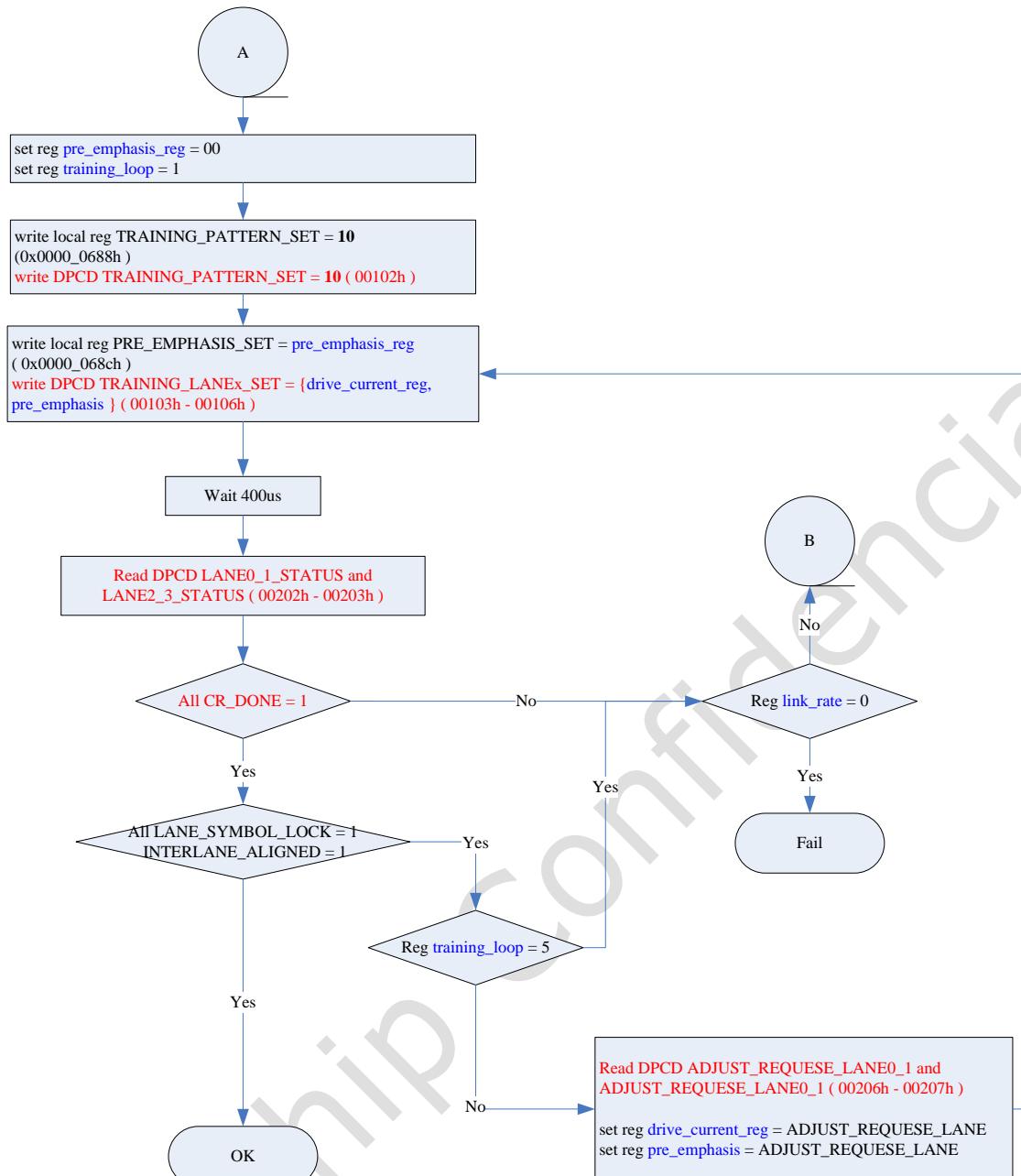


Fig. 11-26 Link Training Initial and Clock Recovery Training



Note : link_rate, lane_count, drive_current_reg, pre_emphasis_reg and training_loop are temporary variables.

Fig. 11-27 Equalizer Training

11.3.18 SSC (Spread-Spectrum Clock) Generation

DPTX implements the programmable SSC down-spreading with up to 0.5% modulation amplitude and 30k/33k modulation frequency. The frequency modulation envelop is linear tri-angle as shown in following figure (F_0 is the nominal frequency before modulation which is 1.62G or 2.7G, A_M and T_M is the modulation amplitude and modulation period respectively).

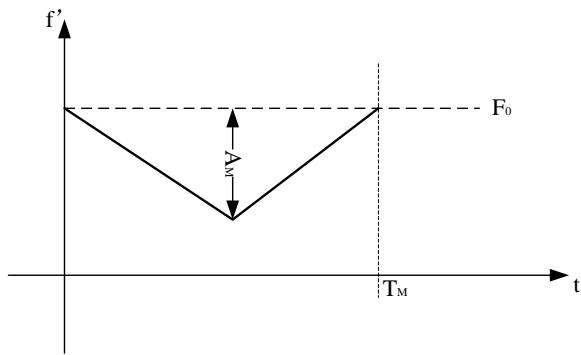


Fig. 11-28 High-speed Link Down-spreading Frequency vs, Time

In order to generate the frequency modulation, the equivalent phase (P) modulation is applied based on the following formula:

$$\Delta P = \int \Delta f * dt$$

The ΔP calculation is done in digital circuit and the phase value is sent to an interpolator circuit to final generate the phase-modulated clock. The modulation amplitude AM is programmable from 0 to 0.5%* F_0 .

11.3.19 SRAM Interface

The SRAM interface is implemented to read/write the HDCP key from/to the external efuse memory. The HDCP key is programmed into SRAM memory by user. After the key is programmed, the SoC can read HDCP key out of the efuse memory in normal work mode. The HDCP key in the efuse memory cannot be read out from the APB bus. The following is the interface timing of efuse interface.

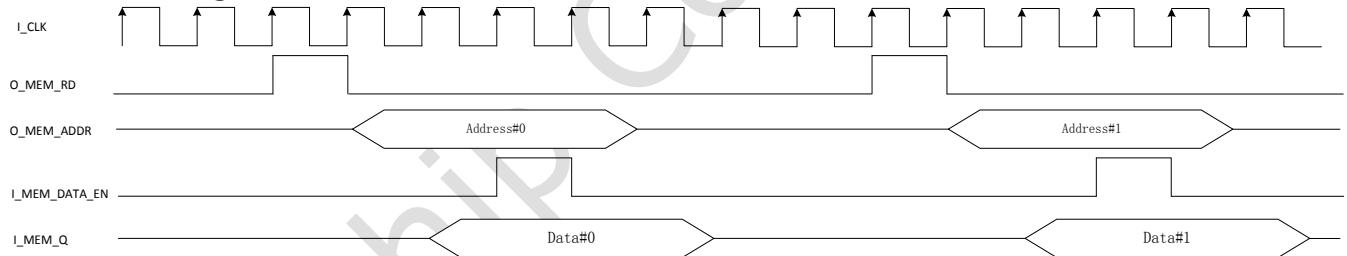


Fig. 11-29 interface timing of SRAM interface

11.3.20 HDCP Key Arrangement

To do HDCP authentication, the system may burst load all the product key to the DP TX IP core, so all the keys in memory should follow the dedicated structure to match the arithmetic of HDCP unit.

The data in memory contains 4 parts

- Product keys 285 bytes (address 1 to 285)
- Key check sum 1 byte (address 286)

The first five byte of product key should always be aksv [39:0], followed with the 280 byte product keys (40x56 bit). To protect aksv, the first byte of aksv should be located at the "0_0000_0001" of input address.

To add all the product keys with the key check sum byte will get the result 0000_0000 (don't care about the carry), which can be used to protect the product keys.

So the detail structure of data arranged in the memory is defined as bellow:

Table 11-9 HDCP Key Arrangement

Addr[7:0]	Content	Description	Addr[7:0]	Content	Description
001	aksv[39:32]	aksv	282	keys39[31:24]	other product keys
002	aksv[31:24]		283	keys39[23:16]	
003	aksv[23:16]		284	keys39[15:08]	
004	aksv[15:8]		285	keys39[07:00];	
005	aksv[7:0]		286	hdcp_check_sum[7:0]	Checksum value
006	keys00[55:48]		287		
007	keys00[47:40]	other product keys	288		
008	keys00[39:32]		289		
009	keys00[31:24]		290		
010	keys00[23:16]		291		
011	keys00[15:08]		292		
012	keys00[07:00]		293		
013	keys01[55:48]		294		
014	keys01[47:40]		295		
015	keys01[39:32]		296		
016	keys01[31:24]		297		
.....		298		
.....		299		
279	keys39[55:48]		300		
280	keys39[47:40]		301		
281	keys39[39:32]		302		

11.3.21 APB Bus Interface

The APB Bus interface is used at the configuration registers interface. DP_TX will take the following APB address space:

Base Address + 0000_0000 ~ Base Address + 0000_23FC

11.3.22 DP IP Registers

Terminology

	Description
R/C	Read-clear, field will return read value and be cleared by hardware.
RO	Read only register, field may be read but not written. Write have no effect.
R/W	Read/Write accessible register, filed may be written or read. Read-data will equal write data.
S/C or SC	Write-auto-clear, field may be written to and will be cleared by hardware.
W/C1	Write-once-clear, field will be cleared to zero if written with a one.
WO	Write-only, field may be written to, but reads will always return zero.
W/OC	Write-once, field may be written to, but hardware will update read value.
R/U	Read-update, field will be updated by hardware after read

	Description
Reserved	A reserved register bit may not be physically implemented in the device or could be implemented to control a proprietary function. Therefore, register bits labeled "Reserved" should not be changed by software. On reads, software must use appropriate masks to extract the defined bits and not rely on reserved bits being any particular value. On writes, software must ensure that the values of reserved bit positions are preserved. That is to say, the values of reserved bit positions must first be read, merged with the new values for other bit positions and then written back. For conciseness, this document notes the default value of a reserved register bit as "0" even though default values for reserved bits may actually be unspecified.
[mm:nn]	This denotes a group of register bits: mm represents the most significant bits and nn the least significant among the quantity referenced. By convention, the less significant bits have lower offset, so that bit 0 in a register is always the least significant bit.
Table X-X	Blue text indicates a linked cross-reference. Click on the link to jump to the reference information.

Register MAP

General Control Register Definition

General Control Register Definition

Name	Address	Type	Description	Reset Value
DP_TX_VERSION	Base + 0x0010	RO	DP_TX version register	0x0000_0060
FUNC_EN_1	Base + 0x0018	R/W	Function Enable Register 1	0x0000_007D
FUNC_EN_2	Base + 0x001C	R/W	Function Enable Register 2	0x0000_0087
VIDEO_CTL_1	Base + 0x0020	R/W	Video Control 1	0x0000_0000
VIDEO_CTL_2	Base + 0x0024	R/W	Video Control 2	0x0000_0010
VIDEO_CTL_3	Base + 0x0028	R/W	Video Control 3	0x0000_0000
VIDEO_CTL_4	Base + 0x002C	R/W	Video Control 4	0x0000_0000
VIDEO_CTL_8	Base + 0x003C	R/W	Video Control 8	0x0000_0020
VIDEO_CTL_10	Base + 0x0044	R/W	Video Control 10	0x0000_0000
TOTAL_LINE_CFG_L	Base + 0x0048	R/W	Total Line Low Byte Configure Register	0x0000_0000
TOTAL_LINE_CFG_H	Base + 0x004C	R/W	Total Line High Byte Configure Register	0x0000_0000
ACTIVE_LINE_CFG_L	Base + 0x0050	R/W	Active Line Low Byte Configure Register	0x0000_0000
ACTIVE_LINE_CFG_H	Base + 0x0054	R/W	Active Line High Byte Configure Register	0x0000_0000
V_F_PORCH_CFG	Base + 0x0058	R/W	Vertical Front Porch Configure Register	0x0000_0000
V_SYNC_WIDTH_CFG	Base + 0x005C	R/W	Vertical Sync Width Configure Register	0x0000_0000
V_B_PORCH_CFG	Base + 0x0060	R/W	Vertical Back Porch Configure Register	0x0000_0000
TOTAL_PIXEL_CFG_L	Base + 0x0064	R/W	Total Pixel Low Byte Configure Register	0x0000_0000
TOTAL_PIXEL_CFG_H	Base + 0x0068	R/W	Total Pixel High Byte	0x0000_0000

General Control Register Definition				
Name	Address	Type	Description	Reset Value
			Configure Register	
ACTIVE_PIXEL_CFG_L	Base + 0x006C	R/W	Active Pixel Low Byte Configure Register	0x0000_0000
ACTIVE_PIXEL_CFG_H	Base + 0x0070	R/W	Active Pixel High Byte Configure Register	0x0000_0000
H_F_PORCH_CFG_L	Base + 0x0074	R/W	Horizon Front Porch Low Byte Configure Register	0x0000_0000
H_F_PORCH_CFG_H	Base + 0x0078	R/W	Horizon Front Porch High Byte Configure Register	0x0000_0000
H_SYNC_CFG_L	Base + 0x007C	R/W	Horizon Sync Width Low Byte Configure Register	0x0000_0000
H_SYNC_CFG_H	Base + 0x0080	R/W	Horizon Sync Width High Byte Configure Register	0x0000_0000
H_B_PORCH_CFG_L	Base + 0x0084	R/W	Horizon Back Porch Low Byte Configure Register	0x0000_0000
H_B_PORCH_CFG_H	Base + 0x0088	R/W	Horizon Back Porch High Byte Configure Register	0x0000_0000
VIDEO_STATUS	Base + 0x008C	RO	Video Status Register	0x0000_0003
TOTAL_LINE_STA_L	Base + 0x0090	RO	Total Line Status Low Byte Register	0x0000_0001
TOTAL_LINE_STA_H	Base + 0x0094	RO	Total Line Status High Byte Register	0x0000_0000
ACTIVE_LINE_STA_L	Base + 0x0098	RO	Active Line Status Low Byte Register	0x0000_0000
ACTIVE_LINE_STA_H	Base + 0x009C	RO	Active Line Status High Byte Register	0x0000_0000
V_F_PORCH_STA	Base + 0x00A0	RO	Vertical Front Porch Status Register	0x0000_0001
V_SYNC_STA	Base + 0x00A4	RO	Vertical Sync Width Status Register	0x0000_0000
V_B_PORCH_STA	Base + 0x00A8	RO	Vertical Back Porch Status Register	0x0000_0000
TOTAL_PIXEL_STA_L	Base + 0x00AC	RO	Total Pixel Status Low Byte Register	0x0000_0000
TOTAL_PIXEL_STA_H	Base + 0x00B0	RO	Total Pixel Status High Byte Register	0x0000_0000
ACTIVE_PIXEL_STA_L	Base + 0x00B4	RO	Active Pixel Status Low Byte Register	0x0000_0000
ACTIVE_PIXEL_STA_H	Base + 0x00B8	RO	Active Pixel Status High Byte Register	0x0000_0000
H_F_PORCH_STA_L	Base + 0x00BC	RO	Horizon Front Porch Status Low Byte Register	0x0000_0000
H_F_PORCH_STA_H	Base + 0x00C0	RO	Horizon Front Porch Status High Byte Register	0x0000_0000
H_SYNC_STA_L	Base + 0x00C4	RO	Horizon Sync Width Status Low Byte Register	0x0000_0000
H_SYNC_STA_H	Base + 0x00C8	RO	Horizon Sync Width Status High Byte Register	0x0000_0000
H_B_PORCH_STA_L	Base + 0x00CC	RO	Horizon Back Porch Status Low Byte Register	0x0000_0000
H_B_PORCH_STA_H	Base + 0x00D0	RO	Horizon Back Porch Status High Byte Register	0x0000_0000
SPDIF_AUDIO_CTL_0	Base + 0x00D8	R/W	SPDIF Audio Control Register 0	0x0000_0000

General Control Register Definition				
Name	Address	Type	Description	Reset Value
DP_AUDIO_CTL_1	Base + 0x00DC	R/W	SPDIF Audio Control Register 1	0x0000_0000
SPDIF_AUDIO_STA_0	Base + 0x00E0	RO	SPDIF Audio Status Register 0	0x0000_0000
SPDIF_AUDIO_STA_1	Base + 0x00E4	RO	SPDIF Audio Status Register 1	0x0000_0000
SPDIF_ERR_THRD	Base + 0x00E8	R/W	SPDIF Error Threshold Register	0x0000_0001
SPDIF_ERR_CNT	Base + 0x00EC	RO, SC	SPDIF Error Counter Register	0x0000_0000
AUDIO_BIST_CTL	Base + 0x00F0	R/W	Audio BIST Control Register	0x0000_0000
AUD_FREQ_CNT_1	Base + 0x00F4	RO	Audio Input Clock Frequency Counter Register 1.	0x0000_0000
AUD_FREQ_CNT_2	Base + 0x00F8	RO	Audio Input Clock Frequency Counter Register 2.	0x0000_0000
AVI_DB1 ~ AVI_DB13	Base + 0x01D0~Base + 0x0200	R/W	AVI InfoFrame Packet Data Byte	0x0000_0000
AUDIO_DB0~AUDIO_DB10	Base + 0x021C~Base + 0x0240	R/W	Audio InfoFrame Packet Data Byte	0x0000_0000
IF_TYPE	Base + 0x0244	R/W	InfoFrame Packet Type Code.	0x0000_0000
IF_PKT_DB1~IF_PKT_DB25	Base + 0x0254~Base + 0x02B4	R/W	InfoFrame Packet Data Byte	0x0000_0000
MPEG_DB1~MPEG_DB10	Base + 0x02D0~Base + 0x02F4	R/W	MPEG Source InfoFrame Packet Data Byte	0x0000_0000
REUSE_SPD_HB	Base + 0x02F8~Base + 0x0304	R/W	Reuse SPD HB0 ~ HB3	0x0000_0000
REUSE_SPD_PB	Base + 0x0308~Base + 0x0314	R/W	Reuse SPD PB0 ~ PB3	0x0000_0000
PSR_FRAME_UPDATA_CTRL	Base + 0x0318	R/W	Frame update control for PSR	0x0000_0000
VSC_SHADOW_DB0~VSC_SHADOW_DB7	Base+ 0x031C~Base+ 0x0338	R/W	VSC shadow data bytes 0 ~ 7	0x0000_0000
VSC_SHADOW_PB0~VSC_SHADOW_PB1	Base+ 0x033C~Base+ 0x0340	R/W	VSC shadow parity byte 0 ~ 1	0x0000_0000
AUDIO_I2S_CH_STA_1	Base + 0x0344	R/W	Audio I2S Channel Status Register 1	0x0000_0000
AUDIO_I2S_CH_STA_2	Base + 0x0348	R/W	Audio I2S Channel Status Register 2	0x0000_0000
AUDIO_I2S_CH_STA_3	Base + 0x034C	R/W/C 1	Audio I2S Channel Status Register 3	0x0000_0000
AUDIO_I2S_CH_STA_4	Base + 0x0350	R/W/C 1	Audio I2S Channel Status Register 4	0x0000_0000
AUDIO_I2S_CH_STA_5	Base + 0x0354	R/W	Audio I2S Channel Status Register 5	0x0000_000B
LANE_MAP	Base + 0x035C	R/W	Lane Map Register	0x0000_00E4
ANALOG_CTL_2	Base + 0x0374	R/W	Analog Control Register 2	0x0000_0008
HIDDEN_REG	Base + 0x0390	R/W	Debug Register	0x0000_0003
INT_STATE	Base + 0x03C0	RO	Interrupt Status Register	0x0000_0000
COMMON_INT_STA_1	Base + 0x03C4	R/W	Common Interrupt Status Register 1	0x0000_0000

General Control Register Definition				
Name	Address	Type	Description	Reset Value
COMMON_INT_STA_2	Base + 0x03C8	R/W	Common Interrupt Status Register 2	0x0000_0000
COMMON_INT_STA_3	Base + 0x03CC	R/W/C 1	Common Interrupt Status Register 3	0x0000_0000
COMMON_INT_STA_4	Base + 0x03D0	R/W/C 1	Common Interrupt Status Register 4	0x0000_0000
SPDIF_BIPHASE_INT_STA	Base + 0x03D4	WO	SPDIF Biphase Interrupt Status Register	0x0000_0000
DP_INT_STA	Base + 0x03DC	R/W/C 1	DisplayPort Interrupt Status Register	0x0000_0000
COMMON_INT_MASK_1	Base + 0x03E0	R/W	Common Interrupt Mask Register1	0x0000_0000
COMMON_INT_MASK_2	Base + 0x03E4	R/W	Common Interrupt Mask Register2	0x0000_0000
COMMON_INT_MASK_3	Base + 0x03E8	R/W	Common Interrupt Mask Register3	0x0000_0000
COMMON_INT_MASK_4	Base + 0x03EC	R/W	Common Interrupt Mask Register4	0x0000_0000
DP_INT_STA_MASK	Base + 0x03F8	R/W	DisplayPort Interrupt enable Register	0x0000_0000
INT_CTL	Base + 0x03FC	R/W	Interrupt Control Register	0x0000_0000

HDCP Register Definition**Register Definition for HDCP Function**

Name	Address	Type	Description	Reset Value
HDCP_STA	Base + 0x0400	RO	HDCP Status Register	0x0000_0000
HDCP_CTL_0	Base + 0x0404	R/W	HDCP Control Register 0	0x0000_0000
HDCP_CTL_1	Base + 0x0408	R/W	HDCP Control Register 1	0x0000_0000
AKSV0	Base + 0x0414	RO	HDCP AKSV Register 0	0x0000_0000
AKSV1	Base + 0x0418	RO	HDCP AKSV Register 1	0x0000_0000
AKSV2	Base + 0x041C	RO	HDCP AKSV Register 2	0x0000_0000
AKSV3	Base + 0x0420	RO	HDCP AKSV Register 3	0x0000_0000
AKSV4	Base + 0x0424	RO	HDCP AKSV Register 4	0x0000_0000
AN0	Base + 0x0428	RO	HDCP AN Register 0	0x0000_0000
AN1	Base + 0x042C	RO	HDCP AN Register 1	0x0000_0000
AN2	Base + 0x0430	RO	HDCP AN Register 2	0x0000_0000
AN3	Base + 0x0434	RO	HDCP AN Register 3	0x0000_0000
AN4	Base + 0x0438	RO	HDCP AN Register 4	0x0000_0000
AN5	Base + 0x043C	RO	HDCP AN Register 5	0x0000_0000
AN6	Base + 0x0440	RO	HDCP AN Register 6	0x0000_0000
AN7	Base + 0x0444	RO	HDCP AN Register 7	0x0000_0000
BKSV0	Base + 0x0448	R/W	HDCP BKSV Register 0	0x0000_0000
BKSV1	Base + 0x044C	R/W	HDCP BKSV Register 1	0x0000_0000
BKSV2	Base + 0x0450	R/W	HDCP BKSV Register 2	0x0000_0000
BKSV3	Base + 0x0454	R/W	HDCP BKSV Register 3	0x0000_0000
BKSV4	Base + 0x0458	R/W	HDCP BKSV Register 4	0x0000_0000
RI0	Base + 0x045C	R/W	HDCP RI Register 0	0x0000_0000
RI1	Base + 0x0460	R/W	HDCP RI Register 1	0x0000_0000
HW_RX_CAPS	Base + 0x0468	RO	HDCP Receiver BCAPS Register	0x0000_0000
HW_RX_BINFO_0	Base + 0x046C	RO	HDCP Receiver BINFO Register 0	0x0000_0000
HW_RX_BINFO_1	Base + 0x0470	RO	HDCP Receiver BINFO Register 1	0x0000_0000

Register Definition for HDCP Function				
Name	Address	Type	Description	Reset Value
HW_SKIP_RPT_ZERO_DEV	Base + 0x0474	R/W	HDCP Debug Control Register	0x0000_0000
SPSRAM_CFG_1	Base + 0x0488	R/W	SPSRAM Access Configure Register 1.	0x0000_0020
HDCP_AUTH_DBG	Base + 0x049C	RO	HDCP AUTH FSM status	0x0000_0000
HDCP_ENC_DBG	Base + 0x04A0	RO	HDCP ENC FSM status	0x0000_0000
HDCP_FRAME_NUM	Base + 0x04A4	RO	HDCP Frame Counter Register	0x0000_0000
HDCP_VID_0	Base + 0x04A8	R/W	HDCP Embedded "Blue Screen" Content Registers 0	0x0000_0000
HDCP_VID_1	Base + 0x04AC	R/W	HDCP Embedded "Blue Screen" Content Registers 1	0x0000_0000
HDCP_VID_2	Base + 0x04B0	R/W	HDCP Embedded "Blue Screen" Content Registers 2	0x0000_0000
HDCP_AM0_0	Base + 0x04C0	RO	HDCP AM0 Register 0	0x0000_0000
HDCP_AM0_1	Base + 0x04C4	RO	HDCP AM0 Register 1	0x0000_0000
HDCP_AM0_2	Base + 0x04C8	RO	HDCP AM0 Register 2	0x0000_0000
HDCP_AM0_3	Base + 0x04CC	RO	HDCP AM0 Register 3	0x0000_0000
HDCP_AM0_4	Base + 0x04D0	RO	HDCP AM0 Register 4	0x0000_0000
HDCP_AM0_5	Base + 0x04D4	RO	HDCP AM0 Register 5	0x0000_0000
HDCP_AM0_6	Base + 0x04D8	RO	HDCP AM0 Register 6	0x0000_0000
HDCP_AM0_7	Base + 0x04DC	RO	HDCP AM0 Register 7	0x0000_0000
HW_WRITE_AKSV_WAIT	Base + 0x0500	R/W	HDCP Wait R0 Timing Register	0X0000_0064
LINK_CHECK_TIMER	Base + 0x0504	R/W	Link check Timer Register	0X0000_0076
HW_RPTR_RDY_TIMER	Base + 0x0508	R/W	HDCP Repeater Ready Wait Timer Register	0X0000_0083
READY_POLL_TIMER	Base + 0x050C	R/W	Poll timing value for READY	0X0000_0009
HDCP_HIDDEN_REG	Base + 0x0510	R/W	HDCP HIDDEN Register	0X0000_0000
HDCP_B_INIT_RND0	Base + 0x0514	WO	HDCP B initial value[7:0]	0X0000_00C7
HDCP_B_INIT_RND1	Base + 0x0518	WO	HDCP B initial value[15:8]	0X0000_00D7
HDCP_B_INIT_RND2	Base + 0x051C	WO	HDCP B initial value[23:16]	0X0000_0074
HDCP_B_INIT_RND3	Base + 0x0520	WO	HDCP B initial value[31:24]	0X0000_0032
HDCP_B_INIT_RND4	Base + 0x0524	WO	HDCP B initial value[39:32]	0X0000_00D3
HDCP_B_INIT_RND5	Base + 0x0528	WO	HDCP B initial value[47:40]	0X0000_00D0
HDCP_B_INIT_RND6	Base + 0x052C	WO	HDCP B initial value[55:48]	0X0000_007F
HDCP_B_INIT_RND7	Base + 0x0530	WO	HDCP B initial value[63:56]	0X0000_00C4
HDCP_B_INIT_RND8	Base + 0x0534	WO	HDCP B initial value[64]	0X0000_0001
HDCP_K_INIT_RND0	Base + 0x0538	WO	HDCP B initial value[7:0]	0X0000_001C
HDCP_K_INIT_RND1	Base + 0x053C	WO	HDCP B initial value[15:8]	0X0000_00C3

Register Definition for HDCP Function				
Name	Address	Type	Description	Reset Value
HDCP_K_INIT_RND_2	Base + 0x0540	WO	HDCP B initial value[23:16]	0X0000_00F6
HDCP_K_INIT_RND_3	Base + 0x0544	WO	HDCP B initial value[31:24]	0X0000_00E5
HDCP_K_INIT_RND_4	Base + 0x0548	WO	HDCP B initial value[39:32]	0X0000_00C3
HDCP_K_INIT_RND_5	Base + 0x054C	WO	HDCP B initial value[47:40]	0X0000_00E7
HDCP_K_INIT_RND_6	Base + 0x0550	WO	HDCP B initial value[55:48]	0X0000_00DF
HDCP_K_INIT_RND_7	Base + 0x0554	WO	HDCP B initial value[63:56]	0X0000_00D6
HDCP_K_INIT_RND_8	Base + 0x0558	WO	HDCP B initial value[71:64]	0X0000_00D7
HDCP_K_INIT_RND_9	Base + 0x055C	WO	HDCP B initial value[79:72]	0X0000_006E
HDCP_K_INIT_RND_1	Base + 0x0560	WO	HDCP B initial value[83:80]	0X0000_0001

DisplayPort Register Definition

Register Definition for DisplayPort Function				
Name	Address	Type	Description	Reset Value
SYS_CTL_1	Base + 0x0600	R/W	System Control Register #1	0x0000_0000
SYS_CTL_2	Base + 0x0604	R/W	System Control Register #2	0X0000_0040
SYS_CTL_3	Base + 0x0608	R/W, RO	System Control Register #3	0x0000_0000
SYS_CTL_4	Base + 0x060C	R/W	System Control Register #4	0x0000_0000
DP_VID_CTL	Base + 0x0610	RO	DP Video Control Register	0x0000_0020
DP_AUD_CTL	Base + 0x0618	R/W	DP Audio Control Register	0x0000_0000
PKT_SEND_CTL	Base + 0x0640	R/W	Packet Send Control Register	0x0000_0000
DP_HDCP_CTL	Base + 0x0648	R/W	DisplayPort HDCP Control Register	0x0000_0000
SPDIF_PHASE1_CTL_0	Base + 0x0650	R/W	SPDIF Phase 1 Control Register 0	0x0000_0000
SPDIF_PHASE1_CTL_1	Base + 0x0654	R/W	SPDIF Phase 1 Control Register 1	0x0000_0000
SPDIF_PHASE2_CTL_0	Base + 0x0658	R/W	SPDIF Phase 2 Control Register 0	0x0000_0000
SPDIF_PHASE2_CTL_1	Base + 0x065C	R/W	SPDIF Phase 2 Control Register 1	0x0000_0000
SPDIF_PHASE3_CTL_0	Base + 0x0660	R/W	SPDIF Phase 3 Control Register 0	0x0000_0000
SPDIF_PHASE3_CTL_1	Base + 0x0664	R/W	SPDIF Phase 3 Control Register 1	0x0000_0000
LINK_BW_SET	Base + 0x0680	R/W	Main Link Bandwidth Setting Register	0x0000_000A
LANE_COUNT_SET	Base + 0x0684	R/W	DP Main Link Lane Number Register	0x0000_0004
DP_TRAINING_PTN_SET	Base + 0x0688	R/W	DP Training Pattern Set Register	0x0000_0000
DP_LN0_LINK_TRAINING_CTL	Base + 0x068C	R/W, RO	DP Lane 0 Link Training Control Register	0x0000_0000

Register Definition for DisplayPort Function				
Name	Address	Type	Description	Reset Value
DP_LN1_LINK_TRAINING_CTL	Base + 0x0690	R/W, RO	DP Lane 1 Link Training Control Register	0x0000_0000
DP_LN2_LINK_TRAINING_CTL	Base + 0x0694	R/W, RO	DP Lane 2 Link Training Control Register	0x0000_0000
DP_LN3_LINK_TRAINING_CTL	Base + 0x0698	R/W, RO	DP Lane 3 Link Training Control Register	0x0000_0000
DP_HW_LINK_TRAINING_CONTROL	Base + 0x06A0	R/W, RO	DP HW LINK TRAINING_CONTROL Register	0x0000_0000
DP_DEBUG_CTL	Base + 0x06C0	R R/W	DP Debug Control Register #1	0x0000_0000
HPD_DEGLITCH_L	Base + 0x06C4	R/W	DP HPD De-glitch Low Byte Register	0x0000_005E
HPD_DEGLITCH_H	Base + 0x06C8	R/W	DP HPD De-glitch High Byte Register	0x0000_001A
POLLING_PERIOD	Base + 0x06CC	R/W	DP polling period	0x0000_000E
DP_LINK_DEBUG_CTL	Base + 0x06E0	R/W	DP Link Debug Control Register	0x0000_0010
DP_SINK_COUNT	Base + 0x06E4	RO	DP Sink Count	0x0000_0000
DP_IRD_VECTOR	Base + 0x06E8	RO	DP Ird Vector	0x0000_0000
DP_LINK_STATUS0	Base + 0x06EC	RO	DP Lane0 and Lane1 Status	0x0000_0000
DP_LINK_STATUS1	Base + 0x06F0	RO	DP Lane2 and Lane3 Status	0x0000_0000
DP_ALIGN_STATUS`	Base + 0x06F4	RO	DP Align Status	0x0000_0000
DP_SINK_STATUS	Base + 0x06F8	RO	DP Sink Status	0x0000_0000
M_VID_0	Base + 0x0700	R/W	DP M_VID Configure Register #0	0x0000_0000
M_VID_1	Base + 0x0704	R/W	DP M_VID Configure Register #1	.0x0000_0000
M_VID_2	Base + 0x0708	R/W	DP M_VID Configure Register #2	0x0000_0000
N_VID_0	Base + 0x070C	R/W	DP N_VID Configure Register #0	0x0000_0000
N_VID_1	Base + 0x0710	R/W	DP N_VID Configure Register #1	0x0000_0080
N_VID_2	Base + 0x0714	R/W	DP N_VID Configure Register #2	0x0000_0000
M_VID_MON	Base + 0x0718	RO	DP M_VID value monitoring register	0x0000_0000
DP_VIDEO_FIFO_THRESHOLD	Base + 0x0730	R/W	DP FIFO Threshold Register	0x0000_0000
DP_AUDIO_MARGIN	Base + 0x073C	R/W	DP Audio Margin Register	0x0000_0020
M_AUD_MON	Base + 0x0740	RO	DP M_AUD value monitoring register	0x0000_0000
M_AUD_0	Base + 0x0748	R/W	M_AUD Configure Register #0	0x0000_0000
M_AUD_1	Base + 0x074C	R/W	M_AUD Configure Register #1	0x0000_0000
M_AUD_2	Base + 0x0750	R/W	M_AUD Configure Register #2	0x0000_0000
N_AUD_0	Base + 0x0754	R/W	DP N_AUD Configure Register #0	0x0000_0000
N_AUD_1	Base + 0x0758	R/W	DP N_AUD Configure Register #1	0x0000_0080
N_AUD_2	Base + 0x075C	R/W	DP N_AUD Configure	0x0000_0000

Register Definition for DisplayPort Function				
Name	Address	Type	Description	Reset Value
			Register #2	
DP_M_CAL_CTL	Base + 0x0760	R/W	DP M Value Calculation Control Register	0x0000_0000
M_VID_GEN_FILTER_TH	Base + 0x0764	R/W	DP M_VID Value Calculation Control Register	0x0000_0004
M_AUD_GEN_FILTE_R_TH	Base + 0x0778	R/W	DP M_AUD Value Calculation Control Register	0x0000_0002
AUX_CH_STA	Base + 0x0780	R/W	AUX Channel Access Status Register	0x0000_0000
AUX_ERR_NUM	Base + 0x0784	RO	AUX Channel Access Error Code Register	0x0000_0000
AUX_CH_DEFERCTL	Base + 0x0788	R/W	DP AUX CH DEFER Control Register	0x0000_007F
AUX_RX_COMM	Base + 0x078C	RO	DP AUX RX Command Register	0x0000_0000
BUFFER_DATA_CTL	Base + 0x0790	R/W, RO	DP Buffer Data Count Register	0x0000_0000
AUX_CH_CTL_1	Base + 0x0794	R/W	DP AUX Channel Control Register 1	0x0000_0000
AUX_ADDR_7_0	Base + 0x0798	R/W	DP AUX CH Address Register #0	0x0000_0000
AUX_ADDR_15_8	Base + 0x079C	R/W	DP AUX CH Address Register #1	0x0000_0000
AUX_ADDR_19_16	Base + 0x07A0	R/W	DP AUX CH Address Register #2	0x0000_0000
AUX_CH_CTL_2	Base + 0x07A4	R/W	DP AUX CH Control Register 2	0x0000_0000
BUF_DATA_0	Base + 0x07C0	R/W	AUX CH buffer data	0x0000_00FF
BUF_DATA_1	Base + 0x07C4	R/W	AUX CH buffer data	0x0000_00FF
BUF_DATA_2	Base + 0x07C8	R/W	AUX CH buffer data	0x0000_00FF
BUF_DATA_3	Base + 0x07CC	R/W	AUX CH buffer data	0x0000_00FF
BUF_DATA_4	Base + 0x07D0	R/W	AUX CH buffer data	0x0000_00FF
BUF_DATA_5	Base + 0x07D4	R/W	AUX CH buffer data	0x0000_00FF
BUF_DATA_6	Base + 0x07D8	R/W	AUX CH buffer data	0x0000_00FF
BUF_DATA_7	Base + 0x07DC	R/W	AUX CH buffer data	0x0000_00FF
BUF_DATA_8	Base + 0x07E0	R/W	AUX CH buffer data	0x0000_00FF
BUF_DATA_9	Base + 0x07E4	R/W	AUX CH buffer data	0x0000_00FF
BUF_DATA_10	Base + 0x07E8	R/W	AUX CH buffer data	0x0000_00FF
BUF_DATA_11	Base + 0x07EC	R/W	AUX CH buffer data	0x0000_00FF
BUF_DATA_12	Base + 0x07F0	R/W	AUX CH buffer data	0x0000_00FF
BUF_DATA_13	Base + 0x07F4	R/W	AUX CH buffer data	0x0000_00FF
BUF_DATA_14	Base + 0x07F8	R/W	AUX CH buffer data	0x0000_00FF
BUF_DATA_15	Base + 0x07FC	R/W	AUX CH buffer data	0x0000_00FF

Register definitions for SoC IP implementation

Register definitions for SoC IP implementation				
Name	Address	Type	Description	Reset Value
SOC_GENERAL_CTL	Base + 0x0800	R/W	General control register	0x0000_0101
ATE_TEST_CTL	Base + 0x0804	R/W SC	ATE test control register	0x0000_0000
ATE_TEST_STATUS	Base + 0x0808	RO	ATE test status register	0x0000_0000

Register definitions for SoC IP implementation				
Name	Address	Type	Description	Reset Value
ATE_TEST_ERR_C_NT0	Base + 0x080C	RO	Lane0 ATE test error counter register	0x0000_0000
ATE_TEST_ERR_C_NT1	Base + 0x0810	RO	Lane1 ATE test error counter register	0x0000_0000
ATE_TEST_ERR_C_NT2	Base + 0x0814	RO	Lane2 ATE test error counter register	0x0000_0000
ATE_TEST_ERR_C_NT3	Base + 0x0818	RO	Lane3 ATE test error counter register	0x0000_0000
DP_TEST_80B_PATTERNO	Base + 0x081C	R/W	80b pattern [29:0]	0x0000_0000
DP_TEST_80B_PATTERN1	Base + 0x0820	R/W	80b pattern [59:30]	0x0000_0000
DP_TEST_80B_PATTERN2	Base + 0x0824	R/W	80b pattern [79:60]	0x0000_0000
DP_TEST_HBR2_PATTERN	Base + 0x0828	R/W	Hbr2 compliance SR count	0x0000_0000
AUD_CTL	Base + 0x0834	R/W	Audio control register	0x0000_0001
CRC_CON	Base + 0x0890	R/W	CRC control register	0x0000_0000
CRC_RESULT	Base + 0x0894	R	CRC result register	0x0000_0000
ANALOG_CTL_5	Base + 0x0914	R/W	PC2 Control Register	0x0000_0000
ANALOG_CTL_6	Base + 0x0918	R/W	AMP_400MV_0DB	0x0000_0050
ANALOG_CTL_7	Base + 0x091C	R/W	AMP_600MV_0DB	0x0000_0078
ANALOG_CTL_8	Base + 0x0920	R/W	AMP_800MV_0DB	0x0000_00A0
ANALOG_CTL_9	Base + 0x0924	R/W	AMP_1200MV_0DB	0x0000_00F0
ANALOG_CTL_10	Base + 0x0928	R/W	AMP_400MV_3P5DB	0x0000_0064
ANALOG_CTL_11	Base + 0x092C	R/W	AMP_600MV_3P5DB	0x0000_0096
ANALOG_CTL_12	Base + 0x0930	R/W	AMP_800MV_3P5DB	0x0000_00C8
ANALOG_CTL_13	Base + 0x0934	R/W	AMP_400MV_6DB	0x0000_0078
ANALOG_CTL_14	Base + 0x0938	R/W	AMP_600MV_6DB	0x0000_00B4
ANALOG_CTL_15	Base + 0x093C	R/W	AMP_400MV_9DB	0x0000_00A0
ANALOG_CTL_16	Base + 0x0940	R/W	EMP_400MV_0DB	0x0000_0000
ANALOG_CTL_17	Base + 0x0944	R/W	EMP_600MV_0DB	0x0000_0000
ANALOG_CTL_18	Base + 0x0948	R/W	EMP_800MV_0DB	0x0000_0000
ANALOG_CTL_19	Base + 0x094C	R/W	EMP_1200MV_0DB	0x0000_0000
ANALOG_CTL_20	Base + 0x0950	R/W	EMP_400MV_3P5DB	0x0000_0028
ANALOG_CTL_21	Base + 0x0954	R/W	EMP_600MV_3P5DB	0x0000_003C
ANALOG_CTL_22	Base + 0x0958	R/W	EMP_800MV_3P5DB	0x0000_0050
ANALOG_CTL_23	Base + 0x095C	R/W	EMP_400MV_6DB	0x0000_0050
ANALOG_CTL_24	Base + 0x0960	R/W	EMP_600MV_6DB	0x0000_0078
ANALOG_CTL_25	Base + 0x0964	R/W	EMP_400MV_9DB	0x0000_00A0
ANALOG_CTL_26	Base + 0x0968	R/W	PC2_400MV_0DB	0x0000_0004
ANALOG_CTL_27	Base + 0x096C	R/W	PC2_600MV_0DB	0x0000_0006
ANALOG_CTL_28	Base + 0x0970	R/W	PC2_800MV_0DB	0x0000_0008
ANALOG_CTL_29	Base + 0x0974	R/W	PC2_1200MV_0DB	0x0000_000C
ANALOG_CTL_30	Base + 0x0978	R/W	PC2_400MV_3P5DB	0x0000_0006
ANALOG_CTL_31	Base + 0x097C	R/W	PC2_600MV_3P5DB	0x0000_0009
ANALOG_CTL_32	Base + 0x0980	R/W	PC2_800MV_3P5DB	0x0000_000C
ANALOG_CTL_33	Base + 0x0984	R/W	PC2_400MV_6DB	0x0000_0008
ANALOG_CTL_34	Base + 0x0988	R/W	PC2_600MV_6DB	0x0000_000C
ANALOG_CTL_35	Base + 0x098C	R/W	PC2_400MV_9DB	0x0000_000C
ANALOG_CTL_36	Base + 0x0990	R/W	CH0_AMP_FORCE_VALUE	0x0000_0050
ANALOG_CTL_37	Base + 0x0994	R/W	CH0_EMP_FORCE_VALUE	0x0000_0000
ANALOG_CTL_38	Base + 0x0998	R/W	CH0_PC2_FORCE_VALUE	0x0000_0004

Register definitions for SoC IP implementation				
Name	Address	Type	Description	Reset Value
ANALOG_CTL_39	Base + 0x099C	R/W	CH1_AMP_FORCE_VALUE	0x0000_0050
ANALOG_CTL_40	Base + 0x09A0	R/W	CH1_EMP_FORCE_VALUE	0x0000_0000
ANALOG_CTL_41	Base + 0x09A4	R/W	CH1_PC2_FORCE_VALUE	0x0000_0004
ANALOG_CTL_42	Base + 0x09A8	R/W	CH0_CH1_FORCE_CTRL	0x0000_0000
ANALOG_CTL_43	Base + 0x09AC	R/W	CH2_AMP_FORCE_VALUE	0x0000_0050
ANALOG_CTL_44	Base + 0x09B0	R/W	CH2_EMP_FORCE_VALUE	0x0000_0000
ANALOG_CTL_45	Base + 0x09B4	R/W	CH2_PC2_FORCE_VALUE	0x0000_0004
ANALOG_CTL_46	Base + 0x09B8	R/W	CH3_AMP_FORCE_VALUE	0x0000_0050
ANALOG_CTL_47	Base + 0x09BC	R/W	CH3_EMP_FORCE_VALUE	0x0000_0000
ANALOG_CTL_48	Base + 0x09C0	R/W	CH3_PC2_FORCE_VALUE	0x0000_0004
ANALOG_CTL_49	Base + 0x09C4	R/W	CH2_CH3_FORCE_CTRL	0x0000_0000
I2S_CTRL	Base + 0x09C8	R/W	I2S control register	0x0000_0000
I2S_CH_SWAP	Base + 0x09CC	R/W	I2S channel swap	0x0000_000b
I2S_CH_CTRL	Base + 0x09D0	R/W	I2S channel control	0x0000_00e4
I2S_CH_CTRL1	Base + 0x09D4	R/W	I2S channel control_1	0x0000_0000
LINK_POLICY	Base + 0x09D8	R/W	Dp Link Policy	0x0000_0050
PLL_REG_1	Base + 0x00FC	R/W	PII_control_1	0x0000_0011
PLL_REG_2	Base + 0x09E4	R/W	PII_control_2	0x0000_0011
PLL_REG_3	Base + 0x09E8	R/W	PII_control_3	0x0000_002B
PLL_REG_4	Base + 0x09EC	R/W	PII_control_4	0x0000_0023
PLL_REG_5	Base + 0x0A00	R/W	PII_control_5	0x0000_0000
PLL_REG_MAC	Base + 0x0A04	R/W	PII_control_MAC	0x0000_0000
FREQ_IN_REG	Base + 0x0A10	R/W	freq_in_reg	0x0000_0080
P_REG_FRQ	Base + 0x0A14	RO	frequency counter ,digital output for debug	0x0000_0000
P_REG_FRQ_COU NT_RDY	Base + 0x0A18	RO	frequency counter ready indicator	0x0000_0000
P_BAND_DEC_RESET	Base + 0x0A1C	WO	reset band decoder	0x0000_0000
SSC_REG	Base + 0x0104	R/W	SSC control	0x0000_000A
TX_COMMON	Base + 0x0114	R/W	Tx terminal resistor control	0x0000_003A
TX_COMMON2	Base + 0x0118	R/W	Tx terminal resistor control2	0x0000_0050
TX_COMMON3	Base + 0x0A08	R/W	Tx terminal resistor control3	0x0000_0000
DP_AUX	Base + 0x0120	R/W	Aux control	0x0000_0007
DP_BIAS	Base + 0x0124	R/W	Bias control	0x0000_0034
DP_TEST	Base + 0x0128	R/W	Test mode	0x0000_0000
DP_PD	Base + 0x012C	R/W	Power down control	0x0000_00FF
DP_RESERV1	Base + 0x0130	R/W	RESERVD1	0x0000_0000
DP_RESERV2	Base + 0x0134	R/W	RESERVD2	0x0000_0011

General Control Register Definition

Table 11-10 DP_TX Version (DP_TX_VERSION)

Register	Address	Type	Description	Reset Value
DP_TX_VERSION	Base + 0x0010	RO	DP_TX_VERSION	0x0000_0060

DP_TX_VERSION	Bit	Description	Initial State
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DP_TX_VERSION	[31:0]	<7:5> process 011 (Global Foundry 28nm) <4:3>: Version 00: Rev A <2:0>: Minor revision 000: rev .1 Notion: It is effective when PAD_DVDD is supplied	0x60
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Table 11-11 Function Enable Register 1(FUNC_EN_1)

Register	Address	Type	Description	Reset Value
FUNC_EN_1	Base + 0x0018	R/W	Function Enable Register 1	0x0000_007D

FUNC_EN_1	Bit	Description	Initial State
-	[31:7]	Reserved	0
VID_CAP_FUNC_EN_N	[6]	Video capture functions enable. 0: Normal operation, 1: Disable video capture.	1
VID_FIFO_FUNC_EN_N	[5]	Video FIFO functions enable. 0: Normal operation, 1: Disable video FIFO.	1
AUD_FIFO_FUNC_EN_N	[4]	Audio FIFO functions enable. 0: Normal operation, 1: Disable Audio FIFO.	1
AUD_FUNC_EN_N	[3]	Audio FIFO and capture module function enable. 0 = Normal operation, 1: Disable Audio FIFO and capture module. If audio data (DMA or SPDIF) should be transmitted, AUD_FUNC_EN_N and AUD_FIFO_FUNC_EN_N should be set to 0 (enable).	1
HDCP_FUNC_EN_N	[2]	HDCP module functions enable. 0: Normal operation, 1: Disable HDCP logic. By disabling and enabling HDCP, all of registers in HDCP are cleared, except for the HDCP key inside of SPSRAM. Therefore, as an easy way to prepare re-authentication, firmware can disable and enable again to clear all HDCP registers.	1
-	[1]	Reserved	0
SW_FUNC_EN_N	[0]	Software defined function enable. 0: Normal operation, 1: Disable All the function modules. The bit has the highest priority, if the bit is 1, other function enable bits does not work.	1

Table 11-12 Function Enable Register 2 (FUNC_EN_2)

Register	Address	Type	Description	Reset Value
FUNC_EN_2	Base + 0x001C	R/W	Function Enable Register 2	0x0000_0087

FUNC_EN_2	Bit	Description	Initial State
-	[31:8]	Reserved	0

FUNC_EN_2	Bit	Description	Initial State
SSC_FUNC_EN_N	[7]	SSC module enable. 0: Normal mode, 1: Disable SSC module. To apply updated SSC parameters into SSC operation, firmware must disable and enable this bit.	1
-	[6:3]	Reserved	0
AUX_FUNC_EN_N	[2]	AUX channel module function enable. 0: Normal operation, 1: Disable AUX channel module.	1
SERDES_FIFO_FUNC_EN_N	[1]	Serdes FIFO function enable. 0: Normal mode, 1: Disable Serdes FIFO. To reset the serdes fifo, firmware must disable and enable this bit.	1
LS_CLK_DOMAIN_FUNC_EN_N	[0]	Link symbol clock domain modules functions enable. 0: Normal mode, 1: Disable the modules in link symbol clock domain. To reset the modules in link symbol clock domain, firmware must disable and enable this bit.	1

Table 11-13 Video Control Register 1 (VIDEO_CTL_1)

Register	Address	Type	Description	Reset Value
VIDEO_CTL_1	Base + 0x0020	R/W	Video Control Register 1	0x0000_0000

VIDEO_CTL_1	Bit	Description	Initial State
-	[31:8]	Reserved	0
VIDEO_EN	[7]	Video data input enable. 0: Disable video data input. 1: Enable video data input, It takes effect at next video frame.	0
VIDEO_MUTE	[6]	Video mute enable. In video mute mode, the solid color, specified in Base + 0x04A8 ~ Base + 0x04B0, is displayed. 0: Disable, 1: Enable. Output video data is changed properly as soon as this bit is configured.	0
-	[5:0]	Reserved	0

Table 11-14 Video Control Register 2 (VIDEO_CTL_2)

Register	Address	Type	Description	Reset Value
VIDEO_CTL_2	Base + 0x0024	R/W	Video Control Register 2	0x0000_0010

VIDEO_CTL_2	Bit	Description	Initial State
-	[31:8]	Reserved	0
IN_D_RANGE	[7]	Dynamic range. This bit field is used to specify video data format in main stream attribute data. 1: CEA range (16 ~ 235), 0: VESA range (0 ~ 255).	0

VIDEO_CTL_2	Bit	Description	Initial State
IN_BPC	[6:4]	Video input bit per color/ component (bpc). This bit field is used to specify video data format in main stream attribute data. Note that 6 bpc mode is invalid in YCbCr 422 mode. 100, 101, 110, 111: Reserved, 011: 12 bits, 010: 10 bits, 001: 8 bits, 000: 6 bits.	001
-	[3:2]	Reserved	0
IN_COLOR_F	[1:0]	Colorimetric format of input video. This is used to specify video data format in main stream attribute data. 11: Reserved, 10: YCbCr444, 01: YcbCr422, 00: RGB.	0

Table 11-15 Video Control Register 3 (VIDEO_CTL_3)

Register	Address	Type	Description	Reset Value
VIDEO_CTL_3	Base + 0x0028	R/W	Video Control Register 3	0x0000_0000

VIDEO_CTL_3	Bit	Description	Initial State
-	[31:8]	Reserved	0
IN_YC_COEFFI	[7]	YCbCr Coefficients of input video. This is used to specify video data format in main stream attribute data. 1: ITU709. 0: ITU601.	0
-	[6:5]	Reserved	0
VID_CHK_UPDATE_TYPE	[4]	Select video format stability check method in video capture block. 1: Check stability with the difference between adjacent frames. 0: Check stability with the difference of differences between adjacent frames. Compares difference of 1st and 2nd to difference of 3rd and 4th frame.	0
-	[3:0]	Reserved	0

Table 11-16 Video Control Register 4 (VIDEO_CTL_4)

Register	Address	Type	Description	Reset Value
VIDEO_CTL_4	Base + 0x002C	R/W	Video Control Register 4	0x0000_0000

VIDEO_CTL_4	Bit	Description	Initial State
-	[31:4]	Reserved	0
BIST_EN	[3]	Video BIST enable. 1: Enable video BIST, 0: Normal operation mode.	0
BIST_WIDTH	[2]	Control display BIST color bar width. 1: Each bar is 64 pixel width, 0: Each bar is 32 pixel width.	0

VIDEO_CTL_4	Bit	Description	Initial State
BIST_TYPE	[1:0]	Display BIST type. 00: Color bar, 01: White, gray and black bar, 10: Mobile white bar, 11: Reserved.	0

Table 11-17 Video Control Register 8 (VIDEO_CTL_8)

Register	Address	Type	Description	Reset Value
VIDEO_CTL_8	Base + 0x003C	R/W	Video Control Register 8	0x0000_0020

VIDEO_CTL_8	Bit	Description	Initial State
-	[31:8]	Reserved	0
VID_HRES_TH	[7:4]	Video Frame Horizontal Resolution variation threshold for video capture block. This bit field is used by CAPTURE block to determine whether STRM_VALID should be asserted.	2
VID_VRES_TH	[3:0]	Video Frame Vertical Resolution variation threshold for video capture block. This bit field is used by CAPTURE block to determine whether STRM_VALID should be asserted.	0

Table 11-18 Video Control Register 10 (VIDEO_CTL_10)

Register	Address	Type	Description	Reset Value
VIDEO_CTL_10	Base + 0x0044	R/W	Video Control Register 10	0x0000_0000

VIDEO_CTL_10	Bit	Description	Initial State
-	[31:5]	Reserved	0
F_SEL	[4]	Video format select. 1: Video format information from register, 0: Video format information from video_capture module. According to the configuration of this bit field, the values of video format status registers in Base + 0x008C~ 0x00D0 are determined, which are transferred as main stream attribute packet. Note that if BIST_EN is set to 1, F_SEL must be cleared to 0 although video format information comes from registers set by user.	0
-	[3]	Reserved	0
SLAVE_I_SCAN_CFG	[2]	Interlace scan mode configuration. 0: Progressive, 1: Interlace. When F_SEL is 1, this value is sent in main stream attribute packet. When BIST_EN is 1, this bit field is used to specify the BIST video stream format.	0
SLAVE_VSYNC_P_CFG	[1]	Slave mode VSYNC polarity configuration. 1: Low is active, 0: High is active. When F_SEL is 1, this value is sent in main stream attribute packet. When BIST_EN is 1, this bit field is used to specify the BIST video stream format.	0

VIDEO_CTL_10	Bit	Description	Initial State
SLAVE_HSYNC_P_CFG	[0]	Slave mode HSYNC polarity configuration. 1: Low is active, 0: High is active. When F_SEL is 1, this value is sent in main stream attribute packet. When BIST_EN is 1, this bit field is used to specify the BIST video stream format.	0

Table 11-19 Total Line Low Byte Configure Register (TOTAL_LINE_CFG_L)

Register	Address	Type	Description	Reset Value
TOTAL_LINE_CFG_L	Base + 0x0048	R/W	Total Line Byte Configure Register	0x0000_0000

TOTAL_LINE_CFG_L	Bit	Description	Initial State
-	[31:8]	Reserved	0
TOTAL_LINE_CFG_L	[7:0]	TOTAL_LINE_CFG is used to specify the number of lines in each frame. This register is TOTAL_LINE_CFG [7:0]. When F_SEL is 1, this value is sent in main stream attribute packet. When BIST_EN is 1, this bit field is used to specify the BIST video stream format.	0

Table 11-20 Total Line High Byte Configure Register (TOTAL_LINE_CFG_H)

Register	Address	Type	Description	Reset Value
TOTAL_LINE_CFG_H	Base + 0x004C	R/W	Total Line High Byte Configure Register	0x0000_0000

TOTAL_LINE_CFG_H	Bit	Description	Initial State
-	[31:4]	Reserved	0
TOTAL_LINE_CFG_H	[3:0]	TOTAL_LINE_CFG is used to specify the number of lines in each frame. This register is TOTAL_LINE_CFG [11:8]. When F_SEL is 1, this value is sent in main stream attribute packet. When Video BIST_EN is enabled, this bit must be configured right to generate right video format.	0

Table 11-21 Active Line Low Byte Configure Register (ACTIVE_LINE_CFG_L)

Register	Address	Type	Description	Reset Value
ACTIVE_LINE_CFG_L	Base + 0x0050	R/W	Active Line Low Byte Configure Register	0x0000_0000

ACTIVE_LINE_CFG_L	Bit	Description	Initial State
-	[31:8]	Reserved	0

ACTIVE_LINE_CFG_L	[7:0]	ACTIVE_LINE_CFG is used to specify the number of active lines in each frame. This register is ACTIVE_LINE_CFG [7:0]. When F_SEL is 1, this value is sent in main stream attribute packet. When BIST_EN is 1, this bit field is used to specify the BIST video stream format.	0
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Table 11-22 Active Line High Byte Configure Register (ACTIVE_LINE_CFG_H)

Register	Address	Type	Description	Reset Value
ACTIVE_LINE_CFG_H	Base + 0x0054	R/W	Active Line High Byte Configure Register	0x0000_0000

ACTIVE_LINE_CFG_H	Bit	Description	Initial State
-	[31:4]	Reserved	0
ACTIVE_LINE_CFG_H	[3:0]	ACTIVE_LINE_CFG is used to specify the number of active lines in each frame. This register is ACTIVE_LINE_CFG [11:8]. When F_SEL is 1, this value is sent in main stream attribute packet. When BIST_EN is 1, this bit field is used to specify the BIST video stream format.	0

Table 11-23 Vertical Front Porch Configure Register (V_F_PORCH_CFG)

Register	Address	Type	Description	Reset Value
V_F_PORCH_CFG	Base + 0x0058	R/W	Vertical Front Porch Configure Register	0x0000_0000
V_F_PORCH_CFG	Bit	Description	Initial State	
-	[31:8]	Reserved	0	

V_F_PORCH_CFG	[7:0]	This is used to specify the number of lines in vertical front porch part. When F_SEL is 1, this value is sent in main stream attribute packet. When BIST_EN is 1, this bit field is used to specify the BIST video stream format.	0
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Table 11-24 Vertical Sync Width Configure Register (V_SYNC_WIDTH_CFG)

Register	Address	Type	Description	Reset Value
V_SYNC_WIDTH_CFG	Base + 0x005C	R/W	Vertical Sync Width Configure Register	0x0000_0000

V_SYNC_WIDTH_CFG	Bit	Description	Initial State
-	[31:8]	Reserved	0
V_SYNC_WIDTH_CFG	[7:0]	This is used to specify the number of lines in VSYNC period. When F_SEL is 1, this value is sent in main stream attribute packet. When BIST_EN is 1, this bit field is used to specify the BIST video stream format.	0

Table 11-25 Vertical Back Porch Configure Register (V_B_PORCH_CFG)

Register	Address	Type	Description	Reset Value
V_B_PORCH_CFG	Base + 0x0060	R/W	Vertical Back Porch Configure Register	0x0000_0000

V_B_PORCH_CFG	Bit	Description	Initial State
-	[31:8]	Reserved	0
V_B_PORCH_CFG	[7:0]	This is used to specify the number of lines in frame back porch part. When F_SEL is 1, this value is sent in main stream attribute packet. When BIST_EN is 1, this bit field is used to specify the BIST video stream format.	0

Table 11-26 Total Pixel Low Byte Configure Register (TOTAL_PIXEL_CFG_L)

Register	Address	Type	Description	Reset Value
TOTAL_PIXEL_CFG_L	Base + 0x0064	R/W	Total Pixel Low Byte Configure Register	0x0000_0000

TOTAL_PIXEL_CFG_L	Bit	Description	Initial State
-	[31:8]	Reserved	0
TOTAL_PIXEL_CFG_L	[7:0]	TOTAL_PIXEL_CFG is used to specify the number of pixels in each line. This register is TOTAL_PIXEL_CFG[7:0]. When F_SEL is 1, this value is sent in main stream attribute packet. When BIST_EN is 1, this bit field is used to specify the BIST video stream format.	0

Table 11-27 Total Pixel High Byte Configure Register (TOTAL_PIXEL_CFG_H)

Register	Address	Type	Description	Reset Value
TOTAL_PIXEL_CFG_H	Base + 0x0068	R/W	Total Pixel High Byte Configure Register	0x0000_0000

TOTAL_PIXEL_CFG_H	Bit	Description	Initial State
-	[31:6]	Reserved	0
TOTAL_PIXEL_CFG_H	[5:0]	TOTAL_PIXEL_CFG is used to specify the number of pixels in each line. This register is TOTAL_PIXEL_CFG [13:8]. When F_SEL is 1, this value is sent in main stream attribute packet. When BIST_EN is 1, this bit field is used to specify the BIST video stream format.	0

Table 11-28 Active Pixel Low Byte Configure Register (ACTIVE_PIXEL_CFG_L)

Register	Address	Type	Description	Reset Value
ACTIVE_PIXEL_CFG_L	Base + 0x006C	R/W	Active Pixel Low Byte Configure Register	0x0000_0000

ACTIVE_PIXEL_CFG_L	Bit	Description	Initial State
-	[31:8]	Reserved	0

ACTIVE_PIXEL_CFG_L	[7:0]	ACTIVE_PIXEL_CFG is used to specify the number of active pixels in each line. This register is ACTIVE_PIXEL_CFG [7:0]. When F_SEL is 1, this value is sent in main stream attribute packet. When BIST_EN is 1, this bit field is used to specify the BIST video stream format.	0
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Table 11-29 Active Pixel High Byte Configure Register (ACTIVE_PIXEL_CFG_H)

Register	Address	Type	Description	Reset Value
ACTIVE_PIXEL_CFG_H	Base + 0x0070	R/W	Active Pixel High Byte Configure Register	0x0000_0000

ACTIVE_PIXEL_CFG_H	Bit	Description	Initial State
-	[31:6]	Reserved	0
ACTIVE_PIXEL_CFG_H	[5:0]	ACTIVE_PIXEL_CFG is used to specify the number of active pixels in each line. This register is ACTIVE_PIXEL_CFG [13:8]. When F_SEL is 1, this value is sent in main stream attribute packet. When BIST_EN is 1, this bit field is used to specify the BIST video stream format.	0

Table 11-30 Horizon Front Porch Low Byte Configure Register (H_F_PORCH_CFG_L)

Register	Address	Type	Description	Reset Value
H_F_PORCH_CFG_L	Base + 0x0074	R/W	Horizon Front Porch Low Byte Configure Register	0x0000_0000

H_F_PORCH_CFG_L	Bit	Description	Initial State
-	[31:8]	Reserved	0
H_F_PORCH_CFG_L	[7:0]	H_F_PORCH_CFG is used to specify the number of pixels in frame horizon front porch part. This register is H_F_PORCH_CFG[7:0] When F_SEL is 1, this value is sent in main stream attribute packet. When BIST_EN is 1, this bit field is used to specify the BIST video stream format.	0

Table 11-31 Horizon Front Porch High Byte Configure Register (H_F_PORCH_CFG_H)

Register	Address	Type	Description	Reset Value
H_F_PORCH_CFG_H	Base + 0x0078	R/W	Horizon Front Porch High Byte Configure Register	0x0000_0000

H_F_PORCH_CFG_H	Bit	Description	Initial State
-	[31:4]	Reserved	0
H_F_PORCH_CFG_H	[3:0]	H_F_PORCH_CFG is used to specify the number of pixels in frame horizon front porch part. This register is H_F_PORCH_CFG [11:8] When F_SEL is 1, this value is sent in main stream attribute packet. When BIST_EN is 1, this bit field is used to specify the BIST video stream format.	0

Table 11-32 Horizon Sync Width Low Byte Configure Register (H_SYNC_CFG_L)

Register	Address	Type	Description	Reset Value
H_SYNC_CFG_L	Base + 0x007C	R/W	Horizon Sync Width Low Byte Configure Register	0x0000_0000

H_SYNC_CFG_L	Bit	Description	Initial State
-	[31:8]	Reserved	0
H_SYNC_CFG_L	[7:0]	H_SYNC_CFG is used to specify the number of pixels in HSYNC period. This register is H_SYNC_CFG [7:0]. When F_SEL is 1, this value is sent in main stream attribute packet. When BIST_EN is 1, this bit field is used to specify the BIST video stream format.	0

Table 11-33 Horizon Sync Width High Byte Configure Register (H_SYNC_CFG_H)

Register	Address	Type	Description	Reset Value
H_SYNC_CFG_H	Base + 0x0080	R/W	Horizon Sync Width High Byte Configure Register	0x0000_0000

H_SYNC_CFG_H	Bit	Description	Initial State
-	[31:4]	Reserved	0
H_SYNC_CFG_H	[3:0]	H_SYNC_CFG is used to specify the number of pixels in HSYNC period. This register is H_SYNC_CFG [11:8]. When F_SEL is 1, this value is sent in main stream attribute packet. When BIST_EN is 1, this bit field is used to specify the BIST video stream format.	0

Table 11-34 Horizon Back Porch Low Byte Configure Register (H_B_PORCH_CFG_L)

Register	Address	Type	Description	Reset Value
H_B_PORCH_CFG_L	Base + 0x0084	R/W	Horizon Back Porch Low Byte Configure Register	0x0000_0000

H_B_PORCH_CFG_L	Bit	Description	Initial State
-	[31:8]	Reserved	0
H_B_PORCH_CFG_L	[7:0]	H_B_PORCH_CFG is used to specify the number of pixel in frame horizon back porch part. This register is H_B_PORCH_CFG [7:0]. When F_SEL is 1, this value is sent in main stream attribute packet. When BIST_EN is 1, this bit field is used to specify the BIST video stream format.	0

Table 11-35 Horizon Back Porch High Byte Configure Register (H_B_PORCH_CFG_H)

Register	Address	Type	Description	Reset Value
H_B_PORCH_CFG_H	0x0000_0088	R/W	Horizon Back Porch High Byte Configure Register	0x0000_0000

H_B_PORCH_CFG_H	Bit	Description	Initial State
-	[31:4]	Reserved	0

H_B_PORCH_CFG_H	[3:0]	H_B_PORCH_CFG is used to specify the number of pixel in frame horizon back porch part. This register is H_B_PORCH_CFG [11:8]. When F_SEL is 1, this value is sent in main stream attribute packet. When BIST_EN is 1, this bit field is used to specify the BIST video stream format.	0
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Table 11-36 Video Status Register (VIDEO_STATUS)

Register	Address	Type	Description	Reset Value
VIDEO_STATUS	Base + 0x008C	RO	Input Video Status Register	0x0000_0003

VIDEO_STATUS	Bit	Description	Initial State
-	[31:4]	Reserved	0
FIELD_S	[3]	Interlace scan field status. 1: Second field, 0: First field. This bit field is valid only when STRM_VALID is high. And STRM_VALID becomes high when two successive frames are determined as stable.	0
I_SCAN_S	[2]	Auto-detect interlace or progressive scan status: 1: Interlace scan, 0: Progressive scan. This bit field is valid only when STRM_VALID is high. And STRM_VALID becomes high when two successive frames are determined as stable.	0
VSYNC_P_S	[1]	Auto-detect VSYNC polarity: 1: Low is active, 0: High is active. This bit field is valid only when STRM_VALID is high. And STRM_VALID becomes high when two successive frames are determined as stable.	1
HSYNC_P_S	[0]	Auto-detect HSYNC polarity: 1: Low is active, 0: High is active. This bit field is valid only when STRM_VALID is high. And STRM_VALID becomes high when two successive frames are determined as stable.	1

Table 11-37 Total Line Status Low Byte Register (TOTAL_LINE_STA_L)

Register	Address	Type	Description	Reset Value
TOTAL_LINE_STA_L	Base + 0x0090	RO	Total Line Status Low Byte Register	0x0000_0001

TOTAL_LINE_STA_L	Bit	Description	Initial State
-	[31:8]	Reserved	0
TOTAL_LINE_STA_L	[7:0]	TOTAL_LINE [7:0] which is detected by video capture module. This bit field is valid only when STRM_VALID is high. And STRM_VALID becomes high when two successive frames are determined as stable.	1

Table 11-38 Total Line Status High Byte Register (TOTAL_LINE_STA_H)

Register	Address	Type	Description	Reset Value
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TOTAL_LINE_STA_H	Base + 0x0094	RO	Total Line Status High Byte Register	0x0000_0000
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TOTAL_LINE_STA_H	Bit	Description	Initial State
-	[31:5]	Reserved	0
TOTAL_LINE_STA_H	[4:0]	TOTAL_LINE [11:8] which is detected by video capture module. This bit field is valid only when STRM_VALID is high. And STRM_VALID becomes high when two successive frames are determined as stable.	0

Table 11-39 Active Line Status Low Byte Register (ACTIVE_LINE_STA_L)

Register	Address	Type	Description	Reset Value
ACTIVE_LINE_STA_L	Base + 0x0098	RO	Active Line Status Low Byte Register	0x0000_0000

ACTIVE_LINE_STA_L	Bit	Description	Initial State
-	[31:8]	Reserved	0
ACTIVE_LINE_STA_L	[7:0]	ACTIVE_LINE [7:0] which is detected by video capture module. This bit field is valid only when STRM_VALID is high. And STRM_VALID becomes high when two successive frames are determined as stable.	0

Table 11-40 Active Line Status High Byte Register (ACTIVE_LINE_STA_H)

Register	Address	Type	Description	Reset Value
ACTIVE_LINE_STA_H	Base + 0x009C	RO	Active Line Status High Byte Register	0x0000_0000

ACTIVE_LINE_STA_H	Bit	Description	Initial State
-	[31:5]	Reserved	0
ACTIVE_LINE_STA_H	[4:0]	ACTIVE_LINE [11:8] which is detected by video capture module. This bit field is valid only when STRM_VALID is high. And STRM_VALID becomes high when two successive frames are determined as stable.	0

Table 11-41 Vertical Front Porch Status Register (V_F_PORCH_STA)

Register	Address	Type	Description	Reset Value
V_F_PORCH_STA	Base + 0x00A0	RO	Vertical Front Porch Status Register	0x0000_0001

V_F_PORCH_STA	Bit	Description	Initial State
-	[31:8]	Reserved	0
V_F_PORCH_STA	[7:0]	V_F_PORCH (vertical front porch) which is detected by video capture module. This bit field is valid only when STRM_VALID is high. And STRM_VALID becomes high when two successive frames are determined as stable.	1

Table 5-42 Vertical Sync Width Status Register (V_SYNC_STA)

Register	Address	Type	Description	Reset Value
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V_SYNC_STA	Base + 0x00A4	RO	Vertical Sync Width Status Register	0x0000_0000
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V_SYNC_STA	Bit	Description	Initial State
-	[31:8]	Reserved	0
V_SYNC_STA	[7:0]	V_SYNC_WIDTH (vertical sync width) which is detected by video capture module. This bit field is valid only when STRM_VALID is high. And STRM_VALID becomes high when two successive frames are determined as stable.	0

Table 11-43 Vertical Back Porch Status Register (V_B_PORCH_STA)

Register	Address	Type	Description	Reset Value
V_B_PORCH_STA	Base + 0x00A8	RO	Vertical Back Porch Status Register	0x0000_0000

V_B_PORCH_STA	Bit	Description	Initial State
-	[31:8]	Reserved	0
V_B_PORCH_STA	[7:0]	V_B_PORCH (vertical back porch) which is detected by video capture module. This bit field is valid only when STRM_VALID is high. And STRM_VALID becomes high when two successive frames are determined as stable.	0

Table 11-44 Total Pixel Status Low Byte Register (TOTAL_PIXEL_STA_L)

Register	Address	Type	Description	Reset Value
TOTAL_PIXEL_STA_L	Base + 0x00Ac	RO	Total Pixel Status Low Byte Register	0x0000_0000

TOTAL_PIXEL_STA_L	Bit	Description	Initial State
-	[31:8]	Reserved	0
TOTAL_PIXEL_STA_L	[7:0]	TOTAL_PIXEL [7:0] which is detected by video capture module. This bit field is valid only when STRM_VALID is high. And STRM_VALID becomes high when two successive frames are determined as stable.	0

Table 11-45 Total Pixel Status High Byte Register (TOTAL_PIXEL_STA_H)

Register	Address	Type	Description	Reset Value
TOTAL_PIXEL_STA_H	Base + 0x00B0	RO	Total Pixel Status High Byte Register	0x0000_0000

TOTAL_PIXEL_STA_H	Bit	Description	Initial State
-	[31:6]	Reserved	0
TOTAL_PIXEL_STA_H	[5:0]	TOTAL_PIXEL [13:8] which is detected by video capture module. This bit field is valid only when STRM_VALID is high. And STRM_VALID becomes high when two successive frames are determined as stable.	0

Table 11-46 Active Pixel Status Low Byte Register (ACTIVE_PIXEL_STA_L)

Register	Address	Type	Description	Reset Value
ACTIVE_PIXEL_STA_L	Base + 0x00B4	RO	Active Pixel Status Low Byte Register	0x0000_0000

ACTIVE_PIXEL_STA_L	Bit	Description	Initial State
-	[31:8]	Reserved	0
ACTIVE_PIXEL_STA_L	[7:0]	ACTIVE_PIXEL [7:0] which is detected by video capture module. This bit field is valid only when STRM_VALID is high. And STRM_VALID becomes high when two successive frames are determined as stable.	0

Table 11-47 Active Pixel Status High Byte Register (ACTIVE_PIXEL_STA_H)

Register	Address	Type	Description	Reset Value
ACTIVE_PIXEL_STA_H	Base + 0x00B8	RO	Active Pixel Status High Byte Register	0x0000_0000

ACTIVE_PIXEL_STA_H	Bit	Description	Initial State
-	[31:6]	Reserved	0
ACTIVE_PIXEL_STA_H	[5:0]	ACTIVE_PIXEL [13:8] which is detected by video capture module. This bit field is valid only when STRM_VALID is high. And STRM_VALID becomes high when two successive frames are determined as stable.	0

Table 11-48 Horizon Front Porch Status Low Byte Register (H_F_PORCH_STA_L)

Register	Address	Type	Description	Reset Value
H_F_PORCH_STA_L	Base + 0x00BC	RO	Horizon Front Porch Status Low Byte Register	0x0000_0000

H_F_PORCH_STA_L	Bit	Description	Initial State
-	[31:8]	Reserved	0
H_F_PORCH_STA_L	[7:0]	H_F_PORCH [7:0] (horizon front porch) which is detected by video capture module. This bit field is valid only when STRM_VALID is high. And STRM_VALID becomes high when two successive frames are determined as stable.	0

Table 11-49 Horizon Front Porch Status High Byte Register (H_F_PORCH_STA_H)

Register	Address	Type	Description	Reset Value
H_F_PORCH_STA_H	Base + 0x00C0	RO	Horizon Front Porch Status High Byte Register	0x0000_0000

H_F_PORCH_STA_H	Bit	Description	Initial State
-	[31:4]	Reserved	0
H_F_PORCH_STA_H	[3:0]	H_F_PORCH [11:8] (horizon front porch) which is detected by video capture module. This bit field is valid only when STRM_VALID is high. And STRM_VALID becomes high when two successive frames are determined as stable.	0

Table 11-50 Horizon Sync Width Status Low Byte Register (H_SYNC_STA_L)

Register	Address	Type	Description	Reset Value

H_SYNC_STA_L	Base + 0x00C4	RO	Horizon Sync Width Status Low Byte Register	0x0000_0000
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H_SYNC_STA_L	Bit	Description	Initial State
-	[31:8]	Reserved	0
H_SYNC_STA_L	[7:0]	H_SYNC [7:0] (horizon sync width) which is detected by video capture module. This bit field is valid only when STRM_VALID is high. And STRM_VALID becomes high when two successive frames are determined as stable.	0

Table 11-51 Horizon Sync Width Status High Byte Register (H_SYNC_STA_H)

Register	Address	Type	Description	Reset Value
H_SYNC_STA_H	Base + 0x00C8	RO	Horizon Sync Width Status High Byte Register	0x0000_0000

H_SYNC_STA_H	Bit	Description	Initial State
-	[31:4]	Reserved	0
H_SYNC_STA_H	[3:0]	H_SYNC [11:8] (horizon sync width) which is detected by video capture module. This bit field is valid only when STRM_VALID is high. And STRM_VALID becomes high when two successive frames are determined as stable.	0

Table 11-52 Horizon Back Porch Status Low Byte Register (H_B_PORCH_STA_L)

Register	Address	Type	Description	Reset Value
H_B_PORCH_STA_L	Base + 0x00CC	RO	Horizon Back Porch Status Low Byte Register	0x0000_0000

H_B_PORCH_STA_L	Bit	Description	Initial State
-	[31:8]	Reserved	0
H_B_PORCH_STA_L	[7:0]	H_B_PORCH [7:0] (horizon back porch) which is detected by video capture module. This bit field is valid only when STRM_VALID is high. And STRM_VALID becomes high when two successive frames are determined as stable.	0

Table 11-53 Horizon Back Porch Status High Byte Register (H_B_PORCH_STA_H)

Register	Address	Type	Description	Reset Value
H_B_PORCH_STA_H	Base + 0x00D0	RO	Horizon Back Porch Status High Byte Register	0x0000_0000

H_B_PORCH_STA_H	Bit	Description	Initial State
-	[31:4]	Reserved	0
H_B_PORCH_STA_H	[3:0]	H_B_PORCH [11:8] (horizon back porch) which is detected by video capture module. This bit field is valid only when STRM_VALID is high. And STRM_VALID becomes high when two successive frames are determined as stable.	0

Table 11-54 SPDIF Audio Control Register 0 (SPDIF_AUDIO_CTL_0)

Register	Address	Type	Description	Reset Value
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SPDIF_AUDIO_CTL_0	Base + 0x00D8	R/W	SPDIF Audio Control Register 0	0x0000_0000
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SPDIF_AUDIO_CTL_0	Bit	Description	Initial State
-	[31:8]	Reserved	0
AUD_SPDIF_EN	[7]	Set SPDIF audio stream input enable. 0: Disable, 1: Enable.	0
-	[6:4]	Reserved	0
REUSE_SPD_EN	[3]	Reuse spd inforframe registers.	0
FORCE_SPDIF_DET	[2]	Force SPDIF_STREAM_DET, which is SPDIF detect status, to 1. (Test purpose only) 1: Force SPDIF_STREAM_DET to 1, 0: SPDIF_STREAM_DET is set by hardware detector.	0
SPDIF_PARITY_CTRL	[1]	Control the SPDIF parity generation scheme. In the IEC-60958, audio packet is 28-bit. But in the DP standard v1.1, the audio packet is 32-bit, 4 more control bits have been added. The control bit selects the parity scheme of original 28 bit defined in IEC-60958 or parity scheme of 32 bit defined in DP standard v1.1. 1: Parity of DP link audio sample 32 bit, 0: Parity of SPDIF audio sample 28 bit.	0
SPDIF_CLK_DET_RESET_BYPASS	[0]	Bypass SPDIF clock detect auto reset: 1: Bypass SPDIF clock detect auto reset, SPDIF module will not be reset even SPDIF clock is not detected. 0: If SPDIF clock is not detected, SPDIF module is reset automatically.	0

Table 11-55 DP Audio Control Register 1 (DP_AUDIO_CTL_1)

Register	Address	Type	Description	Reset Value
DP_AUDIO_CTL_1	Base + 0x00DC	R/W	DP Audio Control Register 1	0x0000_0000

DP_AUDIO_CTL_1	Bit	Description	Initial State
-	[31:6]	Reserved	0
AUD_MUTE_EN4	[5]	Audio data auto mute control enable for audio FIFO under run interrupt. 1: Enable 0: Disable.	0
AUD_MUTE_EN3	[4]	Audio data auto mute control enable for audio FIFO overrun interrupt. 1: Enable 0: Disable.	0
AUD_MUTE_EN2	[3]	Audio data auto mute control enable for HDCP failed interrupt. 1: Enable 0: Disable.	0
AUD_MUTE_EN1	[2]	Audio data auto mute control enable for SPDIF unstable interrupt. 1: Enable 0: Disable.	0
AUD_MUTE_EN0	[1]	Audio data auto mute control enable for Audio clock change interrupt. 1: Enable 0: Disable.	0
-	[0]	Reserved	0

Table 11-56 SPDIF Audio Status Register 0 (SPDIF_AUDIO_STA_0)

Register	Address	Type	Description	Reset Value
SPDIF_AUDIO_STA_0	Base + 0x00E0	RO	SPDIF Audio Status Register 0	0x0000_0000

SPDIF_AUDIO_STA_0	Bit	Description	Initial State
-	[31:8]	Reserved	0
SPDIF_CLK_DET	[7]	SPDIF audio clock detected flag. 1: Clock detected 0: Clock not detected.	0

SPDIF_AUDIO_STA_0	Bit	Description	Initial State
-	[6:1]	Reserved	0
SPDIF_STREAM_DET	[0]	SPDIF audio stream detected flag. 1: Input detected 0: No input detected.	0

Table 11-57 Audio SPDIF Status Register 1 (SPDIF_AUDIO_STA_1)

Register	Address	Type	Description	Reset Value
SPDIF_AUDIO_STA_1	Base + 0x00E4	RO	Audio SPDIF Status Register 1	0x0000_0000

SPDIF_AUDIO_STA_1	Bit	Description	Initial State
-	[31:8]	Reserved	0
SPDIF_FS_FREQ	[7:4]	Sampling clock frequency (corresponding to channel status bits [27:24]). 0000: 44.1 KHz, 0010: 48 KHz, 0011: 32 KHz, 1000: 88.2 KHz, 1010: 96 KHz, 1110: 192 KHz, Others: Reserved. SPDIF_FS_FREQ can be read when SPDIF_STREAM_DET and VSYNC_DET are high.	0
SPDIF_WORD_LEN	[3:0]	Audio word length (corresponding to channel status bits [35:32]). 0010: 16 bits, 0011: 20 bits, 0100: 18 bits, 0101: 22 bits, 1000: 19 bits, 1001: 23 bits, 1010: 20 bits, 1011: 24 bits, 1100: 17 bits, 1101: 21 bits. SPDIF_WORD_LEN can be read when SPDIF_STREAM_DET and VSYNC_SET are high.	0

Table 11-58 SPDIF Error Threshold Register (SPDIF_ERR_THRD)

Register	Address	Type	Description	Reset Value
SPDIF_ERR_THRD	Base + 0x00E8	R/W	SPDIF Error Threshold Register	0x0000_0001

SPDIF_ERR_THRD	Bit	Description	Initial State
-	[31:8]	Reserved	0
SPDIF_ERR_THRD	[7:0]	SPDIF parity error threshold for the SPDIF_ERR interrupt. When SPDIF stream data parity error occurs, the SPDIF_ERR_CNT will increase by 1. And when SPDIF_ERR_CNT equals to SPDIF_ERR_THRD, SPDIF_ERR interrupt happens.	1

Table 11-59 SPDIF Error Counter Register (SPDIF_ERR_CNT)

Register	Address	Type	Description	Reset Value
SPDIF_ERR_CNT	Base + 0x00EC	RO SC	SPDIF Error Counter Register	0x0000_0000

SPDIF_ERR_CNT	Bit	Description	Initial State
-	[31:8]	Reserved	0

SPDIF_ERR_CNT	[7:0]	SPDIF parity errors counter. Write any value to clear.	0
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Table 11-60 Audio BIST Control Register (AUDIO_BIST_CTL)

Register	Address	Type	Description	Reset Value
AUDIO_BIST_CTL	Base + 0x00F0	R/W	Audio BIST Control Register	0x0000_0000

AUDIO_BIST_CTL	Bit	Description	Initial State
-	[31:8]	Reserved	0
SIN_AMPL	[7:4]	Set the Sin wave amplitude for audio BIST data. 0000: ± 255, 0001: ± 510, 0010: ± 1020, 0011: ± 2040, 0100: ± 4080, 0101: ± 8160, 0110: ± 16320, 0111: ± 32640, 1000: ± 65280, 1001: ± 130560, 1010: ± 261120, 1011: ± 522240, 1100: ± 1044480, 1101: ± 2088960, 1110: ± 4177920, 1111: ± 8355840	0
-	[3:1]	Reserved	0
AUD_BIST_EN	[0]	Audio BIST enable. 1: Enable 0: Disable.	0

Table 11-61 Audio Input Clock Frequency Counter Register_1(AUD_FREQ_CNT_1)

Register	Address	Type	Description	Reset Value
AUD_FREQ_CNT_1	Base + 0x00F4	RO	Audio Input Clock Frequency Counter Register 1	0x0000_0000

AUD_FREQ_CNT_1	Bit	Description	Initial State
-	[31:8]	Reserved	0
AUD_FREQ_CNT_L	[7:0]	Audio input clock frequency counter register. For test purpose only.	0

Table 11-62 Audio Input Clock Frequency Counter Register_2(AUD_FREQ_CNT_2)

Register	Address	Type	Description	Reset Value
AUD_FREQ_CNT_2	Base + 0x00F8	RO	Audio Input Clock Frequency Counter Register 2	0x0000_0000

AUD_FREQ_CNT_2	Bit	Description	Initial State
-	[31:4]	Reserved	0
AUD_FREQ_CNT_H	[3:0]	Audio input clock frequency counter register. For test purpose only.	0

Table 11-63 PLL control Register_1(PLL_REG_1)

Register	Address	Type	Description	Reset Value
PLL_REG_1	Base + 0x00FC	R/W	PLL control 1	0x0000_0011

PLL_REG_1	Bit	Description	Initial State
-	[31:6]	Reserved	0
LINK_SPEED(RO)	[5:4]	FVCO: 00:1.62G 01:2.7G 1x:Reserved	1
-	[3:1]	Reserved	0
PLL_REF_CLK_FREQ	[0]	reference CLOCK frequency: 1(default):24MHz 0:27MHz	0

Table 11-64 PLL control Register_2(PLL_REG_2)

Register	Address	Type	Description	Reset Value
PLL_REG_2	Base + 0x09E4	R/W	Pll_control_2	0x0000_0011

PLL_REG_2	Bit	Description	Initial State
-	[31:8]	Reserved	0
LDO_OUTPUT_V_SEL	[7:6]	1.5v LDO output voltage select 00:1.35v 01:1.40v 10:1.45v(default) 11:1.50v	2'b10
KVCO	[5:4]	KVCO to control VCO band 00: decrease KVCO by 15% 01:(default) 10:increase KVCO by 10% 11:increase KVCO by 20%	2'b01
CHG_PUMP_CURRENT_SEL	[3:2]	charge pump current select 00:2.5u 01(default):5u 10:7.5u 11:10u	2'b01
V2I_CURRENT_SEL	[1:0]	v2i current select 00: no adding current 01: adding 1mA current(default) 10: adding 2mA current 11: adding 4.5mA current	2'b01

Table 11-65 PLL control Register_3(PLL_REG_3)

Register	Address	Type	Description	Reset Value
PLL_REG_3	Base + 0x09E8	R/W	Pll_control_3	0x0000_002B

PLL_REG_3	Bit	Description	Initial State
-	[31:7]	Reserved	0
LOCK_DET_CNT_SEL	[6:5]	lock detector output counter select, counter period is twice of reference clock 00: 64 cycle 01: 128 cycle 10: 256 cycle (default) 11: 512 cycle	2'b10
LOOP_FILTER_RESET_SEL	[4]	loop filter control voltage reset select 1: reset to the value below DVDD 0: reset to DVDD (default)	0

PLL_REG_3	Bit	Description	Initial State
PALL_SSC_RESET	[3]	PLL and ssc reset control 1: reset 0: normal	0
LOCK_DET_BYPASS	[2]	lock detector bypass select 0: not bypass (default) 1: bypass lock detector in ssc	0
PLL_LOCK_DET_MODE	[1]	PLL lock detector mode select 0: fractional N (default) 1: integer N	0
PLL_LOCK_DET_FORCE	[0]	force PLL lock detector lock 0: not force lock (default) 1: force PLL lock	0

Table 11-66 PLL control Register_4(PLL_REG_4)

Register	Address	Type	Description	Reset Value
PLL_REG_4	Base + 0x09EC	R/W	PLL_control_4	0x0000_0023

PLL_REG_4	Bit	Description	Initial State
-	[31:8]	Reserved	0
-	[7:0]	Reserved	0

Table 5-67 PLL control Register_5(PLL_REG_5)

Register	Address	Type	Description	Reset Value
PLL_REG_5	Base + 0x0A00	R/W	PLL_control_5	0x0000_0000

PLL_REG_5	Bit	Description	Initial State
-	[31:7]	Reserved	0
REGULATOR_V_SEL	[6:4]	slave regulator output voltage select 000900V 0010.925V 0100.950V(default) 0110.975V 1001.000V 1011.025V 1101.050V	3'b010
STANDBY_CURRENT_SEL	[3]	slave standby current select 1: adding 200uA standby current 0: keep 300uA standby current (default)	0
CHG_PUMP_INPUT_CTRL	[2:1]	control charge pump input voltage for 0.95V master regulator 00: 1.1V 01: 1.2V(default) 10: 1.3V 11: 1.4V	2'b01
CHG_PUMP_INPUT_CTRL_OP	[0]	option to control charge pump input voltage for 0.95V master regulator 0: set by pll_reg5<2:1>(default) 1: 1.8V	0

Table 11-68 PLL control Register_mac(PLL_REG_mac)

Register	Address	Type	Description	Reset Value
PLL_REG_MAC	Base + 0x0A04	R/W	PLL_control_mac	0x0000_0000

PLL_REG_MAC	Bit	Description	Initial State
-	[31:8]	Reserved	0
ANALOG_BACKUP1	[7:0]	Reserved	0

Table 11-69 Freq Register (FREQ_IN_REG)

Register	Address	Type	Description	Reset Value
FREQ_IN_REG	Base + 0x0A10	R/W	frequency set from register for freq counter	0x0000_0080

FREQ_IN_REG	Bit	Description	Initial State
-	[31:8]	Reserved	0
FREQ_REG	[7:0]	frequency set from register for freq counter	80

Table 11-70 Freq Register (P_REG_FRQ)

Register	Address	Type	Description	Reset Value
P_REG_FRQ	Base + 0x0A14	RO	digital output for debug	0x0000_0000

P_REG_FRQ	Bit	Description	Initial State
-	[31:8]	Reserved	0
FRQ	[7:0]	digital output for debug, controlled by pll_reg1<7> and pll_reg4<4> when pll_reg1<7>=0 & pll_reg4<4>=0: half video clock frequency calculated by frequency counter When pll_reg1<7>=0 & pll_reg4<4>=1: half video clock frequency calculated frq_vid_ck_in<8:0> when pll_reg1<7>=1: frq<1:0>: <n_over, n_under> frq<3:2>: band<1:0> frq<7:4>: 0	00

Table 11-71 Freq Register (P_REG_FRQ_COUNT_RDY)

Register	Address	Type	Description	Reset Value
P_REG_FRQ_COUNT_RDY	Base + 0x0A18	RO	frequency counter ready indicator (frequency counter for VCO band selection)	0x0000_0000

P_REG_FRQ_COUNT_RDY	Bit	Description	Initial State
-	[31:1]	Reserved	0
FRQ_COUNT_RDY	[0]	frequency counter ready indicator (frequency counter for VCO band selection) 1: frequency counter ready, its output is the real value of video PLL 0: frequency counter not ready, its output is not the real value	0

Table 11-72 Freq Register (P_BAND_DEC_RESET)

Register	Address	Type	Description	Reset Value
P_BAND_DEC_RESET	Base + 0x0A1C	WO	band decoder reset	0x0000_0000

P_BAND_DEC_RESET	Bit	Description	Initial State
-	[31:1]	Reserved	0
R_BAND_DEC_RESET	[0]	1: reset band decoder 0: band decoder works	0

Table 11-73 SSC control Register_2(SSC_REG)

Register	Address	Type	Description	Reset Value
SSC_REG	Base + 0x0104	R/W	SSC control	0x0000_000A

SSC_REG	Bit	Description	Initial State
-	[31:8]	Reserved	0
SSC_OFFSET	[7:6]	00: no 01: up 100ppm 10: down 100ppm 11: down 200ppm	0
SSC_MODE	[5:4]	00:disable 01:down spread 10:center spread 11:up spread	2'b01
SSC_DEPTH	[3:0]	0000:disable 0001:500ppm 0010:1000ppm 0011:1500ppm 0100:2000ppm 0101:2500ppm 0110:3000ppm 0111:3500ppm 1000:4000ppm 1001:4500ppm 1010:5000ppm 1011:5500ppm 1100-1111:6000ppm	4'h9

Table 11-74 TX_COMMON Register (TX_COMMON)

Register	Address	Type	Description	Reset Value
TX_REG_COMMON	Base + 0x0114	R/W	TX COMMON 1 register	0x0000_003A

TX_COMMON	Bit	Description	Initial State
-	[31:8]	Reserved	0
TX_SWING_PRE_EMP_MODE_SEL	[7]	TX swing and pre emphasis control mode selection 1: TX swing and pre emphasis control by register dp_reserv2<7:0> 0: TX swing and pre emphasis control by register chx_reg_swing<7:0> and chx_reg_pre<7:0>	1

PRE_DRIVER_PW_CTRL1	[6:5]	Pre-driver extra power control 0: disable 1: enable	0
LP_MODE_CLK_REGULATOR	[4]	Low power mode control for clock regulator 0:low power mode 1:high power mode	0
RESISTOR_MSB_CTRL	[3]	TX terminal resistor MSB control	0
RESISTOR_CTRL	[2:0]	TX terminal resistor control when tx_common<3>=0 000: 58.54 011:54.6 111:50 when tx_common<6>=1 000: 49 011:46 111:42.6	3'h7

Table 11-75 TX_COMMON2 Register (TX_COMMON2)

Register	Address	Type	Description	Reset Value
TX_COMMON2	Base + 0x0118	R/W	TX_COMMON2	0x0000_0050

TX_COMMON2	Bit	Description	Initial State
-	[31:8]	Reserved	0
TX_OUTPUT_PN_INVERSE_CH3	[7]	TX ch3 output p-n inverse control: 0: not inverse 1: output p and n inverse	0
TX_OUTPUT_PN_INVERSE_CH2	[6]	TX ch2 output p-n inverse control: 0: not inverse 1: output p and n inverse	1
TX_OUTPUT_PN_INVERSE_CH1	[5]	TX ch1 output p-n inverse control: 0: not inverse 1: output p and n inverse	0
TX_OUTPUT_PN_INVERSE_CH0	[4]	TX ch0 output p-n inverse control: 0: not inverse 1: output p and n inverse	1
TX_OUT_PATTERN_EN	[3]	TX output pattern enable 0: normal TX 1: dedicate pattern	0
TX_DATA_PATTEN	[2:0]	TX data Patten 000:all zero 001:all one 010:D10.2 011:1100 100:K28.5 101:K28.7 110:1111100000 111:111111111000000000	0

Table 11-76 TX_COMMON3 Register (TX_COMMON3)

Register	Address	Type	Description	Reset Value
TX_COMMON3	Base + 0x0A08	R/W	TX_COMMON3	0x0000_0000

TX_COMMON3	Bit	Description	Initial State
-	[31:8]	Reserved	0
CLK_DLY_SEL	[7:3]	Select /20 clock delay (clk_div2_ssc & tx_txd_clk) 00000 : delay=150ps 00001 : delay=150ps+1*70ps 00010 : delay=150ps+2*70ps 00011: delay=150ps+3*70ps	0
CLK_INVERSE_EN	[2]	TX input clock inverse enable 0: normal 1: TX input clock inverse	0
SCAN_CLK_SEL	[1]	ch0 select i_ref_clk_24m for scan 0:select tx_bscan_data<0> 1:select i_ref_clk_24m	0
-	[0]	Reserved	0

Table 11-77 DP_AUX Register (DP_AUX)

Register	Address	Type	Description	Reset Value
DP_AUX	Base + 0x0120	R/W	Aux control	0x0000_0007

DP_AUX	Bit	Description	Initial State
-	[31:5]	Reserved	0
DP_AUX_COMMON_MODE	[4]	AUX RX CM voltage control 0: AUX CH use VCC1/2 as CM voltage (have static current consumption) 1: use VCC1 as CM voltage	0
DP_AUX_EN(R/O)	[3]	AUX TX enable 0: AUX CH configured as RX 1: AUX CH configured as TX	0
-	[2]	Reserved	0
AUX_TERM	[1:0]	AUX CH impedance control bits: only control TX impedance 00 : 500ohm 01 : 250ohm 10 : 100ohm 11 : 50ohm	3

Table 11-78 DP_BIAS Register (DP_BIAS)

Register	Address	Type	Description	Reset Value
DP_BIAS	Base + 0x0124	R/W	BIAS control	0x0000_0034

DP_BIAS	Bit	Description	Initial State
-	[31:7]	Reserved	0
DP_BG_OUT_SEL	[6:4]	Select band gap out 000:0.56V 100:0.6V(default) 111:0.63V	4
DP_DB_CUREENT_CTRL	[3]	Band gap start up current control 0: balance 1: unbalance	0
DP_BG_SEL	[2]	Select band gap 0:sel Register 1:sel Band gap	1

DP_RESISTOR_TUNE_BG_CTRL	[1:0]	Resistor tune for band gap TC control 00 : 25uV/°C 01: 10uV/°C 10: -10uV/°C 11: -25uV/°C	0
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Table 11-79 DP_TEST Register (DP_TEST)

Register	Address	Type	Description	Reset Value
DP_TEST	Base + 0x0128	R/W	TEST	0x0000_0000

DP_TEST	Bit	Description	Initial State
-	[31:8]	Reserved	0
DP_TEST_MODE	[7:6]	00&01: test disables dc_tp/atesto/dtesto output hiz. 10: atesto test enable 11: dtesto test enable	0
	[5:3]	When <7:6> ==10, test analog blocks: 000-- disable analog test 001: enable ch0 analog test mux <1:0>(00/01/10/11)--->(avdd10_pre_drv,avdd10_p2s, vddu_p2s,avss) 010: enable ch1 analog test mux <1:0>(00/01/10/11)--->(avdd10_pre_drv,avdd10_p2s, vddu_p2s,avss) 011: enable ch2 analog test mux <1:0>(00/01/10/11)--->(avdd10_pre_drv,avdd10_p2s, vddu_p2s,avss) 100: enable ch3 analog test mux <1:0>(00/01/10/11)--->(avdd10_pre_drv,avdd10_p2s, vddu_p2s,avss) 101: enable pll analog test mux <1:0>(00/01/10/11)--->(vdd10_cln,v1p45_v2i, avdd18,vco_ctrl) 110: enable charge pump regulator analog test mux <1:0> (00/01/10/11)---->(v1v_regu, vregu_out,v0.5_ref,null) 111: test band gap output When <7:6>==11, test digital blocks: 000-- disable digital test 001: enable pll digital test mux <1:0>--(00/01/10/11)--->pll_ref,vco_fb, vss,vss. 010: test charge pump regulator OSC clock.	0
-	[2:0]	Reserved	0

Table 11-80 DP_PD Register (DP_PD)

Register	Address	Type	Description	Reset Value
DP_PD	Base + 0x012C	R/W	Power down. Power down sequence: dp_pd=ff => dp_pd=7f => wait 10us => dp_pd=00	0x0000_00FF

DP_PD	Bit	Description	Initial State
-	[31:8]	Reserved	0
PD_INC_BG	[7]	Power down all including band gap	1
PD_EXP_BG	[6]	Power down all except band gap	1
PD_AUX_CH	[5]	Power down AUX channel	1

DP_PD	Bit	Description	Initial State
PD_PLL	[4]	Power down PLL	1
PD_CH3	[3]	Power down ch3	1
PD_CH2	[2]	Power down ch2	1
PD_CH1	[1]	Power down ch1	1
PD_CH0	[0]	Power down ch0	1

Table 11-81 DP_RESERV1 Register (DP_RESERV1)

Register	Address	Type	Description	Reset Value
RESERVE1	Base + 0x0130	R/W	ATE Test enable	0x0000_0000

DP_RESERV1	Bit	Description	Initial State
-	[31:4]	Reserved	0
SSC_MODE_LOCK	[7]	SSC mode lock	0
-	[6]	Reserved	0
PRE_DRIVER_PW_CTRL2	[5:4]	Pre-driver extra power control 0: disable 1:enable	0
ATE_EN_CH3	[3]	Set 1 to enable CH3 ATE test	0
ATE_EN_CH2	[2]	Set 1 to enable CH2 ATE test	0
ATE_EN_CH1	[1]	Set 1 to enable CH1 ATE test	0
ATE_EN_CH0	[0]	Set 1 to enable CH0 ATE test	0

Table 11-82 DP_RESERV2 Register (DP_RESERV2)

Register	Address	Type	Description	Reset Value
DP_RESERV2	Base + 0x0134	R/W	RESERVED	0x0000_0000

DP_RESERV2	Bit	Description	Initial State
-	[31:8]	Reserved	0
CH1_CH3_SWING_EMP_CTRL	[7:4]	ch1,3 swing and pre emphasis control for firmware when tx_common<7>=1 0000 : swing0 pre emphasis 0 dB 0001 : swing1 pre emphasis 0 dB 0010 : swing2 pre emphasis 0 dB 0011 : swing3 pre emphasis 0 dB 0100 : swing0 pre emphasis 3.5 dB 0101 : swing1 pre emphasis 3.5 dB 0110 : swing2 pre emphasis 3.5 dB 1000 : swing0 pre emphasis 6 dB 1001 : swing1 pre emphasis 6 dB 1100 : swing0 pre emphasis 9.5 dB others : swing0 pre emphasis 9.5 dB	5

DP_RESERV2	Bit	Description	Initial State
CH0_CH2_SWING_EMP_CTRL	[3:0]	ch0,2 swing and pre emphasis control for firmware when tx_common<7>=1 0000 : swing0 pre emphasis 0 dB 0001 : swing1 pre emphasis 0 dB 0010 : swing2 pre emphasis 0 dB 0011 : swing3 pre emphasis 0 dB 0100 : swing0 pre emphasis 3.5 dB 0101 : swing1 pre emphasis 3.5 dB 0110 : swing2 pre emphasis 3.5 dB 1000 : swing0 pre emphasis 6 dB 1001 : swing1 pre emphasis 6 dB 1100 : swing0 pre emphasis 9.5 dB others : swing0 pre emphasis 9.5 dB	5

Table 11-83 AVI InfoFrame Packet Data Byte (AVI_DB1 ~ AVI_DB13)

Register	Address	Type	Description	Reset Value
AVI_DB1 ~ AVI_DB13	Base + 0x01D0 ~ Base + 0x0200	R/W	AVI InfoFrame Packet Data Byte	0x0000_0000

AVI_DB1 ~ AVI_DB13	Bit	Description	Initial State
-	[31:8]	Reserved	0
AVI_DB1 ~ AVI_DB13	[7:0]	AVI Data Byte 1 ~ 13	0

Table 11-84 Audio InfoFrame Packet Data Byte (AUDIO_DB1 ~ AUDIO_DB10)

Register	Address	Type	Description	Reset Value
AUDIO_DB1 ~ AUDIO_DB10	Base + 0x021C ~ Base + 0x0240	R/W	Audio InfoFrame Packet Data Byte	0x0000_0000

AUDIO_DB1 ~ AUDIO_DB10	Bit	Description	Initial State
-	[31:8]	Reserved	0
AUDIO_DB1 ~ AUDIO_DB10	[7:0]	Audio InfoFrame Data Byte 1 ~ 10	0

Table 11-85 InfoFrame Packet Type Code (IF_TYPE)

Register	Address	Type	Description	Reset Value
IF_TYPE	Base + 0x0244	R/W	InfoFrame Packet Type Code.	0x0000_0000

IF_TYPE	Bit	Description	Initial State
-	[31:8]	Reserved	0
IF_TYPE	[7:0]	InfoFrame Packet Type Code. It can be set as (0x80 + InfoFrame Type Code) and send any type of infoframe defined in CEA-861C. Commonly, we set it as 0x83(0x80 + 0x03, 0x03 is the type code of SPD InfoFrame) and send SPD infoframe.	0

Table 11-86 InfoFrame Packet Data Byte (IF_PKT_DB1~25)

Register	Address	Type	Description	Reset Value
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IF_PKT_DB1 ~ IF_PKT_DB25	Base + 0x0254 ~ Base + 0x02B4	R/W	InfoFrame Packet Data Byte	0x0000_0000
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IF_PKT_DB1 ~ IF_PKT_DB25	Bit	Description	Initial State
-	[31:8]	Reserved	0
IF_PKT_DB1 ~ IF_PKT_DB25	[7:0]	InfoFrame Packet Data Byte 1 ~ 25. The registers define the data in the InfoFrame and the InfoFrame type is defined by IF_TYPE.	0

Table 11-87 MPEG Source InfoFrame Packet Data Byte (MPEG_DB1 ~ MPEG_DB10)

Register	Address	Type	Description	Reset Value
MPEG_DB1 ~ MPEG_DB10	Base + 0x02D0 ~ Base + 0x02F4	R/W	MPEG Source InfoFrame Packet Data Byte	0x0000_0000

MPEG_DB1 ~ MPEG_DB10	Bit	Description	Initial State
-	[31:8]	Reserved	0
MPEG_DB1 ~ MPEG_DB10	[7:0]	MPEG InfoFrame Data Byte 1 ~ 10	0

Table 11-88 Reuse SPD Header Bytes registers(HB0—HB3)

Register	Address	Type	Description	Reset Value
REUSE_SPD_HB	Base + 0x02F8 ~ Base + 0x0304	R/W	Reuse SPD HB0 ~ HB3	0x0000_0000

REUSE_SPD_HB	Bit	Description	Initial State
-	[31:8]	Reserved	0
REUSE_SPD_HB	[7:0]	Reuse SPD HB0 ~ HB3	0

Table 11-89 REUSE SPD Parity Bytes registers(PB0—PB3)

Register	Address	Type	Description	Reset Value
REUSE_SPD_PB	Base + 0x0308 ~ Base + 0x0314	R/W	REUSE SPD PB0 ~ PB3	0x0000_0000

REUSE_SPD_PB	Bit	Description	Initial State
-	[31:8]	Reserved	0
REUSE_SPD_PB	[7:0]	Reuse SPD PB0 ~ PB3	0

Table 11-90 PSR Frame Update Control Register

Register	Address	Type	Description	Reset Value
PSR_FRAME_UPDATA_CTRL	Base + 0x0318	R/W	PSR frame update control	0x0000_0000

PSR_FRAME_UPDATA_CTRL	Bit	Description	Initial State
-	[31:2]	Reserved	0

PSR_FRAME_UP_TYPE	[1]	Select PSR Frame Update type. 1 = Burst single frame update. 0 = Single frame update.	0
PSR_FRAME_UPDATE(C)	[0]	Enable PSR Frame Update	0

Table 11-91 VSC Shadow Data Bytes Register

Register	Address	Type	Description	Reset Value
VSC_SHADOW_DB0~	Base+ 0x031C			0x0000_0000
VSC_SHADOW_DB7	~ Base+ 0x0338	R/W	VSC shadow data bytes 0 ~ 7	

VSC_SHADOW_DATA_BYTES	Bit	Description	Initial State
-	[31:8]	Reserved	0
VSC_SHADOW_DB0~	[7:0]	VSC shadow data bytes 0 ~ 7	0
VSC_SHADOW_DB7			

Table 11-92 VSC Shadow Parity Bytes Register

Register	Address	Type	Description	Reset Value
VSC_SHADOW_PB0~	Base+ 0x033C			0x0000_0000
VSC_SHADOW_PB1	~ Base+ 0x0340	R/W	VSC shadow parity bytes 0 ~ 1	

VSC_SHADOW_PARITY_BYTES	Bit	Description	Initial State
-	[31:8]	Reserved	0
VSC_SHADOW_PB0~	[7:0]	VSC shadow parity bytes 0 ~ 1	0
VSC_SHADOW_PB1			

Table 11-93 Audio I2S Channel Status Register 1 (AUDIO_I2S_CH_STA1)

Register	Address	Type	Description	Reset Value
AUDIO_I2S_CH_STA1	Base + 0x0344	R/W	Audio I2S Channel Status Register 1	0x0000_0000

AUDIO_I2S_CH_STA1	Bit	Description	Initial State
-	[31:8]	Reserved	0
AUDIO_MODE	[7:6]	00: PCM Audio, Others: No PCM Audio stream	0
PCM_MODE	[5:3]	000: 2 audio channels without pre-emphasis, 001: 2 audio channels with 50/15 pre-emphasis	0
SW_CPRGT	[2]	0: Software for which copyright is asserted, 1: Software for which no copyright is asserted	0
NON_PCM	[1]	0: Audio sample word represents linear PCM samples, 1: Audio sample word used for other purposes.	0
PROF_APP	[0]	0: Consumer applications, 1: Professional applications.	0

Table 11-94 Audio I2S Channel Status Register 2 (AUDIO_I2S_CH_STA2)

Register	Address	Type	Description	Reset Value
AUDIO_I2S_CH_STA2	Base + 0x0348	R/W	Audio I2S Channel Status Register 2	0x0000_0000

AUDIO_I2S_CH_STA2	Bit	Description	Initial State

-	[31:8]	Reserved	0
CAT_CODE	[7:0]	Category code (corresponding to channel status bits [15:8])	0

Table 11-95 Audio I2S Channel Status Register 3 (AUDIO_I2S_CH_STA3)

Register	Address	Type	Description	Reset Value
AUDIO_I2S_CH_STA3	Base + 0x034C	R/W	Audio I2S Channel Status Register 3	0x0000_0000

AUDIO_I2S_CH_STA3	Bit	Description	Initial State
-	[31:8]	Reserved	0
CH_NUM	[7:4]	Channel number (corresponding to channel status bits [23:20]). Only 2_channel is supported in BIST mode	0
SOURCE_NUM	[3:0]	Source number (corresponding to channel status bits [19:16]). Only 2_channel is supported in BIST mode	0

Table 11-96 Audio I2S Channel Status Register 4 (AUDIO_I2S_CH_STA4)

Register	Address	Type	Description	Reset Value
AUDIO_I2S_CH_STA4	Base + 0x0350	R/W	I2S Channel Status Register 4	0x0000_0000

AUDIO_I2S_CH_STA4	Bit	Description	Initial State
-	[31:8]	Reserved	0
CHNL_BIT1	[7:6]	corresponding to channels status bits [31:30]	0
CLK_ACCUR	[5:4]	Clock accuracy (corresponding to channels status bits [29:28]). These two bits define the sampling frequency tolerance. The bits are set in the transmitter.	0
FS_FREQ	[3:0]	Sampling clock frequency (corresponding to channel status bits [27:24]). 0000: 44.1 KHz, 0010: 48 KHz, 0011: 32 KHz, 1000: 88.2 KHz, 1010: 96 KHz, 1110: 192 KHz, Others: Reserved. When set SPDIF_FS_OVRWR to "1", the four bits sample clock frequency in channel status is replaced by this register setting. Note that the audio sine wave frequency equals to Audio Sample Frequency/128. For example, if the sampling clock frequency is 44.1K, the sine wave frequency is 44,100/128 = 344.6Hz.	0

Table 11-97 Audio I2S Channel Status Register 5 (AUDIO_I2S_CH_STA5)

Register	Address	Type	Description	Reset Value
AUDIO_I2S_CH_STA5	Base + 0x0354	R/W	Audio Channel Status Register 5	0x0000_000B

AUDIO_I2S_CH_STA5	Bit	Description	Initial State
-	[31:8]	Reserved	0

CHNL_BIT2	[7:4]	corresponding to channels status bits [39:36]	0
WORD_LENGTH	[3:1]	Audio word length (corresponding to channel status bits [35:33]). When WORD_MAX: 0, 001: 16 bits, 010: 18 bits, 100: 19 bits, 101: 20 bits, 110: 17 bits, When WORD_MAX: 1, 001: 20 bits, 010: 22 bits, 100: 23 bits, 101: 24 bits, 110: 21 bits.	5
WORD_MAX	[0]	Audio word length Max (corresponding to channel status bits 32). 0: Maximal word length is 20 bits, 1: Maximal word length is 24 bits.	1

Table 11-98 Lane Map Register (LANE_MAP)

Register	Address	Type	Description	Reset Value
LANE_MAP	Base + 0x035C	R/W	Lane Map Register	0x0000_00E4

LANE_MAP	Bit	Description	Initial State
-	[31:8]	Reserved	0
LANE3_MAP	[7:6]	Control physical lane 3 will map to which logic lane: 0x11: Logic lane 3, 0x10: Logic lane 2, 0x01: Logic lane 1, 0x00: Logic lane 0,	3
LANE2_MAP	[5:4]	Control physical lane 2 will map to which logic lane: 0x11: Logic lane 3, 0x10: Logic lane 2, 0x01: Logic lane 1, 0x00: Logic lane 0,	2
LANE1_MAP	[3:2]	Control physical lane 1 will map to which logic lane: 0x11: Logic lane 3, 0x10: Logic lane 2, 0x01: Logic lane 1, 0x00: Logic lane 0,	1
LANE0_MAP	[1:0]	Control physical lane 0 will map to which logic lane: 0x11: Logic lane 3, 0x10: Logic lane 2, 0x01: Logic lane 1, 0x00: Logic lane 0,	0

Table 11-99 Analog Control Register 2 (ANALOG_CTL_2)

Register	Address	Type	Description	Reset Value
ANALOG_CTL_2	Base + 0x0374	R/W	Analog Control Register 2	0x0000_0008

ANALOG_CTL_2	Bit	Description	Initial State
-	[31:4]	Reserved	0
SEL_24M	[3]	Choose the reference clock of PHY use 24M or 27M: 1: Use 24M clock, 0: Use 27M clock.	1

Table 11-100 Hidden Register (INT_STATE_0)

Register	Address	Type	Description	Reset Value
INT_STATE_0	Base + 0x0390	R/W	Hidden Register for debug	0x0000_0003

INT_STATE_0	Bit	Description	Initial State
-	[31:12]	Reserved	0
AUX_CH_DATA_IN(RO)	[11]	AUX received data for debug when AUX_CH_TEST_MODE = 1 and AUX_CH_EN_TEST=0 This bit is read only	0
AUX_SEND_0_1_EN	[10]	1: Force 0/1 toggle in AUX CH when AUX_CH_TEST_MODE = 0 0: normal AUX data transmitting in AUX CH when AUX_CH_TEST_MODE = 0	0
AUX_CH_TEST_MODE	[9]	1: AUX CH is in test mode. 0: AUX CH is in normal mode.	0
AUX_CH_T_TEST	[8]	AUX transmitted data when AUX_CH_TEST_MODE = 1	0
AUX_CH_EN_TEST	[7]	AUX TX enable when AUX_CH_TEST_MODE = 1. 0: disable 1: enable	0
M_VID_DEBUG_EN	[6]	Enable M_VID debugging	0
BIST_YCBCR422_CRL	[5]	For YCbCr422 BIST control	0
AUX_TC	[4:3]	AUX TC Register	0
AUX_RETRY_TIMER	[2:0]	AUX Retry Timer Register	3

Table 11-101 Interrupt Status Register (INT_STATE_1)

Register	Address	Type	Description	Reset Value
INT_STATE_1	Base + 0x03C0	RO	Interrupt Status Register	0x0000_0000

INT_STATE_1	Bit	Description	Initial State
-	[31:1]	Reserved	0
INT_STATE	[0]	Interrupt request status 1: Interrupt service is requested, 0: No interrupt service is requested.	0

Table 11-102 Common Interrupt Status Register 1 (COMMON_INT_STA_1)

Register	Address	Type	Description	Reset Value
COMMON_INT_STA_1	Base + 0x03C4	R/W C1	Common Interrupt Status Register 1	0x0000_0000

COMMON_INT_STA_1	Bit	Description	Initial State
-	[31:8]	Reserved	0
VSYNC_DET	[7]	1: VSYNC active edge has been detected. Write 1 to clear.	0
PLL_LOCK_CHG	[6]	1: PLL lock state is changed. Write 1 to clear. Check PLL_LOCK of register DP_DEBUG_CTL for PLL lock status.	0
SPDIF_ERR	[5]	1: SPDIF parity errors. Write 1 to clear. Software can change this interrupt generation by setting the register SPDIF_ERR_THRD. When SPDIF_ERR, software shall check SPDIF status on register SPDIF_AUDIO_STA_0	0

SPDIF_UNSTBL	[4]	1: Not find expected preamble for SPDIF input. Write 1 to clear.	0
VID_FORMAT_CHG	[3]	1: Video input format change is detected. Write 1 to clear.	0
AUD_CLK_CHG	[2]	1: Audio input clock change is detected. Write 1 to clear.	0
VID_CLK_CHG	[1]	1: Video input clock change is detected.	0
SW_INT	[0]	1: Software-induced interrupt. Write 1 to clear.	0

Note: All of interrupt status bits are edge triggered.

Note: Interrupt status bits are set regardless of the value of the corresponding interrupt mask bits. But if a mask bit is set, then the corresponding interrupt status is not routed to INT_STATE, which is connected to the system.

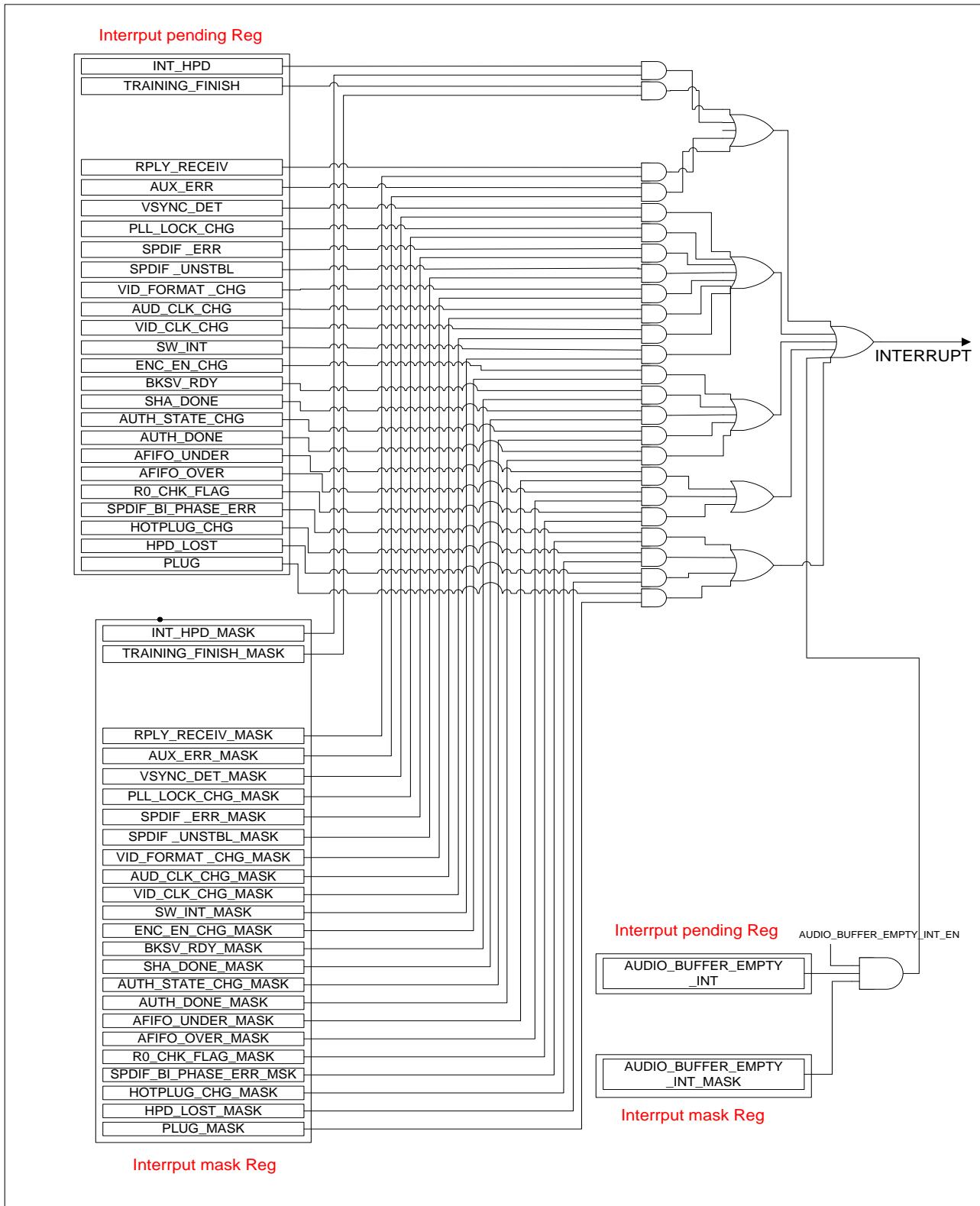


Fig. 11-30 Interrupt Status Registers and Mask Registers
Table 11-103 Common Interrupt Status Register 2 (COMMON_INT_STA_2)

Register	Address	Type	Description	Reset Value
COMMON_INT_STA_2	Base + 0x03C8	R/W C1	Common Interrupt Status Register 2	0x0000_0000

COMMON_INT_STA_2	Bit	Description	Initial State
-	[31:7]	Reserved	0

COMMON_INT_STA_2	Bit	Description	Initial State
ENC_EN_CHG	[6]	1: HDCP_ENC_EN changed detected. Write 1 to clear. ENC_EN_CHG happens whenever HDCP_ENC_EN is changed from 1 to 0 or from 0 to 1. This interrupt is generated when the internal HDCP cipher module find out that encryption status is changed. Software can check encryption status on bit ENCRYPT of register HDCP_STA.	0
-	[5:4]	Reserved	0
HW_BKSV_RDY	[3]	1: BKSV is ready. Write 1 to clear. It is for H/W HDCP	0
HW_SHA_DONE	[2]	1: HDCP hardware computing V has ended. Write 1 to clear. During H/W HDCP authentication, it is generated after calculating V.	0
HW_AUTH_STATE_CHG	[1]	1: H/W HDCP authentication state has changed. Write 1 to clear. HW_AUTH_STATE_CHG happens after H/W HDCP is enabled Software can check hardware authentication status on bit HW_AUTHEN_PASS of register HDCP_STA This bit is set only when authentication success or failure status is changed. So, successive authentication failure does not set this bit.	0
HW_AUTH_DONE	[0]	1: H/W HDCP authentication has ended. Write 1 to clear. This bit is set when H/W HDCP authentication is finished regardless of success or failure. Software can check hardware authentication status on bit HW_AUTHEN_PASS of register HDCP_STA	0

Table 11-104 Common Interrupt Status Register 3 (COMMON_INT_STA_3)

Register	Address	Type	Description	Reset Value
COMMON_INT_STA_3	Base + 0x03CC	R/W C1	Common Interrupt Status Register 3	0x0000_0000

COMMON_INT_STA_3	Bit	Description	Initial State
-	[31:8]	Reserved	0
AFIFO_UNDER	[7]	1: Audio FIFO is under run. Write 1 to clear.	0
AFIFO_OVER	[6]	1: Audio FIFO is overrun. Write 1 to clear.	0

COMMON_INT_STA_3	Bit	Description	Initial State
R0_CHK_FLAG	[5]	For hardware authentication (with HDCP repeater): 1: R0 check is finished. For software authentication: 1: R0 is ready for software check. Write 1 to clear. If H/W re-authentication is needed and this bit is set to 1, then this bit must be cleared before H/W re-authentication.	0
DPCD_SPECIFIC_IRQ	[4]	1: Sink specific interrupt in DPCD is detected. Write 1 to clear	0
MYDP_PLUG_IN	[3]	1: MYDP plug out event is detected. Write 1 to clear	0
MYDP_PLUG_OUT	[2]	1: MYDP plug out event is detected. Write 1 to clear	0
MYDP_HPD_IRQ	[1]	1: MYDP HPD interrupt is detected. Write 1 to clear	0
HDCP_LINK_CHECK_FAIL	[0]	1: HDCP link check failure is detected. Write 1 to clear.	0

Table 11-105 Common Interrupt Status Register 4 (COMMON_INT_STA_4)

Register	Address	Type	Description	Reset Value
COMMON_INT_STA_4	Base + 0x03D0	R/W C1	Common Interrupt Status Register 4	0x0000_0000

COMMON_INT_STA_4	Bit	Description	Initial State
-	[31:6]	Reserved	0
SPDIF_BI_PHASE_ERR	[5]	1: SPDIF bi-phase error has occurred. Write 1 to clear. Software reset will not clear this interrupt.	0
-	[4:3]	Reserved	0
HOTPLUG_CHG	[2]	1: Hot plug change detected. Write 1 to clear. HOTPLUG_CHG happens whenever the pin I_DP_HDP changes and the change remains for at least hot plug deglitch time. And the hot plug deglitch time is defined in HPD_DEGLITCH_L and HPD_DEGLITCH_H. When HOTPLUG_CHG is high, software shall check the status of HPD signal on register HPD_STATUS.	0
HPD_LOST	[1]	Hot plug detect signal lost timer larger than 2ms, that means cable is plugged out: 1: Interrupt assert, 0: Not interrupt occurred Write 1 to this bit to clear this interrupt source.	0
PLUG	[0]	Hot plug detect signal lost time is larger than 2ms before cable plugged, it means cable is plugged in: 1: Interrupt assert, 0: Not interrupt occurred Write 1 to this bit to clear this interrupt source.	0

Table 11-106 SPDIF Biphase Interrupt Status Register (SPDIF_BIPHASE_INT_STA)

Register	Address	Type	Description	Reset Value
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SPDIF_BIPHASE_INT_STA	Base + 0x03D4	WO	SPDIF Biphase Interrupt Status Register	0x0000_0000
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SPDIF_BIPHASE_INT_STA	Bit	Description	Initial State
-	[31:8]	Reserved	0
SPDIF_BIPHASE_ERR_CLR(WO)	[7]	SPDIF biphase error	0
-	[6:0]	Reserved	0

Table 11-107 DisplayPort Interrupt Status Register (DP_INT_STA)

Register	Address	Type	Description	Reset Value
DP_INT_STA	Base + 0x03DC	R/W C1	DisplayPort Interrupt Status Register	0x0000_0000

DP_INT_STA	Bit	Description	Initial State
-	[31:7]	Reserved	0
INT_HPD	[6]	IRQ (HPD de-asserted less than 2ms) detect interrupt: 1: IRQ interrupt assert, 0: Not interrupt occurred Write 1 to this bit to clear this interrupt source.	0
HW_TRAINING_FINISH	[5]	Training FSM module finish link training procedure: 1: Hardware link training finished, 0: Not interrupt occurred Write 1 to this bit to clear this interrupt source.	0
-	[4]	Reserved	0
SINK_LOST	[3]	Sink lost interrupt 1: Sink lost occurred 0: Not interrupt occurred Write 1 to this bit to clear this interrupt source.	0
LINK_LOST	[2]	Link lost interrupt 1: Link lost occurred 0: Not interrupt occurred Write 1 to this bit to clear this interrupt source.	0
RPLY_RECEIV	[1]	AUX channel command reply is received: 1: Interrupt assert, 0: Not interrupt occurred Write 1 to this bit to clear this interrupt source.	0
AUX_ERR	[0]	AUX channel access error interrupt: 1: Interrupt assert, 0: Not interrupt occurred Write 1 to this bit to clear this interrupt source.	0

Table 11-108 Interrupt Mask Register (COMMON_INT_MASK_1)

Register	Address	Type	Description	Reset Value
COMMON_INT_MASK_1	Base + 0x03E0	R/W	Interrupt Mask Register	0x0000_0000

COMMON_INT_MASK_1	Bit	Description	Initial State
-	[31:8]	Reserved	0
COMMON_INT_MASK_1[7:0]	[7:0]	Each bit corresponds to the same bit in Common Interrupt Status Register 1. 0: Mask interrupt 1: Enable interrupt	0

Table 11-109 Interrupt Mask Register (COMMON_INT_MASK_2)

Register	Address	Type	Description	Reset Value
COMMON_INT_MASK_2	Base + 0x03E4	R/W	Interrupt Mask Register	0x0000_0000

COMMON_INT_MASK_2	Bit	Description	Initial State
-	[31:7]	Reserved	0
COMMON_INT_MASK_2[6]	[6]	Each bit corresponds to the same bit in Common Interrupt Status Register 2. 0: Mask interrupt 1: Enable interrupt	0
-	[5:4]	Reserved	0
COMMON_INT_MASK_2[3:0]	[3:0]	Each bit corresponds to the same bit in Common Interrupt Status Register 2. 0: Mask interrupt 1: Enable interrupt	0

Table 11-110 Interrupt Mask Register (COMMON_INT_MASK_3)

Register	Address	Type	Description	Reset Value
COMMON_INT_MASK_3	Base + 0x03E8	R/W	Interrupt Mask Register	0x0000_0000

COMMON_INT_MASK_3	Bit	Description	Initial State
-	[31:8]	Reserved	0
COMMON_INT_MASK_3[7:5]	[7:0]	Each bit corresponds to the same bit in Common Interrupt Status Register 3. 0: Mask interrupt 1: Enable interrupt	0

Table 11-111 Interrupt Mask Register (COMMON_INT_MASK_4)

Register	Address	Type	Description	Reset Value
COMMON_INT_MASK_4	Base + 0x03EC	R/W	Interrupt Mask Register	0x0000_0000

COMMON_INT_MASK_4	Bit	Description	Initial State
-	[31:6]	Reserved	0
COMMON_INT_MASK_4[5]	[5]	Each bit corresponds to the same bit in Common Interrupt Status Register 3. 0: Mask interrupt 1: Enable interrupt	0
-	[4:3]	Reserved	0
COMMON_INT_MASK_4[2:0]	[2:0]	Each bit corresponds to the same bit in Common Interrupt Status Register 3. 0: Mask interrupt 1: Enable interrupt	0

Table 11-112 DP Interrupt Mask Register (DP_INT_STA_MASK)

Register	Address	Type	Description	Reset Value
DP_INT_STA_MASK	Base + 0x03F8	R/W	Interrupt enable Register	0x0000_0000

DP_INT_STA_MASK	Bit	Description	Initial State
-	[31:7]	Reserved	0

DP_INT_STA_MASK	[6:0]	Each bit corresponds to the same bit in DisplayPort Interrupt Status Register (DP_INT_STA). 1: Enable interrupt. 0: Mask interrupt.	0
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Table 11-113 Interrupt Control Register (INT_CTL)

Register	Address	Type	Description	Reset Value
INT_CTL	Base + 0x03FC	R/W	Interrupt Control Register	0x0000_0001

INT_CTL	Bit	Description	Initial State
-	[31:6]	Reserved	0
SERDES_OVERFLOW_CLEAR	[5]	1: clear SerDes FIFO overflow flag	0
SERDES_UNDERFLOW_CLEAR	[4]	1: clear SerDes FIFO underflow flag	0
-	[3]	Reserved	0
SOFT_INT_CTRL	[2]	Set Software Interrupt: 1: Set interrupt, 0: Do not set interrupt,	0
-	[1]	Reserved	0
INT_POL	[0]	INT pin assertion polarity: 1: Assert high, 0: Assert low	1

Register Definition for HDCP Function

Table 11-114 HDCP Status Register (HDCP_STA)

Register	Address	Type	Description	Reset Value
HDCP_STA	Base + 0x0400	RO	HDCP Status Register	0x0000_0000

HDCP_STA	Bit	Description	Initial State
-	[31:4]	Reserved	0
REAUTH_REQUEST	[7]	1: reauthentication request is active 0: reauthentication request is inactive	0
AUTH_FAIL	[6]	1: Authentication fail 0: Authentication not fails.	0
HARD_1ST_HDCP_AUTHED	[5]	1: 1ST authentication is ok 0: 1ST authentication is not ok	0
BLOCK_DONE	[4]	1: HDCP cipher block is finished. 0: HDCP cipher block is not finish.	0
BKSV_VALID	[3]	BKSV validity status. Valid BKSV must contain 20 ones and 20 zeros. For H/W authentication, this status 1: BKSV is valid. 0: BKSV is not valid.	0
ENCRYPT	[2]	HDCP module encryption status. It is set to 1 after CPSR is detected. And it is set to 0 after SR is detected. 1: Encryption is active, 0: Encryption is inactive.	0
HW_AUTHEN_PASS	[1]	H/W HDCP Authentication success status. 1: H/W HDCP authentication is finished successfully, 0: H/W HDCP authentication is not passed.	0
LOAD_KEY_DONE	[0]	1: HDCP external key load done 0: External key is loading.	0

Table 11-115 HDCP Control Register 0 (HDCP_CTL_0)

Register	Address	Type	Description	Reset Value
HDCP_CTL_0	Base + 0x0404	R/W	HDCP Control Register 0	0x0000_0000
HDCP_CTL_0	Bit	Description		Initial State
-	[31:8]	Reserved		0
SW_STORE_AN	[7]	<p>Start or stop PRNG. The result of PRNG is used for session key, AN. The initial seed number is hardwired. The interval between start and stop command creates different AN. Current AN is always used as new seed value of PRNG.</p> <p>0: Start PRNG, 1: Stop PRNG and save the 64 bit random number to AN.</p> <p>The bit field is controllable only after valid BKSVs are written into BKSV0~BKSV4 registers. The validity of BKSVs can be checked by BKSV_ACTIVE. The bit filed is for S/W HDCP authentication.</p>		0
HW_RE_AUTHEN	[5]	H/W HDCP authentication is restarted when this bit is set to 1. It must be cleared by firmware right after set to 1.		0
SW_AUTH_OK	[4]	<p>S/W HDCP authentication success status indicator. When checking R0 = R0', software shall set this bit to 1. Otherwise set to 0. Encryption module will not start when set to 0.</p> <p>This bit can be set to 1 at the same time with HDCP_ENC_EN for S/W authentication if S/W HDCP authentication is successful.</p> <p>1: Software HDCP authentication is finished successfully, 0: Software HDCP authentication is not passed.</p>		0
HW_AUTH_EN	[3]	<p>H/W HDCP authentication enabled.</p> <p>1: Enable 0: Disable.</p> <p>If set to 1, H/W authentication starts. When using software HDCP, this bit shall be cleared.</p> <p>This bit must not be cleared until re-authentication is necessary. Otherwise, clearing this bit will break data integrity.</p>		0
HDCP_ENC_EN	[2]	<p>HDCP encryption mode enabled.</p> <p>1: Enable 0: Disable.</p> <p>It is for both H/W HDCP and S/W HDCP.</p> <p>For software HDCP, before setting this bit to 1, SW_AUTH_OK must be set to 1.</p>		0
HW_1ST_PART_AUTHENTICATION_EN	[1]	<p>1st part H/W HDCP authentication enables. It must be set to 1 before starting H/W or S/W authentication. Otherwise authentication will fail.</p> <p>1: Enable normal 1st part H/W HDCP authentication, 0: Disable normal 1st part H/W HDCP authentication.</p>		0
HW_2ND_PART_AUTHENTICATION_EN	[0]	<p>2nd part H/W HDCP authentication enables. It must be set to 1 before starting H/W authentication. Without setting this bit, H/W authentication always turns out to fail as long as DP Rx is a repeater.</p> <p>1: Enable normal 2nd part H/W HDCP authentication, 0: Disable normal 2nd part H/W HDCP authentication.</p>		0

Table 11-116 HDCP Control Register 1 (HDCP_CTL_1)

Register	Address	Type	Description	Reset Value
HDCP_CTL_1	Base + 0x0408	R/W	HDCP Control Register 1	0x0000_0000

HDCP_CTL_1	Bit	Description	Initial State
-	[31:4]	Reserved	0
DPCD_REV_1_2	[3]	DPCD revision 1.2	0x0
	[2:0]	Reserved	0x0

Table 11-117 HDCP AKSV Register 0(AKSV0)

Register	Address	Type	Description	Reset Value
AKSV0	Base + 0x0414	RO	HDCP AKSV Register 0	0x0000_0000

AKSV0	Bit	Description	Initial State
-	[31:8]	Reserved	0
AKSV0	[7:0]	AKSV bit [7:0]	0x00

Table 11-118 HDCP AKSV Register 1(AKSV1)

Register	Address	Type	Description	Reset Value
AKSV1	Base + 0x0418	RO	HDCP AKSV Register 1	0x0000_0000

AKSV1	Bit	Description	Initial State
-	[31:8]	Reserved	0
AKSV1	[7:0]	AKSV bit [15:8]	0x00

Table 11-119 HDCP AKSV Register 2(AKSV2)

Register	Address	Type	Description	Reset Value
AKSV2	Base + 0x041C	RO	HDCP AKSV Register 2	0x0000_0000

AKSV2	Bit	Description	Initial State
-	[31:8]	Reserved	0
AKSV2	[7:0]	AKSV bit [23:16]	0x00

Table 11-120 HDCP AKSV Register 3(AKSV3)

Register	Address	Type	Description	Reset Value
AKSV3	Base + 0x0420	RO	HDCP AKSV Register 3	0x0000_0000

AKSV3	Bit	Description	Initial State
-	[31:8]	Reserved	0
AKSV3	[7:0]	AKSV bit [31:24]	0x00

Table 11-121 HDCP AKSV Register 4(AKSV4)

Register	Address	Type	Description	Reset Value
AKSV4	Base + 0x0424	RO	HDCP AKSV Register 4	0x0000_0000

AKSV4	Bit	Description	Initial State
-	[31:8]	Reserved	0
AKSV4	[7:0]	AKSV bit [39:32].	0x00

Table 11-122 HDCP AN Register 0(AN0)

Register	Address	Type	Description	Reset Value
AN0	Base + 0x0428	RO	HDCP AN Register 0	0x0000_0000

AN0	Bit	Description	Initial State

-	[31:8]	Reserved	0
AN0	[7:0]	AN bit [7:0] AN can be read when BKSVACTIVE is high.	0

Table 11-123 HDCP AN Register 1(AN1)

Register	Address	Type	Description	Reset Value
AN1	Base + 0x042C	RO	HDCP AN Register 1	0x0000_0000

AN1	Bit	Description	Initial State
-	[31:8]	Reserved	0
AN1	[7:0]	AN bit [15:8]. AN can be read when BKSVACTIVE is high.	0

Table 11-124 HDCP AN Register 2(AN2)

Register	Address	Type	Description	Reset Value
AN2	Base + 0x0430	RO	HDCP AN Register 2	0x0000_0000

AN2	Bit	Description	Initial State
-	[31:8]	Reserved	0
AN2	[7:0]	AN bit [23:16]. AN can be read when BKSVACTIVE is high.	0

Table 11-125 HDCP AN Register 3(AN3)

Register	Address	Type	Description	Reset Value
AN3	Base + 0x0434	RO	HDCP AN Register 3	0x0000_0000

AN3	Bit	Description	Initial State
-	[31:8]	Reserved	0
AN3	[7:0]	AN bit [31:24] AN can be read when BKSVACTIVE is high.	0

Table 11-126 HDCP AN Register 4(AN4)

Register	Address	Type	Description	Reset Value
AN4	Base + 0x0438	RO	HDCP AN Register 4	0x0000_0000

AN4	Bit	Description	Initial State
-	[31:8]	Reserved	0
AN4	[7:0]	AN bit [39:32]. AN can be read when BKSVACTIVE is high.	0

Table 11-127 HDCP AN Register 5(AN5)

Register	Address	Type	Description	Reset Value
AN5	Base + 0x043C	RO	HDCP AN Register 5	0x0000_0000

AN5	Bit	Description	Initial State
-	[31:8]	Reserved	0
AN5	[7:0]	AN bit [47:40] AN can be read when BKSVACTIVE is high.	0

Table 11-128 HDCP AN Register 6(AN6)

Register	Address	Type	Description	Reset Value
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AN6	Base + 0x0440	RO	HDCP AN Register 6	0x0000_0000
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AN6	Bit	Description	Initial State
-	[31:8]	Reserved	0
AN6	[7:0]	AN bit [55:48] AN can be read when BKSV_ACTIVE is high.	0

Table 11-129 HDCP AN Register 7(AN7)

Register	Address	Type	Description	Reset Value
AN7	Base + 0x0444	RO	HDCP AN Register 7	0x0000_0000

AN7	Bit	Description	Initial State
-	[31:8]	Reserved	0
AN7	[7:0]	AN bit [63:56] AN can be read when BKSV_ACTIVE is high.	0

Table 11-130 BKSV Register 0(BKSV0)

Register	Address	Type	Description	Reset Value
BKSV0	Base + 0x0448	R/W	HDCP BKSV Register 0	0x0000_0000

BKSV0	Bit	Description	Initial State
-	[31:8]	Reserved	0
BKSV0	[7:0]	BKSV bit [7:0]	0

Table 11-131 HDCP BKSV Register 1(BKSV1)

Register	Address	Type	Description	Reset Value
BKSV1	Base + 0x044C	R/W	HDCP BKSV Register 1	0x0000_0000

BKSV1	Bit	Description	Initial State
-	[31:8]	Reserved	0
BKSV1	[7:0]	BKSV bit [15:8]	0

Table 11-132 HDCP BKSV Register 2(BKSV2)

Register	Address	Type	Description	Reset Value
BKSV2	Base + 0x0450	R/W	HDCP BKSV Register 2	0x0000_0000

BKSV2	Bit	Description	Initial State
-	[31:8]	Reserved	0
BKSV2	[7:0]	BKSV bit [23:16]	0

Table 11-133 HDCP BKSV Register 3(BKSV3)

Register	Address	Type	Description	Reset Value
BKSV3	Base + 0x0454	R/W	HDCP BKSV Register 3	0x0000_0000

BKSV3	Bit	Description	Initial State
-	[31:8]	Reserved	0
BKSV3	[7:0]	BKSV bit [31:24]	0

Table 11-134 HDCP BKSv Register 4(BKSv4)

Register	Address	Type	Description	Reset Value
BKSv4	Base + 0x0458	R/W	HDCP BKSv Register 4	0x0000_0000

BKSv4	Bit	Description	Initial State
-	[31:8]	Reserved	0
BKSv4	[7:0]	BKSv bit [39:32] Hardware will start to calculate R0 when BKSv4 is set. The BKSv4 should be the last byte of BKSv written into register.	0

Table 11-135 HDCP RI Register 0(RI0)

Register	Address	Type	Description	Reset Value
RI0	Base + 0x045C	RO	HDCP RI Register 0	0x0000_0000

RI0	Bit	Description	Initial State
-	[31:8]	Reserved	0
RI0	[7:0]	RI bit [7:0]	0

Table 11-136 HDCP RI Register 1(RI1)

Register	Address	Type	Description	Reset Value
RI1	Base + 0x0460	RO	HDCP RI Register 1	0x0000_0000

RI1	Bit	Description	Initial State
-	[31:8]	Reserved	0
RI1	[7:0]	RI bit [15:8]	0

Table 11-137 Receiver BCAPS Register (HW_RX_CAPS)

Register	Address	Type	Description	Reset Value
HW_RX_CAPS	Base + 0x0468	RO	Receiver BCAPS Register	0x0000_0000

HW_RX_CAPS	Bit	Description	Initial State
-	[31:8]	Reserved	0
HW_RX_CAPS	[7:0]	HDCP ReceiverBcaps[7:0].it is for H/W HDCP	0

Table 11-138 HDCP Receiver BINFO Register 0(HW_RX_BINFO_0)

Register	Address	Type	Description	Reset Value
HW_RX_BINFO_0	Base + 0x046C	RO	HDCP Receiver B_info Register 0	0x0000_0000

HW_RX_BINFO_0	Bit	Description	Initial State
-	[31:8]	Reserved	0
HW_RX_BINFO_0	[7:0]	HDCP Receiver B_info [7:0]. It is for H/W HDCP	0

Table 11-139 HDCP Receiver BINFO Register 1(HW_RX_BINFO_1)

Register	Address	Type	Description	Reset Value
HW_RX_BINFO_1	Base + 0x0470	RO	HDCP Receiver B_info Register 1	0x0000_0000

HW_RX_BINFO_1	Bit	Description	Initial State
-	[31:8]	Reserved	0
HW_RX_BINFO_1	[7:0]	HDCP Receiver B_info [15:8]. It is for H/W HDCP	0

Table 11-140 HDCP Debug Control Register (HW_SKIP_RPT_ZERO_DEV)

Register	Address	Type	Description	Reset Value
HW_SKIP_RPT_ZERO_DEV	Base + 0x0474	R/W	HDCP Debug Control Register	0x0000_0000

HW_SKIP_RPT_ZERO_DEV	Bit	Description	Initial State
-	[31:1]	Reserve	0
HW_SKIP_RPT_ZERO_DEV	[0]	Configuration for HDCP repeater authentication method when device counter is zero. 1: not perform KSV list SHA computing. 0: Perform KSV list SHA computing. It is for H/W HDCP	0

Table 11-141 SPSRAM Access Configure Register 1 (SPSRAM_CFG_1)

Register	Address	Type	Description	Reset Value
SPSRAM_CFG_1	Base + 0x0488	R/W	Configure SPSRAM Access register 1.	0x0000_0020

SPSRAM_CFG	Bit	Description	Initial State
-	[31:6]	Reserved	0
SRAM_R/W_DONE(RO)	[5]	Indication of Memory command if last Memory operation is finished. 1: The Memory controller has finished the accessing of Memory. 0: Doesn't finish. The bit is read only.	1
-	[4:1]	Reserved	0
KSV_READ_EN(C)	[0]	1: Read KSV Data from External Memory 0: No Read KSV Operation The bit is self clear.	0

Table 11-142 HDCP auth debug register (HDCP_AUTH_DBG)

Register	Address	Type	Description	Reset Value
HDCP_AUTH_DBG	Base + 0x049C	RO	HDCP AUTH FSM status	0x0000_0000

HDCP_AUTH_DBG	Bit	Description	Initial State
-	[31:8]	Reserved	0
HDCP_AUTH_DBG	[7:0]	HDCP AUTH FSM status	0

Table 11-143 HDCP enc debug register (HDCP_ENC_DBG)

Register	Address	Type	Description	Reset Value
HDCP_ENC_DBG	Base + 0x04A0	RO	HDCP ENC FSM status	0x0000_0000

HDCP_ENC_DBG	Bit	Description	Initial State
-	[31:8]	Reserved	0

HDCP_ENC_DBG	[7:0]	HDCP ENC FSM status	0
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Table 11-144 HDCP Embedded “Blue Screen” Content Registers 0 (HDCP_VID_0)

Register	Address	Type	Description	Reset Value
HDCP_VID_0	Base + 0x04A8	R/W	HDCP Embedded “blue screen” Content Registers 0	0x0000_0000

HDCP_VID_0	Bit	Description	Initial State
-	[31:8]	Reserved	0
HDCP_VID_0	[7:0]	Blue or Cb component for HDCP Embedded “blue screen” when HDCP authentication failed. For higher bpc than 8 bit, lower bits are padded with 0s.	0

Table 11-145 HDCP Embedded “Blue Screen” Content Registers 1 (HDCP_VID_1)

Register	Address	Type	Description	Reset Value
HDCP_VID_1	Base + 0x04AC	R/W	HDCP Embedded “blue screen” Content Registers 1	0x0000_0000

HDCP_VID_1	Bit	Description	Initial State
-	[31:8]	Reserved	0
HDCP_VID_1	[7:0]	Green or Y component for HDCP Embedded “blue screen” when HDCP authentication failed. For higher bpc than 8 bit, lower bits are padded with 0s.	0

Table 11-146 HDCP Embedded “Blue Screen” Content Registers 2 (HDCP_VID_2)

Register	Address	Type	Description	Reset Value
HDCP_VID_2	Base + 0x04B0	R/W	HDCP Embedded “blue screen” Content Registers 2	0x0000_0000

HDCP_VID_2	Bit	Description	Initial State
-	[31:8]	Reserved	0
HDCP_VID_2	[7:0]	Red or Cr component for HDCP Embedded “blue screen” when HDCP authentication failed. For higher bpc than 8 bit, lower bits are padded with 0s.	0

Table 11-147 HDCP AM0 Register 0 (HDCP_AM0_0)

Register	Address	Type	Description	Reset Value
HDCP_AM0_0	Base + 0x04C0	RO	HDCP AM0 [7:0]	0x0000_0000

HDCP_AM0_0	Bit	Description	Initial State
-	[31:8]	Reserved	0
HDCP_AM0_0	[7:0]	HDCP AM0 [7:0], HDCP AM0 can be read when R0_CHK_FLAG is high.	0

Table 11-148 HDCP AM0 Register 1 (HDCP_AM0_1)

Register	Address	Type	Description	Reset Value
HDCP_AM0_1	Base + 0x04C4	RO	HDCP AM0 [15:8]	0x0000_0000

HDCP_AM0_1	Bit	Description	Initial State
-	[31:8]	Reserved	0
HDCP_AM0_1	[7:0]	HDCP AM0 [15:8], HDCP AM0 can be read when R0_CHK_FLAG is high.	0

Table 11-149 HDCP AM0 Register 2 (HDCP_AM0_2)

Register	Address	Type	Description	Reset Value
HDCP_AM0_2	Base + 0x04C8	RO	HDCP AM0 [23:16]	0x0000_0000

HDCP_AM0_2	Bit	Description	Initial State
-	[31:8]	Reserved	0
HDCP_AM0_2	[7:0]	HDCP AM0 [23:16], HDCP AM0 can be read when R0_CHK_FLAG is high.	0

Table 11-150 HDCP AM0 Register 3 (HDCP_AM0_3)

Register	Address	Type	Description	Reset Value
HDCP_AM0_3	Base + 0x04CC	RO	HDCP AM0 [31:24]	0x0000_0000

HDCP_AM0_3	Bit	Description	Initial State
-	[31:8]	Reserved	0
HDCP_AM0_3	[7:0]	HDCP AM0 [31:24], HDCP AM0 can be read when R0_CHK_FLAG is high.	0

Table 11-151 HDCP AM0 Register 4, reg (HDCP_AM0_4)

Register	Address	Type	Description	Reset Value
HDCP_AM0_4	Base + 0x04D0	RO	HDCP AM0 [39:32]	0x0000_0000

HDCP_AM0_4	Bit	Description	Initial State
-	[31:8]	Reserved	0
HDCP_AM0_4	[7:0]	HDCP AM0 [39:32], HDCP AM0 can be read when R0_CHK_FLAG is high.	0

Table 11-152 HDCP AM0 Register 5 (HDCP_AM0_5)

Register	Address	Type	Description	Reset Value
HDCP_AM0_5	Base + 0x04D4	RO	HDCP AM0 [47:40]	0x0000_0000

HDCP_AM0_5	Bit	Description	Initial State
-	[31:8]	Reserved	0
HDCP_AM0_5	[7:0]	HDCP AM0 [47:40], HDCP AM0 can be read when R0_CHK_FLAG is high.	0

Table 11-153 HDCP AM0 Register 6 (HDCP_AM0_6)

Register	Address	Type	Description	Reset Value
HDCP_AM0_6	Base + 0x04D8	RO	HDCP AM0 [55:48]	0x0000_0000

HDCP_AM0_6	Bit	Description	Initial State
-	[31:8]	Reserved	0
HDCP_AM0_6	[7:0]	HDCP AM0 [55:48], HDCP AM0 can be read when R0_CHK_FLAG is high.	0

Table 11-154 HDCP AM0 Register 7 (HDCP_AM0_7)

Register	Address	Type	Description	Reset Value
HDCP_AM0_7	Base + 0x04DC	RO	HDCP AM0 [63:56]	0x0000_0000

HDCP_AM0_7	Bit	Description	Initial State
-	[31:8]	Reserved	0
HDCP_AM0_7	[7:0]	HDCP AM0 [63:56], HDCP AM0 can be read when R0_CHK_FLAG is high.	0

Table 11-155 HDCP Wait R0 Timing Register (HW_WRITE_AKSV_WAIT)

Register	Address	Type	Description	Reset Value
HW_WRITE_AKSV_WAIT	Base+0x0500	R/W	Wait timing value for R0	0x0000_0064

HW_WRITE_AKSV_WAIT	Bit	Description	Initial State
-	[31:8]	Reserved	0
HW_WRITE_AKSV_WAIT	[7:0]	Wait timing value for R0 checking of HDCP first step H/W authentication after writing AKSV to receiver. Default value is 100 ms. Unit: 1ms	0x64

Table 11-156 LINK_CHECK_TIMER Register (LINK_CHECK_TIMER)

Register	Address	Type	Description	Reset Value
LINK_CHECK_TIMER	Base+0x0504	R/W	Wait timing value for R0	0x0000_0076

HW_WRITE_AKSV_WAIT	Bit	Description	Initial State
-	[31:8]	Reserved	0
LINK_CHECK_TIMER	[7:0]	Link Check Timer. Unit: 1ms	0x76

Table 11-157 HDCP Repeater Ready Wait Timer Register (HW_RPTR_RDY_TIMER)

Register	Address	Type	Description	Reset Value
HW_RPTR_RDY_TIMER	Base + 0x0508	R/W	Wait timing value for Repeater KSVFIFO ready in HDCP second step authentication	0x0000_0083

HW_RPTR_RDY_TIMER	Bit	Description	Initial State
-	[31:8]	Reserved	0

HW_RPTR_RDY_TIMER	[7:0]	Timeout value for Repeater KSVFIFO ready in HDCP second step H/W authentication. This is used to specify the timeout value of the counter which is enabled since DP Tx writes AKSV into DP Rx. So, if bstatus[0] in DPCD 0x68029 is not ready before timeout, HW HDCP authenticator will keep polling DPCD 0x68029; if bstatus[0] in DPCD 0x68029 is not ready after timeout, HW HDCP authenticator will restart HW HDCP authentication from the first step authentication reading BKSV from RX. Default value 0x83 means is 4.2s waiting time. Unit: 32 ms The waiting time = (HW_RPTR_RDY_TIMER * 32+8)ms	0x83
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Table 11-158 READY_POLL_TIMER Register (READY_POLL_TIMER)

Register	Address	Type	Description	Reset Value
READY_POLL_TIMER	Base+0x050C	R/W	Poll timing value for READY	0x0000_0009

READY_POLL_TIMER	Bit	Description	Initial State
-	[31:8]	Reserved	0
READY_POLL_TIMER	[7:0]	Poll timing value for READY	0x9

Table 11-159 HDCP HIDDEN Register (HDCP_HIDDEN_REG)

Register	Address	Type	Description	Reset Value
HDCP_HIDDEN_REG	Base+0x0510	R/W	HDCP_HIDDEN_REG	0x0000_0000

HDCP_HIDDEN_REG	Bit	Description	Initial State
-	[31:3]	Reserved	0
DERIVE_NEXT_AN	[2]	Derive next an	0
-	[1:0]	Reserved	0

Table 11-160 HDCP B INITIAIL VALUE Register (HDCP_B_INIT_RND0)

Register	Address	Type	Description	Reset Value
HDCP_B_INIT_RND0	Base+0x0514	W	HDCP B initial value[7:0]	0x0000_00C7

HDCP_B_INIT_RND0	Bit	Description	Initial State
-	[31:8]	Reserved	0
HDCP_B_INIT_RND0	[7:0]	HDCP B initial value[7:0]	0xC7

Table 11-161 HDCP B INITIAIL VALUE Register (HDCP_B_INIT_RND1)

Register	Address	Type	Description	Reset Value
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HDCP_B_INIT_RN D1	Base+0x05 18	W	HDCP B initial value[15:8]	0x0000_00 D7
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HDCP_B_INIT_RND1	Bit	Description	Initial State
-	[31:8]	Reserved	0
HDCP_B_INIT_RND1	[7:0]	HDCP B initial value[15:8]	0xD7

Table 11-162 HDCP B INITIAIL VALUE Register (HDCP_B_INIT_RND2)

Register	Address	Type	Description	Reset Value
HDCP_B_INIT_RN D2	Base+0x05 1C	W	HDCP B initial value[23:16]	0x0000_00 74

HDCP_B_INIT_RND2	Bit	Description	Initial State
-	[31:8]	Reserved	0
HDCP_B_INIT_RND2	[7:0]	HDCP B initial value[23:16]	0x74

Table 11-163 HDCP B INITIAIL VALUE Register (HDCP_B_INIT_RND3)

Register	Address	Type	Description	Reset Value
HDCP_B_INIT_RN D3	Base+0x05 20	W	HDCP B initial value[31:24]	0x0000_00 32

HDCP_B_INIT_RND3	Bit	Description	Initial State
-	[31:8]	Reserved	0
HDCP_B_INIT_RND3	[7:0]	HDCP B initial value[31:24]	0x32

Table 11-164 HDCP B INITIAIL VALUE Register (HDCP_B_INIT_RND4)

Register	Address	Type	Description	Reset Value
HDCP_B_INIT_RN D4	Base+0x05 24	W	HDCP B initial value[7:0]	0x0000_00 D3

HDCP_B_INIT_RND4	Bit	Description	Initial State
-	[31:8]	Reserved	0
HDCP_B_INIT_RND4	[7:0]	HDCP B initial value[39:32]	0xD3

Table 11-165 HDCP B INITIAIL VALUE Register (HDCP_B_INIT_RND5)

Register	Address	Type	Description	Reset Value
HDCP_B_INIT_RN D5	Base+0x0 528	W	HDCP B initial value[7:0]	0x0000_00 D0

HDCP_B_INIT_RND5	Bit	Description	Initial State
-	[31:8]	Reserved	0
HDCP_B_INIT_RND5	[7:0]	HDCP B initial value[47:40]	0xD0

Table 11-166 HDCP B INITIAIL VALUE Register (HDCP_B_INIT_RND6)

Register	Address	Type	Description	Reset Value
HDCP_B_INIT_RN_D6	Base+0x052C	W	HDCP B initial value[55:48]	0x0000_007F

HDCP_B_INIT_RND6	Bit	Description	Initial State
-	[31:8]	Reserved	0
HDCP_B_INIT_RND6	[7:0]	HDCP B initial value[55:48]	0x7F

Table 11-167 HDCP B INITIAIL VALUE Register (HDCP_B_INIT_RND7)

Register	Address	Type	Description	Reset Value
HDCP_B_INIT_RN_D7	Base+0x0530	W	HDCP B initial value[63:56]	0x0000_00C4

HDCP_B_INIT_RND7	Bit	Description	Initial State
-	[31:8]	Reserved	0
HDCP_B_INIT_RND7	[7:0]	HDCP B initial value[63:56]	0xC4

Table 11-168 HDCP B INITIAIL VALUE Register (HDCP_B_INIT_RND8)

Register	Address	Type	Description	Reset Value
HDCP_B_INIT_RN_D8	Base+0x0534	W	HDCP B initial value[64]	0x0000_0001

HDCP_B_INIT_RND8	Bit	Description	Initial State
-	[31:1]	Reserved	0
HDCP_B_INIT_RND8	[0]	HDCP B initial value[64]	0x01

Table 11-169 HDCP K INITIAIL VALUE Register (HDCP_K_INIT_RND0)

Register	Address	Type	Description	Reset Value
HDCP_K_INIT_RN_D0	Base+0x0538	W	HDCP K initial value[7:0]	0x0000_001c

HDCP_K_INIT_RND0	Bit	Description	Initial State
-	[31:8]	Reserved	0
HDCP_K_INIT_RND0	[7:0]	HDCP K initial value[7:0]	0x01

Table 11-170 HDCP K INITIAIL VALUE Register (HDCP_K_INIT_RND1)

Register	Address	Type	Description	Reset Value
HDCP_K_INIT_RN_D1	Base+0x053C	W	HDCP K initial value[15:8]	0x0000_00C3

HDCP_K_INIT_RND1	Bit	Description	Initial State
-	[31:8]	Reserved	0
HDCP_K_INIT_RND1	[7:0]	HDCP K initial value[15:8]	0xC3

Table 11-171 HDCP K INITIAIL VALUE Register (HDCP_K_INIT_RND2)

Register	Address	Type	Description	Reset Value
HDCP_K_INIT_RN_D2	Base+0x0540	W	HDCP K initial value[23:16]	0x0000_00F6

HDCP_K_INIT_RND2	Bit	Description	Initial State
-	[31:8]	Reserved	0
HDCP_K_INIT_RND2	[7:0]	HDCP K initial value[23:16]	0xF6

Table 11-172 HDCP K INITIAIL VALUE Register (HDCP_K_INIT_RND3)

Register	Address	Type	Description	Reset Value
HDCP_K_INIT_RN_D3	Base+0x0544	W	HDCP K initial value[31:24]	0x0000_00E5

HDCP_K_INIT_RND3	Bit	Description	Initial State
-	[31:8]	Reserved	0
HDCP_K_INIT_RND3	[7:0]	HDCP K initial value[31:24]	0xE5

Table 11-173 HDCP K INITIAIL VALUE Register (HDCP_K_INIT_RND4)

Register	Address	Type	Description	Reset Value
HDCP_K_INIT_RN_D4	Base+0x0548	W	HDCP K initial value[39:32]	0x0000_00C3

HDCP_K_INIT_RND4	Bit	Description	Initial State
-	[31:8]	Reserved	0
HDCP_K_INIT_RND4	[7:0]	HDCP K initial value[39:32]	0xC3

Table 11-174 HDCP K INITIAIL VALUE Register (HDCP_K_INIT_RND5)

Register	Address	Type	Description	Reset Value
HDCP_K_INIT_RN_D5	Base+0x054C	W	HDCP K initial value[47:40]	0x0000_00E7

HDCP_K_INIT_RND5	Bit	Description	Initial State
-	[31:8]	Reserved	0
HDCP_K_INIT_RND5	[7:0]	HDCP K initial value[47:40]	0xE7

Table 11-175 HDCP K INITIAIL VALUE Register (HDCP_K_INIT_RND6)

Register	Address	Type	Description	Reset Value
HDCP_K_INIT_RN_D6	Base+0x0550	W	HDCP K initial value[55:48]	0x0000_00DF

HDCP_K_INIT_RND6	Bit	Description	Initial State
-	[31:8]	Reserved	0
HDCP_K_INIT_RND6	[7:0]	HDCP K initial value[55:48]	0xDF

Table 11-176 HDCP K INITIAIL VALUE Register (HDCP_K_INIT_RND7)

Register	Address	Type	Description	Reset Value
HDCP_K_INIT_RN D7	Base+0x0 554	W	HDCP K initial value[63:56]	0x0000_00 D6

HDCP_K_INIT_RND7	Bit	Description	Initial State
-	[31:8]	Reserved	0
HDCP_K_INIT_RND7	[7:0]	HDCP K initial value[63:56]	0xD6

Table 11-177 HDCP K INITIAIL VALUE Register (HDCP_K_INIT_RND8)

Register	Address	Type	Description	Reset Value
HDCP_K_INIT_RN D8	Base+0x0 558	W	HDCP K initial value[71:64]	0x0000_00 D7

HDCP_K_INIT_RND8	Bit	Description	Initial State
-	[31:8]	Reserved	0
HDCP_K_INIT_RND8	[7:0]	HDCP K initial value[71:64]	0xD7

Table 11-178 HDCP K INITIAIL VALUE Register (HDCP_K_INIT_RND9)

Register	Address	Type	Description	Reset Value
HDCP_K_INIT_RN D9	Base+0x0 55C	W	HDCP K initial value[79:72]	0x0000_00 6E

HDCP_K_INIT_RND9	Bit	Description	Initial State
-	[31:8]	Reserved	0
HDCP_K_INIT_RND9	[7:0]	HDCP K initial value[79:72]	0x6E

Table 11-179 HDCP K INITIAIL VALUE Register (HDCP_K_INIT_RND10)

Register	Address	Type	Description	Reset Value
HDCP_K_INIT_RN D10	Base+0x0 560	W	HDCP K initial value[83:80]	0x0000_00 01

HDCP_K_INIT_RND10	Bit	Description	Initial State
-	[31:8]	Reserved	0
HDCP_K_INIT_RND10	[7:0]	HDCP K initial value[83:80]	0x01

Register Definition for DisplayPort Function

Table 11-180 System Control Register #1 (SYS_CTL_1)

Register	Address	Type	Description	Reset Value
SYS_CTL_1	Base + 0x0600	R/W	System Control Register #1.	0x0000_00 00

SYS_CTL_1	Bit	Description	Initial State

-	[31:5]	Reserved	0
HBR2_EYE_SY_CTRL	[4:3]	HBR2 pattern control	0
DET_STA	[2]	Video stream clock detect status, It will not affect video output. 1: Stream clock detected 0: Stream clock not detected Write any value to update the current status.	0
FORCE_DET	[1]	Force video stream clock detect, this bit is only active when DET_CTRL is 1 1: Force video stream clock detected 0: Force video stream clock not detected This bit's type is R/W.	0
DET_CTRL	[0]	Video stream clock detect status control: 1: Use force detect status 0: Use auto-detected status This bit's type is R/W.	0

Table 11-181 DP System Control Register #2 (SYS_CTL_2)

Register	Address	Type	Description	Reset Value
SYS_CTL_2	Base + 0x0604	R/W	System Control Register #2	0x0000_0040

SYS_CTL_2	Bit	Description	Initial State
-	[31:8]	Reserved	0
CHA_CRI	[7:4]	Pixel clock change detection threshold. The incoming pixel clock input is counted continuously by the 24Mhz reference clock. This register defines a number, if the counter number change is more than this value for 2 pixel clock edges, the CHA_STA bit is asserted. This bit's type is R/W.	4
-	[3]	Reserved	0
CHA_STA	[2]	Video stream clock change status, It will not affect video output 1: Clock frequency changed 0: Clock frequency not changed Write any value to update the current status.	0
FORCE_CHA	[1]	Force stream clock change status, this bit only active when CHA_CTRL is 1 1: Force clock change. When asserted, CHA_STA is '1'. 0: Force clock not change This bit's type is R/W.	0
CHA_CTRL	[0]	Pixel clock frequency change status control 1: Use force change status 0: Use auto-detected status This bit's type is R/W.	0

Table 11-182 DP System Control Register #3 (SYS_CTL_3)

Register	Address	Type	Description	Reset Value
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SYS_CTL_3	Base + 0x0608	R/W, RO	System Control Register #3.	0x0000_0000
SYS_CTL_3	Bit	Description	Initial State	
-	[31:7]	Reserved	0	
HPD_STATUS(RO)	[6]	<p>Hot plug detect status. 1: HPD is 1, 0: HPD is 0. This bit's type is RO. When this bit is 0, AUX CH will not work. Note that the HPD_STATUS is only changed after the change of the pin I_DP_HPD remains for no less than hot plug deglitch time. And the hot plug deglitch time is defined in HPD_DEGLITCH_L and HPD_DEGLITCH_H.</p>	0	
F_HPD	[5]	<p>Force hot plug detect. 1: Force HPD 1, 0: Force HPD 0. This bit's type is R/W.</p>	0	
HPD_CTRL	[4]	<p>Hot plug detect manual control. 1: Force HPD with F_HPD, 0: Use PIN_HPD state. This bit's type is R/W.</p>	0	
HDCP_RDY(RO)	[3]	<p>HDCP ready status. 1: HDCP is ready, 0: HDCP is not ready. This bit's type is RO. This bit is an indicator of whether HDCP is ready to perform. Usually, it is set as soon as HPD signal is detected as plugged.</p>	0	
STRM_VALID	[2]	<p>Input stream have constant video format, and this stream is valid to send out through link. 1: Input stream is valid, 0: Input stream is not valid. Write any value to update the current status. Hardware will not send out video through link when this bit is 0.</p>	0	
F_VALID	[1]	<p>Force stream valid, this bit only active when VALID_CTRL is 1. 1: Force input video stream valid, 0: Force input video stream not valid. This bit's type is R/W.</p>	0	
VALID_CTRL	[0]	<p>Stream valid control. 1: Use F_VALID bit to control video stream valid status 0: Use video stream valid auto-detect This bit's type is R/W.</p>	0	

Table 11-183 DP System Control Register #4 (SYS_CTL_4)

Register	Address	Type	Description	Reset Value

SYS_CTL_4	Base + 0x060C	R/W	System Control Register #2.	0x0000_0000
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SYS_CTL_4	Bit	Description	Initial State
-	[31:5]	Reserved	0
FIX_M_AUD	[4]	Fix M_AUD value 1: Use register M_AUD value to be sent out, 0: Use calculates M_AUD value to be sent out.	0
ENHANCED	[3]	DisplayPort Enhanced mode enable 1: Enhanced mode, 0: Normal mode.	0
FIX_M_VID	[2]	Fix M_VID value 1: Use register M_VID value to be sent out, 0: Use calculates M_VID value to be sent out.	0
M_VID_UPDATE_CTRL	[1:0]	Control M_VID update frequency 11: 1/8 X update rate, 10: 1/4 X update rate, 01: 1/2 X update rate, 00: Normal rate.	0

Table 11-184 DP Video Control Register (DP_VID_CTL)

Register	Address	Type	Description	Reset Value
DP_VID_CTL	Base + 0x0610	RO	DP Video Control Register	0x0000_0020

DP_VID_CTL	Bit	Description	Initial State
-	[31:8]	Reserved	0
BPC	[7:5]	Bit per color/ component with video which transferred via DP main link 101, 110, 111, 100: Reserved, 011: 12 bits, 010: 10 bits, 001: 8 bits, 000: 6 bits.	1
YC_COEFF	[4]	YcbCr Coefficients with video which transferred via DP main link 1: ITU709, 0: ITU601.	0
D_RANGE	[3]	Dynamic range 1: CEA range, 0: VESA range (from 0 to the maximum).	0
COLOR_F	[2:1]	Colorimetric format with video which transferred via DP main link 11: Reserved, 10: YcbCr444, 01: YcbCr422, 00: RGB.	0
-	[0]	Reserved	0

Table 11-185 DP Audio Control Register (DP_AUD_CTL)

Register	Address	Type	Description	Reset Value
DP_AUD_CTL	Base + 0x0618	R/W	DP Audio Control Register.	0x0000_0000

DP_AUD_CTL	Bit	Description	Initial State
-	[31:5]	Reserved	0
MISC_CTRL_RESET	[4]		0
-	[3]	Reserved	0
DP_AUDIO_REF_CLK_SEL	[2:1]	00: 11: 10: 11:	0
DP_AUDIO_EN	[0]	This register enables to send the audio stream via main link. 1: Enable 0: Disable.	0

Table 11-186 Packet Send Control Register (PKT_SEND_CTL)

Register	Address	Type	Description	Reset Value
PKT_SEND_CTL	Base + 0x0640	R/W	Packet Send Control Register.	0x0000_0000

PKT_SEND_CTL	Bit	Description	Initial State
-	[31:8]	Reserved	0
AUDIO_INFO_UP(C)	[7]	Audio InfoFrame content has been updated. 1: Updated, 0: Don't care. Write 1 to this bit after Audio Packet Content Registers have been configured as Audio InfoFrame content has been updated. This bit's type is R/W. This bit is self cleared after the register configured content has been used to update the InfoFrame.	0
AVI_INFO_UP(C)	[6]	AVI InfoFrame content has been updated. 1: Updated, 0: Don't care. Write 1 to this bit after AVI Packet Content Registers have been configured as AVI InfoFrame content has been updated. This bit's type is R/W. This bit is self cleared after the register configured content has been used to update the InfoFrame.	0
MPEG_INFO_UP(C)	[5]	MPEG InfoFrame content has been updated. 1: Updated, 0: Don't care. Write 1 to this bit after MPEG Packet Content Registers have been configured as MPEG InfoFrame content has been updated. This bit's type is R/W. This bit is self cleared after the register configured content has been used to update the InfoFrame.	0

PKT_SEND_CTL	Bit	Description	Initial State
IF_UP(C)	[4]	Configurable InfoFrame content has been updated. 1: Updated, 0: Don't care. Write 1 to this bit after IF_TYPE and IF_PKT_DB1~25 Registers have been configured as configurable InfoFrame content have been updated. This bit's type is R/W. This bit is self cleared after the register configured content has been used to update the InfoFrame.	0
AUDIO_INFO_EN	[3]	Audio InfoFrame send enable. 1: Send Audio InfoFrame, 0: Don't send Audio InfoFrame. Make sure that the Audio Packet Content Registers had been configured correctly and the AUDIO_INFO_UP had been written with 1. This bit's type is R/W.	0
AVI_INFO_EN	[2]	AVI InfoFrame send enable. 1: Send AVI InfoFrame, 0: Don't send AVI InfoFrame. Make sure that the AVI Packet Content Registers had been configured correctly and the AVI_INFO_UP had been written with 1. This bit's type is R/W.	0
MPEG_INFO_EN	[1]	MPEG InfoFrame send enable. 1: Send MPEG InfoFrame, 0: Don't send MPEG InfoFrame. Make sure that the MPEG Packet Content Registers had been configured correctly and the MPEG_INFO_UP had been written with 1. This bit's type is R/W.	0
IF_EN	[0]	Configurable InfoFrame send enable. 1: Send InfoFrame defined in IF_TYPE and IF_PKT_DB1~25, 0: Don't send InfoFrame. Make sure that the IF_TYPE and IF_PKT_DB1~25 Registers had been configured correctly and the IF_UP had been written with 1. This bit's type is R/W.	0

Table 11-187 DisplayPort HDCP Control Register (DP_HDCP_CTL)

Register	Address	Type	Description	Reset Value
DP_HDCP_CTL	Base + 0x0648	R/W	DisplayPort HDCP Control Register.	0x0000_0000

DP_HDCP_CTL	Bit	Description	Initial State
-	[31:7]	Reserved	0

HDCP_HPD_RST	[6]	HDCP block reset control. 0: No reset for HDCP block when HPD is low, 1: Reset HDCP when HPD is low.	0
-	[5:2]	Reserved	0
LINK_CHECK_MODE	[1]	HDCP link integrity check mode: 1 = HDCP polling link integrity check status, and re-start HDCP Authentication automatically when detected link integrity check fail; 0 = HDCP don't polling link integrity check status.	0
HW_HDCP_INT(C)	[0]	The DP receiver initiates a HDCP interrupt through Hot Plug Detect Pin to DP transmitter whenever DP receiver finds R0' calculation done, downstream KSV list is ready and V' calculation done, or HDCP link integrity check failure. A firmware on DP transmitter must set this bit to 1 in order to make H/W HDCP authentication module do some proper action when firmware of DP transmitter find it out that the interrupt about HDCP. This bit is self cleared.	0

Table 11-188 SPDIF Phase 1 Control Register (SPDIF_PHASE1_CTL_0)

Register	Address	Type	Description	Reset Value
SPDIF_PHASE1_CTL_0	Base + 0x0650	R/W	This register control SPDIF 1 cycle phase counter value [7:0]	0x0000_0000

SPDIF_PHASE1_CTL_0	Bit	Description	Initial State
-	[31:8]	Reserved	0
SPDIF_PHASE1_CTL_0	[7:0]	This register control SPDIF 1 cycle phase counter value [7:0], if bit SPDIF_PHASE1_CTL_EN is 0, the 1 cycle phase counter value [7:0] is read out. If the register SPDIF_PHASE1_CTL_EN is 1, firmware can force this value by writing data to this register. The bits can be read only when SPDIF_STREAM_DET is one. SPDIF_PHASE1_CTL should be set as Fs_clk / (32*audio_frequency * AudioChannelNum * 2). Here 2 are for biphase encoding and 32 is for each sub frame. For example if audio_frequency is 44.1KHz, Audio Channel Number is 2 and Fs_clk frequency is 135M Hz. $135,000,000 / (32*44,100*2*2) = 23.9$. SPDIF_PHASE1_CTL should set to 24.	0

Table 11-189 SPDIF Phase 1 Control ENABLE Register 0 (SPDIF_PHASE1_CTL_1)

Register	Address	Type	Description	Reset Value
SPDIF_PHASE1_CTL_1	Base + 0x0654	R/W	This register enables force of the 1 cycle phase counter value [8]	0x0000_0000

SPDIF_PHASE1_CTL_1	Bit	Description	Initial State
-	[31:8]	Reserved	0
SPDIF_PHASE1_CTL_EN	[7]	This register enables force of the 1 cycle phase counter value function. 0: SPDIF 1 cycle phase counter value use chip counted value. 1: SPDIF 1 cycle phase counter value use the data written to register SPDIF_PHASE1_CTL_0 and SPDIF_PHASE1_CTL_1.	0
-	[6:1]	Reserved	0
SPDIF_PHASE1_CTL_1	[0]	This register control SPDIF 1 cycle phase counter value [8], if bit PHASE_1_CONTROL_EN is 0, the 1 cycle phase counter value [8] is read out. If the register SPDIF_PHASE1_CTL_EN is 1, firmware can force this value by writing data to this register.	0

Table 11-190 SPDIF Phase 2 Control Register 0 (SPDIF_PHASE2_CTL_0)

Register	Address	Type	Description	Reset Value
SPDIF_PHASE2_CTL_0	Base + 0x0658	R/W	This register control SPDIF 2 cycle phase counter value [7:0]	0x0000_0000

SPDIF_PHASE2_CTL_0	Bit	Description	Initial State
-	[31:8]		0
SPDIF_PHASE2_CTL_0	[7:0]	This register control SPDIF 2 cycle phase counter value [7:0], if bit SPDIF_PHASE2_CTL_EN is 0, the 2 cycle phase counter value [7:0] is read out. If the register SPDIF_PHASE2_CTL_EN is 1, firmware can force this value by writing data to this register. The bits can be read only when SPDIF_STREAM_DET is one. SPDIF_PHASE2_CTL should be set as $2 * \text{Fs}_\text{clk} / (32 * \text{audio_frequency} * \text{AudioChannelNum} * 2)$. Here 2 are for biphase encoding and 32 is for each sub frame. For example if audio_frequency is 44.1KHz, Audio Channel Number is 2 and Fs_clk frequency is 135M Hz. $2 * 135,000,000 / (32 * 44,100 * 2 * 2) = 47.8$. SPDIF_PHASE2_CTL should set to 48.	0

Table 11-191 SPDIF Phase 2 Control Register 1 (SPDIF_PHASE2_CTL_1)

Register	Address	Type	Description	Reset Value
SPDIF_PHASE2_CTL_1	Base + 0x065C	R/W	This register control SPDIF 2 cycle phase counter value [8]	0x0000_0000

SPDIF_PHASE2_CTL_1	Bit	Description	Initial State
-	[31:8]	Reserved	0
SPDIF_PHASE2_CTL_EN	[7]	This register enables force of the 2 cycle phase counter value function. 0: SPDIF 2 cycle phase counter value use chip counted value. 1: SPDIF 2 cycle phase counter value use the data written to register SPDIF_PHASE2_CTL_0 and SPDIF_PHASE2_CTL_1.	0
-	[6:1]	Reserved	0
SPDIF_PHASE2_CTL_1	[0]	This register control SPDIF 2 cycle phase counter value [8], if bit SPDIF_PHASE2_CTL_EN is 0, the 2 cycle phase counter value [8] is read out. If the register SPDIF_PHASE2_CTL_EN is 1, firmware can force this value by writing data to this register.	0

Table 11-192 SPDIF Phase 3 Control Register 0 (SPDIF_PHASE3_CTL_0)

Register	Address	Type	Description	Reset Value
SPDIF_PHASE3_CTL_0	Base + 0x0660	R/W	This register control SPDIF 3 cycle phase counter value [7:0]	0x0000_0000

SPDIF_PHASE3_CTL_0	Bit	Description	Initial State
-	[31:0]	Reserved	0
SPDIF_PHASE3_CTL_0	[7:0]	This register control SPDIF 3 cycle phase counter value [7:0], if bit SPDIF_PHASE3_CTL_EN is 0, the 3 cycle phase counter value [7:0] is read out. If the register SPDIF_PHASE3_CTL_EN is 1, firmware can force this value by writing data to this register. The bits can be read only when SPDIF_STREAM_DET is one. SPDIF_PHASE3_CTL should be set as $3 * \text{Ils_clk} / (\text{32} * \text{audio_frequency} * \text{AudioChannelNum} * 2)$. Here 2 are for biphasic encoding and 32 is for each sub frame. For example if audio_frequency is 44.1KHz, Audio Channel Number is 2 and ls_clk frequency is 135M Hz. $3 * 135,000,000 / (32 * 44,100 * 2 * 2) = 71.7$. SPDIF_PHASE3_CTL should be set to 72.	0

Table 11-193 SPDIF Phase 3 Control Register 1 (SPDIF_PHASE3_CTL_1)

Register	Address	Type	Description	Reset Value
SPDIF_PHASE3_CTL_1	Base + 0x0664	R/W	This register control SPDIF 3 cycle phase counter value [8]	0x0000_0000

SPDIF_PHASE3_CTL_1	Bit	Description	Initial State
-	[31:8]	Reserved	0
SPDIF_PHASE3_CTL_EN	[7]	This register enables force of the 3 cycle phase counter value function. 0: SPDIF 3 cycle phase counter value use chip counted value. 1: SPDIF 3 cycle phase counter value use the data written to register SPDIF_PHASE3_CTL_0 and SPDIF_PHASE3_CTL_1.	0
-	[6:1]	Reserved	0
SPDIF_PHASE3_CTL_1	[0]	This register control SPDIF 3 cycle phase counter value [8], if bit SPDIF_PHASE3_CTL_EN is 0, the 3 cycle phase counter value [8] is read out. If the register SPDIF_PHASE3_CTL_EN is 1, firmware can force this value by writing data to this register.	0

Table 11-194 DP Main Link Bandwidth Setting Register (LINK_BW_SET)

Register	Address	Type	Description	Reset Value
LINK_BW_SET	Base + 0x0680	R/W	Main link bandwidth setting	0x0000_000A

LINK_BW_SET	Bit	Description	Initial State
-	[31:4]	Reserved	0
LINK_BW_SET	[3:0]	Main link bandwidth setting: 0x06: 1.62Gpbs per lane 0xa: 2.7Gpbs per lane other: Reserved	A

Table 11-195 DP Main Link Lane Count Register (LANE_COUNT_SET)

Register	Address	Type	Description	Reset Value
LANE_COUNT_SET	Base + 0x0684	R/W	Main link lane count	0x0000_0004

LANE_COUNT_SET	Bit	Description	Initial State
-	[31:3]	Reserved	0
LANE_COUNT_SET	[2:0]	Main link lane count 0x1: one lane 0x2: two lanes 0x4:four lanes other: Reserved	4

Table 11-196 DP Training Pattern Set Register (DP_TRAINING_PTN_SET)

Register	Address	Type	Description	Reset Value
DP_TRAINING_PTN_SET	Base + 0x0688	R/W	DP Training Pattern Set Register	0x0000_0000

DP_TRAINING_PTN_SE	Bit	Description	Initial State
-	[31:6]	Reserved	0
SCRAMBLING_DISABLE	[5]	Disable scramble 1: Disable 0: Normal operation	0
LINK_QUAL_PATTERN_SET	[4:2]	Link quality pattern setting. 101 = HBR2 Compliance 100 = 80 bit test pattern 011 = PRBS 7 bit 010 = symbol error rate measurement pattern is sent; 001 = D10.2 test pattern is sent; 000= link quality test pattern not sent	0
SW_TRAINING_PATTERN_SET	[1:0]	Link training pattern setting. SW_TRAINING_PATTERN_SET has higher priority than LINK_QUAL_PATTERN_SET. 11: Reserved 10: Sending training pattern 2 01: Sending training pattern 1 00: Training pattern not sent	0

Table 11-197 DP Lane 0 Link Training Control Register (DP_LN0_LINK_TRAINING_CTL)

Register	Address	Type	Description	Reset Value
DP_LN0_LINK_TRAINING_CTL	Base + 0x068C	R/W, RO	DP Lane 0 Link Training Control Register.	0x0000_0000

DP_LN0_LINK_TRAINING_CTL	Bit	Description	Initial State
-	[31:6]	Reserved	0

DP_LN0_LINK_TRAINING_CTL	Bit	Description	Initial State																																	
MAX_PRE_REACH_0(RO)	[5]	<p>This bit field is set to 1 automatically when max pre-emphasis level of DP Tx is reached. This bit's type is RO.</p> <p>Note that the MAX_PRE_REACH_0 and MAX_DRIVE_REACH_0 have the same value like the following table.</p> <table border="1"> <thead> <tr> <th colspan="2"></th> <th colspan="4">Pre-emphasis (dB)</th> </tr> <tr> <th colspan="2"></th> <th>0</th> <th>3.5</th> <th>6.0</th> <th>9.5</th> </tr> </thead> <tbody> <tr> <td rowspan="4">Driving Current (mV)</td> <td>400</td> <td>0</td> <td>0</td> <td>0</td> <td>1</td> </tr> <tr> <td>600</td> <td>0</td> <td>0</td> <td>1</td> <td>1</td> </tr> <tr> <td>800</td> <td>0</td> <td>1</td> <td>1</td> <td>1</td> </tr> <tr> <td>1200</td> <td>1</td> <td>1</td> <td>1</td> <td>1</td> </tr> </tbody> </table> <p>Both of MAX_PRE_REACH_0 and MAX_DRIVE_REACH_0 are for test purpose only.</p>			Pre-emphasis (dB)						0	3.5	6.0	9.5	Driving Current (mV)	400	0	0	0	1	600	0	0	1	1	800	0	1	1	1	1200	1	1	1	1	0
		Pre-emphasis (dB)																																		
		0	3.5	6.0	9.5																															
Driving Current (mV)	400	0	0	0	1																															
	600	0	0	1	1																															
	800	0	1	1	1																															
	1200	1	1	1	1																															
PRE_EMPHASIS_SET_0	[4:3]	<p>Lane 0 pre-emphasis level setting</p> <p>11: 9.5 dB, 10: 6.0 dB, 01: 3.5 dB, 00: 0 dB (No pre-emphasis).</p> <p>This bit's type is R/W.</p>	0																																	
MAX_DRIVE_REACH_0(RO)	[2]	<p>This bit field is set to 1 automatically when max driving current level of DP Tx is reached. For test purpose only. This bit's type is RO. For more information, refer to MAX_PRE_REACH_0.</p>	0																																	
DRIVE_CURRENT_SET_0	[1:0]	<p>Lane 0 output amplitude setting</p> <p>11: 1200 mV, 10: 800 mV, 01: 600 mV, 00: 400 mV.</p> <p>This bit's type is R/W.</p>	0																																	

Table 11-198 DP Lane 1 Link Training Control Register (DP_LN1_LINK_TRAINING_CTL)

Register	Address	Type	Description	Reset Value
DP_LN1_LINK_TRAINING_CTL	Base + 0x0690	R/W, RO	DP Lane 1 Link Training Control Register.	0x0000_0000

DP_LN1_LINK_TRAINING_CTL	Bit	Description	Initial State
-	[31:6]	Reserved	0

DP_LN1_LINK_TRAINING_CTL	Bit	Description	Initial State																																	
MAX_PRE_REACH_1(RO)	[5]	<p>This bit field is set to 1 automatically when max pre-emphasis level of DP Tx is reached. Note that the MAX_PRE_REACH_1 and MAX_DRIVE_REACH_1 have the same value like the following table.</p> <table border="1"> <thead> <tr> <th colspan="2"></th> <th colspan="4">Pre-emphasis (dB)</th> </tr> <tr> <th colspan="2"></th> <th>0</th> <th>3.5</th> <th>6.0</th> <th>9.5</th> </tr> </thead> <tbody> <tr> <td rowspan="4">Driving Current (mV)</td> <td>400</td> <td>0</td> <td>0</td> <td>0</td> <td>1</td> </tr> <tr> <td>600</td> <td>0</td> <td>0</td> <td>1</td> <td>1</td> </tr> <tr> <td>800</td> <td>0</td> <td>1</td> <td>1</td> <td>1</td> </tr> <tr> <td>1200</td> <td>1</td> <td>1</td> <td>1</td> <td>1</td> </tr> </tbody> </table> <p>Both of MAX_PRE_REACH_1 and MAX_DRIVE_REACH_1 are for test purpose only. This bit's type is RO.</p>			Pre-emphasis (dB)						0	3.5	6.0	9.5	Driving Current (mV)	400	0	0	0	1	600	0	0	1	1	800	0	1	1	1	1200	1	1	1	1	0
		Pre-emphasis (dB)																																		
		0	3.5	6.0	9.5																															
Driving Current (mV)	400	0	0	0	1																															
	600	0	0	1	1																															
	800	0	1	1	1																															
	1200	1	1	1	1																															
PRE_EMPHASIS_SET_1	[4:3]	<p>Lane 1 pre-emphasis level setting 11: 9.5 dB, 10: 6.0 dB, 01: 3.5 dB, 00: 0 dB (No pre-emphasis). This bit's type is R/W.</p>	0																																	
MAX_DRIVE_REACH_1(RO)	[2]	<p>This bit field is set to 1 automatically when max driving current level of DP Tx is reached. For more information, refer to MAX_PRE_REACH_1. For test purpose only. This bit's type is RO.</p>	0																																	
DRIVE_CURRENT_SET_1	[1:0]	<p>Lane 1 output amplitude setting 11: 1200 mV, 10: 800 mV, 01: 600 mV, 00: 400 mV. This bit's type is R/W.</p>	0																																	

Table 11-199 DP Lane 2 Link Training Control Register (DP_LN2_LINK_TRAINING_CTL)

Register	Address	Type	Description	Reset Value
DP_LN2_LINK_TRAINING_CTL	Base + 0x0694	R/W, RO	DP Lane 2 Link Training Control Register.	0x0000_0000

DP_LN2_LINK_TRAINING_CTL	Bit	Description	Initial State
-	[31:6]	Reserved	0

DP_LN2_LINK_TRAINING_CTL	Bit	Description	Initial State																																	
MAX_PRE_REACH_2(RO)	[5]	<p>This bit field is set to 1 automatically when max pre-emphasis level of DP Tx is reached. Note that the MAX_PRE_REACH_2 and MAX_DRIVE_REACH_2 have the same value like the following table.</p> <table border="1"> <thead> <tr> <th colspan="2"></th> <th colspan="4">Pre-emphasis (dB)</th> </tr> <tr> <th colspan="2"></th> <th>0</th> <th>3.5</th> <th>6.0</th> <th>9.5</th> </tr> </thead> <tbody> <tr> <td rowspan="4">Driving Current (mV)</td> <td>400</td> <td>0</td> <td>0</td> <td>0</td> <td>1</td> </tr> <tr> <td>600</td> <td>0</td> <td>0</td> <td>1</td> <td>1</td> </tr> <tr> <td>800</td> <td>0</td> <td>1</td> <td>1</td> <td>1</td> </tr> <tr> <td>1200</td> <td>1</td> <td>1</td> <td>1</td> <td>1</td> </tr> </tbody> </table> <p>Both of MAX_PRE_REACH_1 and MAX_DRIVE_REACH_2 are for test purpose only. This bit's type is RO.</p>			Pre-emphasis (dB)						0	3.5	6.0	9.5	Driving Current (mV)	400	0	0	0	1	600	0	0	1	1	800	0	1	1	1	1200	1	1	1	1	0
		Pre-emphasis (dB)																																		
		0	3.5	6.0	9.5																															
Driving Current (mV)	400	0	0	0	1																															
	600	0	0	1	1																															
	800	0	1	1	1																															
	1200	1	1	1	1																															
PRE_EMPHASIS_SET_2	[4:3]	<p>Lane 2 pre-emphasis level setting 11: 9.5 dB, 10: 6.0 dB, 01: 3.5 dB, 00: 0 dB (No pre-emphasis). This bit's type is R/W.</p>	0																																	
MAX_DRIVE_REACH_2(RO)	[2]	<p>This bit field is set to 1 automatically when max driving current level of DP Tx is reached. For more information, refer to MAX_PRE_REACH_2. For test purpose only. This bit's type is RO.</p>	0																																	
DRIVE_CURRENT_SET_2	[1:0]	<p>Lane 2 output amplitude setting 11: 1200 mV, 10: 800 mV, 01: 600 mV, 00: 400 mV. This bit's type is R/W.</p>	0																																	

Table 11-200 DP Lane 3 Link Training Control Register (DP_LN3_LINK_TRAINING_CTL)

Register	Address	Type	Description	Reset Value
DP_LN3_LINK_TRAINING_CTL	Base + 0x0698	R/W, RO	DP Lane 3 Link Training Control Register.	0x0000_0000

DP_LN3_LINK_TRAINING_CTL	Bit	Description	Initial State
-	[31:6]	Reserved	0

DP_LN3_LINK_TRAINING_CTL	Bit	Description	Initial State																																				
MAX_PRE_REACH_3(RO)	[5]	<p>This bit field is set to 1 automatically when max pre-emphasis level of DP Tx is reached. Note that the MAX_PRE_REACH_3 and MAX_DRIVE_REACH_3 have the same value like the following table.</p> <table border="1"> <thead> <tr> <th colspan="2"></th> <th colspan="4">Pre-emphasis (dB)</th> </tr> <tr> <th colspan="2"></th> <th>0</th> <th>3.5</th> <th>6.0</th> <th>9.5</th> </tr> </thead> <tbody> <tr> <td>Driving Current (mV)</td> <td>400</td> <td>0</td> <td>0</td> <td>0</td> <td>1</td> </tr> <tr> <td></td> <td>600</td> <td>0</td> <td>0</td> <td>1</td> <td>1</td> </tr> <tr> <td></td> <td>800</td> <td>0</td> <td>1</td> <td>1</td> <td>1</td> </tr> <tr> <td></td> <td>1200</td> <td>1</td> <td>1</td> <td>1</td> <td>1</td> </tr> </tbody> </table> <p>Both of MAX_PRE_REACH_3 and MAX_DRIVE_REACH_3 are for test purpose only. This bit's type is RO.</p>			Pre-emphasis (dB)						0	3.5	6.0	9.5	Driving Current (mV)	400	0	0	0	1		600	0	0	1	1		800	0	1	1	1		1200	1	1	1	1	0
		Pre-emphasis (dB)																																					
		0	3.5	6.0	9.5																																		
Driving Current (mV)	400	0	0	0	1																																		
	600	0	0	1	1																																		
	800	0	1	1	1																																		
	1200	1	1	1	1																																		
PRE_EMPHASIS_SET_3	[4:3]	<p>Lane 3 pre-emphasis level setting 11: 9.5 dB, 10: 6.0 dB, 01: 3.5 dB, 00: 0 dB (No pre-emphasis). This bit's type is R/W.</p>	0																																				
MAX_DRIVE_REACH_3(RO)	[2]	<p>This bit field is set to 1 automatically when max driving current level of DP Tx is reached. For more information, refer to MAX_PRE_REACH_3. For test purpose only. This bit's type is RO.</p>	0																																				
DRIVE_CURRENT_SET_3	[1:0]	<p>Lane 3 output amplitude setting 11: 1200 mV, 10: 800 mV, 01: 600 mV, 00: 400 mV. This bit's type is R/W.</p>	0																																				

Table 11-201 DP HW LINK TRAINING_CONTROL Register (DP_HW_LINK_TRAINING_CTL)

Register	Address	Type	Description	Reset Value
DP_HW_LINK_TRAINING_CTL	Base + 0x06A0	R/W, RO	DP hardware training control registers.	0x0000_0000

DP_HW_LINK_TRAINING_CTL	Bit	Description	Initial State
-	[31:7]	Reserved	0
HW_TRAINING_ERROR_CODE(RO)	[6:4]	<p>Training error code 0: OK 1: AUX_WRITE_ERROR 2: MAX_DRIVE_REACHED 3: WRONG_LANE_COUNT_SETTING 4: LOOP_SAME_5_TIME 5: CR_FAIL_IN_EQ 6: EQ_LOOP_5_TIME This bit's type is RO.</p>	0

DP_HW_LINK_TRAINING_CTL	Bit	Description	Initial State
-	[3:1]	Reserved	0
HW_TRAINING_EN(C)	[0]	Link training sequence enable Write 1 to enable training sequence, write 0 to force training sequence stop, this bit will self-clear when training done. This bit's type is R/W. This bit is self cleared.	0

Table 11-202 DP Debug Register Register #1 (DP_DEBUG_CTL)

Register	Address	Type	Description	Reset Value
DP_DEBUG_CTL	Base + 0x06C0	R/W, RO	DP Debug Control Register #1.	0x0000_0000

DP_DEBUG_CTL	Bit	Description	Initial State
-	[31:7]	Reserved	0
MYDP_HPD_POLLIN_EN	[6]	Enable the MYDP HPD status polling. If this bit and POLLING_EN are enabled and BYPASS_STATUS_POLLING is 0, hardware polling both of link status and MYDP HPD status. 1: Enabled 0: Disabled. This bit's type is RW.	0
BYPASS_STATUS_POLLING	[5]	Bypass link status polling. If this bit, MYDP_HPD_POLLIN_EN and POLLING_EN are all enabled, hardware only polling MYDP HPD status. 1: Enabled 0: Disabled. This bit's type is RW.	0
PLL_LOCK(RO)	[4]	PLL lock status 1: PLL lock, 0: PLL unlock. This bit's type is RO.	0
F_PLL_LOCK	[3]	Force PLL lock, this bit is active when PLL_LOCK_CTRL is 1: 1: Force PLL lock, 0: Force PLL non-lock. This bit's type is R/W	0
PLL_LOCK_CTRL	[2]	PLL lock register control enable 1: PLL lock signal is controlled by register, 0: PLL lock signal is controlled by PLL. This bit's type is R/W	0
POLLING_EN	[1]	Enable hardware state machine to polling the HPD status or link status. The interval of each polling is controlled by POLLING_PERIOD 1: Enable polling function. 0: Disable polling function This bit's type is R/W.	0

PN_INV	[0]	Invert SERDES output polarity 1: Invert output polarity, 0: Normal operation. This bit's type is R/W.	0
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Table 11-203 DP HPD De-glitch Low Byte Register (HPD_DEGLITCH_L)

Register	Address	Type	Description	Reset Value
HPD_DEGLITCH_L	Base + 0x06C4	R/W	HPD_DEGLITCH is used to de-glitch the HPD signal	0x0000_005E

HPD_DEGLITCH_L	Bit	Description	Initial State
-	[31:8]	Reserved	0
HPD_DEGLITCH_L	[7:0]	HPD_DEGLITCH, which is counted at 24 MHz, is used to de-glitch the HPD signal. This register is HPD_DEGLITCH [7:0]. The default value is 0x5E for 280.75 us deglitch time.	0x5E

Table 11-204 DP HPD De-glitch High Byte Register (HPD_DEGLITCH_H)

Register	Address	Type	Description	Reset Value
HPD_DEGLITCH_H	Base + 0x06C8	R/W	HPD_DEGLITCH is used to de-glitch the HPD signal	0x0000_001A

HPD_DEGLITCH_H	Bit	Description	Initial State
-	[31:6]	Reserved	0
HPD_DEGLITCH_H	[5:0]	HPD_DEGLITCH, which is counted at 24 MHz, is used to de-glitch the HPD signal. This register is HPD_DEGLITCH [13:8]. The default value is 0x1A for 280.75 us deglitch time.	0x1A

Table 11-205 DP POLLING_PERIOD Register (POLLING_PERIOD)

Register	Address	Type	Description	Reset Value
POLLING_PERIOD	Base + 0x06CC	R/W	POLLING_PERIOD	0x0000_00OE

POLLING_PERIOD	Bit	Description	Initial State
-	[31:8]	Reserved	0
POLLING_PERIOD	[7:0]	This register controls the interval between each time of polling operation. Interval time = POLLING_PERIOD * 2^16 * Period of 24M clock.	0xE

Table 11-206 DP Link Debug Control Register (DP_LINK_DEBUG_CTL)

Register	Address	Type	Description	Reset Value
DP_LINK_DEBUG_CTL	0x0000_06E0	R/W	DP Link Debug Control Register	0x0000_0010

DP_LINK_DEBUG_CTL	Bit	Description	Initial State
-	[31:5]	Reserved	0
NEW_PRBS7	[4]	Control the PRBS 7 formula. 1: Use new PRBS7 formula in DP 1.1 version 0: Use old PRBS7 formula in DP 1.0 version	1
DIS_FIFO_RST	[3]	Disable video FIFO reset every line 1: Disable, 0: Reset video FIFO every line.	0
DISABLE_AUTO_RESET_ENCODER	[2]	Disable 8b/10 encoder auto reset 1: Disabled auto reset 8b/10 encode before sending Link Training Pattern 2 0: Auto reset 8b/10 encode before sending Link Training Pattern 2	0
-	[1]	Reserved	0
PRBS31_EN	[0]	Enable DisplayPort PRBS 31. 1: Enabled, 0: Normal mode.	0

Table 11-207 DP SINK_COUNT Register (SINK_COUNT)

Register	Address	Type	Description	Reset Value
SINK_COUNT	Base + 0x06E4	RO	SINK_COUNT	0x0000_0000

SINK_COUNT	Bit	Description	Initial State
-	[31:8]	Reserved	0
SINK_COUNT	[7:0]	Sink Count	0x0

Table 11-208 DP IRQ_VECTOR Register (IRQ_VECTOR)

Register	Address	Type	Description	Reset Value
IRQ_VECTOR	Base + 0x06E8	RO	IRQ_VECTOR	0x0000_0000

IRQ_VECTOR	Bit	Description	Initial State
-	[31:8]	Reserved	0
IRQ_VECTOR	[7:0]	Irq_vector	0x0

Table 11-209 DP_LINK_STATUS0 Register (DP_LINK_STATUS0)

Register	Address	Type	Description	Reset Value
DP_LINK_STATUS0	Base + 0x06EC	RO	DP_LINK_STATUS0	0x0000_0000

DP_LINK_STATUS0	Bit	Description	Initial State
-	[31:7]	Reserved	0
LN1_SYMBOL_LOCK	[6]	Lane1 symbol lock	0x0
LN_EQ_DONE	[5]	Lane1 EQ done	0x0
LN_CR_DONE	[4]	Lane1 CR done	0x0
-	[3]	Reserved	0x0

LN0_SYMBOL_LOCK	[2]	Lane0 symbol lock	0x0
LN0_EQ_DONE	[1]	Lane0 EQ done	0x0
LN0_CR_DONE	[0]	Lane0 CR done	0x0

Table 11-210 DP_LINK_STATUS1 Register (DP_LINK_STATUS1)

Register	Address	Type	Description	Reset Value
DP_LINK_STATUS1	Base + 0x06F0	RO	DP_LINK_STATUS1	0x0000_0000

DP_LINK_STATUS1	Bit	Description	Initial State
-	[31:8]	Reserved	0
INTER_LN_ALIGN	[7]	Interlace align	0x0
LN3_SYMBOL_LOCK	[6]	Lane3 symbol lock	0x0
LN3_EQ_DONE	[5]	Lane3 EQ done	0x0
LN3_CR_DONE	[4]	Lane3 CR done	0x0
-	[3]	Reserved	0x0
LN2_SYMBOL_LOCK	[2]	Lane2 symbol lock	0x0
LN2_EQ_DONE	[1]	Lane2 EQ done	0x0
LN2_CR_DONE	[0]	Lane2 CR done	0x0

Table 11-211 DP ALIGN_STATUS Register (ALIGN_STATUS)

Register	Address	Type	Description	Reset Value
ALIGN_STATUS	Base + 0x06F4	RO	ALIGN_STATUS	0x0000_0000

ALIGN_STATUS	Bit	Description	Initial State
-	[31:8]	Reserved	0
ALIGN_STATUS	[7:0]	ALIGN_STATUS	0

Table 11-212 DP_DP_SINK_STATUS Register (DP_SINK_STATUS)

Register	Address	Type	Description	Reset Value
DP_SINK_STATUS	Base + 0x06F8	RO	DP_SINK_STATUS	0x0000_0000

DP_SINK_STATUS	Bit	Description	Initial State
-	[31:2]	Reserved	0
SINK_STA_1	[1]	Debug register	0
SINK_STA_0	[0]	Debug register	0

Table 11-213 M_VID Configure Register #0 (M_VID_0)

Register	Address	Type	Description	Reset Value
M_VID_0	Base + 0x0700	R/W	M_VID[7:0]	0x0000_0000

M_VID_0	Bit	Description	Initial State

-	[31:8]	Reserved	0
M_VID_0	[7:0]	M_VID [7:0]. If FIX_M_VID is 1, this M_VID is used. Otherwise the M_VID value which chip calculated is used	0

Table 11-214 DP M_VID Configure Register #1 (M_VID_1)

Register	Address	Type	Description	Reset Value
M_VID_1	Base + 0x0704	R/W	M_VID[15:8]	0x0000_0000

M_VID_1	Bit	Description	Initial State
-	[31:8]	Reserved	0
M_VID_1	[7:0]	M_VID [15:8]. If FIX_M_VID is 1, this M_VID is used. Otherwise the M_VID value which chip calculated is used	0

Table 11-215 DP M_VID Configure Register #2 (M_VID_2)

Register	Address	Type	Description	Reset Value
M_VID_2	Base + 0x0708	R/W	M_VID[23:16]	0x0000_0000

M_VID_2	Bit	Description	Initial State
-	[31:8]	Reserved	0
M_VID_2	[7:0]	M_VID [23:16]. If FIX_M_VID is 1, this M_VID is used. Otherwise the M_VID value which chip calculated is used	0

Table 11-216 DP N_VID Configure Register #0 (N_VID_0)

Register	Address	Type	Description	Reset Value
N_VID_0	Base + 0x070C	R/W	N_VID[7:0]	0x0000_0000

N_VID_0	Bit	Description	Initial State
-	[31:8]	Reserved	0
N_VID_0	[7:0]	N_VID[7:0] The maximum value of M_VID is 0xFFFF in ASYNC mode.	0

Table 11-217 DP N_VID Configure Register #1 (N_VID_1)

Register	Address	Type	Description	Reset Value
N_VID_1	Base + 0x0710	R/W	N_VID[15:8]	0x0000_0080

N_VID_1	Bit	Description	Initial State
-	[31:8]	Reserved	0
N_VID_1	[7:0]	N_VID[15:8]	0x80

Table 11-218 DP N_VID Configure Register #2 (N_VID_2)

Register	Address	Type	Description	Reset Value
N_VID_2	Base + 0x0714	R/W	N_VID[23:16]	0x0000_0000

N_VID_2	Base + 0x0714	R/W	N_VID[23:16]	0x0000_0000
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N_VID_2	Bit	Description	Initial State
-	[31:8]	Reserved	0
N_VID_2	[7:0]	N_VID[23:16]	0

Table 11-219 DP M_VID_MON register (M_VID_MON)

Register	Address	Type	Description	Reset Value
M_VID_MON	Base + 0x0718	RO	M_VID value monitoring register	0x0000_0000

M_VID_MON	Bit	Description	Initial State
-	[31:24]	Reserved	0
M_VID_MON	[23:0]	This register shows M_VID value which is actually transmitted to Rx for monitoring purpose.	0x0

Table 11-220 DP FIFO Threshold Register (DP_VIDEO_FIFO_THRD)

Register	Address	Type	Description	Reset Value
DP_VIDEO_FIFO_THRD	Base + 0x0730	R/W	DP Video Data FIFO Threshold Register	0x0000_0000

DP_VIDEO_FIFO_THRD	Bit	Description	Initial State
-	[31:5]	Reserved	0
VIDEO_TH_CTRL	[4]	Video Data FIFO threshold control enables. 1: Video Data FIFO threshold uses VIDEO_TH_VALUE. 0: Video Data FIFO threshold uses internal calculate value automatically.	0
VIDEO_TH_VALUE	[3:0]	Video Data FIFO threshold value. If VIDEO_TH_CTRL is 1, and data count in video data FIFO have reached FIFO threshold value, video data is read out from FIFO.	0

Table 11-221 DP GNS Control Register (DP_GNS_CTRL)

Register	Address	Type	Description	Reset Value
DP_GNS_CTRL	Base + 0x0734	R/W	DP GNS CONTROL REGISTER	0x0000_0018

DP_GNS_CTRL	Bit	Description	Initial State
-	[31:7]	Reserved	0
EQ_TRAINING_LOOP_CONTROL	[6]	1: enable 0: disable	0
-	[5]	Reserved	0
SCRAMBLE_CTRL	[4]	Scramble formula control: 1 = new formula; 0 = old formula;	1
IN_EX	[3]	Control scrambler structure: 1 = Internal type. 0 = External type.	1

DISABLE_SERDES_FIFO_RSET	[2]	1 = Disable serdes FIFO auto reset. 0 = Enable serdes FIFO auto reset	0
VIDEO_MAP_CTRL	[1]	Control use or not the video data map in YCbCr 4:2:2 mode: 1 = use video data map in YCbCr 4:2:2 mode. 0 = don't use.	0
RS_CTRL	[0]	Control RS parameter: 1 = parameter define by V1.0. 0 = parameter in GNS	0

Table 11-222 DP Audio Margin Register (DP_AUDIO_MARGIN)

Register	Address	Type	Description	Reset Value
DP_AUDIO_MARGIN	Base + 0x073C	R/W	DP Audio Margin Register	0x0000_0020

DP_AUDIO_MARGIN	Bit	Description	Initial State
-	[31:8]	Reserved	0
FORCE_AUDIO_MARGIN	[7]	Force audio margin 1: Audio margin use register value AUDIO_MARGIN. 0: Audio margin use hardware calculation. It is the default setting.	0
AUDIO_MARGIN	[6:0]	Audio packet is sent out during vertical blank or horizontal blank. This register is used to specify minimum stream clock cycles to transfer audio stream packet. If current remaining stream clock cycles before sending active video data is less than the value, DP postpone sending audio stream packets to the next video blank interval. AUDIO_MARGIN only takes effect when FORCE_AUDIO_MARGIN is set 1.	0x20

Table 11-223 DP M_AUD_MON register (M_AUD_MON)

Register	Address	Type	Description	Reset Value
M_AUD_MON	Base + 0x0740	RO	M_AUD value monitoring register	0x0000_0000

M_AUD_MON	Bit	Description	Initial State
-	[31:24]	Reserved	0
M_AUD_MON	[23:0]	This register shows M_AUD value which is actually transmitted to Rx for monitoring purpose.	0x0

Table 11-224 DP M_AUD Configure Register #0 (M_AUD_0)

Register	Address	Type	Description	Reset Value
M_AUD_0	Base + 0x0748	R/W	M_AUD[7:0]	0x0000_0000

M_AUD_0	Bit	Description	Initial State
-	[31:8]	Reserved	0
M_AUD_0	[7:0]	M_AUD [7:0]. If FIX_M_AUD is 1, this M_AUD is used. Otherwise the calculated M_AUD value is used.	0

Table 11-225 DP M_AUD Configure Register #1 (M_AUD_1)

Register	Address	Type	Description	Reset Value
M_AUD_1	Base + 0x074C	R/W	M_AUD[15:8]	0x0000_0000

M_AUD_1	Bit	Description	Initial State
-	[31:8]	Reserved	0
M_AUD_1	[7:0]	M_AUD [15:8]. If FIX_M_AUD is 1, this M_AUD is used. Otherwise the calculated M_AUD value is used.	0

Table 11-226 DP M_AUD Configure Register #2 (M_AUD_2)

Register	Address	Type	Description	Reset Value
M_AUD_2	Base + 0x0750	R/W	M_AUD[23:16]	0x0000_0000

M_AUD_2	Bit	Description	Initial State
-	[31:8]	Reserved	0
M_AUD_2	[7:0]	M_AUD [23:16]. If FIX_M_AUD is 1, this M_AUD is used. Otherwise the calculated M_AUD value is used.	0

Table 11-227 DP N_AUD Configure Register #0 (N_AUD_0)

Register	Address	Type	Description	Reset Value
N_AUD_0	Base + 0x0754	R/W	N_AUD[7:0]	0x0000_0000

N_AUD_0	Bit	Description	Initial State
-	[31:8]	Reserved	0
N_AUD_0	[7:0]	N_AUD[7:0]	0

Table 11-228 DP N_AUD Configure Register #1 (N_AUD_1)

Register	Address	Type	Description	Reset Value
N_AUD_1	Base + 0x0758	R/W	N_AUD[15:8]	0x0000_0080

N_AUD_1	Bit	Description	Initial State
-	[31:8]	Reserved	0
N_AUD_1	[7:0]	N_AUD[15:8]	0x80

Table 11-229 DP N_AUD Configure Register #2 (N_AUD_2)

Register	Address	Type	Description	Reset Value
N_AUD_2	Base + 0x075C	R/W	N_AUD[23:16]	0x0000_0000

N_AUD_2	Bit	Description	Initial State
-	[31:8]	Reserved	0
N_AUD_2	[7:0]	N_AUD [23:16].	0

Table 11-230 DP M Value Calculation Control Register (DP_M_CAL_CTL)

Register	Address	Type	Description	Reset Value
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DP_M_CAL_CTL	Base + 0x0760	R/W	DP M Value Calculation Control Register	0x0000_0000
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DP_M_CAL_CTL	Bit	Description	Initial State
-	[31:4]	Reserved	0
M_AUD_GEN_FILTER_EN	[3]	Enable M_AUD value generation filter to reduce the variation of M_AUD value. This filter is a low-pass filter to smooth out the M_AUD variation 1: Enable the filter 0: Disable the filter Note: Refer to page 22 for details.	0
M_VID_GEN_FILTER_EN	[2]	Enable M_VID value generation filter to reduce the variation of M_VID value. This filter is a low-pass filter to smooth out the M_VID variation 1: Enable the filter 0: Disable the filter Note: Refer to page 22 for details.	0
-	[1]	Reserved	0
M_GEN_CLK_SEL	[0]	Select which link clock is used to generate the M value 1: Clock with down spreading is used 0: Clock without down spreading is used	0

Table 11-231 DP M_VID Value Calculation Control Register (M_VID_GEN_FILTER_TH)

Register	Address	Type	Description	Reset Value
M_VID_GEN_FILTER_TH	Base + 0x0764	R/W	The threshold of M_VID generation filter	0x0000_0004

M_VID_GEN_FILTER_TH	Bit	Description	Initial State
-	[31:8]	Reserved	0
M_VID_GEN_FILTER_TH	[7:0]	The threshold of M_VID generation filter It only takes effect when M_VID_GEN_FILTER_EN is set to 1	4

Table 11-232 DP M_AUD Value Calculation Control Register (M_AUD_GEN_FILTER_TH)

Register	Address	Type	Description	Reset Value
M_AUD_GEN_FILTER_TH	Base + 0x0778	R/W	The threshold of M_AUD generation filter	0x0000_0002

M_AUD_GEN_FILTER_TH	Bit	Description	Initial State
-	[31:8]	Reserved	0
M_AUD_GEN_FILTER_TH	[7:0]	The threshold of M_AUD generation filter It only takes effect when M_AUD_GEN_FILTER_EN is set to 1	2

Table 11-233 AUX Channel Access Status Register (AUX_CH_STA)

Register	Address	Type	Description	Reset Value
AUX_CH_STA	Base + 0x0780	RO	AUX Channel Access Status Register	0x0000_0000

AUX_CH_STA	Bit	Description	Initial State
-	[31:5]	Reserved	0
AUX_BUSY	[4]	AUX channel status bit. If this bit is read as 1, AUX channel access should be halted. 1: AUX CH is busy 0: AUX CH is idle	0
AUX_STATUS	[3:0]	This register indicate the AUX channel access status 0: OK 1: NACK_ERROR 2: TIMEOUT_ERROR 3: UNKNOWN_ERROR 4: MUCH_DEFER_ERROR 5: TX_SHORT_ERROR 6: RX_SHORT_ERROR 7: NACK_WITHOUT_M_ERROR 8: I2C_NACK_ERROR Other: Reserved.	0

Table 11-234 AUX Channel Access Error Code Register (AUX_ERR_NUM)

Register	Address	Type	Description	Reset Value
AUX_ERR_NUM	Base + 0x0784	RO	AUX Channel Access Error Code Register	0x0000_0000

AUX_ERR_NUM	Bit	Description	Initial State
-	[31:8]	Reserved	0
AUX_ERR_NUM	[7:0]	The error number counter of AUX channel counts when AUX channel access failed. In AUX CH reading, this number indicates the number of read back byte. In AUX CH writing, this number indicates the number of reply command.	0

Table 11-235 DP AUX CH DEFER Control Register (AUX_CH_DEFER_CTL)

Register	Address	Type	Description	Reset Value
AUX_CH_DEFER_CTL	Base + 0x0788	R/W	DP AUX CH DEFER Control Register	0x0000_007F

AUX_CH_DEFER_CTL	Bit	Description	Initial State
-	[31:8]	Reserved	0
DEFER_CTRL_EN	[7]	AUX CH received DEFER command count control enable 1: If the count that AUX CH receive DEFER command equal to (DEFER_COUNT * 64), the AUX CH transaction is terminated, and the AUX_STATUS is 0100 0: The count that AUX CH receive DEFER command is unlimited	0

DEFER_COUNT	[6:0]	The count is defined to limit the max count AUX CH receive DEFER command When DEFER_CTRL_EN is 1 and AUX CH received (DEFER_COUNT * 64) DEFER command, the AUX CH will terminate the transaction	0x7F
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Table 11-236 DP AUX RX Command Register (AUX_RX_COMM)

Register	Address	Type	Description	Reset Value
AUX_RX_COMM	Base + 0x078C	RO	AUX CH received command	0x0000_0000

AUX_RX_COMM	Bit	Description	Initial State
-	[31:4]	Reserved	0
AUX_RX_COMM	[3:0]	AUX CH received command	0

Table 11-237 DP Buffer Data Count Register (BUFFER_DATA_CTL)

Register	Address	Type	Description	Reset Value
BUFFER_DATA_CTL	Base + 0x0790	RO/C	DP Buffer Data Count Register	0x0000_0000

BUFFER_DATA_CTL	Bit	Description	Initial State
-	[31:8]	Reserved	0
BUF_CLR(C)	[7]	Write 1 to this bit to clear AUX CH data buffer (BUF_DATA_0 ~ BUF_DATA_15). Always read back 0 from this bit. This bit's type is R/W. This bit is self cleared. Note: For the write operation, set this bit to 1 before writing data to BUF_DATA_0~15. And for READ operation, this bit has only to be set before starting data transfer by setting AUX_EN.	0
-	[6:5]	Reserved	0
BUF_HAVE_DATA(RO)	[4]	0:buffer have data,1:buffer have not data	0
BUF_DATA_COUNT(RO)	[3:0]	The counts of data AUX CH buffer have. This bit's type is RO.	0

Table 11-238 DP AUX Channel Control Register 1 (AUX_CH_CTL_1)

Register	Address	Type	Description	Reset Value
AUX_CH_CTL_1	Base + 0x0794	R/W	DP AUX Channel Control Register 1	0x0000_0000

AUX_CH_CTL_1	Bit	Description	Initial State
-	[31:8]	Reserved	0
AUX_LENGTH	[7:4]	Register control AUX CH transaction length.	0
AUX_TX_COMM	[3:0]	Register control AUX CH transaction command.	0

Table 11-239 DP AUX CH Address Register #0 (AUX_ADDR_7_0)

Register	Address	Type	Description	Reset Value
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AUX_ADDR_7_0	Base + 0x0798	R/W	AUX_ADDR[7:0]	0x0000_0000
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AUX_ADDR_7_0	Bit	Description	Initial State
-	[31:8]	Reserved	0
AUX_ADDR_7_0	[7:0]	AUX_ADDR[7:0], Register control AUX CH address	0

Table 11-240 DP AUX CH Address Register #1 (AUX_ADDR_15_8)

Register	Address	Type	Description	Reset Value
AUX_ADDR_15_8	Base + 0x079C	R/W	AUX_ADDR[15:8]	0x0000_0000

AUX_ADDR_15_8	Bit	Description	Initial State
-	[31:8]	Reserved	0
AUX_ADDR_15_8	[7:0]	AUX_ADDR[15:8], Register control AUX CH address	0

Table 11-241 DP AUX CH Address Register #2 (AUX_ADDR_19_16)

Register	Address	Type	Description	Reset Value
AUX_ADDR_19_16	Base + 0x07A0	R/W	AUX_ADDR[19:16]	0x0000_0000

AUX_ADDR_19_16	Bit	Description	Initial State
-	[31:4]	Reserved	0
AUX_ADDR_19_16	[3:0]	AUX_ADDR[7:0], Register control AUX CH address	0

Table 11-242 DP AUX CH Control Register 2 (AUX_CH_CTL_2)

Register	Address	Type	Description	Reset Value
AUX_CH_CTL_2	Base + 0x07A4	R/W /C	DP AUX CH Control Register 2	0x0000_0000

AUX_CH_CTL_2	Bit	Description	Initial State
-	[31:4]	Reserved	0
PD_AUX_IDLE	[3]	Power down AUX CH when AUX CH is in idle state. 1 : Power down AUX CH in idle state. 0 : Keep AUX CH power up in idle state.	0
AUX_PN_INV	[2]	Invert AUX CH PN 1: Invert PN 0: Normal mode	0
ADDR_ONLY	[1]	AUX CH issue "address only" command 1: Issue "address only" command 0: Normal AUX CH command	0
AUX_EN(C)	[0]	Register control AUX CH operation enable Write 1 to this bit to enable AUX CH operation This bit will self-clear when AUX CH operation is finished. This bit is self cleared.	0

Table 11-243 DP AUX Buffer Data Register (BUF_DATA_0 ~ BUF_DATA_15)

Register	Address	Type	Description	Reset Value
BUF_DATA_0 ~ BUF_DATA_15	Base + 0x07C0 ~ Base+0x07FC	R/W	AUX CH buffer data 0 ~ 15	0x0000_00FF

BUF_DATA_0 ~ BUF_DATA_15	Bit	Description	Initial State
-	[31:8]	Reserved	0
BUF_DATA_0 ~ BUF_DATA_15	[7:0]	AUX CH buffer data 0 ~ 15	0xFF

Register definitions for SoC IP implementation

Table 11-244 General control register (SOC_GENERAL_CTL)

Register	Address	Type	Description	Reset Value
SOC_GENERAL_CTL	Base + 0x0800	R/W	General control register	0x0000_0000

SOC_GENERAL_CTL	Bit	Description	Initial State
-	[31:18]	Reserved	0
AUDIO_BIT_MAPPING_TYPE	[17:16]	Audio bit mapping type in 16bit audio mode 0: Type 0, 1: Type 1 2: Type 2, 3: Reserved	0
-	[15]	Reserved	0
PCM_SIZE	[14:13]	PCM data bit size 00: 16 bit, 01: 20 bit 10: 24 bit, 11: Reserved	0
-	[12:6]	Reserved	0
AUDIO_CH_STATUS_SAME	[5]	Select the channel status bits for audio channel 3~8. 1: Use the same data channel status bits from AUDIO_GPO_STATUS_n registers. 0: Use each channel status bits from the corresponding AUDIO_GPx_STATUS_n registers.	0
-	[4:0]	Reserved	0

Table 11-245 ATE test control register (ATE_TEST_CTL)

Register	Address	Type	Description	Reset Value
ATE_TEST_CTL	Base + 0x0804	R/W C	ATE test control register	0x0000_0000

ATE_TEST_CTL	Bit	Description	Initial State
-	[31:9]	Reserved	0

TX_ATE	[15:8]	ATE test enable Bit 15~12: Reserved for analog test. Bit 11: ate_en in ch3, Bit 10: ate_en in ch2, Bit 9: ate_en in ch1 Bit 8: ate_en in ch0	0
-	[7:6]	Reserved	0
ATE_TEST_DATA_INV	[5]	Invert ate test data	0
ATE_ERR_GEN_EN_IN(C)	[4]	Insert a ERR for PHY ATE test. Self clear	0
ATE_CLR_ERR(C)	[3:0]	Clear error counter [3]:lane3,[2]:lane2,[1]:lane1,[0]:lane0	0

Table 11-246 ATE test status register (ATE_TEST_STATUS)

Register	Address	Type	Description	Reset Value
ATE_TEST_STATUS	Base + 0x0808	RO	ATE test control register	0x0000_0000

ATE_TEST_STATUS	Bit	Description	Initial State
-	[31:20]	Reserved	0
ERROR_INC	[19:16]	ERROR indicator [19]:lane3,[18]:lane2,[17]:lane1,[16]:lane0	0
PRBS7 CHECK FSM STATE	[15:0]	PRBS7 check FSM state [15:12]:lane3,[11:8]:lane2,[7:4]:lane1,[3:0]:lane0	0

Table 11-247 ATE test error counter register (ATE_TEST_ERR_CNT)

Register	Address	Type	Description	Reset Value
ATE_TEST_ERR_CNT	Base + 0x080C~ Base + 0x0818	RO	ATE test error counter register	0x0000_0000

ATE_TEST_STATUS	Bit	Description	Initial State
ATE_TEST_ERR_CNT	[31:0]	ATE test error counter register.0x080C—lane0, 0x0810—lane1, 0x0814—lane2, 0x0818—lane3	0

Table 11-248 DP test 80bit pattern0 (DP_TEST_80B_PATTERN0)

Register	Address	Type	Description	Reset Value
DP_TEST_80B_PATTERN0	Base + 0x081C	R/W	DP test 80bit pattern0	0x0000_0000

DP_TEST_80B_PATTERN0	Bit	Description	Initial State
-	[31:30]	Reserved	0
DP_TEST_80B_PATTERN0	[29:0]	DP test 80bit pattern0[29:0]	0

Table 11-249 DP test 80bit pattern1 (DP_TEST_80B_PATTERN1)

Register	Address	Type	Description	Reset Value
DP_TEST_80B_PATTERN1	Base + 0x0820	R/W	DP test 80bit pattern1	0x0000_0000

DP_TEST_80B_PATTERN1	Bit	Description	Initial State
-	[31:30]	Reserved	0
DP_TEST_80B_PATTERN1	[29:0]	DP test 80bit pattern0[59:30]	0x0000_0000

Table 11-250 DP test 80bit pattern2 (DP_TEST_80B_PATTERN2)

Register	Address	Type	Description	Reset Value
DP_TEST_80B_PATTERN2	Base + 0x0824	R/W	DP test 80bit pattern2	0x0000_0000

DP_TEST_80B_PATTERN0	Bit	Description	Initial State
-			

-	[31:20]	Reserved	0
DP_TEST_80B_PATTERNO	[19:0]	DP test 80bit pattern0[79:60]	0x0000_0000

Table 11-251 DP test HBR2 SR COUNT (DP_TEST_HBR2_PATTERN)

Register	Address	Type	Description	Reset Value
DP_TEST_HBR2_PATTERN	Base + 0x0828	R/W	Hbr2 compliance SR count	0x0000_0010

DP_TEST_80B_PATTERNO	Bit	Description	Initial State
-	[31:16]	Reserved	0
DP_TEST_HBR2_PATTERN	[15:0]	Hbr2 compliance SR count	0x0000_0010

Table 11-252 Audio Control register (AUD_CTL)

Register	Address	Type	Description	Reset Value
AUD_CTL	Base + 0x0834	R/W	Audio Control register	0x0000_0001

AUD_CTL	Bit	Description	Initial State
-	[31:3]	Reserved	0
AUD_CHANNEL_COUNT	[2:0]	Audio Channel Number; 3'b001:2 channel 3'b011:4 channel 3'b101:6 channel	1

Table 11-253 CRC check control register (CRC_CON)

Register	Address	Type	Description	Reset Value
CRC_CON	Base + 0x0890	R/W	CRC check control	0x0000_0000

CRC_CON	Bit	Description	Initial State
-	[31:3]	Reserved	0
VID_CRC_FLUSH	[2]	Video CRC flush enable. The video CRC value is initialized at every v-sync.	0
-	[1]	Reserved	0
VID_CRC_ENABLE	[0]	Video CRC enable. 0: Disable, 1: Enable	0

Table 11-254 CRC Result (CRC_RESULT)

Register	Address	Type	Description	Reset Value
CRC_RESULT	Base + 0x0894	RO	CRC result	0x0000_0000

CRC_RESULT	Bit	Description	Initial State
AUD_CRC_RESULT	[31:16]	Audio CRC result	0
VID_CRC_RESULT	[15:0]	Video CRC result	0

Table 11-255 Analog Control Register 5 (ANALOG_CTL_5)

Register	Address	Type	Description	Reset Value
ANALOG_CTL_5	Base + 0x0914	R/W	Analog Control Register 5	0x0000_0000

ANALOG_CTL_5	Bit	Description	Initial State
-	[31:8]	Reserved	0

CH3_PC2_SEL	[7:6]	Ch3 post cursor2 setting: CH3_PC2_SEL: post cursor2 0x0: 0 0x1: 0.05 0x2: 0.1 0x3: 0.15	0
CH2_PC2_SEL	[5:4]	Ch2 post cursor2 setting: CH2_PC2_SEL: post cursor2 0x0: 0 0x1: 0.05 0x2: 0.1 0x3: 0.15	0
CH1_PC2_SEL	[3:2]	Ch1 post cursor2 setting: CH1_PC2_SEL: post cursor2 0x0: 0 0x1: 0.05 0x2: 0.1 0x3: 0.15	0
CH0_PC2_SEL	[1:0]	Ch0 post cursor2 setting: CH0_PC2_SEL: post cursor2 0x0: 0 0x1: 0.05 0x2: 0.1 0x3: 0.15	0

Table 11-256 Analog Control Register 6 (ANALOG_CTL_6)

Register	Address	Type	Description	Reset Value
ANALOG_CTL_6	Base + 0x0918	R/W	Analog Control Register 6	0x0000_0050

ANALOG_CTL_6	Bit	Description	Initial State
-	[31:8]	Reserved	0
R_AMP_400MV_0DB	[7:0]	The lookup-table 1(for calculating chx_swing_bit) value when V_diff is 400mv and Pre_emphasis is 0 db.	0x50

Table 11-257 Analog Control Register 7 (ANALOG_CTL_7)

Register	Address	Type	Description	Reset Value
ANALOG_CTL_7	Base + 0x091C	R/W	Analog Control Register 7	0x0000_0078

ANALOG_CTL_7	Bit	Description	Initial State
-	[31:8]	Reserved	0
R_AMP_600MV_0DB	[7:0]	The lookup-table 1(for calculating chx_swing_bit) value when V_diff is 600mv and Pre_emphasis is 0 db.	0x78

Table 11-258 Analog Control Register 8 (ANALOG_CTL_8)

Register	Address	Type	Description	Reset Value
ANALOG_CTL_8	Base + 0x0920	R/W	Analog Control Register 8	0x0000_00A0

ANALOG_CTL_8	Bit	Description	Initial State
-	[31:8]	Reserved	0

R_AMP_800MV_0DB	[7:0]	The lookup-table 1(for calculating chx_swing_bit) value when V_diff is 800mv and Pre_emphasis is 0 db.	0xA0
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Table 11-259 Analog Control Register 9 (ANALOG_CTL_9)

Register	Address	Type	Description	Reset Value
ANALOG_CTL_9	Base + 0x0924	R/W	Analog Control Register 9	0x0000_00F0

ANALOG_CTL_9	Bit	Description	Initial State
-	[31:8]	Reserved	0
R_AMP_1200MV_0DB	[7:0]	The lookup-table 1(for calculating chx_swing_bit) value when V_diff is 1200mv and Pre_emphasis is 0 db.	0xF0

Table 11-260 Analog Control Register 10 (ANALOG_CTL_10)

Register	Address	Type	Description	Reset Value
ANALOG_CTL_10	Base + 0x0928	R/W	Analog Control Register 10	0x0000_0064

ANALOG_CTL_10	Bit	Description	Initial State
-	[31:8]	Reserved	0
R_AMP_400MV_3P5DB	[7:0]	The lookup-table 1(for calculating chx_swing_bit) value when V_diff is 400mv and Pre_emphasis is 3.5 db.	0x64

Table 11-261 Analog Control Register 11 (ANALOG_CTL_11)

Register	Address	Type	Description	Reset Value
ANALOG_CTL_11	Base + 0x092C	R/W	Analog Control Register 11	0x0000_0096

ANALOG_CTL_11	Bit	Description	Initial State
-	[31:8]	Reserved	0
R_AMP_600MV_3P5DB	[7:0]	The lookup-table 1(for calculating chx_swing_bit) value when V_diff is 600mv and Pre_emphasis is 3.5 db.	0x96

Table 11-262 Analog Control Register 12 (ANALOG_CTL_12)

Register	Address	Type	Description	Reset Value
ANALOG_CTL_12	Base + 0x0930	R/W	Analog Control Register 12	0x0000_00C8

ANALOG_CTL_12	Bit	Description	Initial State
-	[31:8]	Reserved	0
R_AMP_800MV_3P5DB	[7:0]	The lookup-table 1(for calculating chx_swing_bit) value when V_diff is 800mv and Pre_emphasis is 3.5 db.	0XC8

Table 11-263 Analog Control Register 13 (ANALOG_CTL_13)

Register	Address	Type	Description	Reset Value
ANALOG_CTL_13	Base + 0x0934	R/W	Analog Control Register 13	0x0000_0078

ANALOG_CTL_13	Bit	Description	Initial State
-	[31:8]	Reserved	0
R_AMP_400MV_6DB	[7:0]	The lookup-table 1(for calculating chx_swing_bit) value when V_diff is 400mv and Pre_emphasis is 6db.	0x78

Table 11-264 Analog Control Register 14 (ANALOG_CTL_14)

Register	Address	Type	Description	Reset Value
ANALOG_CTL_14	Base + 0x0938	R/W	Analog Control Register 14	0x0000_00B4

ANALOG_CTL_14	Bit	Description	Initial State
-	[31:8]	Reserved	0
R_AMP_600MV_6DB	[7:0]	The lookup-table 1(for calculating chx_swing_bit) value when V_diff is 600mv and Pre_emphasis is 6db.	0xB4

Table 11-265 Analog Control Register 15 (ANALOG_CTL_15)

Register	Address	Type	Description	Reset Value
ANALOG_CTL_15	Base + 0x093C	R/W	Analog Control Register 15	0x0000_00A0

ANALOG_CTL_15	Bit	Description	Initial State
-	[31:8]	Reserved	0
R_AMP_400MV_9DB	[7:0]	The lookup-table 1(for calculating chx_swing_bit) value when V_diff is 400mv and Pre_emphasis is 9db.	0xA0

Table 11-266 Analog Control Register 16 (ANALOG_CTL_16)

Register	Address	Type	Description	Reset Value
ANALOG_CTL_16	Base + 0x0940	R/W	Analog Control Register 16	0x0000_0000

ANALOG_CTL_16	Bit	Description	Initial State
-	[31:8]	Reserved	0
R_EMP_400MV_0DB	[7:0]	The lookup-table 2(for calculating chx_pre_emp_bit) value when V_diff is 400mv and Pre_emphasis is 0db.	0x00

Table 11-267 Analog Control Register 17 (ANALOG_CTL_17)

Register	Address	Type	Description	Reset Value
ANALOG_CTL_17	Base + 0x0944	R/W	Analog Control Register 17	0x0000_0000

ANALOG_CTL_17	Bit	Description	Initial State
-			

-	[31:8]	Reserved	0
R_EMP_600MV_0DB	[7:0]	The lookup-table 2(for calculating chx_pre_emp_bit) value when V_diff is 600mv and Pre_emphasis is 0 db.	0x00

Table 11-268 Analog Control Register 18 (ANALOG_CTL_18)

Register	Address	Type	Description	Reset Value
ANALOG_CTL_18	Base + 0x0948	R/W	Analog Control Register 18	0x0000_0000

ANALOG_CTL_18	Bit	Description	Initial State
-	[31:8]	Reserved	0
R_EMP_800MV_0DB	[7:0]	The lookup-table 2(for calculating chx_pre_emp_bit) value when V_diff is 800mv and Pre_emphasis is 0 db.	0x00

Table 11-269 Analog Control Register 19 (ANALOG_CTL_19)

Register	Address	Type	Description	Reset Value
ANALOG_CTL_19	Base + 0x094C	R/W	Analog Control Register 19	0x0000_0000

ANALOG_CTL_19	Bit	Description	Initial State
-	[31:8]	Reserved	0
R_EMP_1200MV_0DB	[7:0]	The lookup-table 2(for calculating chx_pre_emp_bit) value when V_diff is 1200mv and Pre_emphasis is 0 db.	0x00

Table 11-270 Analog Control Register 20 (ANALOG_CTL_20)

Register	Address	Type	Description	Reset Value
ANALOG_CTL_20	Base + 0x0950	R/W	Analog Control Register 20	0x0000_0028

ANALOG_CTL_20	Bit	Description	Initial State
-	[31:8]	Reserved	0
R_EMP_400MV_3P5DB	[7:0]	The lookup-table 2(for calculating chx_pre_emp_bit) value when V_diff is 400mv and Pre_emphasis is 3.5 db.	0x28

Table 11-271 Analog Control Register 21 (ANALOG_CTL_21)

Register	Address	Type	Description	Reset Value
ANALOG_CTL_21	Base + 0x0954	R/W	Analog Control Register 21	0x0000_003C

ANALOG_CTL_21	Bit	Description	Initial State
-	[31:8]	Reserved	0
R_EMP_600MV_3P5DB	[7:0]	The lookup-table 2(for calculating chx_pre_emp_bit) value when V_diff is 600mv and Pre_emphasis is 3.5 db.	0x3C

Table 11-272 Analog Control Register 22 (ANALOG_CTL_22)

Register	Address	Type	Description	Reset Value
ANALOG_CTL_22	Base + 0x0958	R/W	Analog Control Register 22	0x0000_0050

ANALOG_CTL_22	Bit	Description	Initial State
-	[31:8]	Reserved	0
R_EMP_800MV_3P5DB	[7:0]	The lookup-table 2(for calculating chx_pre_emp_bit) value when V_diff is 800mv and Pre_emphasis is 3.5 db.	0X50

Table 11-273 Analog Control Register 23 (ANALOG_CTL_23)

Register	Address	Type	Description	Reset Value
ANALOG_CTL_23	Base + 0x095C	R/W	Analog Control Register 23	0x0000_0050

ANALOG_CTL_23	Bit	Description	Initial State
-	[31:8]	Reserved	0
R_EMP_400MV_6DB	[7:0]	The lookup-table 2(for calculating chx_pre_emp_bit) value when V_diff is 400mv and Pre_emphasis is 6db.	0x50

Table 11-274 Analog Control Register 24 (ANALOG_CTL_24)

Register	Address	Type	Description	Reset Value
ANALOG_CTL_24	Base + 0x0960	R/W	Analog Control Register 24	0x0000_0078

ANALOG_CTL_24	Bit	Description	Initial State
-	[31:8]	Reserved	0
R_EMP_600MV_6DB	[7:0]	The lookup-table 2(for calculating chx_pre_emp_bit) value when V_diff is 600mv and Pre_emphasis is 6db.	0x78

Table 11-275 Analog Control Register 25 (ANALOG_CTL_25)

Register	Address	Type	Description	Reset Value
ANALOG_CTL_25	Base + 0x0964	R/W	Analog Control Register 25	0x0000_00A0

ANALOG_CTL_25	Bit	Description	Initial State
-	[31:8]	Reserved	0
R_EMP_400MV_9DB	[7:0]	The lookup-table 2(for calculating chx_pre_emp_bit) value when V_diff is 400mv and Pre_emphasis is 9db.	0xA0

Table 11-276 Analog Control Register 26 (ANALOG_CTL_26)

Register	Address	Type	Description	Reset Value
ANALOG_CTL_26	Base + 0x0968	R/W	Analog Control Register 26	0x0000_0004

ANALOG_CTL_26	Bit	Description	Initial State
-	[31:6]	Reserved	0
R_PC2_400MV_0DB	[5:0]	The lookup-table 3(for calculating chx_swing_bit and chx_pc2_bit) value when V_diff is 400mv and Pre_emphasis is 0db.	0x04

Table 11-277 Analog Control Register 27 (ANALOG_CTL_27)

Register	Address	Type	Description	Reset Value
ANALOG_CTL_27	Base + 0x096C	R/W	Analog Control Register 27	0x0000_0006

ANALOG_CTL_27	Bit	Description	Initial State
-	[31:6]	Reserved	0
R_PC2_600MV_0DB	[5:0]	The lookup-table 3(for calculating chx_swing_bit and chx_pc2_bit) value when V_diff is 600mv and Pre_emphasis is 0 db.	0x06

Table 11-278 Analog Control Register 28 (ANALOG_CTL_28)

Register	Address	Type	Description	Reset Value
ANALOG_CTL_28	Base + 0x0970	R/W	Analog Control Register 28	0x0000_0008

ANALOG_CTL_28	Bit	Description	Initial State
-	[31:6]	Reserved	0
R_PC2_800MV_0DB	[5:0]	The lookup-table 3(for calculating chx_swing_bit and chx_pc2_bit) value when V_diff is 800mv and Pre_emphasis is 0 db.	0x08

Table 11-279 Analog Control Register 29 (ANALOG_CTL_29)

Register	Address	Type	Description	Reset Value
ANALOG_CTL_29	Base + 0x0974	R/W	Analog Control Register 29	0x0000_000C

ANALOG_CTL_29	Bit	Description	Initial State
-	[31:6]	Reserved	0
R_PC2_1200MV_0DB	[5:0]	The lookup-table 3(for calculating chx_swing_bit and chx_pc2_bit) value when V_diff is 1200mv and Pre_emphasis is 0 db.	0x0C

Table 11-280 Analog Control Register 30 (ANALOG_CTL_30)

Register	Address	Type	Description	Reset Value
ANALOG_CTL_30	Base + 0x0978	R/W	Analog Control Register 30	0x0000_0006

ANALOG_CTL_30	Bit	Description	Initial State
-	[31:6]	Reserved	0
R_PC2_400MV_3P5DB	[5:0]	The lookup-table 3(for calculating chx_swing_bit and chx_pc2_bit) value when V_diff is 400mv and Pre_emphasis is 3.5 db.	0x06

Table 11-281 Analog Control Register 31 (ANALOG_CTL_31)

Register	Address	Type	Description	Reset Value
ANALOG_CTL_31	Base + 0x097C	R/W	Analog Control Register 31	0x0000_0009

ANALOG_CTL_31	Bit	Description	Initial State
-	[31:6]	Reserved	0
R_PC2_600MV_3P5DB	[5:0]	The lookup-table 3(for calculating chx_swing_bit and chx_pc2_bit) value when V_diff is 600mv and Pre_emphasis is 3.5 db.	0x09

Table 11-282 Analog Control Register 32 (ANALOG_CTL_32)

Register	Address	Type	Description	Reset Value
ANALOG_CTL_32	Base + 0x0980	R/W	Analog Control Register 32	0x0000_000C

ANALOG_CTL_32	Bit	Description	Initial State
-	[31:6]	Reserved	0
R_PC2_800MV_3P5DB	[5:0]	The lookup-table 3(for calculating chx_swing_bit and chx_pc2_bit) value when V_diff is 800mv and Pre_emphasis is 3.5 db.	0X0C

Table 11-283 Analog Control Register 33 (ANALOG_CTL_33)

Register	Address	Type	Description	Reset Value
ANALOG_CTL_33	Base + 0x0984	R/W	Analog Control Register 33	0x0000_0008

ANALOG_CTL_33	Bit	Description	Initial State
-	[31:6]	Reserved	0
R_PC2_400MV_6DB	[5:0]	The lookup-table 3(for calculating chx_swing_bit and chx_pc2_bit) value when V_diff is 400mv and Pre_emphasis is 6db.	0x08

Table 11-284 Analog Control Register 34 (ANALOG_CTL_34)

Register	Address	Type	Description	Reset Value
ANALOG_CTL_34	Base + 0x0988	R/W	Analog Control Register 34	0x0000_000C

ANALOG_CTL_34	Bit	Description	Initial State
-	[31:6]	Reserved	0
R_PC2_600MV_6DB	[5:0]	The lookup-table 3(for calculating chx_swing_bit and chx_pc2_bit) value when V_diff is 600mv and Pre_emphasis is 6db.	0x0C

Table 11-285 Analog Control Register 35 (ANALOG_CTL_35)

Register	Address	Type	Description	Reset Value
ANALOG_CTL_35	Base + 0x098C	R/W	Analog Control Register 35	0x0000_000C

ANALOG_CTL_35	Bit	Description	Initial State
-	[31:6]	Reserved	0
R_PC2_400MV_9DB	[5:0]	The lookup-table 3(for calculating chx_swing_bit and chx_pc2_bit) value when V_diff is 400mv and Pre_emphasis is 9db.	0x0C

Table 11-286 Analog Control Register 36 (ANALOG_CTL_36)

Register	Address	Type	Description	Reset Value
ANALOG_CTL_36	Base + 0x0990	R/W	Analog Control Register 36	0x0000_0050

ANALOG_CTL_36	Bit	Description	Initial State
-	[31:8]	Reserved	0
R_CH0_AMP_FORCE_VALUE	[7:0]	The forced ch0 amp value (for calculating ch0_swing_bit) value in specific V_diff and Pre_emphasis.	0x50

Table 11-287 Analog Control Register 37 (ANALOG_CTL_37)

Register	Address	Type	Description	Reset Value
ANALOG_CTL_37	Base + 0x0994	R/W	Analog Control Register 37	0x0000_0000

ANALOG_CTL_37	Bit	Description	Initial State
-	[31:8]	Reserved	0
R_CH0_EMP_FORCE_VALUE	[7:0]	The forced ch0 emp value (for calculating ch0_pre_emphasis_bit) value in specific V_diff and Pre_emphasis.	0x00

Table 11-288 Analog Control Register 38 (ANALOG_CTL_38)

Register	Address	Type	Description	Reset Value
ANALOG_CTL_38	Base + 0x0998	R/W	Analog Control Register 38	0x0000_0004

ANALOG_CTL_38	Bit	Description	Initial State
-	[31:6]	Reserved	0
R_CH0_PC2_FORCE_VALUE	[5:0]	The forced ch0 PC2 value (for calculating ch0_swing_bit and ch0_pc2_bit) value in specific V_diff and Pre_emphasis.	0x04

Table 11-289 Analog Control Register 39 (ANALOG_CTL_39)

Register	Address	Type	Description	Reset Value
ANALOG_CTL_39	Base + 0x099C	R/W	Analog Control Register 39	0x0000_0050

ANALOG_CTL_39	Bit	Description	Initial State
-	[31:8]	Reserved	0
R_CH1_AMP_FORCE_VALUE	[7:0]	The forced ch1 amp value (for calculating ch1_swing_bit) value in specific V_diff and Pre_emphasis.	0x50

Table 11-290 Analog Control Register 40 (ANALOG_CTL_40)

Register	Address	Type	Description	Reset Value
ANALOG_CTL_40	Base + 0x09A0	R/W	Analog Control Register 40	0x0000_0000

ANALOG_CTL_40	Bit	Description	Initial State
-	[31:8]	Reserved	0
R_CH1_EMP_FORCE_VALUE	[7:0]	The forced ch1 emp value (for calculating ch1_pre_emphasis_bit) value in specific V_diff and Pre_emphasis.	0x00

Table 11-291 Analog Control Register 41 (ANALOG_CTL_41)

Register	Address	Type	Description	Reset Value
ANALOG_CTL_41	Base + 0x09A4	R/W	Analog Control Register 41	0x0000_0004

ANALOG_CTL_41	Bit	Description	Initial State
-	[31:6]	Reserved	0
R_CH1_PC2_FORCE_VALUE	[5:0]	The forced ch1 PC2 value (for calculating ch1_swing_bit and ch1_pc2_bit) value in specific V_diff and Pre_emphasis.	0x04

Table 11-292 Analog Control Register 42 (ANALOG_CTL_42)

Register	Address	Type	Description	Reset Value
ANALOG_CTL_42	Base + 0x09A8	R/W	Analog Control Register 42	0x0000_0000

ANALOG_CTL_42	Bit	Description	Initial State
-	[31:6]	Reserved	0
R_FORCE_CH1_AMP	[5]	0x1: The result of ch1 swing bit is decide by R_CH1_AMP_FORCE_VALUE value 0x0: The result of ch1 swing bit is decide by different V_diff and Pre_emphasis	0
R_FORCE_CH1_EMP	[4]	0x1: The result of ch1 pre emphasis bit is decide by R_CH1_EMP_FORCE_VALUE value 0x0: The result of ch1 swing bit is decide by different V_diff and Pre_emphasis	0
R_FORCE_CH1_PC2	[3]	0x1: The result of ch1 pc2 bit is decide by R_CH1_PC2_FORCE_VALUE value 0x0: The result of ch1 swing bit is decide by different V_diff and Pre_emphasis	0
R_FORCE_CH0_AMP	[2]	0x1: The result of ch0 swing bit is decide by R_CH1_AMP_FORCE_VALUE value 0x0: The result of ch0 swing bit is decide by different V_diff and Pre_emphasis	0
R_FORCE_CH0_EMP	[1]	0x1: The result of ch0 pre emphasis bit is decide by R_CH1_EMP_FORCE_VALUE value 0x0: The result of ch0 swing bit is decide by different V_diff and Pre_emphasis	0

R_FORCE_CH0_PC2	[0]	0x1: The result of ch0 pc2 bit is decide by R_CH1_PC2_FORCE_VALUE value 0x0: The result of ch0 swing bit is decide by different V_diff and Pre_emphasis	0
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Table 11-293 Analog Control Register 43 (ANALOG_CTL_43)

Register	Address	Type	Description	Reset Value
ANALOG_CTL_43	Base + 0x09AC	R/W	Analog Control Register 43	0x0000_0050

ANALOG_CTL_43	Bit	Description	Initial State
-	[31:8]	Reserved	0
R_CH2_AMP_FORCE_VALUE	[7:0]	The forced ch2 amp value (for calculating ch2_swing_bit) value in specific V_diff and Pre_emphasis.	0x50

Table 11-294 Analog Control Register 44 (ANALOG_CTL_44)

Register	Address	Type	Description	Reset Value
ANALOG_CTL_44	Base + 0x09B0	R/W	Analog Control Register 44	0x0000_0000

ANALOG_CTL_44	Bit	Description	Initial State
-	[31:8]	Reserved	0
R_CH2_EMP_FORCE_VALUE	[7:0]	The forced ch2 emp value (for calculating ch2_pre_emphasis_bit) value in specific V_diff and Pre_emphasis.	0x00

Table 11-295 Analog Control Register 45 (ANALOG_CTL_45)

Register	Address	Type	Description	Reset Value
ANALOG_CTL_45	Base + 0x09B4	R/W	Analog Control Register 45	0x0000_0004

ANALOG_CTL_45	Bit	Description	Initial State
-	[31:6]	Reserved	0
R_CH2_PC2_FORCE_VALUE	[5:0]	The forced ch2 PC2 value (for calculating ch2_swing_bit and ch2_pc2_bit) value in specific V_diff and Pre_emphasis.	0x04

Table 11-296 Analog Control Register 46 (ANALOG_CTL_46)

Register	Address	Type	Description	Reset Value
ANALOG_CTL_46	Base + 0x09B8	R/W	Analog Control Register 46	0x0000_0050

ANALOG_CTL_46	Bit	Description	Initial State
-	[31:8]	Reserved	0
R_CH3_AMP_FORCE_VALUE	[7:0]	The forced ch3 amp value (for calculating ch3_swing_bit) value in specific V_diff and Pre_emphasis.	0x50

Table 11-297 Analog Control Register 47 (ANALOG_CTL_47)

Register	Address	Type	Description	Reset Value
ANALOG_CTL_47	Base + 0x09BC	R/W	Analog Control Register 47	0x0000_0000

ANALOG_CTL_47	Bit	Description	Initial State
-	[31:8]	Reserved	0
R_CH3_EMP_FORCE_VALUE	[7:0]	The forced ch3 emp value (for calculating ch3_pre_emphasis_bit) value in specific V_diff and Pre_emphasis.	0x00

Table 11-298 Analog Control Register 48 (ANALOG_CTL_48)

Register	Address	Type	Description	Reset Value
ANALOG_CTL_48	Base + 0x09C0	R/W	Analog Control Register 48	0x0000_0004

ANALOG_CTL_48	Bit	Description	Initial State
-	[31:6]	Reserved	0
R_CH3_PC2_FORCE_VALUE	[5:0]	The forced ch3 PC2 value (for calculating ch3_swing_bit and ch3_pc2_bit) value in specific V_diff and Pre_emphasis.	0x04

Table 11-299 Analog Control Register 49 (ANALOG_CTL_49)

Register	Address	Type	Description	Reset Value
ANALOG_CTL_49	Base + 0x09C4	R/W	Analog Control Register 49	0x0000_0000

ANALOG_CTL_49	Bit	Description	Initial State
-	[31:6]	Reserved	0
R_FORCE_CH3_AMP	[5]	0x1: The result of ch3 swing bit is decide by R_CH1_AMP_FORCE_VALUE value 0x0: The result of ch3 swing bit is decide by different V_diff and Pre_emphasis	0
R_FORCE_CH3_EMP	[4]	0x1: The result of ch3 pre emphasis bit is decide by R_CH1_EMP_FORCE_VALUE value 0x0: The result of ch3 swing bit is decide by different V_diff and Pre_emphasis	0
R_FORCE_CH3_PC2	[3]	0x1: The result of ch3 pc2 bit is decide by R_CH1_PC2_FORCE_VALUE value 0x0: The result of ch3 swing bit is decide by different V_diff and Pre_emphasis	0
R_FORCE_CH2_AMP	[2]	0x1: The result of ch2 swing bit is decide by R_CH1_AMP_FORCE_VALUE value 0x0: The result of ch2 swing bit is decide by different V_diff and Pre_emphasis	0
R_FORCE_CH2_EMP	[1]	0x1: The result of ch2 pre emphasis bit is decide by R_CH1_EMP_FORCE_VALUE value 0x0: The result of ch2 swing bit is decide by different V_diff and Pre_emphasis	0
R_FORCE_CH2_PC2	[0]	0x1: The result of ch2 pc2 bit is decide by R_CH1_PC2_FORCE_VALUE value 0x0: The result of ch2 swing bit is decide by different V_diff and Pre_emphasis	0

Table 11-300 I2S_CTRL (I2S_CTRL)

Register	Address	Type	Description	Reset Value
I2S_CTRL	Base + 0x09C8	R/W	I2S_CTRL	0x0000_0000

I2S_CTRL	Bit	Description	Initial State
-	[31:8]	Reserved	0
I2S_EN	[7:4]	I2S enable	0
I2S_FMT_CTRL	[3:0]	I2S Format Control	0

Table 11-301 I2S_CH_SWAP (I2S_CH_SWAP)

Register	Address	Type	Description	Reset Value
I2S_CH_SWAP	Base + 0x09CC	R/W	I2S channel swap	0x0000_000b

I2S_CH_SWAP	Bit	Description	Initial State
-	[31:8]	Reserved	0
I2S_CH_SWAP	[7:4]	I2S channel swap	0
I2S_WD_LEN	[3:0]	I2S word length	0xb

Table 11-302 I2S_CH_CTRL (I2S_CH_CTRL)

Register	Address	Type	Description	Reset Value
I2S_CH_CTRL	Base + 0x09D0	R/W	I2S channel control	0x0000_00e4

I2S_CH_CTRL	Bit	Description	Initial State
-	[31:8]	Reserved	0
I2S_CH_CTRL	[7:0]	I2S channel control	0xe4

Table 11-303 I2S_CH_CTRL1 (I2S_CH_CTRL1)

Register	Address	Type	Description	Reset Value
I2S_CH_CTRL1	Base + 0x09D4	R/W	I2S channel control 1	0x0000_0000

I2S_CH_CTRL1	Bit	Description	Initial State
-	[31:3]	Reserved	0
I2S_AUD_LAYOUT	[2]	Audio layout	0
I2S_AUD_V_BIT	[1]	Audio v_bit	0
I2S_AUT_EXT_STA	[0]	Audio ext channel status	0

Table 11-304 LINK_POLICY (LINK_POLICY)

Register	Address	Type	Description	Reset Value
LINK_POLICY	Base + 0x09D8	R/W	Link_Policy	0x0000_0050

LINK_POLICY	Bit	Description	Initial State
-	[31:8]	Reserved	0
ALTERNATE_SR_EN	[7]	Alternate SR enable	0
LINK_TRAIN_CR_LP_IN	[6:4]	Link training CR loop in	5
LINK_TRAIN_WR_EN	[3]	Training first write en	0
LINK_TRAIN_405G	[2]	405g training enable	0
LINK_TRAIN_INV	[1]	Invert training bit enable	0

FRAME_CHANGE_EN	[0]	Framing change enable	0
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IO Definitions

Digital Core IO Definition

Name	Type	width	Active state	Reset value	Reset restraint	Description
Misc signals						
I_CLK_24M	I		Pulse	-	Pulse	Crystal Clock
I_DP_HPD	I		1'b1		1'b0	Hot plug
I_STMODE	I		1'b1		1'b0	Scan test mode signal. Active high
I_DP_VERSION	I	7:0	Any		8'b0	<7:5> process 00 (tsmc28nm) <4:3>: Version 00: Rev A <2:0>: Minor revision 000: rev .1
I_HDCP_PROTECT	I		1'b1		1'b1	HDCP function protection, 1=protect
I_BIST_EN	I		1'b1		1'b1	PHY BIST function enabled, 1=enable.
I_CLK_200M	I		Any		Pulse	200M clock input for S/PDIF oversample.
Video slave interface						
I_STRM_CLK	I		Pulse	-	Pulse	Pixel clock of video slave interface.
I_D_R_SLAVE	I	11:0	Any	-	12'b0	Video data R/Cr of video slave interface.
I_D_G_SLAVE	I	11:0	Any	-	12'b0	Video data G/Y of video slave interface.
I_D_B_SLAVE	I	11:0	Any	-	12'b0	Video data B/Cb of video slave interface.
I_V_SYNC_SLAVE	I		Any	-	1'b0	V_SYNC signal of video slave interface.
I_H_SYNC_SLAVE	I		Any	-	1'b0	H_SYNC signal video slave interface.
I_DE_SLAVE	I		Any	-	1'b0	DE signal of video slave interface.
Audio interface						
I_SPDIF_IN	I		Any	-	1'b0	S/PDIF input
I_I2S_SD0_IN	I		Any	-	1'b0	I2S data0
I_I2S_SD1_IN	I		Any	-	1'b0	I2S data1
I_I2S_SD2_IN	I		Any	-	1'b0	I2S data2
I_I2S_SD3_IN	I		Any		1'b0	I2S data3
I_I2S_SCK_IN	I		Any		1'b0	I2S clock
I_I2S_WS_IN	I		Any		1'b0	I2S word select
HDCP SRAM interface						
I_DP_MEM_Q	I	7:0	Any	-	8'b0	HDCP key data from memory
I_HDMI_HDCP_SRAM_DATA_EN	I		1'b1	1'b0		Floating
I_HDCP_PROTECT	I		1'b1		1'b0	Enable HDCP control registers write
O_DP_MEM_A	O	8:0	Any	9'b0	-	HDCP key data address
O_DP_MEM_R	O		1'b1	1'b0		External SRAM chip Read enable
AUX CH						
I_AUX_DATA_R	I		Any	-	1'b0	AUX CH serial data input.
O_AUX_DATA_T	O		1'b1	1'b0	-	AUX CH serial data output
Main link						
O_CH0_TXD	O	19:0	Any	20'b0	-	Main link channel 0 data output.
O_CH1_TXD	O	19:0	Any	20'b0	-	Main link channel 1 data output.
O_CH2_TXD	O	19:0	Any	20'b0	-	Main link channel 2 data output.
O_CH3_TXD	O	19:0	Any	20'b0	-	Main link channel 3 data output.
APB interface						
I_PRESETn	I		1'b0	-	1'b0	APB interface reset, low active.
I_PCLK	I		Pulse	-	Pulse	APB interface clock

Name	Type	width	Active state	Reset value	Reset restraint	Description
I_PENABLE	I		1'b1	-	1'b0	APB interface ready signal
I_PSEL	I		1'b1	-	1'b0	APB interface select signal
I_PWRITE;	I		Any	-	1'b0	APB interface write/read indication signal
I_PADDR	I	31:0	Any	-	8'b0	APB interface address.
I_PWDATA	I	31:0	Any	-	1'b0	APB interface write data bus
O_PREADY	O		1'b1	1'b0		APB interface ready output
O_PSLVERR	O		1'b1	1'b0		APB interface error signal
O_PRDATA	O	31:0	Any	31'b0	-	APB interface read data
Interrupt						
O_DP_INTP	O		1'b1	1'b0	-	Interrupt signal of DP core
Analog interface						
I_PLL_G_LOCK_DET	I		1'b1		1'b0	PLL lock detector
I_LINK_CLK	I		Pulse		Pulse	Main link clock
I_CH_TXD_CL_K	I		Pulse		Pulse	Half of I_LINK_CLK
I_CLK_DIV2	I		Pulse		Pulse	Half of I_LINK_CLK
I_TX_ATE_DATA	I	3:0	Any		4'b0	PHY BIST result data.
O_SSC_RESET_N	O		1'b0	1'b1		SSC reset, low active
O_PLL_REG_1	O	7:0	Any	8'h02		<7:6>--reserved <5:4>--PLL work mode select 00: 1.62G 01: 2.7G 10: reserved 11: reserved <3:1>--reserved <0>--PLL reference clock select 0: 24M (default) 1: 27M
O_PLL_REG_2	O	7:0	Any	8'h95		<7:6>--1.5v LDO output voltage select 00:1.35v 01:1.40v 10:1.45v(default) 11:1.50v <5:4>--KVCO to control VCO band 00: decrease KVCO by 15% 01:(default) 10: increase KVCO by 10% 11: increase KVCO by 20% <3:2>--charge pump current select 00:2.5u 01:5u(default) 10:7.5u 11:10u <1:0>--v2i current select 00: no adding current 01: adding 1mA current(default) 10: adding 2mA current 11: adding 4.5mA current
O_PLL_REG_3	O	7:0	Any	8'h40		<7>--reserved <6:5>--lock detector output counter select, counter period is twice of reference clock 00: 64 cycle 01: 128 cycle 10: 256 cycle (default) 11: 512 cycle <4>--loop filter control voltage reset select 1: reset to the value below DVDD 0: reset to DVDD (default) <3>--PLL and SSC reset control 1: reset 0: normal

Name	Type	width	Active state	Reset value	Reset restraint	Description					
						<2>--lock detector bypass select 0: not bypass (default) 1: bypass lock detector in ssc <1>--PLL lock detector mode select 0: fractional N (default) 1: integer N <0>--force PLL lock detector lock 0: not force lock (default) 1: force PLL lock					
O_PLL_REG_4	O	7:0	Any	8'h58		Reserved					
O_PLL_REG_5	O	7:0	Any	8'h22		<7>--reserved <6:4>--slave regulator output voltage select 000 : 0.900V 001 : 0.925V 010 : 0.950V(default) 011 : 0.975V 100 : 1.000V 101 : 1.025V 110 : 1.050V <3>--slave standby current select 1: adding 200uA standby current 0: keep 300uA standby current (default) <2:1>--control charge pump input voltage for 0.95V master regulator 00: 1.1V 01: 1.2V(default) 10: 1.3V 11: 1.4V <0>--option to control charge pump input voltage for 0.95V master regulator 0: set by pll_reg5<2:1> (default) 1: 1.8V					
O_PLL_MAC	O	7:0	Any	8'h00		Reserved					
O_SSC_REG	O	7:0	Any	8'b0		<7:6>--ssc offset 00: no 01: up 100ppm 10: down 100ppm 11: down 200ppm <5:4>--ssc mode 00:disable 01:down spread 10:center spread 11:up spread <3:0>--ssc depth 0000:disable 0001:500ppm 0010:1000ppm 0011:1500ppm 0100:2000ppm 0101:2500ppm 0110:3000ppm 0111:3500ppm 1000:4000ppm 1001:4500ppm 1010:5000ppm 1011:5500ppm 1100-1111:6000ppm					
O_CH0_REG_SWING	O	7:0	Any	8'h07			swin_g0	pre_0db	pre_3.5 db	pre_6db	pre_9.5 db
O_CH1_REG_SWING	O	7:0	Any	8'h07			swin_g1	0x01	0x71	0x73	0x7F
O_CH2_REG_SWING	O	7:0	Any	8'h07			swin	0x03	0x6B	0x7F	Not Allowed
O_CH3_REG_	O	7:0	Any	8'h07			swin	0x07	0x7F	Not	Not

Name	Type	width	Active state	Reset value	Reset restraint	Description				
SWING						g2			Allowed	Allowed
						swin_g3	0x7F	Not Allowed	Not Allowed	Not Allowed
O_CH0_REG_PRE	O	7:0	Any	8'b0			pre_0db	pre_3.5 db	pre_6db	pre_9.5 db
O_CH1_REG_PRE	O	7:0	Any	8'b0		swin_g0	0x00	0x0C	0x3E	0x7E
O_CH2_REG_PRE	O	7:0	Any	8'b0		swin_g1	0x00	0x42	0x72	Not Allowed
O_CH3_REG_PRE	O	7:0	Any	8'b0		swin_g2	0x00	0x1E	Not Allowed	Not Allowed
						swin_g3	0x00	Not Allowed	Not Allowed	Not Allowed
O_CH0_REG_P_C2	O	7:0	Any	8'b0		Reserved				
O_CH1_REG_P_C2	O	7:0	Any	8'b0		Reserved				
O_CH2_REG_P_C2	O	7:0	Any	8'b0		Reserved				
O_CH3_REG_P_C2	O	7:0	Any	8'b0		Reserved				
O_TX_COMMON	O	7:0	Any	8'h87		<7>--TX swing and pre emphasis control mode selection 1: TX swing and pre emphasis control by register dp_reserv2<7:0> 0: TX swing and pre emphasis control by register chx_reg_swing<7:0> and chx_reg_pre<7:0> <6:5>--pre-driver extra power control 0:disable 1:enable <4>--low power mode control for clock regulator 0: low power mode 1: high power mode <3>--TX terminal resistor MSB control <2:0>--TX terminal resistor control when tx_common<3>=0 000: 58.54 011:54.6 111:50 when tx_common<6>=1 000: 49 011:46 111:42.6				
O_TX_COMMON2	O	7:0	Any	8'h50		<7>--CH3 output P-N inverse 0: output p and n inverse 1: not inverse <6>--CH2 output P-N inverse 0: not inverse 1: output p and n inverse <5>--CH1 output P-N inverse 0: output p and n inverse 1: not inverse <4>--CH0 output P-N inverse 0: not inverse 1: output p and n inverse <3>--TX output pattern enable 0: normal TX 1: dedicate pattern				

Name	Type	width	Active state	Reset value	Reset restraint	Description
						<2:0> TX data pattern 000:all zero 001:all one 010:D10.2 011:1100 100:K28.5 101:K28.7 110:1111100000 111:11111111110000000000
O_TX_COMMON3	O	7:0	Any	8'h00		<7:3>--select /20 clock delay (clk_div2_ssc_tx_txd_clk) 00000 delay=150ps 00001 delay=150ps+1*70ps 00010 delay=150ps+2*70ps 00011 delay=150ps+3*70ps <2>--TX input clock inverse enable 0: normal 1: TX input clock inverse <1>--ch0 select i_ref_clk_24m for scan 0:select tx_bscan_data<0> 1:select i_ref_clk_24m <0>--Reserved
O_TX_ATE	O	7:0	Any	8'b0		<7:4>--Reserved <3>--ate_en in ch3 <2>--ate_en in ch2 <1>--ate_en in ch1 <0>--ate_en in ch0
O_DP_AUX	O	7:0	Any	8'h03		<7:5>--Reserved <4>--AUX RX CM voltage control 0: AUX CH use VCC1/2 as CM voltage (have static current consumption) 1: CM voltage is 0 <3>--AUX TX/RX enable control 0 - AUX CH configured as RX 1 - AUX CH configured as TX <2>--Reserved <1:0>--AUX CH TX impedance control: 00 - 600ohm 01 - 300ohm 10 - 100ohm 11 - 50ohm
O_DP_BIAS	O	7:0	Any	8'h46		<7>--Reserved <6:4>-- band gap output voltage tuning 000:0.56V 100:0.6V(default) 111:0.63V <3>--band gap start up current control 0: balance 1: unbalance <2>--band gap selection control 0:sel resistor divider 1:sel band gap <1:0>resistor tune for band gap TC control 00: 25uV/°C 01: 10uV/°C 10: -10uV/°C 11: -25uV/°C
O_DP_TEST	O	7:0	Any	8'h00		<7:6> 00&01: test disable, dc_tp/atesto/dtesto output hiz 10: atesto test enable 11: dtesto test enable <5:3>

Name	Type	width	Active state	Reset value	Reset restraint	Description
						<p>when <7:6> ==10, test analog blocks:</p> <p>000-- disable analog test</p> <p>001: enable ch0 analog test mux <1:0> (00/01/10/11)---> (avdd10_pre_drv,avdd10_p2s, vddu_p2s,avss)</p> <p>010: enable ch1 analog test mux <1:0> (00/01/10/11)---> (avdd10_pre_drv,avdd10_p2s, vddu_p2s,avss)</p> <p>011: enable ch2 analog test mux <1:0> (00/01/10/11)---> (avdd10_pre_drv,avdd10_p2s, vddu_p2s,avss)</p> <p>100: enable ch3 analog test mux <1:0> (00/01/10/11)---> (avdd10_pre_drv,avdd10_p2s, vddu_p2s,avss)</p> <p>101: enable pll analog test mux <1:0> (00/01/10/11)---> (vdd10_cln,v1p45_v2i, avdd18,vco_ctrl)</p> <p>110: enable chargepump regulator analog test mux <1:0> (00/01/10/11)---->(v1v_regu, vregu_out,v0.5_ref,null)</p> <p>111: test bandgap output</p> <p>When<7:6>==11, test digital blocks:</p> <p>000: disable digital test</p> <p>001: enable pll digital test mux <1:0>--(00/01/10/11)--->pll_ref,vco_fb, vss,vss.</p> <p>010: test chgpmp regulator osc clock. <2>--Reserved</p>
O_DP_PD	O	7:0	Any	8'hC0		<p><7> pd all including band gap</p> <p><6> pd all except band gap</p> <p><5> power down aux channel</p> <p><4> power down PLL</p> <p><3> power down ch3</p> <p><2> power down ch2</p> <p><1> power down ch1</p> <p><0> power down ch0</p> <p>0:normal</p> <p>1:power down</p>
O_DP_RESERV1	O	7:0	Any	8'h00		<p><7>--SSC mode lock</p> <p><6>--Reserved</p> <p><5:4>--Pre-driver extra power control</p> <p>0: disable</p> <p>1: enable</p> <p><3>--ch3 ate enable</p> <p>1: enable / 0: disable</p> <p><2>--ch2 ate enable</p> <p>1: enable / 0: disable</p> <p><1>--ch1 ate enable</p> <p>1: enable / 0: disable</p> <p><0>--ch0 ate enable</p> <p>1: enable / 0: disable</p>
O_DP_RESERV2	O	7:0	Any	8'h55		<p><7:4>: ch1,3 swing and pre emphasis control for firmware when tx_common<7>=1</p> <p>0000 : swing0 pre emphasis 0 dB</p> <p>0001 : swing1 pre emphasis 0 dB</p> <p>0010 : swing2 pre emphasis 0 dB</p> <p>0011 : swing3 pre emphasis 0 dB</p> <p>0100 : swing0 pre emphasis 3.5 dB</p> <p>0101 : swing1 pre emphasis 3.5 dB</p> <p>0110 : swing2 pre emphasis 3.5 dB</p> <p>1000 : swing0 pre emphasis 6 dB</p> <p>1001 : swing1 pre emphasis 6 dB</p> <p>1100 : swing0 pre emphasis 9.5 dB</p>

Name	Type	width	Active state	Reset value	Reset restraint	Description
						others : swing0 pre emphasis 9.5 dB <3:0>: ch0,2 swing and pre emphasis control for firmware when tx_common<7>=1 0000 : swing0 pre emphasis 0 dB 0001 : swing1 pre emphasis 0 dB 0010 : swing2 pre emphasis 0 dB 0011 : swing3 pre emphasis 0 dB 0100 : swing0 pre emphasis 3.5 dB 0101 : swing1 pre emphasis 3.5 dB 0110 : swing2 pre emphasis 3.5 dB 1000 : swing0 pre emphasis 6 dB 1001 : swing1 pre emphasis 6 dB 1100 : swing0 pre emphasis 9.5 dB others : swing0 pre emphasis 9.5 dB
I_DP_VERSIO N	I	7:0	Any	8'hA0		<7:5>--process 011 Global Foundry <4:3>--Version 00: Rev A <2:0>--Minor revision 000: rev .1
I_FRQ	I			8'h00		Digital output for debug, controlled by pll_reg1<7> and pll_reg4<4>: When pll_reg1<7>=0 & pll_reg4<4>=0 half video clock frequency calculated by frequency counter When pll_reg1<7>=0 & pll_reg4<4>=1 half video clock frequency calculated frq_vid_ck_in<8:0> When pll_reg1<7>=1: frq<7:4>: 0 frq<3:2>: band<1:0> frq<1:0>: <n_over, n_under>
I_FRQ_COUNT _RDY	I			1'b0		frequency counter ready indicator (frequency counter for VCO band selection) 1: frequency counter ready, its output is the real value of video PLL 0: frequency counter not ready, its output is not the real value
O_BAND_DEC _RESET	O		1'b1	1'b0		1: reset band decoder. 0: band decoder works.

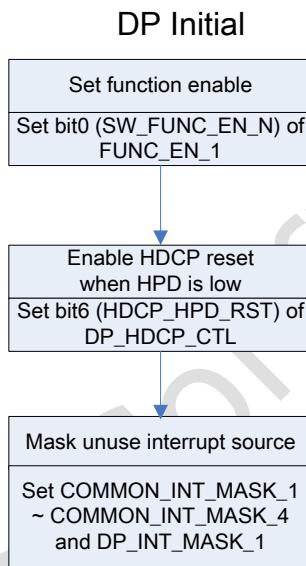
APPENDIX: Programming GUIDE

Contents

- A1. How to initialize DP
- A2. How to detect hot plug insertion
- A3. How to access DPCD space in DP Rx
- A4. How to write into EDID space in DP Rx
- A5. How to read from EDID space in DP Rx
- A6. How to do SW link training
 - A6.1. State machine of SW link training
 - A6.2. State LT_INITIAL
 - A6.3. State LT_START
 - A6.4. State CHANNEL_CR
 - A6.5. State CHANNEL_EQ
- A7. How to setup main stream attribute data
 - A7.1. Attribute of video timing

- A7.2. Attribute of color depth
- A7.3. Attribute of color space
- A8. How to do HDCP authentication and encryption
 - A8.1. SW HDCP state machine
 - A8.2. SW HDCP flowchart
- A9. How to configure video
- A10. How to configure audio
- A11. How to process interrupt
- A12. How to send Auxiliary Information Packets
- A13. Primitive functions and test codes for DisplayPort LLD
- A14. How to configure Video BIST

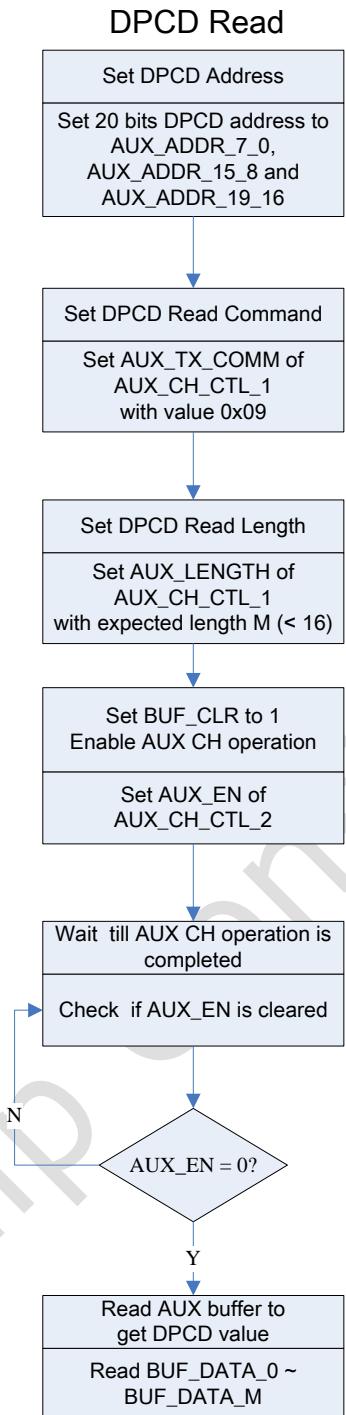
How to initialize DP

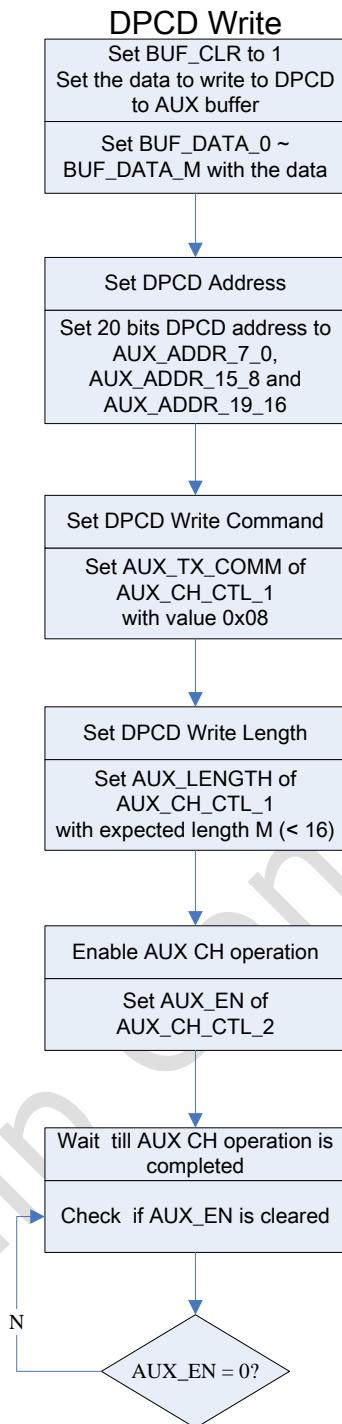


How to Detect hot plug insertion

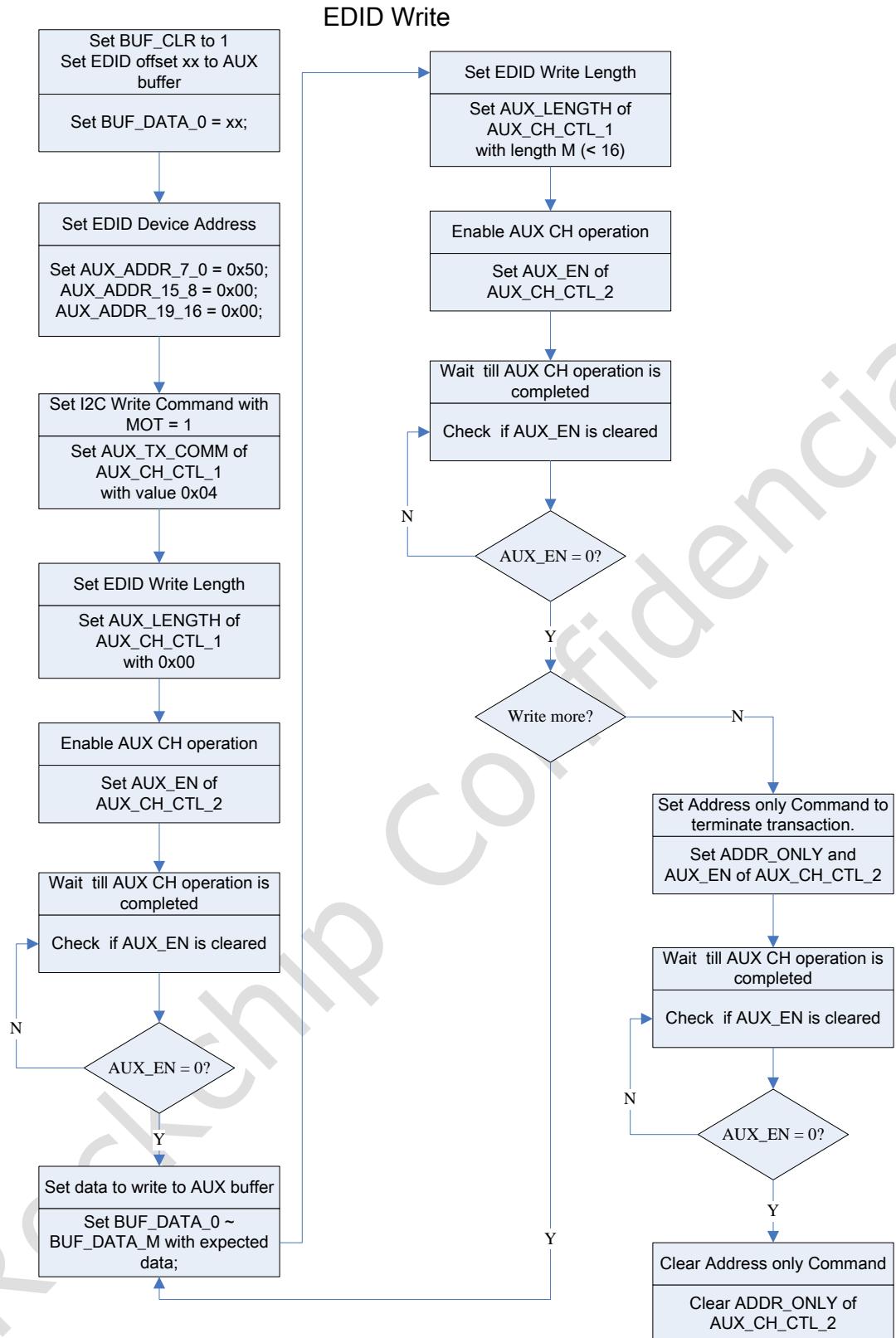
In Wait Hot plug state, chip is in power down status. System only responds to hot plug change interrupt. When a hot plug interrupt is detected, in the interrupt routine, firmware will judge whether it is a receiver plug-in or un-plug or link training request. If plug-in, chip will be powered on and system state will be set to Read and Parse EDID.

How to access DPCD space in DP Rx

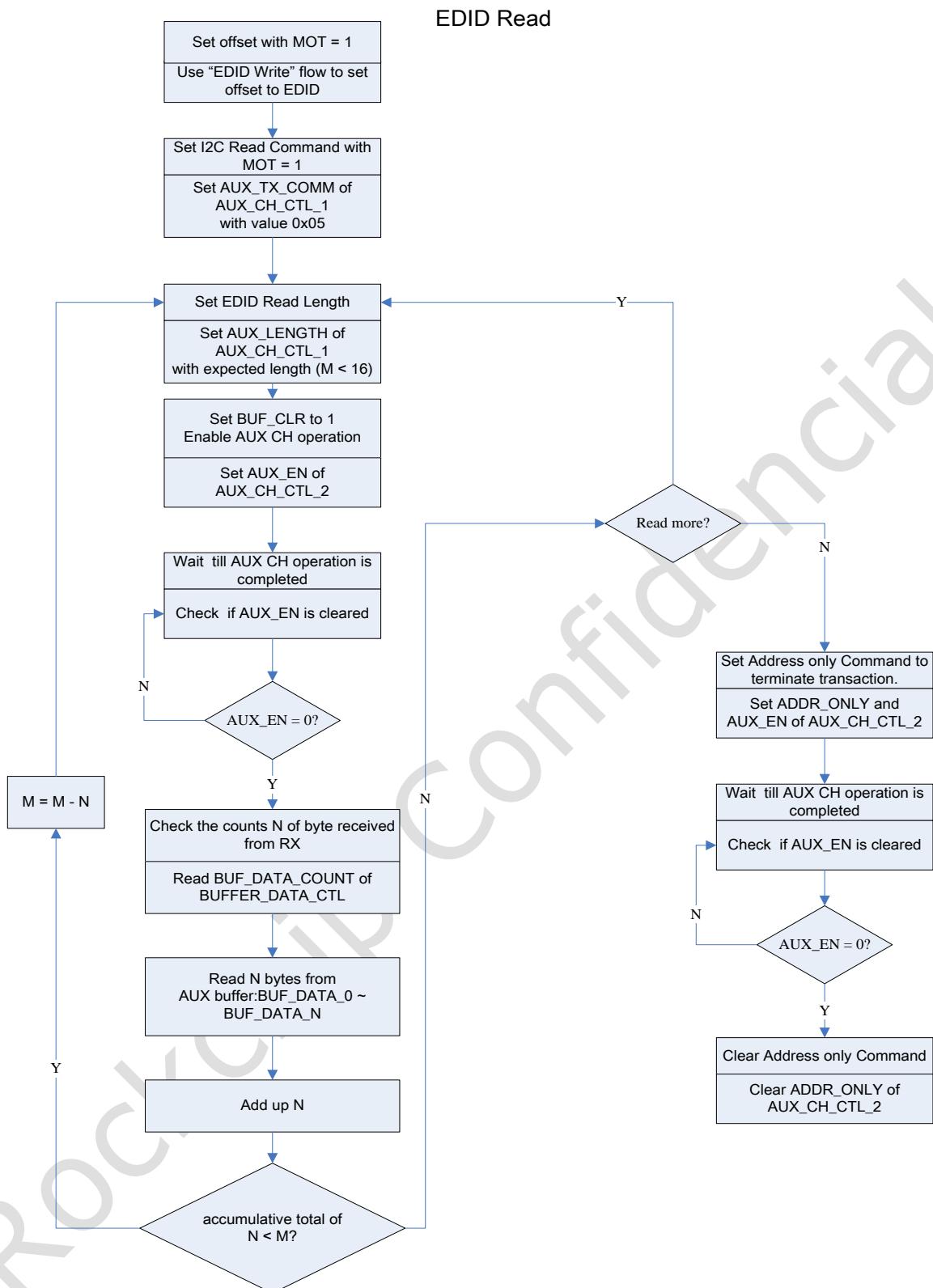




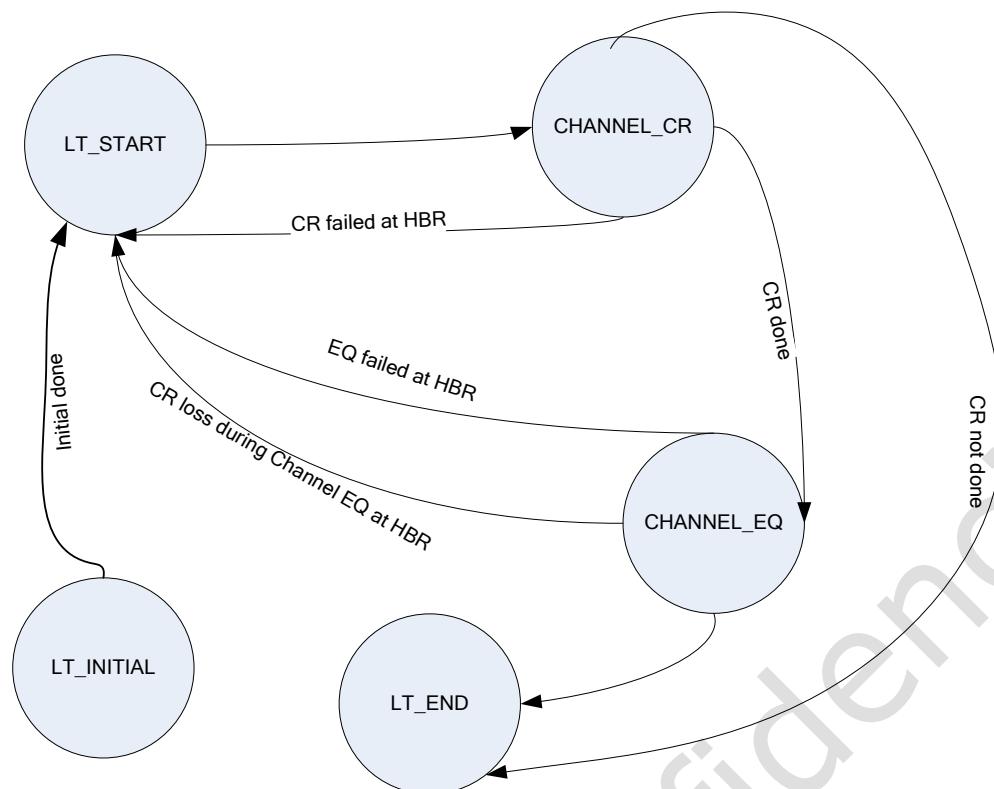
How to Write into EDID space in DP Rx



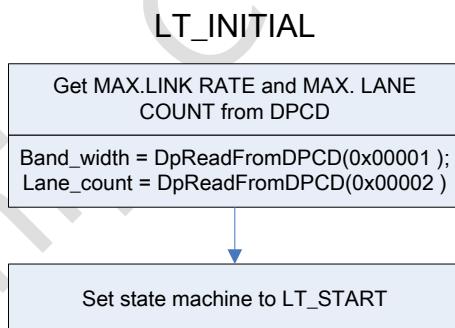
How to READ from EDID space in DP Rx



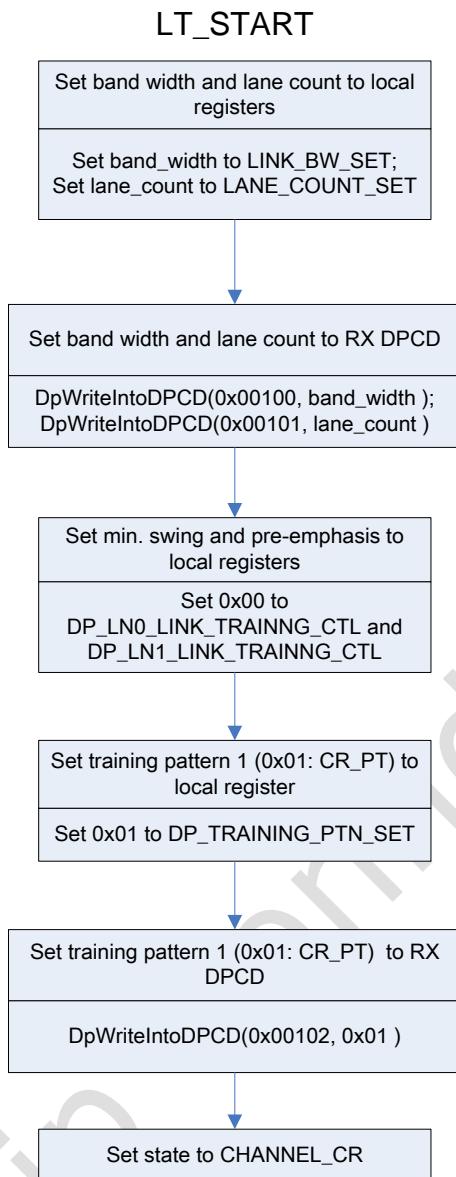
How to do SW link training
State Machine of SW Link Training



State LT_INITIAL



State LT_START



State CHANNEL_CR

Refer to 错误!未找到引用源。. Link Training Initial and Clock Recovery Training

State CHANNEL_EQ

Refer to 错误!未找到引用源。.

How to setup main stream attribute data

Attribute of Video timing

Chip hardware setups attribute of video timing automatically.

Attribute of Color Depth

Set IN_BPC of with VIDEO_CTL_2 correct value.

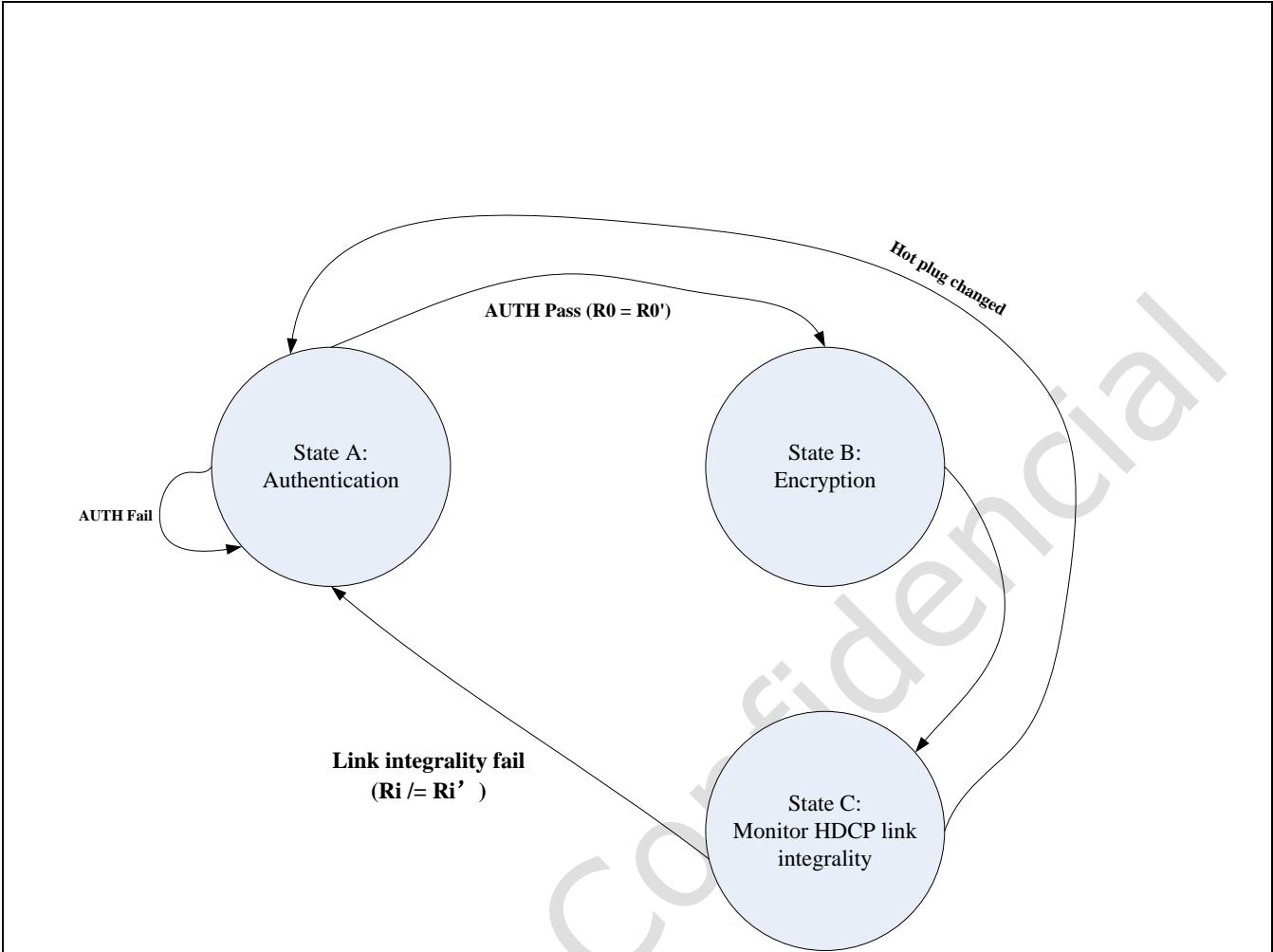
Attribute of Color Space

Set IN_COLOR_F of VIDEO_CTL_2 with correct value.

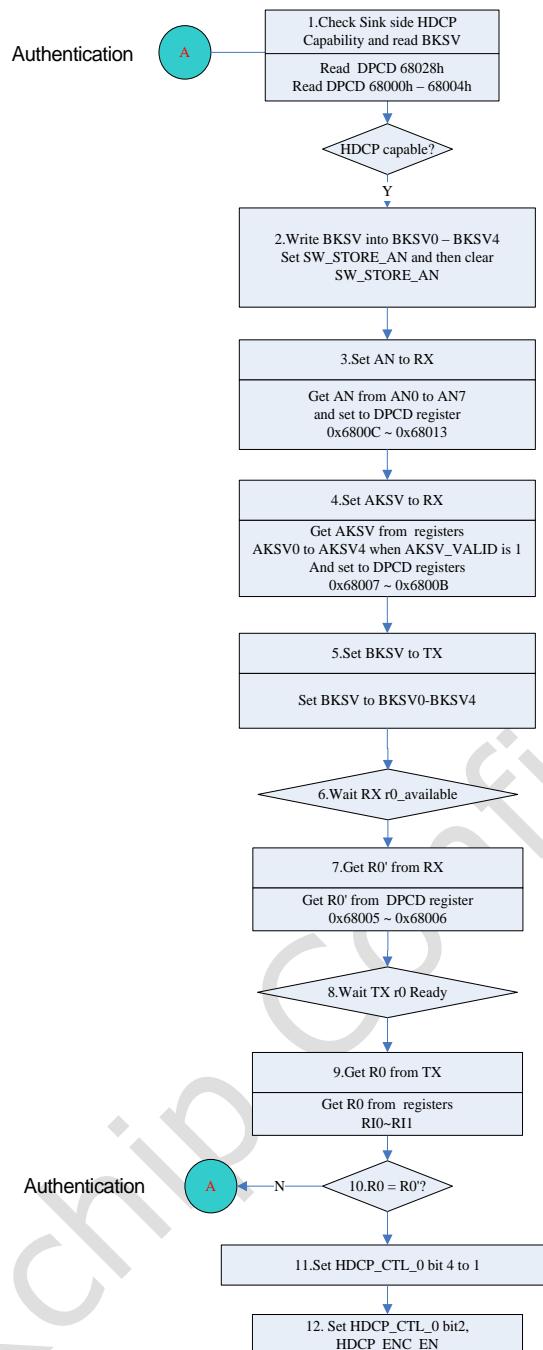
IN_YC_COEFFI of VIDEO_CTL_3 [7] also must be set.

How to do HDCP authentication and encryption

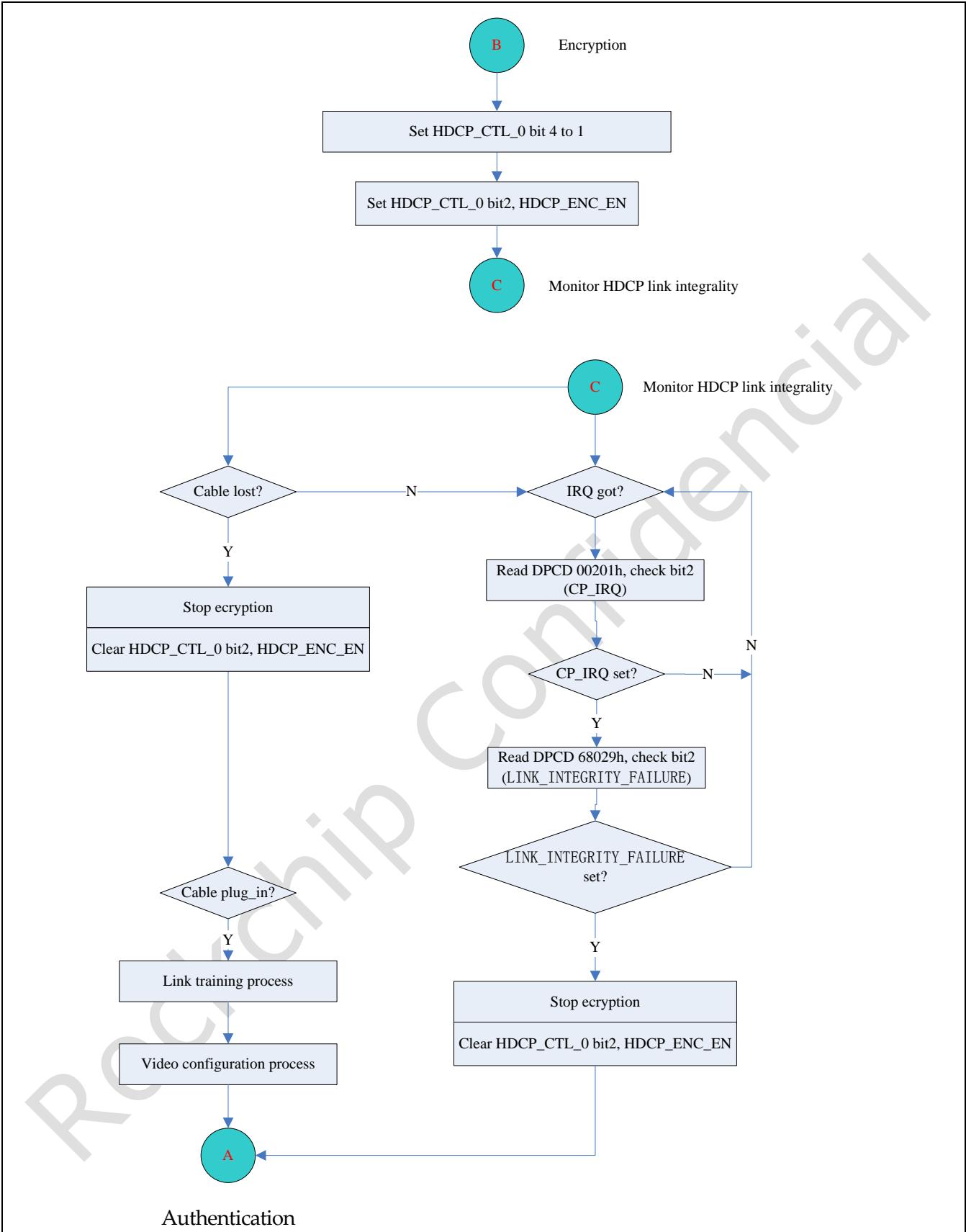
SW HDCP State Machine



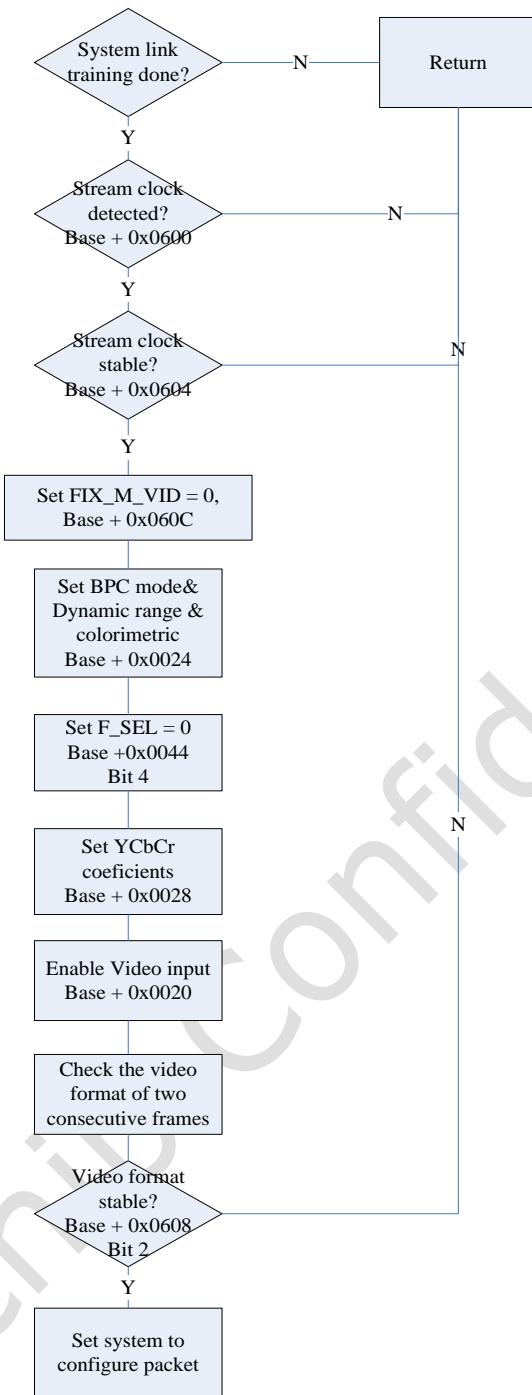
SW HDCP Flowchart



Note that BKSV to BKSV0~BKSV4 are loaded two times in step2 and in step5. With the first BKSV writing, AKSV starts to be loaded and SW_STORE_AN function is enabled. As another function, validity of BKSV is possible by the bit filed, BKSV_VALID. In the other hand, the second BKSV writing starts the R0 calculation.



How to configure video



Slave mode video configuration process (M value auto-generated)

Note: Usually, you do not need to set FIX_M_VID to 1. If FIX_M_VID is 0, then the hardware calculated M_VID value is used. But, if FIX_M_VID must be set to 1 by any reason, then M_VID_0, M_VID_1 and M_VID_2 should be set by using following formula.

$$M_VID = F_STRM_CLK * N_VID / FLS_CLK$$

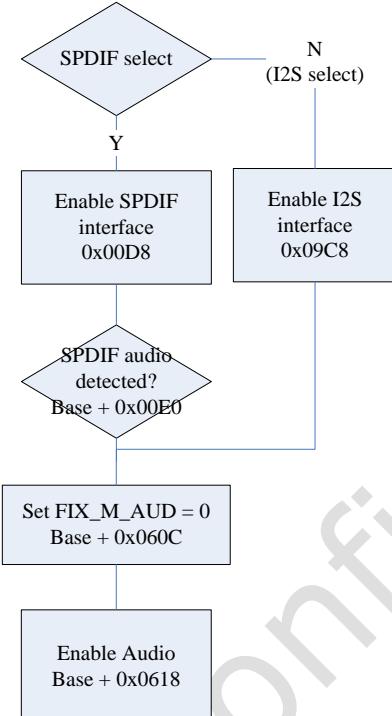
N_VID must be choose let the result of this equation is an integer, for example N_VID is 13500 (0x34bc) in 2.7G and 8100 (0x1fa4) in 1.62G.

$$2.7G: M_VID = F_STRM_CLK * 0x34BC / 135M$$

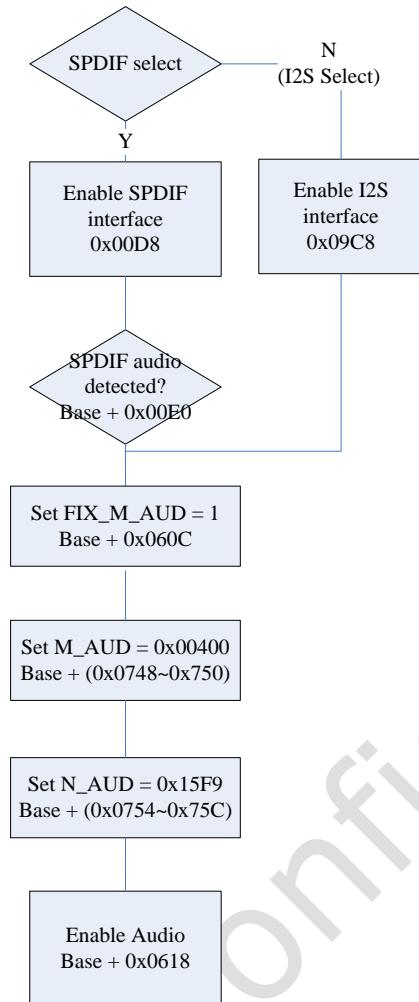
$$1.62G: M_VID = F_STRM_CLK * 0x1FA4 / 81M$$

For example, if input is 1400x1050/108M, RGB888, 2.7G,
→ M_VID = $108 \times 0x34BC / 135 = 0x2A30$,
→ set M_VID_0 = 0x30, set M_VID_1 = 0x2A, set M_VID_2 = 0.

How to configure audio



Slave mode audio configuration process (M value auto-generated)



Slave mode audio configuration process (Register defined M value, 48 KHz, 2.7 G)

Note: Usually, you do not need to set FIX_M_AUD to 1. If FIX_M_AUD is 0, then the hardware calculated M_AUD value is used. But, if FIX_M_AUD must be set to 1 by any reason, then M_AUD_0, M_AUD_1, M_AUD_2 and N_AUD_0, N_AUD_1, N_AUD_2 should be set by using following formula.

$$M_AUD = 512 * Faud_sample * N_AUD / 2 * Fls_clk$$

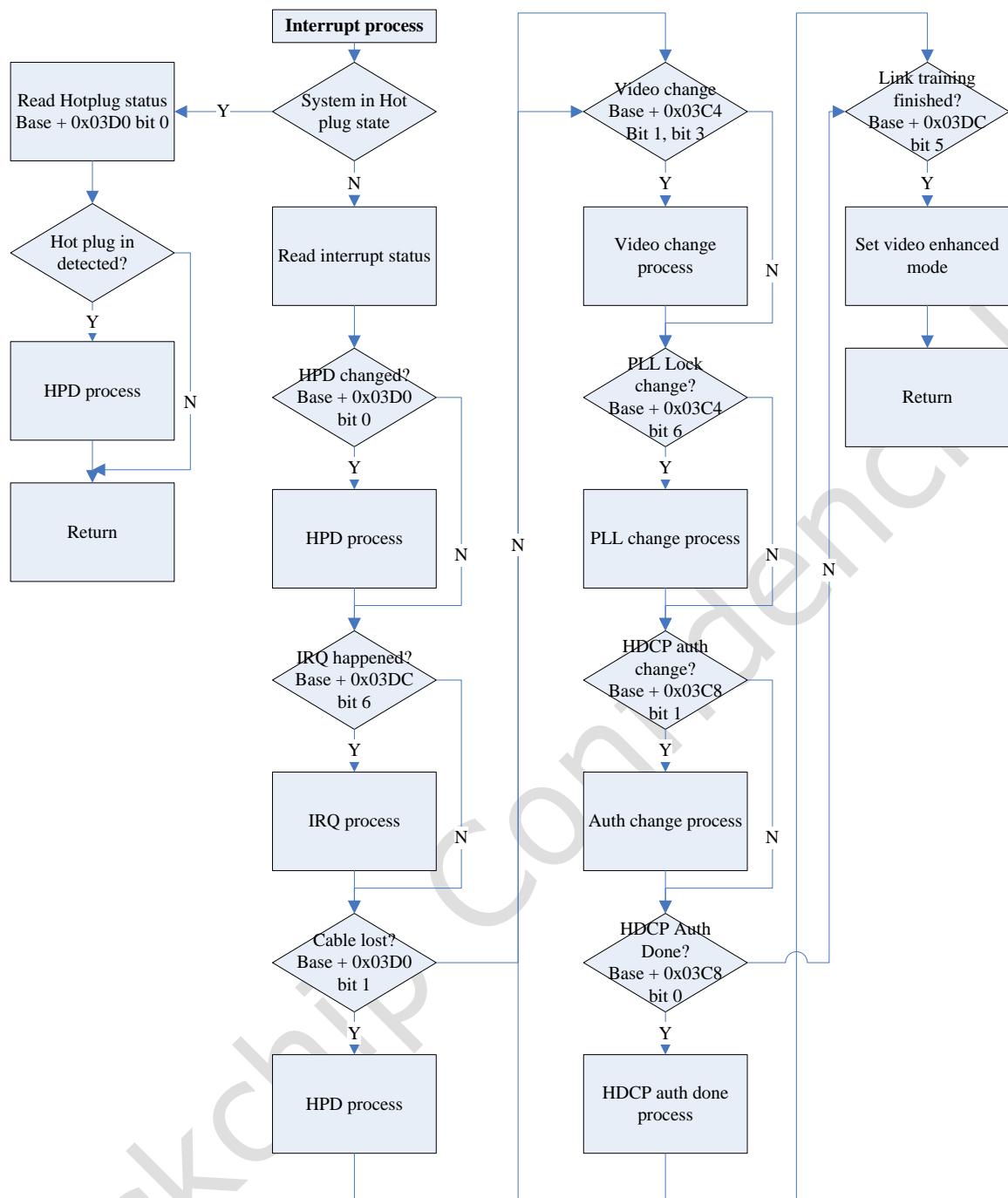
$$2.7G \quad M_AUD = 512 * Faud_sample * N_AUD / 270,000,000$$

$$1.62G \quad M_AUD = 512 * Faud_sample * N_AUD / 162,000,000$$

Please check the 错误!未找到引用源。 for the examples of M_AUD and N_AUD.

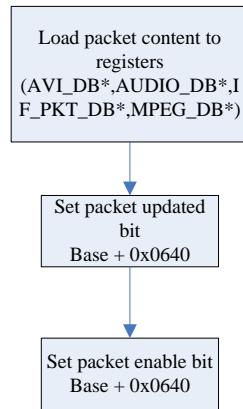
Examples of M_AUD and N_AUD

How to PROCESS interrupt

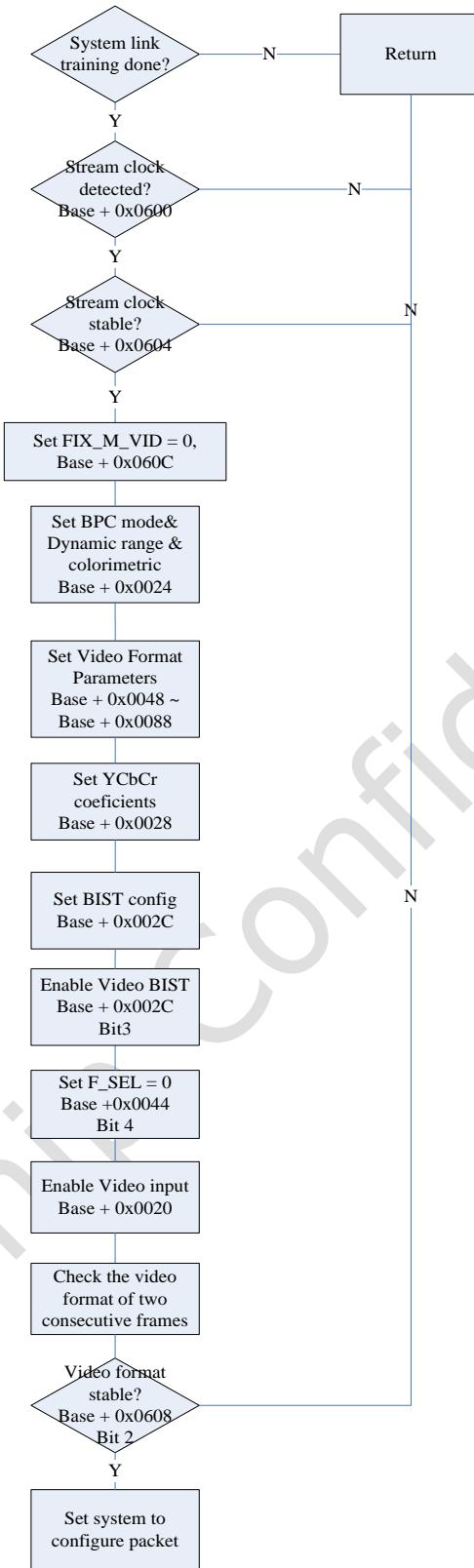


Interrupt process

How to Send Secondary-data Packets



How to configure Video BIST



11.4 Interface Description

11.4.1 Video Input Source

In RK3288, the eDP TX video source comes from vop0 or vop1.

GRF_SOC_CON6[5] == 1'b0, video source from vop0.

GRF_SOC_CON6[5] == 1'b1, video source from vop1.

11.4.2 Audio Input Source

In RK3288, the eDP TX audio source can come from I2S_8CH and SPDIF, and the SPDIF source comes from SPDIF_2CH or SPDIF_8CH.

GRF_SOC_CON2[1] == 1'b0, SPDIF source from SPDIF_8CH.

GRF_SOC_CON2[1] == 1'b1, SPDIF source from SPDIF_2CH

11.4.3 Hot plug

There is a hot plug input signal to eDP TX. This signal is muxed with GPIO7_B[3], and is enabled by "GPIO7B_IOMUX[7:6] = 2'b10".

11.5 Application Notes

Please refer to CH.eDP TX IP for detail information.

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Chapter 12 MIPI D-PHY

12.1 Overview

The MIPI D-PHY is compliant with the MIPI D-PHY interface specification, revision 1.1. The D-PHY can be reused for both master and slave applications. The lane modules are bidirectional with HS-TX, HS-RX, LP-TX, LP-RX, and LP-CD functions.

The D-PHY is targeted for the digital data transmission between a host processor and display drivers or camera interfaces in mobile applications, supporting a maximum effective bit rate of 1.5Gbps per lane. The assembled four-data-lane system enables up to 6Gbps aggregate communication throughputs, delivering the bandwidth needed for high-throughput data transfer.

There were three D-PHY in RK3288, one is for DSI, one is for CSI, another can configure to DSI or CSI.

The MIPI D-PHY supports the following features:

- Attachable PLL clock multiplication unit for master-side functionality
- Flexible input clock reference – 5MHz to 500MHz
- 50% DDR output clock duty-cycle
- Lane operation ranging from 80Mbps to 1.5Gbps in forward direction
- Aggregate throughput up to 6Gbps with four data lanes
- PHY-Protocol Interface (PPI) for clock and data lanes
- Low-power Escape modes and Ultra Low Power state
- $1.8V \pm 10\%$ analog supply operation
- $1.0V \pm 10\%$ digital supply operation

12.2 Block Diagram

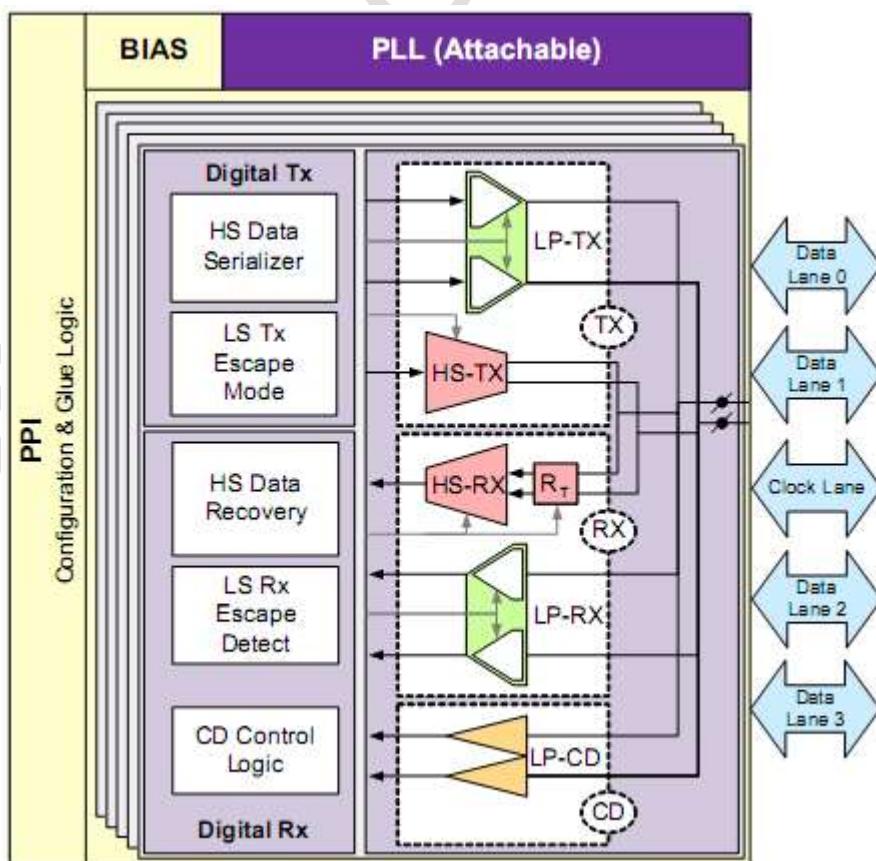


Fig. 12-1 MIPI D-PHY detailed block diagram

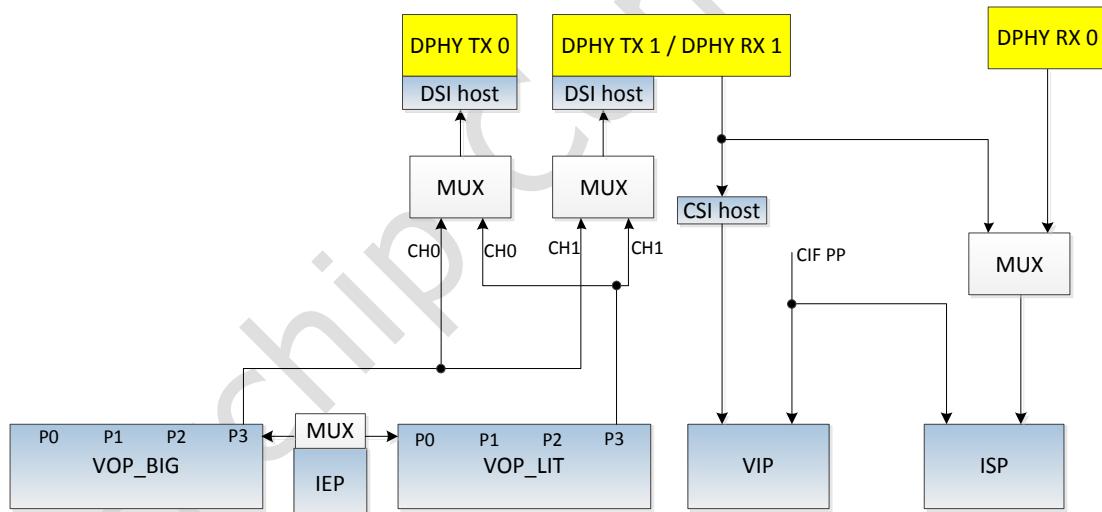
HS Driver/Receiver
Implements high-speed TX and RX functionalities
Replicated for each lane
LP Driver/Receiver
Implements the low-power TX and RX functionalities
Replicated for each lane
Contention Detectors
Used for contention detector when there is a direction change in the low-power mode
Replicated for each lane
PLL
Generates high-speed clocks required in Master Mode
Can be attached to D-PHY for Master applications
Digital Block: Includes all control logic as well as PPI

MIPI CSI2 D-PHY configuration contains one Clock Lane Module and four Data Lane Modules. Each of these PHY Lane Modules communicates via two lines to a complementary part at the other side of the Lane Interconnect.

12.3 Function Description

12.3.1 System Connection

There are three D-PHY in RK3288, their connection are shown as following figure:



D-PHY RX0

D-PHY RX0 is only used for RX, receive the Mipi Camera data then send to ISP. In this mode, you must set grf_con_isp_dphy_sel (bit[1] of GRF_SOC_CON6) to 1'b0.

D-PHY TX0

D-PHY TX0 is only used for TX, send the data from VOP_BIG or VOP_LIT to the Mipi Panel. You can select data from VOP_BIG or VOP_LIT by setting grf_con_dsi0_lcdc_sel (bit[6] of GRF_SOC_CON6)

D-PHY TX1RX1

D-PHY TX1RX1 can configure to for TX or for RX.

The D-PHY can be configured to for TX by setting grf_dphy_tx1rx1_masterslavez = 1'b0, and setting grf_dphy_tx1rx1_basedir = 1'b0, and you can set the grf_con_dsi1_lcdc_sel (bit[9] of GRF_SOC_CON6) to select the data from VOP_BIG or from VOP_LIT.

If you want the D-PHY work as for RX, you must set grf_dphy_tx1rx1_masterslavez = 1'b1, and set grf_dphy_tx1rx1_basedir = 1'b1, then you must select the data from D-PHY RX1 to CSI Host or ISP by setting grf_con_isp_dphy_sel (bit[1] of GRF_SOC_CON6)

The detail register setting is as following table:

Table 12-1 Register Config For D-PHY Mode Select

TX0 + VOP_BIG	TX0 + VOP_LIT	TX1RX1 + VOP_BIG	TX1RX1 + VOP_LIT
bit[6] of GRF_SOC_CON6 = 1'b0	bit[6] of GRF_SOC_CON6 = 1'b1	bit[9] of GRF_SOC_CON6 = 1'b0	bit[9] of GRF_SOC_CON6 = 1'b1
		bit[14] of GRF_SOC_CON6 = 1'b0	bit[14] of GRF_SOC_CON6 = 1'b0
		bit[14] of GRF_SOC_CON14 = 1'b1	bit[14] of GRF_SOC_CON14 = 1'b1
		bit[15] of GRF_SOC_CON14 = 1'b0	bit[15] of GRF_SOC_CON14 = 1'b0
bit[8:7] of GRF_SOC_CON6	bit[8:7] of GRF_SOC_CON6	bit[11:10] of GRF_SOC_CON6	bit[11:10] of GRF_SOC_CON6
bit[11:0] of GRF_SOC_CON8	bit[11:0] of GRF_SOC_CON8	bit[15:0] of GRF_SOC_CON9	bit[15:0] of GRF_SOC_CON9
bit[10:8] of GRF_SOC_CON15	bit[10:8] of GRF_SOC_CON15	bit[12] of GRF_SOC_CON14	bit[12] of GRF_SOC_CON14
		bit[7:4] of GRF_SOC_CON15	bit[7:4] of GRF_SOC_CON15
bit[0] of GRF_SOC_CON16	bit[0] of GRF_SOC_CON16	bit[1] of GRF_SOC_CON16	bit[1] of GRF_SOC_CON16
RX0 + ISP	TX1RX1 + ISP	TX1RX1 + CSI_Host + VIP	
bit[1] of GRF_SOC_CON6 = 1'b0	bit[1] of GRF_SOC_CON6 = 1'b1	bit[14] of GRF_SOC_CON6 = 1'b1	
	bit[14] of GRF_SOC_CON6 = 1'b1	bit[13] of GRF_SOC_CON14 = 1'b0	
	bit[13] of GRF_SOC_CON14 = 1'b1	bit[14] of GRF_SOC_CON14 = 1'b0	
	bit[14] of GRF_SOC_CON14 = 1'b0	bit[15] of GRF_SOC_CON14 = 1'b1	
bit[15:0] of GRF_SOC_CON10	bit[15:0] of GRF_SOC_CON9	bit[15:0] of GRF_SOC_CON9	
bit[10:0] of GRF_SOC_CON14	bit[12] of GRF_SOC_CON14	bit[12] of GRF_SOC_CON14	
bit[3:0] of GRF_SOC_CON15	bit[7:4] of GRF_SOC_CON15	bit[7:4] of GRF_SOC_CON15	

12.3.2 Operating Modes

This section describes the various operating modes of the MIPI D-PHY, the following Figure illustrates the various modes of the MIPI D-PHY during initialization and active operating mode.

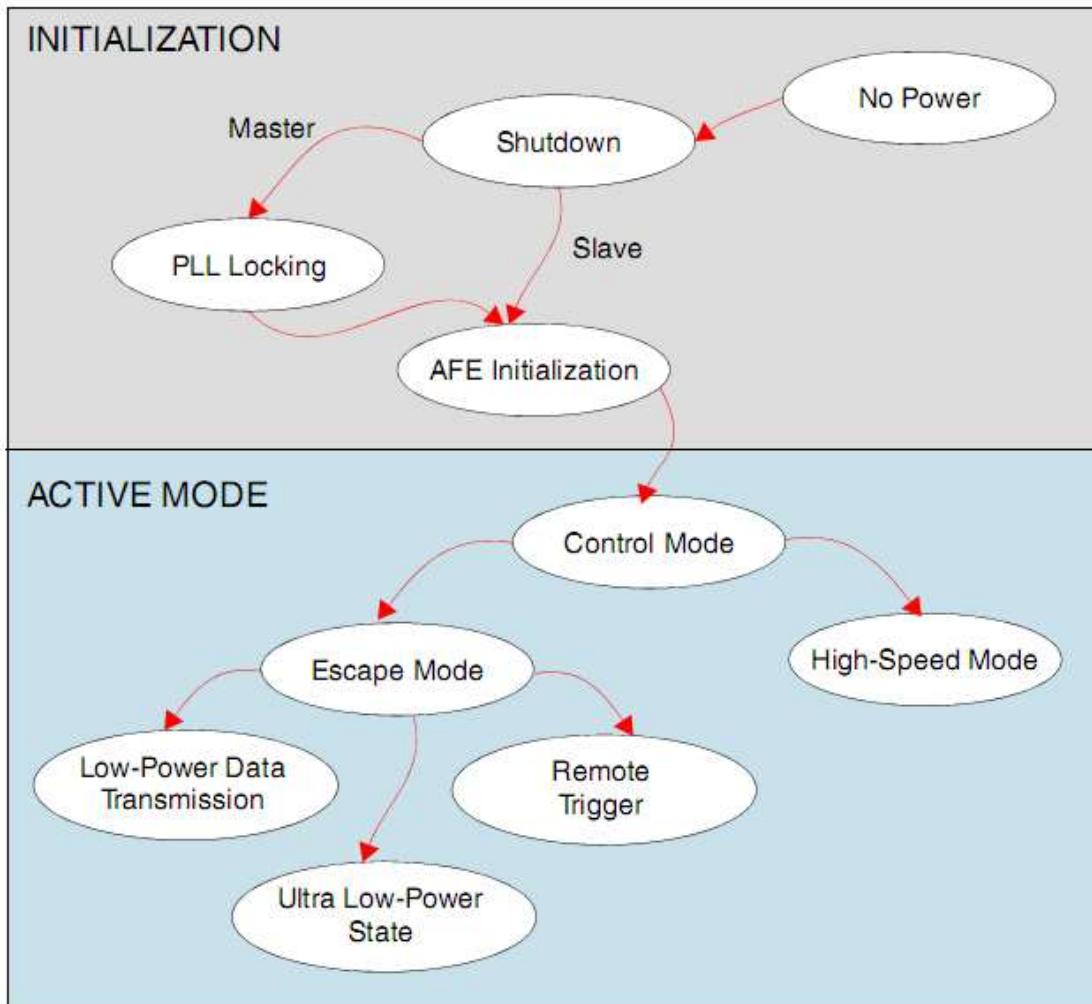


Fig. 12-2 MIPI D-PHY Initialization from Shutdown to Idle Modes

Initialization

No Power Mode

The No Power mode is characterized by the non-existence of any supply voltage applied to MIPI D-PHY. In order to get to the powered modes, proper voltages should be applied sequentially to MIPI D-PHY, this task is usually done by the SoC PMU or eventually by global powering up sequence.

The recommended powering up sequence is that the core voltage (VDD) powers up first and the I/O voltage (AVDD) powers up next. This is not considered as a constraint, but instead a guideline, as it results in the best-case operating scenario, where power-down currents are kept to a minimum.

For complex SoCs, it is likely that core voltage islands exist for different main blocks/macros, while the I/O voltage is always present. This means that VDD may power up after the I/O voltage and not follow the previous guideline. This is not considered a problem because MIPI D-PHY supports power collapsing, which ensures valid logical levels across power domains even when one of the supplies is not present at a given time.

The digital core voltage (VDD) and I/O analog voltage (AVDD) domains are isolated by the use of level shifter cells. No additional leakage is expected when there is a lack of VDD and/or AVDD.

Shutdown Mode

This mode is the lowest power consumption mode, where all analog blocks are disabled, and digital logic is reset. The current consumption is given by the analog stand-by current and the digital logic leakage current. It is entered asynchronously when RSTZ and SHUTDOWNZ are in low state. It should be ensured that the TESTCLR signal is asserted by default, as it acts as an active high reset to the control block responsible for the configuration values preset. In this mode, the differential lines of DATAN/DATAP and CLKN/CLKP are high impedance (Hi-Z).

Depending on the MIPI D-PHY usage, some additional steps can be performed. By default, MIPI D-PHY is configured to work only on the lower operation range of 80-110 Mbps. If higher bit rate operation is required, you should set the register `hsfreqrange` (HS RX Control of Lane 0) with the proper code. If MIPI D-PHY is expected to work always at the same bit rate, this additional step can be performed while in Shutdown mode as the control interface is independent of the rest of MIPI D-PHY. Conversely, if the MIPI D-PHY is expected to change the bit rate after initialization, `hsfreqrange` should be updated while in Idle mode. For more information on these options, see "Active Modes".

In addition, when working in Master mode, the PLL must be configured to select the proper input frequency and the desired output frequency, which determines the bit rate on the transmission path. For more information, see "PLL Requirements".

When `RSTZ` and `SHUTDOWNZ` are set to logic high level, MIPI D-PHY leaves this state and starts an initialization procedure.

PLL Locking Mode and AFE Initialization

The MIPI D-PHY consists of four data lanes, but applications can use four or lesser number data lanes. In such cases, you are granted access to individual enabling signals (`ENABLE_N`) that control which lanes should be used and evolve through all the necessary initialization steps. It is assumed that such configurations are static or at least are stable prior to leaving the Shutdown mode.

After the reset signals (`RSTZ` and `SHUTDOWNZ`) are released, the MIPI D-PHY begins an initialization sequence that allows its correct operation. Sequence of the release of signals is not critical but it is recommended that `SHUTDOWNZ` precedes `RSTZ`. It is also assumed that the `CFG_CLK` signal is available and stable by that time.

If there are no test or configuration operations to be performed, the `TESTCLR` signal can be kept at logic high level. Otherwise, the `TESTCLR` must be de-asserted to bring the control logic out of reset and allow for the necessary configuration steps through the control interface.

The D-PHY specification has many timing intervals which have to be followed to ensure proper operation. The fact that those timing intervals often have both a relative Unit Interval (UI) and absolute timing components, makes it difficult to meet the maximum and minimum values across the complete data rate range (80 Mbps-1.5 Gbps) by just using default settings. To cope with this, MIPI D-PHY implements a set of frequency ranges that needs to be configured prior to starting normal operation. Those ranges, when in Master operation, also define the operating bit rate, assuming `REFCLK` is equal to 27MHz. If the desired bit rate or `REFCLK` frequencies are different, directly configure the PLL as described in "PLL Requirements". All these steps come under the category of configurations that need to be performed through the control interface with `TESTCLR` de-asserted.

The following Table lists the frequency ranges.

Table 12-2 Frequency Ranges

Range (Mbps)	hsfreqrange[5:0]	Default Bit Rate (Mbps)
80-90 (default)	000000	81
90-100	010000	90
100-110	100000	108
110-130	000001	126
130-140	010001	135
140-150	100001	144
150-170	000010	162
170-180	010010	180
180-200	100010	198

Range (Mbps)	hsfreqrange[5:0]	Default Bit Rate (Mbps)
200-220	000011	216
220-240	010011	234
240-250	100011	243
250-270	000100	270
270-300	010100	297
300-330	000101	324
330-360	010101	360
360-400	100101	396
400-450	000110	450
450-500	010110	486
500-550	000111	540
550-600	010111	594
600-650	001000	648
650-700	011000	684
700-750	001001	738
750-800	011001	783
800-850	101001	846
850-900	111001	900
900-950	001010	945
950-1000	011010	999
1000-1050	101010	1044
1050-1100	111010	1080
1100-1150	001011	1134
1150-1200	011011	1188
1200-1250	101011	1242
1250-1300	111011	1296
1300-1350	001100	1350
1350-1400	011100	1386
1400-1450	101100	1440
1450-1500	111100	1494

The hsfreqrange field is accessible through control code 0x44 ("HS RX Control of Lane 0") when TESTDIN[7] = 0 and TESTDIN[0] = 0. The hsfreqrange[5:0] field is programmed with the

contents of TESTDIN[6:1] at every rising edge of TESTCLK.

If the MIPI D-PHY is configured to work as a Master (MASTERSLAVEZ=1'b1), the PLL becomes active and MIPI D-PHY goes through the PLL Locking mode, in which the MIPI D-PHY waits for the PLL to acquire lock, indicated by the LOCK output going high. A valid REFCLK (FREFCLK) should be provided.

Following the PLL lock, the rest of the AFE is initialized leading to the enabling of the low-power drivers. After completing these transitory states, the lines go to the Stop state (LP = 11) and the TX achieves active mode.

In the case of a Slave configuration (MASTERSLAVEZ = 1'b0), PLL is inactive, therefore only the rest of AFE initialization takes place.

The initialization sequence determines that bandgap and biasing blocks are enabled first. After the related voltage and current references get settled, a second step is triggered where the internal calibrations are performed, and this can include internal resistors, receivers offset compensation, and so on.

When this second step is complete, the control is passed to the lanes, which handle the power management for LP/HS requests, enabling or disabling the corresponding drivers and receivers.

All initialization steps are performed once the STOPSTATEDATA_N and STOPSTATECLK outputs get asserted.

Initialization period (TINIT) is a protocol dependent parameter with a minimum 100 μ s defined by the specification. The MIPI D-PHY does not set any limit to the initialization period, meaning it drives a Stop state (LP-11) immediately after the AFE initialization and PLL lock when in Master mode, or alternatively starts decoding the LP commands after the AFE initialization in Slave mode. It is up to the controller or the upper layers to ensure the proper initialization times through the correct handling of MIPI D-PHY control signals. This time must conform to D-PHY specification and obey the minimum specified 100 μ s value.

Following Figure shows a possible power-up sequence for a Slave application when the default setting is 80-110 Mbps operation.

If the desired operation mode is different from the default one, additional configuration steps can be performed during the T2+T3 time window.

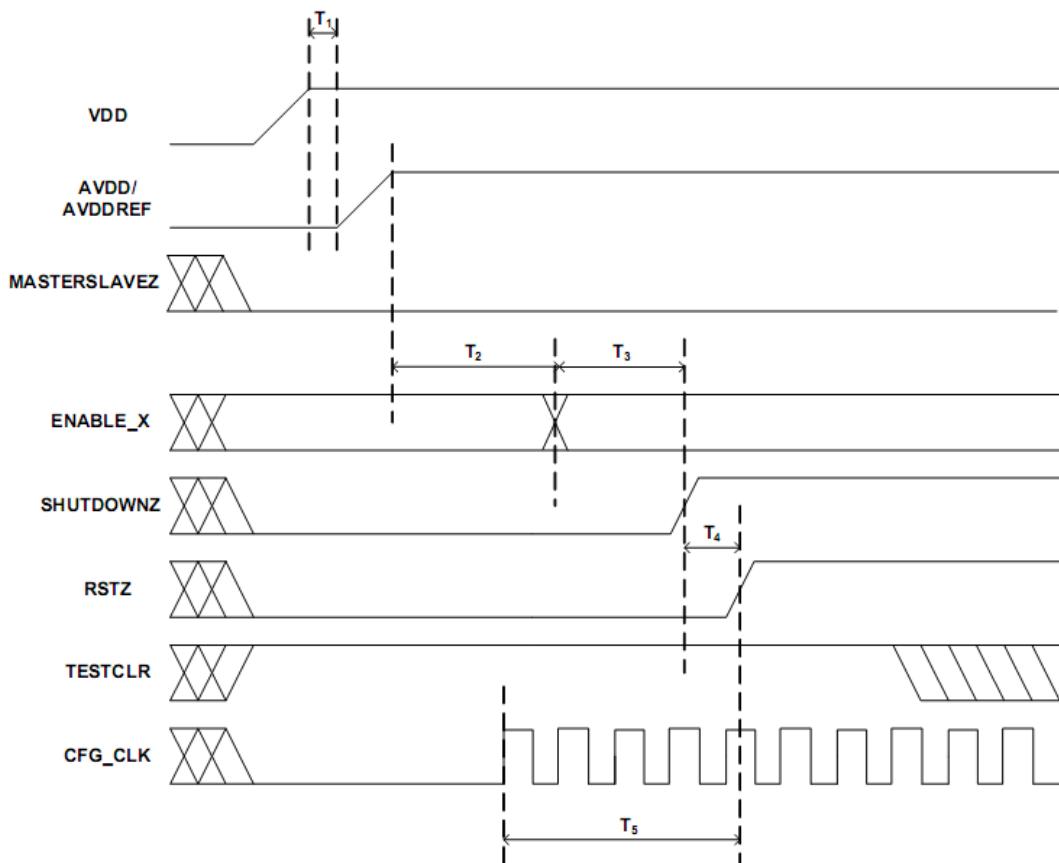


Fig. 12-3 Power-Up Sequence for Slave Operation

Table 12-3 Power-Up Sequence Timings

Parameter	Symbol	Minimum	Typical	Units
Delay from stable VDD to AVDD/AVDDREF start	T1	0	1	us
Delay from stable AVDD/AVDDREF to ENABLE_X definition	T2	0		ns
Delay for assertion of SHUTDOWNZ after ENABLE_X definition	T3	5		ns
Delay from SHUTDOWNZ assertion to RSTZ assertion	T4	5		ns
Time for CFG_CLK setting before the assertion of RSTZ	T5	1		CFG_CLK

Active Modes

Idle Mode

Idle mode is the default operating mode. After the initialization is completed (analog calibrations and PLL locking for Master configurations), the MIPI D-PHY remains in this default mode until some request is placed. The request is placed either by the protocol layer for TX, or directly through the sequence of low-power signals in the lanes in case of RX. While in control mode, the transmitter side sets the LP-11 state in the lines - this is called the Stop state. The receiver side remains in control mode while receiving LP-11 in the lines. Any request must start from and end in Stop state. Following a request, a lane can leave control mode for either high-speed data transfer mode, Escape mode, or Ultra Low Power state.

High-Speed Data Transfer Mode

Once the initialization sequence is completed, the MIPI D-PHY remains in control mode, which is the default operating mode, until some request appears. High-speed is one of the possible requests at this point. High-speed data transfer occurs in bursts. Only during these bursts the lane is in high-speed mode. A high-speed burst must start from and return to a Stop state (control mode). A high-speed burst allows for the transmission of payload data by the data lanes. Inherent to such data transmission is the existence of a valid DDR clock in the clock lane. High-speed data bursts are independent for each lane, which means that each data lane can start and end a high-speed transmission independently of the state of the remaining data lanes.

A burst contains the low-power initialization sequence, the high-speed data payload, and also the end of transmission sequence.

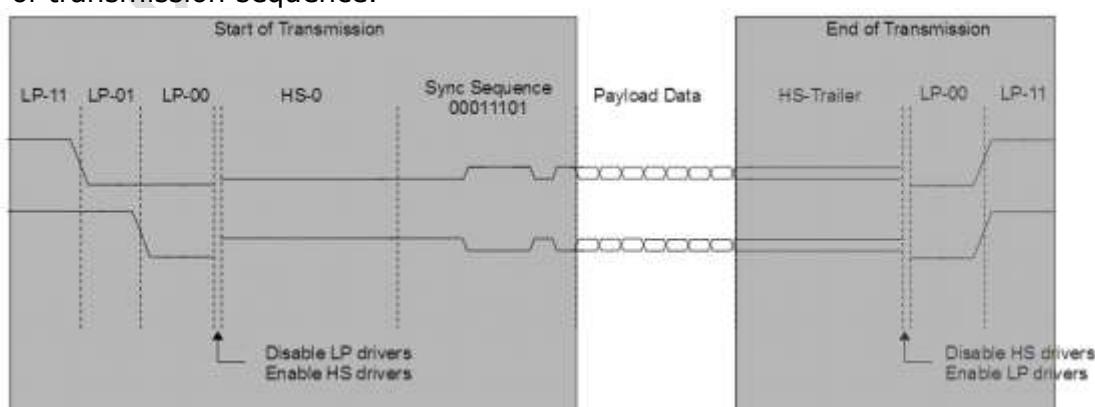


Fig. 12-4 HS Data Transfer Sequence

From the transmitter side, high-speed mode is entered when the corresponding TXREQUESTHS input is set high (assuming that MIPI D-PHY is in Stop state). This request is processed in a slightly different way for clock and data lanes. For a clock lane, the high-speed request is followed by the transmission of a low-power sequence that represents this request for the

receiver side (a lane high-speed request). Only after generating this sequence the low-power driver is disabled, and the high-speed driver enabled. After the time necessary to settle, the transmission of the high-speed DDR clock starts. For a data lane, the high-speed request also starts with a lane high-speed request, and in addition, extend the payload data with a leader and a trailer sequence that allow for the receiver synchronization. The transmission of such sequence requires the existence of a valid high-speed clock signal in the clock lane.

When the high-speed request input is disabled, each lane leaves the high-speed data transmission mode. It is important that a clock lane must be in high-speed mode during the complete high-speed data transmission state of all the lanes. The clock lane must enter the high-speed mode before a high-speed data transmission begins and it must not leave this state before all the lanes finish their respective high-speed data transmission bursts. The operation sequence when leaving the high-speed mode is also slightly different for data and clock lanes. For a clock lane, the high-speed transmission always ends with a HS-0 state, followed by the disabling of the high-speed driver, and enabling of low-power driver. As for a data lane, the transmission ends with the differential state opposite to the last bit transmitted, followed by the disabling of the high-speed driver, and enabling of the low-power driver.

The receiver side enters the high-speed mode following the sequence of low-power states in the lines: LP-11, LP-01, and LP-00. This sequence is seen as a high-speed mode request, and toggles the enabling of the high-speed receivers. The synchronization is then achieved through the identification of the leader sequence in the received differential high-speed data. Once the synchronization is achieved, the MIPI D-PHY outputs the received bytes through the protocol layer, until a Stop state (LP-11) is detected in the lane.

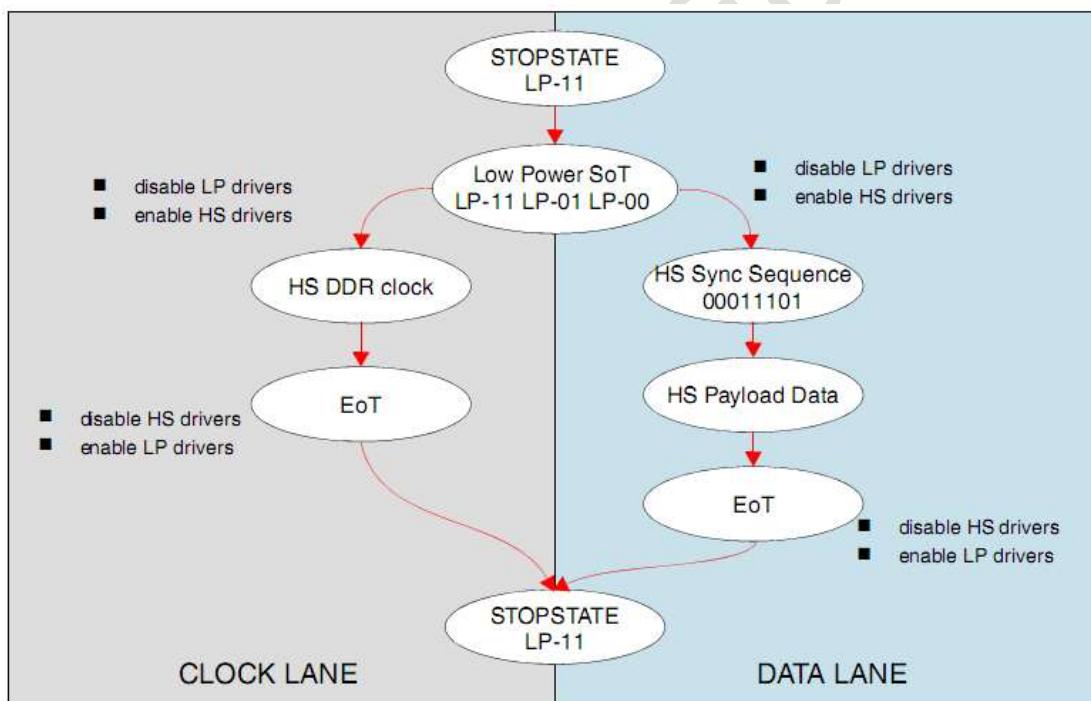


Fig. 12-5 HS Data Transfer State Diagram

The current implementation does not feature EoT processing which should be done at the controller level. This affects the behavior of the RXActiveHs and RXValidHS signals as illustrated in "Timing Diagrams".

Escape Mode

Escape mode is a special mode of operation that uses the data lanes to communicate asynchronously using the low-power states at low-speed. The MIPI D-PHY supports this mode in both directions. A Data Lane enters the Escape mode through an Escape mode entry procedure (LP-11, LP-10, LP-00, LP-01, LP-00), if an LP-11 is detected before reaching LP-00 state, the entry is aborted and the receiver returns to the Stop state. Once the sequence is correctly completed, the transmitter sends an 8-bit command to indicate a requested action.

The following Table shows the Escape mode supported actions. If the entry command is not valid, it is ignored, ERRESC error flag goes high, and the receiver waits until the transmitter returns to the Stop state. The MIPI D-PHY applies Spaced-One-Hot encoding (a Mark state is interleaved with a Space state) on commands and data.

Each symbol consists of the following two parts:

- One-Hot phase
 - Space state

To transmit one bit, a Mark-1 should be sent followed by the Space state. In the case of a zero bit, a Mark-0 should be sent followed by Space state.

Table 12-4 Possible Escape Mode Sequences for Data Lanes

Escape Mode Action	Entry Command	Command
Low-Power Data Transmission	8'b11100001	mode
Ultra-Lower Power State	8'b00011110	mode
Reset Trigger	8'b01100010	trigger
Unknown-3	8'b01011101	trigger
Unknown-4	8'b00100001	trigger
Unknown-5	8'b10100000	trigger

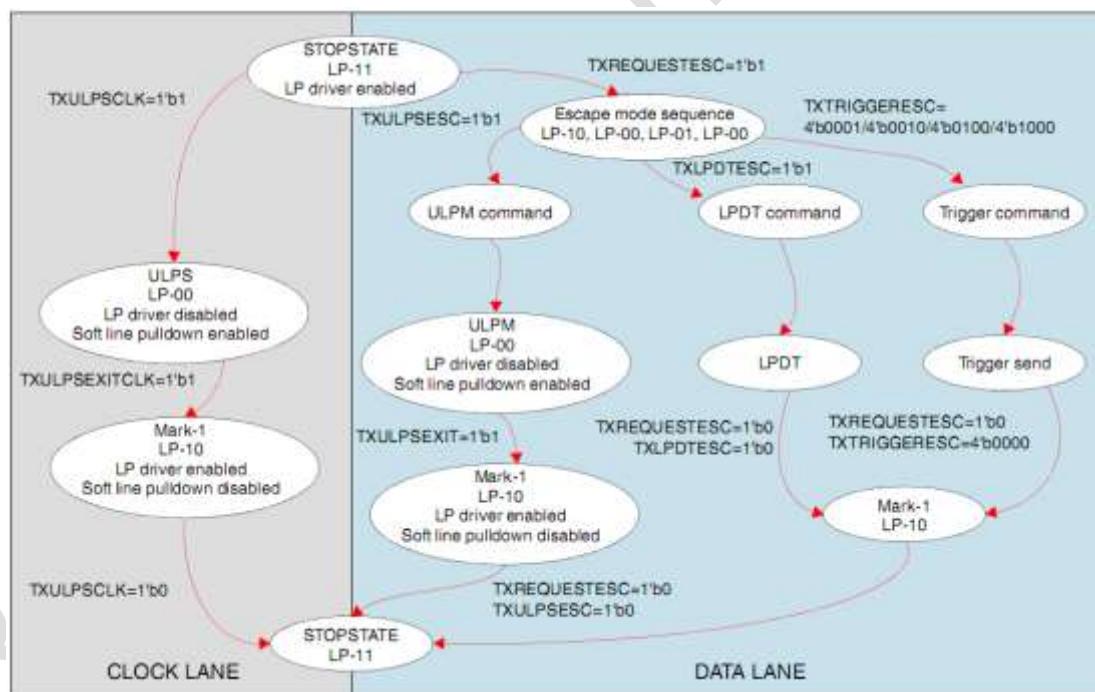


Fig. 12-6 Escape Mode Sequences State Diagram

12.4 Test and Control modes Description

12.4.1 Definition

The MIPI D-PHY contains a set of test and control codes that can be used for testing either under the scope of normal silicon characterization or for production test in the ATE environment. These control codes are primarily used for the configuration of normal operation of the MIPI D-PHY, but for the test purposes they are referred to as test codes.

12.4.2 Interface Timing

This section contains the timing diagrams for configuring a test code in MIPI D-PHY. The standard procedure is two-folded; first the necessary test code is programmed and then the related test data words are fed to the registers.

To configure a test code, have the MIPI D-PHY in shutdown mode (SHUTDOWNZ=0, by set CSIHOST_PHY_SHUTDOWNZ[0]=0) and then reset it (RSTZ=0, by set CSIHOST_DPHY_RSTZ[0]=0). This avoids the transient periods in the operation during re-configuration procedures. It is also recommended to apply a tester reset pulse (TESTCLR = 1, by set CSIHOST_PHY_TEST_CTRL0[1] = 1) before any test code configuration.

The test code programming is done using the following steps:

1. Set the desired test code
 - a) Ensure that CSIHOST_PHY_TEST_CTRL0[1] is set to high.
 - b) Place the 8-bit word corresponding to the test code in MIPIC_PHY_TST_CTRL_1[7:0].
 - c) Set MIPIC_PHY_TST_CTRL_1[16] to high.
 - d) Set CSIHOST_PHY_TEST_CTRL0[1] to low.

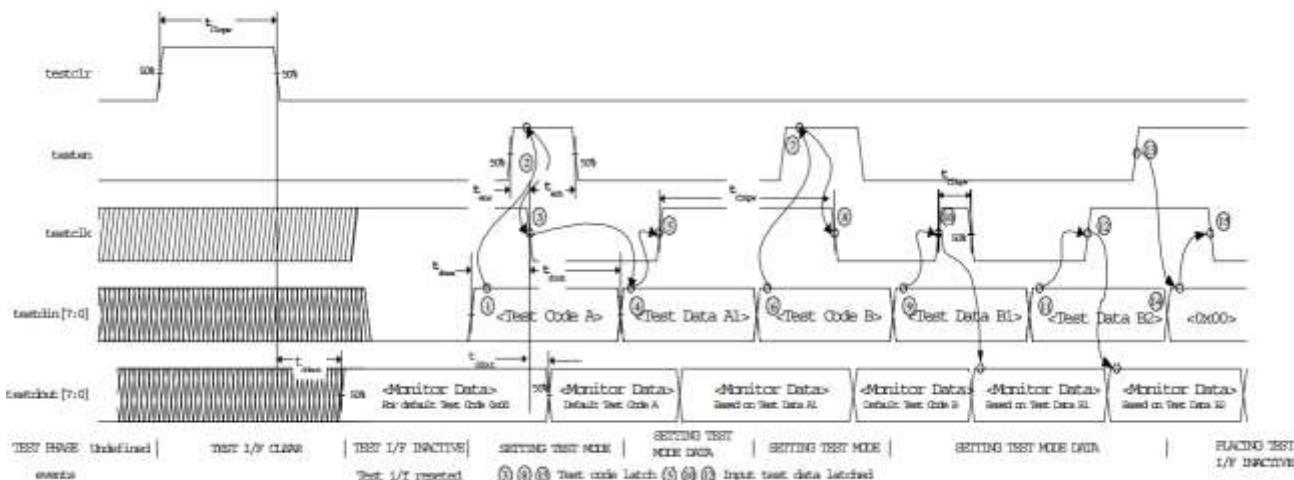
With the falling edge on CSIHOST_PHY_TEST_CTRL0[1] , the MIPIC_PHY_TST_CTRL_1[7:0] is latched internally as the current test code.

2. Set MIPIC_PHY_TST_CTRL_1[16] to low.
 - a) Enter the necessary test data
 - b) Set CSIHOST_PHY_TEST_CTRL0[1] to low, if not done already.
 - c) Place the 8-bit word corresponding to the required test data in MIPIC_PHY_TST_CTRL_1[7:0].
 - d) Set CSIHOST_PHY_TEST_CTRL0[1] to high.
Test data is programmed internally.
 - e) Repeat the steps to add more test data for the same test code.

Repeat the above procedure to program subsequent test codes. Additionally, a test reset procedure (TESTCLR = 1, by set MIPIC_PHY_TST_CTRL0[0]=1) is only needed prior to the first programming operation or if you wish to reset the MIPI D-PHY's configuration to its default values and override any changes made meanwhile.

shows a generic timing diagram for test operation. After a test code is effectively programmed, MIPIC_PHY_TST_CTRL_1[15:8] asynchronously outputs relevant data for that specific test code, whether it is pureread-back data or other meaningful signals.

Fig. 12-7 Testability Interface Timing Diagram



Some important observations on:

- After the required MIPIC_PHY_TST_CTRL0[0]pulse, MIPIC_PHY_TST_CTRL_1[15:8] outputs monitor data for the default test code (0x00). This is used to get information out after the MIPI D-PHY is powered up. Such information may be relevant to determine the operation status of the MIPI D-PHY and may not be related to any test code in particular. For the current implementation, MIPIC_PHY_TST_CTRL_1[15:8] defaults to 0x00.
 - Monitor data for a specific test code may change in response to the following events:
 - The test code is programmed and the default output data appears in MIPIC_PHY_TST_CTRL_1[15:8].
 - The MIPIC_PHY_TST_CTRL_1[15:8] is populated with the test code already configured.
 - The MIPIC_PHY_TST_CTRL_1[15:8] outputs asynchronous internal signals whose timing is unpredictable.
 - Some test codes require two write data operations, where the first one sees the CSIHOST_PHY_TEST_CTRL0[1] going from high to low. It is crucial that the falling edge in the clock does not occur with MIPIC_PHY_TST_CTRL_1[16] asserted or else the current test data will be latched as an erroneous test code.
 - Placing the test interface in inactive mode is best achieved by programming the test code 0x00 as shown in the final sequence in . Although not mandatory, it is highly recommended to close any reconfiguration with this final sequence.
 - An additional scenario is that of a case in which two test codes must be programmed one after the other without any intermediate test data written to the tester. Caution is in order, as the test code is only latched internally with the falling edge of CSIHOST_PHY_TEST_CTRL0[1], the inevitable rising edge must occur only when MIPIC_PHY_TST_CTRL_1[16] is asserted or else the second test code is wrongly interpreted as the test data for the active test code. For details, see

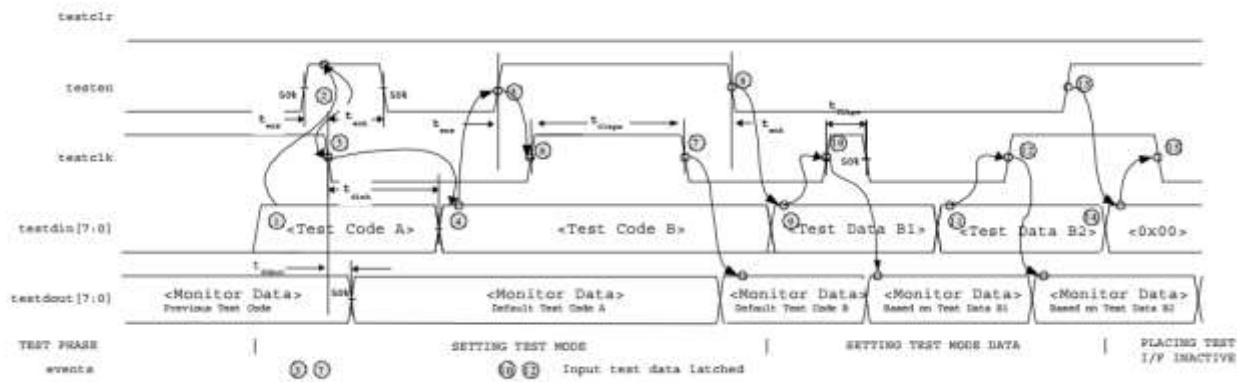


Fig. 12-8 Two Consecutive Test Codes Handling

12.4.3 Test and Control Codes Summary

The performance and testing of the Test and Control mode can be accessed through the Signals listed

Table 12-5 Configuration and Test Interface Signals

Signal name	source	attrt	Reset value	Description
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Signal name	source	attrt	Reset value	Description
TESTCLR	MIPIC_PHY_TST_CTR_L0 [0]	RW	0x1	Function:Vendor-Specific Interface Clear Signal When active, this signal performs vendor-specific interface initialization. Note:This line needs an initial high pulse after power-up for analog programmability default values preset. Active state:High Synchronous to:Asynchronous
TESTEN	MIPIC_PHY_TST_CTR_L_1 [16]	RW	0x0	Function:Vendor-Specific Interface Operation Type Selector When asserted, this signal configures an address write operation on the falling edge of the strobe signal (TESTCLK). When asserted low, it configures a data write operation on the rising edge of strobe signal (TESTCLK). Active state:High Synchronous to:TESTCLK
TESTCLK	MIPIC_PHY_TST_CTR_L0 [1]	RW	0x0	Function:Vendor-Specific Interface Operation Strobe Signal It is used to clock the TESTDIN bus contents into DWC MIPI D-PHY Bidir 4L. Together with TESTEN signal, it controls the operation selection. Active state:High Synchronous to:N/A
TESTDOU_T [7:0]	MIPIC_PHY_TST_CTR_L_1 [15:8]	RW	0x00	Function:Vendor-specific output 8-bit data bus for read-back and internal probing functionalities. Active state:High Synchronous to:TESTCLK
TESTDIN [7:0]	MIPIC_PHY_TST_CTR_L_1 [7:0]	RW	0x00	Function:Vendor-specific input 8-bit data bus for internal register programming and test functionalities access. Active state:High Synchronous to:TESTCLK
CFG_CLK	CRU_CLKGATE5_CON [15]	RW	0x0	Function:Configuration Clock This clock is used for the initialization of DWC MIPI D-PHY Bidir 4L by sequencing the different blocks power-up, performing calibrations, and so on. In addition, it is also used for exiting the Ultra Low Power state. Active state:High Synchronous to:N/A
EXC_CLK	CLKMGR_CFG [7:0]	0	null	Lane 0 LP TX Escape Mode Clock Signal Dependency: DS1_HOST_SNPS_PHY = False and DS1_HOST_NUMBER_OF_LANES = 1 Active State: High Registered: Yes Synchronous to: lanebyteclk

Table8-6 presents a list of all the accessible control/test codes for MIPI D-PHY. For all control/test codes without monitoring functionalities defined, MIPIC_PHY_TST_CTRL_1[15:8] is always 0x00.

Table 12-6 Supported Test Codes for Test Mode

Test Code	Test Description
0x00	No test; Normal Operation
0x01	LP Driver Wake Up Timer Counter after Exiting ULPS
0x02	Delay between LP TX Driver Enable and Start Driving LP = 11 during Initialization Timer Control
0x03	Delay between Enable Calibration and Starting Calibration Timer Control
0x04	Relinquish Control if PHY is Configured as TX
0x05	Tta-goTimer Counter

Test Code	Test Description
0x06	Tta-sure Timer Counter
0x07	Turnaround Request Delay Control
0x08	Delay between HS Receiver Power On and Enabling Calibration Timer Control
0x09	Relinquish Control when PHY is Configured as RX
0x0A	Stop State Watchdog Timer Control
0x0B	Reserved 0x0C Stop State Watchdog Timer Enable and Contention Detection 0x0D BIST Mode
0x10	PLL Bias Current Selector/Filter Capacitance Control/VCO Control
0x11	PLL CP Control / PLL Lock Bypass for Initialization and for ULP
0x12	PLL LPF and CP Control
0x13	PLL Digital Testability
0x14	PLL Phase Error Control
0x15	PLL Locking Filter
0x16	PLL Unlocking Filter
0x17	PLL Input Divider Ratio
0x18	PLL Loop Divider Ratio
0x19	PLL Input and Loop Divider Ratios Control
0x20	Bandgap and Bias Control
0x21	Termination Resistor Control
0x22	AFE/BIAS/Bandgap Analog Programmability
0x30	HS TX and Bias Power on Control of Clock Lane
0x31	LP RX Control of Clock Lane
0x32	LP TX Control of Clock Lane
0x33	LP TX Control of Clock Lane
0x34	HS RX Control of Clock Lane
0x35	CLKP/CLKN Swap for Clock Lane + Tclk_miss Control
0x36	Calibration Machine Outputs Observability of Clock Lane
0x40	HS TX and Bias Power on Control of Lane 0
0x41	LP RX Control of Lane 0
0x42	LP TX Control of Lane 0
0x43	LP TX Control of Lane 0
0x44	HS RX Control of Lane 0
0x45	DATAP/DATAN Swap for Lane 0
0x46	HS RX Lane 0 Outputs and Calibration Errors Observability
0x47	BIST Control and Observability on Lane 0
0x50	HS TX and Bias Power on Control of Lane 1
0x51	LP RX Control of Lane 1
0x52	LP TX Control of Lane 1
0x53	LP TX Control of Lane 1
0x54	HS RX Control of Lane 1
0x55	DATAP/DATAN Swap for Lane 1
0x56	HS RX Lane 1 Outputs and Calibration Errors Observability
0x57	BIST Control and Observability on Lane 1
0x60	HS TX Clock Lane Request State Time (T_{LP}) Control
0x61	HS TX Clock Lane Prepare State Time (TCLK-prepare) Control
0x62	HS TX Clock Lane HS-Zero State Time ($T_{CLK-ZERO}$) Control
0x63	HS TX Clock Lane Trail State Time ($T_{CLK-TRAIL_I}$) Control
0x64	HS TX Clock Lane Exit State Time ($T_{HS-EXIT}$) Control

Test Code	Test Description
0x65	HS TX Clock Lane Clock Post Time ($T_{CLK-POST}$) Control
0x70	HS TX Data Lane Request State Time (T_{LP}) Control
0x71	HS TX Data Lanes Prepare State Time ($T_{HS-PREPARE}$) Control
0x72	HS TX Data Lanes HS-Zero State Time ($T_{HS-ZERO}$) Control
0x73	HS TX Data Lanes Trail State Time ($T_{HS-TRAIL}$) Control
0x74	HS TX Data Lanes Exit State Time ($T_{HS-EXIT}$) Control
0x75	HS RX Data Lanes Settle State Time ($T_{HS-settle}$) Control
0x80	HS TX and Bias Power on Control of Lane 2
0x81	LP RX Control of Lane 2
0x82	LP TX Control of Lane 2
0x83	LP TX Control of Lane 2
0x84	HS RX Control of Lane 2
0x85	DATAP/DATAN Swap for Lane 2
0x86	HS RX Lane 2 Outputs and Calibration Errors Observability
0x87	BIST Control and Observability on Lane 2
0x90	HS TX and Bias Power on Control of Lane 3
0x91	LP RX Control of Lane 3
0x92	LP TX Control of Lane 3
0x93	LP TX Control of Lane 3
0x94	HS RX Control of Lane 3
0x95	DATAP/DATAN Swap for Lane 3
0x96	HS RX Lane 3 Outputs and Calibration Errors Observability
0x97	BIST Control and Observability on Lane 3
All others	Reserved for Synopsys usage

12.4.4 Test and Control Codes Detail Description

12.4.4.1 Normal Operation

Test Code: 0x00

This is the normal operation mode of the MIPI D-PHY and also the wake up state of the test interface. In this mode the test interface is inactive.

12.4.4.2 LP Driver Wake Up Timer Counter after Exiting ULPS

Test Code: 0x01

This test code configures the counter threshold that controls the time between exiting Ultra Low Power state and enabling the low-power driver. It is clocked by CRU_CLKGATE5_CON[15].

Test Data:

Table 12-7 LP Driver Wake Up Timer Counter after Exiting ULPS Test Data

w-8'b10111011
Timer counter

Bits 7...0: Timer counter

'XXXXXXXX' - Timer is loaded with value 10'bXXXXXXXXX11

Testdout:

Table 12-8 LP Driver Wake Up Timer Counter after Exiting ULPS Testdout

r-8'b10111011
Timer counter multiplier bits [9:2] loopback

Delay between LP TX Driver Enable and Start Driving LP = 11 during Initialization

12.4.4.3 Timer Control

Test Code: 0x02

This test code configures the counter threshold that controls the time between LP TX driver enable and start driving LP = 2'b11 during the MIPI D-PHY initialization as TX.

Test Data:

Table 12-9 Timer Control Test Data

r- 8'b00001111
Timer counter multiplier bits [9:2] loopback

Bits 7...0: Timer counter

'XXXXXXXX' - Timer is loaded with value 10'bXXXXXXXXX00

Testdout:

Table 12-10 Timer Control Testout

r- 8'b00001111
Timer counter multiplier bits [9:2] loopback

12.4.4.4 Delay between Enable Calibration and Starting Calibration Timer Control

Test Code: 0x03

This test configures the counter threshold that controls the time between calibration enable and effectively starting it. It is clocked by CRU_CLKGATE5_CON[15].

Test Data:

Table 12-11 Delay between Enable Calibration and Starting Calibration Timer Control testData

w-8'b00111100
Timer counter

Bits 7...0: Timer counter

Testdout:

Table 12-12 Delay between Enable Calibration and Starting Calibration Timer Control Testdout

r-8'b00111100
Timer counter multiplier bits loopback

12.4.4.5 Relinquish Control if PHY is Configured as TX

Test Code: 0x04

This test code controls the time during which all lanes are controlled by a single body. The timer counter starts at the top level reset and after reaching the target value, each lane becomes independent. Default value is 20, assuming a minimum period of 50 ns, only for the MIPI D-PHY configuration as TX. It is clocked by CRU_CLKGATE5_CON[15].

Test Data:

Table 12-13 Relinquish Control if PHY is Configured as TX Test Data

w-8'b10011100
Timer counter

Bits 7...0: Timer counter
 'XXXXXXXX' - Timer is loaded with value 10'bXXXXXXXXX00

Testdout:

Table 12-14 Relinquish Control if PHY is Configured as TX Testdout

r-8'b10011100

Timer counter multiplier bits [9:2] loopback
--

12.4.4.6 Tta-go Timer Counter**Test Code: 0x05**

This test code controls the number of cycles that the TX drives the bridge state during a turnaround procedure (Tta-go). Refer to the D-PHY specification for more information.

Test Data:

Table 12-15 Tta-go Timer Counter Test Data

w-2'b00	w-6'b000100
Reserved	Number of cycles

Bits 5...0: Number of cycles

Testdout:

Table 12-16 Tta-go Timer Counter Testdout

r-2'b00	r-6'b000100
2'b00	Number of cycles loopback

12.4.4.7 Tta-sure Timer Counter**Test Code: 0x06**

This test code controls the number of cycles that the RX waits after a bridge state has been detected during a turnaround procedure (Tta-sure). Refer to the D-PHY specification for more information.

Test Data:

Table 12-17 Tta-sure Timer Counter Test Data

w-2'b00	w-6'b000001
Reserved	Number of cycle

Bits 5...0: Number of cycles

Testdout:

Table 12-18 Tta-sure Timer Counter Testdout

r-2'b00	r-6'b000001
2'b00	Number of cycles loopback

12.4.4.8 Turnaround Request Delay Control**Test Code: 0x07**

This test code controls the number of cycles that the MIPI D-PHY waits for until a turnaround request is processed, allowing LP RX to be ready.

Test Data:

Table 12-19 Turnaround Request Delay Control Test Data

w-2'b00	w-6'b110010
Reserved	Number of cycles

Bits 5...0: Number of cycles

Testdout:

Table 12-20 Turnaround Request Delay Control Test Testdout

r-2'b00	r-6'b110010
2'b00	Number of cles loopback

12.4.4.9 Delay between HS Receiver Power On and Enabling Calibration**Timer Control****Test Code: 0x08**

This test code controls the time between powering on the HS receiver and enabling calibration. It is clocked by CRU_CLKGATE5_CON[15].

Test Data:

Table 12-21 Delay between HS Receiver Power On and Enabling Calibration Timer Control Test Data

w-8'b00000110
Number of cycles

Bits 7...0: Number of cycles

Testdout:

Table 12-22 Delay between HS Receiver Power On and Enabling Calibration Timer Control Testdout

r-8'b00000110
Number of cycles loopback

12.4.4.10 Relinquish Control when PHY is Configured as RX**Test Code: 0x09**

This test code controls the time during which all lanes are controlled by a single body. The timer counter starts at the top level reset and after reaching the target value, each lane becomes independent. It is only for the RX configuration and is clocked by CRU_CLKGATE5_CON[15].

Test Data:

Table 12-23 Relinquish Control when PHY is Configured as RX Test Data:

w-8'b00001111
Timer counter

Bits 7...0: Timer counter

XXXXXXXX - Timer is loaded with value 10'bXXXXXXXXX00

Testdout:

Table 12-24 Relinquish Control when PHY is Configured as RX Testdout

r-8'b00001111
Timer counter multiplier bits [9:2] loopback

12.4.4.11 Stop State Watchdog Timer Control**Test Code: 0x0A**

This test code controls the time for which the MIPI D-PHY receives LP=2'b11 without interruption. If this time exceeds timeoutstopstate threshold, a reset is applied to the corresponding lane. It is disabled by default. It is only for the RX configuration and is clocked by CRU_CLKGATE5_CON[15].

Test Data:

Table 12-25 Stop State Watchdog Timer Control Test Data

w-2'b00	w-6'b110010	
Set 0	timeoutstopstate [5:0]	
w-2'b01	w-6'b011101	
Set 1	timeoutstopstate [11:6]	
w-2'b10	w-3'b000	w-3'b001
Set 2	Reserved	timeoutstopstate [14:12]

Bits 7...6: Program selector

- 00 - Set 0 is programmed (also selects bits 5:0 for observability)
15'bXXXXXXXXX10000
- 01 - Set 1 is programmed (also selects bits 11:6 for observability)
15'bXXX011101XXXXXX
- 10 - Set 2 is programmed (also selects bits 14:12 for observability)
15'b001XXXXXXXXXXXX Bits 5...0: Programmable value

Testdout:

Program selector [7:6] - Set 0

Table 12-26 Stop State Watchdog Timer Control Testdout Set 0

r-2'b00	r-6'b110000
2'b00	timeoutstopstate [5:0]

Program selector [7:6] - Set 1

Table 12-27 Stop State Watchdog Timer Control Testdout Set 1

r-2'b00	r-6'b011101
2'b00	timeoutstopstate [11:6]

Program selector [7:6] - Set 2

Table 12-28 Stop State Watchdog Timer Control Testdout Set 2

r-5'b00000	r-3'b001
5'b00000	timeoutstopstate [14:12]

12.4.4.12 Stop State Watchdog Timer Enable and Contention Detection

Test Code: 0x0C

This test code enables or disables the stop state watchdog timer. It is only for the RX configuration. It also provides control for the contention detection mechanism.

Test Data:

Table 12-29 Stop State Watchdog Timer Enable and Contention Detection Test Data

w-1'b0	w-4'b0000	w-1'b0	w-2'b00
Error contention detection	Reserved	Enable/disable watchdog timer	Reserved

- Bit 7: Error contention detection
 - ◇ 0 - Enable error contention detection only during TA (default)
 - ◇ 1 - Enable error contention detection in all LP modes including TA
- Bits 6...3: Reserved
- Bit 2: Enable/disable watchdog timer
 - ◇ 0 - Disable watchdog timer
 - ◇ 1 - Enable watchdog timer
- Bits 1...0: Reserved

Testdout:

Table 12-30 Stop State Watchdog Timer Enable and Contention Detection Testdout

r-1'b0	r-4'b0000	r-1'b0	r-2'b00
Error contention detection	4'b0000	Enable/disable watchdog timer loopback	2'b00

12.4.4.13 BIST Mode

Test Code: 0x0D

This test code can be used to switch the BIST mode on/off.

Test Data:

Table 12-31 BIST Mode Testdout

w-7'b00000000	w-1'b1
Reserved	BIST mode on/off

- Bits 7...1: Reserved
 - Bit 0: BIST mode on/off
 - ◊ 0 - BIST mode off
 - ◊ 1 - BIST mode on

Testdout:

Table 12-32 BIST Mode testdout

r-7'b00000000	r-1'b1
7'b00000000	BIST mode on/off

12.4.4.14 PLL Bias Current Selector/Filter Capacitance Control/VCO Control

Control

Test Code: 0x10

This test code controls the biasing of the PLL and the VCO transfer function.

Test Data:

Table 12-33 PLL Bias Current Selector/Filter Capacitance Control/VCO Control TestData

w-1'b0	w-1'b0	w-3'b000	w-2'b00	w-1'b1
Bypass VCO range	Reserved	VCO range control	VCO internal capacitance control	Reference bias current selector

- Bit 7: Bypass VCO range
 - ◊ 0 - VCO range is programmed with the default values for the corresponding hsfreqrange (HS RX Control of Lane 0)
 - ◊ 1 - VCO range is programmed with bits 5...3
- Bit 6: Reserved
- Bits 5...3: VCO range control
 - ◊ 000 - fvco frequency is between 80 and 200 MHz
 - ◊ 001 - fvco frequency is between 200 and 300 MHz
 - ◊ 010 - fvco frequency is between 300 and 500 MHz
 - ◊ 011 - fvco frequency is between 500 and 700 MHz
 - ◊ 100 - fvco frequency is between 700 and 900 MHz
 - ◊ 101 - fvco frequency is between 900 and 1100 MHz
 - ◊ 110 - fvco frequency is between 1100 and 1300 MHz
 - ◊ 111 - fvco frequency is between 1300 and 1500 MHz
- Bits 2...1: VCO internal capacitance control
 - ◊ 00 - Default capacitance
 - ◊ 01 - Low capacitance (four times lower than the default value)
 - ◊ 10 - High capacitance (double the default value)

- ◆ 11 - Not allowed
- Bit 0: Reference bias current selector
 - ◆ 0 - Internal biasing
 - ◆ 1 - Clean external current source of 20 μ A

Testdout:

Table 12-34 PLL Bias Current Selector/Filter Capacitance Control/VCO Control Testdout

r-1'b0	r-1'b0	r-3'b000	r-2'b00	r-1'b1
Bypass VCOrange loopback	1'b0	VCO range control loopback	VCO internal capacitance control loopback	Reference bias current selector loopback

12.4.4.15 PLL CP Control / PLL Lock Bypass for Initialization and for ULP

Test Code: 0x11

This test code controls the charge pump current and the bypass of the PLL lock for initialization, and ULP exit.

Test Data:

Table 12-35 PLL CP Control / PLL Lock Bypass for Initialization and for ULP TestData

w-4'b0000	w-4'b0010
PLL lock bypass	CP current

- Bits 7...4: PLL lock bypass
 - ◆ xxx0 - Bypass PLL lock during initialization
 - ◆ x11x - Bypass PLL lock after exiting ULP
- Bits 3...0: CP current (μ A)

■	0000	1.5
■	0001	3
■	0010	4.5
■	0011	6
■	0100	2.5
■	0101	5
■	0110	7.5
■	0111	10
■	1000	3
■	1001	6
■	1010	9
■	1011	12
■	1100	4
■	1101	8
■	1110	12
■	1111	16

Testdout:

Table 12-36 PLL CP Control / PLL Lock Bypass for Initialization and for ULP Testdout

w-4'b0000	w-4'b0010
PLL lock bypass loopback	CP current loopback

12.4.4.16 PLL LPF and CP Control

Test Code: 0x12

This test code controls the Charge-Pump (CP) current and the Low Pass Filter (LPF) resistor.

Table 12-37 PLL LPF and CP Control TestData

w-1'b0	w-1'b0
Bypass CP default values	Bypass LPF default values

- Bit 7: Bypass CP default values
 - ✧ 0 - CP is programmed with the default values for the corresponding hsfreqrange (test code 8'h44, HS RX Control of Lane 0)
 - ✧ 1 - CP is programmed with bits 3...0 using test code 8'h11 (PLL CP Control / PLL Lock Bypass for Initialization and for ULP).
- Bit 6: Bypass LPF default values
 - ✧ 0 - LPF is programmed with the default values for the corresponding hsfreqrange (test code 8'h44, HS RX Control of Lane 0)
 - ✧ 1 - LPF is programmed with bits 5...0
- Bits 5...0: LPF resistors ($k\Omega$)

000000	18.5
000001	16
000010	15.5
000100	14.5
001000	13.5
010000	13
100000	12

All others – Reserved

Testdout:

Table 12-38 PLL LPF and CP Control Testdout

r-1'b0	r-1'b0
CP bypass loopback	LPF bypass loopback

12.4.4.17 PLL Digital Testability

Test Code: 0x13

This test code provides access to the internal signals of the PLL.

Test Data:

Table 12-39 PLL Digital Testability TestData

w-1'b0	w-1'b0	w-1'b0	w-1'b0	w-3'b000
Reserved	Power override enable	Reserved	Power on/off	Observability control

- Bit 7: Reserved
- Bit 6: Power override enable
 - ✧ 0 - PLL's power is managed by the internal FSM
 - ✧ 1 - PLL's power is controlled by the test interface
- Bit 5: Reserved
- Bit 4: Power on/off (requires power override enable at 1)
 - ✧ 0 - Analog blocks are turned off
 - ✧ 1 - Analog blocks are turned on
- Bits 3..1: Observability control

- ◊ 000 - Internal lock signal
- ◊ 001 - PFDs reference clock
- ◊ 010 - PFD's feedback clock
- ◊ 011 - PLL's input clock (gated with bypass)
- ◊ 100 - Reserved
- ◊ 101 - Reserved
- ◊ 110 - VCO clock (buffered)
- ◊ 111 - Reserved

- Bit 0: Reserved

Testdout:

Table 12-40 PLL Digital Testability Testdout

w-1'b0	w-1'b0	w-1'b0	w-1'b0	w-3'b000
Test lock	Power override enable loopback	1'b0	Power on/off loopback	Observability control loopback

12.4.4.18 PLL Phase Error Control

Test Code: 0x14

This test code controls the allowed phase error before the PLL lock is issued. This phase error is measured in VCO clock cycles.

Test Data:

Table 12-41 PLL Phase Error Control TestData

w-1'b0	w-2'b00	w-5'b00100
Set 0	Reserved	Phase error [4:0]
w-1'b1	w-2'b00	w-5'b00000
Set 1	Reserved	Phase error [9:5]

- Bit 7: Program selector
 - ◊ 0 - Set 0 is programmed (also selects bits 4:0 for observability)
10'bXXXXX00100
 - ◊ 1 - Set 1 is programmed (also selects bits 9:5 for observability)
10'b00000XXXXX
- Bits 6...5: Reserved
- Bits 4...0: Phase error value

Testdout:

MIPIC_PHY_TST_CTRL_1[7] - Set 0:

Table 12-42 PLL Phase Error Control Testdout

r-3'b000	r-5'b00100
3'b000	Phase error[4:0] loopback

MIPIC_PHY_TST_CTRL_1[7] - Set 1:

Table 12-43 PLL Phase Error Control Testdout

r-3'b000	r-5'b00000
3'b000	Phase error[9:5] loopback

12.4.4.19 PLL Locking Filter

Test Code: 0x15

This test code controls the length of the PLL lock filter. This filter avoids having false lock indications. This filter represents the number of cycles where a phase error smaller than

the defined must be observed before the lock is issued.

Test Data:

Table 12-44 PLL Locking Filter TestData

r-8'b11111111
PLL's lock filter

Testdout:

Table 12-45 PLL Locking Filter Testdout

r-8'b11111111
PLL's lock filter loopback

12.4.4.20 PLL Unlocking Filter

Test Code: 0x16

This test code controls the length of the PLL unlock filter. This filter avoids the temporary disturbances like peak jitter or the supply noise that causes the loss of lock. This filter represents the number of cycles where a phase error higher than the defined (see "PLL Locking Filter") must be observed before the lock is de-asserted.

Test Data:

Table 12-46 PLL Unlocking Filter TestData

r-8'b00000010
PLL's unlock filter

Testdout:

Table 12-47 PLL Unlocking Filter Testdout

r-8'b00000010
PLL's unlock filter loopback

12.4.4.21 PLL Input Divider Ratio

Test Code: 0x17

This test code controls the PLL's input divider. It is the divided reference clock which is fed into the phase frequency detector. The obtained frequency is as follows:

reference clock frequency / N

where:

- N = n + 1
 - ◊ N is the input frequency division ratio
 - ◊ n is the input divider (value programmed on test code)

For the input divider to be effective, bit 4 of the register 0x19 (PLL Input and Loop Divider Ratios Control)

must be 1. For more information, refer to "PLL Requirements".

Test Data:

Table 12-48 PLL Input Divider Ratio TestData

w-1'b0	w-7'b0000001
Reserved	Input divider

Testdout:

Table 12-49 PLL Input Divider Ratio Testdout

r-1'b0	r-7'b0000001
r-1'b0	Input divider loopback

12.4.4.22 PLL Loop Divider Ratio

Test Code: 0x18

This test code controls the PLL's feedback divider. It is the divided VCO clock which is fed into the phase-frequency-detector. The obtained frequency is as follows:

VCO clock frequency / M

where:

- $M = m + 1$
 - ◊ M is the feedback multiplication ratio
 - ◊ m is the feedback divider (value programmed on test code)

For the input divider to be effective, bit 5 of the register 0x19 (PLL Input and Loop Divider Ratios Control)

must be 1 prior to applying register settings. For more information, refer to "PLL Requirements".

Test Data:

Table 12-50 PLL Loop Divider Ratio TestData

w-1'b0	w-2'b00	w-5'b00101
Set 0	Reserved	Feedback divider [4:0]
w-1'b1	w-3'b000	w-4'b0000
Set 1	Reserved	Feedback divider [8:5]

- Bit 7: Program selector
 - ◊ 0 - Set 0 is programmed (also selects this half of the register for observability)
9'bXXXX11101
 - ◊ 1 - Set 1 is programmed (also selects this half of the register for observability)
9'b0000XXXXX
- Bits 6...5: Reserved
- Bits 4...0: Feedback divider

Testdout:

MIPIC_PHY_TST_CTRL_1[7] - Set 0

Table 12-51 PLL Loop Divider Ratio Testdout

r-3'b000	r-5'b00101
3'b000	Feedback divider [4:0] loopback

MIPIC_PHY_TST_CTRL_1[7] - Set 1

Table 12-52 PLL Loop Divider Ratio Testdout

r-4'b0000	r-4'b0101
4'b0000	Feedback divider [8:5] loopback

12.4.4.23 PLL Input and Loop Divider Ratios Control

Test Code: 0x19

This test code controls the PLL input and loop divider ratios.

Test Data:

Table 12-53 PLL Input and Loop Divider Ratios Control TestData

w-2'b00	w-1'b0	w-1'b0	w-4'b0000
Reserved	Bypass PLL loop divider default values	Bypass PLL input divider default values	Reserved

- Bits 7...6: Reserved
- Bit 5: Bypass the PLL loop divider default values
 - ◊ 0 - PLL loop divider is programmed with the default values for the corresponding hsfreqrange
(HS RX Control of Lane 0)

- ◊ 1 - PLL loop divider is programmed using the test code 8'h18 (PLL Loop Divider Ratio)
 - Bit 4: Bypass PLL input divider default values
- ◊ 0 - PLL input divider is programmed with the default values for the corresponding hsfreqrange (test code 8'h44, HS RX Control of Lane 0)
- ◊ 1 - PLL input divider is programmed using test code 8'h17 (PLL Input Divider Ratio)
- Bits 3...0: Reserved

Testdout:

Table 12-54 PLL Input and Loop Divider Ratios Control Testdout

r-2'b00	r-1'b00	r-1'b00	r-4'b0000
2'b00	Bypass PLL loop divider default loopback	Bypass PLL input divider loopback	4'b0000

12.4.4.24 Bandgap and Bias Control**Test Code: 0x20**

This test code controls the bandgap and biasing unit power management.

Test Data:

Table 12-55 Bandgap and Bias Control TestData

w-1'b0	w-1'b0	w-2'b00	w-1'b0	w-1'b0	w-1'b0	w-1'b0
Reserved	Power override enable	Reserved	Biassing scheme selector	Bias block power-on	Reserved	Bandgap power-on

- Bit 7: Reserved
- Bit 6: Power override enable
 - ◊ 0 - Power is managed by the internal FSM
 - ◊ 1 - Power is controlled by the test interface
- Bits 5...4: Reserved
- Bit 3: Biassing scheme selector (requires bandgap)
 - ◊ 0 - Reference current is generated through the external resistor
 - ◊ 1 - Reference current is generated through an internal resistor
- Bit 2: Bias block power-on (requires bandgap)
 - ◊ 0 - Bias block is powered off
 - ◊ 1 - Bias block is powered on
- Bit 1: Reserved
- Bit 0: Bandgap power-on
 - ◊ 0 - Bandgap is powered off
 - ◊ 1 - Bandgap is powered on

Testdout:

Table 12-56 Bandgap and Bias Control Testdout

r-1'b0	r-1'b0	r-2'b00	r-1'b0	r-1'b0	r-1'b0	r-1'b0
BandgapOK	Power override enable loopback	2'b00	Biassing scheme selector loopback	Bias block power-on loopback	1'b0	Bandgap power-on

- Bit 7: Bandgap OK
 - ◊ 0 - Bandgap voltage is not at the target value yet
 - ◊ 1 - Bandgap voltage is stable at the target value

12.4.4.25 Termination Resistor Control

Test Code: 0x21

This test code controls the termination resistor's value.

Test Data:

Table 12-57 Termination Resistor Control TestData

w-3'b000	w-3'b011	w-1'b0	w-1'b0
Reserved	Termination resistor value	Termination resistor power override enable	Termination resistor power-on

- Bits 7...5: Reserved
- Bits 4...2: Termination resistor value (requires termination resistor power-on)
- Bit 1: Termination resistor power override enable
 - ◊ 0 - Power is managed by the internal FSM
 - ◊ 1 - Power is managed by the test interface
- Bit 0: Termination resistor power-on (requires power override enable)
 - ◊ 0 - Termination resistors are turned off
 - ◊ 1 - Termination resistors are turned on

Testdout:

MIPIC_PHY_TST_CTRL_1[7] - Set 0:

Table 12-58 Termination Resistor Control Testdout

r-1'b0	r-1'b0	r-1'b0	r-3'b000	r-1'b0	r-1'b0
Resistor comparator	Resistor calibration error	Resistor calibration done	Termination resistor value loopback	1'b0	Termination resistor power-on loopback

- Bit 7: Resistor comparator
 - ◊ 0 - Termination resistor is lower than the external resistor
 - ◊ 1 - Termination resistor is higher than the external resistor
- Bit 6: Resistor calibration error
 - ◊ 0 - Termination calibration is performed without errors
 - ◊ 1 - Termination calibration is performed with errors
- Bit 5: Resistor calibration done
 - ◊ 0 - Termination calibration is not completed
 - ◊ 1 - Termination calibration is completed
- Bits 4...2: Termination resistor value loopback
- Bit 1: Reserved
- Bit 0: Termination resistor power on loopback
 - ◊ 0 - Termination resistors are turned off
 - ◊ 1 - Termination resistors are turned on

MIPIC_PHY_TST_CTRL_1[7] - Set 1:

Table 12-59 Termination Resistor Control Testdout

r-1'b0	r-1'b0	r-1'b0	r-3'b000	r-1'b0	r-1'b0
Resistor comparator	Analog programmability level shifter power-on	1'b0	Termination resistor value loopback	Termination resistor power override enable loopback	Termination resistor power-on loopback

- Bit 7: Resistor comparator
 - ◊ 0 - Termination resistor lower than external resistor
 - ◊ 1 - Termination resistor higher than external resistor
- Bit 6: Analog programmability level shifter power on
 - ◊ 0 - Level shifters are powered off

- ◆ 1 - Level shifters are powered on
- Bit 5: Reserved
- Bits 4...2: Termination resistor value loopback
- Bit 1: Termination resistor power override enable loopback
 - ◆ 0 - Power is managed by the internal FSM
 - ◆ 1 - Power is managed by the test interface
- Bit 0: Termination resistor power on loopback
 - ◆ 0 - Termination resistors are turned off
 - ◆ 1 - Termination resistors are turned on

12.4.4.26 AFE/BIAS/Bandgap Analog Programmability

Test Code: 0x22

This test code controls the various parameters in the MIPI D-PHY.

Test Data:

Table 12-60 AFE/BIAS/Bandgap Analog Programmability TestData

w-1'b0	w-7'b0000000	
Set 0	Analog programmability[6:0]	
w-1'b1	w-3'b000	w-4'b0000
Set 1	Reserved	
	Analog programmability[10:7]	

- Bit 7: Program selector
 - ◆ 0 – Set 0 is programmed (also selects bits 6:0 for observability)
11'bXXXX0000000
 - ◆ 1 – Set 1 is programmed (also selects bits 10:7 for observability)
11'b0000XXXXXX
- Bits 6...0: Analog programmability
 - ◆ 10 – 1.5 Gbps support. Should be enabled for speeds higher than 1 Gbps and up to 1.5 Gbps.
 - 0 – 1.5 Gbps analog circuitry support disabled
 - 1 – 1.5 Gbps analog circuitry support enabled
 - ◆ 9:7: Adjust bandgap reference voltage (typical corner)
 - 111 – 96.10%
 - 110 – 95.12%
 - 101 – 94.15%
 - 100 – 93.17%
 - 011 – 100.00%
 - 010 – 99.02%
 - 001 – 98.05%
 - 000 – 97.07%
 - ◆ 6: Adjust LP RX bias current
 - 0 – 100%
 - 1 – 50%
 - ◆ 5:3: Adjust LP TX bias current
 - 000 – 76.92%
 - 001 – 83.33%
 - 010 – 90.91%
 - 011 – 100.00%
 - 100 – 111.10%
 - 101 – 125.00%
 - 110 – 142.80%
 - 111 – 166.70%
 - ◆ 2:0: Biasextr: adjust internal resistor
 - 111 : 127.7%
 - 110 : 118.8%
 - 101 : 111.88%

100 : 105.94%
 011 : 100%
 010 : 95.9%
 001 : 91.5%
 000 : 87.1%

Testdout:

MIPIC_PHY_TST_CTRL_1[7] - Set 0:

Table 12-61 AFE/BIAS/Bandgap Analog Programmability Testdout

r-1'b0	r-7'b0000000
1'b0	Analog programmability[6:0] loopback

MIPIC_PHY_TST_CTRL_1[7] - Set 1:

Table 12-62 AFE/BIAS/Bandgap Analog Programmability Testdout

r-4'b0000	r-4'b0000
4'b0000	Analog programmability[10:7] loopback

12.4.4.27 HS TX and Bias Power on Control of Clock Lane**Test Code: 0x30**

Table 12-63 HS TX and Bias Power on Control of Clock Lane TestData

w-1'b0	w-1'b0	w-1'b0	w-1'b0	w-1'b0	w-1'b0	w-1'b0
Bypass HS TX data-in	HS TXdata-in	Bypass HS TX enable	HS TXenable	Bypass HS TXpower-on	HS TXpower-on	Bypass Bias power-on

- Bit 7: Bypass high-speed driver data
 - ◊ 0 - Internal high-speed driver data is controlled by the internal FSM
 - ◊ 1 - Internal high-speed driver data is controlled by the test interface
- Bit 6: High-speed driver data
 - ◊ 0 - Internal high-speed driver transmits a low level voltage signal 0
 - ◊ 1 - Internal high-speed driver transmits a high level voltage signal 1
- Bit 5: Bypass high-speed driver enable
 - ◊ 0 - Internal high-speed driver enable is controlled by the internal FSM
 - ◊ 1 - Internal high-speed driver enable is controlled by the test interface
- Bit 4: High-speed driver enable
 - ◊ 0 - Internal high-speed driver is disabled
 - ◊ 1 - Internal high-speed driver is enabled
- Bit 3: Bypass high-speed driver power-on
 - ◊ 0 - Internal high-speed driver power-on is controlled by the internal FSM
 - ◊ 1 - Internal high-speed driver power-on is controlled by the test interface
- Bit 2: High-speed Driver power-on
 - ◊ 0 - Internal high-speed driver is powered off
 - ◊ 1 - Internal high-speed driver is powered on
- Bit 1: Bypass clock lane bias block power-on
 - ◊ 0 - Internal biasing block is controlled by the internal FSM
 - ◊ 1 - Internal biasing block is controlled by the test interface
- Bit 0: Clock lane bias block power-on
 - ◊ 0 - Internal biasing block is powered off
 - ◊ 1 - Internal biasing block is powered on

Testdout:

Table 12-64 HS TX and Bias Power on Control of Clock Lane Testdout

r-1'b0	r-1'b0	r-1'b0	r-1'b0	r-1'b0	r-1'b0	r-1'b0
Bypass HS TX data-in	HS TX data-in	Bypass HS TX	HS TX enable	Bypass HS TX	HS TX power-on loopback	Bypass Bias power-on

loopback	loopback	enable loopback	loopback	power-on loopback		loopback
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12.4.4.28 LP RX Control of Clock Lane

Test Code: 0x31

This test code controls the low-power single-ended receivers of the clock lane by overriding the control signals sent by the FSM.

Table 12-65 LP RX Control of Clock Lane TestData

w-1'b0	w-1'b0	w-1'b0	w-1'b0	w-1'b0	w-1'b0	w-1'b0
Set 1	Reserved	Bypass LP CD power-on	LP CDpower-on	Bypass ULPpower-on	ULPpower-on	Bypass LPpower-on

- Bit 7: Program selector
 - ◊ 0 - Does not program anything
 - ◊ 1 - Programs Set 1 registers
- Bit 6: Reserved
 - ◊ 0 - Signals controlled by the internal FSM
 - ◊ 1 - LP RX controlled by the test interface
- Bit 5: Bypass LP CD power-on
 - ◊ 0 - LP CD power-on is controlled by the internal FSM
 - ◊ 1 - LP CD power-on is controlled by the test interface
- Bit 4: LP CD power-on
 - ◊ 0 - LP CD is powered off
 - ◊ 1 - LP CD is powered on
- Bit 3: Bypass ULP RX power-on
 - ◊ 0 - ULP RX power-on is controlled by the internal FSM
 - ◊ 1 - ULP RX power-on is controlled by the test interface
- Bit 2: ULP RX power-on
 - ◊ 0 - ULP RX is powered off
 - ◊ 1 - ULP RX is powered on
- Bit 1: Bypass LP RX power-on
 - ◊ 0 - LP RX power-on is controlled by the internal FSM
 - ◊ 1 - LP RX power-on is controlled by the test interface
- Bit 0: LP RX power-on
 - ◊ 0 - LP RX is powered off
 - ◊ 1 - LP RX is powered on

Testdout:

Table 12-66 LP RX Control of Clock Lane Testdout

r-2'b00	r-1'b0	r-1'b0	r-1'b0	r-1'b0	r-1'b0	r-1'b0
2'b00	Bypass LP CD power-on loopback	LP CD power-on loopback	Bypass ULP power-on loopback	ULP power-on loopback	Bypass LP power-on loopback	Bypass Bias power-on loopback
2'b00	LP CD data-out		ULP RX data-out		LP RX data-out	

- First row of Table if MIPIC_PHY_TST_CTRL_1[7] = 1'b1
Set 1 loopback
- Second row of Table if MIPIC_PHY_TST_CTRL_1[7] = 1'b0
 - ◊ Bits 7...6: Reserved
 - ◊ Bits 5...4: LP CD data-out
 - Data from the two single-ended low-power contention detectors
 - ◊ Bits 3....2: ULP RX data-out
 - Data from the two single-ended low-power receivers used to detect that the TX

- has left the Ultra Low Power state
- ❖ Bits 1...0: LP RX data-out
Data from the two single-ended low-power receivers when in low-power mode

12.4.4.29 LP TX Control of Clock Lane

Test Code: 0x32

This test code controls the low-power single-ended drivers of the clock lane by overriding the control signals sent by the FSM.

Test Data:

Table 12-67 LP TX Control of Clock Lane TestData

w-1'b0	w-1'b0	w-1'b0	w-1'b0	w-1'b0	w-1'b0	w-1'b0	w-1'b0
Bypass LP TXenable idle low-power	LP TX enable idle low-power	Bypass LP TX enable pull-down	LP TX enable pull-down	Bypass LP TXenable	LP TXenable	Bypass LP TX power-on	LP TXpower-on

- Bit 7: Bypass LP TX enable idle low-power
 - ❖ 0 - LP TX enable idle low-power is controlled by the internal FSM
 - ❖ 1 - LP TX enable idle low-power is controlled by the test interface
- Bit 6: LP TX enable ULP
 - ❖ 0 - Disable low-power for idle mode
 - ❖ 1 - Enable low-power for idle mode
- Bit 5: Bypass LP TX enable pull-down
 - ❖ 0 - LP TX enable pull-down is controlled by the internal FSM
 - ❖ 1 - LP TX enable pull-down is controlled by the test interface
- Bit 4: LP TX enable pull-down
 - ❖ 0 - Pull-down functionality is turned off
 - ❖ 1 - A LP-00 state is forced at the output of the low-power drivers
- Bit 3: Bypass LP TX enable
 - ❖ 0 - LP TX enable is controlled by the internal FSM
 - ❖ 1 - LP TX enable is controlled by the test interface
- Bit 2: LP TX enable
 - ❖ 0 - Driver does not transmit incoming data
 - ❖ 1 - Driver transmits incoming data
- Bit 1: Bypass LP TX power-on
 - ❖ 0 - LP TX is powered off
 - ❖ 1 - LP TX is powered on
- Bit 0: LP TX power-on
 - ❖ 0 - LP TX is powered off
 - ❖ 1 - LP TX is powered on

Testdout:

Table 12-68 LP TX Control of Clock Lane Testdout

r-1'b0	r-1'b0	r-1'b0	r-1'b0	r-1'b0	r-1'b0	r-1'b0	r-1'b0
Bypass LP TX enable pull-up loopback	LP TX enable pull-up loopback	Bypass LP TX enable pull-down loopback	LP TX enable pull-down loopback	Bypass LP TX enable loopback	LP TX enable loopback	Bypass LP TX power-on loopback	LP TX power-on loopback

12.4.4.30 LP TX Control of Clock Lane

Test Code: 0x33

This test code controls the low-power single-ended drivers of the clock lane by overriding

the control signals sent by the FSM.

Test Data:

Table 12-69 LP TX Control of Clock Lane TestData

w-5'b00000	w-1'b0	w-2'b00
Reserved	Bypass LP TX driver data-in	LP TX driver data-in

- Bits 7...3: Reserved
- Bit 2: Bypass LP TX driver data-in
 - ◆ 0 - Inputs of LP TX driver are controlled by the internal FSM
 - ◆ 1 - Inputs of LP TX driver are controlled by the test interface
- Bit 1...0: LP TX driver data-in

Inputs of LP TX driver

Testdout:

Table 12-70 LP TX Control of Clock Lane Testdout

r-5'b00000	r-1'b0	r-2'b00
5'b00000	Bypass LP TX driver data-in loopback	LP TX driver data-in loopback

12.4.4.31 HS RX Control of Clock Lane

Test Code: 0x34

This test code controls the high-speed differential receiver of the clock lane by overriding the control signals sent by the FSM.

Test Data:

Table 12-71 HS RX Control of Clock Lane TestData

w-2'b00	w-1'b0	w-1'b0	w-1'b0	w-1'b0	w-1'b0	w-1'b0
Set 0	Bypass HS RX termination enable	HS RX termination enable	Bypass HS RX offset calibration enable	HS RX offset calibration enable	Bypass HS RXpower-on	HS RXpower-on
Set 1	Bypass HS RX offset compensation setting					
Set 2	Reserved				Bypass HS RXsettle filter	

- Bits 7...6: Program selector
 - ◆ 10 - Set 0 is programmed
 - ◆ 11 - Set 1 is programmed
 - ◆ 0x - Set 2 is programmed

Set 0:

- Bit 5: Bypass HS RX termination enable
 - ◆ 1 - HS RX termination enable is controlled by the test interface
 - ◆ 0 - HS RX termination enable is controlled by the internal FSM
- Bit 4 HS RX termination enable
 - ◆ 0 - Termination is not enabled
 - ◆ 1 - Termination is enabled
- Bit 3: Bypass HS RX calibration enable
 - ◆ 0 - HS RX calibration enable is controlled by the internal FSM
 - ◆ 1 - HS RX calibration enable is controlled by the test interface
- Bit 2: HS RX calibration enable
 - ◆ 0 - HS RX calibration is not enabled

- ◆ 1 - HS RX calibration is enabled
- Bit 1: Bypass HS RX power-on
 - ◆ 0 - HS RX power-on is controlled by the internal FSM
 - ◆ 1 - HS RX power-on is controlled by the test interface
- Bit 0: HS RX power-on
 - ◆ 0 - HS RX is powered off
 - ◆ 1 - HS RX is powered on

Set 1:

- Bit 5: Bypass HS RX offset compensation setting
- Bits 4...0: HS RX offset compensation setting

Set 2:

- Bits 5...1: Reserved
- Bit 0: Bypass HS settle filter

Testdout:

Table 12-72 HS RX Control of Clock Lane Testdout

r-2'b00	r-1'b0	r-1'b0	r-1'b0	r-1'b0	r-1'b0	r-1'b0
2'b00	Bypass HS RX termination enable loopback	HS RX termination enable loopback	Bypass HS RX offset calibration enable loopback	HS RX offset calibration enable loopback	Bypass HS RX power-on loopback	HS RX power-on loopback
2'b00	Bypass HS RX offset compensation setting loopback	HS RX offset compensation setting loopback				
7'b00000000						Bypass HS RX settle filter loopback

- First row of Table if MIPIC_PHY_TST_CTRL_1[7:6] = 2'b10
- Second row of Table if MIPIC_PHY_TST_CTRL_1[7:6] = 2'b11
- Third row of Table if MIPIC_PHY_TST_CTRL_1[7:6] = 2'b0x, where x = 0 or 1

12.4.4.32 CLKP/CLKN Swap for Clock Lane + Tclk_miss Control

Test Code: 0x35

This test code ensures the correct clock lane operation when a CLKP/CLKN swap is required.

Test Data:

Table 12-73 CLKP/CLKN Swap for Clock Lane + Tclk_miss Control TestData

w-6'b000000	w-1'b0	w-1'b0
Reserved	Clock Miss force	Polarity change

- Bits 7...2: Reserved
- Bit 1: Clock miss force
 - ◆ 0 - Tclk_miss evaluation mechanism is enabled
 - ◆ 1 - Tclk_miss evaluation mechanism is disabled

Testdout:

Table 12-74 CLKP/CLKN Swap for Clock Lane + Tclk_miss Control Testdout

r-6'b000000	r-1'b0	r-1'b0
6'b000000	Clock miss force loopback	Polarity change loopback

12.4.4.33 Calibration Machine Outputs Observability of Clock Lane

Test Code: 0x36

This test code allows the observability of some outputs of the calibration machine and HS RX of clock lane.

Testdout:

Table 12-75 Calibration Machine Outputs Observability of Clock Lane Testdout

r-1'b0	r-1'b0	r-1'b0	r-1'b0	r-4'b0000
3'b000		HS RX offset compensation setting		
HS RX asynchronous output		HS RX synchronous output		HS RX calibration errors

- First row of Table if MIPIC_PHY_TST_CTRL_1[7] = 1'b0
- Second row of Table if MIPIC_PHY_TST_CTRL_1[7] = 1'b1
 - ◆ Bits 7...6: HS RX asynchronous output
Asynchronous output of HS RX received in the differential pair
 - ◆ Bits 5...4: HS RX synchronous output
Synchronous output of HS RX (clock from the clock lane used to sample)
 - ◆ Bits 3...0: HS RX calibration error flags

12.4.4.34 HS TX and Bias Power on Control of Lane 0

Test Code: 0x40
Test Data:

Table 12-76 H S TX and Bias Power on Control of Lane 0 TestData

w-1'b0	w-1'b0	w-1'b0	w-1'b0	w-1'b0	w-1'b0	w-1'b0
Bypass HS TX data-in	HS TXdata-in	Bypass HS TX enable	HS TXenable	Bypass HS TXpower-on	HS TXpower-on	Bypass Bias power-on

- Bit 7: Bypass high-speed Driver Data
 - ◆ 0 - Internal high-speed driver data is controlled by the internal FSM
 - ◆ 1 - Internal high-speed driver data is controlled by the test interface
- Bit 6: High-speed Driver Data
 - ◆ 0 - Internal high-speed driver transmits a low level voltage signal 0
 - ◆ 1 - Internal high-speed driver transmits a high level voltage signal 1
- Bit 5: Bypass high-speed Driver enable
 - ◆ 0 - Internal high-speed driver enable is controlled by the internal FSM
 - ◆ 1 - Internal high-speed driver enable is controlled by the test interface
- Bit 4: High-speed Driver enable
 - ◆ 0 - Internal high-speed driver is disabled
 - ◆ 1 - Internal high-speed driver is enabled
- Bit 3: Bypass high-speed Driver power-on
 - ◆ 0 - Internal high-speed driver power-on is controlled by the internal FSM
 - ◆ 1 - Internal high-speed driver power-on is controlled by the test interface
- Bit 2: High-speed Driver power-on
 - ◆ 0 - Internal high-speed driver is powered off
 - ◆ 1 - Internal high-speed driver is powered on
- Bit 1: Bypass clock lane bias block power-on
 - ◆ 0 - Internal biasing block is controlled by the internal FSM
 - ◆ 1 - Internal biasing block is controlled by the test interface
- Bit 0: Clock lane bias block power-on
 - ◆ 0 - Internal biasing block is powered off
 - ◆ 1 - Internal biasing block is powered on

Testdout:

Table 12-77 H S TX and Bias Power on Control of Lane 0 Testdout

r-1'b0	r-1'b0	r-1'b0	r-1'b0	r-1'b0	r-1'b0	r-1'b0
Bypass HS TX data-in loopback	HS TX data-in loopback	Bypass HS TX enable loopback	HS TX enable loopback	Bypass HS TX Power-on loopback	HS TX power-on loopback	Bypass Bias power-on loopback

12.4.4.35 LP RX Control of Lane 0

Test Code: 0x41

This test code controls the low-power single-ended receivers of lane 0 by overriding the control signals sent by the FSM.

Test Data:

Table 12-78 L P RX Control of Lane 0 TestData

w-1'b0	w-1'b0	w-1'b0	w-1'b0	w-1'b0	w-1'b0	w-1'b0	w-1'b0
Set 1	Reserved	Bypass LP CD power-on	LP CDpower-on	Bypass ULPpower-on	ULPpower-on	Bypass LPpower-on	LP power-on

- Bit 7: Program selector
 - ◊ 0 - Does not program anything
 - ◊ 1 - Programs Set 1 registers
- Bit 6: Reserved
- Bit 5: Bypass LP CD power-on
 - ◊ 0 - LP CD power-on is controlled by the internal FSM
 - ◊ 1 - LP CD power-on is controlled by the test interface
- Bit 4: LP CD power-on
 - ◊ 0 - LP CD is powered off
 - ◊ 1 - LP CD is powered on
- Bit 3: Bypass ULP RX power-on
 - ◊ 0 - ULP RX power-on is controlled by the internal FSM
 - ◊ 1 - ULP RX power-on is controlled by the test interface
- Bit 2: ULP RX power-on
 - ◊ 0 - ULP RX is powered off
 - ◊ 1 - ULP RX is powered on
- Bit 1: Bypass LP RX power-on
 - ◊ 0 - LP RX power-on is controlled by the internal FSM
 - ◊ 1 - LP RX power-on is controlled by the test interface
- Bit 0: LP RX power-on
 - ◊ 0 - LP RX is powered off
 - ◊ 1 - LP RX is powered on

Testdout:

Table 12-79 L P RX Control of Lane 0 Testdout

r-2'b00	r-1'b0	r-1'b0	r-1'b0	r-1'b0	r-1'b0	r-1'b0	r-1'b02'b00
Bypass LP CD power-on loopback	LP CD power-on loopback	Bypass ULP power-on loopback	ULP power-on loopback	Bypass LP power-on loopback	LP power-on loopback		
2'b00	LP CD data-out		ULP RX data-out		LP RX data-out		

- First row of Table if MIPIC_PHY_TST_CTRL_1[7] = 1'b1
Set 1: loopback
- Second row of Table if MIPIC_PHY_TST_CTRL_1[7] = 1'b0
 - ◊ Bits 7...6: Reserved
 - ◊ Bits 5...4: LP CD data-out
 - Data from the two single-ended low-power contention detectors
 - ◊ Bits 3....2: ULP RX data-out
 - Data from the two single-ended low-power receivers used to detect that the TX has left Ultra Low Power state
 - ◊ Bits 1...0: LP RX data-out
 - Data from the two single-ended low-power receivers when in low-power mode

12.4.4.36 LP TX Control of Lane 0

Test Code: 0x42

This test code controls the low-power single-ended drivers of the clock lane by overriding the control signals sent by the FSM.

Test Data:

Table 12-80 LP TX Control of Lane 0 TestData

w-1'b0	w-1'b0	w-1'b0	w-1'b0	w-1'b0	w-1'b0	w-1'b0	w-1'b0
Bypass LP TXenable idle low-power	LP TX enable idle low-power	Bypass LP TX enable pull-down	LP TX enable pull-down	Bypass LP TXenable	LP TXenable	Bypass LP TX power-on	LP TXpower-on

- Bit 7: Bypass LP TX enable idle low-power
 - ❖ 0 - LP TX enable idle low-power is controlled by the internal FSM
 - ❖ 1 - LP TX enable idle low-power is controlled by the test interface
- Bit 6: LP TX enable ULP
 - ❖ 0 - Disable low-power for idle mode
 - ❖ 1 - Enable low-power for idle mode
- Bit 5: Bypass LP TX enable pull-down
 - ❖ 0 - LP TX enable pull-down is controlled by the internal FSM
 - ❖ 1 - LP TX enable pull-down is controlled by the test interface
- Bit 4: LP TX enable pull-down
 - ❖ 0 - Pull down functionality is turned off
 - ❖ 1 - A LP-00 state is forced at the output of the low-power drivers
- Bit 3: Bypass LP TX enable
 - ❖ 0 - LP TX enable is controlled by the internal FSM
 - ❖ 1 - LP TX enable is controlled by the test interface
- Bit 2: LP TX enable
 - ❖ 0 - Driver does not transmit incoming data
 - ❖ 1 - Driver transmits incoming data
- Bit 1: Bypass LP TX power-on
 - ❖ 0 - LP TX is powered off
 - ❖ 1 - LP TX is powered on
- Bit 0: LP TX power-on
 - ❖ 0 - LP TX is powered off
 - ❖ 1 - LP TX is powered on

Table 12-81 LP TX Control of Lane 0 Testdout

r-1'b0	r-1'b0	r-1'b0	r-1'b0	r-1'b0	r-1'b0	r-1'b0	r-1'b0
Bypass LP TX enable pull-up loopback	LP TX enable pull-up loopback	Bypass LP TX enable pull-down loopback	LP TX enable pull-down loopback	Bypass LP TX enable loopback	LP TX enable loopback	Bypass LP TX power-on loopback	LP TX power-on loopback

12.4.4.37 LP TX Control of Lane 0

Test Code: 0x43

This test code controls the low-power single-ended drivers of the clock lane by overriding the control signals sent by the FSM.

Test Data:

Table 12-82 LP TX Control of Lane 0 TestData

w-5'b00000	w-1'b0	w-2'b00
Reserved	Bypass LP TX driver data-in	LP TX driver data-in

- Bits 7...3: Reserved
- Bit 2: Bypass LP TX driver data-in

- ◆ 0 - Inputs of the LP TX driver are controlled by the internal FSM
- ◆ 1 - Inputs of the LP TX driver are controlled by the test interface
- Bits 0...1: LP TX driver data-in
Inputs of LP TX driver

Testdout:

Table 12-83 LP TX Control of Lane 0 Testdout

r-5'b00000	r-1'b0	r-2'b00
5'b00000	Bypass LP TX driver data-in loopback	LP TX driver data-in loopback

12.4.4.38 HS RX Control of Lane 0**Test Code: 0x44**

This test code controls the high-speed differential receiver of the data lane 0 by overriding the control signals sent by the FSM.

Table 12-84 HS RX Control of Lane 0 TestData

w-1'b0	w-1'b0	w-1'b0	w-1'b0	w-1'b0	w-1'b0	w-1'b0w-1'b0	w-1'b0
Set 0		Bypass HS RX termination enable	HS RX termination enable	Bypass HS RX offset calibration enable	HS RX offset calibration enable	Bypass HS RX power-on	HS RX power-on
Set 1		Bypass HS RX offset compensation setting		HS RX offset compensation setting			
Set 2	HS operating frequency range selection(hsfreqrange)					Bypass HS -RX settle filter loopback	

- Bits 7...6: Program selector
 - ◆ 10 - Set 0 is programmed
 - ◆ 11 - Set 1 is programmed
 - ◆ 0x - Set 2 is programmed

Set 0:

- Bit 5: Bypass HS RX termination enable
 - ◆ 0 - HS RX termination enable is controlled by the internal FSM
 - ◆ 1 - HS RX termination enable is controlled by the test interface
- Bit 4: HS RX termination enable.
 - ◆ 0 - Termination not enabled
 - ◆ 1 - Termination is enabled
- Bit 3: Bypass HS RX calibration enable
 - ◆ 0 - HS RX calibration enable is controlled by the internal FSM
 - ◆ 1 - HS RX calibration enable is controlled by the test interface
- Bit 2: HS RX calibration enable
 - ◆ 0 - HS RX calibration is not enabled
 - ◆ 1 - HS RX calibration is enabled
- Bit 1: Bypass HS RX power-on
 - ◆ 0 - HS RX power-on is controlled by the internal FSM
 - ◆ 1 - HS RX power-on is controlled by the test interface
- Bit 0: HS RX power-on
 - ◆ 0 - HS RX is powered off
 - ◆ 1 - HS RX is powered on

Set 1:

- Bit 5: Bypass HS RX offset compensation setting
- Bits 4...0: HS RX offset compensation setting

Set 2:

- Bits 6...1: HS frequency range selection
- Bit 0: Bypass HS settle filter

Testdout:

Table 12-85 HS RX Control of Lane 0 Testdout

r-1'b0	r-1'b0	r-1'b0	r-1'b0	r-1'b0	r-1'b0	r-1'b0	r-1'b0
2'b00	Bypass HS RX termination enable loopback	HS RX termination enable loopback	Bypass HS RX offset calibration enable loopback	HS RX offset calibration enable loopback	Bypass HS RX power-on loopback	HS RX power-on loopback	
2'b00	Bypass HS RX offset compensation setting loopback	HS RX offset compensation setting loopback					
1'b0	HS operating frequency range selection loopback (hsfreqrange)						Bypass HS -RX settle filter loopback

- First row of Table , if MIPIC_PHY_TST_CTRL_1 [7:6] = 2'b10
- Second row of Table , if MIPIC_PHY_TST_CTRL_1 [7:6] = 2'b11
- Third row of Table , if MIPIC_PHY_TST_CTRL_1 [7:6] = 2'b0x, where x = 0 or 1

12.4.4.39 DATAP/DATAN Swap for Lane 0

Test Code: 0x45

This test code sets the correct behavior of data lane 0 when a DATAP/DATAN swap is required.

Test Data:

Table 12-86 DATAP/DATAN Swap for Lane 0 TestData

w-7'b0000000	w-1'b0
7'b0000000	Polarity change

- Bits 7...1: Reserved
- Bit 0: Polarity change
 - ◊ 0 - Two MIPI D-PHYs with DATAP/DATAN ports connected to DATAP/DATAN respectively
 - ◊ 1 - Two MIPI D-PHYs with DATAP/DATAN ports connected to DATAN/DATAP respectively

Testdout:

Table 12-87 DATAP/DATAN Swap for Lane 0 Testdout

r-7'b0000000	r-1'b0
7'b0000000	Polarity change loopback

12.4.4.40 HS RX Lane 0 Outputs and Calibration Errors Observability

Test Code: 0x46

This test code allows the observability of some outputs of the calibration machine and HS RX of lane 0.

Testdout:

Table 12-88 HS RX Lane 0 Outputs and Calibration Errors Observability Testdout

r-1'b0	r-1'b0	r-1'b0	r-1'b0	r-4'b0000
3'b000		HS RX offset compensation setting		
HS RX asynchronous output		HS RX synchronous output		HS RX calibration errors

- First row of Table 9-88, if MIPIC_PHY_TST_CTRL_1 [7] = 1'b0
- Second row of Table 9-88, if MIPIC_PHY_TST_CTRL_1 [7] = 1'b1
 - ◊ Bits 7...6: HS RX asynchronous output
Asynchronous output of HS RX received in the differential pair
 - ◊ Bits 5...4: HS RX synchronous output
Synchronous output of HS RX (clock from the clock lane used to sample)
 - ◊ Bits 3...0: HS RX calibration error flags

12.4.4.41 BIST Control and Observability on Lane 0

Test Code: 0x47

This test code allows the control and observability of the BIST internal machine mechanism for lane 0.

Test Data:

Table 12-89 B IST Control and Observability on Lane 0 TestData

w-6'b000000	w-1'b0	w-1'b1
Reserved	BIST no lock	BIST enable/disable

- Bits 7...2: Reserved
- Bits 1: BIST no lock
 - ◊ 0 - BIST stops when it reaches the last value
 - ◊ 1 - BIST in loop
- Bits 0: BIST lane enable/disable
 - ◊ 0 - Disable BIST lane 0
 - ◊ 1 - Enable BIST lane 0

Testdout:

Table 12-90 BIST Control and Observability on Lane 0 Testdout

r-3'b000	r-1'b0	r-1'b0	r-1'b0	r-1'b0	r-1'b1
3'b000	BIST error	BIST ok	BIST ongoing	BIST no lock	BIST enable/disable

r-3'b000 r-1'b0 r-1'b0 r-1'b0 r-1'b0 r-1'b1
 3'b000 BIST error BIST ok BIST ongoing BIST no lock BIST enable/disable

12.4.4.42 HS TX and Bias Power on Control of Lane 1

Test Code: 0x50

Test Data:

Table 12-91 HS TX and Bias Power on Control of Lane 1 TestData

w-1'b0	w-1'b0	w-1'b0	w-1'b0	w-1'b0	w-1'b0	w-1'b0	w-1'b0
Bypass HS TX data-in	HS TXdata-in	Bypass HS TX enable	HS TXenable	Bypass HS TX Power-on	HS TXpower-on	Bypass Bias power-on	Bias power-on

- Bit 7: Bypass high-speed driver data
 - ◊ 0 - Internal high-speed driver data is controlled by the internal FSM
 - ◊ 1 - Internal high-speed driver data is controlled by the test interface
- Bit 6: High-speed driver data
 - ◊ 0 - Internal high-speed driver transmits a low level voltage signal 0
 - ◊ 1 - Internal high-speed driver transmits a high level voltage signal 1
- Bit 5: Bypass high-speed driver enable
 - ◊ 0 - Internal high-speed driver enable is controlled by the internal FSM
 - ◊ 1 - Internal high-speed driver enable is controlled by the test interface
- Bit 4: High-speed driver enable
 - ◊ 0 - Internal high-speed driver is disabled
 - ◊ 1 - Internal high-speed driver is enabled

- Bit 3: Bypass high-speed driver power-on
 - ◆ 0 - Internal high-speed driver power-on is controlled by the internal FSM
 - ◆ 1 - Internal high-speed driver power-on is controlled by the test interface
- Bit 2: High-speed driver power-on
 - ◆ 0 - Internal high-speed driver is powered off
 - ◆ 1 - Internal high-speed driver is powered on
- Bit 1: Bypass clock lane bias block power-on
 - ◆ 0 - Internal biasing block is controlled by the internal FSM
 - ◆ 1 - Internal biasing block is controlled by the test interface
- Bit 0: Clock lane bias block power-on
 - ◆ 0 - Internal biasing block is powered off
 - ◆ 1 - Internal biasing block is powered on

Testdout:

Table 12-92 HS TX and Bias Power on Control of Lane 1 Testdout

r-1'b0	r-1'b0	r-1'b0	r-1'b0	r-1'b0	r-1'b0	r-1'b0	r-1'b0
Bypass HS TX data-in loopback	HS TX data-in loopback	Bypass HS TX enable loopback	HS TX enable loopback	Bypass HS TX Power-on loopback	HS TX power-on loopback	Bypass Bias power-on loopback	Bias power-on loopback

12.4.4.43 LP RX Control of Lane 1**Test Code: 0x51**

This test code controls the low-power single-ended receivers of lane 1 by overriding the control signals sent by the FSM.

Test Data:

Table 12-93 L P RX Control of Lane 1 TestData

w-1'b0	w-1'b0	w-1'b0	w-1'b0	w-1'b0	w-1'b0	w-1'b0	w-1'b0
Set 1	Reserved	Bypass LP CD power-on	LP CDpower-on	Bypass ULPpower-on	ULPpower-on	Bypass LPpower-on	LP power-on

- Bit 7: Program selector
 - ◆ 0 - Does not program anything
 - ◆ 1 - Programs the Set 1 registers
- Bit 6: Reserved
- Bit 5: Bypass LP CD power-on
 - ◆ 0 - LP CD power-on is controlled by the internal FSM
 - ◆ 1 - LP CD power-on is controlled by the test interface
- Bit 4: LP CD power-on
 - ◆ 0 - LP CD is powered off
 - ◆ 1 - LP CD is powered on
- Bit 3: Bypass ULP RX power-on
 - ◆ 0 - ULP RX power-on is controlled by the internal FSM
 - ◆ 1 - ULP RX power-on is controlled by the test interface
- Bit 2: ULP RX power-on
 - ◆ 0 - ULP RX is powered off
 - ◆ 1 - ULP RX is powered on
- Bit 1: Bypass LP RX power-on
 - ◆ 0 - LP RX power-on is controlled by the internal FSM
 - ◆ 1 - LP RX power-on is controlled by the test interface
- Bit 0: LP RX power-on
 - ◆ 0 - LP RX is powered off
 - ◆ 1 - LP RX is powered on

Testdout:

Table 12-94 L P RX Control of Lane 1 Testdout

r-2'b00	r-1'b0	r-1'b0	r-1'b0	r-1'b0	r-1'b0	r-1'b0	r-1'b0
2'b00	Bypass LP CD power-on loopback	LP CD power-on loopback	Bypass ULP power-on loopback	ULP power-on loopback	Bypass LP power-on loopback	LP power-on loopback	
2'b00	LP CD data-out		ULP RX data-out		LP RX data-out		

- First row of Table if MIPIC_PHY_TST_CTRL_1[7] = 1'b1
Set 1 loopback
- Second row of Table if MIPIC_PHY_TST_CTRL_1[7] = 1'b0
 - ◊ Bits 7...6: Reserved
 - ◊ Bits 5...4: LP CD data-out
Data from the two single-ended low-power contention detectors
 - ◊ Bits 3....2: ULP RX data-out
Data from the two single-ended low-power receivers used to detect that TX has left Ultra Low Power state
 - ◊ Bits 1...0: LP RX data-out
Data from the two single-ended low-power receivers when in low-power mode

12.4.4.44 LP TX Control of Lane 1

Test Code: 0x52

This test code allows the control over the low-power single-ended drivers of the clock lane by overriding the control signals sent by the FSM.

Test Data:

Table 12-95 H P TX Control of Lane 1 TestData

w-1'b0	w-1'b0	w-1'b0	w-1'b0	w-1'b0	w-1'b0	w-1'b0	w-1'b0
Bypass LP TX enable idlelow-power	LP TX enable idle low-power	Bypass LP TX enable pull-down	LP TX enable pull-down	Bypass LP TXenable	LP TXenable	Bypass LP TX power-on	LP TXpower-on

- Bit 7: Bypass LP TX enable idle low-power
 - ◊ 0 - LP TX enable idle low-power is controlled by the internal FSM
 - ◊ 1 - LP TX enable idle low-power is controlled by the test interface
- Bit 6: LP TX enable ulp
 - ◊ 0 - Disable low-power for idle mode
 - ◊ 1 - Enable low-power for idle mode
- Bit 5: Bypass LP TX enable pull-down
 - ◊ 0 - LP TX enable pull-down is controlled by the internal FSM
 - ◊ 1 - LP TX enable pull-down is controlled by the test interface
- Bit 4: LP TX enable pull-down
 - ◊ 0 - Pull down functionality is turned off
 - ◊ 1 - An LP-00 state is forced at the output of the low-power drivers
- Bit 3: Bypass LP TX enable
 - ◊ 0 - LP TX enable is controlled by the internal FSM
 - ◊ 1 - LP TX enable is controlled by the test interface
- Bit 2: LP TX enable
 - ◊ 0 - Driver does not transmit incoming data
 - ◊ 1 - Driver does transmit incoming data
- Bit 1: Bypass LP TX power-on
 - ◊ 0 - LP TX is powered off
 - ◊ 1 - LP TX is powered on
- Bit 0: LP TX power-on

- ◊ 0 - LP TX is powered off
- ◊ 1 - LP TX is powered on

Testdout:

Table 12-96 H P TX Control of Lane 1 Testdout

r-1'b0	r-1'b0	r-1'b0	r-1'b0	r-1'b0	r-1'b0	r-1'b0	r-1'b0
Bypass LP TX enable pull-up loopback	LP TX enable pull-up loopback	Bypass LP TX enable pull-down loopback	LP TX enable pull-down loopback	Bypass LP TX enable loopback	LP TX enable loopback	Bypass LP TX power-on loopback	LP TX power-on loopback

12.4.4.45 LP TX Control of Lane 1**Test Code: 0x53**

This test code controls the low-power single-ended drivers of the clock lane by overriding the control signals sent by the FSM.

Test Data:

Table 12-97 L P TX Control of Lane 1 TestData

w-5'b00000	w-1'b0	w-2'b00
Reserved	Bypass LP TX driver data-in	LP TX driver data-in

Bits 7...3: Reserved

- Bit 2: Bypass LP TX driver data-in
 - ◊ 0 - Inputs of the LP TX driver are controlled by the internal FSM
 - ◊ 1 - Inputs of the LP TX driver are controlled by the test interface
- Bits 1...0: LP TX driver data-in
 - Inputs of the LP TX driver

Testdout:

Table 12-98 L P TX Control of Lane 1 Testdout

r-5'b00000	r-1'b0	r-2'b00
5'b00000	Bypass LP TX driver data-in loopback	LP TX driver data-in loopback

12.4.4.46 HS RX Control of Lane 1**Test Code: 0x54**

This test code controls the high-speed differential receiver of the data lane 1 by overriding the control signals sent by the FSM.

Test Data:

Table 12-99 H S RX Control of Lane 1 TestDat:

w-2'b00	w-1'b0	w-1'b0	w-1'b0	w-1'b0	w-1'b0	w-1'b0
Set 0	Bypass HS RXtermination enable	HS RX termination enable	Bypass HS RX offset calibration enable	HS RX offset calibration enable	Bypass HS RXpower-on	HS RXpower-on
Set 1	Bypass HS RX offset compensation setting	HS RX offset compensation setting				
Set 2	Reserved					

- Bits 7...6: Program selector
 - ◊ 01 - Nothing is programmed (combination is used for observability only)
 - ◊ 10 - Set 0 is programmed
 - ◊ 11 - Set 1 is programmed
 - ◊ 00 - Set 2 is programmed

Set 0:

- Bit 5: Bypass HS RX termination enable
 - ✧ 0 - HS RX termination enable is controlled by the internal FSM
 - ✧ 1 - HS RX termination enable is controlled by the test interface
- Bit 4: HS RX termination enable
 - ✧ 0 - Termination is not enabled
 - ✧ 1 - Termination is enabled
- Bit 3: Bypass HS RX calibration enable
 - ✧ 0 - HS RX calibration enable is controlled by the internal FSM
 - ✧ 1 - HS RX calibration enable is controlled by the test interface
- Bit 2: HS RX calibration enable
 - ✧ 0 - HS RX calibration is not enabled
 - ✧ 1 - HS RX calibration is enabled
- Bit 1: Bypass HS RX power-on
 - ✧ 0 - HS RX power-on is controlled by the internal FSM
 - ✧ 1 - HS RX power-on is controlled by the test interface
- Bit 0: HS RX power-on
 - ✧ 0 - HS RX is powered off
 - ✧ 1 - HS RX is powered on

Set 1:

- Bit 5: Bypass HS RX offset compensation setting
- Bits 4...0: HS RX offset compensation setting

Set 2:

- Bits 5...1: Reserved
- Bit 0: Bypass HS RX settle filter

Testdout:

Table 12-100 H S RX Control of Lane 1 Testdout

r-2'b00	r-1'b0	r-1'b0	r-1'b0	r-1'b0	r-1'b0	r-1'b0
2'b00	Bypass HS RX termination enable loopback	HS RX termination enable loopback	Bypass HS RX offset calibration enable loopback	HS RX offset calibration enable loopback	Bypass HS RX power-on loopback	HS RX power-on loopback
2'b00	Bypass HS RX offset compensation setting loopback	HS RX offset compensation setting loopback				
7'b00000000				Bypass HS RX settle filter loopback		

- First row of Table , if MIPIC_PHY_TST_CTRL_1 [7:6] = 2'b10
- Second row of Table , if MIPIC_PHY_TST_CTRL_1 [7:6] = 2'b11
- Third row of Table , if MIPIC_PHY_TST_CTRL_1 [7:6] = 2'b0x, where x = 0 or 1

12.4.4.47 DATAP/DATAN Swap for Lane 1**Test Code: 0x55**

This test code sets the correct operation of data lane 1 when a DATAP/DATAN swap is required.

Test Data:

Table 12-101 DATAP/DATAN Swap for Lane 1 TestData

w-7'b0000000	w-1'b0
7'b0000000	Polarity change

- Bits 7...1: Reserved
- Bit 0: Polarity change
 - ✧ 0 - Two MIPI D-PHY with DATAP/DATAN ports connected to DATAP/DATAN

- respectively
- ◊ 1 - Two MIPI D-PHY with DATAP/DATAN ports connected to DATAN/DATAP respectively

Testdout:

Table 12-102 DATAP/DATAN Swap for Lane 1 Testdout

r-7'b00000000	r-1'b0
7'b0000000	Polarity change loopback

12.4.4.48 HS RX Lane 1 Outputs and Calibration Errors Observability**Test Code: 0x56**

This test code allows the observability of the outputs of the calibration machine and HS RX of lane 1.

Testdout:

Table 12-103 HS RX Lane 1 Outputs and Calibration Errors Observability Testdout

r-1'b0	r-1'b0	r-1'b0	r-1'b0	r-4'b0000
3'b000			HS RX offset compensation setting	
HS RX asynchronous output		HS RX synchronous output		HS RX calibration errors

- First row of Table , if MIPIC_PHY_TST_CTRL_1 [7] = 1'b0
- Second row of Table , if MIPIC_PHY_TST_CTRL_1 [7] = 1'b1
 - ◊ Bits 7...6: HS RX asynchronous output
Asynchronous output of HS RX received in the differential pair
 - ◊ Bits 5...4: HS RX synchronous output
Synchronous output of HS RX (clock from the clock lane used to sample)
 - ◊ Bits 3....0: HS RX calibration error flags

12.4.4.49 BIST Control and Observability on Lane 1**Test Code: 0x57**

This test code allows the control and observability of the BIST internal machine mechanism for lane 1.

Test Data:

Table 12-104 BIST Control and Observability on Lane 1 TestData

w-6'b000000	w-1'b0	w-1'b1
Reserved	BIST no lock	BIST enable/disable

- Bits 7...2: Reserved
- Bits 1: BIST no lock
 - ◊ 0 - BIST stops when it reaches the last value
 - ◊ 1 - BIST in loop
- Bits 0: BIST lane enable/disable
 - ◊ 0 - Disable BIST lane 1
 - ◊ 1 - Enable BIST lane 1

Testdout:

Table 12-105 BIST Control and Observability on Lane 1 Testdout

r-3'b000	r-1'b0	r-1'b0	r-1'b0	r-1'b0	r-1'b1
3'b000	BIST error	BIST ok	BIST ongoing	BIST no lock	BIST enable/disable

12.4.4.50 HS TX Clock Lane Request State Time (T_{LP}) Control

Test Code: 0x60

This test code controls the time when the clock lane CLKP/CLKN lines are at HS request state (LP-01) during a HS clock transmission. Refer to the D-PHY specification for more information. Most of T_{LP} is contributed by the counter programming:

$$T_{LP} = ((counter_threshold + 1) \times TXBYTECLKHS) + constant_time$$

where:

constant_time corresponds to internal D-PHY FSM state and Analog Front End (AFE) timing variation

Test Data:

Table 12-106 HS TX Clock Lane Request State Time (TLP) Control TestData

w-1'b0	w-7'b0001011
Bypass T_{LP} clock lane counter threshold	T_{LP} clock lane counter threshold

- Bit 7: Bypass T_{LP} clock lane counter threshold default
 - 0 - HS TX clock lane request state time (T_{LP}) is programmed with the default values for the corresponding hsfreqrange (HS RX Control of Lane 0)
 - 1 - HS TX clock lane request state time (T_{LP}) programmed with bits 6...0
- Bits 6..0: T_{LP} clock lane counter threshold

Testdout:

Table 12-107 HS TX Clock Lane Request State Time (TLP) Control Testdout

r-1'b0	r-7'b0001011
Bypass T_{LP} clock lane counter threshold default loopback	T_{LP} clock lane counter threshold loopback

12.4.4.51 HS TX Clock Lane Prepare State Time ($T_{CLK\text{-}prepare}$) Control

Test Code: 0x61

This test code controls the time that clock lane CLKP/CLKN lines are at the HS prepare state (LP-00) during a HS clock transmission. Refer to the D-PHY specification for more information.

$$T_{CLK\text{-}PREPARE} = ((counter_threshold + 1) \times TXDDRCLKHSI_IN) + constant_time$$

where:

constant_time corresponds to internal D-PHY FSM state and Analog Front End (AFE) timing variation

Test Data:

Table 12-108 HS TX Clock Lane Prepare State Time (TCLK-prepare) Control TestData

w-1'b0	w-7'b0000101
Bypass TCLK-prepare counter threshold default	TCLK-prepare counter threshold

- Bit 7: Bypass $T_{CLK\text{-}prepare}$ counter threshold default
 - 0 - HS TX clock lane prepare state time ($T_{CLK\text{-}prepare}$) is programmed with the default values for the corresponding hsfreqrange (HS RX Control of Lane 0)
 - 1 - HS TX clock lane prepare state time ($T_{CLK\text{-}prepare}$) programmed with bits 6...0
- Bits 6...0: TCLK-prepare counter threshold

Testdout:

Table 12-109 HS TX Clock Lane Prepare State Time (TCLK-prepare) Control Testdout

r-1'b0	r-7'b0000101
Bypass TCLK-prepare counter threshold default loopback	T _{CLK-prepare} counter threshold loopback

12.4.4.52 HS TX Clock Lane HS-Zero State Time (T_{CLK-zero}) Control

Test Code: 0x62

This test code controls the time that clock lane CLKP/CLKN lines are at HS-zero state (HS-0) during a HS clock transmission. Refer to the D-PHY specification for more information. Most of T_{CLK-ZERO} is contributed by the counter programming:

$$T_{CLK-ZERO} = ((counter_threshold + 1) \times TXBYTECLKHS) + constant_time$$

where:

constant_time corresponds to internal D-PHY FSM state and Analog Front End (AFE) timing variation

Test Data:

Table 12-110 HS TX Clock Lane HS-Zero State Time (TCLK-zero) Control TestData

w-1'b0	w-1'b0	w-6'b001010
Reserved	Bypass T _{CLK-ZERO} counter threshold default	T _{CLK-Zero} counter threshold

- Bit 7: Reserved
- Bit 6: Bypass T_{CLK-ZERO} counter threshold default
 - ◆ 0 - HS TX clock lane HS-zero state time (T_{CLK-ZERO}) is programmed with the default values for the corresponding hsfreqrange (HS RX Control of Lane 0)
 - ◆ 1 - HS TX clock lane HS-zero state time (T_{CLK-ZERO} o) programmed with bits 5...0
- Bits 5...0: T_{CLK-ZERO} counter threshold

Testdout:

Table 12-111 HS TX Clock Lane HS-Zero State Time (TCLK-zero) Control Testdout

r-1'b0	r-1'b0	r-6'b001010
1'b0	Bypass T _{CLK-ZERO} counter threshold default loopback	T _{CLK-ZERO} counter threshold loopback

12.4.4.53 HS TX Clock Lane Trail State Time (T_{CLK-TRAIL}) Control

Test Code: 0x63

This test code controls the time that clock lane CLKP/CLKN lines are at state HS-trail state (HS-0) during a HS clock transmission. Refer to the D-PHY specification for more information. Most of T_{CLK-TRAIL} is contributed by the counter programming:

$$T_{CLK-TRAIL} = ((counter_threshold + 1) \times TXDDRCLKHSI_IN) + constant_time$$

where:

constant_time corresponds to internal D-PHY FSM state and Analog Front End (AFE) timing variation

Test Data:

Table 12-112 HS TX Clock Lane Trail State Time (TCLK-TRAIL) Control TestData

w-1'b0	w-7'b0000110
Bypass TCLK-trail counter threshold default	T _{CLK-TRAIL} counter threshold

- Bit 7: Bypass $T_{CLK-TRAIL}$ counter threshold default
 - ❖ 0 - HS TX clock lane trail state time ($T_{CLK-TRAIL}$) is programmed with the default values for the corresponding hsfreqrange (HS RX Control of Lane 0)
 - ❖ 1 - HS TX clock lane trail state time ($T_{CLK-TRAIL}$) programmed with bits 6...0
- Bits 6...0: $T_{CLK-TRAIL}$ counter threshold

Testdout:

Table 12-113 HS TX Clock Lane Trail State Time (TCLK-TRAIL) Control Testdout

r-1'b0	r-7'b00000110
Bypass $T_{CLK-TRAIL}$ counter threshold default loopback	$T_{CLK-TRAIL}$ counter threshold loopback

12.4.4.54 HS TX Clock Lane Exit State Time ($T_{HS-EXIT}$) Control**Test Code: 0x64**

This test code controls the time when the clock lane CLKP/CLKN lines are at HS-exit state (LP-11) after a

HS clock transmission. Refer to the D-PHY specification for more information.

Most of $T_{HS-EXIT}$ is contributed by the counter programming:

$$T_{HS-EXIT} = ((counter_threshold + 1) \times TXBYTECLKHS) + constant_time$$

where:

constant_time corresponds to internal D-PHY FSM state and Analog Front End (AFE) timing variation

Test Data:

Table 12-114 HS TX Clock Lane Exit State Time (THS-EXIT) Control TestData

w-2'b00	w-1'b0	w-5'b00100
Reserved	Bypass $T_{HS-EXIT}$ clock lane counter threshold default	$T_{HS-EXIT}$ clock lane counter threshold

- Bit 7...6: Reserved
- Bit 5: Bypass $T_{HS-EXIT}$ counter threshold default
 - ❖ 0 - HS TX clock lane HS-exit state time ($T_{HS-EXIT}$) programmed with the default values for the corresponding hsfreqrange (HS RX Control of Lane 0)
 - ❖ 1 - HS TX clock lane HS-exit state time ($T_{HS-EXIT}$) is programmed with bits 4...0
- Bits 4..0: $T_{HS-EXIT}$ counter threshold

Testdout:

Table 12-115 HS TX Clock Lane Exit State Time (THS-EXIT) Control Testdout

r-2'b00	r-1'b0	r-5'b00100
2'b00	Bypass $T_{HS-EXIT}$ clock lane counter threshold default loopback	$T_{HS-EXIT}$ clock lane counter threshold loopback

12.4.4.55 HS TX Clock Lane Clock Post Time ($T_{CLK-POST}$) Control**Test Code: 0x65**

This test code controls the time during which the clock lane keeps sending the HS-clock after the last associated data lane has transitioned to LP mode. Refer to the D-PHY specification for more information.

$$T_{CLK-POST} = ((counter_threshold + 1) \times TXBYTECLKHS) + constant_time$$

where:

constant_time corresponds to internal D-PHY FSM state and Analog Front End (AFE) timing variation

Test Data:

Table 12-116 HS TX Clock Lane Clock Post Time (TCLK-POST) Control TestData

w-2'b00	w-1'b0	w-5'b01001
Reserved	Bypass T _{CLK-POST} counter threshold default	T _{CLK-POST} counter threshold

- Bits 7...6: Reserved
- Bit 5: Bypass T_{CLK-POST} counter threshold default
 - ❖ 0 - HS TX clock post state time (T_{CLK-POST}) is programmed with the default values for the corresponding hsfreqrange (HS RX Control of Lane 0)
 - ❖ 1 - HS-TX clock post state time (T_{CLK-POST}) is programmed with bits 4...0
- Bits 4...0: T_{CLK-POST} counter threshold

Table 12-117 HS TX Clock Lane Clock Post Time (TCLK-POST) Control Testdout

r-2'b00	r-1'b0	r-5'b01001
2'b00	Bypass T _{CLK-POST} clock lane counter threshold default loopback	T _{CLK-POST} clock lane counter threshold loopback

12.4.4.56 HS TX Data Lane Request State Time (T_{LP}) Control

Test Code: 0x70

This test code controls the time when the data lanes DATAP/DATAN lines are at HS request state (LP-01)

during a HS transmission. Refer to the D-PHY specification for more information.

Most of T_{LP} is contributed by the counter programming:

$$T_{LP} = ((counter_threshold + 1) \times TXBYTECLKHS) + constant_timem$$

where:

constant_time corresponds to internal D-PHY FSM state and Analog Front End (AFE) timing variation

Test Data:

Table 12-118 HS TX Data Lane Request State Time (TLP) Control TestData

w-1'b0	w-7'b0001011
Bypass T _{LP} data lanes counter threshold default	T _{LP} data lanes counter threshold

- Bit 7: Bypass T_{LP} data lanes counter threshold default
 - ❖ 0 - HS TX data lanes request state time (T_{LP}) is programmed with the default values for the corresponding hsfreqrange (HS RX Control of Lane 0)
 - ❖ 1 - HS-TX data lanes request state time (T_{LP}) is programmed with bits 6...0
- Bits 6...0: T_{LP} data lanes counter threshold

Testdout:

Table 12-119 HS TX Data Lane Request State Time (TLP) Control Testdout

r-1'b0	r-7'b0001011
Bypass T _{LP} data lanes counter threshold default loopback	T _{LP} data lanes counter threshold loopback

12.4.4.57 HS TX Data Lanes Prepare State Time ($T_{HS-PREPARE}$) Control

Test Code: 0x71

This test code controls the time when the data lanes DATAP/DATAN lines are at HS prepare state (LP-00)

during a HS transmission. Refer to the D-PHY specification for more information.

Most of $T_{HS-PREPARE}$ is contributed by the counter programming:

$$T_{HS-PREPARE} = ((counter_threshold + 1) \times TXDDRCLKHSI_IN) + constant_time$$

where:

constant_time corresponds to internal D-PHY FSM state and Analog Front End (AFE) timing variation

Test Data:

Table 12-120 HS TX Data Lanes Prepare State Time (THS-PREPARE) Control TestData

w-1'b0	w-7'b0001010
Bypass $T_{HS-PREPARE}$ counter threshold default	$T_{HS-PREPARE}$ counter threshold

- Bit 7: Bypass $T_{HS-PREPARE}$ counter threshold default
 - ❖ 0 - HS TX data lanes prepare state time ($T_{HS-PREPARE}$) is programmed with the default values for the corresponding hsfreqrange (HS RX Control of Lane 0)
 - ❖ 1 - HS TX data lanes prepare state time ($T_{HS-PREPARE}$) programmed with bits 6...0
- Bits 6...0: $T_{HS-PREPARE}$ counter threshold

Testdout:

Table 12-121 HS TX Data Lanes Prepare State Time (THS-PREPARE) Control Testdout

r-1'b0	r-7'b0001010
Bypass $T_{HS-PREPARE}$ counter threshold default loopback	$T_{HS-PREPARE}$ counter threshold loopback

12.4.4.58 HS TX Data Lanes $T_{HS-ZERO}$ State Time ($T_{HS-ZERO}$) Control

Test Code: 0x72

This test code controls the time when the data lanes DATAP/DATAN lines are at HS-zero state (HS-0)

during a HS transmission. Refer to the D-PHY specification for more information.

Most of $T_{HS-ZERO}$ is contributed by the counter programming:

$$T_{HS-ZERO} = ((counter_threshold + 1) \times TXBYTECLKHS) + constant_time$$

where:

constant_time corresponds to internal D-PHY FSM state and Analog Front End (AFE) timing variation

Test Data:

Table 12-122 HS TX Data Lanes THS-ZERO State Time (THS-ZERO) Control TestData

w-1'b0	w-1'b0	w-6'b000110
Reserved	Bypass $T_{HS-ZERO}$ counter threshold default	$T_{HS-ZERO}$ counter threshold

- Bit 7: Reserved
- Bit 6: Bypass $T_{HS-ZERO}$ counter threshold default
 - ❖ 0 - HS TX data lanes HS-zero state time ($T_{HS-ZERO}$) is programmed with the default values for the corresponding hsfreqrange (HS RX Control of Lane 0)

- ◆ 1 - HS TX data lanes HS-zero state time ($T_{HS-ZERO}$) is programmed with bits 5...0
- Bits 5...0: $T_{HS-ZERO}$ counter threshold

Testdout:

Table 12-123 HS TX TX Data Lanes THS-ZERO State Time (THS-ZERO) Control Testdout

r-1'b0	r-1'b0	r-6'b000110
1'b0	Bypass THS-Zero counter threshold default loopback	THS-Zero counter threshold loopback

12.4.4.59 HS TX Data Lanes Trail State Time ($T_{HS-TRAIL}$) Control**Test Code: 0x73**

This test code controls the time when the data lanes DATAP/DATAN lines are at HS-trail state (HS-0) during a HS clock transmission. Refer to the D-PHY specification for more information. Most of $T_{HS-TRAIL}$ is contributed by the counter programming:

$$T_{HS-TRAIL} = ((counter_threshold + 1) \times TXDDRCLKHSI_IN) + constant_time$$

where:

constant_time corresponds to internal D-PHY FSM state and Analog Front End (AFE) timing variation

Test Data:

Table 12-124 HS TX Data Lanes Trail State Time (THS-TRAIL) Control TestData

w-1'b0	w-7'b0001110
Bypass $T_{HS-TRAIL}$ counter threshold default	$T_{HS-TRAIL}$ counter threshold

- Bit 7: Bypass $T_{HS-TRAIL}$ counter threshold default
 - ◆ 0 - HS TX data lanes trail state time ($T_{HS-TRAIL}$) is programmed with the default values for correspondent hsfreqrange (HS RX Control of Lane 0)
 - ◆ 1 - HS TX data lanes trail state time ($T_{HS-TRAIL}$) is programmed with bits 6...0
- Bits 6...0: $T_{HS-TRAIL}$ counter threshold

Testdout:

Table 12-125 HS TX Data Lanes Trail State Time (THS-TRAIL) Control Testdout

r-1'b0	r-7'b0001110
Bypass $T_{HS-TRAIL}$ counter threshold default loopback	$T_{HS-TRAIL}$ counter threshold loopback

12.4.4.60 HS TX Data Lanes Exit State Time ($T_{HS-EXIT}$) Control**Test Code: 0x74**

This test code controls the time when the data lanes DATAP/DATAN lines are at state HS-exit state (LP-11) after a HS clock transmission. Refer to the D-PHY specification for more information. Most of $T_{HS-EXIT}$ is contributed by the counter programming:

$$T_{HS-EXIT} = ((counter_threshold + 1) \times TXBYTECLKHS) + constant_time$$

where:

constant_time corresponds to internal D-PHY FSM state and Analog Front End (AFE) timing variation

Test Data:

Table 12-126 HS TX Data Lanes Exit State Time (THS-EXIT) Control TestData

w-2'b00	w-1'b0	w-5'b00100
Reserved	Bypass $T_{HS-EXIT}$ data lanes counter	$T_{HS-EXIT}$ data lanes counter

	threshold default	threshold
--	-------------------	-----------

- Bit 7...6: Reserved
- Bit 5: Bypass $T_{HS-EXIT}$ counter threshold default
 - ✧ 0 - HS TX data lanes HS-exit state time ($T_{HS-EXIT}$) is programmed with the default values for the corresponding hsfreqrange (HS RX Control of Lane 0)
 - ✧ 1 - HS-TX data lanes HS-exit state time ($T_{HS-EXIT}$) is programmed with bits 4...0.
- Bits 4...0: $T_{HS-EXIT}$ counter threshold

Testdout:

Table 12-127 HS TX Data Lanes Exit State Time (THS-EXIT) Control Testdout

r-2'b00	r-1'b0	r-5'b00100
2'b00	Bypass $T_{HS-EXIT}$ data lanes counter threshold default loopback	$T_{HS-EXIT}$ data lanes counter threshold loopback

12.4.4.61 HS RX Data Lanes Settle State Time (THS-settle) Control**Test Code: 0x75**

This test code controls the time interval during which the HS receiver ignores any Data Lane HS transitions. Refer to the D-PHY specification for more information.

Most of $T_{HS-SETTLE}$ is contributed by the counter programming:

$$T_{HS-SETTLE} = ((counter_threshold + 1) \times TXBYTECLKHS) + constant_time$$

where:

constant_time corresponds to internal D-PHY FSM state and Analog Front End (AFE) timing variation

Test Data:

Table 12-128 HS RX Data Lanes Settle State Time (THS-settle) Control TestData

w-1'b0	w-7'b0001000
Bypass THS-settle counter threshold default	THS-settle counter threshold

- Bit 7: Bypass $T_{HS-SETTLE}$ counter threshold default
 - ✧ 0 - HS RX data lanes settle state time ($T_{HS-SETTLE}$) programmed with default values for the correspondent hsfreqrange (HS RX Control of Lane 0)
 - ✧ 1 - HS RX data lanes settle state time ($T_{HS-SETTLE}$) programmed with bits 6...0
- Bits 6...0: $T_{HS-SETTLE}$ counter threshold

Testdout:

Table 12-129 HS RX Data Lanes Settle State Time (THS-settle) Control Testdout

r-1'b0	r-7'b0001000
Bypass THS-settle counter threshold default loopback	THS-settle counter threshold loopback

12.4.4.62 HS TX and Bias Power on Control of Lane 2**Test Code: 0x80****Test Data:**

Table 12-130 HS RX Data Lanes Settle State Time (THS-settle) Control TestData

w-1'b0	w-1'b0	w-1'b0	w-1'b0	w-1'b0	w-1'b0	w-1'b0	w-1'b0
Bypass HS TX data-in	HS TXdata-in	Bypass HS TX enable	HS TXenable	Bypass HS TXpower-on	HS TXpower-on	Bypass Bias power-on	Bias power-on

- Bit 7: Bypass high-speed driver data
 - ◊ 0 - Internal high-speed driver data is controlled by the internal FSM
 - ◊ 1 - Internal high-speed driver data is controlled by the test interface
- Bit 6: High-speed driver data
 - ◊ 0 - Internal high-speed driver transmits a low level voltage signal '0'
 - ◊ 1 - Internal high-speed driver transmits a high level voltage signal '1'
- Bit 5: Bypass high-speed driver enable
 - ◊ 0 - Internal high-speed driver enable is controlled by the internal FSM
 - ◊ 1 - Internal high-speed driver enable is controlled by the test interface
- Bit 4: High-speed driver enable
 - ◊ 0 - Internal high-speed driver is disabled
 - ◊ 1 - Internal high-speed driver is enabled
- Bit 3: Bypass high-speed driver power-on
 - ◊ 0 - Internal high-speed driver power-on is controlled by the internal FSM
 - ◊ 1 - Internal high-speed driver power-on is controlled by the test interface
- Bit 2: High-speed driver power-on
 - ◊ 0 - Internal high-speed driver is powered off
 - ◊ 1 - Internal high-speed driver is powered on
- Bit 1: Bypass clock lane bias block power-on
 - ◊ 0 - Internal biasing block is controlled by the internal FSM
 - ◊ 1 - Internal biasing block is controlled by the test interface
- Bit 0: Clock lane bias block power-on
 - ◊ 0 - Internal biasing block is powered off
 - ◊ 1 - Internal biasing block is powered on

Testdout:

Table 12-131 HS RX Data Lanes Settle State Time (THS-settle) Control Testdout

r-1'b0	r-1'b0	r-1'b0	r-1'b0	r-1'b0	r-1'b0	r-1'b0	r-1'b0
Bypass HS TX data-in loopback	HS TX data-in loopback	Bypass HS TX enable loopback	HS TX enable loopback	Bypass HS TX power-on loopback	HS TX power-on loopback	Bypass Bias power-on loopback	Bias power-on loopback

12.4.4.63 LP RX Control of Lane 2**Test Code: 0x81**

This test code controls the low-power single-ended receivers of lane 0 by overriding the control signals sent by the FSM.

Test Data:

Table 12-132 LP RX Control of Lane 2 TestData

w-1'b0	w-1'b0	w-1'b0	w-1'b0	w-1'b0	w-1'b0	w-1'b0	w-1'b0
Set 1	Reserved	Bypass LP CD power-on	LP CDpower-on	Bypass ULPpower-on	ULPpower-on	Bypass LPpower-on	LP power-on

- Bit 7: Program selector
 - ◊ 0 - Does not program anything
 - ◊ 1 - Programs Set 1 registers
- Bit 6: Reserved
- Bit 5: Bypass LP CD power-on
 - ◊ 0 - LP CD power-on is controlled by the internal FSM
 - ◊ 1 - LP CD power-on is controlled by the test interface
- Bit 4: LP CD power-on
 - ◊ 0 - LP CD is powered off
 - ◊ 1 - LP CD is powered on
- Bit 3: Bypass ULP RX power-on
 - ◊ 0 - ULP RX power-on is controlled by the internal FSM

- ◆ 1 - ULP RX power-on is controlled by the test interface
- Bit 2: ULP RX power-on
 - ◆ 0 - ULP RX is powered off
 - ◆ 1 - ULP RX is powered on
- Bit 1: Bypass LP RX power-on
 - ◆ 0 - LP RX power-on is controlled by the internal FSM
 - ◆ 1 - LP RX power-on is controlled by the test interface
- Bit 0: LP RX power-on
 - ◆ 0 - LP RX is powered off
 - ◆ 1 - LP RX is powered on

Testdout:

Table 12-133 LP RX Control of Lane 2 Testdout

r-2'b00	r-1'b0	r-1'b0	r-1'b0	r-1'b0	r-1'b0	r-1'b0
2'b00	Bypass LP CD power-on loopback	LP CD power-on loopback	Bypass ULP power-on loopback	ULP power-on loopback	Bypass LP power-on loopback	LP power-on loopback
2'b00	LP CD data-out			ULP RX data-out		LP RX data-out

- First row of Table , if MIPIC_PHY_TST_CTRL_1 [7] = 1'b1
Set 1 loopback
- Second row of Table , if MIPIC_PHY_TST_CTRL_1 [7] = 1'b0
 - ◆ Bits 7...6: Reserved
 - ◆ Bits 5...4: LP CD data-out
- Data from the two single-ended low-power contention detectors
 - ◆ Bits 3...2: ULP RX data-out
 - Data from the two single-ended low-power receivers used to detect that TX has left Ultra Low Power state
 - ◆ Bits 1...0: LP RX data-out
 - Data from the two single-ended low-power receivers when in low-power mode

12.4.4.64 LP TX Control of Lane 2**Test Code: 0x82**

This test code controls the low-power single-ended drivers of the clock lane by overriding the control signals sent by the FSM.

Test Data:

Table 12-134 LP TX Control of Lane 2 TestData

w-1'b0	w-1'b0	w-1'b0	w-1'b0	w-1'b0	w-1'b0	w-1'b0
Bypass LP TXenable idle low-power	LP TX enable idle low-power	Bypass LP TXenable pull-down	LP TX enable pull-down	Bypass LP TXenable	LP TXenable	Bypass LP TX power-on

- Bit 7: Bypass the LP TX enable idle low-power
 - ◆ 0 - LP TX enable idle low-power is controlled by the internal FSM
 - ◆ 1 - LP TX enable idle low-power is controlled by the test interface
- Bit 6: LP TX enable ulp
 - ◆ 0 - Disable low-power for idle mode
 - ◆ 1 - Enable low-power for idle mode
- Bit 5: Bypass LP TX enable pull-down
 - ◆ 0 - LP TX enable pull-down is controlled by the internal FSM
 - ◆ 1 - LP TX enable pull-down is controlled by the test interface
- Bit 4: LP TX enable pull-down

- ◊ 0 - Pull down functionality is turned off
- ◊ 1 - A LP-00 state is forced at the output of the low-power drivers
- Bit 3: Bypass LP TX enable
 - ◊ 0 - LP TX enable is controlled by the internal FSM
 - ◊ 1 - LP TX enable is controlled by the test interface
- Bit 2: LP TX enable
 - ◊ 0 - Driver does not transmit the incoming data
 - ◊ 1 - Driver transmits the incoming data
- Bit 1: Bypass LP TX power-on
 - ◊ 0 - LP TX is powered off
 - ◊ 1 - LP TX is powered on
- Bit 0: LP TX power-on
 - ◊ 0 - LP TX is powered off
 - ◊ 1 - LP TX is powered on

Testdout:

Table 12-135 LP TX Control of Lane 2 Testdout

r-1'b0	r-1'b0	r-1'b0	r-1'b0	r-1'b0	r-1'b0	r-1'b0
Bypass LP TX enable pull-up loopback	LP TX enable pull-up loopback	Bypass LP TX enable pull-down loopback	LP TX enable pull-down loopback	Bypass LP TX enable loopback	LP TX enable loopback	Bypass LP TX power-on loopback

12.4.4.65 LP TX Control of Lane 2**Test Code: 0x83**

This test code controls the low-power single-ended drivers of the clock lane by overriding the control signals sent by the FSM.

Test Data:

Table 12-136 LP TX Control of Lane 2 TestData

w-5'b00000	w-1'b0	w-2'b00
Reserved	Bypass LP TX driver data-in	LP TX driver data-in

- Bits 7...3: Reserved
- Bit 2: Bypass LP TX driver data-in
 - ◊ 0 - Inputs of LP TX driver are controlled by the internal FSM
 - ◊ 1 - Inputs of LP TX driver are controlled by the test interface
- Bits 0...1: LP TX driver data-in
 - Inputs of LP TX driver

Testdout:

Table 12-137 LP TX Control of Lane 2 Testdout

r-5'b00000	r-1'b0	r-2'b00
5'b00000	Bypass LP TX driver data-in loopback	LP TX driver data-in loopback

12.4.4.66 HS RX Control of Lane 2**Test Code: 0x84**

This test code controls the high-speed differential receiver of the data lane 2 by overriding the control signals sent by the FSM.

Table 12-138 HS RX Control of Lane 2 TestData

w-2'b00	w-1'b0	w-1'b0	w-1'b0	w-1'b0	w-1'b0	w-1'b0
Set 0	Bypass HS RXtermination enable	HS RX termination enable	Bypass HS RX offset calibration enable	HS RX offset calibration enable	Bypass HS RXpower-on	HS RX power-on
Set 1	Bypass HS RX offset	HS RX offset compensation setting				

	compensation setting	
Set 2	Reserved	BypassHS-RX settlefilter

- Bits 7...6: Program selector
 - ◊ 01 - Nothing is programmed (combination is used for observability only)
 - ◊ 10 - Set 0 is programmed
 - ◊ 11 - Set 1 is programmed
 - ◊ 00 - Set 2 is programmed

Set 0:

- Bit 5: Bypass HS RX termination enable
 - ◊ 0 - HS RX termination enable is controlled by the internal FSM
 - ◊ 1 - HS RX termination enable is controlled by the test interface
- Bit 4: HS RX termination enable
 - ◊ 1 - Termination is enabled
 - ◊ 0 - Termination is not enabled
- Bit 3: Bypass HS RX calibration enable
 - ◊ 0 - HS RX calibration enable is controlled by the internal FSM
 - ◊ 1 - HS RX calibration enable is controlled by the test interface
- Bit 2: HS RX calibration enable
 - ◊ 0 - HS RX calibration is not enabled
 - ◊ 1 - HS RX calibration is enabled
- Bit 1: Bypass HS RX power-on
 - ◊ 0 - HS RX power-on is controlled by the internal FSM
 - ◊ 1 - HS RX power-on is controlled by the test interface
- Bit 0: HS RX power-on
 - ◊ 0 - HS RX is powered off
 - ◊ 1 - HS RX is powered on

Set 1:

- Bit 5: Bypass HS RX offset compensation setting
- Bits 4...0: HS RX offset compensation setting

Set 2:

- Bits 5...1: Reserved
- Bit 0: Bypass HS RX settle filter

Testdout:

Table 12-139 HS RX Control of Lane 2 Testdout

r-2'b00	r-1'b0	r-1'b0	r-1'b0	r-1'b0	r-1'b0	r-1'b0					
2'b00	Bypass HS RX termination enable loopback	HS RX termination enable loopback	Bypass HS RX offset calibration enable loopback	HS RX offset calibration enable loopback	Bypass HS RX power-on loopback	HS RX power-on loopback					
2'b00	Bypass HS RX offset compensation setting loopback	HS RX offset compensation setting loopback									
7'b00000000											
	Bypass HS RX settle filter loopback										

- First row of table in 12.4.4.66 if MIPIC_PHY_TST_CTRL_1 [7:6] = 2'b10
- Second row of table in 12.4.4.66, if MIPIC_PHY_TST_CTRL_1[7:6] = 2'b11
- Third row of table in 12.4.4.66, if MIPIC_PHY_TST_CTRL_1[7:6] = 2'b0x, where x = 0 or 1

12.4.4.67 DATAP/DATAN Swap for Lane 2

Test Code: 0x85

This test code sets the correct behavior of data lane 2 in case a DATAP/DATAN swap is required.

Test Data:

Table 12-140 DATAP/DATAN Swap for Lane 2 TestData

w-7'b0000000	w-1'b0
Reserved	Polarity change

- Bits 7...1: Reserved
- Bit 0: Polarity change
 - ❖ 0 - Two MIPI D-PHY with DATAP/DATAN ports connected to DATAP/DATAN respectively
 - ❖ 1 - Two MIPI D-PHY with DATAP/DATAN ports connected to DATAN/DATAP respectively

Testdout:

Table 12-141 DATAP/DATAN Swap for Lane 2 Testdout

r-7'b0000000	r-1'b0
Reserved	Polarity change loopback

12.4.4.68 HS RX Lane 2 Outputs and Calibration Errors Observability

Test Code: 0x86

This test code allows the observability of some outputs of the calibration machine and HS RX of lane 2.

Test

Data:

Testdout:

Table 12-142 HS RX Lane 2 Outputs and Calibration Errors Observability Testdout

r-1'b0	r-1'b0	r-1'b0	r-1'b0	r-4'b0000
3'b000	HS RX offset compensation setting			
HS RX asynchronous output	HS RX synchronous output		HS RX calibration errors	

- First row of Table, if MIPIC_PHY_TST_CTRL_1 [7] = 1'b0
- Second row of Table, if MIPIC_PHY_TST_CTRL_1 [7] = 1'b1
 - ❖ Bits 7...6: HS RX asynchronous output
Asynchronous output of HS RX received in the differential pair
 - ❖ Bits 5...4: HS RX synchronous output
Synchronous output of HS RX (clock from the clock lane used to sample)
 - ❖ Bits 3...0: HS RX calibration error flags

12.4.4.69 BIST Control and Observability on Lane 2

Test Code: 0x87

This test code allows the control and observability of the BIST internal machine mechanism for lane 2.

Test Data:

Table 12-143 BIST Control and Observability on Lane 2 TestData

w-6'b000000	w-1'b0	w-1'b1
Reserved	BIST no lock	BIST enable/disable

- Bits 7...2: Reserved
- Bits 1: BIST no lock
 - ❖ 0 - BIST stops when it reaches the last value

- ◊ 1 - BIST in loop
- Bits 0: BIST lane enable/disable
 - ◊ 0 - Disable BIST lane 2
 - ◊ 1 - Enable BIST lane 2

Testdout:

Table 12-144 BIST Control and Observability on Lane 2 Testdout

r-3'b000	r-1'b0	r-1'b0	r-1'b0	r-1'b0	r-1'b1	r-3'b000
3'b000	BIST error	BIST ok	BIST ongoing	BIST no lock	BIST enable/disable	3'b000

12.4.4.70 HS TX and Bias Power on Control of Lane 3**Test Code: 0x90****Test Data:**

Table 12-145 HS TX and Bias Power on Control of Lane 3 Testdata

w-1'b0	w-1'b0	w-1'b0	w-1'b0	w-1'b0	w-1'b0	w-1'b0	w-1'b0
Bypass HS TX data-in	HS TXdata-in	Bypass HS TX enable	HS TXenable	Bypass HS TXpower-on	HS TXpower-on	Bypass Bias power-on	Bias power-on

- Bit 7: Bypass high-speed driver data
 - ◊ 0 - Internal high-speed driver data is controlled by the internal FSM
 - ◊ 1 - Internal high-speed driver data is controlled by the test interface
- Bit 6: High-speed driver data
 - ◊ 0 - Internal high-speed driver transmits a low level voltage signal 0
 - ◊ 1 - Internal high-speed driver transmits a high level voltage signal 1
- Bit 5: Bypass high-speed driver enable
 - ◊ 0 - Internal high-speed driver enable is controlled by the internal FSM
 - ◊ 1 - Internal high-speed driver enable is controlled by the test interface
- Bit 4: High-speed driver enable
 - ◊ 0 - Internal high-speed driver is disabled
 - ◊ 1 - Internal high-speed driver is enabled
- Bit 3: Bypass high-speed driver power-on
 - ◊ 0 - Internal high-speed driver power-on is controlled by the internal FSM
 - ◊ 1 - Internal high-speed driver power-on is controlled by the test interface
- Bit 2: High-speed driver power-on
 - ◊ 0 - Internal high-speed driver is powered off
 - ◊ 1 - Internal high-speed driver is powered on
- Bit 1: Bypass clock lane bias block power-on
 - ◊ 0 - Internal biasing block is controlled by the internal FSM
 - ◊ 1 - Internal biasing block is controlled by the test interface
- Bit 0: Clock lane bias block power-on
 - ◊ 0 - Internal biasing block is powered off
 - ◊ 1 - Internal biasing block is powered on

Testdout:

Table 12-146 HS TX and Bias Power on Control of Lane 3 Testdout

r-1'b0	r-1'b0	r-1'b0	r-1'b0	r-1'b0	r-1'b0	r-1'b0	r-1'b0
Bypass HS TX data-in loopback	HS TX data-in loopback	Bypass HS TX enable loopback	HS TX enable loopback	Bypass HS TX power-on loopback	HS TX power-on loopback	Bypass Bias power-on loopback	Bias power-on loopback

12.4.4.71 LP RX Control of Lane 3**Test Code: 0x91**

This test code controls the low-power single-ended receivers of lane 3 by overriding the control signals sent by the FSM.

Test Data:

Table 12-147 LP RX Control of Lane 3 TestData

w-1'b0	w-1'b0	w-1'b0	w-1'b0	w-1'b0	w-1'b0	w-1'b0	w-1'b0
Set 1	Reserved	Bypass LP CD power-on	LP CDpower-on	Bypass ULPpower-on	ULPpower-on	Bypass LPpower-on	LP power-on

- Bit 7: Program selector
 - ◇ 0 - Does not program anything
 - ◇ 1 - Programs Set 1 registers
- Bit 6: Reserved
- Bit 5: Bypass LP CD power-on
 - ◇ 0 - LP CD power-on is controlled by the internal FSM
 - ◇ 1 - LP CD power-on is controlled by the test interface
- Bit 4: LP CD power-on
 - ◇ 0 - LP CD is powered off
 - ◇ 1 - LP CD is powered on
- Bit 3: Bypass ULP RX power-on
 - ◇ 0 - ULP RX power-on is controlled by the internal FSM
 - ◇ 1 - ULP RX power-on is controlled by the test interface
- Bit 2: ULP RX power-on
 - ◇ 0 - ULP RX is powered off
 - ◇ 1 - ULP RX is powered on
- Bit 1: Bypass LP RX power-on
 - ◇ 0 - LP RX power on is controlled by the internal FSM
 - ◇ 1 - LP RX power on is controlled by the test interface
- Bit 0: LP RX power-on
 - ◇ 0 - LP RX is powered off
 - ◇ 1 - LP RX is powered on

Testdout:

Table 12-148 LP RX Control of Lane 3 Testdout

r-2'b00	r-1'b0	r-1'b0	r-1'b0	r-1'b0	r-1'b0	w-1'b0
2'b00	Bypass LP CD power-on loopback	LP CD power-on loopback	Bypass ULP power-on loopback	ULP power-on loopback	Bypass LP power-on loopback	LP power-on
2'b00	LP CD data-out		ULP RX data-out			LP RX data-out

- First row of Table, if MIPIC_PHY_TST_CTRL_1 [7] = 1'b1
Set 1 loopback
- Second row of Table, if MIPIC_PHY_TST_CTRL_1 [7] = 1'b0
 - ◇ Bits 7...6: Reserved
 - ◇ Bits 5...4: LP CD data-out
 - Data from the two single-ended low-power contention detectors
 - ◇ Bits 3...2: ULP RX data-out
 - Data from the two single-ended low-power receivers used to detect that TX has left Ultra Low Power state
 - ◇ Bits 1...0: LP RX data-out
 - Data from the two single-ended low-power receivers when in low-power mode

12.4.4.72 LP TX Control of Lane 3

Test Code: 0x92

This test code controls the low-power single-ended drivers of the clock lane by overriding

the control signals sent by the FSM.

Test Data:

Table 12-149 LP TX Control of Lane 3 TestData

w-1'b0	w-1'b0	w-1'b0	w-1'b0	w-1'b0	w-1'b0	w-1'b0	w-1'b0
Bypass LP TX enable idlelow-power	LP TX enable idle low-power	Bypass LP TX nable pull-down	LP TX enable pull-down	Bypass LP TXenable	LP TX enable	Bypass LP TX power-on	LP TXpower-on

- Bit 7: Bypass LP TX enable idle low-power
 - ◆ 0 - LP TX enable idle low-power is controlled by the internal FSM
 - ◆ 1 - LP TX enable idle low-power is controlled by the test interface
- Bit 6: LP TX enable ulp
 - ◆ 0 - Disable low-power for idle mode
 - ◆ 1 - Enable low-power for idle mode
- Bit 5: Bypass LP TX enable pull-down
 - ◆ 0 - LP TX enable pull-down is controlled by the internal FSM
 - ◆ 1 - LP TX enable pull-down is controlled by the test interface
- Bit 4: LP TX enable pull-down
 - ◆ 0 - Pull down functionality is turned off
 - ◆ 1 - A LP-00 state is forced at the output of the low-power drivers
- Bit 3: Bypass LP TX enable
 - ◆ 0 - LP TX enable is controlled by the internal FSM
 - ◆ 1 - LP TX enable is controlled by the test interface
- Bit 2: LP TX enable
 - ◆ 0 - Driver does not transmit incoming data
 - ◆ 1 - Driver does transmit incoming data
- Bit 1: Bypass LP TX power-on
 - ◆ 0 - LP TX is powered off
 - ◆ 1 - LP TX is powered on
- Bit 0: LP TX power on
 - ◆ 0 - LP TX is powered off
 - ◆ 1 - LP TX is powered on

Testdout:

Table 12-150 LP TX Control of Lane 3 Testdout

r-1'b0	r-1'b0	r-1'b0	r-1'b0	r-1'b0	r-1'b0	r-1'b0	r-1'b0	r-1'b0
Bypass LP TX enable pull-up loopback	LP TX enable pull-up loopback	Bypass LP TX enable pull-down loopback	LP TX enable pull-down loopback	Bypass LP TX enable loopback	LP TX enable loopback	Bypass LP TX power-on loopback	LP TX power-on loopback	Bypass LP TX enable pull-up loopback

12.4.4.73 LP TX Control of Lane 3

Test Code: 0x93

This test code controls the low-power single-ended drivers of the clock lane by overriding the control signals sent by the FSM.

Test Data:

Table 12-151 LP TX Control of Lane 3 TestData

w-5'b00000	w-1'b0	w-2'b00
Reserved	Bypass LP TX driver data-in	LP TX driver data-in

- Bits 7...3: Reserved
- Bit 2: Bypass LP TX driver data-in
 - ◆ 0 - Inputs of LP TX driver are controlled by the internal FSM
 - ◆ 1 - Inputs of LP TX driver are controlled by the test interface

- Bits 0...1: LP TX driver data-in
Inputs of LP TX driver

Testdout:

Table 12-152 LP TX Control of Lane 3 Testdout

r-5'b00000	r-1'b0	r-2'b00
5'b00000	Bypass LP TX driver data-in loopback	LP TX driver data-in loopback

12.4.4.74 HS RX Control of Lane 3**Test Code: 0x94**

This test code controls the high-speed differential receiver of the data lane 3 by overriding the control signals sent by the FSM.

Test Data:

Table 12-153 HS RX Control of Lane 3 TestData

w-2'b00	w-1'b0	w-1'b0	w-1'b0	w-1'b0	w-1'b0	w-1'b0
Set 0	Bypass HS RXtermination enable	HS RX termination enable	Bypass HS RX offset calibration enable	HS RX offset calibration enable	Bypass HS RXpower-on	HS RXpower-on
Set 1	Bypass HS RX offset compensation setting	HS RX offset compensation setting				
Set 2	Reserved					

- Bits 7...6: Program selector
 - ◊ 01 - Nothing is programmed (combination is used for observability only)
 - ◊ 10 - Set 0 is programmed
 - ◊ 11 - Set 1 is programmed
 - ◊ 00 - Set 2 is programmed
- Set 0:
 - Bit 5: Bypass HS RX termination enable
 - ◊ 0 - HS RX termination enable is controlled by the internal FSM
 - ◊ 1 - HS RX termination enable is controlled by the test interface
 - Bit 4: HS RX termination enable
 - ◊ 0 - Termination is not enabled
 - ◊ 1 - Termination is enabled
 - Bit 3: Bypass HS RX calibration enable
 - ◊ 0 - HS RX calibration enable is controlled by the internal FSM
 - ◊ 1 - HS RX calibration enable is controlled by the test interface
 - Bit 2: HS RX calibration enable
 - ◊ 0 - HS RX calibration is not enabled.
 - ◊ 1 - HS RX calibration is enabled
 - Bit 1: Bypass HS RX power on
 - ◊ 0 - HS RX power on is controlled by the internal FSM
 - ◊ 1 - HS RX power on is controlled by the test interface
 - Bit 0: HS RX power on
 - ◊ 0 - HS RX is powered off
 - ◊ 1 - HS RX is powered on
- Set 1:
 - Bit 5: Bypass HS RX offset compensation setting
 - Bits 4...0: HS RX offset compensation setting
- Set 2:
 - Bits 5...1: Reserved
 - Bit 0: Bypass HS RX settle filter

Testdout:

Table 12-154 HS RX Control of Lane 3 Testdout

r-7'b0000000 0	r-1'b0	r-7'b0000000 0	r-1'b0	r-7'b0000000 0	r-1'b0	r-1'b0
Reserved	Polarity change loopback	Reserved	Polarity change loopback	Reserved	Bypass HS RX power-on loopback	HS RX power-on loopback
2'b00	Bypass HS RX offset compensation setting loopback	HS RX offset compensation setting loopback				
7'b00000000	Bypass HS RX settle filter loopback					

- First row of Table, if MIPIC_PHY_TST_CTRL_1[7:6] = 2'b10
- Second row of Table, if MIPIC_PHY_TST_CTRL_1 [7:6] = 2'b11
- Third row of Table, if MIPIC_PHY_TST_CTRL_1 [7:6] = 2'b0x, where x = 0 or 1

12.4.4.75 DATAP/DATAN Swap for Lane 3**Test Code: 0x95**

This test code sets the correct behavior of data lane 3 when a DATAP/DATAN swap is required.

Test Data:

Table 12-155 DATAP/DATAN Swap for Lane 3 TestData

w-7'b0000000	w-1'b0
Reserved	Polarity change

- Bits 7...1: Reserved
- Bit 0: Polarity change
 - ◊ 0 - Two DWC MIPI BD 4L D-PHY with DATAP/DATAN ports connected to DATAP/DATAN respectively
 - ◊ 1 - Two DWC MIPI BD 4L D-PHY with DATAP/DATAN ports connected to DATAN/DATAP respectively

Testdout:

Table 12-156 DATAP/DATAN Swap for Lane 3 Testdout

r-7'b0000000	r-1'b0
Reserved	Polarity change loopback

12.4.4.76 HS RX Lane 3 Outputs and Calibration Errors Observability**Test Code: 0x96**

This test code allows the observability of the outputs of the calibration machine and HS RX of lane 3.

Testdout:

Table 12-157 HS RX Lane 3 Outputs and Calibration Errors Observability Testdout

r-1'b0	r-1'b0	r-1'b0	r-1'b0	r-4'b0000
3'b000		HS RX offset compensation setting		
HS RX asynchronous output		HS RX synchronous output		HS RX calibration errors

- First row of Table , if MIPIC_PHY_TST_CTRL_1 [7] = 1'b0
- Second row of Table , if MIPIC_PHY_TST_CTRL_1 [7] = 1'b1
 - ◊ Bits 7...6: HS RX asynchronous output
Asynchronous output of HS RX received in the differential pair
 - ◊ Bits 5...4: HS RX synchronous output
Synchronous output of HS RX (clock from the clock lane used to sample)
 - ◊ Bits 3...0: HS RX calibration error flags

12.4.4.77 BIST Control and Observability on Lane 3

Test Code: 0x97

This test code allows the control and observability of the BIST internal machine mechanism for lane 3.

Test Data:

Table 12-158 BIST Control and Observability on Lane 3 Test Data

w-6'b000000	w-1'b0	w-1'b1
Reserved	BIST no lock	BIST enable/disable

- Bits 7...2: Reserved
- Bits 1: BIST no lock
 - ◊ 0 - BIST stops when it reaches the last value
 - ◊ 1 - BIST in loop
 - Bits 0: BIST lane enable/disable
 - ◊ 0 - Disable BIST lane 3
 - ◊ 1 - Enable BIST lane 3

Testdout:

Table 12-159 BIST Control and Observability on Lane 3 Testdout

r-3'b000	r-1'b0	r-1'b0	r-1'b0	r-1'b0	r-1'b1
3'b000	BIST error	BIST ok	BIST ongoing	BIST no lock	BIST enable/disable

12.5 Application Notes

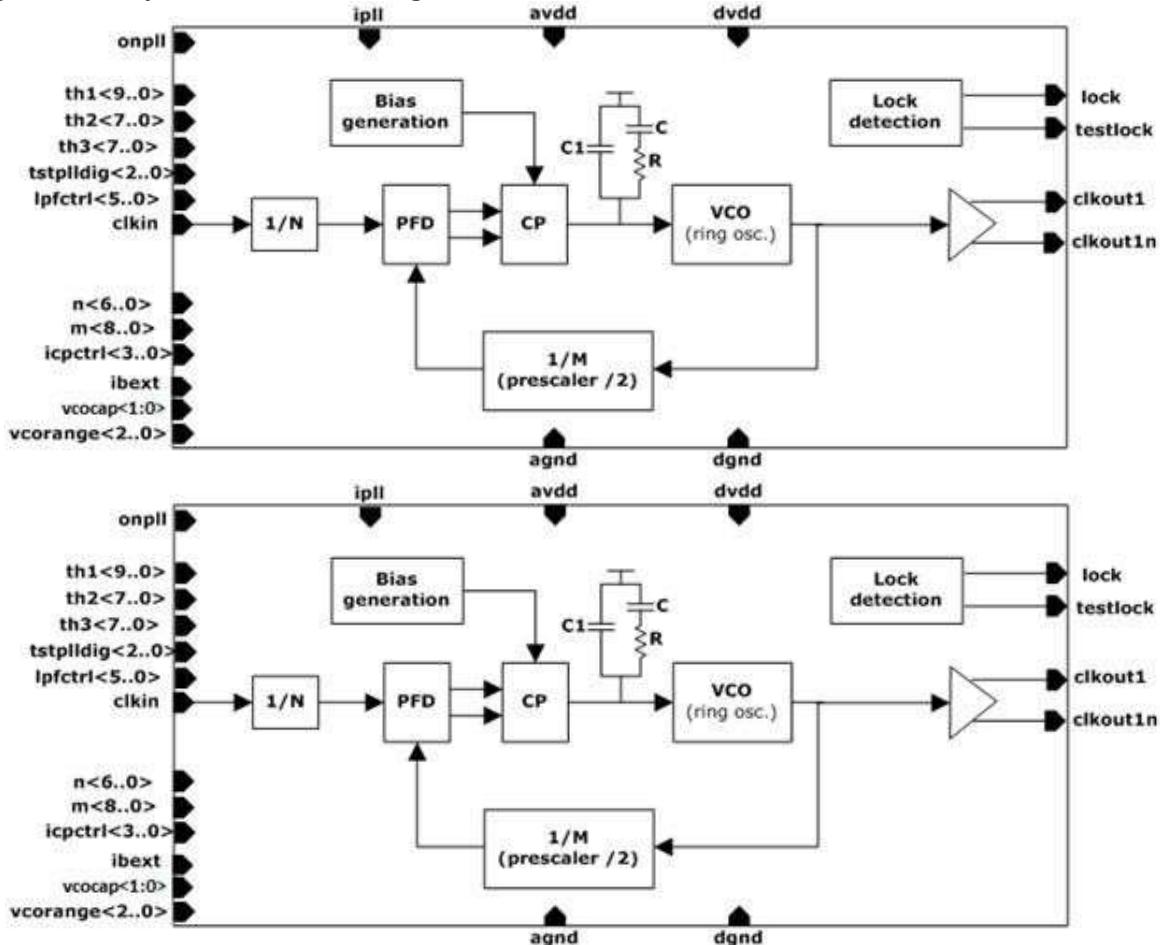
12.5.1 PLL Requirements

12.5.1.1 PLL Programming

Fig. 12-9 PLL System-Level Block Diagram As the MIPI D-PHY is expected to be used in applications where the lane bit rate requirements can change dramatically from system to system, it features a very flexible PLL architecture, fully programmable through the MIPI D-PHY tester interface.

shows a block diagram at the PLL system level.

Fig. 12-9 PLL System-Level Block Diagram



The VCO oscillating frequency is a function of the input reference frequency and of the multiplication and division ratios. It can be determined as follows:

$$f_{vco} = \frac{M}{N} \cdot f_{REFCLK}$$

$$f_{vco} = \frac{M}{N} \cdot f_{REFCLK}$$

Where:

- M is Feedback Multiplication Ratio
- N is Input Frequency Division Ratio

However, the following limit applies:

The VCO ranges are selected as shown in

$$40 \text{ MHz} \geq \frac{f_{REFCLK}}{N} \geq 5 \text{ MHz}$$

$$40 \text{ MHz} \geq \frac{f_{REFCLK}}{N} \geq 5 \text{ MHz}$$

Table 12-160 VCO Ranges

vcorange<2..0>	VCOFrequency(MHz)
000	80-200
001	200-300

010	300-500
011	500-700
100	700-900
101	900-1100
110	1100-1300
111	1300-1500

f_{vco} is the output, full-rate clock used for bit serialization. A 1500 Mbps bit rate on the data lanes assumes f_{vco} to be equal to 1500 MHz.

Finally, the output clock frequency is derived from a programmable division of the VCO frequency:

$$f_{clkout1} = f_{vco}$$

$$f_{clkout1} = f_{vco}$$

Table 12-161 Division Ratios for the Attachable PLL shows the selection bit correspondence

Table 12-161 Division Ratios for the Attachable PLL

m<8..0>= M-1	M	n<6..0>= N-1	N
9'h1	2	7'h0	1
9'h3	4	7'h1	2
...
9'h127	296	7'h61	98
9'h129	298	7'h62	99
9'h12B	300	7'h63	100

Some combinations of N and M are not allowed, since they violate the limits of operation of the VCO or the minimum allowed comparison frequency. Due to the use of a "by 2 pre-scaler," the range of the feedback multiplication value M is limited to even division numbers.

These N and M values should be programmed on the meaningful control registers as presented in 12.4.4 Test and Control Codes Detail Description.

To ensure proper operation of the PLL, the loop bandwidth should be configured depending on the selected frequency. The control over the CP current (icpctrl[3:0]), the LPF characteristics (lpfctrl[5..0]), Table 12-162 PLL CP and LPF Control Bits and vcorange control signals is granted. presents the bits correspondence.

Table 12-162 PLL CP and LPF Control Bits

VCOmin(MHz)	VCOmax(MHz)	Vcorange <2..0>	Icpctrl <3..0>	Lpfctrl <5:0>
80	110	000	1000	001000
110	150		1000	000001
150	200		1000	000000
200	250	001	1000	000010

VCOofmin(MHz)	VCOofmax(MHz)	Vcorange <2..0>	Icpctrl <3..0>	Lpfctrl <5:0>
250	300		0010	000100
300	400	010	0010	010000
400	500		0010	000100
500	600	011	0010	000100
600	700		1001	001000
700	900	100	1001	001000
900	1100	101	0110	100000
1100	1300	110	0110	010000
1300	1500	111	0110	010000

Default value of the input clock is 27 MHz.

Table8-164 shows the default internal setup of the PLL for the different hsfreqrange[5:0] frequency ranges selectable through the control code 0x44.

Table 12-163 PLL Settings for 27 MHz Reference Clock and Selectable Ranges

Range(MHz)	m[8:0] ^a	n[6:0] ^b	Icpctrl <3..0>	Lpfctrl <5..0>	Vcorange <2..0>	Fout ^c [MHz]
80-90	5	1	1000	001000	000	81
90-100	9	2	1000	001000	000	90
100-110	11	2	1000	001000	000	108
110-130	13	2	1000	000001	000	126
130-140	9	1	1000	000001	000	135
140-150	15	2	1000	000001	000	144
150-170	17	2	1000	000000	000	162
170-180	19	2	1000	000000	000	180
180-200	21	2	1000	000000	000	198
200-220	23	2	1000	000010	001	216
220-240	25	2	1000	000010	001	234
240-250	17	1	1000	000010	001	243
250-270	29	2	0010	000100	001	270
270-300	21	1	0010	000100	001	297
300-330	23	1	0010	010000	010	324
330-360	39	2	0010	010000	010	360
360-400	43	2	0010	010000	010	396
400-450	49	2	0010	000100	010	450
450-500	17	0	0010	000100	010	486

Range(MHz)	m[8:0] ^a	n[6:0] ^b	Icpctrl <3..0>	Lpfctrl <5..0>	Vcorange <2..0>	Fout ^c [MHz]
500-550	59	2	0010	000100	011	540
550-600	43	1	0010	000100	011	594
600-650	23	0	1001	001000	011	648
650-700	75	2	1001	001000	011	684
700-750	81	2	1001	001000	100	738
750-800	57	1	1001	001000	100	783
800-850	93	2	1001	001000	100	846
850-900	99	2	1001	001000	100	900
900-950	69	1	0110	100000	101	945
950-1000	73	1	0110	100000	101	999
1050-1100	39	0	0110	100000	101	1080
1100-1150	125	2	0110	010000	110	1134
1150-1200	131	2	0110	010000	110	1188
1200-1250	45	0	0110	010000	110	1242
1250-1300	47	0	0110	010000	110	1296
1300-1350	149	2	0110	010000	111	1350
1350-1400	153	2	0110	010000	111	1386
1400-1450	159	2	0110	010000	111	1440
1450-1500	165	2	0110	010000	111	1494

a.m=M-1 represents the feedback divider, the control word in decimal notation.

b.n = N-1 represents the input divider, the control word in decimal notation.

c. This is the frequency visible at the clkout1 and clkout1n PLL clock outputs.

For reference clock frequencies other than 27 MHz, it is required to configure the PLL using the following control codes described in "Test and Configuration Modes".

- PLL Input Divider Ratio (N): Register 0x17 configuration (n) + 1
- PLL Loop Divider Ratio (M): Register 0x18 configuration (m) + 1
- PLL Post Divider Ratio, PLL Input, and Loop Divider Ratios Control: Register 0x19 : bit 5:4 = 1

Make the previously configured N and M factors effective

NOTE:

Always configure the VCO range, CP and LPF control bits, and hsfreqrange[5:0] correctly, regardless of the PLL reference clock (REFCLK) value.

12.5.1.2 PLL Programming Example

This section illustrates a PLL configuration using REFCLK of 27 MHz, and 24 MHz for an operating bit rate at 324 MHz and 756 MHz.

12.5.1.2.1 REFCLK = 27 MHz

Assuming a REFCLK equal to 27 MHz, the following are cases for an operating bit rate at

324 MHz and 756 MHz:

Case 1 (324 MHz)

To get an operating frequency range of 324 MHz, configure hsfreqrange[5:0] configuration as follows:

hsfreqrange[5:0] = 000101(0x44 = 0x0A).

Case 2 (756 MHz)

To get an operating frequency range of 756 MHz, configure the following:

1. hsfreqrange[5:0] = 011001 (0x44 = 0x3).
2. Input divider ratio programmed: 0x17 = 0x01
PLL Input Divider Ratio (N) = 2
3. Loop divider ratio programmed: 0x18 = 0x17 (LSB)
4. Loop divider ratio programmed: 0x18 = 0x81 (MSB)
PLL Loop Divider Ratio (M) = 56
5. Allow 0x17 and 0x18 programming to be set to: 0x19 = 0x30

12.5.1.2.2 REFCLK = 24 MHz

Assuming a REFCLK not equal to 27 MHz—that is, assuming 24 MHz—the following is a case for an operating bit rate at 324 MHz:

Case 1 (324MHz)

To get an operation frequency range of 324 MHz, configure the following:

1. hsfreqrange[5:0] = 000101 (0x44 = 0x0A).
If no additional testcodes are programmed, the operating frequency range is 288 MHz
2. Input divider ratio programmed: 0x17 = 0x03
PLL Input Divider Ratio (N) = 4
3. Loop divider ratio programmed: 0x18 = 0x15 (LSB)
4. Loop divider ratio programmed: 0x18 = 0x81 (MSB)
PLL Loop Divider Ratio (M) = 54
5. Allow 0x17 and 0x18 programming to be set to: 0x19 = 0x30

12.5.2 Calibration Requirements

12.5.2.1 Introduction

A calibration machine is implemented inside the MIPI D-PHY, to ensure that the following parameters meet the specification throughout silicon corners:

- LP transmitter output impedance - ZOLP
- LP output signalslew rate - $\partial V / \partial t_{SR}$
- HS differential input impedance - ZID
- HS single ended output impedance – ZOS

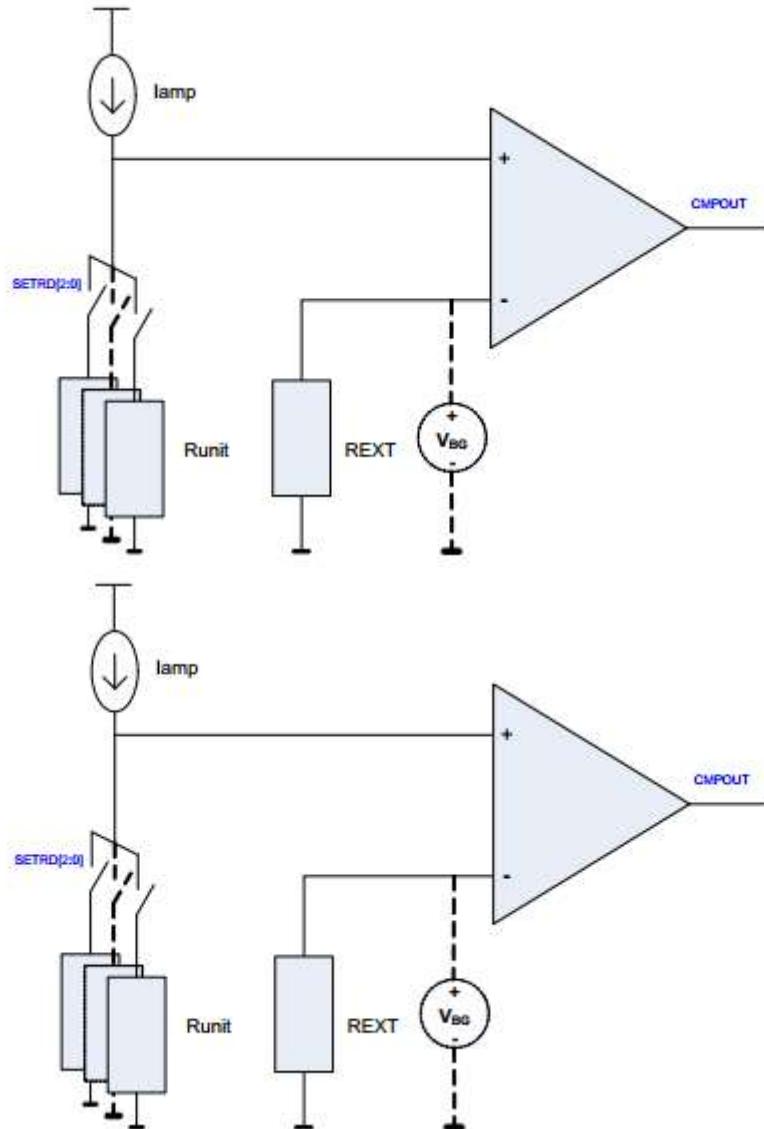
The calibration machine relies on an internal replica resistor that is matched to the external REXT high precision resistor. This is done by a set of switches, controlled by SETRD bus, that are progressively enabled and disabled resulting in an overall internal resistance value higher or lower than REXTscan mode. The results "higher than" and "lower than" are actually the output of internal OTA comparator.

After a complete sweep of all settings, the algorithm selects the optimum setting as the one that yields the internal resistor value closer to REXT. This setting is then used throughout the complete AFE for tuning of internal circuitry to compensate for process variation.

In case of an eventual calibration failure, the default settings of this calibration machine is sufficient to ensure proper functionality of all circuitry within the MIPI D-PHY, but fails some D-PHY performance parameters across PVT corner variation.

This procedure is performed at system start-up and is repeated for each power-up.

Fig. 12-10 Resistor Tuning Circuitry



As an alternative to the MIPI D-PHY internal calibration process, a software virtual calibration machine can be implemented outside MIPI D-PHY using the Procedure explained on.

12.5.2.2 Calibration Machine Algorithm

Software calibration machine should be implemented by controlling the input pin MIPIC_PHY_TST_CTRL_1[4:0] and observing the output pin MIPIC_PHY_TST_CTRL_1[7] of the control code 0x21 (Termination Resistor Control). The mapping is as follows:

- MIPIC_PHY_TST_CTRL_1[4:2] - SETRD: Internal termination resistor value control
 - MIPIC_PHY_TST_CTRL_1[1] - RTUNPON_EN: Termination resistor power override enable
 - MIPIC_PHY_TST_CTRL_1[0] - RTUNPON: Termination resistor power-on
 - MIPIC_PHY_TST_CTRL_1[15] - CMPOUT: Output of internal resistor comparator
- Every access to MIPIC_PHY_TST_CTRL_1[7:0] is followed by the corresponding rising edge in CSIHOST_PHY_TEST_CTRL0[1] while MIPIC_PHY_TST_CTRL_1[16] =0. This ensures that the MIPIC_PHY_TST_CTRL_1[7:0] contents are latched internally and applied to the relevant circuitry. These additional steps are not included in the description.

12.5.2.2.1 Procedure

Initial Conditions

1. Enter CONTROL CODE 0x21 as defined in Termination Resistor Control.
2. Set MIPIC_PHY_TST_CTRL_1[1] and MIPIC_PHY_TST_CTRL_1[0] to high and MIPIC_PHY_TST_CTRL_1[7:5] to 000 for the entire period of the calibration process.

Steps

1. Set MIPIC_PHY_TST_CTRL_1[4:2] to 000 and wait for 100 ns (settling time). Check MIPIC_PHY_TST_CTRL_1[15] and store the value as AUX_TRIPU. The value is expected to be 1 in typical cases.
2. Sweep MIPIC_PHY_TST_CTRL_1[4:2] from 001 to 111. Wait for 100 ns between every control word change.
3. Check MIPIC_PHY_TST_CTRL_1[15]. If MIPIC_PHY_TST_CTRL_1[15] is different from AUX_TRIPU, then set the following:
 - AUX_A = MIPIC_PHY_TST_CTRL_1[4:2]
 - AUX_TRIPU = MIPIC_PHY_TST_CTRL_1[15]
 It is possible that the output of the comparator MIPIC_PHY_TST_CTRL_1[15] does not change its value during this sweep depending on the process corner. In such a case, do the following:
 - If MIPIC_PHY_TST_CTRL_1[15] = 1 throughout the complete sweep, then set MIPIC_PHY_TST_CTRL_1[12:10] to 111.
 - If MIPIC_PHY_TST_CTRL_1[15] = 0 throughout the complete sweep, then set MIPIC_PHY_TST_CTRL_1[12:10] to 000.
4. Once MIPIC_PHY_TST_CTRL_1[4:2] = 111, check MIPIC_PHY_TST_CTRL_1[15] and store the value as AUX_TRIPD. It is not expected that MIPIC_PHY_TST_CTRL_1[15] toggles more than once during a sweep. If AUX_TRIPD ≠ AUX_TRIPU, then MIPIC_PHY_TST_CTRL_1[4:2] = 011. Flag an error.
5. Sweep MIPIC_PHY_TST_CTRL_1[4:2] from 110 down to 000. Wait for 100 ns between every control word change. Check MIPIC_PHY_TST_CTRL_1[15]. If MIPIC_PHY_TST_CTRL_1[15] is different from AUX_TRIPD, then set the following:
 - AUX_B = MIPIC_PHY_TST_CTRL_1[12:10]
 - AUX_TRIPD = MIPIC_PHY_TST_CTRL_1[15]
6. Set MIPIC_PHY_TST_CTRL_1 [4:2] to ROUND_MAX[(AUX_A+AUX_B)/2].

NOTE:

Observe MIPIC_PHY_TST_CTRL_1[12:10] to ensure that the optimum value found has effectively been programmed.

12.5.3 Registers Summary

Ref 8.4 Control/Test Codes of MIPI D-PHY Bidir 4L for GF28-nm SLP/1.8V Databook

12.5.4 Detail Register Description

Ref 8.4 Control/Test Codes of MIPI D-PHY Bidir 4L for GF28-nm SLP/1.8V Databook

12.5.5 Electrical and Timing Information

The following Tables provides the electrical and timing characteristics of MIPI D-PHY, the following conditions are applicable unless otherwise noted:

Vdd (core) = 1.0V

Vdd (I/O) = 1.8V

Ta° = T_{min} to T_{max}

Table 12-164 DC Specifications

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Input DC Specifications – Apply to CLKP/N and DATAP/N Inputs						

V_I	Input signal voltage range		-50		1350	mV
I_{LEAK}	Input leakage current	$V_{GNDH(\min)} \leq V_I \leq V_{GNDH(\max)}$ $+ V_{OH(\text{absmax})}$ Lane module in LP receive mode				uA
V_{GNDH}	Ground shift		-50		50	mV
$V_{OH(\text{absmax})}$	Maximum transient output voltage level		-0.15		1.45	V
$t_{VOH(\text{absmax})}$	Maximum transient time above $V_{OH(\text{absmax})}$				20	ns

HS Line Drivers DC Specifications

$ V_{OD} $	HS Transmit Differential output voltage magnitude	$80 \Omega \leq R_L \leq 125 \Omega$	140	200	270	mV
$\Delta V_{OD} $	Change in Differential output voltage magnitude between logic states	$80 \Omega \leq R_L \leq 125 \Omega$			14	mV
V_{CMTX}	Steady-state command-mode output voltage	$80 \Omega \leq R_L \leq 125 \Omega$	150	200	250	mV
$\Delta V_{CMTX(1,0)}$	Changes in steady-state common-mode output voltage between logic states	$80 \Omega \leq R_L \leq 125 \Omega$			5	mV
V_{OHS}	HS output high voltage	$80 \Omega \leq R_L \leq 125 \Omega$			360	mV
Z_{os}	Single-ended output impedance		40	50	62.5	Ω
ΔZ_{os}	Single-ended output impedance mismatch				10	%

LP Line Drivers DC Specifications

V_{OL}	Ouput Low-level SE voltage		-50		50	mV
V_{OH}	Ouput high-level SE voltage		1.1	1.2	1.3	V
Z_{OLP}	Single-ended output impedance		110			Ω
$\Delta Z_{OLP(01,10)}$	Single-ended ouput impedance mismatch driving opposite level				20	%
$\Delta Z_{OLP(00,11)}$	Single-ended ouput impedance mismatch driving same level				5	%

HS Line Receiver DC Specifications

V_{IDTH}	Differential input high voltage threshold				70	mV
V_{IDTL}	Differential input low voltage threshold		-70			mV

V_{IHHS}	Single ended input high voltage				460	mV
V_{ILHS}	Single ended input low voltage		-40			mV
V_{CMRXDC}	Input common mode voltage		70		330	mV
Z_{ID}	Differential input impedance		80		125	Ω

LP Line Receiver DC Specifications

V_{IL}	Input low voltage				550	mV
V_{IH}	Input high voltage		880			mV
V_{HYST}	Input hysteresis		25			mV

Contention Line Receiver DC Specifications

V_{ILF}	Input low fault threshold				200	mV
V_{IHF}	Input high fault threshold		450			mV

12.5.6 Switching Characteristics

This section provides the various specifications for the switching characteristics of MIPI D-PHY

Table 12-165 Switching Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Configuration Clock Specifications						
F_{CFG_CLK}	CFG_CLK frequency		17		27	MHz
DC_{CFG_CLK}	CFG_CLK duty cycle		40	50	60	%
HS Line Drivers AC Specifications						
-	Maximum Serial Data rate (forward direction)	On DATAP/N outputs. $80 \Omega \leq R_L \leq 125 \Omega$	80		1500	Mbps
F_{DDRCLK}	DDR CLK frequency	On CLKP/N outputs	40		750	MHz
P_{DDRCLK}	DDR CLK period	$80 \Omega \leq R_L \leq 125 \Omega$	1.3		25	ns
UI_{INST}	UI instantaneous				12.5	ns ^a
ΔUI	UI variation		-10%		10%	UI ^b
			-5%		5%	UI ^c
t_{CDC}	DDR CLK duty cycle	$t_{CDC} = t_{CPH}/P_{DDRCLK}$		50		%
t_{CPH}	DDR CLK high time			1		UI

t_{CPL}	DDR CLK low time			1		UI
-	DDR CLK/DATA Jittler ^d			75		ps pk-pk
$t_{SKEW[PN]}$	Intra-Pair (Pulse) skew			0.075		UI
$t_{SKEW[TX]}$	Data to Clock Skew		-0.15		0.15	UI ^e
			-0.20		0.20	UI ^f
$t_{SETUP[RX]}$	Data to Clock Receiver Setup time		0.15			UI ^g
			0.20			UI ^h
$t_{HOLD[RX]}$	Clock to Data Receiver Hold time		0.15			UI ^g
			0.20			UI ^h
t_r	Differential output signal rise time	20% to 80%, $R_L=50\Omega$			0.30	UI ⁱ
					0.35	UI ^j
			100			ps ^k
t_f	Differential output signal fall time	20% to 80%, $R_L=50\Omega$			0.30	UI ⁱ
					0.35	UI ^j
			100			ps ^k
$\Delta V_{CMTX(HF)}$	Common level variation above 450MHz	$80 \Omega \leq R_L \leq 125 \Omega$			15	mVrms
$\Delta V_{CMTX(LF)}$	Common level variation between 50MHz and 450MHz	$80 \Omega \leq R_L \leq 125 \Omega$			25	mVp

Table 12-166 AC Specifications

Symbol	Parameter	Condition	Min	Typ	Max	Unit
LP Line Drivers AC Specifications						
t_{rip} , t_{fip}	Single ended output rise/fall time	15% to 85%, $C_L < 70\text{pF}$			25	ns
t_{reot}		30% to 85%, $C_L < 70\text{pF}$			35	ns
$\partial V / \partial t_{SR}$	Signal slew rate ^l	15% to 85%, $C_L < 70\text{pF}$			150	mV/ns
C_L	Load capacitance		0		70	pF ^m
HS Line Receiver AC Specifications						
$\Delta V_{CMRX(HF)}$	Common mode interference beyond 450MHz				200	mVpp

$\Delta V_{CMRX(LF)}$	Common mode interference between 50MHz and 450MHz		-50		50	mVpp
C_{CM}	Common mode termination				60	pF ⁿ
LP Line Receiver AC Specifications						
e^{SPIKE}	Input pulse rejection				300	V.ps
T_{MIN}	Minimum pulse response		20			ns
V_{INT}	Pk-to-Pk interference voltage				300	mVpp
f_{INT}	Interference frequency		450			MHz
Model Parameters Used for Driver Load Switching Performance Evaluation						
C_{PAD}	Equivalent Single ended I/O PAD capacitance				1	pF
C_{PIN}	Equivalent Signal Ended Package + PCB capacitance				2	pF
L_s	Equivalent wire bond series inductance				1.5	nH
R_s	Equivalent wire bond series resistance				0.15	Ω
R_L	Load Resistance		80	100	125	Ω

Notes:

- a. This value corresponds to a minimum Mbps data rate.
- b. When $UI \geq 1\text{ns}$, within a single burst.
- c. When $UI < 1\text{ns}$, within a single burst.
- d. Jitter specification with clean clock at REFCLK input.
- e. Total silicon and package skew delay budget of $0.3 * UIINST$ when D-PHY is supporting maximum data rate = 1 Gbps.
- f. Total silicon and package skew delay budget of $0.4 * UIINST$ when D-PHY is supporting maximum data rate > 1 Gbps.
- g. Total setup and hold window for receiver of $0.3 * UIINST$ when D-PHY is supporting maximum data rate = 1 Gbps.
- h. Total setup and hold window for receiver of $0.4 * UIINST$ when D-PHY is supporting maximum data rate > 1 Gbps.
- i. Applicable when operating at HS bit rates $\leq 1\text{ Gbps}$ ($UI \geq 1\text{ ns}$).
- j. Applicable when operating at HS bit rates > 1 Gbps ($UI < 1\text{ ns}$).
- k. Applicable for all HS bit rates. However, to avoid excessive radiation, bit rates $\leq 1\text{ Gbps}$ ($UI \geq 1\text{ ns}$), should not use values below 150 ps.
- l. Measured as average across any 50 mV of the output signal transition.
- m. CLOAD includes the low-frequency equivalent transmission line capacitance. The capacitance of TX and RX are assumed to always be <10pF. The distributed line capacitance can be up to 50pF for a transmission line with 2ns delay.
- n. For higher bit rates a 14pF capacitor will be needed to meet the common-mode return loss specification.

Chapter 13 MIPI CSI Host Controller

13.1 Overview

The CSI-2 Host Controller implements the CSI-2 protocol on the host side. The CSI-2 link protocol specification is a part of communication protocols defined by MIPI Alliance standards intended for mobile system chip-to-chip communications. The CSI-2 specification is for the image application processor communication in cameras.

The CSI-2 Host Controller is designed to receive data from a CSI-2 compliant camera sensor. A D-PHY configured as a Slave acts as the physical layer.

The MIPI CSI-2 Host Controller supports the following features:

- Compliant with MIPI Alliance Specification for CSI-2, Version 1.01.00-9 November 2010
- Interface with MIPI D-PHY following PHY Protocol Interface, as defined in MIPI Alliance Specification for D-PHY, Version 1.1-7 November 2011
- Up to four D-PHY RX data lanes
- Dynamically configurable multi-lane merging
- Long and Short packet decoding
- Timing accurate signaling of Frame and Line synchronization packets
- Several Frame formats
 - General Frame or Digital Interlaced Video with or without accurate sync timing
 - Data Type (Packet or Frame Level) and Virtual Channel interleaving
- 32-bit Image Data Interface delivering data formatted as recommended in CSI-2 Specification
- All primary and secondary data formats
 - RGB, YUV, and RAW color space definitions
 - From 24-bit down to 6-bit per pixel
 - Generic or user-defined byte-based data types
- Error detection and correction
 - PHY level
 - Packet level
 - Line level
 - Frame level

13.2 Block Diagram

The following diagram shows the MIPI CSI-2 Host Controller architecture.

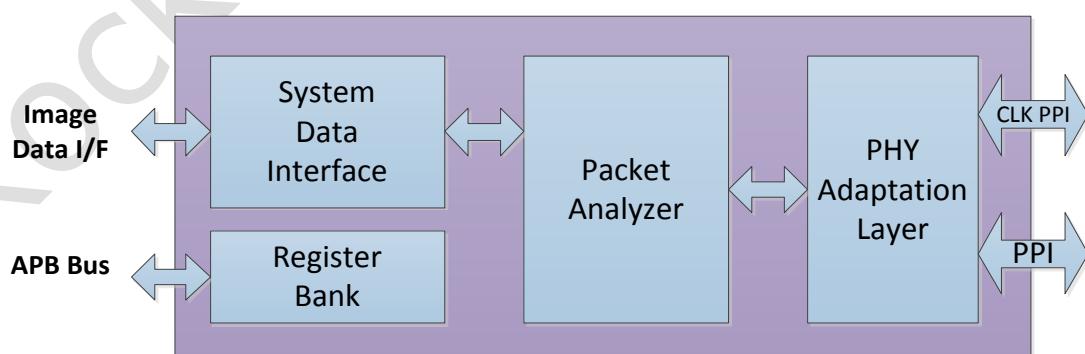


Fig. 13-1 MIPI CSI-2 Host Controller architecture

PHY Adaptation Layer: Manages the D-PHY PPI interface

Packet Analyzer: Merges the data from the different lanes

Image Data Interface: Reorders pixels into 32-bit data for memory storage and generates timing accurate video synchronization signals

AMBA-APB Register Bank: Provides access to configuration and control registers

13.3 Function Description

13.3.1 Supported Resolutions and Frame Rates

The CSI-2 specification does not define the supported standard resolutions or frame rates. Camera sensor resolution, blanking periods, synchronization events, frame rates, and pixel color depth play a fundamental role in the required bandwidth. All these variables make it difficult to define a standard procedure to estimate the minimum lane rate and the minimum number of lanes that support a specific CSI-2 device.

Table 10-1 presents some predefined and supported camera settings, assuming the following:

Clock lane frequency is 500 MHz or 750 MHz that results in a bandwidth of 1 Gbps or 1.5 Gbps respectively, for each data lane.

No significant control/reserved traffic is present on the link when pixel data is being transmitted.

The last column of Table 10-1 presents the minimum number of lanes required for each configuration.

Table 13-1 Supported Camera Settings

Mega Pixels	Mega Pixels with Overhead	Refresh Rate (Hz)	Color Depth (bpp)	CSI2 BW (Mbits)	D-PHY at 1 Gbps Number of Lanes	D-PHY at 1.5Gbps Number of Lanes
2MP	2560000	15	24	922	1	1
2MP	2560000	30	24	1843	2	2
3MP	3840000	15	16	922	1	1
3MP	3840000	30	16	1843	2	2
3MP	3840000	30	24	2765	3	2
5MP	6400000	15	16	1536	2	2
5MP	6400000	15	24	2304	3	2
5MP	6400000	30	16	3072	4	3
8MP	10240000	15	16	2458	3	2
8MP	10240000	15	24	3686	4	3
8MP	10240000	30	12	3686	4	3
12MP	15360000	15	12	2765	3	2
12MP	15360000	15	16	3686	4	3
14MP	17920000	15	12	3226	4	3
16MP	20480000	15	12	3686	4	3
Video Formats						
1280x720 pixels(720p)	921600	30	24	664	1	1
1280x720 pixels(720p)	921600	60	24	1327	2	1
1920x1080 pixels(1080p)	2073600	60	24	2986	3	2

13.3.2 Error Detection

The CSI-2 Host Controller analyzes the received packets and determines if there are protocol errors. It is possible to monitor the following errors:

Frame errors such as incorrect Frame sequence, reception of a CRC error in the most recent frame, and the mismatch between Frame Start and Frame End

Line errors such as incorrect line sequence and mismatch between Line Start and Line End

Packet errors such as ECC or CRC mismatch

D-PHY errors such as synchronization pattern mismatch

Table 37-2 shows all the errors that CSI-2 Host Controller can identify.

Table 13-2 Errors Identified by the CSI-2 Host Controller

Error	Description	Level	Action
phy_errsotsynchs_*	Start of transmission error on data lane* with no synchronization achieved	PHY	Packets with this error are not delivered in IDI interface

Error	Description	Level	Action
phy_erreesc_*	Escape entry error (ULPM) on data lane*	PHY	Informative only. Error is acknowledged in the register and the interrupt pin is raised.
phy_errsoths_*	Start of transmission error on data lane* but synchronization can still be achieved	PHY	Informative only since PHY can recover from this error. Error is acknowledged in register and the interrupt pin is raised.
vc*_err_crc	Checksum error detected on virtual channel*	Packet	Informative only. Error is acknowledged in the register and Interrupt pin is raised.
vc*_err_crc	Header ECC contains one error detected on virtual channel*	Packet	Informative only since controller can recover the correct header. Error is acknowledged in the register and the interrupt pin is raised.
err_ecc_double	Header ECC contains two errors. Unrecoverable.	Packet	Packets with this error are not delivered in IDI.s
err_id_vc*	Unrecognized or unimplemented data type detected in virtual channel*	Packet	Informative only. Error is acknowledged in the register and the interrupt pin is raised
err_f_bndry_match_vc*	Error matching Frame Start with Frame End for virtual channel*	Frame	Informative only. Error is acknowledged in register and the interrupt pin is raised if not masked.
err_f_seq_vc*	Incorrect Frame Sequence detected in virtual channel*	Frame	Informative only. Error is acknowledged in register and the interrupt pin is raised if not masked.
err_frame_data_vc*	Last received frame, in virtual channel*, had at least one CRC error	Frame	Informative only. Error is acknowledged in the register and the interrupt pin is raised.

13.4 Register Description

This section describes the control/status registers of the design.

13.4.1 Register Summary

Name	Offset	Size	Reset Value	Description
CSIHOST_VERSION	0x0000	W	0x00000000	Version of the CSI2 Host
CSIHOST_N_LANES	0x0004	W	0x00000001	Number of active data lanes
CSIHOST_PHY_SHUTDOWNZ	0x0008	W	0x00000000	PHY shutdown control
CSIHOST_DPHY_RSTZ	0x000c	W	0x00000000	DPHY reset control
CSIHOST_CSI2_RESETN	0x0010	W	0x00000000	CSI-2 Controller reset
CSIHOST_PHY_STATE	0x0014	W	0x00000000	General settings for all blocks
CSIHOST_ERR1	0x0020	W	0x00000000	Error state register 1
CSIHOST_ERR2	0x0024	W	0x00000000	Error state register 2
CSIHOST_MSK1	0x0028	W	0x00000000	Masks for errors 1
CSIHOST_MSK2	0x002c	W	0x00000000	Masks for errors 2
CSIHOST_PHY_TEST_CTRL0	0x0030	W	0x00000000	D-PHY test interface control 0
CSIHOST_PHY_TEST_CTRL1	0x0034	W	0x00000000	D-PHY test interface control 1

Notes: **S**-Size: **B**- Byte (8 bits) access, **H****W**- Half WORD (16 bits) access, **W**-WORD (32 bits) access

13.4.2 Detail Register Description

CSIHOST_VERSION

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	VERSION Version of the mipi csi2 host

CSIHOST_N_LANES

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1:0	RW	0x1	N_LANES Number of active data lanes 00: 1 data lane (lane 0) 01: 2 data lanes (lanes 0 and 1) 10: 3 data lanes (lanes 0, 1, and 2) 11: 4 data lanes (All) Can only be updated when the D-PHY lane is in Stop state.

CSIHOST_PHY_SHUTDOWNZ

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	PHY_SHUTDOWNZ D-PHY shutdown input. active low

CSIHOST_DPHY_RSTZ

Address: Operational Base + offset (0x000c)

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	DPHY_RSTZ D-PHY reset output. active low

CSIHOST_CSII_RESETN

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	CSI2_RESETN CSI-2 controller reset output. active low

CSIHOST_PHY_STATE

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:11	RO	0x0	reserved
10	RO	0x0	PHY_STOPSTATECLK Clock lane in stop state
9	RO	0x0	PHY_RXULPSCLKNOT This signal indicates that the clock lane module has entered the Ultra Low Power state, active low
8	RO	0x0	PHY_RXCLKACTIVEHS Indicates that the clock lane is actively receiving a DDR clock
7	RO	0x0	PHY_STOPSTATEDATA_3 Data lane 3 in stop state

Bit	Attr	Reset Value	Description
6	RO	0x0	PHY_STOPSTATEDATA_2 Data lane 2 in stop state
5	RO	0x0	PHY_STOPSTATEDATA_1 Data lane 1 in stop state
4	RO	0x0	PHY_STOPSTATEDATA_0 Data lane 0 in stop state
3	RO	0x0	PHY_RXULPSESC_3 lane module 3 has entered the Ultra Low Power mode
2	RO	0x0	PHY_RXULPSESC_2 lane module 2 has entered the Ultra Low Power mode
1	RO	0x0	PHY_RXULPSESC_1 lane module 1 has entered the Ultra Low Power mode
0	RO	0x0	PHY_RXULPSESC_0 lane module 0 has entered the Ultra Low Power mode

CSIHOST_ERR1

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28	RO	0x0	err_ecc_double Header ECC contains 2 errors, unrecoverable
27	RO	0x0	vc3_err_crc Checksum error detected on virtual channel 3
26	RO	0x0	vc2_err_crc Checksum error detected on virtual channel 2
25	RO	0x0	vc1_err_crc Checksum error detected on virtual channel 1
24	RO	0x0	vc0_err_crc Checksum error detected on virtual channel 0
23	RO	0x0	err_l_seq_di3 Error in the sequence of lines for vc3 and dt3
22	RO	0x0	err_l_seq_di2 Error in the sequence of lines for vc2 and dt2
21	RO	0x0	err_l_seq_di1 Error in the sequence of lines for vc1 and dt1
20	RO	0x0	err_l_seq_di0 Error in the sequence of lines for vc0 and dt0
19	RO	0x0	err_l_bndry_match_di3 Error matching line start with line end for vc3 and dt3

Bit	Attr	Reset Value	Description
18	RO	0x0	err_l_bndry_match_di2 Error matching line start with line end for vc2 and dt2
17	RO	0x0	err_l_bndry_match_di1 Error matching line start with line end for vc1 and dt1
16	RO	0x0	err_l_bndry_match_di0 Error matching line start with line end for vc0 and dt0
15	RO	0x0	err_frame_data_vc3 Last received frame, in virtual channel 3, had at least one CRC error
14	RO	0x0	err_frame_data_vc2 Last received frame, in virtual channel 2 had at least one CRC error
13	RO	0x0	err_frame_data_vc1 Last received frame, in virtual channel 1, had at least one CRC error
12	RO	0x0	err_frame_data_vc0 Last received frame, in virtual channel 0, had at least one CRC error
11	RO	0x0	err_f_seq_vc3 Error in the sequence of lines for vc3 and dt3
10	RO	0x0	err_f_seq_vc2 Error in the sequence of lines for vc2 and dt2
9	RO	0x0	err_f_seq_vc1 Error in the sequence of lines for vc1 and dt1
8	RO	0x0	err_f_seq_vc0 Error in the sequence of lines for vc0 and dt0
7	RO	0x0	err_f_bndry_match_vc3 Error matching frame start with frame end for virtual channel 3
6	RO	0x0	err_f_bndry_match_vc2 Error matching frame start with frame end for virtual channel 2
5	RO	0x0	err_f_bndry_match_vc1 Error matching frame start with frame end for virtual channel 1
4	RO	0x0	err_f_bndry_match_vc0 Error matching frame start with frame end for virtual channel 0
3	RO	0x0	phy_errsotsynchs_3 Start of transmission error on data lane 3(no synchronization achieved)

Bit	Attr	Reset Value	Description
2	RO	0x0	phy_errsotsynchs_2 Start of transmission error on data lane 2 (no synchronization achieved)
1	RO	0x0	phy_errsotsynchs_1 Start of transmission error on data lane 1 (no synchronization achieved)
0	RO	0x0	phy_errsotsynchs_0 Start of transmission error on data lane 0 (no synchronization achieved)

CSIHOST_ERR2

Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23	RO	0x0	err_l_seq_di7 Error in the sequence of lines for vc7 and dt7
22	RO	0x0	err_l_seq_di6 Error in the sequence of lines for vc6 and dt6
21	RO	0x0	err_l_seq_di5 Error in the sequence of lines for vc5 and dt5
20	RO	0x0	err_l_seq_di4 Error in the sequence of lines for vc4 and dt4
19	RO	0x0	err_l_bndry_match_di7 Error matching line start with line end for vc7 and dt7
18	RO	0x0	err_l_bndry_match_di6 Error matching line start with line end for vc6 and dt6
17	RO	0x0	err_l_bndry_match_di5 Error matching line start with line end for vc5 and dt5
16	RO	0x0	err_l_bndry_match_di4 Error matching line start with line end for vc4 and dt4
15	RO	0x0	err_id_vc3 Unrecognized or unimplemented data type detected in virtual channel 3
14	RO	0x0	err_id_vc2 Unrecognized or unimplemented data type detected in virtual channel 2
13	RO	0x0	err_id_vc1 Unrecognized or unimplemented data type detected in virtual channel 1

Bit	Attr	Reset Value	Description
12	RO	0x0	err_id_vc0 Unrecognized or unimplemented data type detected in virtual channel 0
11	RO	0x0	vc3_err_ecc_corrected Header error detected and corrected on virtual channel 3
10	RO	0x0	vc2_err_ecc_corrected Header error detected and corrected on virtual channel 2
9	RO	0x0	vc1_err_ecc_corrected Header error detected and corrected on virtual channel 1
8	RO	0x0	vc0_err_ecc_corrected Header error detected and corrected on virtual channel 0
7	RO	0x0	phy_errsoths_3 Start of transmission error on data lane 3 (synchronization can still be achieved)
6	RO	0x0	phy_errsoths_2 Start of transmission error on data lane 2 (synchronization can still be achieved)
5	RO	0x0	phy_errsoths_1 Start of transmission error on data lane 1 (synchronization can still be achieved)
4	RO	0x0	phy_errsoths_0 Start of transmission error on data lane 0 (synchronization can still be achieved)
3	RO	0x0	phy_erresc_3 Escape entry error (ULPM) on data lane 3
2	RO	0x0	phy_erresc_2 Escape entry error (ULPM) on data lane 2
1	RO	0x0	phy_erresc_1 Escape entry error (ULPM) on data lane 1
0	RO	0x0	phy_erresc_0 Escape entry error (ULPM) on data lane 0

CSIHOST_MSK1

Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28	RW	0x0	mask_err_ecc_double Mask for err_ecc_double
27	RW	0x0	mask_vc3_err_crc Mask for vc3_err_crc

Bit	Attr	Reset Value	Description
26	RW	0x0	mask_vc2_err_crc Mask for vc2_err_crc
25	RW	0x0	mask_vc1_err_crc Mask for vc1_err_crc
24	RW	0x0	mask_vc0_err_crc Mask for vc0_err_crc
23	RW	0x0	mask_err_l_seq_di3 Mask for err_l_seq_di3
22	RW	0x0	mask_err_l_seq_di2 Mask for err_l_seq_di2
21	RW	0x0	mask_err_l_seq_di1 Mask for err_l_seq_di1
20	RW	0x0	mask_err_l_seq_di0 Mask for err_l_seq_di0
19	RW	0x0	mask_err_l_bndry_match_di3 Mask for err_l_bndry_match_di3
18	RW	0x0	mask_err_l_bndry_match_di2 Mask for err_l_bndry_match_di2
17	RW	0x0	mask_err_l_bndry_match_di1 Mask for err_l_bndry_match_di1
16	RW	0x0	mask_err_l_bndry_match_di0 Mask for err_l_bndry_match_di0
15	RW	0x0	mask_err_frame_data_vc3 Mask for err_frame_data_vc3
14	RW	0x0	mask_err_frame_data_vc2 Mask for err_frame_data_vc2
13	RW	0x0	mask_err_frame_data_vc1 Mask for err_frame_data_vc1
12	RW	0x0	mask_err_frame_data_vc0 Mask for err_frame_data_vc0
11	RW	0x0	mask_err_f_seq_vc3 Mask for err_f_seq_vc3
10	RW	0x0	mask_err_f_seq_vc2 Mask for err_f_seq_vc2
9	RW	0x0	mask_err_f_seq_vc1 Mask for err_f_seq_vc1
8	RW	0x0	mask_err_f_seq_vc0 Mask for err_f_seq_vc0
7	RW	0x0	mask_err_f_bndry_match_vc3 Mask for err_f_bndry_match_vc1
6	RW	0x0	mask_err_f_bndry_match_vc2 Mask for err_f_bndry_match_vc1
5	RW	0x0	mask_err_f_bndry_match_vc1 Mask for err_f_bndry_match_vc1

Bit	Attr	Reset Value	Description
4	RW	0x0	mask_err_f_bndry_match_vc0 Mask for err_f_bndry_match_vc0
3	RW	0x0	mask_phy_errsotsynchs_3 Mask for phy_errsotsynchs_3
2	RW	0x0	mask_phy_errsotsynchs_2 Mask for phy_errsotsynchs_2
1	RW	0x0	mask_phy_errsotsynchs_1 Mask for phy_errsotsynchs_1
0	RW	0x0	mask_phy_errsotsynchs_0 Mask for phy_errsotsynchs_0

CSIHOST_MSK2

Address: Operational Base + offset (0x002c)

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23	RO	0x0	err_l_seq_di7 Error in the sequence of lines for vc7 and dt7
22	RO	0x0	err_l_seq_di6 Error in the sequence of lines for vc6 and dt6
21	RO	0x0	err_l_seq_di5 Error in the sequence of lines for vc5 and dt5
20	RO	0x0	err_l_seq_di4 Error in the sequence of lines for vc4 and dt4
19	RO	0x0	err_l_bndry_match_di7 Error matching line start with line end for vc7 and dt7
18	RO	0x0	err_l_bndry_match_di6 Error matching line start with line end for vc6 and dt6
17	RO	0x0	err_l_bndry_match_di5 Error matching line start with line end for vc5 and dt5
16	RO	0x0	err_l_bndry_match_di4 Error matching line start with line end for vc4 and dt4
15	RO	0x0	err_id_vc3 Unrecognized or unimplemented data type detected in virtual channel 3
14	RO	0x0	err_id_vc2 Unrecognized or unimplemented data type detected in virtual channel 2
13	RO	0x0	err_id_vc1 Unrecognized or unimplemented data type detected in virtual channel 1

Bit	Attr	Reset Value	Description
12	RO	0x0	err_id_vc0 Unrecognized or unimplemented data type detected in virtual channel 0
11	RO	0x0	vc3_err_ecc_corrected Header error detected and corrected on virtual channel 3
10	RO	0x0	vc2_err_ecc_corrected Header error detected and corrected on virtual channel 2
9	RO	0x0	vc1_err_ecc_corrected Header error detected and corrected on virtual channel 1
8	RO	0x0	vc0_err_ecc_corrected Header error detected and corrected on virtual channel 0
7	RO	0x0	phy_errsoths_3 Start of transmission error on data lane 3 (synchronization can still be achieved)
6	RO	0x0	phy_errsoths_2 Start of transmission error on data lane 2 (synchronization can still be achieved)
5	RO	0x0	phy_errsoths_1 Start of transmission error on data lane 1 (synchronization can still be achieved)
4	RO	0x0	phy_errsoths_0 Start of transmission error on data lane 0 (synchronization can still be achieved)
3	RW	0x0	mask_phy_erresc_3 Mask for phy_erresc_3
2	RW	0x0	mask_phy_erresc_2 Mask for phy_erresc_2
1	RW	0x0	mask_phy_erresc_1 Mask for phy_erresc_1
0	RW	0x0	mask_phy_erresc_0 Mask for phy_erresc_0

CSIHOST_PHY_TEST_CTRLO

Address: Operational Base + offset (0x0030)

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	RW	0x0	phy_testclk D-PHY test interface strobe signal It is used to clock TESTDIN bus into the D-PHY. In conjunction with TESTEN signal controls controls the operation selection

Bit	Attr	Reset Value	Description
0	RW	0x0	phy_testclr D-PHY test interface clear It is used when active performs vendor specific interface initialization (active high)

CSIHOST_PHY_TEST_CTRL1

Address: Operational Base + offset (0x0034)

Bit	Attr	Reset Value	Description
31:17	RO	0x0	reserved
16	RW	0x0	phy_testen D-PHY test interface operation selector: 1: configures address write operation on the falling edge of TESTCLK 0: configures a data write operation on the rising edge of TESTCLK
15:8	RO	0x00	phy_testdout D-PHY output 8-bit data bus for read-back and internal probing functionalities
7:0	RW	0x00	phy_testdin D-PHY test interface input 8-bit data bus for internal register programming and test functionlities access

Chapter 14 MIPI DSI Host Controller

14.1 Overview

The Display Serial Interface (DSI) is part of a group of communication protocols defined by the MIPI Alliance. The MIPI Controller is a digital core that implements all protocol functions defined in the MIPI DSI Specification. The MIPI Controller provides an interface between the system and the MIPI D-PHY, allowing the communication with a DSI-compliant display. The MIPI Controller supports one to four lanes for data transmission with MIPI D-PHY.

The MIPI Controller supports the following features:

- Compliant with MIPI Alliance standards
- Support the DPI interface color coding mappings into 24-bit Interface
 - 16 bits per pixel, configurations 1,2, and 3
 - 18 bits per pixel, configurations 1 and 2
 - 24 bits per pixel
- Programmable polarity of all DPI interface signals
- Extended resolutions beyond the DPI standard maximum resolution of 800x480 pixels:
 - Up to 2047 vertical active lines
 - Up to 63 vertical back porch lines
 - Up to 63 vertical front porch lines
 - Maximum resolution is limited by available DSI Physical link bandwidth which depends on the number of lanes and maximum speed per lane
- All commands defined in MIPI Alliance Specification for Display Command Set (DCS)
- Interface with MIPI D-PHY following PHY Protocol Interface (PPI), as defined in MIPI Alliance Specification for D-PHY
- Up to four D-PHY Data Lanes
- Bidirectional communication and escape mode support through data lane 0
- Transmission of all generic commands
- ECC and Checksum capabilities
- End of Transmission Packet(EOTP)
- Ultra Low-Power mode
- Fault recovery schemes

14.2 Block Diagram

The following diagram shows the MIPI Controller architecture.

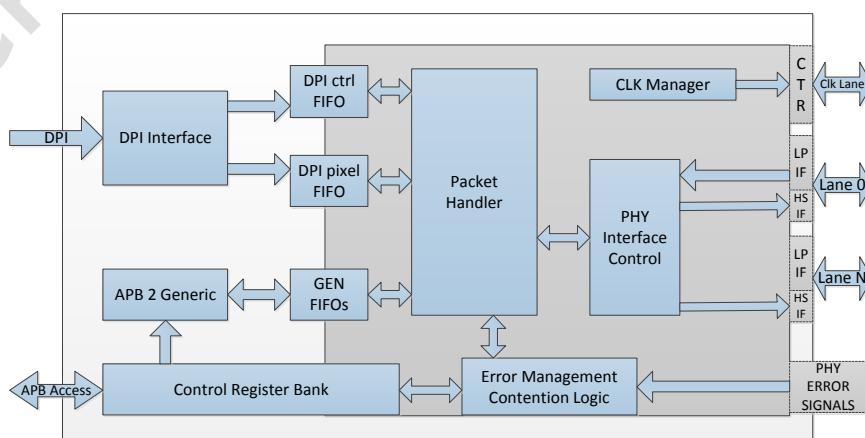


Fig. 14-1 MIPI Controller architecture

The DPI interface captures the data and control signals and conveys them to a FIFO for video control signals and another one for pixel data. This data is then used to build Video packets,

hen in Video mode.

The Register Bank is accessible through a standard AMBA-APB slave interface, providing access to the MIPI Controller registers for configuration and control. There is also a fully programmable interrupt generator to inform the system about certain events.

The PHY Interface Control is responsible for managing the D-PHY PPI interface. It acknowledges the current operation and enables low-power transmission/reception or a high-speed transmission. It also performs data splitting between available D-PHY lanes for high-speed transmission.

The Packet Handler schedules the activities inside the link. It performs several functions based on the interfaces that are currently DPI and the video transmission mode that is used (burst mode or non-burst mode with sync pulse or sync events). It builds long or short packet generating correspondent ECC and CRC codes. This block also performs the following functions: Packet reception, Validation of packet header by checking the ECC, Header correction and notification for single-bit errors, Termination of reception, Multiple header error notification.

The APB-to-Generic block bridges the APB operations into FIFOs holding the Generic commands. The block interfaces with the following FIFOs: Command FIFO, Write payload FIFO, Read payload FIFO.

The Error Management notifies and monitors the error conditions on the DSI link. It controls the timers used to determine if a timeout condition occurred, performing an internal soft reset and triggering an interruption notification.

14.3 Function Description

14.3.1 DPI interface function

The DPI interface follows the MIPI DPI specification with pixel data bus width up to 24 bits. It is used to transmit the information in Video mode in which the transfers from the host processor to the peripheral take the form of a real-time pixel stream. This interface allows sending ShutDown (SD) and ColorMode (CM) commands, which are triggered directly by writing to the register of CFG_MISC_CON[2:1]. To transfer additional commands(for example, to initialize the display), use another interface such as APB Slave Generic Interface to complement the DPI interface.

The DPI interface captures the data and control signals and conveys them to the FIFO interfaces that transmit them to the DSI link. Two different streams of data are presented at the interface; video control signals and pixel data. Depending on the interface color coding, the pixel data is disposed differently throughout the dpipixdata bus. The following table shows the Interface pixel color coding.

Table 14-1 Color table

Signal Line	16-bit			18-bit		24-bit
	Config1	Config2	Config3	Config1	Config2	
dipiidata23	Not used	R7				
dipiidata22	Not used	R6				
dipiidata21	Not used	Not used	R4	Not used	R5	R5
dipiidata20	Not used	R4	R3	Not used	R4	R4
dipiidata19	Not used	R3	R2	Not used	R3	R3
dipiidata18	Not used	R2	R1	Not used	R2	R2
dipiidata17	Not used	R1	R0	R5	R1	R1
dipiidata16	Not used	R0	Not used	R4	R0	R0
dipiidata15	R4	Not used	Not used	R3	Not used	G7
dipiidata14	R3	Not used	Not used	R2	Not used	G6
dipiidata13	R2	G5	G5	R1	G5	G5
dipiidata12	R1	G4	G4	R0	G4	G4
dipiidata11	R0	G3	G3	G5	G3	G3
dipiidata10	G5	G2	G2	G4	G2	G2
dipiidata9	G4	G1	G1	G3	G1	G1
dipiidata8	G3	G0	G0	G2	G0	G0
dipiidata7	G2	Not used	Not used	G1	Not used	B7
dipiidata6	G1	Not used	Not used	G0	Not used	B6
dipiidata5	G0	Not used	B5	B5	B5	B5
dipiidata4	B4	B4	B4	B4	B4	B4
dipiidata3	B3	B3	B3	B3	B3	B3
dipiidata2	B2	B2	B2	B2	B2	B2
dipiidata1	B1	B1	B1	B1	B1	B1
dipiidata0	B0	B0	Not used	B0	B0	B0

The DPI interface can be configured to increase flexibility and promote correct usage of this interface for several systems. These configuration options are as follows:

- Polarity control: All the control signals are programmable to change the polarity depending on system requirements.

After the MIPI Controller reset, DPI waits for the first VSYNC active transition to start signal sampling, including pixel data, and preventing image transmission in the middle of a frame. If interface pixel color coding is 18 bits and the 18-bit loosely packed stream is disabled, the number of lines programmed in the pixels per lines configuration is a multiple of four. This means that in this mode, the two LSBs in the configuration are always inferred as zero. The specification states that in this mode, the pixel line size should be a multiple of four.

14.3.2 APB Slave Generic Interface

The APB Slave interface allows the transmission of generic information in Command mode, and follows the proprietary register interface. Commands sent through this interface are not constrained to comply with the DCS specification, and can include generic commands described in the DSI specification as manufacturer-specific.

The MIPI Controller supports the transmission or write and read command mode packets as described in the DSI specification. These packets are built using the APB register access. The GEN_PLD_DATA register has two distinct functions based on the operation. Writing to this register sends the data as payload when sending a Command mode packet. Reading this register returns the payload of a read back operation. The GEN_HDR register contains the Command mode packet header type and header data. Writing to this register triggers the transmission of the packet implying that for a long Command mode packet, the packet's payload needs to be written in advance in the GEN_PLD_DATA register.

The valid packets available to be transmitted through the Generic interface are as follows:

- Generic Write Short Packet 0 Parameters
- Generic Write Short Packet 1 Parameters
- Generic Write Short Packet 2 Parameter

Generic Write Short Packet 0 Parameter
 Generic Write Short Packet 1 Parameters
 Generic Write Short Packet 2 Parameter
 Maximum Read Packet Configuration
 Generic Long Write Packet
 DCS Write Short Packet 0 Parameter
 DCS Write Short Packet 1 Parameter
 DCS Write Short Packet 0 Parameter
 DCS Write Long Packet

A set of bits in the CMD_PKT_STATUS register report the status of the FIFOs associated with APB interface support.

Generic interface packets are always transported using one of the DSI transmission modes; Video mode or Command mode. If neither of these mode are selected, the packets are not transmitted through the link and the released FIFOs eventually get overflowed.

The transfer of packets through the APB bus is based on the following conditions:

The APB protocol defines that the write and read procedure takes two clock cycles each to be executed. This means that the maximum input data rate through the APB interfaces is always half the speed of the APB clock.

The data input bus has a maximum width of 32 bits. This allows for a relation to be defined between the input APB clock frequency and maximum bi rate achievable by the APB interface.

The DSI link bit rate when using solely APB is equal to (APB clock frequency) *16 Mbps.

The bandwidth is dependent on the APB clock frequency; the available bandwidth increases with the clock frequency.

To drive the APB interface to achieve high bandwidth Command mode traffic transported by the DSI link, the MIPI Controller should operate in the Command mode only and the APB interface should be the only data source that is currently in use. Thus, the APB interface has the entire bandwidth of the DSI link and does not share it with any another input interface source.

The memory write commands require maximum throughout from the APB interface, because they contain the most amount of data conveyed by the DSI link. While writing the packet information, first write the payload of a given packet into the payload FIFO using the GEN_PLD_DATA register. When the payload data is for the command parameters, place the first byte to be transmitted in the least significant byte position of the APB data bus.

After writing the payload, write the packet header into the command FIFO. For more information and it should follow the pixel to byte conversion organization referred in the Annexure A of the DCS specification. The follow figures show how the pixel data should be organized in the APB data write bus. The memory write commands are conveyed in DCS long packets. DCS long packets are encapsulated in a DSI packet. The DSI included in the diagrams. In the follow figures, the Write Memory Command can be replaced by the DCS command Write Memory Start and Write Memory Continue.

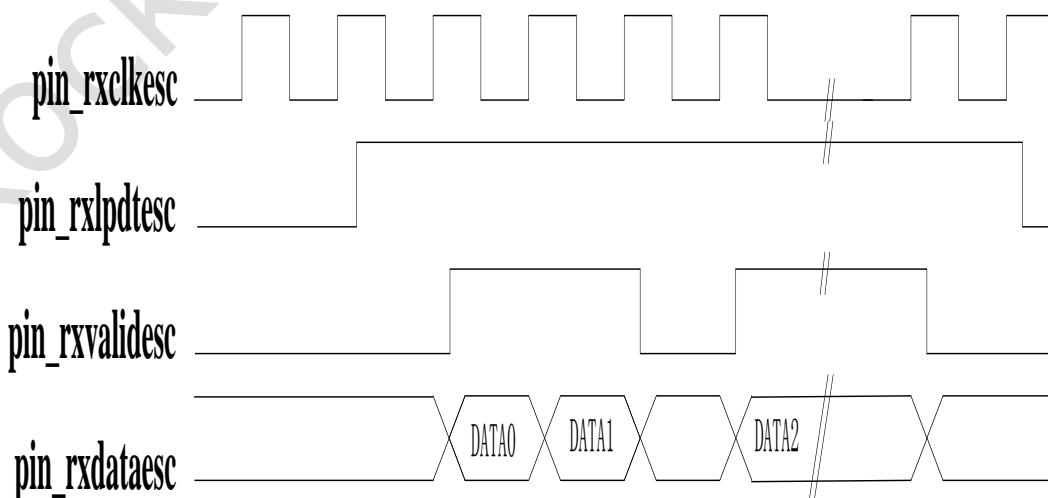


Fig. 14-2 24bpp APB Pixel to Byte Organization

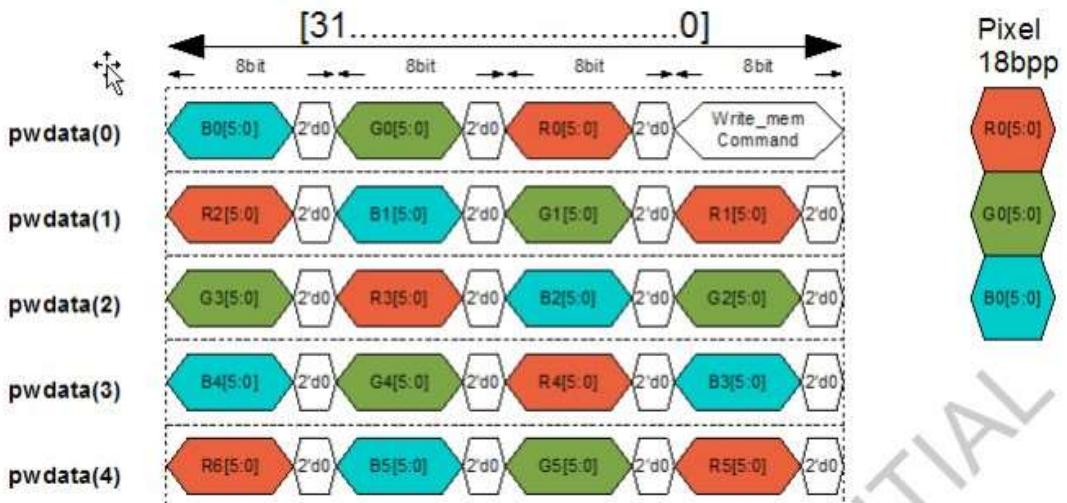


Fig. 14-3 18 bpp APB Pixel to Byte Organization

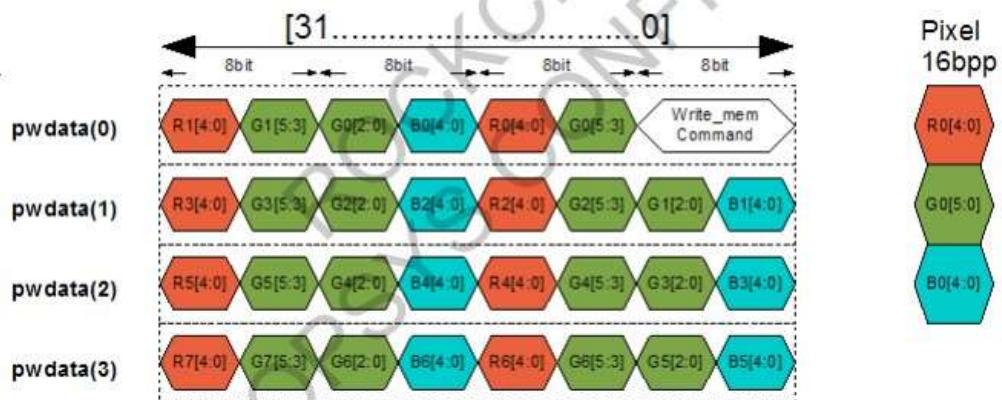


Fig. 14-4 16 bpp APB Pixel to Byte Organization

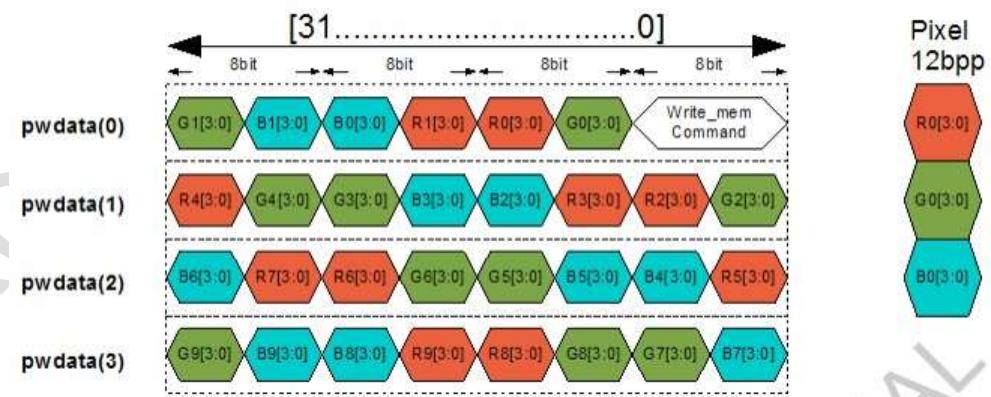


Fig. 14-5 12 bpp APB Pixel to Byte Organization

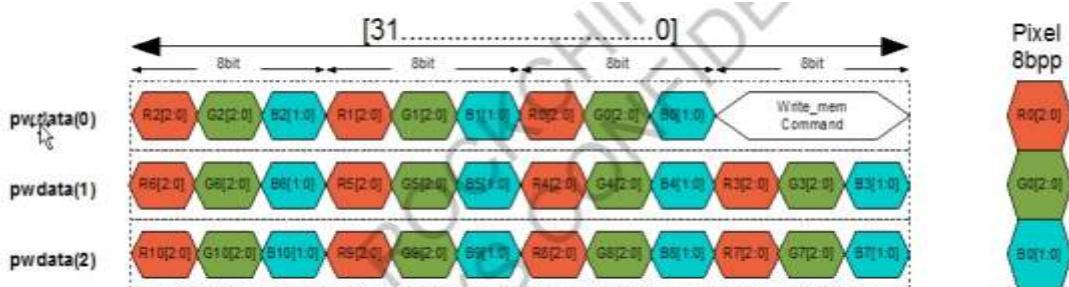


Fig. 14-6 8bpp APB Pixel to Byte Organization

14.3.3 Transmission of Commands in Video Mode

The MIPI Controller supports the transmission of commands, both in high-speed and low-power, while in Video mode. The DSI controller uses Blanking or Low-Power(BLLP) periods to transmit commands inserted through the APB Generic interface. Those periods correspond to the shaded areas of the following figure.

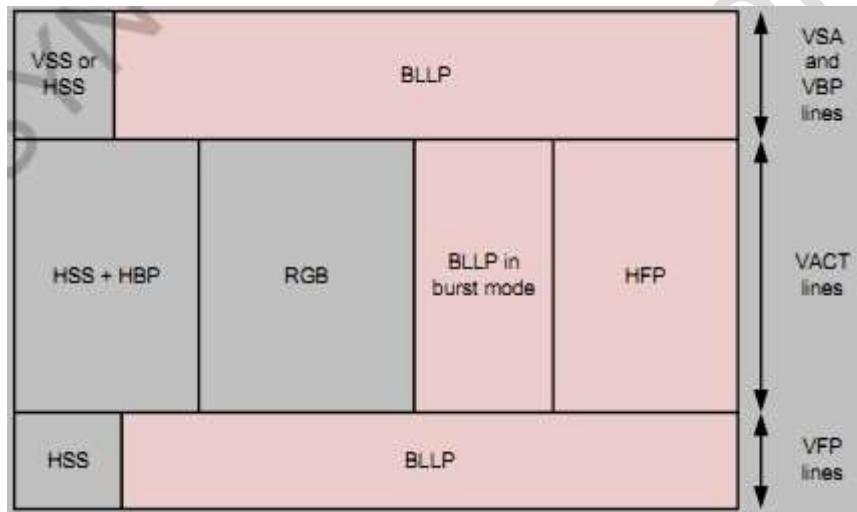


Fig. 14-7 Command Transmission Periods within the Image Area

Commands are transmitted in the blanking periods after the following packet/states:

- Vertical Sync Start (VSS) packets, if the Video Sync pulses are not enabled
- Horizontal Sync End (HSE) packets, in the VSA, VBP, and VFP regions
- Horizontal Sync Start (HSS) packets, if the Video Sync pulses are not enabled in the VSA, VBP, and VFP regions
- Horizontal Active (HACT) state

Only one command is transmitted per line, even in the case of the last line of a frame but one command is possible for each line.

The MIPI Controller avoids sending commands in the last line because it is possible that the last line is shorter than the other ones. For instance, the line time (t_L) could be half a cycle longer than the t_L on the DPI interface, that is, each line in the frame taking half a cycle from time for the last line. This results in the last line being $(1/2 \text{ cycle}) * (\text{number of lines} - 1)$ shorter than t_L . The dpicolorm and dpishutdn input signals are also able to trigger the sending of command packets. The commands are DSI data types Color Mode On, Color Mode Off, Shut Down Peripheral, and Turn on Peripheral. These commands are not sent in the VACT region. If the lpcmden bit of the VID_MODE_CFG register is 1, these commands are sent in LP mode. In LP mode, the ouvact_lpcmd_time field of the LP_CMD_TIM register is used to determine if these commands can be transmitted. It is assumed that outvact_lpcmd_time is greater than or equal to 4 bytes (number of bytes in a short packet), because the DWC_mipi_dsi_host does not transmit these commands on the last line.

If the frame_BTA_ack field is set in the VID_MODE_CFG register, a BTA is generated by DWC_mipi_dsi_host after the last line of a frame. This may coincide with a write command or a read command. In either case, the edpihalt signal is held asserted until an acknowledge has been received (control of the DSI bus is returned to the host).

If the lpcmden bit of the VID_MODE_CFG register is set to 1, the commands are sent in low-power in Video mode. In this case, it is necessary to calculate the time available, in bytes, to transmit a command in LP mode for Horizontal Front Porch (HFP), Vertical Sync Active (VSA), Vertical Back Porch (VBP), and Vertical Front Porch(VFP) regions.

The outvact_lpcmd_time field of the LP_CMD_TIM register indicates the time available (in bytes) to transmit a command in LP mode, based on the escape clock, on a line during the VSA, VBP, and the VFP

$$\text{Outvact_lpcmd_time} = (\text{tL} - (\text{Time to transmit HSS and HSE frames} + \text{tHSA} + \text{Time to enter and leave LP mode} + \text{Time to send the D-PHY LPDT command})) / \text{escape clock period} / 8 / 2$$

Where,

tL =Line time

tHSA =Time to send a short packet (for sync events) or time of the HAS pulse (for sync pulses)

In the above equation, division by eight is done to convert the time available to bytes and division by two is done because one bit is transmitted once in every two escape clock cycles.

The outvact_lpcmd_time filed can be compared directly with the size of the command to be transmitted to determine if there is enough time to transmit the command. The maximum size of a command that can be transmitted in LP mode is limited to 255 bytes by this field. This register must be programmed to a value greater than or equal to 4 bytes for the transmission of the DCTRL commands such as shutdown and colorm in LP mode.

Consider an example with $12.6\ \mu\text{s}$ per line and assume an escape clock frequency of 15 MHz. In this case, 189 escape clock cycles are available to enter and exit LP mode and transmit command. The following are assumed:

Sync pulses are not being transmitted

Two lane byte clock ticks are required to transmit a short packet

```
phy_lp2hs_time=16
phy_lp2p_time=20
```

In this example, a 11-byte command can be transmitted as follows:

$$\text{outvact_lpcmd_time} = (12.6\ \mu\text{s} - (2*10\ \text{ns}) - (16*10\ \text{ns}) - (20*10\ \text{ns}) - (8*66\ \text{ns})) / 66\ \text{ns} / 8 / 2 = 11\ \text{bytes}$$

The invact_lpcmd_time field of the LP_CMD_TIM register indicates the time available (in bytes) to transmite a command in LP mode (based on the escape clock) in the Vertical Active (VACT) region. This time is calculated as follows:

$$\text{Invact_lpcmd_time} = ((\text{tHFP}-\text{Time to enter and leave low-power mode} + \text{Blanking period before the HFP when in Burst mode} - \text{Time to send the D-PHY LPDT command}) / \text{escape clock period}) / 8$$

Where,

tHFP =line time-tHSA-tHBP-tHACT

tHACT =vid_pkt_size*bits_per_pixel*lane_byte_clock_period / num_lanes

The invact_lpcmd_time field can be compared directly with the size of the command to be transmitted to determined if there is time to transmit the command.

Consider an example where the refresh rate is 60 Hz. The number of lines is 1320 (typical). The tL in this case is $12.6\ \mu\text{s}$. With a lane byte clock of 100 MHz, 1260 clock ticks are availabel to transmit a single frame. If 800 ticks are used for pixel data then 460 ticks ($4.6\ \mu\text{s}$) are available for Horizontal Sync Start (HSS), HFP, and HBP. Assuming that $2.3\ \mu\text{s}$ is available for HFP and the escape clock is 15MHz, only 34 LP clock ticks are available to enter LP, transmit a command, and return from LP mode. Approximately 12 escape clock ticks are required to enter and leave LP mode. Therefore, only 1 byte could be transmitted in this period.

A short packet (for example, generic short write) requires a minimum of 4 bytes. Therefore, in this exampled, commands are not sent in the VACT region. If Burst mode is enabled, more time is available to transmit commands in the VACT region. The following are assumed:

The controller is not in Burst mode

```
phy_lp2hs_time=16
```

phy_lp2hs_time=16

In this example invact_lpcmd_time is calculated as follows:

$$\text{Invact_lpcmd_time} = (2.3\mu\text{s} - (16*10\text{ ns}) - (20*10\text{ ns}) - (8*66\text{ ns})) / 66\text{ ns} / 8 = 2 \text{ bytes}$$

The outvact_lpcmd_time and invact_lpcmd_time fields allow a simple comparison to determine if a command can be transmitted in any of the BLLP periods.

Fig. 38-8 illustrates the meaning of invact_lpcmd_time and outvact_lpcmd_time, matching them with the shaded areas and the VACT region.

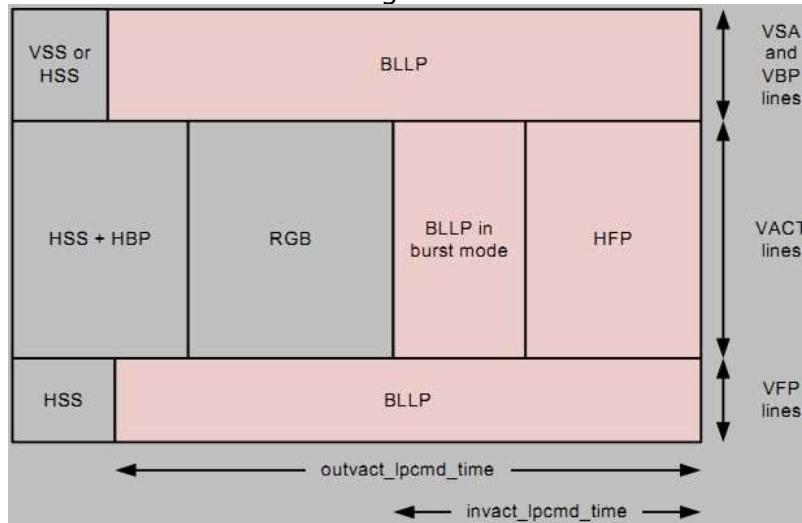


Fig. 14-8 Location in the Image Area

If the lpcmden bit of the VID_MODE_CFG register is 0, the commands are sent in high_speed in Video Mode. In this case, the DWC_mipi_dsi_host automatically determines the area where each command can be sent and no programming or calculation is required.

On read command Transmission, the max_rd_time field of the PHY_TMR_CFG register configures the maximum amount of time required to perform a read command in lane byte clock cycles.

The maximum time required to perform a read command in Lane byte clock cycles (max_rd_time) = Time to transmit the read command in LP mode + Time to enter and leave LP mode + Time to return the read data packet from the peripheral device.

The time to return the read data packet from the peripheral depends on the number of bytes read and the escape clock frequency of the peripheral; not the escape clock of the host. The max_rd_time field is used in both HS and LP mode to determine if there is time to complete a read command in a BLLP period.

In high-speed mode (lpcmden=0), max_rd_time is calculated as follows:

$$\text{max_rd_time} = \text{phy_hs2lp_time} + \text{Time to return the read data packet from the peripheral device} + \text{phy_hs2hs_time}$$

In low-power mode (lpcmden = 1), max_rd_time is calculated as follows:

$$\text{max_rd_time} = \text{phy_hs2lp_time} + \text{LPDT command time} + \text{Read command time in LP mode} + \text{Time to return the data read from the peripheral device} + \text{phy_lp2hs_time}$$

Where,

$$\text{LPDT command time} = (8 * \text{Host escape clock period}) / \text{Lane byte clock period}$$

$$\text{Read command time in LP mode} = (32 * \text{host escape clock period}) / \text{lane byte clock period}$$

It is recommended to keep the maximum number of bytes read from the peripheral to a minimum to have sufficient time available to issue the read commands on a line. Ensure that max_rd_time * Lane byte clock period is less than outvact_lpcmd_time * 8 * Escape clock period of the host.

Otherwise, the read commands are serviced on the last line of a frame and the edpihalt signal may be asserted. If it is necessary to read a large number of parameters (>16), increase the max_rd_time while the read command is being executed. When the read has completed, decrease the max_rd_time to a lower value.

14.4 Register Description

This section describes the control/status registers of the design.

14.4.1 Registers Summary

Name	Offset	Size	Reset Value	Description
MIPIC_VERSION	0x00000	W	0x3133302a	Version of the mihi controller
MIPIC_PWR_UP	0x00004	W	0x00000000	Core power-up
MIPIC_CLKMGR_CFG	0x00008	W	0x00000000	Configuration of the internal clock dividers
MIPIC_DPI_VCID	0x0000c	W	0x00000000	The DPI interface configuration.
MIPIC_DPI_COLOR_CODING	0x00010	W	0x00000000	
MIPIC_DPI_CFG_POL	0x00014	W	0x00000000	
MIPIC_LP_CMD_TIM	0x00018	W	0x00000000	Low-power Command Timing Configuration Register.
MIPIC_PCKHDL_CFG	0x0002c	W	0x00000000	Packet handler configuration
MIPIC_GEN_VCID	0x00030	W	0x00000000	
MIPIC_MODE_CFG	0x00034	W	0x00000000	
MIPIC_VID_MODE_CFG	0x00038	W	0x00000000	Video mode configuration.
MIPIC_VID_PKT_SIZE	0x0003c	W	0x00000000	
MIPIC_VID_NUM_CHUNKS	0x00040	W	0x00000000	
MIPIC_VID_NULL_SIZE	0x00044	W	0x00000000	
MIPIC_VID_HSA_TIME	0x00048	W	0x00000000	Line timing configuration.
MIPIC_VID_HBP_TIME	0x0004c	W	0x00000000	
MIPIC_VID_HLINE_TIME	0x00050	W	0x00000000	
MIPIC_VID_VSA_LINES	0x00054	W	0x00000000	Vertical timing configuration.
MIPIC_VID_VBP_LINES	0x00058	W	0x00000000	
MIPIC_VID_VFP_LINES	0x0005c	W	0x00000000	
MIPIC_VID_VACTIVE_LINES	0x00060	W	0x00000000	
MIPIC_EDPI_CMD_SIZE	0x00064	W	0x00000000	
MIPIC_CMD_MODE_CFG	0x00068	W	0x00000000	Command mode configuration
MIPIC_GEN_HDR	0x0006c	W	0x00000000	Generic packet header configuration.
MIPIC_GEN_PLD_DATA	0x00070	W	0x00000000	Generic payload data in and out.
MIPIC_CMD_PKT_STATUS	0x00074	W	0x00000000	Command packet status
MIPIC_TO_CNT_CFG	0x00078	W	0x00000000	Timeout timers configuration
MIPIC_HS_RD_TO_CNT	0x0007c	W	0x00000000	
MIPIC_LP_RD_TO_CNT	0x00080	W	0x00000000	
MIPIC_HS_WR_TO_CNT	0x00084	W	0x00000000	
MIPIC_LP_WR_TO_CNT	0x00088	W	0x00000000	
MIPIC_BTA_TO_CNT	0x0008c	W	0x00000000	
MIPIC_LPCLK_CTRL	0x00094	W	0x00000000	
MIPIC_PHY_TMR_LPCLK_CFG	0x00098	W	0x00000000	

Name	Offset	Size	Reset Value	Description
MIPIC_PHY_TMR_CFG	0x0009c	W	0x00000000	D-PHY timing configuration
MIPIC_PHY_RSTZ	0x000a0	W	0x00000000	D-PHY reset control
MIPIC_PHY_IF_CFG	0x000a4	W	0x00000000	D-PHY interface configuration
MIPIC_PHY_ULPS_CTRL	0x000a8	W	0x00000000	D-PHY PPI interface control
MIPIC_PHY_TX_TRIGGERES	0x000ac	W	0x00000000	
MIPIC_PHY_STATUS	0x000b0	W	0x00000000	D-PHY PPI status interface
MIPIC_PHY_TST_CTRL0	0x000b4	W	0x00000001	
MIPIC_PHY_TST_CTRL_1	0x000b8	W	0x00000000	
MIPIC_ERROR_ST0	0x000bc	W	0x00000000	Interrupt status register 0
MIPIC_ERROR_ST1	0x000c0	W	0x00000000	Interrupt status register 1
MIPIC_MSK0	0x000c4	W	0x00000000	Masks the interrupt generation triggerd by the ERROR_ST0 reg
MIPIC_MSK1	0x000c8	W	0x00000000	Masks the interrupt generation triggerd by the ERROR_ST1 reg
MIPIC_INT_FORCE0	0x000d8	W	0x00000000	
MIPIC_INT_FORCE1	0x000dc	W	0x00000000	
MIPIC_VID_SHADOW_CTRL	0x00100	W	0x00000000	
MIPIC_Copy0 DPI_VCID	0x0010c	W	0x00000000	The DPI interface configuration.
MIPIC_Copy0 DPI_COLOR_CODING	0x00110	W	0x00000000	
MIPIC_Copy0 LP_CMD_TIM	0x00118	W	0x00000000	Low-power Command Timing Configuration Register.
MIPIC_Copy0 VID_MODE_CFG	0x00138	W	0x00000000	Video mode configuration.
MIPIC_Copy0 VID_PKT_SIZE	0x0013c	W	0x00000000	
MIPIC_Copy0 VID_NUM_CHUNKS	0x00140	W	0x00000000	
MIPIC_Copy0 VID_NULL_SIZE	0x00144	W	0x00000000	
MIPIC_Copy0 VID_HSA_TIME	0x00148	W	0x00000000	Line timing configuration.
MIPIC_Copy0 VID_HBP_TIME	0x0014c	W	0x00000000	
MIPIC_Copy0 VID_HLINE_TIME	0x00150	W	0x00000000	
MIPIC_Copy0 VID_VSA_LINES	0x00154	W	0x00000000	Vertical timing configuration.
MIPIC_Copy0 VID_VBP_LINES	0x00158	W	0x00000000	
MIPIC_Copy0 VID_VFP_LINES	0x0015c	W	0x00000000	
MIPIC_Copy0 VID_VACTIVE_LINES	0x00160	W	0x00000000	

Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access

14.4.2 Detail Register Description

MIPIC_VERSION

Address: Operational Base + offset (0x00000)

Version of the mipi controller

Bit	Attr	Reset Value	Description
31:0	RO	0x3133302a	version indicates the version of the mipi_controller

MIPIC_PWR_UP

Address: Operational Base + offset (0x00004)

Core power-up

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	shutdownz This bit indicates the core power-up or the reset 0-Reset 1-Power-up

MIPIC_CLKMGR_CFG

Address: Operational Base + offset (0x00008)

Configuration of the internal clock dividers

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:8	RW	0x00	TO_CLK_DIVISION This field indicates the division factor for the Time Out clock used as the timing unit in the configuration of HS to LP and LP to HS transition error.
7:0	RW	0x00	TX_ESC_CLK_DIVISION Field0000 Abstract This field indicates the division factor for the TX_Escape clock source(lanebyteclk).The value 0 and 1 stop the TX_ESC clock generation

MIPIC_DPI_VCID

Address: Operational Base + offset (0x0000c)

The DPI interface configuration.

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved

Bit	Attr	Reset Value	Description
1:0	RW	0x0	dpi_vid This field configures the DPI virtual channel id that is indexed to the Video mode packets.

MIPIC_DPI_COLOR_CODING

Address: Operational Base + offset (0x00010)

Bit	Attr	Reset Value	Description
31:9	RO	0x0	reserved
8	RW	0x0	en18_loosely When set to 1, this bit enables 18 loosely packed pixel stream.
7:4	RO	0x0	reserved
3:0	RW	0x0	dpi_color_coding This field configures the DPI color coding as follows: 000:16bit configuration 1 001:16bit configuration 2 010:16bit configuration 3 011:18bit configuration 1 100:18bit configuration 2 101:24bit

MIPIC_DPI_CFG_POL

Address: Operational Base + offset (0x00014)

Bit	Attr	Reset Value	Description
31:5	RO	0x0	reserved
4	RW	0x0	colorm_active_low When set to 1, this bit configures the color mode pin as active low
3	RW	0x0	shutd_active_low When set to 1, this bit configures the shutdown pin as active low
2	RW	0x0	hsync_active_low When set to 1, this bit configures the horizontal synchronism pin as active low.
1	RW	0x0	vsync_active_low When set to 1, this bit configures the vertical synchronism pin as active low
0	RW	0x0	dataen_active_low When set to 1, this bit configures the data enable pin as active low

MIPIC_LP_CMD_TIM

Address: Operational Base + offset (0x00018)
 Low-power Command Timing Configuration Register.

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23:16	RW	0x00	outvact_lpcmd_time outside VACT region command time.This field configures the time available to transmit a command in low-power mode.The time value is expressed in a number of bytes format.The number of bytes represents the maximum size of a packet that can fit in a line during the VSA,VBP, and VFP region. This field must be configured with a value greater than or equal to four bytes to allow the transmission of the DCTRL commands such as shutdown and colorm in low-power mode.
15:8	RO	0x0	reserved
7:0	RW	0x00	invact_lpcmd_time Inside VACT region command time.This field configures the time available to transmit a command in low-power mode.The time value is expressed in a number of bytes format.The number of bytes represents the maximum size of the packet that can fit a line during the VACT region.

MIPIC_PCKHDL_CFG

Address: Operational Base + offset (0x0002c)

Packet handler configuration

Bit	Attr	Reset Value	Description
31:5	RO	0x0	reserved
4	RW	0x0	en_CRC_rx When set to 1, this bit enables the CRC reception and error reporting
3	RW	0x0	en_ECC_rx When set to 1, this bit enables the ECC reception, error correction, and reporting
2	RW	0x0	en_BTA When set to 1, this bit enables the Bus Turn-Around(BTA) request.
1	RW	0x0	en_EOTP_rx Field0000 Abstract When set to 1, this bit enables the EOTP reception

Bit	Attr	Reset Value	Description
0	RW	0x0	en_EOTP_tx Field0000 Abstract When set to 1, this bit enables the EOTP transmission

MIPIC_GEN_VCID

Address: Operational Base + offset (0x00030)

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1:0	RW	0x0	gen_vcid_rx the Generic interface read-back virtual channel identification

MIPIC_MODE_CFG

Address: Operational Base + offset (0x00034)

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	en_video_mode When set to 1, this bit enables the DPI Video mode transmission.

MIPIC_VID_MODE_CFG

Address: Operational Base + offset (0x00038)

Video mode configuration.

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24	RW	0x0	vpg_orientation This field indicates the color bar orientation as follows: 0:Vertical mode 1:Horizontal mode
23:21	RO	0x0	reserved
20	RW	0x0	vpg_mode This field is to select the pattern 0:Color bar(horizontal or vertical) 1:BER pattern(vertical only)
19:17	RO	0x0	reserved
16	RW	0x0	vpg_en When set to 1, this bit enables the video mode pattern generator

Bit	Attr	Reset Value	Description
15	RW	0x0	lpcmden When set to 1, this bit enables the command transmission only in low-power mode
14	RW	0x0	frame_BTA_ack When set to 1, this bit enables the request for an acknowledge response at the end of a frame
13	RW	0x0	en_lp_hfp When set to 1, this bit enables the return to low-power inside the HFP period when timing allows.
12	RW	0x0	en_lp_hbp When set to 1, this bit enables the return to low-power inside the HBP period when timing allows.
11	RW	0x0	en_lp_vact When set to 1, this bit enables the return to low-power inside the VACT period when timing allows.
10	RW	0x0	en_lp_vfp When set to 1, this bit enables the return to low-power inside the VFP period when timing allows.
9	RW	0x0	en_lp_vbp When set to 1, this bit enables the return to low-power inside the VBP period when timing allows.
8	RW	0x0	en_lp_vsa When set to 1, this bit enables the return to low-power inside the VSA period when timing allows.
7:2	RO	0x0	reserved
1:0	RW	0x0	vid_mode_type This field indicates the video mode transmission type as follows: 00: Non-burst with sync pulses 01: Non-burst with sync events 10 and 11: Burst with sync pulses

MIPIC_VID_PKT_SIZE

Address: Operational Base + offset (0x0003c)

Bit	Attr	Reset Value	Description
31:14	RO	0x0	reserved

Bit	Attr	Reset Value	Description
13:0	RW	0x0000	vid_pkt_size This field configures the number of pixels on a single video packet. If you use the 18-bit mode and do not enable loosely packed stream, this value must be a multiple of 4.

MIPIC_VID_NUM_CHUNKS

Address: Operational Base + offset (0x00040)

Bit	Attr	Reset Value	Description
31:13	RO	0x0	reserved
12:0	RW	0x0000	num_chunks This field configures the number of chunks to be transmitted during a line period (a chunk is a video packet or a null packet)

MIPIC_VID_NULL_SIZE

Address: Operational Base + offset (0x00044)

Bit	Attr	Reset Value	Description
31:13	RO	0x0	reserved
12:0	RW	0x0000	null_pkt_size This field configures the number of bytes in a null packet

MIPIC_VID_HSA_TIME

Address: Operational Base + offset (0x00048)

Line timing configuration.

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:0	RW	0x000	hsa_time This field configures the Horizontal Synchronization Active period in lane byte clock cycles.

MIPIC_VID_HBP_TIME

Address: Operational Base + offset (0x0004c)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:0	RW	0x000	hbp_time This field configures the Horizontal Back Porch period in lane byte clock cycles

MIPIC_VID_HLINE_TIME

Address: Operational Base + offset (0x00050)

Bit	Attr	Reset Value	Description
31:15	RO	0x0	reserved
14:0	RW	0x0000	hline_time This field configures the size of the total lines counted in lane byte cycles.

MIPIC_VID_VSA_LINES

Address: Operational Base + offset (0x00054)

Vertical timing configuration.

Bit	Attr	Reset Value	Description
31:10	RO	0x0	reserved
9:0	RW	0x000	vsa_lines This field configures the Vertical Synchronism Active period measured in number of horizontal lines.

MIPIC_VID_VBP_LINES

Address: Operational Base + offset (0x00058)

Bit	Attr	Reset Value	Description
31:10	RO	0x0	reserved
9:0	RW	0x000	vbp_lines This field configures the Vertical Back Porch period measured in horizontal lines.

MIPIC_VID_VFP_LINES

Address: Operational Base + offset (0x0005c)

Bit	Attr	Reset Value	Description
31:10	RO	0x0	reserved
9:0	RW	0x000	vfp_lines This field configures the Vertical Front Porch period measured in horizontal lines.

MIPIC_VID_VACTIVE_LINES

Address: Operational Base + offset (0x00060)

Bit	Attr	Reset Value	Description
31:14	RO	0x0	reserved
13:0	RW	0x0000	v_active_line This field configures the Vertical Active period measured in horizontal lines.

MIPIC_EDPI_CMD_SIZE

Address: Operational Base + offset (0x00064)

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:0	RW	0x0000	edpi_allowed_cmd_size This field configures the maximum allowed size for an eDPI write memory command, measured in pixels. Automatic partitioning of data obtained from eDPI is permanently enabled.

MIPIC_CMD_MODE_CFG

Address: Operational Base + offset (0x00068)

Command mode configuration

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24	RW	0x0	max_rd_pkt_size This bit configures the maximum read packet size command transmission type: 0:High-speed 1:Low-power
23:20	RO	0x0	reserved
19	RW	0x0	dcs_lw_tx This bit configures the DCS long write packet command transmission type: 0:high-speed 1:low-power
18	RW	0x0	dcs_sr_0p_tx This bit configures the DCS short read packet with zero parameter command transmission type: 0:High-speed 1:Low-power
17	RW	0x0	dcs_sw_1p_tx This bit configures the DCS short write packet with one parameter command transmission type: 0:High-speed 1:Low-power
16	RW	0x0	dcs_sw_0p_tx This bit configures the DCS short write packet with zero parameter command transmission type: 0:High-speed 1:Low-power

Bit	Attr	Reset Value	Description
15	RO	0x0	reserved
14	RW	0x0	gen_lw_tx This bit configures the Generic long write packet command transmission type: 0:high-speed 1:low-power
13	RW	0x0	gen_sr_2p_tx This bit configures the Generic short read packet with two parameter command transmission type: 0:High-speed 1:Low-power
12	RW	0x0	gen_sr_1p_tx This bit configures the Generic short read packet with one parameter command transmission type: 0:High-speed 1:Low-power
11	RW	0x0	gen_sr_0p_tx This bit configures the Generic short read packet with zero parameter command transmission type: 0:High-speed 1:Low-power
10	RW	0x0	gen_sw_2p_tx This bit configures the Generic short write packet with two parameter command transmission type: 0:High-speed 1:Low-power
9	RW	0x0	gen_sw_1p_tx This bit configures the Generic short write packet with one parameter command transmission type: 0:High-speed 1:Low-power
8	RW	0x0	gen_sw_0p_tx This bit configures the Generic short write packet with zero parameter command transmission type: 0:High-speed 1:Low-power
7:2	RO	0x0	reserved

Bit	Attr	Reset Value	Description
1	RW	0x0	ack_rqst_en When set to 1, this bit enables the acknowledge request after each packet transmission
0	RW	0x0	tear_fx_en When set to 1, this bit enables the tearing effect acknowledge request

MIPIC_GEN_HDR

Address: Operational Base + offset (0x0006c)

Generic packet header configuration.

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23:16	RW	0x00	gen_WC_MSbyte This field configures the most significant byte of the header packet's Word count for long packets or data 1 for short packets.
15:8	RW	0x00	gen_WC_LSbyte This field configures the least significant byte of the header packet's Word count for long packets or data 0 for short packets.
7:6	RW	0x0	gen_VC This field configures the virtual channel id of the header packet.
5:0	RW	0x00	gen_DT This field configures the packet data type of the header packet

MIPIC_GEN_PLD_DATA

Address: Operational Base + offset (0x00070)

Generic payload data in and out.

Bit	Attr	Reset Value	Description
31:24	RW	0x00	gen_pld_b4 This field indicates byte 4 of the packet payload.
23:16	RW	0x00	gen_pld_b3 This field indicates byte 3 of the packet payload.
15:8	RW	0x00	gen_pld_b2 This field indicates byte 2 of the packet payload.
7:0	RW	0x00	gen_pld_b1 This field indicates byte 1 of the packet payload.

MIPIC_CMD_PKT_STATUS

Address: Operational Base + offset (0x00074)

Command packet status

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7	RW	0x0	reserved reserved
6	RW	0x0	gen_rd_cmd_busy This bit is set when a read command is issued and cleared when the entire response is stored in the FIFO
5	RW	0x0	gen_pld_r_full This bit indicates the full status of the generic read payload FIFO Value after reset:0x0
4	RO	0x0	gen_pld_r_empty This bit indicates the empty status of the generic read payload FIFO Value after reset:0x1
3	RO	0x0	gen_pld_w_full This bit indicates the full status of the generic write payload FIFO Value after reset:0x0
2	RO	0x0	gen_pld_w_empty This bit indicates the empty status of the generic write payload FIFO Value after reset:0x1
1	RO	0x0	gen_cmd_full This bit indicates the full status of the generic command FIFO Value after reset:0x0
0	RO	0x0	gen_cmd_empty This bit indicates the empty status of the generic command FIFO Value after reset:0x1

MIPIC_TO_CNT_CFG

Address: Operational Base + offset (0x00078)

Timeout timers configuration

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	hstx_to_cnt This field configures the timeout counter that triggers a high-speed transmission timeout contention detection(measured in TO_CLK_DIVISION cycles)

Bit	Attr	Reset Value	Description
15:0	RW	0x0000	lpx_to_cnt This field configures the timeout counter that triggers a low-power reception timeout contention detection(measured in TO_CLK_DIVISION cycles)

MIPIC_HS_RD_TO_CNT

Address: Operational Base + offset (0x0007c)

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:0	RW	0x0000	hs_rd_to_cnt This field sets a period for which the MIPI Controller keeps the link still,after sending a high-speed read operation.This period is measured in cycles of lanebyteclk.The counting starts when the D-PHY enters the Stop state and causes no interrupts.

MIPIC_LP_RD_TO_CNT

Address: Operational Base + offset (0x00080)

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:0	RW	0x0000	lp_rd_to_cnt This field sets a period for which MIPI Controller keeps the link still,after sending a low-power read operation.This period is measured in cycles of lanebyteclk.The counting starts when the D-PHY enters the Stop state and causes no interrupts.

MIPIC_HS_WR_TO_CNT

Address: Operational Base + offset (0x00084)

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved

Bit	Attr	Reset Value	Description
24	RW	0x0	<p>presp_to_mode</p> <p>When set to 1, this bit ensures that the peripheral response timeout caused by hs_wr_to_cnt is used only once per eDPI frame, when both the following conditions are met:</p> <ul style="list-style-type: none"> .dpirsync_edpiwms has risen and fallen .packets originated from eDPI have been transmitted and its FIFO is empty again.
23:16	RO	0x0	reserved
15:0	RW	0x0000	<p>hs_wr_to_cnt</p> <p>This field sets a period for which the MIPI Controller keeps the link inactive after sending a high-speed write operation. This period is measured in cycles of lanebyteclk. The counting starts when the D-PHY enters the Stop state and causes no interrupts.</p>

MIPIC_LP_WR_TO_CNT

Address: Operational Base + offset (0x00088)

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:0	RW	0x0000	<p>lp_wr_to_cnt</p> <p>This field sets a period for which the DSI Controller keeps the link still, after sending a low-power write operation. This period is measured in cycles of lanebyteclk. The counting starts when the D-PHY enters the Stop state and causes no interrupts.</p>

MIPIC_BTA_TO_CNT

Address: Operational Base + offset (0x0008c)

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:0	RW	0x0000	<p>bta_to_cnt</p> <p>This field sets a period for which the DSI Controller keeps the link still, after completing a Bus Turn-Around. This period is measured in cycles of lanebyteclk. The counting starts when the D-PHY enters the Stop state and causes no interrupts.</p>

MIPIC_LPCLK_CTRL

Address: Operational Base + offset (0x00094)

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	RW	0x0	auto_clklane_ctrl This bit enables the automatic mechanism to stop providing clock in the clock lane when time allows.
0	RW	0x0	phy_txrequestclkhs This bit controls the D-PHY PPI tx requestclkhs signal

MIPIC_PHY_TMR_LPCLK_CFG

Address: Operational Base + offset (0x00098)

Bit	Attr	Reset Value	Description
31:26	RO	0x0	reserved
25:16	RW	0x000	phy_hs2lp_time This field configures the maximum time that the PHY takes to go from high-speed to low-power transmission measured in lane byte clock cycles.(clock lane)
15:10	RO	0x0	reserved
9:0	RW	0x000	phy_lp2hs_time This field configures the maximum time that the PHY takes to go from low-power to high-speed transmission measured in lane byte clock cycles.(clock lane)

MIPIC_PHY_TMR_CFG

Address: Operational Base + offset (0x0009c)

D-PHY timing configuration

Bit	Attr	Reset Value	Description
31:24	RW	0x00	phy_hs2lp_time This field configures the maximum time that the PHY takes to go from high-speed to low-power transmission measured in lane byte clock cycles.
23:16	RW	0x00	phy_lp2hs_time This field configures the maximum time that the PHY takes to go from low-power to high-speed transmission measured in lane byte clock cycles.
15	RW	0x0	reserved reserved for future use

Bit	Attr	Reset Value	Description
14:0	RW	0x0000	max_rd_time This field configures the maximum time required to perform a read command in lane byte clock cycles. This register can only be modified when read commands are not in progress.

MIPIC_PHY_RSTZ

Address: Operational Base + offset (0x000a0)

D-PHY reset control

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved
3	RW	0x0	phy_forcepll When the D-PHY is in ULPS, this bit enables the D-PHY PLL
2	RW	0x0	phy_enableclk When set to 1, this bit enables the D-PHY Clock Lane Module
1	RW	0x0	phy_rstz When set to 0, this bit places the digital section of the D-PHY in the reset state
0	RW	0x0	phy_shutdownz When set to 0, this bit places the D-PHY macro in power-down state

MIPIC_PHY_IF_CFG

Address: Operational Base + offset (0x000a4)

D-PHY interface configuration

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:8	RW	0x00	phy_stop_wait_time This field configures the minimum wait period to request a high-speed transmission after the Stop state is accounted in clock lane cycles.
7:2	RO	0x0	reserved
1:0	RW	0x0	n_lanes This field configures the number of active data lanes: 00:One data lane(lane 0) 01:Two data lane(lanes 0 and 1) 10:Three data lanes(lanes 0,1, and 2) 11:Four data lanes(lanes 0,1,2, and 3)

MIPIC_PHY_ULPS_CTRL

Address: Operational Base + offset (0x000a8)

D-PHY PPI interface control

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved
3	RW	0x0	phy_txexitulpslan ULPS mode Exit on all active data lanes
2	RW	0x0	phy_txrequlpslan ULPS mode Request on all active data lanes
1	RW	0x0	phy_txexitulpsclk ULPS mode Exit on clock lane
0	RW	0x0	phy_txrequlpsclk ULPS mode Request on clock lane

MIPIC_PHY_TX_TRIGGER

Address: Operational Base + offset (0x000ac)

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved
3:0	RW	0x0	phy_tx_triggers This field controls the trigger transmissions.

MIPIC_PHY_STATUS

Address: Operational Base + offset (0x000b0)

D-PHY PPI status interface

Bit	Attr	Reset Value	Description
31:13	RO	0x0	reserved
12	RO	0x0	ulpsactivenot3lane This bit indicates the status of ulpsactivenot3lane D-PHY signal
11	RO	0x0	phystopstate3lane This bit indicates the status of phystopstate3lane D-PHY signal
10	RO	0x0	ulpsactivenot2lane This bit indicates the status of ulpsactivenot2lane D-PHY signal
9	RO	0x0	phystopstate2lane This bit indicates the status of phystopstate2lane D-PHY signal
8	RO	0x0	ulpsactivenot1lane This bit indicates the status of ulpsactivenot1lane D-PHY signal
7	RO	0x0	phystopstate1lane This bit indicates the status of phystopstate1lane D-PHY signal

Bit	Attr	Reset Value	Description
6	RW	0x0	rxulpsesc0lane This bit indicates the status of rxulpsesc0lane D-PHY signal
5	RO	0x0	ulpsactivenot0lane This bit indicates the status of ulpsactivenot0lane D-PHY signal
4	RO	0x0	phystopstate0lane This bit indicates the status of phystopstate0lane D-PHY signal
3	RO	0x0	phyulpsactivenotclk This bit indicates the status of phyulpsactivenotclk D-PHY signal
2	RO	0x0	phystopstateclklane This bit indicates the status of phystopstateclklane D-PHY signal
1	RO	0x0	phydirection This bit indicates the status of phydirection D-PHY signal
0	RO	0x0	phylock This bit indicates the status of phylock D-PHY signal

MIPIC_PHY_TST_CTRL0

Address: Operational Base + offset (0x000b4)

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	RW	0x0	phy_testclk This bit is used to clock the TESTDIN bus into the D-PHY
0	RW	0x1	phy_testclr PHY test interface clear(active high)

MIPIC_PHY_TST_CTRL_1

Address: Operational Base + offset (0x000b8)

Bit	Attr	Reset Value	Description
31:17	RO	0x0	reserved
16	RW	0x0	phy_testen PHY test interface operation selector: 1:The address write operation is set on the falling edge of the testclk signal 0:The data write operation is set on the rising edge of the testclk signal

Bit	Attr	Reset Value	Description
15:8	RW	0x00	phy_testdout PHY output 8-bit data bus for read-back and internal probing functionalities
7:0	RW	0x00	phy_testdin PHY test interface input 8-bit data bus for internal register programming and test functionalities access

MIPIC_ERROR_ST0

Address: Operational Base + offset (0x000bc)

Interrupt status register 0

Bit	Attr	Reset Value	Description
31:21	RO	0x0	reserved
20	RO	0x0	dphy_errors_4 This bit indicates LP1 contention error ErrContentionLP1 from Lane 0
19	RO	0x0	dphy_errors_3 This bit indicates LP0 contention error ErrContentionLP0 from Lane 0
18	RO	0x0	dphy_errors_2 This bit indicates control error ErrControl from Lane 0
17	RO	0x0	dphy_errors_1 This bit indicates ErrSyncEsc low-power data transmission synchronization error from Lane 0
16	RO	0x0	dphy_errors_0 This bit indicates ErrEsc escape entry error from Lane 0
15	RO	0x0	ack_with_err_15 This bit retrieves the DSI protocol violation from the Display Acknowledge error report
14	RO	0x0	ack_with_err_14 This bit retrieves the reserved(specific to device) from the Display Acknowledge error report
13	RO	0x0	ack_with_err_13 This bit retrieves the invalid transmission length from the Display Acknowledge error report
12	RO	0x0	ack_with_err_12 This bit retrieves the DSI VC ID Invalid from the Display Acknowledge error report

Bit	Attr	Reset Value	Description
11	RO	0x0	ack_with_err_11 This bit retrieves the not recognized DSI data type from the Display Acknowledge error report
10	RO	0x0	ack_with_err_10 This bit retrieves the checksum error(long packet only) from the Display Acknowledge error report
9	RO	0x0	ack_with_err_9 This bit retrieves the ECC error,multi-bit(detected and corrected) from the Display Acknowledge error report
8	RO	0x0	ack_with_err_8 This bit retrieves the ECC error,single-bit(detected and corrected) from the Display Acknowledge error report
7	RO	0x0	ack_with_err_7 This bit retrieves the reserved(specific to device) error from the Display Acknowledge error report
6	RO	0x0	ack_with_err_6 This bit retrieves the False Control error from the Display Acknowledge error report
5	RO	0x0	ack_with_err_5 This bit retrieves the HS Receive Timeout error from the Display Acknowledge error report
4	RO	0x0	ack_with_err_4 This bit retrieves the LP Transmit Sync error from the Display Acknowledge error report
3	RO	0x0	ack_with_err_3 This bit retrieves the Escape Mode Entry command error from the Display Acknowledge error report
2	RO	0x0	ack_with_err_2 This bit retrieves the EoT sync error from the Display Acknowledge error report
1	RO	0x0	ack_with_err_1 This bit retrieves the SoT Sync error from the Display Acknowledge error report
0	RO	0x0	ack_with_err_0 This bit retrieves the SoT error from the Display Acknowledge error report

MIPIC_ERROR_ST1

Address: Operational Base + offset (0x000c0)

Interrupt status register 1

Bit	Attr	Reset Value	Description
31:13	RO	0x0	reserved
12	RO	0x0	gen_pld_recv_err This bit indicates that during a generic interface packet read back, the payload FIFO becomes full and the received data is corrupted.
11	RO	0x0	gen_pld_rd_err This bit indicates that during a DCS read data, the payload FIFO becomes empty and the data sent to the interface is corrupted
10	RO	0x0	gen_pld_send_err This bit indicates that during a Generic interface packet build, the payload FIFO becomes empty and corrupt data is sent.
9	RO	0x0	gen_pld_wr_err This bit indicates that the system tried to write a payload data through the Generic interface and the FIFO is full. Therefore, the command is not written.
8	RO	0x0	gen_cmd_wr_err This bit indicates that the system tried to write a command through the Generic interface and the FIFO is full. Therefore, the command is not written.
7	RO	0x0	dpi_pld_wr_err This bit indicates that during a DPI pixel line storage, the payload FIFO becomes full and the data stored is corrupted.
6	RO	0x0	eotp_err This bit indicates that the EOTP packet is not received at the end of the incoming peripheral transmission.
5	RO	0x0	pkt_size_err This bit indicates that the packet size error is detected during the packet reception.
4	RO	0x0	crc_err This bit indicates that the CRC error is detected in a received packet.
3	RO	0x0	ecc_multi_err This bit indicates that the ECC multiple error is detected and corrected in a received packet.

Bit	Attr	Reset Value	Description
2	RO	0x0	ecc_single_err This bit indicates that the ECC single error is detected and corrected in a received packet.
1	RO	0x0	to_lp_rx This bit indicates that the low-power reception timeout counter reached the end and contention detection is detected.
0	RO	0x0	to_hs_tx This bit indicates that the high-speed transmission timeout counter reached the end and contention detection is detected.

MIPIC_MSK0

Address: Operational Base + offset (0x000c4)

Masks the interrupt generation triggered by the ERROR_ST0 reg

Bit	Attr	Reset Value	Description
31:21	RO	0x0	reserved
20	RW	0x0	dphy_errors_4 This bit indicates LP1 contention error ErrContentionLP1 from Lane 0
19	RW	0x0	dphy_errors_3 This bit indicates LP0 contention error ErrContentionLP0 from Lane 0
18	RW	0x0	dphy_errors_2 This bit indicates control error ErrControl from Lane 0
17	RW	0x0	dphy_errors_1 This bit indicates ErrSyncEsc low-power data transmission synchronization error from Lane 0
16	RW	0x0	dphy_errors_0 This bit indicates ErrEsc escape entry error from Lane 0
15	RW	0x0	ack_with_err_15 This bit retrieves the DSI protocol violation from the Display Acknowledge error report
14	RW	0x0	ack_with_err_14 This bit retrieves the reserved(specific to device) from the Display Acknowledge error report
13	RW	0x0	ack_with_err_13 This bit retrieves the invalid transmission length from the Display Acknowledge error report

Bit	Attr	Reset Value	Description
12	RW	0x0	ack_with_err_12 This bit retrieves the DSI VC ID Invalid from the Display Acknowledge error report
11	RW	0x0	ack_with_err_11 This bit retrieves the not recognized DSI data type from the Display Acknowledge error report
10	RW	0x0	ack_with_err_10 This bit retrieves the checksum error(long packet only) from the Display Acknowledge error report
9	RW	0x0	ack_with_err_9 This bit retrieves the ECC error,multi-bit(detected and corrected) from the Display Acknowledge error report
8	RW	0x0	ack_with_err_8 This bit retrieves the ECC error,single-bit(detected and corrected) from the Display Acknowledge error report
7	RW	0x0	ack_with_err_7 This bit retrieves the reserved(specific to device) error from the Display Acknowledge error report
6	RW	0x0	ack_with_err_6 This bit retrieves the False Control error from the Display Acknowledge error report
5	RW	0x0	ack_with_err_5 This bit retrieves the HS Receive Timeout error from the Display Acknowledge error report
4	RW	0x0	ack_with_err_4 This bit retrieves the LP Transmit Sync error from the Display Acknowledge error report
3	RW	0x0	ack_with_err_3 This bit retrieves the Escape Mode Entry command error from the Display Acknowledge error report
2	RW	0x0	ack_with_err_2 This bit retrieves the EoT sync error from the Display Acknowledge error report
1	RW	0x0	ack_with_err_1 This bit retrieves the SoT Sync error from the Display Acknowledge error report

Bit	Attr	Reset Value	Description
0	RW	0x0	ack_with_err_0 This bit retrieves the SoT error from the Display Acknowledge error report

MIPIC_MSK1

Address: Operational Base + offset (0x000c8)

Masks the interrupt generation triggered by the ERROR_ST1 reg

Bit	Attr	Reset Value	Description
31:13	RO	0x0	reserved
12	RO	0x0	gen_pld_recv_err This bit indicates that during a generic interface packet read back, the payload FIFO becomes full and the received data is corrupted.
11	RO	0x0	gen_pld_rd_err This bit indicates that during a DCS read data, the payload FIFO becomes empty and the data sent to the interface is corrupted
10	RO	0x0	gen_pld_send_err This bit indicates that during a Generic interface packet build, the payload FIFO becomes empty and corrupt data is sent.
9	RO	0x0	gen_pld_wr_err This bit indicates that the system tried to write a payload data through the Generic interface and the FIFO is full. Therefore, the command is not written.
8	RO	0x0	gen_cmd_wr_err This bit indicates that the system tried to write a command through the Generic interface and the FIFO is full. Therefore, the command is not written.
7	RO	0x0	dpi_pld_wr_err This bit indicates that during a DPI pixel line storage, the payload FIFO becomes full and the data stored is corrupted.
6	RO	0x0	eotp_err This bit indicates that the EOTP packet is not received at the end of the incoming peripheral transmission.
5	RO	0x0	pkt_size_err This bit indicates that the packet size error is detected during the packet reception.

Bit	Attr	Reset Value	Description
4	RO	0x0	crc_err This bit indicates that the CRC error is detected in a received packet.
3	RO	0x0	ecc_multi_err This bit indicates that the ECC multiple error is detected and corrected in a received packet.
2	RO	0x0	ecc_single_err This bit indicates that the ECC single error is detected and corrected in a received packet.
1	RO	0x0	to_lp_rx This bit indicates that the low-power reception timeout counter reached the end and contention detection is detected.
0	RO	0x0	to_hs_tx This bit indicates that the high-speed transmission timeout counter reached the end and contention detection is detected.

MIPIC_INT_FORCE0

Address: Operational Base + offset (0x000d8)

Bit	Attr	Reset Value	Description
31:21	RO	0x0	reserved
20	RO	0x0	dphy_errors_4 This bit indicates LP1 contention error ErrContentionLP1 from Lane 0
19	RO	0x0	dphy_errors_3 This bit indicates LP0 contention error ErrContentionLP0 from Lane 0
18	RO	0x0	dphy_errors_2 This bit indicates control error ErrControl from Lane 0
17	RO	0x0	dphy_errors_1 This bit indicates ErrSyncEsc low-power data transmission synchronization error from Lane 0
16	RO	0x0	dphy_errors_0 This bit indicates ErrEsc escape entry error from Lane 0
15	RO	0x0	ack_with_err_15 This bit retrieves the DSI protocol violation from the Display Acknowledge error report

Bit	Attr	Reset Value	Description
14	RO	0x0	ack_with_err_14 This bit retrieves the reserved(specific to device) from the Display Acknowledge error report
13	RO	0x0	ack_with_err_13 This bit retrieves the invalid transmission length from the Display Acknowledge error report
12	RO	0x0	ack_with_err_12 This bit retrieves the DSI VC ID Invalid from the Display Acknowledge error report
11	RO	0x0	ack_with_err_11 This bit retrieves the not recognized DSI data type from the Display Acknowledge error report
10	RO	0x0	ack_with_err_10 This bit retrieves the checksum error(long packet only) from the Display Acknowledge error report
9	RO	0x0	ack_with_err_9 This bit retrieves the ECC error,multi-bit(detected and corrected) from the Display Acknowledge error report
8	RO	0x0	ack_with_err_8 This bit retrieves the ECC error,single-bit(detected and corrected) from the Display Acknowledge error report
7	RO	0x0	ack_with_err_7 This bit retrieves the reserved(specific to device) error from the Display Acknowledge error report
6	RO	0x0	ack_with_err_6 This bit retrieves the False Control error from the Display Acknowledge error report
5	RO	0x0	ack_with_err_5 This bit retrieves the HS Receive Timeout error from the Display Acknowledge error report
4	RO	0x0	ack_with_err_4 This bit retrieves the LP Transmit Sync error from the Display Acknowledge error report

Bit	Attr	Reset Value	Description
3	RO	0x0	ack_with_err_3 This bit retrieves the Escape Mode Entry command error from the Display Acknowledge error report
2	RO	0x0	ack_with_err_2 This bit retrieves the EoT sync error from the Display Acknowledge error report
1	RO	0x0	ack_with_err_1 This bit retrieves the SoT Sync error from the Display Acknowledge error report
0	RO	0x0	ack_with_err_0 This bit retrieves the SoT error from the Display Acknowledge error report

MIPIC_INT_FORCE1

Address: Operational Base + offset (0x000dc)

Bit	Attr	Reset Value	Description
31:13	RO	0x0	reserved
12	RO	0x0	gen_pld_recv_err This bit indicates that during a generic interface packet read back, the payload FIFO becomes full and the received data is corrupted.
11	RO	0x0	gen_pld_rd_err This bit indicates that during a DCS read data, the payload FIFO becomes empty and the data sent to the interface is corrupted
10	RO	0x0	gen_pld_send_err This bit indicates that during a Generic interface packet build, the payload FIFO becomes empty and corrupt data is sent.
9	RO	0x0	gen_pld_wr_err This bit indicates that the system tried to write a payload data through the Generic interface and the FIFO is full. Therefore, the command is not written.
8	RO	0x0	gen_cmd_wr_err This bit indicates that the system tried to write a command through the Generic interface and the FIFO is full. Therefore, the command is not written.

Bit	Attr	Reset Value	Description
7	RO	0x0	dpi_pld_wr_err This bit indicates that during a DPI pixel line storage, the payload FIFO becomes full and the data stored is corrupted.
6	RO	0x0	eopt_err This bit indicates that the EOTP packet is not received at the end of the incoming peripheral transmission.
5	RO	0x0	pkt_size_err This bit indicates that the packet size error is detected during the packet reception.
4	RO	0x0	crc_err This bit indicates that the CRC error is detected in a received packet.
3	RO	0x0	ecc_multi_err This bit indicates that the ECC multiple error is detected and corrected in a received packet.
2	RO	0x0	ecc_single_err This bit indicates that the ECC single error is detected and corrected in a received packet.
1	RO	0x0	to_lp_rx This bit indicates that the low-power reception timeout counter reached the end and contention detection is detected.
0	RO	0x0	to_hs_tx This bit indicates that the high-speed transmission timeout counter reached the end and contention detection is detected.

MIPIC_VID_SHADOW_CTRL

Address: Operational Base + offset (0x00100)

Bit	Attr	Reset Value	Description
31:17	RO	0x0	reserved
16	RW	0x0	vid_shadow_pin_req When set to 1, the video request is done by external pin. In this mode, vid_shadow_req is ignored
15:9	RO	0x0	reserved
8	RW	0x0	vid_shadow_req When set to 1, the DPI registers are copied to the auxiliary registers. After coping, this bit is auto cleared.
7:1	RO	0x0	reserved

Bit	Attr	Reset Value	Description
0	RW	0x0	vid_shadow_en When set to 1,DPI receives the active configuration from the auxiliary registers.When this bit is set along with the vid_shadow_req bit,the auxiliary registers are automatically updated.

MIPIC_Copy0 DPI_VCID

Address: Operational Base + offset (0x0010c)

The DPI interface configuration.

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1:0	RW	0x0	dpi_vid This field configures the DPI virtual channel id that is indexed to the Video mode packets.

MIPIC_Copy0 DPI_COLOR_CODING

Address: Operational Base + offset (0x00110)

Bit	Attr	Reset Value	Description
31:9	RO	0x0	reserved
8	RW	0x0	en18_loosely When set to 1,this bit enables 18 loosely packed pixel stream.
7:4	RO	0x0	reserved
3:0	RW	0x0	dpi_color_coding This field configures the DPI color coding as follows: 000:16bit configuration 1 001:16bit configuration 2 010:16bit configuration 3 011:18bit configuration 1 100:18bit configuration 2 101:24bit

MIPIC_Copy0 LP_CMD_TIM

Address: Operational Base + offset (0x00118)

Low-power Command Timing Configuration Register.

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved

Bit	Attr	Reset Value	Description
23:16	RW	0x00	outvact_lpcmd_time outside VACT region command time.This field configures the time available to transmit a command in low-power mode.The time value is expressed in a number of bytes format.The number of bytes represents the maximum size of a packet that can fit in a line during the VSA,VBP, and VFP region. This field must be configured with a value greater than or equal to four bytes to allow the transmission of the DCTRL commands such as shutdown and colorm in low-power mode.
15:8	RO	0x0	reserved
7:0	RW	0x00	invact_lpcmd_time Inside VACT region command time.This field configures the time available to transmit a command in low-power mode.The time value is expressed in a number of bytes format.The number of bytes represents the maximum size of the packet that can fit a line during the VACT region.

MIPIC_Copy0 VID_MODE_CFG

Address: Operational Base + offset (0x00138)

Video mode configuration.

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24	RW	0x0	vpg_orientation This field indicates the color bar orientation as follows: 0:Vertical mode 1:Horizontal mode
23:21	RO	0x0	reserved
20	RW	0x0	vpg_mode This field is to select the pattern 0:Color bar(horizontal or vertical) 1:BER pattern(vertical only)
19:17	RO	0x0	reserved
16	RW	0x0	vpg_en When set to 1, this bit enables the video mode pattern generator
15	RW	0x0	lpcmden When set to 1, this bit enables the command transmission only in low-power mode

Bit	Attr	Reset Value	Description
14	RW	0x0	frame_BTA_ack When set to 1, this bit enables the request for an acknowledge response at the end of a frame
13	RW	0x0	en_lp_hfp When set to 1, this bit enables the return to low-power inside the HFP period when timing allows.
12	RW	0x0	en_lp_hbp When set to 1, this bit enables the return to low-power inside the HBP period when timing allows.
11	RW	0x0	en_lp_vact When set to 1, this bit enables the return to low-power inside the VACT period when timing allows.
10	RW	0x0	en_lp_vfp When set to 1, this bit enables the return to low-power inside the VFP period when timing allows.
9	RW	0x0	en_lp_vbp When set to 1, this bit enables the return to low-power inside the VBP period when timing allows.
8	RW	0x0	en_lp_vsa When set to 1, this bit enables the return to low-power inside the VSA period when timing allows.
7:2	RO	0x0	reserved
1:0	RW	0x0	vid_mode_type This field indicates the video mode transmission type as follows: 00: Non-burst with sync pulses 01: Non-burst with sync events 10 and 11: Burst with sync pulses

MIPIC_Copy0 VID_PKT_SIZE

Address: Operational Base + offset (0x0013c)

Bit	Attr	Reset Value	Description
31:14	RO	0x0	reserved

Bit	Attr	Reset Value	Description
13:0	RW	0x0000	vid_pkt_size This field configures the number of pixels on a single video packet. If you use the 18-bit mode and do not enable loosely packed stream, this value must be a multiple of 4.

MIPIC_Copy0 VID_NUM_CHUNKS

Address: Operational Base + offset (0x00140)

Bit	Attr	Reset Value	Description
31:13	RO	0x0	reserved
12:0	RW	0x0000	num_chunks This field configures the number of chunks to be transmitted during a line period (a chunk is a video packet or a null packet)

MIPIC_Copy0 VID_NULL_SIZE

Address: Operational Base + offset (0x00144)

Bit	Attr	Reset Value	Description
31:13	RO	0x0	reserved
12:0	RW	0x0000	null_pkt_size This field configures the number of bytes in a null packet

MIPIC_Copy0 VID_HSA_TIME

Address: Operational Base + offset (0x00148)

Line timing configuration.

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:0	RW	0x000	hsa_time This field configures the Horizontal Synchronism Active period in lane byte clock cycles.

MIPIC_Copy0 VID_HBP_TIME

Address: Operational Base + offset (0x0014c)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:0	RW	0x000	hbp_time This field configures the Horizontal Back Porch period in lane byte clock cycles

MIPIC_Copy0 VID_HLINE_TIME

Address: Operational Base + offset (0x00150)

Bit	Attr	Reset Value	Description
31:15	RO	0x0	reserved
14:0	RW	0x0000	hline_time This field configures the size of the total lines counted in lane byte cycles.

MIPIC_Copy0 VID_VSA_LINES

Address: Operational Base + offset (0x00154)

Vertical timing configuration.

Bit	Attr	Reset Value	Description
31:10	RO	0x0	reserved
9:0	RW	0x000	vsa_lines This field configures the Vertical Synchronism Active period measured in number of horizontal lines.

MIPIC_Copy0 VID_VBP_LINES

Address: Operational Base + offset (0x00158)

Bit	Attr	Reset Value	Description
31:10	RO	0x0	reserved
9:0	RW	0x000	vbp_lines This field configures the Vertical Back Porch period measured in horizontal lines.

MIPIC_Copy0 VID_VFP_LINES

Address: Operational Base + offset (0x0015c)

Bit	Attr	Reset Value	Description
31:10	RO	0x0	reserved
9:0	RW	0x000	vfp_lines This field configures the Vertical Front Porch period measured in horizontal lines.

MIPIC_Copy0 VID_VACTIVE_LINES

Address: Operational Base + offset (0x00160)

Bit	Attr	Reset Value	Description
31:14	RO	0x0	reserved
13:0	RW	0x0000	v_active_line This field configures the Vertical Active period measured in horizontal lines.

14.5 Application Notes

Low Power Mode is a special feature for D-PHY. You can control this function by using proper registers from the Innosilicon D-PHY with few operations. The following is a step by step instruction for low power mode in and out.

Perform the following steps to configure the DPI packet transmission:

Step1:Global configuration:

Configure n_lanes (PHY_IF_CFG-[1:0]) to define the number of lanes in which the controller has to perform high-speed transmissions.

Step2:Configure the DPI Interface to define how the DPI interface interacts with the controller.

Configure dpi_vid (DPI_CFG-[1:0]): This field configures the virtual channel that the packet generated by the DPI interface is indexed to.

Configure dpi_color_coding (DPI_CFG-[4:2]): This field configures the bits per pixels that the interface transmits and also the variant configuration of each bpp. If you select 18 bpp, and the Enable_18_loosely_packed is not active, the number or pixels per line should be a multiple of four.

Configure dataen_active_low (DPI_CFG-[5]): This bit configures the polarity of the dpidataen signal and enables if it is active low.

Configure vsync_active_low(DPI_CFG-[6]): This bit configures the polarity of the dpivsync signal and enables if it is active low.

Configure vsync_active_low(DPI_CFG-[7]): This bit configures the polarity of the dpivsync signal and enables if it is active low.

Configure vsync_active_low(DPI_CFG-[8]): This bit configures the polarity of the dpishutdn signal and enables if it is active low.

Configure vsync_active_low(DPI_CFG-[9]): This bit configures the polarity of the dpicolorm signal and enables if it is active low.

Configure en18_loosely(DPI_CFG-[10]): This bit configures if the pixel packing is done loosely or packed when dpi_color_coding is 18 bpp. This bit enables loosely packing.

Step3: Select the Video Transmission Mode to define how the processor requires the video line to be transported through the DSI link.

Configure low-power transitions (VID_MODE_CFG-[8:3]): This defines the video line to be transported through the DSI link.

Configure low-power transitions (VID_MODE_CFG-[8:3]): This defines the video periods which are permitted to go to low-power if there is available time to do so.

Configure frame_BTA_ack (VID_MODE_CFG-[11]): This specifies if the controller should request the peripheral acknowledge message at the end of frames.

Burst mode: In this mode, the entire active pixel line is buffered into a FIFO and transmitted in a single packed with no interruptions. This transmission mode requires that the DPI Pixel FIFO has the capacity to store a full line of active pixel data inside it. This mode is optimally used if the difference between pixel required bandwidth and DSI link bandwidth is very different. This enables the DWC_mipi_dsi_host to quickly dispatch the entire active video line in a single burst of data and then return to low-power mode.

Configure the register field vid_mode_type (VID_MODE_CFG-[10]), num_chunks (VID_PKT_CFG-[20:11]), and null_pkt_size (VID_PKT_CFG-[30:21]) are automatically ignored by the DWC_mipi_dsi_host.

Non-Burst mode: In this mode, the processor uses the partitioning properties of the DWC_mipi_dsi_host to divide the video line transmission into several DSI packets. This is done to match the pixel required bandwidth with the DSI link bandwidth. With this mode, the controller configuration does not require a full line of pixel data to be stored inside the DPI Pixel FIFO. It requires only the content of one video packet.

Configure the vid_mode_type field (VID_MODE_CFG-[2:1]) with 2'b0x.

Configure the vid_mode_type field (VID_MODE_CFG-[2:1]) with 2'b00x to enable the transmission of sync pulses.

Configure the vid_mode_type field (VID_MODE_CFG-[2:1]) with 2'b01 to enable the transmission of sync events.

Configure the vid_mode_type field (VID_MODE_CFG-[10:0]) with the number of pixels to be transmitted in a single packet.

Configure the en_multi_pkt field (VID_MODE_CFG-[9]) to enable the division of the active video transmission into more than one packet.

Configure the num_chunks field (VID_MODE_CFG-[20:11]) with the number of video chunks that the active video transmission is divided into.

Configure the en_null_pkt field (VID_MODE_CFG-[10]) to enable the insertion of null packets between video packets.

The field is effective only when en_multi_pkt field is activated, otherwise the controller ignores it and does not sent the null packets.

Configure the null_pkt_size field (VID_MODE_CFG-[30:21]) with the actual size of the inserted null packet.

Step4: Define the DPI Horizontal timing configuration as follows:

Configure the hline_time field (TMR_LINE_CFG-[31:18]) with the time taken by a DPI video line accounted in Clock Lane bytes clock cycles (for a clock lane at 500 MHz the Lane byte clock period is 8 ns). When the DPI clock and Clock Lane clock are not multiples, the hline_time is a result of a round of a number. If the DWC_mipi_dsi_host is configured to go to low-power, it is possible that the error included in a line is incremented with the next one. At the end of several lines, the DWC_mipi_dsi_host can have a number of errors that can cause a malfunction of the video transmission.

Configure the hsa_time field (TMR_LINE_CFG-[8:0]) with the time taken by a DPI Horizontal Sync Active period accounted in Clock Lane byte clock cycles (normally a period of 8ns).

Configure the hbp_time field (TMR_LINE_CFG-[17:9]) with the time taken by a DPI Horizontal Sync Active period accounted in Clock Lane byte clock cycles (normally a period of 8ns). Special attention should be given to the calculation of this parameter.

Step5: Define the Vertical line configuration:

Configure the vsa_lines field (VTIMING_CFG-[3:0]) with the number of lines existing in the DPI Vertical Sync Active period.

Configure the vbp_lines field (VTIMING_CFG-[9:4]) with the number of lines existing in the DPI Vertical Back Porch period.

Configure the vfp_lines field (VTIMING_CFG-[15:10]) with the number of lines existing in the DPI Vertical Front Porch period.

Configure the v_active_lines field (VTIMING_CFG-[26:16]) with the number of lines existing in the DPI Vertical Active period.

Chapter 15 Raster Graphic Acceleration (RGA)

15.1 Overview

RGA is a separate 2D raster graphic acceleration unit. It accelerates 2D graphics operations, such as point/line drawing, image scaling, rotation, BitBLT, alpha blending and image blur/sharpness.

15.1.1 Features

- **Data format**
 - Input data: ARGB/RGB888/RGB565/RGB4444/RGB5551/YUV420/YUV422
 - Output data: ARGB/RGB888/RGB565/RGB4444/RGB5551/YUV420/YUV422
 - Pixel Format conversion, BT.601/BT.709
 - Dither operation
 - Max resolution: 8192x8192 source, 4096x4096 destination
- **Scaling**
 - Down-scaling: Average filter
 - Up-scaling: Bi-cubic filter(source>2048 would use Bi-linear)
 - Arbitrary non-integer scaling ratio, from 1/16 to 16
- **Rotation**
 - 0, 90, 180, 270 degree rotation
 - x-mirror, y-mirror & rotation operation
- **BitBLT**
 - Block transfer
 - Color palette/Color fill, support with alpha
 - Transparency mode (color keying/stencil test, specified value/value range)
 - Two source BitBLT:
 - A+B=B only BitBLT, not support scale/rotate mode
 - A+B=C second source (B) has same attribute with (C) plus rotation function
- **Alpha Blending**
 - New comprehensive per-pixel alpha(color/alpha channel separately)
 - Fading
- **Raster operation**
 - ROP2/ROP3/ROP4
- **MMU**
 - 4k/64k page size
 - Four channel: SRC/SRC1/DST/CMD, individual base address and enable control bit
 - TLB pre-fetch

15.2 Block Diagram

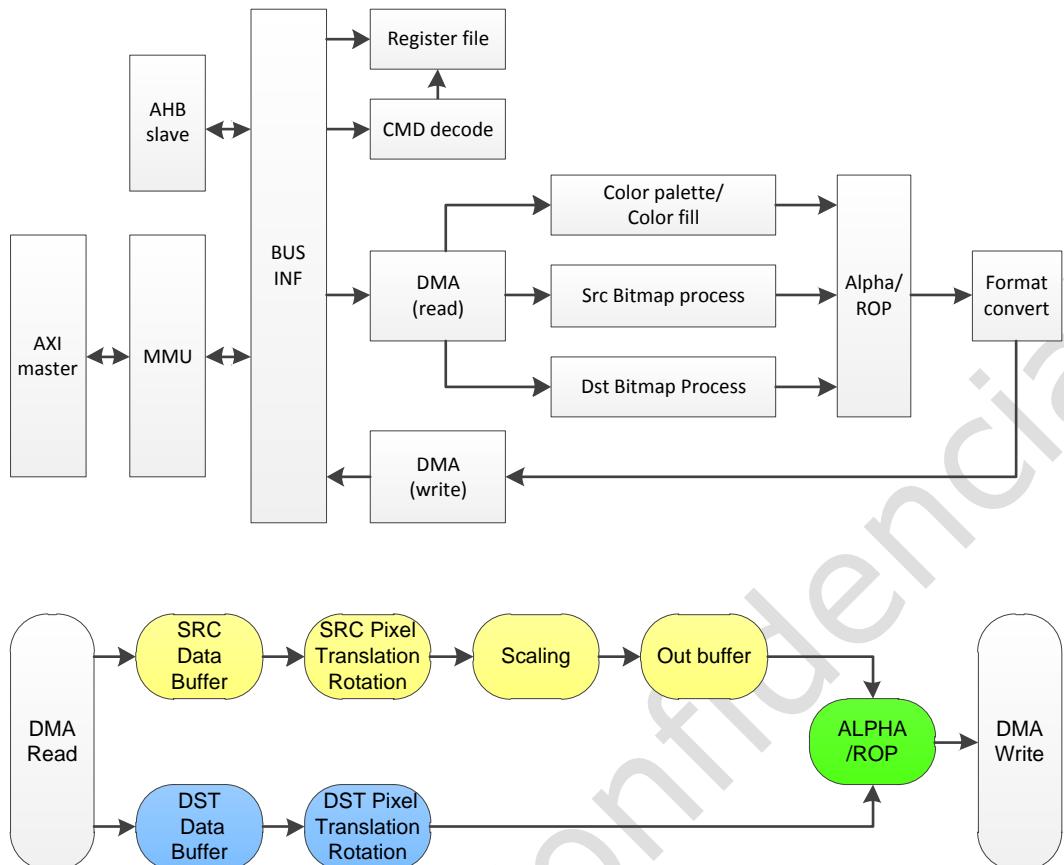


Fig. 15-1 RGA2 Block Diagram

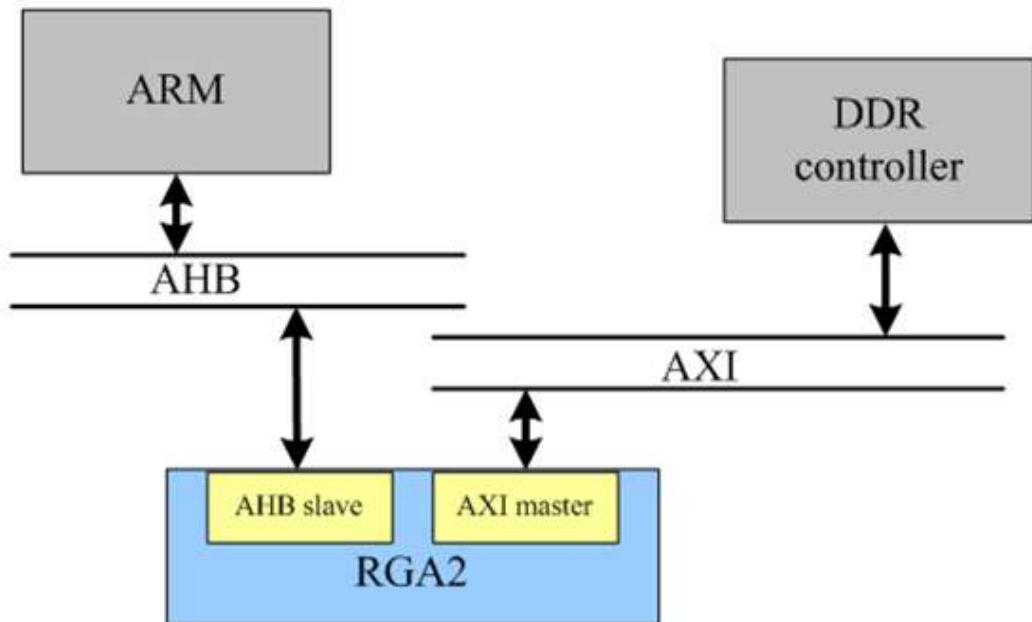


Fig. 15-2 RGA2 in SOC

15.3 Function Description

15.3.1 Data Format

RGB_565	15 R 11 G 5 B 0
ARGB_4444	15 A 12 R 8 G 4 B 0
RGBA_4444	15 R 12 G 8 B 4 A 0
ARGB_1555	15 A 14 R 10 G 5 B 0
RGBA_5551	15 R 11 G 6 B 1 A 0
ARGB_8888 XRGB_8888	31 A/X 24 R 16 G 8 B 0
BGRA_8888 BGRX_8888	31 B 24 G 16 R 8 A/X 0
ABGR_8888 XBGR_8888	31 A/X 24 B 16 G 8 R 0
RGBA_8888 RGBX_8888	31 R 24 G 16 B 8 A/X 0
RGB_888 packed	31 R1 24 B0 16 G0 8 R0 31 G2 24 R2 16 B1 8 G1 31 B3 24 G3 16 R3 8 B2
YCbCr422-SP YCbCr420-SP	31 Y03 24 Y02 16 Y01 8 Y00 31 Y07 24 Y06 16 Y05 8 Y04
	YCbCr422-P YCbCr420-P
	31 Cb03 24 Cr02 16 Y01 8 Y00 31 Cb07 24 Cr06 16 Y05 8 Y04
	Cb03 Cb02 Cb01 Cb00
	31 Cr03 24 Cr02 16 Cr1 8 Cr00

Fig. 15-3 RGA Input Data Format

All input datas (defined by SRC_IN_FMT/DST_IN_FMT) are converted to ABGR8888. The results are converted to the output data format (defined by DST_OUT_FMT).

15.3.2 Dithering

There could have dithering operation for source image when the source image format is not RGB565 and the destination format is RGB565.

The down-dithering is done using Dither Allegro.

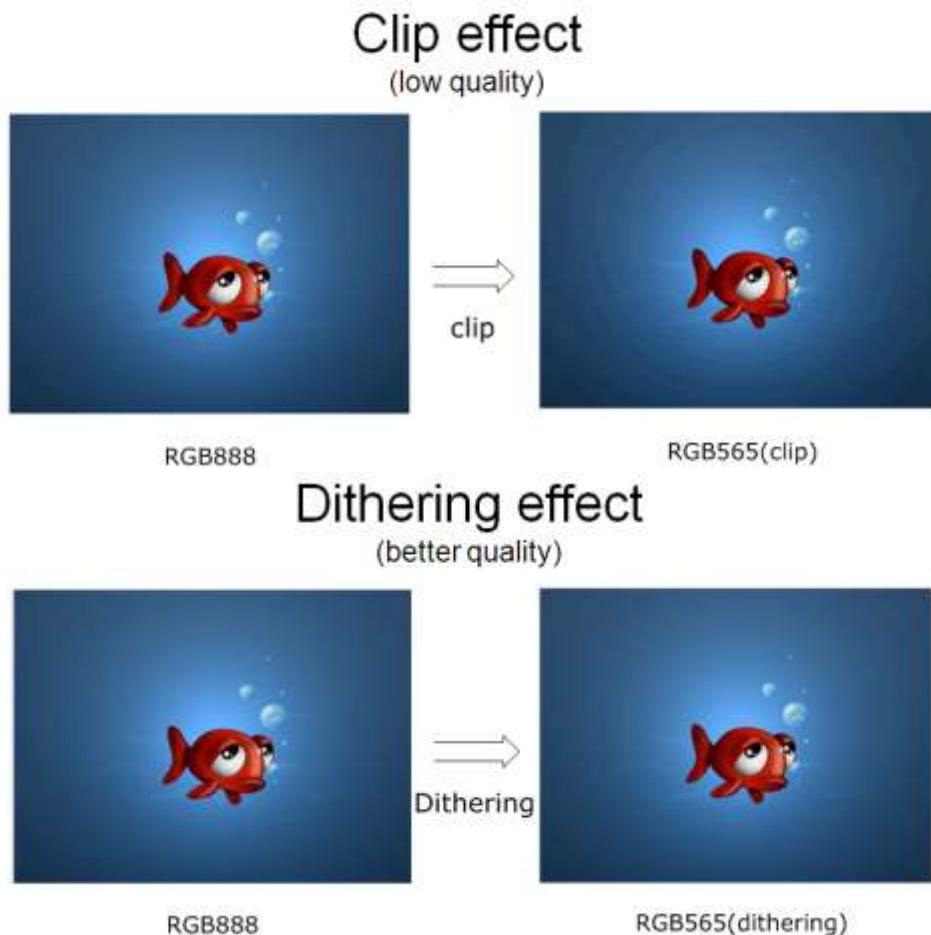
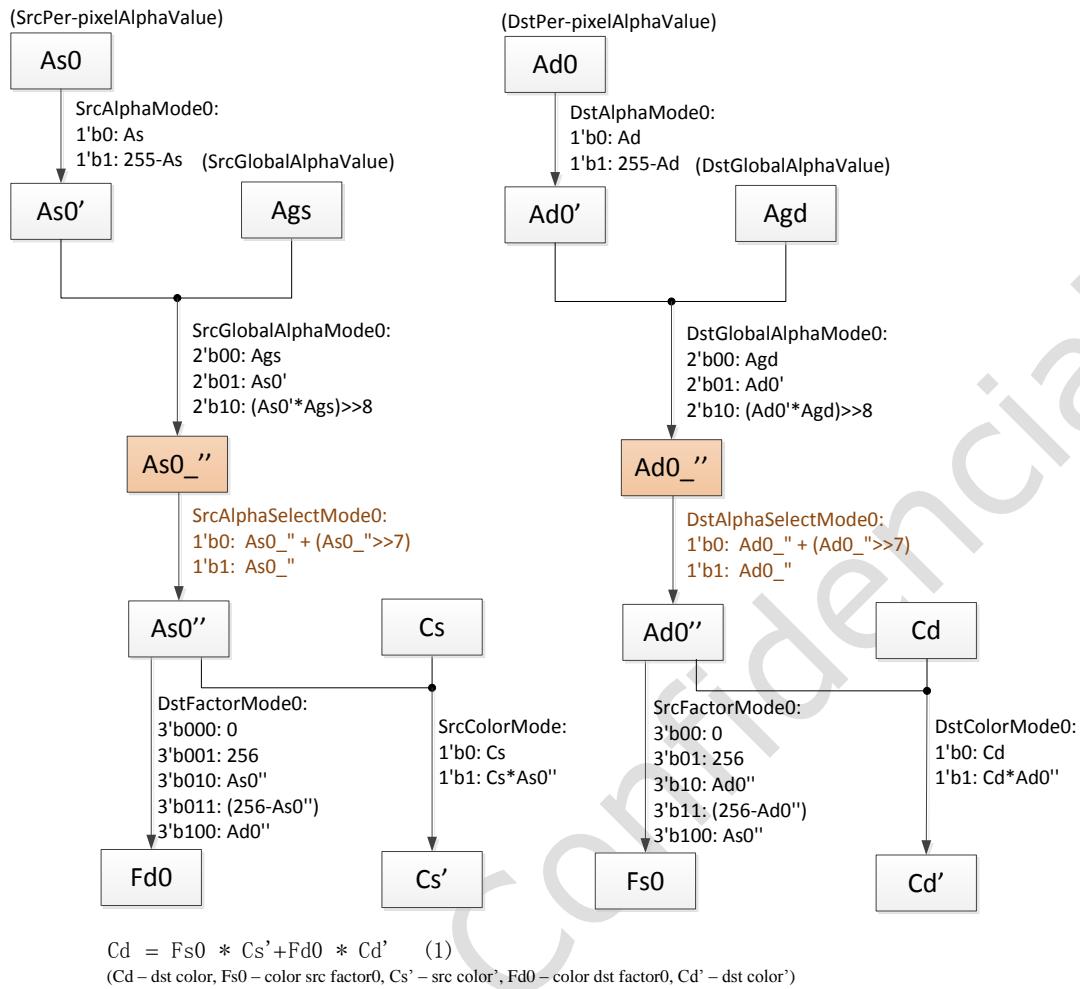
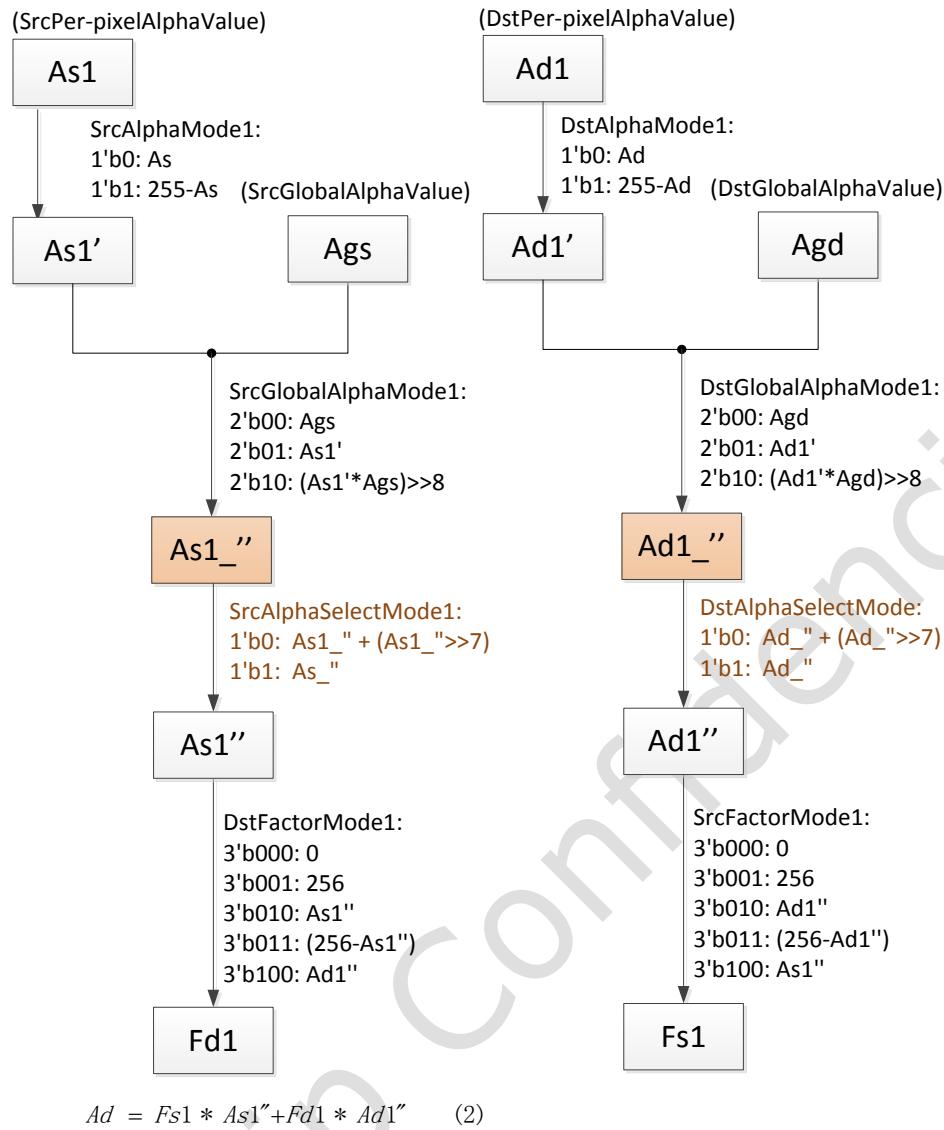


Fig. 15-4 RGA Dither effect

15.3.3 Alpha mode





15.3.4 Color fill

Two modes of color fill can be done by RGA: solid fill and gradient fill.

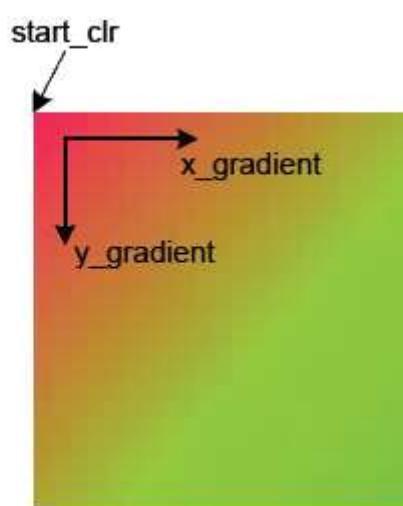


Fig. 15-5 RGA Gradient Fill

Gradient fill using following equations for ARGB calculation of every pixel in different coordinate.

```
A_cur = (A_start + x*x_A_gradient) +y*y_A_gradient;
R_cur = (R_start + x*x_R_gradient) +y*y_R_gradient;
G_cur = (G_start + x*x_G_gradient) +y*y_G_gradient;
B_cur = (B_start + x*x_B_gradient) +y*y_B_gradient;
```

A_start, R_start, G_start, B_start is the ARGB value of start point. There are four pairs of values for horizontal and vertical gradient. Saturation operation could be enabled or disabled if the color overflows 255 or underflows 0.

15.3.5 Raster Operation (ROP)

Raster operation (ROP) is a Boolean operation between operands, which involve AND, OR, XOR, and NOT operations. For ROP2, operands are P (select pattern) and D (Destination bitmap). For ROP3, operands are P (pattern), S (source bitmap) and D (Destination bitmap). For ROP4, operands are P (pattern), S (source bitmap), D (Destination bitmap) and MASK.

Table 15-1 RGA ROP Boolean operations

Operator	Meaning
a	Bitwise AND
n	Bitwise NOT (inverse)
o	Bitwise OR
x	Bitwise exclusive OR (XOR)

15.3.6 Scaling

The scaling operation is the imageresizing processing of source image. Scaling is done base on ARGB8888 format.

There are three sampling modes: scale down (Average); scale up(Bi-cubic);

15.4 Register description

15.4.1 Register Summary

Name	Offset	Size	Reset Value	Description
RGA2_RGA_SYS_CTRL	0x0000	W	0x00000004	RGA system control register
RGA2_RGA_CMD_CTRL	0x0004	W	0x00000000	RGA command control register
RGA2_RGA_CMD_BASE	0x0008	W	0x12345678	RGA command codes base address register
RGA2_RGA_STATUS	0x000c	W	0x00000000	RGA status register
RGA2_RGA_INT	0x0010	W	0x00000000	RGA interrupt register
RGA2_RGA_MMU_CTRL0	0x0014	W	0x00000000	RGA MMU control 0 register
RGA2_RGA_MMU_CMD_BASE	0x0018	W	0x00000000	Register0000 Abstract
RGA2_RGA_MODE_CTRL	0x0100	W	0x00000000	RGA mode control register
RGA2_RGA_SRC_INFO	0x0104	W	0x00000000	RGA source information register
RGA2_RGA_SRC_BASE0	0x0108	W	0x00000000	source image Y/RGB base address
RGA2_RGA_SRC_BASE1	0x010c	W	0x00000000	RGA source image Cb/Cbr base address register
RGA2_RGA_SRC_BASE2	0x0110	W	0x00000000	RGA source image Cr base address register

Name	Offset	Size	Reset Value	Description
RGA2_RGA_SRC_BASE3	0x0114	W	0x00000000	RGA source image 1 base address register
RGA2_RGA_SRC_VIR_INFO	0x0118	W	0x00000000	RGA source image virtual stride / RGA source image tile number
RGA2_RGA_SRC_ACT_INFO	0x011c	W	0x00000000	RGA source image active width/height register
RGA2_RGA_SRC_X_FACTOR	0x0120	W	0x00000000	RGA source image horizontal scaling factor
RGA2_RGA_SRC_Y_FACTOR	0x0124	W	0x00000000	RGA source image vertical scaling factor
RGA2_RGA_SRC_BG_COLOR	0x0128	W	0x00000000	RGA source image background color
RGA2_RGA_SRC_FG_COLOR	0x012c	W	0x00000000	RGA source image foreground color
RGA2_RGA_CP_GR_A	0x0130	W	0x00000000	RGA source image transparency color min value
RGA2_RGA_SRC_TR_COLOR0	0x0130	W	0x00000000	RGA source image transparency color min value
RGA2_RGA_CP_GR_B	0x0134	W	0x00000000	RGA source image transparency color max value
RGA2_RGA_SRC_TR_COLOR1	0x0134	W	0x00000000	Register0000 Abstract
RGA2_RGA_DST_INFO	0x0138	W	0x00000000	RGA destination format register
RGA2_RGA_DST_BASE0	0x013c	W	0x00000000	RGA destination image base address 0 register
RGA2_RGA_DST_BASE1	0x0140	W	0x00000000	RGA destination image base address 1 register
RGA2_RGA_DST_BASE2	0x0144	W	0x00000000	RGA destination image base address 2 register
RGA2_RGA_DST_VIR_INFO	0x0148	W	0x00000000	RGA destination image virtual width/height register
RGA2_RGA_DST_ACT_INFO	0x014c	W	0x00000000	RGA destination image active width/height register
RGA2_RGA_ALPHA_CTRL0	0x0150	W	0x00000000	Alpha control register 0
RGA2_RGA_ALPHA_CTRL1	0x0154	W	0x00000000	Register0000 Abstract
RGA2_RGA_FADE_CTRL	0x0158	W	0x00000000	Fading control register
RGA2_RGA_PAT_CON	0x015c	W	0x00000000	Pattern size/offset register
RGA2_RGA_CP_GR_G	0x0160	W	0x00000000	RGA color gradient fill step register (color fill mode)
RGA2_RGA_ROP_CON0	0x0160	W	0x00000000	ROP code 0 control register
RGA2_RGA_CP_GR_R	0x0164	W	0x00000000	RGA color gradient fill step register (color fill mode)
RGA2_RGA_ROP_CON1	0x0164	W	0x00000000	ROP code 1 control register
RGA2_RGA_MASK_BASE	0x0168	W	0x00000000	RGA mask base address register
RGA2_RGA_MMU_CTRL1	0x016c	W	0x00000000	RGA MMU control register 1

Name	Offset	Size	Reset Value	Description
RGA2_RGA_MMU_SRC_BASE	0x0170	W	0x00000000	RGA source MMU TLB base address
RGA2_RGA_MMU_SRC1_BASE	0x0174	W	0x00000000	RGA source1 MMU TLB base address
RGA2_RGA_MMU_DST_BASE	0x0178	W	0x00000000	RGA destination MMU TLB base address
RGA2_RGA_MMU_ELS_BASE	0x017c	W	0x00000000	RGA ELSE MMU TLB base address

Notes: Size : **B** - Byte (8 bits) access, **HW** - Half WORD (16 bits) access, **W** - WORD (32 bits) access

15.4.2 Detail Register Description

RGA2_RGA_SYS_CTRL

Address: Operational Base + offset (0x0000)

RGA system control register

Bit	Attr	Reset Value	Description
31:6	RO	0x0	reserved
5	RW	0x0	sw_auto_RST it would auto-resetn after one frame finish. 0: disable 1: enable
4	RW	0x0	sw_cclk_sreset_p RGA core clk domain Soft reset, write '1' to this would reset the RGA engine except config registers.
3	WO	0x0	sw_aclk_sreset_p RGA aclk domain Soft reset, write '1' to this would reset the RGA engine except config registers.
2	WO	0x1	sw_auto_ckg RGA auto clock gating enable bit 0: disable 1: enable
1	WO	0x0	sw_cmd_mode RGA command mode 0: slave mode 1: master mode
0	WO	0x0	sw_cmd_op_st_p RGA operation start bit Only used in passive (slave) control mode

RGA2_RGA_CMD_CTRL

Address: Operational Base + offset (0x0004)

RGA command control register

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:13	RO	0x0	reserved
12:3	RW	0x000	sw_cmd_incr_num RGA command increment number
2	WO	0x0	sw_cmd_stop RGA command stop mode Command execution would stop after the current graphic operation finish if set this bit to 1
1	WO	0x0	sw_cmd_incr_valid_p RGA command increment valid (Auto cleared) When setting this bit, 1. The total cmd number would increase by the RGA_INCR_CMD_NUM. 2. RGA would continue running if idle.
0	RW	0x0	sw_cmd_line_st_p RGA command line fetch start (command line reset) (Auto cleared) When fetch start, the total cmd number would reset to RGA_INCR_CMD_NUM.

RGA2_RGA_CMD_BASE

Address: Operational Base + offset (0x0008)

RGA command codes base address register

Bit	Attr	Reset Value	Description
31:0	RW	0x12345678	sw_cmd_base RGA command codes base address

RGA2_RGA_STATUS

Address: Operational Base + offset (0x000c)

RGA status register

Bit	Attr	Reset Value	Description
31:20	RO	0x000	sw_cmd_total_num RGA command total number
19:8	RO	0x000	sw_cmd_cur_num RGA command current number
7:1	RW	0x00	Reserved Reserved
0	RO	0x0	sw_rga_sta RGA engine status 0: idle 1: working

RGA2_RGA_INT

Address: Operational Base + offset (0x0010)

RGA interrupt register

Bit	Attr	Reset Value	Description
31:11	RO	0x0	reserved
10	RW	0x0	sw_intr_af_e All command finished interrupt enable
9	RW	0x0	sw_intr_mmu_e MMU interrupt enable
8	RW	0x0	sw_intr_err_e Error interrupt enable
7	WO	0x0	sw_intr_cf_clr Current command finished interrupt clear
6	WO	0x0	sw_intr_af_clr All command finished interrupt clear
5	WO	0x0	sw_intr_mmu_clr MMU interrupt clear
4	WO	0x0	sw_intr_err_clr Error interrupt clear
3	RO	0x0	sw_intr_cf Current command finished interrupt flag
2	RO	0x0	sw_intr_af All command finished interrupt flag
1	RO	0x0	sw_intr_mmu MMU interrupt
0	RO	0x0	sw_intr_err Error interrupt flag

RGA2_RGA_MMU_CTRL0

Address: Operational Base + offset (0x0014)

RGA MMU control 0 register

Bit	Attr	Reset Value	Description
31:11	RW	0x000000	Reserved
10:9	RW	0x0	sw_els_ch_priority
8:7	RW	0x0	sw_dst_ch_priority
6:5	RW	0x0	sw_src1_ch_priority
4:3	RW	0x0	sw_src_ch_priority
2	RW	0x0	sw_cmd_mmu_flush RGA CMD channel MMU TLB flush: Set 1 to this bit to flush MMU TLB, auto clear
1	RW	0x0	sw_cmd_mmu_en RGA CMD channel MMU enable 0: disable 1: enable
0	RW	0x0	sw_mmu_page_size RGA MMU Page table size 0: 4KB page 1: 64KB page

RGA2_RGA_MMU_CMD_BASE

Address: Operational Base + offset (0x0018)

Register0000 Abstract

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:0	RW	0x0000000	sw_mmu_cmd_base RGA command MMU TLB base address (word)

RGA2_RGA_MODE_CTRL

Address: Operational Base + offset (0x0100)

RGA mode control register

Bit	Attr	Reset Value	Description
31:8	RW	0x000000	Reserved
7	RW	0x0	sw_intr_cf_e Current command finished interrupt enable
6	RW	0x0	sw_gradient_sat Gradient saturation calculation mode 0:clip 1:not-clip
5	RW	0x0	sw_alpha_zero_key ARGB888 alpha zero key mode 0x000000 would be changed to 0x000100(RGB888)/0x0020(RGB565)for ARGB888 to RGBX/RGB565 color key 0: disable 1: enable
4	RW	0x0	sw_cf_rop4_pat Color fill/ROP4 pattern 0: solid color 1: pattern color
3	RW	0x0	sw_bb_mode Bitblt mode 0: SRC + DST => DST 1: SRC + SRC1 => DST
2:0	RW	0x0	sw_render_mode RGA 2D render mode 000: Bitblt 001: Color palette 010: Rectangle fill 011: Update palette LUT/pattern ram

RGA2_RGA_SRC_INFO

Address: Operational Base + offset (0x0104)

RGA source information register

Bit	Attr	Reset Value	Description
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Bit	Attr	Reset Value	Description
31:26	RW	0x00	Reserved
25:24	RW	0x0	<p>sw_bic_coe_sel SRC bicubic scaling coefficient select 00: CATROM 01: MITCHELL 10: HERMITE 11: B-SPLINE</p>
23	RW	0x0	<p>sw_src_dither_up SRC dither up enable 0:disable 1:enable</p>
22:19	RW	0x0	<p>sw_src_trans_e Source transparency enable bits [3]: A value stencil test enable bit [2]: B value stencil test enable bit [1]: G value stencil test enable bit [0]: R value stencil test enable bit</p>
18	RW	0x0	<p>sw_src_trans_mode Source transparency mode 0: normal stencil test (color key) 1: inverted stencil test</p>
17:16	RW	0x0	<p>sw_src_vscl_mode SRC vertical scaling mode 00: no scaling 01: down-scaling 10: up-scaling</p>
15:14	RW	0x0	<p>sw_src_hscl_mode SRC horizontal scaling mode 00: no scaling 01: down-scaling 10: up-scaling</p>
13:12	RW	0x0	<p>sw_src_mir_mode SRC mirror mode 00: no mirror 01: x mirror 10: y mirror 11: x mirror + y mirror</p>
11:10	RW	0x0	<p>sw_src_rot_mode SRC rotation mode 00: 0 degree 01: 90 degree 10: 180 degree 11: 270 degree</p>

Bit	Attr	Reset Value	Description
9:8	RW	0x0	sw_src_csc_mode Source bitmap YUV2RGB conversion mode 00: bypass 01: BT.601-range0 10: BT.601-range1 11: BT.709-range0
7	RW	0x0	sw_cp_endian Source Color palette endian swap 0: big endian 1: little endian
6	RW	0x0	sw_src_uvswap Source Cb-Cr swap 0: CrCb 1: CbCr
5	RW	0x0	sw_src_alpha_swap Source bitmap data alpha swap 0: ABGR 1: BGRA
4	RW	0x0	sw_src_rbswap Source bitmap data RB swap 0: BGR 1: RGB
3:0	RW	0x0	sw_src_fmt Source bitmap data format 0000: ABGR888 0001: XBGR888 0010: BGR packed 0100: RGB565 0101: ARGB1555 0110: ARGB4444 1000: YUV422SP 1001: YUV422P 1010: YUV420SP 1011: YUV420P 1100: 1BPP (color palette) 1101: 2BPP (color palette) 1110: 4BPP (color palette) 1111: 8BPP (color palette)

RGA2_RGA_SRC_BASE0

Address: Operational Base + offset (0x0108)

source image Y/RGB base address

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_src_base0 source image Y/RGB base address

RGA2_RGA_SRC_BASE1

Address: Operational Base + offset (0x010c)

RGA source image Cb/Cbr base address register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_src_base1 source image Cb base address (YUV422/420-P) source image Cb/Cr base address (YUV422/420-SP)

RGA2_RGA_SRC_BASE2

Address: Operational Base + offset (0x0110)

RGA source image Cr base address register

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	sw_src_base2 source image Cr base address (YUV422/420-P)

RGA2_RGA_SRC_BASE3

Address: Operational Base + offset (0x0114)

RGA source image 1 base address register

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	sw_src_base3 source image 1 RGB base address (source bitblt mode1)

RGA2_RGA_SRC_VIR_INFO

Address: Operational Base + offset (0x0118)

RGA source image virtual stride / RGA source image tile number

Bit	Attr	Reset Value	Description
31:26	RW	0x00	Reserved
25:16	RW	0x000	sw_mask_vir_stride mask image virtual stride (words)
15	RW	0x0	Reserved
14:0	RW	0x0000	sw_src_act_width source image active width count from 1

RGA2_RGA_SRC_ACT_INFO

Address: Operational Base + offset (0x011c)

RGA source image active width/height register

Bit	Attr	Reset Value	Description
31:29	RW	0x0	Reserved2

Bit	Attr	Reset Value	Description
28:16	RW	0x0000	sw_src_act_height source image active height
15:13	RW	0x0	Reserved1
12:0	RW	0x0000	sw_src_act_width source image active width

RGA2_RGA_SRC_X_FACTOR

Address: Operational Base + offset (0x0120)

RGA source image horizontal scaling factor

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	sw_src_hsp_factor Source image horizontal up-scaling factor $=(DST_ACT_WIDTH/SRC_ACT_WIDTH) * 65536$
15:0	RW	0x0000	sw_src_hsd_factor Source image horizontal down-scaling factor $=(SRC_ACT_WIDTH/DST_ACT_WIDTH) * 65536$

RGA2_RGA_SRC_Y_FACTOR

Address: Operational Base + offset (0x0124)

RGA source image vertical scaling factor

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	sw_src_vsp_factor Source image vertical up-scaling factor $(DST_ACT_HEIGHT/SRC_ACT_HEIGHT) * 65536$
15:0	RW	0x0000	sw_src_vsd_factor Source image vertical down-scaling factor $(SRC_ACT_HEIGHT/DST_ACT_HEIGHT) * 65536$

RGA2_RGA_SRC_BG_COLOR

Address: Operational Base + offset (0x0128)

RGA source image background color

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_src_bg_color Source image background color ("0" bit color for mono expansion.)

RGA2_RGA_SRC_FG_COLOR

Address: Operational Base + offset (0x012c)

RGA source image foreground color

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_src_fg_color Source image foreground color Source image foreground color ("1" bit color for mono expansion.) Color fill color, Pan color

RGA2_RGA_CP_GR_A

Address: Operational Base + offset (0x0130)

RGA source image transparency color min value

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	sw_gradient_y_a Y gradient value of Alpha (signed 8.8)
15:0	RW	0x0000	sw_gradient_x_a X gradient value of Alpha (signed 8.8)

RGA2_RGA_SRC_TR_COLOR0

Address: Operational Base + offset (0x0130)

RGA source image transparency color min value

Bit	Attr	Reset Value	Description
31:24	RW	0x00	sw_src_trans_amin source image transparency color A min value
23:16	RW	0x00	sw_src_trans_bmin source image transparency color B min value
15:8	RW	0x00	sw_src_trans_gmin source image transparency color G min value
7:0	RW	0x00	sw_src_trans_rmin source image transparency color R min value

RGA2_RGA_CP_GR_B

Address: Operational Base + offset (0x0134)

RGA source image transparency color max value

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	sw_gradient_y_b Y gradient value of Blue (signed 8.8)
15:0	RW	0x0000	sw_gradient_x_b X gradient value of Blue (signed 8.8)

RGA2_RGA_SRC_TR_COLOR1

Address: Operational Base + offset (0x0134)

Register0000 Abstract

Bit	Attr	Reset Value	Description
31:24	RW	0x00	sw_src_trans_amax source image transparency color A max value

Bit	Attr	Reset Value	Description
23:16	RW	0x00	sw_src_trans_bmax source image transparency color B max value
15:8	RW	0x00	sw_src_trans_gmax source image transparency color G max value
7:0	RW	0x00	sw_src_trans_rmax source image transparency color R max value

RGA2_RGA_DST_INFO

Address: Operational Base + offset (0x0138)

RGA destination format register

Bit	Attr	Reset Value	Description
31:19	RW	0x0000	Reserved
18	RW	0x0	sw_dst_csc_clip BGR2YUV Clip mode(from 0~255 clip to 36~235) 1: clip enable; 0: unclip
17:16	RW	0x0	sw_dst_csc_mode DST bitmap RGB2YUV conversion mode 00: Bypass 01: BT.601-range0 10: BT.601-range1 11: BT.709-range0
15:14	RW	0x0	sw_dither_mode DST dither down bit mode 00: 888 to 666 01: 888 to 565 10: 888 to 555 11: 888 to 444
13	RW	0x0	sw_dither_down DST dither down enable 0:disable 1:enable
12	RW	0x0	sw_src1_dither_up DST/SRC1 dither up enable 0:disable 1:enable
11	RW	0x0	sw_src1_alpha_swap Source 1 bitmap data alpha swap 0: ABGR 1: BGRA
10	RW	0x0	sw_src1_rbswap Source 1 bitmap data RB swap 0: BGR 1: RGB

Bit	Attr	Reset Value	Description
9:7	RW	0x0	sw_src1_fmt Source 1 bitmap data format 000: ABGR888 001: XBGR888 010: BGR packed 100: RGB565 101: ARGB1555 110: ARGB4444
6	RW	0x0	sw_dst_uvswap Destination Cb-Cr swap 0: CrCb 1: CbCr
5	RW	0x0	sw_dst_alpha_swap Destination bitmap data alpha swap 0: ABGR 1: BGRA
4	RW	0x0	sw_dst_rbswap Destination bitmap data RB swap 0: BGR 1: RGB
3:0	RW	0x0	sw_dst_fmt Destination bitmap data format 0000: ABGR888 0001: XBGR888 0010: BGR packed 0100: RGB565 0101: ARGB1555 0110: ARGB4444 1000: YUV422SP 1001: YUV422P 1010: YUV420SP 1011: YUV420P

RGA2_RGA_DST_BASE0

Address: Operational Base + offset (0x013c)

RGA destination image base address 0 register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_dst_base0 destination image Y/RGB base address

RGA2_RGA_DST_BASE1

Address: Operational Base + offset (0x0140)

RGA destination image base address 1 register

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_dst_base1 destination image Cb/CbCr base address

RGA2_RGA_DST_BASE2

Address: Operational Base + offset (0x0144)

RGA destination image base address 2 register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_dst_base2 destination image Cr base address

RGA2_RGA_DST_VIR_INFO

Address: Operational Base + offset (0x0148)

RGA destination image virtual width/height register

Bit	Attr	Reset Value	Description
31:28	RW	0x0	Reserved2
30:16	RW	0x000	sw_src1_vir_stride source image 1 virtual stride (words)
15:12	RW	0x0	Reserved1
14:0	RW	0x000	sw_dst_vir_stride destination image virtual stride(words)

RGA2_RGA_DST_ACT_INFO

Address: Operational Base + offset (0x014c)

RGA destination image active width/height register

Bit	Attr	Reset Value	Description
31:28	RW	0x0	Reserved2
27:16	RW	0x000	sw_dst_act_height Destination image active height
15:12	RW	0x0	Reserved1
11:0	RW	0x000	sw_dst_act_width Destination image active width

RGA2_RGA_ALPHA_CTRL0

Address: Operational Base + offset (0x0150)

Alpha control register 0

Bit	Attr	Reset Value	Description
31:21	RW	0x000	Reserved
20	RW	0x0	sw_mask_endian ROP4 mask endian swap 0: big endian 1: little endian
19:12	RW	0x00	sw_dst_global_alpha global alpha value of DST(Agd)

Bit	Attr	Reset Value	Description
11:4	RW	0x00	sw_src_global_alpha global alpha value of SRC(Ags) fading value in fading mod
3:2	RW	0x0	sw_rop_mode ROP mode select 00: ROP 2 01: ROP 3 10: ROP 4
1	RW	0x0	sw_alpha_rop_sel Alpha or ROP select 0: alpha 1: ROP
0	RW	0x0	sw_alpha_rop_e Alpha or ROP enable 0: disable 1: enable

RGA2_RGA_ALPHA_CTRL1

Address: Operational Base + offset (0x0154)

Register0000 Abstract

Bit	Attr	Reset Value	Description
31:30	RW	0x0	Reserved Reserved
29	RW	0x0	sw_src_alpha_m1 Src Transparent/opaque of alpha channel (As1') 0: As 1: 255-As
28	RW	0x0	sw_dst_alpha_m1 Dst Transparent/opaque of alpha channel (Ad1') 0: Ad 1: 255-Ad
27:26	RW	0x0	sw_src_blend_m1 Alpha src blend mode select of alpha channel (As1_) 00: Ags 01: As1' 10: (As1'*Ags)>>8 11: reserved

Bit	Attr	Reset Value	Description
25:24	RW	0x0	sw_dst_blend_m1 Alpha dst blend mode select of alpha channel(Ad1_) 00: Agd 01: Ad1' 10: (Ad1'*Agd)>>8 11: reserved
23	RW	0x0	sw_src_alpha_cal_m1 Alpha src calculate mode of alpha channel(As1") 0: As1"= As1_"+ (As1_>>7) 1: As1"= As1_"
22	RW	0x0	sw_dst_alpha_cal_m1 Alpha dst calculate mode of alpha channel(Ad1") 0: Ad1"= Ad1_ + (Ad1_>>7) 1: Ad1"= Ad1_"
21:19	RW	0x0	w_src_factor_m1 Src factore mode of alpha channel(Fs1) 000: 0 001: 256 010: Ad1" 011: 256-Ad1" 100: As1"
18:16	RW	0x0	sw_dst_factor_m1 Dst factore mode of alpha channel(Fd1) 000: 0 001: 256 010: As1" 011: 256-As1" 100: Ad1"
15	RW	0x0	sw_src_alpha_m0 Src Transparent/opaque of color channel (As0') 0: As 1: 255-As
14	RW	0x0	sw_dst_alpha_m0 Dst Transparent/opaque of color channel (Ad0') 0: Ad 1: 255-Ad

Bit	Attr	Reset Value	Description
13:12	RW	0x0	sw_src_blend_m0 Alpha src blend mode select of color channel (As0_) 00: Ags 01: As0' 10: (As0'*Ags)>>8 11: reserved
11:10	RW	0x0	sw_dst_blend_m0 Alpha dst blend mode select of color channel(Ad0_) 00: Agd 01: Ad0' 10: (Ad0'*Agd)>>8 11: reserved
9	RW	0x0	sw_src_alpha_cal_m0 Alpha src calculate mode of color channel(As0") 0: As0"= As0_ + (As0_>>7) 1: As0"= As0_
8	RW	0x0	sw_dst_alpha_cal_m0 Alpha dst calculate mode of color channel(Ad0") 0: Ad0"= Ad0_ + (Ad0_>>7) 1: Ad0"= Ad0_
7:5	RW	0x0	sw_src_factor_m0 Src factore mode of color channel(Fs0) 000: 0 001: 256 010: Ad0" 011: 256-Ad0" 100: As0"
4:2	RW	0x0	sw_dst_factor_m0 Dst factore mode of color channel(Fd0) 000: 0 001: 256 010: As0" 011: 256-As0" 100: Ad0"
1	RW	0x0	sw_src_color_m0 SRC color select(Cs') 0: Cs 1: Cs * As0"

Bit	Attr	Reset Value	Description
0	RW	0x0	sw_dst_color_m0 SRC color select(Cd') 0: Cd 1: Cd * Ad0''

RGA2_RGA_FADING_CTRL

Address: Operational Base + offset (0x0158)

Fading control register

Bit	Attr	Reset Value	Description
31:25	RW	0x00	Reserved
24	RW	0x0	sw_fading_en Fading enable
23:16	RW	0x00	sw_fading_offset_b Fading offset B value
15:8	RW	0x00	sw_fading_offset_g Fading offset G value (Pattern total number when pattern loading)
7:0	RW	0x00	sw_fading_offset_r Fading offset R value (Start point of pattern ram in pattern mode)

RGA2_RGA_PAT_CON

Address: Operational Base + offset (0x015c)

Pattern size/offset register

Bit	Attr	Reset Value	Description
31:24	RW	0x00	sw_pat_offset_y Pattern y offset
23:16	RW	0x00	sw_pat_offset_x Pattern x offset
15:8	RW	0x00	sw_pat_height Pattern height
7:0	RW	0x00	sw_pat_width Pattern width

RGA2_RGA_CP_GR_G

Address: Operational Base + offset (0x0160)

RGA color gradient fill step register (color fill mode)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	sw_gradient_y_g Y gradient value of Green (signed 8.8)
15:0	RW	0x0000	sw_gradient_x_g X gradient value of Green (signed 8.8)

RGA2_RGA_ROP_CON0

Address: Operational Base + offset (0x0160)

ROP code 0 control register

Bit	Attr	Reset Value	Description
31:25	RW	0x00	Reserved
24:0	RW	0x00000000	sw_rop3_code0 Rop3 code 0 control bits

RGA2_RGA_CP_GR_R

Address: Operational Base + offset (0x0164)

RGA color gradient fill step register (color fill mode)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	sw_gradient_y_r Y gradient value of Red(signed 8.8)
15:0	RW	0x0000	sw_gradient_x_r X gradient value of Red(signed 8.8)

RGA2_RGA_ROP_CON1

Address: Operational Base + offset (0x0164)

ROP code 1 control register

Bit	Attr	Reset Value	Description
31:25	RW	0x00	Reserved
24:0	RW	0x00000000	sw_rop3_code1 Rop3 code 1 control bits

RGA2_RGA_MASK_BASE

Address: Operational Base + offset (0x0168)

RGA mask base address register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_mask_base mask base address in ROP4 mode LUT/ pattern load base address

RGA2_RGA_MMU_CTRL1

Address: Operational Base + offset (0x016c)

RGA MMU control register 1

Bit	Attr	Reset Value	Description
31:14	RW	0x00000	Reserved
13	RW	0x0	sw_els_mmuv_flush RGA ELSE channel MMU TLB flush: Set 1 to this bit to flush MMU TLB, auto clear
12	RW	0x0	sw_els_mmuv_en RGA ELSE channel MMU enable 0: disable 1: enable

Bit	Attr	Reset Value	Description
11	RW	0x0	sw_dst_mmu_prefetch_dir 0:forward 1:backward
10	RW	0x0	sw_dst_mmu_prefetch_en 0:disable 1:enable
9	RW	0x0	sw_dst_mmu_flush RGA DST channel MMU TLB flush: Set 1 to this bit to flush MMU TLB, auto clear
8	RW	0x0	sw_dst_mmu_en RGA DST channel MMU enable 0: disable 1: enable
7	RW	0x0	sw_src1_mmu_prefetch_dir 0:forward 1:backward
6	RW	0x0	sw_src1_mmu_prefetch_en 0:disable 1:enable
5	RW	0x0	sw_src1_mmu_flush RGA SRC1 channel MMU TLB flush: Set 1 to this bit to flush MMU TLB, auto clear
4	RW	0x0	sw_src1_mmu_en RGA SRC1 channel MMU enable 0: disable 1: enable
3	RW	0x0	sw_src_mmu_prefetch_dir 0:forward 1:backward
2	RW	0x0	sw_src_mmu_prefetch_en 0:disable 1:enable
1	RW	0x0	sw_src_mmu_flush RGA SRC channel MMU TLB flush: Set 1 to this bit to flush MMU TLB, auto clear
0	RW	0x0	sw_src_mmu_en RGA SRC channel MMU enable 0: disable 1: enable

RGA2_RGA_MMU_SRC_BASE

Address: Operational Base + offset (0x0170)

RGA source MMU TLB base address

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved

Bit	Attr	Reset Value	Description
27:0	RW	0x0000000	sw_mmu_src_base RGA source MMU TLB base address (128-bit)

RGA2_RGA_MMU_SRC1_BASE

Address: Operational Base + offset (0x0174)

RGA source1 MMU TLB base address

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:0	RW	0x0000000	sw_mmu_src1_base RGA source1 MMU TLB base address (128-bit)

RGA2_RGA_MMU_DST_BASE

Address: Operational Base + offset (0x0178)

RGA destination MMU TLB base address

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:0	RW	0x0000000	sw_mmu_dst_base RGA destination MMU TLB base address (128-bit)

RGA2_RGA_MMU_ELS_BASE

Address: Operational Base + offset (0x017C)

RGA ELSE MMU TLB base address

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:0	RW	0x0000000	sw_mmu_els_base RGA destination MMU TLB base address (128-bit)

15.5 Programming Guide**15.5.1 Register Partition**

There are two types of register in RGA. The first 8 registers (0x0 - 0x1C) are general registers for system configuration including command mode, command parameter, RGA status, general interrupts. The other registers (from 0x100) are command registers for command codes.

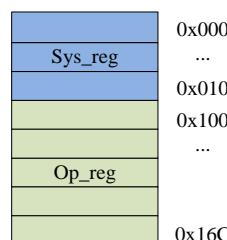


Fig. 15-6 HDMI TX Software Main Sequence Diagram

15.5.2 Command Modes

RGA has two command modes: slave mode and master mode. In slave mode (`RGA_SYS_CTRL[1] = 1'b0`), 2D graphic command only could be run one by one. CPU set all the command registers in RGA and then start RGA running by setting `RGA_SYS_CTRL[1]` to '1'. In master mode (`RGA_SYS_CTRL[1] = 1'b1`), 2D graphic commands could be run sequentially. After setting command's number to `RGA_CMD_CTRL[12:3]`, writing '1' to `RGA_CMD_CTRL[0]` will start the command fetch, then Internal command DMA fetch commands from external command line.

Command line is a collection of several command codes with continuous address. At the first start, the command start address (`RGA_CMD_ADDR`) and command number (`RGA_CMD_CTRL[12:3]`) should be set, then write '1' to `cmd_line_st` (`RGA_CMD_CTRL[0]`) to start the command line fetch. Incremental command is supported by setting `cmd_incr_num` (`RGA_CMD_CTRL[12:3]`) and `cmd_incr_valid` (`RGA_CMD_CTRL[1]=1'b1`)

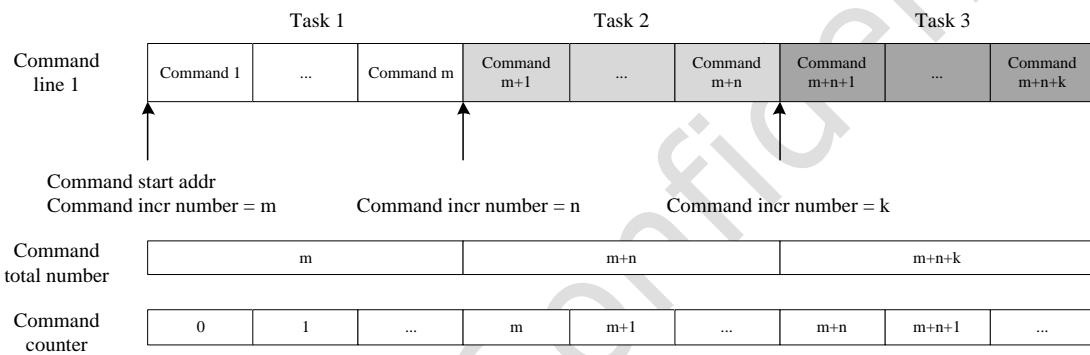


Fig. 15-7 RGA command line and command counter

15.5.3 Command Sync

In slave command mode, command sync is controlled by CPU.

In master command mode, user can enable the `current_cmd_int` command by command to generate a interrupt at the end point of target command operation.

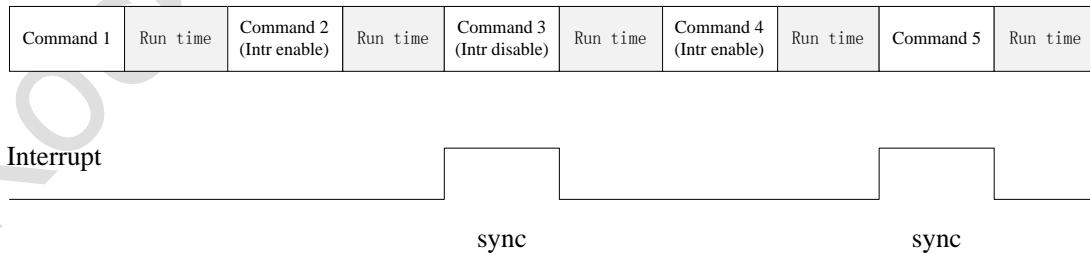


Fig. 15-8 RGA command sync generation

Chapter 16 VPU Combo

16.1 Overview

VPU_Combos is composed by the H.265 (HEVC) decoder and the H.264 encoder/decoder to realize the high quality video decoding. VPU_Combos is connected to the AHB bus through an AHB slave and the AXI bus through an AXI master. The register configuration is fed into the VPU_Combos through the AHB slave interface while the stream data is transacted between DDR and VPU_Combos through the AXI master interface.

In order to improve large data transaction performance, VPU embeds MMU (memory management unit) and supports the cacheable bus operation.

VPU_Combos supports the next-generation video coding standard HEVC (High Efficiency Video Coding, aka H.265) full-HD decoding up to 60fps. With HEVC standard, the data compression ratio can be doubled compared to H.264/MEPG-4 at the same video quality or alternatively to provide substantially improved video at the same bit rate.

16.1.1 Features

- Supports HEVC Main10 Profile up to Level 5.1 High Tier: 4096x2304 @60 fps
 - MMU embedded
 - Supports frame timeout interrupt , frame finish interrupt and bitstream error interrupt
 - Supports RLC write mode, RLC mode and Normal Mode
- Supports decoding of the following standards
 - Output data structure after decoder is YCbCr 4:2:0 semi-planar to have more efficient bus usage, and YCbCr 4:0:0 is also supported for H.264
 - H.264 up to HP level 5.2 including Baseline Profile, Main Profile and High Profile: 3840x2160@24fps
 - MPEG-4: Simple Profile up to Level 6; Advanced Profile up to Level 5 (1920x1088@60fps)
 - MPEG-2: Main Profile up to High Level(3840x2160@24fps)
 - JPEG: Baseline interleaved, and supports ROI (region of image) decode
 - VP8: (3840x2160 @24fps)
 - For H.264, Image cropping not supported
 - For MPEG-4, GMC(global motion compensation) not supported
 - For MPEG-4 SP, using a modified H.264 in-loop filter to implement deblocking filter in post-processor unit
- Built-in post processor in H.264 decoder supports:
 - Stand-alone mode: rotation, RGB conversion, scaling, dithering
 - Pipe-lining mode:, RGB conversion, scaling, dithering and alpha blending
- Supports encoding of the following standards:
 - H.264: up to HP level 4.0
 - VP8
 - Only support I and P slices, not B slices
 - Input data format:
 - ◆ YCbCr 4:2:0 planar
 - ◆ YCbCr 4:2:0 semi-planar
 - ◆ YCbYCr 4:2:2
 - ◆ CbYCrY 4:2:2 interleaved
 - ◆ RGB555 and BGR555
 - ◆ RGB565 and BGR565
 - ◆ RGB888 and BRG888
 - Image size is up to 1920x1080(Full HD)
 - Maximum frame rate is up to 30fps@1920x1080
 - Bit rate supported is up to 20Mbps
 - JPEG: Baseline (DCT sequential)

- ◆ Input JPEG file : YCbCr 4:0:0, 4:2:0, 4:2:2, 4:4:0, 4:1:1 and 4:4:4 sampling formats
 - ◆ Output raw image : YCbCr 4:0:0, 4:2:0, 4:2:2, 4:4:0, 4:1:1 and 4:4:4 semi-planar
 - ◆ Decoder size is up to 8Kx8K
 - ◆ Support JPEG ROI(region of image) decode
- Built-in pre-processor in H.264 encoder supports:
 - Cropping, rotation, YCbCr conversion

16.2 Block Diagram

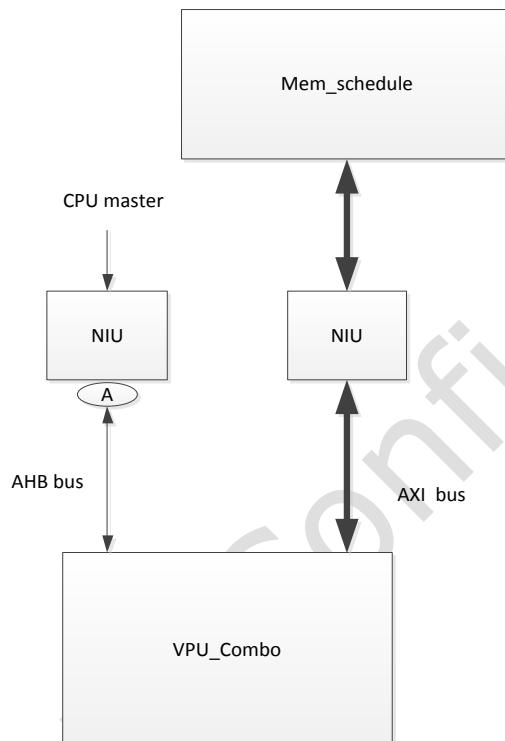


Fig. 16-1 VPU Combo in SOC

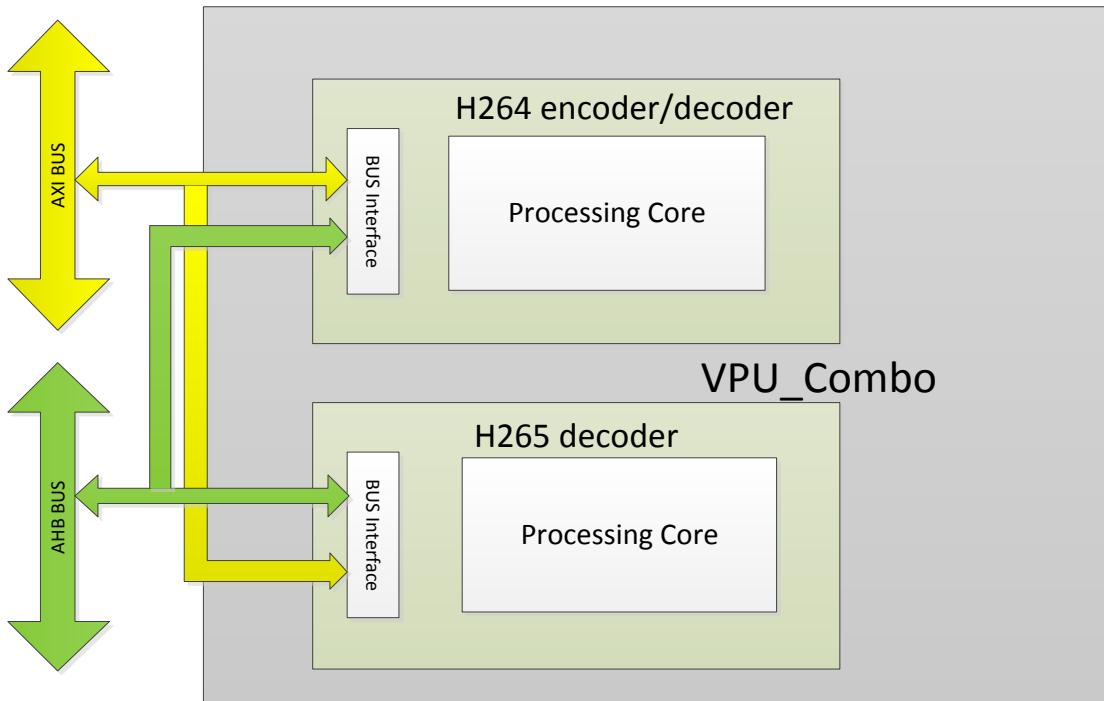


Fig. 16-2 VPU Combo Block Diagram

As shown in the figures above, CPU accesses to HEVC register bank through 32-bit AHB bus. Bitstream and compressed video data are fed into HEVC core through 128-bit AXI read channel, and after several steps of decoding process, decoded pictures are transferred to designated location in the DDR through 64-bit AXI write channel. CPU accesses to H264 encoder/decoder register bank through 32-bit AHB bus. Video data are fed into H.264 core through 64-bit AXI read channel, and after several steps of decoding process, process results are transferred to designated location in the DDR through 64-bit AXI write channel.

16.3 Function Description

16.3.1 HEVC Standard

High Efficiency Video Coding (HEVC) is a video compression standard, a successor to H.264/MPEG-4 AVC (Advanced Video Coding), that was jointly developed by the ISO/IEC Moving Picture Experts Group (MPEG) and ITU-T Video Coding Experts Group (VCEG) as ISO/IEC 23008-2 MPEG-H Part 2 and ITU-T H.265. MPEG and VCEG established a Joint Collaborative Team on Video Coding (JCT-VC) to develop the HEVC standard.

HEVC was designed to substantially improve coding efficiency compared to H.264/MPEG-4 AVC HP, i.e. to reduce bitrate requirements by half with comparable image quality, at the expense of increased computational complexity. HEVC was designed with the goal of allowing video content to have a data compression ratio of up to 1000:1. Depending on the application requirements HEVC encoders can trade off computational complexity, compression rate, robustness to errors, and encoding delay time. Two of the key features where HEVC was improved compared to H.264/MPEG-4 AVC were support for higher resolution video and improved parallel processing methods.

16.3.2 HEVC Coding Tools

1. Coding tree unit

HEVC replaces macroblocks, which were used with previous standards, with Coding Tree Units (CTUs) which can use a larger block structures of up to 64x64 pixels and can better sub-partition the picture into variable sized structures. HEVC initially divides the picture into CTUs which can be 64x64, 32x32, or 16x16 with a larger pixel block size usually increasing the coding efficiency.

2. Parallel processing tools

Tiles allow for the picture to be divided up into a grid of rectangular regions that can independently be decoded/encoded and the main purpose of tiles is to allow for parallel processing. Tiles can be independently decoded and can even allow for random access to specific regions of a picture in a video stream.

Wavefront parallel processing (WPP) is when a slice is divided into rows of CTUs in which the first row is decoded normally but each additional row requires that decisions be made in the previous row. WPP has the entropy encoder use information from the preceding row of CTUs and allows for a method of parallel processing that may allow for better compression than tiles.

Tiles and WPP are allowed but are optional. If tiles are present they must be at least 64 pixels high and 256 pixels wide with a level specific limit on the number of tiles allowed.

Slices can for the most part be decoded independently from each other with the main purpose of tiles being re-synchronization in case of data loss in the video stream. Slices can be defined as self-contained in that prediction is not made across slice boundaries. When in-loop filtering is done on a picture though information across slice boundaries may be required.[1] Slices are CTUs decoded in the order of the raster scan and different coding types can be used for slices such as I types, P types, or B types.

Dependent slices can allow for data related to tiles or WPP to be accessed more quickly by the system than if the entire slice had to be decoded.[1] The main purpose of dependent slices is to allow for low delay video encoding due to its lower latency.

3. Entropy coding

HEVC uses a context-adaptive binary arithmetic coding (CABAC) algorithm that is fundamentally similar to CABAC in H.264/MPEG-4 AVC. CABAC is the only entropy encoder method that is allowed in HEVC while there are two entropy encoder methods allowed by H.264/MPEG-4 AVC. CABAC and the entropy coding of transform coefficients in HEVC were designed for a higher throughput than H.264/MPEG-4 AVC. For instance, the number of context coded bins have been reduced by 8x and the CABAC bypass-mode has been improved in terms of its design to increase throughput. Another improvement with HEVC is that the dependencies between the coded data has been changed to further increase throughput. Context modeling in HEVC has also been improved so that CABAC can better select a context that increases efficiency when compared to H.264/MPEG-4 AVC.

4. Intra prediction

HEVC specifies 33 directional modes for intra prediction compared to the 8 directional modes for intra prediction specified by H.264/MPEG-4 AVC. HEVC also specifies planar and DC intra prediction modes.[1] The intra prediction modes use data from neighboring prediction blocks that have been previously decoded.

5. Motion compensation

For the interpolation of fractional luma sample positions HEVC uses separable application of one-dimensional half-sample interpolation with an 8-tap filter or quarter-sample interpolation with a 7-tap filter while, in comparison, H.264/MPEG-4 AVC uses a two-stage process that first

derives values at half-sample positions using separable one-dimensional 6-tap interpolation followed by integer rounding and then applies linear interpolation between values at nearby half-sample positions to generate values at quarter-sample positions.[1] HEVC has improved precision due to the longer interpolation filter and the elimination of the intermediate rounding error. For 4:2:0 video, the chroma samples are interpolated with separable one-dimensional 4-tap filtering to generate eighth-sample precision, while in comparison H.264/MPEG-4 AVC uses only a 2-tap bilinear filter (also with eighth-sample precision).

As in H.264/MPEG-4 AVC, weighted prediction in HEVC can be used either with uni-prediction (in which a single prediction value is used) or bi-prediction (in which the prediction values from two prediction blocks are combined).

6. Motion vector prediction

HEVC defines a signed 16-bit range for both horizontal and vertical motion vectors (MVs). This was added to HEVC at the July 2012 HEVC meeting with the mvLX variables. HEVC horizontal/vertical MVs have a range of -32768 to 32767 which given the quarter pixel precision used by HEVC allows for a MV range of -8192 to 8191.75 luma samples. This compares to H.264/MPEG-4 AVC which allows for a horizontal MV range of -2048 to 2047.75 luma samples and a vertical MV range of -512 to 511.75 luma samples.

HEVC allows for two MV modes which are Advanced Motion Vector Prediction (AMVP) and merge mode. AMVP uses data from the reference picture and can also use data from adjacent prediction blocks. The merge mode allows for the MVs to be inherited from neighboring prediction blocks. Merge mode in HEVC is similar to "skipped" and "direct" motion inference modes in H.264/MPEG-4 AVC but with two improvements. The first improvement is that HEVC uses index information to select one of several available candidates. The second improvement is that HEVC uses information from the reference picture list and reference picture index.

7. Inverse transforms

HEVC specifies four transform units (TUs) sizes of 4x4, 8x8, 16x16, and 32x32 to code the prediction residual. A CTB may be recursively partitioned into 4 or more TUs.[1] TUs use integer basis functions that are similar to the discrete cosine transform (DCT). In addition 4x4 luma transform blocks that belong to an intra coded region are transformed using an integer transform that is derived from discrete sine transform (DST). This provides a 1% bit rate reduction but was restricted to 4x4 luma transform blocks due to marginal benefits for the other transform cases. Chroma uses the same TU sizes as luma so there is no 2x2 transform for chroma.

8. Loop filters

HEVC specifies two loop filters that are applied sequentially, with the deblocking filter (DBF) applied first and the sample adaptive offset (SAO) filter applied afterwards. Both loop filters are applied in the inter-picture prediction loop, i.e. the filtered image is stored in the decoded picture buffer (DPB) as a reference for inter-picture prediction.

8.1 Deblocking filter

The DBF is similar to the one used by H.264/MPEG-4 AVC but with a simpler design and better support for parallel processing.[1] In HEVC the DBF only applies to a 8x8 sample grid while with H.264/MPEG-4 AVC the DBF applies to a 4x4 sample grid. DBF uses a 8x8 sample grid since it causes no noticeable degradation and significantly improves parallel processing because the DBF no longer causes cascading interactions with other operations. Another change is that HEVC only allows for three DBF strengths of 0 to 2. HEVC also requires that the DBF first apply horizontal filtering for vertical edges to the picture and only after that does it apply vertical filtering for horizontal edges to the picture. This allows for multiple parallel threads to be used

for the DBF.

8.2 Sample adaptive offset

The SAO filter is applied after the DBF and is designed to allow for better reconstruction of the original signal amplitudes by applying offsets stored in a lookup table in the bitstream. Per CTB the SAO filter can be disabled or applied in one of two modes: edge offset mode or band offset mode. The edge offset mode operates by comparing the value of a sample to two of its eight neighbors using one of four directional gradient patterns. Based on a comparison with these two neighbors, the sample is classified into one of five categories: minimum, maximum, an edge with the sample having the lower value, an edge with the sample having the higher value, or monotonic. For each of the first four categories an offset is applied. The band offset mode applies an offset based on the amplitude of a single sample. A sample is categorized by its amplitude into one of 32 bands (histogram bins). Offsets are specified for four consecutive of the 32 bands, because in flat areas which are prone to banding artifacts, sample amplitudes tend to be clustered in a small range.[1][135] The SAO filter was designed to increase picture quality, reduce banding artifacts, and reduce ringing artifacts.

16.3.3 MMU

The MMU divides memory into 4KB pages, where each page can be individually configured. For each page the following parameters are specified:

- Address translation of virtual memory, this enables the processor to work using address that differ from the physical address in the memory system.
- The permitted types of accesses to that page. Each page can permit read, write, both, or none.

The MMU use 2-level page table structure:

1. The first level, the page directory consists of 1024 directory table entries(DTEs), each pointing to a page table.
2. The second level, the page table consists of 1024 page table entries(PTEs), each pointing to a page in memory.

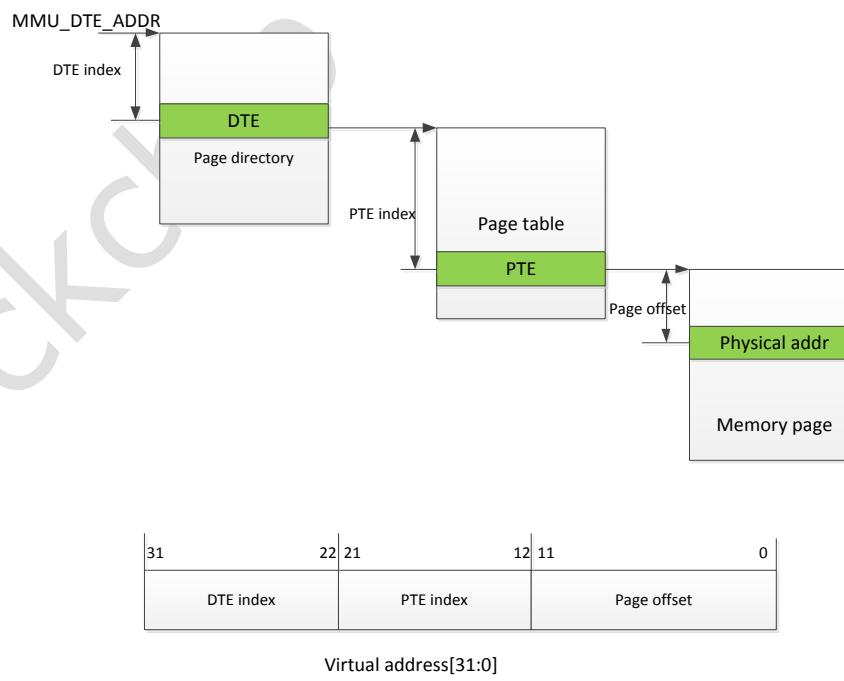


Fig. 16-3 structure of two-level page table

16.3.4 HEVC Working Mode

There are there working modes to be selected for HEVC decoder: RLC Mode, RLC Write Mode, Normal Mode.

The key differences among three working modes are whether CABAC module and Post-CABAC module are involved into the hardware decoding process.

For RLC mode, CABAC are bypassed and the input bitstream to the Post-CABAC module should be already decoded.

For RLC write mode, the decoded results by CABAC are output to the DDR, and the following decoding processes are stopped.

As for the normal mode, all the modules are involved into the decoding process, and complete decoding results are output. Normally, this mode should be selected.

16.3.5 H.264 decoder

The input of the decoder is H.264 standard bit stream in either plain NAL unit format or byte stream format. The input format in use will be automatically detected. The H.264 video encoding allows the use of multiple reference pictures, which means that the decoding order of the pictures may be different from their display order. The decoder can perform internally the display reordering of the decoded pictures or it can skip this and output all the pictures as soon as they are decoded.

The decoder has two operating modes: in the primary mode the HW performs entropy decoding, and in the secondary mode SW performs entropy decoding. Secondary mode is used in H.264 ASO or Slice Group stream decoding.

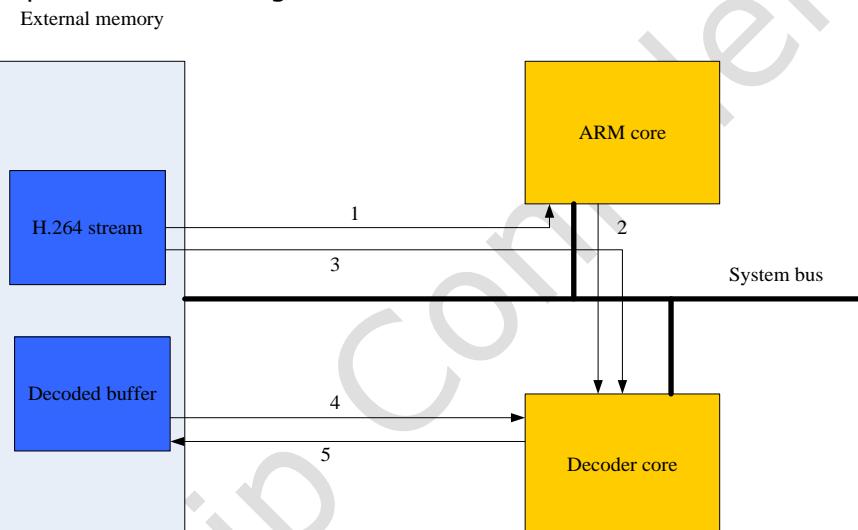


Fig. 16-4 Dataflow of HW performs entropy decoding in video decoder

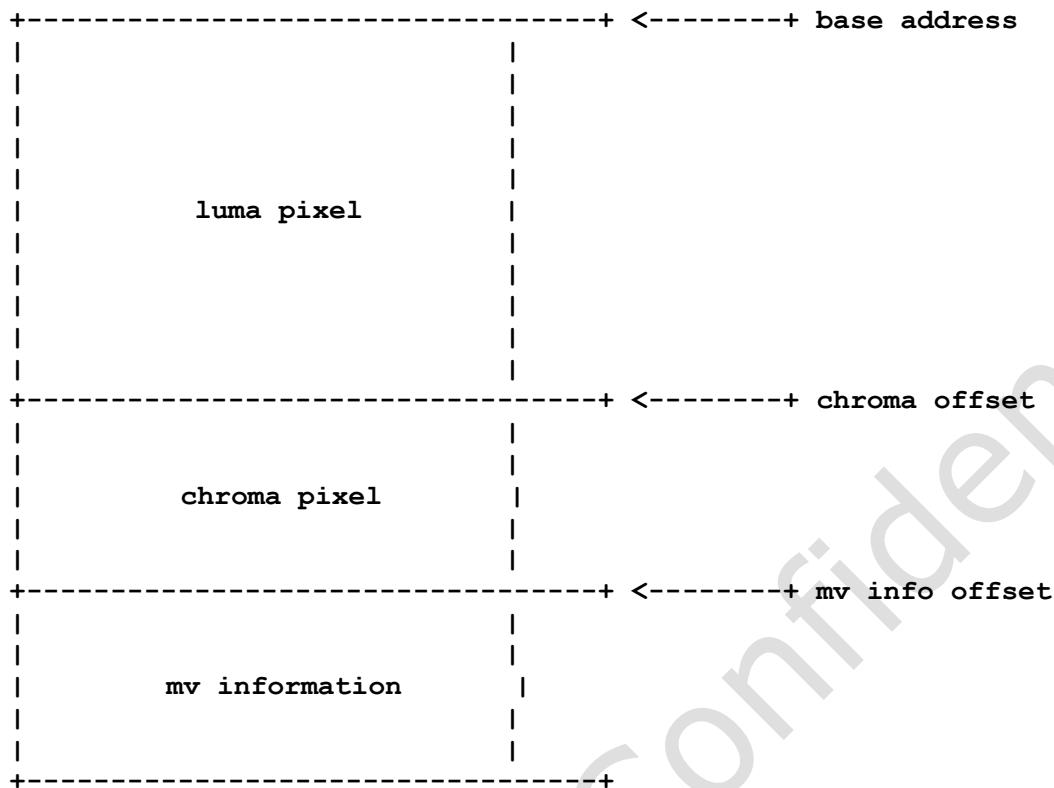
The dataflow of HW performs entropy decoding is as Fig.4-4 shown. The decoder software (SW) starts decoding the first picture by parsing the stream headers (1). Software then setups the hardware control registers (picture size, stream start address etc.) and enables the hardware (2). Hardware decodes the picture by reading stream (3) and the reference pictures (required for inter picture decoding)(4) from the external memory. Hardware writes the decoded output picture to memory one macroblock at a time (5). When the picture has been fully decoded or the hardware has run out of stream data, it gives an interrupt with a proper status flag and provides stream and address for software to continue and returns to initial state.

Table 16-1 H264 decoder external memory accessing contexts

Context	note
Bitstream read	Its length depends on the video bitstream for a frame
Decoder qtable read	It may contain CABAC_TABLE(3680bytes), PICTURE ORDER(136 bytes), MATRIX DATA(224 bytes)
Reference picture read	Max 16 reference frames
Direct mode motion vector read	NA
Direct mode motion vector write	Its base addr is right after decode output picture data Its length is mbwidth*mbheight*64

Context	note
Decode output picture write	Its length is $(\text{mbwidth} * 16) * (\text{mbheight} * 16) + (\text{mbwidth} * 16) * (\text{mbheight} * 16) / 2$

Decode output picture and direct mode motion vector is arranged as below:



offset = mv information address - picture base address

mv information address = picture base address + (mbwidth * 16) * (mbheight * 16) + (mbwidth * 16) * (mbheight * 16) / 2.

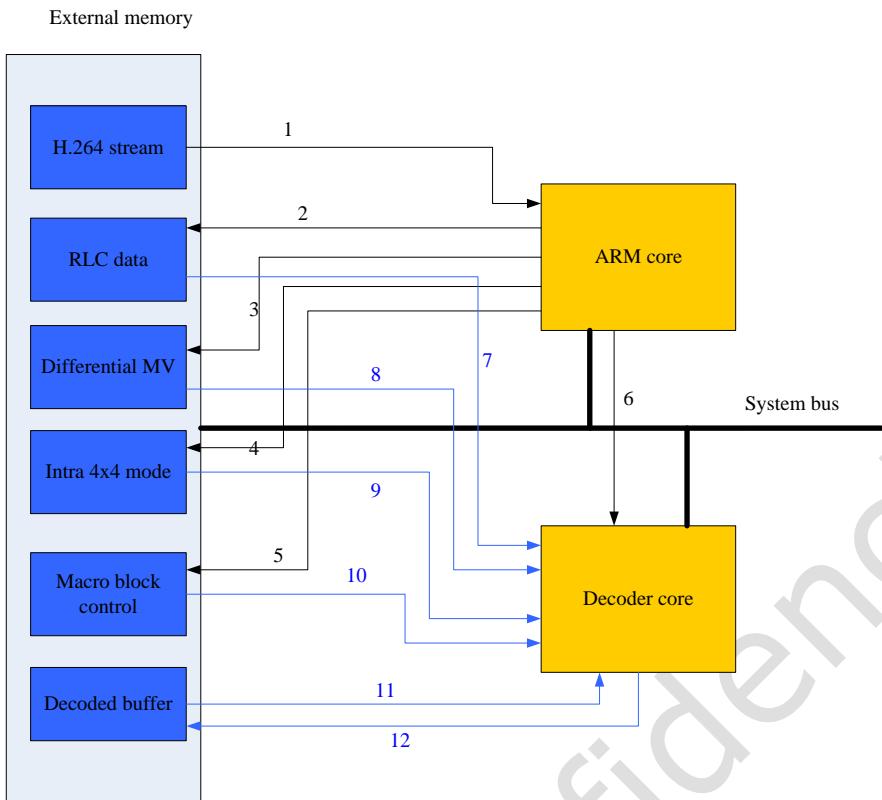


Fig. 16-5 Dataflow of SW performs entropy decoding in video decoder

SW entropy decoding mode (RLC mode) changes the input data format that is transferred from SW to HW. RLC mode for H264 only supports H264 Baseline. The dataflow of this mode is as fig.4-5. In this case the decoder software starts decoding the first picture by parsing the stream headers (1), and by performing entropy decoding. Software then writes the following items to external memory:

Run-length-code (RLC) data (2)

Differential motion vectors (3)

Intra 4x4 prediction modes (4)

Macroblock control data (5)

Last step for the software is to write the hardware control registers and to enable the hardware (6).

Hardware decodes the picture by buffering control data for several macroblocks at a time, and reading then appropriate amount of RLC data, differential motion vectors and intra modes depending on each macroblock type (7)-(10). For the rest of the decoding process (11)-(12), the functionality is identical to the HW entropy decoding mode. When the picture has been fully decoded, hardware can raise an interrupt and write the status bits in the status register.

16.3.6 VP8 decoder

Table 16-2 VP8 decoder external memory accessing contexts

Context	Note
Bitstream read	Its length depends on the video bitstream for a frame
Decoder qtable read	Vp8 tables, it contains 1208 bytes
Reference picture read	Max 3 reference frames
Segmentation data read	NA
Segmentation data write	NA
Decode output picture write	NA

16.3.7 H264 encoder

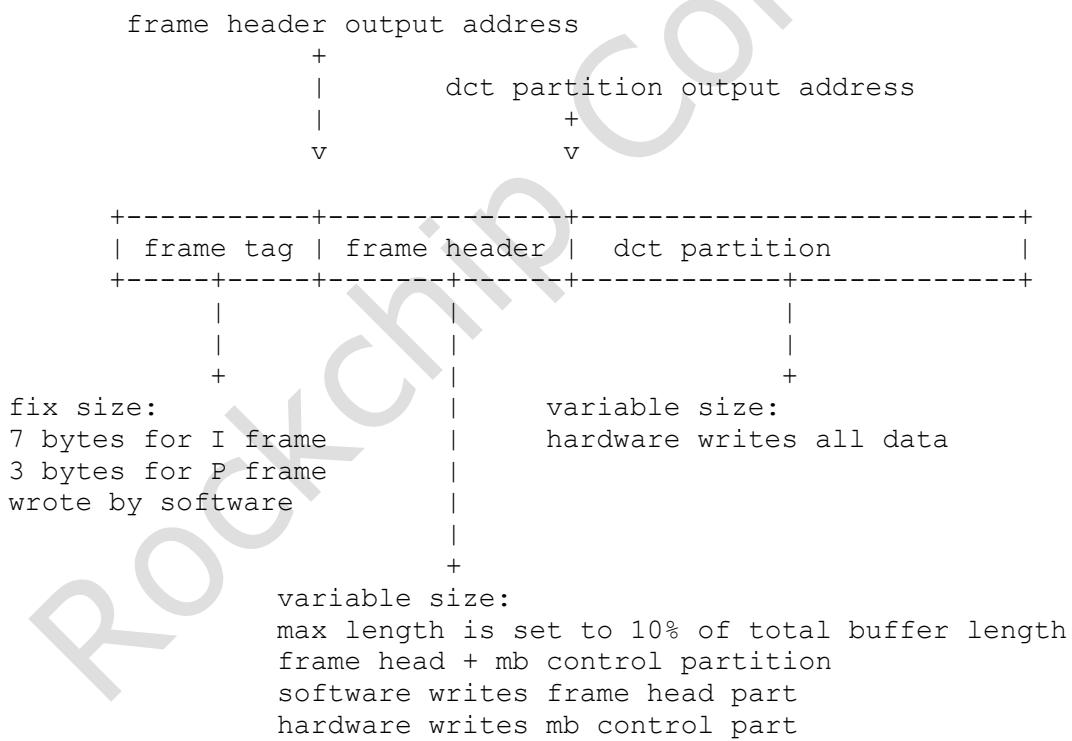
Table 16-3 H264 encoder external memory accessing contexts

Context	note
Input image read	NA
Reference picture read	NA
CABAC initialization table	NA
Stream data writing	NA
Motion vector and quality information writing (for motion detection)	Only if the feature is enabled

16.3.8 VP8 encoder

Table 16-4 vp8 encoder external memory accessing contexts

Context	note
Input image read	NA
VP8 probability table read	Preformed in the beginning of the encoding
Reference picture read	NA
CABAC initialization table	NA
Stream data writing	Some part is written by hardware and some part is written by software, see the picture below
VP8 probability count write	Performed in the end of the encoding



when hardware finishes encoding hardware will write the frame header part size and dct partition size to given memory address. Software needs to read the size and copy two part of stream together.

16.4 Register description

This section describes the control/status registers of the VPU_Combo. HEVC and H.264 decoder/encoder have individual base register address for each other.

If HEVC is chosen to work, HEVC register base address is the base address of the hevc_base. The HEVC reading MMU master register base address is hevc_base+0x440, the writing MMU register base address is vpu_combo_base + 0x480, and the cache control register base address is vpu_combo_base + 0x400.

If H.264 decoder/encoder is chosen to work, VEPU(encoder) register base address is vpu_base, and VDPU(decoder) base address is vpu_base + 0x400. MMU base address is vpu_base +0x800, and VDPU cache control base address is vpu_base + 0xc00.

16.4.1 VDP_HEVC Register Summary

Name	Offset	Size	Reset Value	Description
hevc_swreg0_id	0x0000	W	0x68761100	ID register (read only)
hevc_swreg1_int	0x0004	W	0x00200022	interrupt and decoder enable register
hevc_swreg2_sysctrl	0x0008	W	0x00000000	Data input and output endian setting and sys ctrl
hevc_swreg3_picpar	0x000c	W	0x00000000	picture parameters
hevc_swreg4_strm_rlc_base	0x0010	W	0x00000000	the stream or rlc data base address
hevc_swreg5_stream_rlc_len	0x0014	W	0x00000000	amount of stream bytes or rlc data byte in the input buffer or the
hevc_swreg6_cabactbl_base	0x0018	W	0x00000000	the base address of cabac table
hevc_swreg7_decout_base	0x001c	W	0x00000000	base address of decoder output picture base address
hevc_swreg8_y_virstride	0x0020	W	0x00000000	the ouput picture y virtual stride
hevc_swreg9_yuv_virstride	0x0024	W	0x00000000	the ouput picture yuv virtual stride
hevc_swreg10_refer0_base	0x0028	W	0x00000000	base address for reference picture index 0
hevc_swreg11_refer1_base	0x002c	W	0x00000000	base address for reference picture index 1
hevc_swreg12_refer2_base	0x0030	W	0x00000000	base address for reference picture index 2
hevc_swreg13_refer3_base	0x0034	W	0x00000000	base address for reference picture index 3
hevc_swreg14_refer4_base	0x0038	W	0x00000000	base address for reference picture index 4
hevc_swreg15_refer5_base	0x003c	W	0x00000000	base address for reference picture index 5
hevc_swreg16_refer6_base	0x0040	W	0x00000000	base address for reference picture index 6
hevc_swreg17_refer7_base	0x0044	W	0x00000000	base address for reference picture index 7
hevc_swreg18_refer8_base	0x0048	W	0x00000000	base address for reference picture index 8
hevc_swreg19_refer9_base	0x004c	W	0x00000000	base address for reference picture index 9

Name	Offset	Size	Reset Value	Description
hevc_swreg20_refer10_base	0x0050	W	0x00000000	base address for reference picture index 10
hevc_swreg21_refer11_base	0x0054	W	0x00000000	base address for reference picture index 11
hevc_swreg22_refer12_base	0x0058	W	0x00000000	base address for reference picture index 12
hevc_swreg23_refer13_base	0x005c	W	0x00000000	base address for reference picture index 13
hevc_swreg24_refer14_base	0x0060	W	0x00000000	base address for reference picture index 14
hevc_swreg25_refer0_poc	0x0064	W	0x00000000	the poc of reference picture index 0
hevc_swreg26_refer1_poc	0x0068	W	0x00000000	the poc of reference picture index 1
hevc_swreg27_refer2_poc	0x006c	W	0x00000000	the poc of reference picture index 2
hevc_swreg28_refer3_poc	0x0070	W	0x00000000	the poc of reference picture index 3
hevc_swreg29_refer4_poc	0x0074	W	0x00000000	the poc of reference picture index 4
hevc_swreg30_refer5_poc	0x0078	W	0x00000000	the poc of reference picture index 5
hevc_swreg31_refer6_poc	0x007c	W	0x00000000	the poc of reference picture index 6
hevc_swreg32_refer7_poc	0x0080	W	0x00000000	the poc of reference picture index 7
hevc_swreg33_refer8_poc	0x0084	W	0x00000000	the poc of reference picture index 8
hevc_swreg34_refer9_poc	0x0088	W	0x00000000	the poc of reference picture index 9
hevc_swreg35_refer10_poc	0x008c	W	0x00000000	the poc of reference picture index 10
hevc_swreg36_refer11_poc	0x0090	W	0x00000000	the poc of reference picture index 11
hevc_swreg37_refer12_poc	0x0094	W	0x00000000	the poc of reference picture index 12
hevc_swreg38_refer13_poc	0x0098	W	0x00000000	the poc of reference picture index 13
hevc_swreg39_refer14_poc	0x009c	W	0x00000000	the poc of reference picture index 14
hevc_swreg40_cur_poc	0x00a0	W	0x00000000	the poc of cur picture
hevc_swreg41_rlcread_base	0x00a4	W	0x00000000	the base address or rlcread base addr
hevc_swreg42_pps_base	0x00a8	W	0x00000000	the base address of pps
hevc_swreg43_rps_base	0x00ac	W	0x00000000	the base address of rps
hevc_swreg44_cabac_error_en	0x00b0	W	0x00000000	cabac error enable config
hevc_swreg45_cabac_error_status	0x00b4	W	0x00000000	cabac error status
hevc_swreg46_cabac_error_ctu	0x00b8	W	0x00400000	cabac error ctu
hevc_swreg47_sao_ctu_position	0x00bc	W	0x00000000	sao ctu position
hevc_swreg64_performance_cycle	0x0100	W	0x00000000	hevc performance cycle
hevc_swreg65_axi_ddr_rdata	0x0104	W	0x00000000	axi ddr read data num

Name	Offset	Size	Reset Value	Description
hevc_swreg66_axi_ddr_wd_ata	0x0108	W	0x00000000	axi ddr write data number

Notes:Size: **B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access

16.4.2 VDP_HEVC Detail Register Description

hevc_swreg0_id

Address: Operational Base + offset (0x0000)

ID register (read only)

Bit	Attr	Reset Value	Description
31:16	RO	0x6876	prod_num product number The ascii code of "hv", which is 0x6876
15	RO	0x0	reserved
14	RW	0x0	codec_flag codec flag 0: only dec 1: dec + enc
13	RO	0x0	reserved
12	RW	0x1	profile hevc profile 0: Main 1: Main10
11:9	RO	0x0	reserved
8	RO	0x1	level level 0: FHD 1: UHD
7:0	RO	0x00	minor_ver minor version minor version

hevc_swreg1_int

Address: Operational Base + offset (0x0004)

interrupt and decoder enable register

Bit	Attr	Reset Value	Description
31:23	RO	0x0	reserved
22	RW	0x0	sw_softreset_rdy when it is 1'b1, it says that softreset has been done

Bit	Attr	Reset Value	Description
21	RW	0x1	sw_force_softreset_valid when sw_force_softreset_valid is 1'b1, sw_softrst_en will always be valid to the system no matter that whether the axi bus is idle; when sw_force_softreset_valid is 1'b0, sw_softrst_en will only be valid when the axi bus is idle.
20	RW	0x0	sw_softrst_en_p softreset enable softreset enable signal write 1 to soft reset, write 0 invalid puls register
19	RO	0x0	reserved
18	RW	0x0	sw_cabu_end_sta cabac decode end status cabac decode end status
17	RW	0x0	sw_colmv_ref_error_sta colmv ref error status colmv ref error status when it is 1'b1, it means that inter module read the invalid dpb frame
16	RO	0x0	reserved
15	RW	0x0	sw_dec_timeout_sta decoder timeout interrupt status When high the decoder has been idling for too long. it will self reset the hardware only when sw_dec_timeout_e is 1'b1, this bit is valid
14	RW	0x0	sw_dec_error_sta status bit of input stream error when high, an error is found in input data stream decoding. It will self reset the hardware
13	RW	0x0	sw_dec_bus_sta bus error status When this bit is high, there is error on the axi bus, it will self reset hardware
12	RW	0x0	sw_dec_rdy_sta decoder ready status when this bit is high, decoder has decoded a picture
11:10	RO	0x0	reserved

Bit	Attr	Reset Value	Description
9	RW	0x0	sw_dec_irq_raw the raw status of sw_dec_irq the raw status of sw_dec_irq, SW should reset this bit after interrupt is handled
8	RO	0x0	sw_dec_irq decoder IRQ when high, decoder requests an interrupt. $sw_dec_irq = sw_dec_irq_raw \&& (sw_dec_irq_dis == 1'b0)$
7	RW	0x0	sw_stmerror_waitdecfifo_empty whether the stream error process wait the decfifo empty when it is 1'b0, the stream error process will no wait the ca2decfifo empty when it is 1'b1, the stream error process will wait the ca2decfifo empty
6	RO	0x0	reserved
5	RW	0x1	sw_dec_timeout_e Timeout interrupt enable If enabled HW may return timeout interrupt in case HW gets stucked while decoding picture.
4	RW	0x0	sw_dec_irq_dis decoder IRQ disable When hight, there are no interrupts concerning decoder from HW. Polling must be used to see the interrupt status
3:2	RO	0x0	reserved
1	RW	0x1	sw_dec_clkgate_e decoder dynamic clock gating enable 0 = clock is running for all structures 1 = clock is gated for decoder structures that are not used
0	RW	0x0	sw_dec_e decoder enable Decoder enable. Setting this bit high will start the decoding operation. HW will reset this when picture is processed or stream error is detected or bus error or time out interrupt is given

hevc_swreg2_sysctrl

Address: Operational Base + offset (0x0008)

Data input and output endian setting and sys ctrl

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved

Bit	Attr	Reset Value	Description
18:12	RW	0x00	sw_strm_start_bit exact bit of stream start exact bit of streamd start word where decoding can be started (asosiates with sw_str_rlc_base)
11	RW	0x0	sw_rlc_mode rlc mode enable 0 = HW decodes video from bit stream 1 = HW decodes video from RLC input data
10	RW	0x0	sw_rlc_mode_direct_write cabac decode output direct write cabac decode output direct write enable when this bit is enable , all the module other than cabac and busifd are not work
9	RO	0x0	reserved
8	RW	0x0	sw_out_cbc_swap output cbc swap 1'b0: cb(u) is in the lower address, cr(v) is in the higher address 1'b1: cb(u) is in the higher address,cr(v) is in the lower address sw_in_cbc_swap is the same with sw_out_cbc_swap
7	RW	0x0	sw_out_swap32_e decoder output data and dpb input data 32bit swap may be used for 64 or 128 bit environment 0 = no swapping of 32 bit words 1 = 32 bit data words are swapped
6	RW	0x0	sw_out_endian dec output data and colmv , dpb data and colmv input endian 0 = little endian 1 = big endian for litter enadian , a data 0x12345678, 0x78 is stored in lower address, 0x12 is stored in higher address
5	RW	0x0	sw_str_swap64_e stream 64bit data swap may be used for 128 bit environment 0 = no swapping of 64 bit words 1 = 64 bit data words are swapped

Bit	Attr	Reset Value	Description
4	RW	0x0	sw_str_swap32_e stream 32bit data swap may be used for 64 or 128 bit environment 0 = no swapping of 32 bit words 1 = 32 bit data words are swapped
3	RW	0x0	sw_str_endian stream data input endian mode 0 = little endian 1 = big endian for litter enadian , a data 0x12345678, 0x78 is stored in lower address, 0x12 is stored in higher address
2	RW	0x0	sw_in_swap64_e input 64bit data swap for other than stream and dpb data may be used for 128 bit environment 0 = no swapping of 64 bit words 1 = 64 bit data words are swapped
1	RW	0x0	sw_in_swap32_e input 32bit data swap for other than stream and dpb data may be used for 64 or 128 bit environment 0 = no swapping of 32 bit words 1 = 32 bit data words are swapped
0	RW	0x0	sw_in_endian decoder input endian mode for other than stream and dpb data 0 = little endian 1 = big endian for litter enadian , a data 0x12345678, 0x78 is stored in lower address, 0x12 is stored in higher address

hevc_swreg3_picpar

Address: Operational Base + offset (0x000c)

picture parameters

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved

Bit	Attr	Reset Value	Description
30:21	RW	0x000	sw_slice_num slice number in a frame slice number in a frame (0~199, when it is 0, it real means 1 slice in a frame) just only used for rps read. 2013.11.27 change the meaning from count from 1, so it will be in 1~200 2013.11.30 sw_slice_num max value is change to 600, so sw_slice_num expand to 10bit
20:12	RW	0x000	sw_uv_hor_virstride Field0000 Abstract picture horizontal virtual stride (the unit is 128bit) the max is $(4096 \times 1.5 + 128) / 16 = 0x188$ suggest this register to config to even for advance ddr performance
11:9	RO	0x0	reserved
8:0	RW	0x000	sw_y_hor_virstride picture horizontal virtual stride picture horizontal virtual stride (the unit is 128bit) the max is $(4096 \times 1.5 + 128) / 16 = 0x188$ suggest this register to config to even for advance ddr performance

hevc_swreg4_strm_rlc_base

Address: Operational Base + offset (0x0010)

the stream or rlc data base address

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_strm_rlc_base the stream or rlc data base address when swreg2.sw_rlc_mode =1, it is base address for rlc data when swreg2.sw_rlc_mode =0, it is base address for stream , after a frame is decoded ready or error (stream error , time out , bus error) , it is the last address of the stream the address should 128bit align
3:0	RO	0x0	reserved

hevc_swreg5_stream_rlc_len

Address: Operational Base + offset (0x0014)

amount of stream bytes or rlc data byte in the input buffer or the

Bit	Attr	Reset Value	Description
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Bit	Attr	Reset Value	Description
31:27	RO	0x0	reserved
26:0	RW	0x0000000	<p>sw_stream_len amount of stream (unit is 8bit) in the input buffer amount of stream 8bits in the input buffer the max of sw_stream_len : $4096 \times 2304 \times 1.5 \times 1.5 = 0x1440000$ 128bits unit: $0x1440000 / 16 = 0x144000$ it is count from 0 2013.10.15 change to 23bit for zty's suggestion 2013.10.28, amount of stream data bytes in input buffer. it is count from 1, change to 27bits</p>

hevc_swreg6_cabactbl_base

Address: Operational Base + offset (0x0018)

the base address of cabac table

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	<p>sw_cabactbl_base the base address of cabac table the base address of cabac table the address should 128bit align</p>
3:0	RO	0x0	reserved

hevc_swreg7_decout_base

Address: Operational Base + offset (0x001c)

base address of decoder output picture base address

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	<p>sw_decout_base base address of decoder output picture addr base address of decoder output picture the address should be 128bit align</p>
3:0	RO	0x0	reserved

hevc_swreg8_y_virstride

Address: Operational Base + offset (0x0020)

the ouput picture y virtual stride

Bit	Attr	Reset Value	Description
31:20	RO	0x0	reserved

Bit	Attr	Reset Value	Description
19:0	RW	0x00000	sw_y_virstride the output picture y virtual stride the output picture y virtual stride (the unit is 128bit) the max: (4096x1.5 +128) x 2304 = 0xdc8000 we can know the sw_uvout_base = sw_decout_base + (sw_y_virstride <<4)

hevc_swreg9_yuv_virstride

Address: Operational Base + offset (0x0024)

the ouput picture yuv virtual stride

Bit	Attr	Reset Value	Description
31:21	RO	0x0	reserved
20:0	RW	0x0000000	sw_yuv_virstride the ouput picture yuv virtual stride the output picture yuv virtual stride (the unit is 128bit) the max : (4096x1.5 +128) x 2304 x1.5 = 0x14ac000 we can know the sw_mvout_base = sw_decout_base + (sw_yuv_virstride <<4)

hevc_swreg10_refer0_base

Address: Operational Base + offset (0x0028)

base address for reference picture index 0

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_refer0_base base address for reference picture index0 base address for reference picture index 0 (the address should be 128bit align)
3:0	RW	0x0	sw_ref_valid_0_3 valid flag for picture index 0 ~3 valid flag for picture index 0 ~3

hevc_swreg11_refer1_base

Address: Operational Base + offset (0x002c)

base address for reference picture index 1

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_refer1_base base address for reference picture index 1 base address for reference picture index 1 (the address should be 128bit align)

Bit	Attr	Reset Value	Description
3:0	RW	0x0	sw_ref_valid_4_7 valid flag for picture index 4 ~7 valid flag for picture index 4 ~7

hevc_swreg12_refer2_base

Address: Operational Base + offset (0x0030)

base address for reference picture index 2

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_refer2_base base address for reference picture index 2 base address for reference picture index 2 (the address should be 128bit align)
3:0	RW	0x0	sw_ref_valid_8_11 valid flag for picture index 8~11 valid flag for picture index 8~11

hevc_swreg13_refer3_base

Address: Operational Base + offset (0x0034)

base address for reference picture index 3

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_refer3_base base address for reference picture index 3 base address for reference picture index 3 (the address should be 128bit align)
3	RO	0x0	reserved
2:0	RW	0x0	sw_ref_valid_12_14 valid flag for picture index 12~14 valid flag for picture index 12~14

hevc_swreg14_refer4_base

Address: Operational Base + offset (0x0038)

base address for reference picture index 4

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_refer4_base base address for reference picture index 4 base address for reference picture index 4(the address should be 128bit align)
3:0	RO	0x0	reserved

hevc_swreg15_refer5_base

Address: Operational Base + offset (0x003c)

base address for reference picture index 5

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_refer5_base base address for reference picture index 5 base address for reference picture index 5(the address should be 128bit align)
3:0	RO	0x0	reserved

hevc_swreg16_refer6_base

Address: Operational Base + offset (0x0040)

base address for reference picture index 6

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_refer6_base base address for reference picture index 6 base address for reference picture index 6(the address should be 128bit align)
3:0	RO	0x0	reserved

hevc_swreg17_refer7_base

Address: Operational Base + offset (0x0044)

base address for reference picture index 7

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_refer7_base base address for reference picture index 7 base address for reference picture index 7(the address should be 128bit align)
3:0	RO	0x0	reserved

hevc_swreg18_refer8_base

Address: Operational Base + offset (0x0048)

base address for reference picture index 8

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_refer8_base base address for reference picture index 8 base address for reference picture index 8(the address should be 128bit align)
3:0	RO	0x0	reserved

hevc_swreg19_refer9_base

Address: Operational Base + offset (0x004c)

base address for reference picture index 9

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_refer9_base base address for reference picture index 9 base address for reference picture index 9(the address should be 128bit align)

Bit	Attr	Reset Value	Description
3:0	RO	0x0	reserved

hevc_swreg20_refer10_base

Address: Operational Base + offset (0x0050)

base address for reference picture index 10

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_refer10_base base address for reference picture index 10 base address for reference picture index 10(the address should be 128bit align)
3:0	RO	0x0	reserved

hevc_swreg21_refer11_base

Address: Operational Base + offset (0x0054)

base address for reference picture index 11

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_refer11_base base address for reference picture index 11 base address for reference picture index 11(the address should be 128bit align)
3:0	RO	0x0	reserved

hevc_swreg22_refer12_base

Address: Operational Base + offset (0x0058)

base address for reference picture index 12

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_refer12_base base address for reference picture index 12 base address for reference picture index 12(the address should be 128bit align)
3:0	RO	0x0	reserved

hevc_swreg23_refer13_base

Address: Operational Base + offset (0x005c)

base address for reference picture index 13

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_refer13_base base address for reference picture index 13 base address for reference picture index 13(the address should be 128bit align)
3:0	RO	0x0	reserved

hevc_swreg24_refer14_base

Address: Operational Base + offset (0x0060)

base address for reference picture index 14

Bit	Attr	Reset Value	Description
31:4	RW	0x00000000	sw_refer14_base base address for reference picture index 14 base address for reference picture index 14(the address should be 128bit align)
3:0	RO	0x0	reserved

hevc_swreg25_refer0_poc

Address: Operational Base + offset (0x0064)

the poc of reference picture index 0

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_refer0_poc the poc of reference picture index 0 the poc of reference picture index 0

hevc_swreg26_refer1_poc

Address: Operational Base + offset (0x0068)

the poc of reference picture index 1

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_refer1_poc the poc of reference picture index 1 the poc of reference picture index 1

hevc_swreg27_refer2_poc

Address: Operational Base + offset (0x006c)

the poc of reference picture index 2

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_refer2_poc the poc of reference picture index 2 the poc of reference picture index 2

hevc_swreg28_refer3_poc

Address: Operational Base + offset (0x0070)

the poc of reference picture index 3

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_refer3_poc the poc of reference picture index 3 the poc of reference picture index 3

hevc_swreg29_refer4_poc

Address: Operational Base + offset (0x0074)

the poc of reference picture index 4

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_refer4_poc the poc of reference picture index 4 the poc of reference picture index 4

hevc_swreg30_refer5_poc

Address: Operational Base + offset (0x0078)

the poc of reference picture index 5

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_refer5_poc the poc of reference picture index 5 the poc of reference picture index 5

hevc_swreg31_refer6_poc

Address: Operational Base + offset (0x007c)

the poc of reference picture index 6

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_refer6_poc the poc of reference picture index 6 the poc of reference picture index 6

hevc_swreg32_refer7_poc

Address: Operational Base + offset (0x0080)

the poc of reference picture index 7

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_refer7_poc the poc of reference picture index 7 the poc of reference picture index 7

hevc_swreg33_refer8_poc

Address: Operational Base + offset (0x0084)

the poc of reference picture index 8

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_refer8_poc the poc of reference picture index 8 the poc of reference picture index 8

hevc_swreg34_refer9_poc

Address: Operational Base + offset (0x0088)

the poc of reference picture index 9

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_refer9_poc the poc of reference picture index 9 the poc of reference picture index 9

hevc_swreg35_refer10_poc

Address: Operational Base + offset (0x008c)

the poc of reference picture index 10

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_refer10_poc the poc of reference picture index 10 the poc of reference picture index 10

hevc_swreg36_refer11_poc

Address: Operational Base + offset (0x0090)

the poc of reference picture index 11

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_refer11_poc the poc of reference picture index 11 the poc of reference picture index 11

hevc_swreg37_refer12_poc

Address: Operational Base + offset (0x0094)

the poc of reference picture index 12

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_refer12_poc the poc of reference picture index 12 the poc of reference picture index 12

hevc_swreg38_refer13_poc

Address: Operational Base + offset (0x0098)

the poc of reference picture index 13

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_refer13_poc the poc of reference picture index 13 the poc of reference picture index 13

hevc_swreg39_refer14_poc

Address: Operational Base + offset (0x009c)

the poc of reference picture index 14

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_refer14_poc the poc of reference picture index 14 the poc of reference picture index 14

hevc_swreg40_cur_poc

Address: Operational Base + offset (0x00a0)

the poc of cur picture

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_cur_poc the poc of the cur picture the poc of the cur picture

hevc_swreg41_rlcwrite_base

Address: Operational Base + offset (0x00a4)

the base address or rlcwrite base addr

Bit	Attr	Reset Value	Description
31:3	RW	0x00000000	sw_rlcwrite_base the base address of rlcwrite the base address of rlcwrite(the address should 64bit align) cabac output write to this rlcwrite base address when sw_rlc_mode_direct_write in swreg2_sysctrl is valid
2:0	RO	0x0	reserved

hevc_swreg42_pps_base

Address: Operational Base + offset (0x00a8)

the base address of pps

Bit	Attr	Reset Value	Description
31:4	RW	0x00000000	sw_pps_base the base address of pps the base address of pps (the address should 128bit align) it is for storing sps(sequence parameter set) and pps(picture parameter set)
3:0	RO	0x0	reserved

hevc_swreg43_rps_base

Address: Operational Base + offset (0x00ac)

the base address of rps

Bit	Attr	Reset Value	Description
31:4	RW	0x00000000	sw_rps_base rps base address rps(reference picture set) base address (the address should 128bit align)
3:0	RO	0x0	reserved

hevc_swreg44_cabac_error_en

Address: Operational Base + offset (0x00b0)

cabac error enable config

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved

Bit	Attr	Reset Value	Description
27:0	RW	0x0000000	sw_cabac_error_e cabac error enable regs cabac error enable regs

hevc_swreg45_cabac_error_status

Address: Operational Base + offset (0x00b4)

cabac error status

Bit	Attr	Reset Value	Description
31:28	RW	0x0	sw_colmv_error_ref_picidx colmv error ref picidx when sw_colmv_ref_error_sta is 1'b1, these bits are used for tell which dpb frame is invalid but is read by inter module
27:0	RW	0x0000000	sw_cabac_error_status cabac error status cabac error status

hevc_swreg46_cabac_error_ctu

Address: Operational Base + offset (0x00b8)

cabac error ctu

Bit	Attr	Reset Value	Description
31:23	RO	0x0	reserved
22:16	RW	0x40	sw_streamfifo_space2full stream fifo space to full It is for debug use, to tell the stream fifo space to full
15:8	RW	0x00	sw_cabac_error_ctu_yoffset cabac error ctu yoffset cabac error ctu yoffset
7:0	RW	0x00	sw_cabac_error_ctu_xoffset cabac error ctu xoffset cabac error ctu xoffset

hevc_swreg47_sao_ctu_position

Address: Operational Base + offset (0x00bc)

sao ctu position

Bit	Attr	Reset Value	Description
31:26	RO	0x0	reserved
25:16	RW	0x000	sw_saowr_yoffset saowr y offset saowr y offset , its unit is 4 pixels
15:9	RO	0x0	reserved

Bit	Attr	Reset Value	Description
8:0	RW	0x000	sw_saowr_xoffset saowr x address offset saowr x address offset, its unit is 128bit

hevc_swreg64_performance_cycle

Address: Operational Base + offset (0x0100)

hevc performance cycle

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_performance_cycle hevc running cycle hevc running cycle if just want to analys a frame performance cycle, should set the register 0 before start a frame

hevc_swreg65_axi_ddr_rdata

Address: Operational Base + offset (0x0104)

axi ddr read data num

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_axi_ddr_rdata axi ddr rdata num axi ddr rdata num, the unit is byte

hevc_swreg66_axi_ddr_wdata

Address: Operational Base + offset (0x0108)

axi ddr write data number

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_axi_ddr_wdata hevc write data byte num hevc write data byte num

16.4.3 VDP_HEVC MMU Register Summary

Name	Offset	Size	Reset Value	Description
hevc_mmu_DTE_ADDR	0x00000	W	0x00000000	MMU current page Table address
hevc_mmu_STATUS	0x00004	W	0x00000018	MMU status register
hevc_mmu_COMMAND	0x00008	W	0x00000000	MMU command register
hevc_mmu_PAGE_FAULT_ADDR	0x0000c	W	0x00000000	MMU logical address of last page fault
hevc_mmu_ZAP_ONE_LINE	0x00010	W	0x00000000	MMU Zap cache line register
hevc_mmu_INT_RAWSTAT	0x00014	W	0x00000000	MMU raw interrupt status register
hevc_mmu_INT_CLEAR	0x00018	W	0x00000000	MMU raw interrupt status register

Name	Offset	Size	Reset Value	Description
hevc_mmu_INT_MASK	0x0001c	W	0x00000000	MMU raw interrupt status register
hevc_mmu_INT_STATUS	0x00020	W	0x00000000	MMU raw interrupt status register
hevc_mmu_AUTO_GATING	0x00024	W	0x00000001	mmu auto gating

Notes:Size: **B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access

16.4.4 VDP_HEVC MMU Detail Register Description

hevc_mmu_DTE_ADDR

Address: Operational Base + offset (0x00000)

MMU current page Table address

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	MMU_DTE_ADDR mmu dte base addr mmu dte base addr , the address must be 4kb aligned

hevc_mmu_STATUS

Address: Operational Base + offset (0x00004)

MMU status register

Bit	Attr	Reset Value	Description
31:11	RO	0x0	reserved
10:6	RO	0x00	PAGE_FAULT_BUS_ID page fault bus id Index of master responsible for last page fault
5	RO	0x0	PAGE_FAULT_IS_WRITE page fault access The direction of access for last page fault: 0 = Read 1 = Write
4	RO	0x1	REPLAY_BUFFER_EMPTY replay buffer empty status 1'b1: The MMU replay buffer is empty
3	RO	0x1	MMU_IDLE mmu idle status The MMU is idle when accesses are being translated and there are no unfinished translated accesses. 1'b1: MMU is idle
2	RO	0x0	STAIL_ACTIVE stall active status MMU stall mode currently enabled. The mode is enabled by command 1'b1: MMU is in stall active status

Bit	Attr	Reset Value	Description
1	RO	0x0	PAGE_FAULT_ACTIVE page fault active status MMU page fault mode currently enabled . The mode is enabled by command. 1'b1: page fault is active
0	RO	0x0	PAGING_ENABLED Paging enabled status 1'b0: paging is disabled 1'b1: Paging is enabled

hevc_mmu_COMMAND

Address: Operational Base + offset (0x00008)

MMU command register

Bit	Attr	Reset Value	Description
31:3	RO	0x0	reserved
2:0	WO	0x0	MMU_CMD Field0000 Abstract MMU_CMD. This can be: 0: MMU_ENABLE_PAGING 1: MMU_DISABLE_PAGING 2: MMU_ENABLE_STALL 3: MMU_DISABLE_STALL 4: MMU_ZAP_CACHE 5: MMU_PAGE_FAULT_DONE 6: MMU_FORCE_RESET

hevc_mmu_PAGE_FAULT_ADDR

Address: Operational Base + offset (0x0000c)

MMU logical address of last page fault

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	PAGE_FAULT_ADDR Field0000 Abstract address of last page fault

hevc_mmu_ZAP_ONE_LINE

Address: Operational Base + offset (0x00010)

MMU Zap cache line register

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	MMU_ZAP_ONE_LINE Field0000 Abstract address to be invalidated from the page table cache

hevc_mmu_INT_RAWSTAT

Address: Operational Base + offset (0x00014)

MMU raw interrupt status register

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	RW	0x0	READ_BUS_ERROR Field0000 Abstract read bus error
0	RW	0x0	PAGE_FAULT Field0000 Abstract page fault

hevc_mmu_INT_CLEAR

Address: Operational Base + offset (0x00018)

MMU raw interrupt status register

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	WO	0x0	READ_BUS_ERROR Field0000 Abstract read bus error
0	WO	0x0	PAGE_FAULT Field0000 Abstract page fault

hevc_mmu_INT_MASK

Address: Operational Base + offset (0x0001c)

MMU raw interrupt status register

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	RW	0x0	READ_BUS_ERROR Field0000 Abstract read bus error enable an interrupt source if the corresponding mask bit is set to 1
0	RW	0x0	PAGE_FAULT Field0000 Abstract page fault enable an interrupt source if the corresponding mask bit is set to 1

hevc_mmu_INT_STATUS

Address: Operational Base + offset (0x00020)

MMU raw interrupt status register

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	RO	0x0	READ_BUS_ERROR read bus error status 1'b1: read bus error

Bit	Attr	Reset Value	Description
0	RO	0x0	PAGE_FAULT page fault status 1'b1:page fault

hevc_mmu_AUTO_GATING

Address: Operational Base + offset (0x00024)
mmu auto gating

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x1	mmu_auto_gating mmu auto gating when it is 1'b1, the mmu will auto gating it self

16.4.5 VDP_HEVC Pref_cache Register Summary

Name	Offset	Size	Reset Value	Description
pref_cache_VERSION	0x00000	W	0xcac20101	VERSION register
pref_cache_SIZE	0x00004	W	0x07110206	L2 cache SIZE
pref_cache_STATUS	0x00008	W	0x00000000	Status register
pref_cache_COMMAND	0x00010	W	0x00000000	Command setting register
pref_cache_CLEAR_PAGE	0x00014	W	0x00000000	clear page register
pref_cache_MAX_READS	0x00018	W	0x0000001c	maximum read register
pref_cache_ENABLE	0x0001c	W	0x00000003	enables cacheable accesses and cache read allocation
pref_cache_PERFCNT_SRC0	0x00020	W	0x00000000	performance counter 0 source register
pref_cache_PERFCNT_VAL0	0x00024	W	0x00000000	performance counter 0 value register
pref_cache_PERFCNT_SRC1	0x00028	W	0x00000000	performance counter 0 source register
pref_cache_PERFCNT_VAL1	0x0002c	W	0x00000000	performance counter 1 value register

Notes:Size: **B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access

16.4.6 VDP_HEVC Pref_cache Detail Register Description**pref_cache_VERSION**

Address: Operational Base + offset (0x000000)
VERSION register

Bit	Attr	Reset Value	Description
31:16	RO	0xcac2	PRODUCT_ID Field0000 Abstract Field0000 Description
15:8	RO	0x01	VERSION_MAJOR Field0000 Abstract Field0000 Description

Bit	Attr	Reset Value	Description
7:0	RO	0x01	VERSION_MINOR Field0000 Abstract Field0000 Description

pref_cache_SIZE

Address: Operational Base + offset (0x00004)

L2 cache SIZE

Bit	Attr	Reset Value	Description
31:24	RO	0x07	External_bus_width Field0000 Abstract Log2 external bus width in bits
23:16	RO	0x11	CACHE_SIZE Field0000 Abstract Log2 cache size in bytes
15:8	RO	0x02	ASSOCIATIVITY Field0000 Abstract Log2 associativity
7:0	RO	0x06	LINE_SIZE Field0000 Abstract Log2 line size in bytes

pref_cache_STATUS

Address: Operational Base + offset (0x00008)

Status register

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	RW	0x0	DATA_BUSY Field0000 Abstract set when the cache is busy handling data
0	RW	0x0	CMD_BUSY Field0000 Abstract set when the cache is busy handling commands

pref_cache_COMMAND

Address: Operational Base + offset (0x00010)

Command setting register

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved
3:0	RW	0x0	COMMAND Field0000 Abstract The possible command is 1 = Clear entire cache

pref_cache_CLEAR_PAGE

Address: Operational Base + offset (0x00014)
 clear page register

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	CLEAR_PAGE Field0000 Abstract writing an address, invalidates all lines in that page from the cache

pref_cache_MAX_READS

Address: Operational Base + offset (0x00018)
 maximum read register

Bit	Attr	Reset Value	Description
31:5	RO	0x0	reserved
4:0	RW	0x1c	MAX_READS Field0000 Abstract Limit the number of outstanding read transactions to this amount

pref_cache_ENABLE

Address: Operational Base + offset (0x0001c)
 enables cacheable accesses and cache read allocation

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved
3	RW	0x0	sw_cache_clk_disgate cache clk disgate cache clk disgate when it is 1'b0, enable cache clk auto clkgating when it is 1'b1, disable cache clk auto clkgating
2	RW	0x0	sw_readbuffer_counter_reject_en counter reject enable default is 1'b0, for enhance cacheable read performnace in readbuffer. 1'b1: normal origin counter reject
1	RW	0x1	permit_cache_read_allocate cache read allocate 1'b1: permit cache read allocate
0	RW	0x1	permit_cacheable_access cacheable access 1'b1: permit cacheable access

pref_cache_PERFCNT_SRC0

Address: Operational Base + offset (0x00020)
 performance counter 0 source register

Bit	Attr	Reset Value	Description
31:7	RO	0x0	reserved
6:0	RW	0x00	<p>PERFCNT_SRC0 Field0000 Abstract This register holds all the possible source values for Performance Counter 0</p> <p>0: disabled 1: total clock cycles 2: active clock cycles 3: read transactions, master 4: word reads, master 5: read transactions, slave 6: word reads, slave 7: read hit, slave 8: read misses, slave 9: read invalidates, slave 10: cacheable read transactions, slave 11: bad hit nmber, slave</p>

pref_cache_PERFCNT_VAL0

Address: Operational Base + offset (0x00024)

performance counter 0 value register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	<p>PERFCNT_VAL0 Field0000 Abstract Performance counter 0 value</p>

pref_cache_PERFCNT_SRC1

Address: Operational Base + offset (0x00028)

performance counter 0 source register

Bit	Attr	Reset Value	Description
31:7	RO	0x0	reserved

Bit	Attr	Reset Value	Description
6:0	RW	0x00	PERFCNT_SRC1 Field0000 Abstract This register holds all the possible source values for Performance Counter 1 0: disabled 1: total clock cycles 2: active clock cycles 3: read transactions, master 4: word reads, master 5: read transactions, slave 6: word reads, slave 7: read hit, slave 8: read misses, slave 9: read invalidates, slave 10: cacheable read transactions, slave 11: bad hit nmber, slave

pref_cache_PERFCNT_VAL1

Address: Operational Base + offset (0x00002c)
 performance counter 1 value register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PERFCNT_VAL1 Field0000 Abstract Performance counter 1 value

16.4.7 VEPU Register Summary

Name	Offset	Size	Reset Value	Description
VEPU_swreg0	0x00000	W	0x48310000	product ID
VEPU_swreg1	0x00004	W	0x00000000	interrupt control and status
VEPU_swreg2	0x00008	W	0x01010010	axi control
VEPU_swreg3	0x0000c	W	0x00000000	test control register
VEPU_swreg4	0x00010	W	0x00000000	reserverd
VEPU_swreg5	0x00014	W	0x00000000	addr_output_stream
VEPU_swreg6	0x00018	W	0x00000000	base address for output control
VEPU_swreg7	0x0001c	W	0x00000000	base address for reference luma
VEPU_swreg8	0x00020	W	0x00000000	base address for reference chroma
VEPU_swreg9	0x00024	W	0x00000000	base address for reconstructed luma
VEPU_swreg10	0x00028	W	0x00000000	base address for reconstructed chroma
VEPU_swreg11	0x0002c	W	0x00000000	base addr for input luma
VEPU_swreg12	0x00030	W	0x00000000	base address for input cb
VEPU_swreg13	0x00034	W	0x00000000	base address for input cr
VEPU_swreg14	0x00038	W	0x00000000	enc control
VEPU_swreg15	0x0003c	W	0x00000000	input image control
VEPU_swreg16	0x00040	W	0x00000000	encoder control regster 0

Name	Offset	Size	Reset Value	Description
VEPU_swreg16_reuse	0x00040	W	0x00000000	
VEPU_swreg17_reuse	0x00044	W	0x00000000	
VEPU_swreg17	0x00044	W	0x00000000	encoder control register 1
VEPU_swreg18	0x00048	W	0x00000000	encoder control register 2
VEPU_swreg19	0x0004c	W	0x00000000	encoder control register 3
VEPU_swreg20	0x00050	W	0x00000000	JPEG control register
VEPU_swreg20_reuse	0x00050	W	0x00000000	JPEG control register
VEPU_swreg21	0x00054	W	0x00000000	encoder control register 4
VEPU_swreg22	0x00058	W	0x00000000	stream header remainder bits MSB
VEPU_swreg23	0x0005c	W	0x00000000	stream header remainder bits LSB
VEPU_swreg24	0x00060	W	0x00000000	stream buffer limit
VEPU_swreg25	0x00064	W	0x00000000	MAD control register
VEPU_swreg26	0x00068	W	0x00000000	
VEPU_swreg26_vp8	0x00068	W	0x00000000	
VEPU_swreg27	0x0006c	W	0x00000000	QP register
VEPU_swreg27_vp8	0x0006c	W	0x00000000	
VEPU_swreg28	0x00070	W	0x00000000	checkpoint 1 and 2
VEPU_swreg28_vp8	0x00070	W	0x00000000	
VEPU_swreg29_vp8	0x00074	W	0x00000000	
VEPU_swreg29	0x00074	W	0x00000000	checkpoint 3 and 4
VEPU_swreg30_vp8	0x00078	W	0x00000000	
VEPU_swreg30	0x00078	W	0x00000000	checkpoint 5 and 6
VEPU_swreg31_vp8	0x0007c	W	0x00000000	
VEPU_swreg31	0x0007c	W	0x00000000	checkpoint 7 and 8
VEPU_swreg32	0x00080	W	0x00000000	checkpoint 9 and 10
VEPU_swreg32_vp8	0x00080	W	0x00000000	
VEPU_swreg33	0x00084	W	0x00000000	checkpoint word error 1 and 2
VEPU_swreg33_vp8	0x00084	W	0x00000000	
VEPU_swreg34_vp8	0x00088	W	0x00000000	
VEPU_swreg34	0x00088	W	0x00000000	checkpoint word error 1 and 2
VEPU_swreg35	0x0008c	W	0x00000000	checkpoint word error 1 and 2
VEPU_swreg35_vp8	0x0008c	W	0x00000000	checkpoint word error 1 and 2
VEPU_swreg36	0x00090	W	0x00000000	checkpoint delta QP register
VEPU_swreg36_vp8	0x00090	W	0x00000000	checkpoint delta QP register
VEPU_swreg37	0x00094	W	0x00000000	rlc control
VEPU_swreg38	0x00098	W	0x00000000	mb control register
VEPU_swreg39	0x0009c	W	0x00000000	Base address for next pic
VEPU_swreg40	0x000a0	W	0x00000000	Stabilization minimum value
VEPU_swreg41	0x000a4	W	0x00000000	Stabilization motion sum
VEPU_swreg42	0x000a8	W	0x00000000	stab_matrix1 and stab_gmv_hor
VEPU_swreg43	0x000ac	W	0x00000000	stab_matrix2 and stab_gmv_ver
VEPU_swreg44	0x000b0	W	0x00000000	stab_matrix3
VEPU_swreg45	0x000b4	W	0x00000000	stab_matrix4

Name	Offset	Size	Reset Value	Description
VEPU_swreg46	0x000b8	W	0x00000000	stab_matrix5
VEPU_swreg47	0x000bc	W	0x00000000	stab_matrix6
VEPU_swreg48	0x000c0	W	0x00000000	stab_matrix7
VEPU_swreg49	0x000c4	W	0x00000000	stab_matrix8
VEPU_swreg50	0x000c8	W	0x00000000	stab_matrix9
VEPU_swreg51	0x000cc	W	0x00000000	cabac_table_addr
VEPU_swreg52	0x000d0	W	0x00000000	Base address for MV output
VEPU_swreg53	0x000d4	W	0x00000000	RGB to YUV conversion coefficien A and B
VEPU_swreg54	0x000d8	W	0x00000000	RGB to YUV conversion coefficien C and E
VEPU_swreg55	0x000dc	W	0x00000000	RGB mask MSB bit
VEPU_swreg56	0x000e0	W	0x00000000	intra area control register
VEPU_swreg57	0x000e4	W	0x00000000	CIR intra control reg
VEPU_swreg58_vp8	0x000e8	W	0x00000000	
VEPU_swreg58	0x000e8	W	0x00000000	Intra slice bitmap for slices 0..31
VEPU_swreg59_vp8	0x000ec	W	0x00000000	
VEPU_swreg59	0x000ec	W	0x00000000	Intra slice bitmap for slices32..63
VEPU_swreg60	0x000f0	W	0x00000000	1st ROI area register
VEPU_swreg61	0x000f4	W	0x00000000	Register0061 Abstract
VEPU_swreg62	0x000f8	W	0x00000000	MVC control reg
VEPU_swreg63	0x000fc	W	0x1f522780	Register0063 Abstract
VEPU_swreg64	0x00100	W	0x00000000	JPEG luma quantization 1
VEPU_swreg64_vp8	0x00100	W	0x00000000	
VEPU_swreg65_vp8	0x00104	W	0x00000000	
VEPU_swreg65	0x00104	W	0x00000000	JPEG luma quantization 2
VEPU_swreg66_vp8	0x00108	W	0x00000000	
VEPU_swreg66	0x00108	W	0x00000000	JPEG luma quantization 3
VEPU_swreg67_vp8	0x0010c	W	0x00000000	
VEPU_swreg67	0x0010c	W	0x00000000	JPEG luma quantization 4
VEPU_swreg68_vp8	0x00110	W	0x00000000	
VEPU_swreg68	0x00110	W	0x00000000	JPEG luma quantization 5
VEPU_swreg69_vp8	0x00114	W	0x00000000	
VEPU_swreg69	0x00114	W	0x00000000	JPEG luma quantization 6
VEPU_swreg70_vp8	0x00118	W	0x00000000	
VEPU_swreg70	0x00118	W	0x00000000	JPEG luma quantization 7
VEPU_swreg71_vp8	0x0011c	W	0x00000000	JPEG luma quantization 7
VEPU_swreg71	0x0011c	W	0x00000000	JPEG luma quantization 8
VEPU_swreg72	0x00120	W	0x00000000	JPEG luma quantization 9
VEPU_swreg72_vp8	0x00120	W	0x00000000	
VEPU_swreg73	0x00124	W	0x00000000	Register0073 Abstract
VEPU_swreg73_vp8	0x00124	W	0x00000000	
VEPU_swreg74_vp8	0x00128	W	0x00000000	

Name	Offset	Size	Reset Value	Description
VEPU_swreg74	0x00128	W	0x00000000	JPEG luma quantization 11
VEPU_swreg75	0x0012c	W	0x00000000	JPEG luma quantization 12
VEPU_swreg75_vp8	0x0012c	W	0x00000000	
VEPU_swreg76_vp8	0x00130	W	0x00000000	
VEPU_swreg76	0x00130	W	0x00000000	JPEG luma quantization 13
VEPU_swreg77_vp8	0x00134	W	0x00000000	
VEPU_swreg77	0x00134	W	0x00000000	JPEG luma quantization 14
VEPU_swreg78_vp8	0x00138	W	0x00000000	
VEPU_swreg78	0x00138	W	0x00000000	JPEG luma quantization 15
VEPU_swreg79	0x0013c	W	0x00000000	JPEG luma quantization 16
VEPU_swreg79_vp8	0x0013c	W	0x00000000	
VEPU_swreg80_vp8	0x00140	W	0x00000000	
VEPU_swreg80	0x00140	W	0x00000000	JPEG chroma quantization 1
VEPU_swreg81	0x00144	W	0x00000000	JPEG chroma quantization 2
VEPU_swreg81_vp8	0x00144	W	0x00000000	
VEPU_swreg82_vp8	0x00148	W	0x00000000	
VEPU_swreg82	0x00148	W	0x00000000	JPEG chroma quantization 3
VEPU_swreg83	0x0014c	W	0x00000000	JPEG chroma quantization 4
VEPU_swreg83_vp8	0x0014c	W	0x00000000	
VEPU_swreg84_vp8	0x00150	W	0x00000000	
VEPU_swreg84	0x00150	W	0x00000000	JPEG chroma quantization 5
VEPU_swreg85	0x00154	W	0x00000000	JPEG chroma quantization 6
VEPU_swreg85_vp8	0x00154	W	0x00000000	
VEPU_swreg86_vp8	0x00158	W	0x00000000	
VEPU_swreg86	0x00158	W	0x00000000	JPEG chroma quantization 7
VEPU_swreg87	0x0015c	W	0x00000000	JPEG chroma quantization 8
VEPU_swreg87_vp8	0x0015c	W	0x00000000	
VEPU_swreg88_vp8	0x00160	W	0x00000000	
VEPU_swreg88	0x00160	W	0x00000000	JPEG chroma quantization 9
VEPU_swreg89_vp8	0x00164	W	0x00000000	
VEPU_swreg89	0x00164	W	0x00000000	JPEG chroma quantization 10
VEPU_swreg90_vp8	0x00168	W	0x00000000	
VEPU_swreg90	0x00168	W	0x00000000	JPEG chroma quantization 11
VEPU_swreg91_vp8	0x0016c	W	0x00000000	
VEPU_swreg91	0x0016c	W	0x00000000	JPEG chroma quantization 12
VEPU_swreg92_vp8	0x00170	W	0x00000000	
VEPU_swreg92	0x00170	W	0x00000000	JPEG chroma quantization 13
VEPU_swreg93_vp8	0x00174	W	0x00000000	
VEPU_swreg93	0x00174	W	0x00000000	JPEG chroma quantization 14
VEPU_swreg94_vp8	0x00178	W	0x00000000	
VEPU_swreg94	0x00178	W	0x00000000	JPEG chroma quantization 15
VEPU_swreg95_vp8	0x0017c	W	0x00000000	
VEPU_swreg95	0x0017c	W	0x00000000	JPEG chroma quantization 16

Name	Offset	Size	Reset Value	Description
VEPU_swreg96	0x00180	W	0x00000000	DMV 4p/1p penalty values 0-3
VEPU_swreg97	0x00184	W	0x00000000	DMV 4p/1p penalty values 4-7
VEPU_swreg98	0x00188	W	0x00000000	DMV 4p/1p penalty values
VEPU_swreg99	0x0018c	W	0x00000000	DMV 4p/1p penalty values
VEPU_swreg100	0x00190	W	0x00000000	DMV 4p/1p penalty values
VEPU_swreg101	0x00194	W	0x00000000	DMV 4p/1p penalty values
VEPU_swreg102	0x00198	W	0x00000000	DMV 4p/1p penalty values
VEPU_swreg103	0x0019c	W	0x00000000	DMV 4p/1p penalty values
VEPU_swreg104	0x001a0	W	0x00000000	DMV 4p/1p penalty values
VEPU_swreg105	0x001a4	W	0x00000000	DMV 4p/1p penalty values
VEPU_swreg106	0x001a8	W	0x00000000	DMV 4p/1p penalty values
VEPU_swreg107	0x001ac	W	0x00000000	DMV 4p/1p penalty values
VEPU_swreg108	0x001b0	W	0x00000000	DMV 4p/1p penalty values
VEPU_swreg109	0x001b4	W	0x00000000	DMV 4p/1p penalty values
VEPU_swreg110	0x001b8	W	0x00000000	DMV 4p/1p penalty values
VEPU_swreg111	0x001bc	W	0x00000000	DMV 4p/1p penalty values
VEPU_swreg112	0x001c0	W	0x00000000	DMV 4p/1p penalty values
VEPU_swreg113	0x001c4	W	0x00000000	DMV 4p/1p penalty values
VEPU_swreg114	0x001c8	W	0x00000000	DMV 4p/1p penalty values
VEPU_swreg115	0x001cc	W	0x00000000	DMV 4p/1p penalty values
VEPU_swreg116	0x001d0	W	0x00000000	DMV 4p/1p penalty values
VEPU_swreg117	0x001d4	W	0x00000000	DMV 4p/1p penalty values
VEPU_swreg118	0x001d8	W	0x00000000	DMV 4p/1p penalty values
VEPU_swreg119	0x001dc	W	0x00000000	DMV 4p/1p penalty values
VEPU_swreg120	0x001e0	W	0x00000000	DMV 4p/1p penalty values
VEPU_swreg121	0x001e4	W	0x00000000	DMV 4p/1p penalty values
VEPU_swreg122	0x001e8	W	0x00000000	DMV 4p/1p penalty values
VEPU_swreg123	0x001ec	W	0x00000000	DMV 4p/1p penalty values
VEPU_swreg124	0x001f0	W	0x00000000	DMV 4p/1p penalty values
VEPU_swreg125	0x001f4	W	0x00000000	DMV 4p/1p penalty values
VEPU_swreg126	0x001f8	W	0x00000000	DMV 4p/1p penalty values
VEPU_swreg127	0x001fc	W	0x00000000	DMV 4p/1p penalty values
VEPU_swreg128	0x00200	W	0x00000000	DMV 4p/1p penalty values
VEPU_swreg129	0x00204	W	0x00000000	DMV 4p/1p penalty values
VEPU_swreg130	0x00208	W	0x00000000	DMV 4p/1p penalty values
VEPU_swreg131	0x0020c	W	0x00000000	DMV 4p/1p penalty values
VEPU_swreg132	0x00210	W	0x00000000	DMV 4p/1p penalty values
VEPU_swreg133	0x00214	W	0x00000000	DMV 4p/1p penalty values
VEPU_swreg134	0x00218	W	0x00000000	DMV 4p/1p penalty values
VEPU_swreg135	0x0021c	W	0x00000000	DMV 4p/1p penalty values
VEPU_swreg136	0x00220	W	0x00000000	DMV 4p/1p penalty values
VEPU_swreg137	0x00224	W	0x00000000	DMV 4p/1p penalty values
VEPU_swreg138	0x00228	W	0x00000000	DMV 4p/1p penalty values

Name	Offset	Size	Reset Value	Description
VEPU_swreg139	0x0022c	W	0x00000000	DMV 4p/1p penalty values
VEPU_swreg140	0x00230	W	0x00000000	DMV 4p/1p penalty values
VEPU_swreg141	0x00234	W	0x00000000	DMV 4p/1p penalty values
VEPU_swreg142	0x00238	W	0x00000000	DMV 4p/1p penalty values
VEPU_swreg143	0x0023c	W	0x00000000	DMV 4p/1p penalty values
VEPU_swreg144	0x00240	W	0x00000000	DMV 4p/1p penalty values
VEPU_swreg145	0x00244	W	0x00000000	DMV 4p/1p penalty values
VEPU_swreg146	0x00248	W	0x00000000	DMV 4p/1p penalty values
VEPU_swreg147	0x0024c	W	0x00000000	DMV 4p/1p penalty values
VEPU_swreg148	0x00250	W	0x00000000	DMV 4p/1p penalty values
VEPU_swreg149	0x00254	W	0x00000000	DMV 4p/1p penalty values
VEPU_swreg150	0x00258	W	0x00000000	DMV 4p/1p penalty values
VEPU_swreg151	0x0025c	W	0x00000000	DMV 4p/1p penalty values
VEPU_swreg152	0x00260	W	0x00000000	DMV 4p/1p penalty values
VEPU_swreg153	0x00264	W	0x00000000	DMV 4p/1p penalty values
VEPU_swreg154	0x00268	W	0x00000000	DMV 4p/1p penalty values
VEPU_swreg155	0x0026c	W	0x00000000	DMV 4p/1p penalty values
VEPU_swreg156	0x00270	W	0x00000000	DMV 4p/1p penalty values
VEPU_swreg157	0x00274	W	0x00000000	DMV 4p/1p penalty values
VEPU_swreg158	0x00278	W	0x00000000	DMV 4p/1p penalty values
VEPU_swreg159	0x0027c	W	0x00000000	DMV 4p/1p penalty values
VEPU_swreg160	0x00280	W	0x00000000	vp8 control
VEPU_swreg161	0x00284	W	0x00000000	VP8 bit cost of golden ref frame
VEPU_swreg162	0x00288	W	0x00000000	vp8 loop filter delta registers
VEPU_swreg163	0x0028c	W	0x00000000	vp8 loop filter delta register

Notes: Size : **B** - Byte (8 bits) access, **HW** - Half WORD (16 bits) access, **W** -WORD (32 bits) access

16.4.8 Detail Register Description

VEPU_swreg0

Address: Operational Base + offset (0x00000)

product ID

Bit	Attr	Reset Value	Description
31:16	RO	0x4831	prod_id Product ID
15:12	RW	0x0	major_num Major number
11:4	RW	0x00	minor_num Minor number
3:0	RW	0x0	synthesis

VEPU_swreg1

Address: Operational Base + offset (0x00004)

interrupt control and status

Bit	Attr	Reset Value	Description
31:9	RO	0x0	reserved
8	RW	0x0	irq_slice_ready IRQ slice ready status bit
7	RO	0x0	reserved
6	RW	0x0	irq_timeout IRQ HW timeout status bit
5	RW	0x0	irq_buffer_full irq buffer full
4	RW	0x0	irq_reset irq SW reset
3	RW	0x0	irq_bus_error
2	RW	0x0	irq_frame_rdy IRQ frame ready status bit. Encoder has finished a frame
1	RW	0x0	irq_dis IRQ disable. No interrupts from HW. SW must use polling
0	RW	0x0	enc_irq HINTenc interrupt from HW. SW resets at IRQ handler.

VEPU_swreg2

Address: Operational Base + offset (0x000008)

axi control

Bit	Attr	Reset Value	Description
31:24	RW	0x01	axi_write_id axi write id axi write id
23:16	RW	0x01	axi_rd_id axi read id axi read id
15	RW	0x0	output_swap16 enable output swap 16-bits
14	RW	0x0	input_swap16 enable input swap 16-bits
13:8	RW	0x00	burst_len burst length
7	RW	0x0	disable_burst disable burst mode for AXI disable burst mode for AXI bus

Bit	Attr	Reset Value	Description
6	RW	0x0	burst_incr burst increment burst increment. 1: INCR burst allowed 0: use SINGLE burst
5	RW	0x0	burst_discard enable burst data dicard enable burst data dicard. 2 or 3 long reads are using BURST4
4	RW	0x1	clk_gating_en enable clock gating enable clock gating
3	RW	0x0	output_swap32 enable output swap 32-bits enable output swap 32-bits
2	RW	0x0	input_swap32 enable input swap 32-bits enable input swap 32-bits
1	RW	0x0	output_swap8 enable output swap 8-bits enable output swap 8-bits
0	RW	0x0	input_swap8 enable input swap 8-bits enable input swap 8-bits

VEPU_swreg3

Address: Operational Base + offset (0x0000c)
test control register

Bit	Attr	Reset Value	Description
31:28	RW	0x0	test_counter test counter
27:21	RO	0x0	reserved
20:3	RW	0x00000	test_len test data length
2	RW	0x0	test_memory test memory coherency
1	RW	0x0	test_reg test register coherency
0	RW	0x0	test_irq test irq

VEPU_swreg4

Address: Operational Base + offset (0x00010)
reserverd

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	Field0000 Abstract Field0000 Description

VEPU_swreg5

Address: Operational Base + offset (0x00014)
addr_output_stream

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	addr_output_stream base address for output stream

VEPU_swreg6

Address: Operational Base + offset (0x00018)
base address for output control

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	addr_output_control base address for output control base address for output control

VEPU_swreg7

Address: Operational Base + offset (0x0001c)
base address for reference luma

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	addr_reflum base address for reference luma base address for reference luma

VEPU_swreg8

Address: Operational Base + offset (0x00020)
base address for reference chroma

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	addr_refchroma base address for reference chroma base address for reference chroma

VEPU_swreg9

Address: Operational Base + offset (0x00024)
base address for reconstructed luma

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	addr_recon_luma base address for reconstructed luma

VEPU_swreg10

Address: Operational Base + offset (0x00028)

base address for reconstructed chroma

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	addr_recon_chroma base address for reconstructed chroma

VEPU_swreg11

Address: Operational Base + offset (0x0002c)

base addr for input luma

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	addr_input_luma base addr for input luma

VEPU_swreg12

Address: Operational Base + offset (0x00030)

base address for input cb

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	addr_input_cb base address for input cb

VEPU_swreg13

Address: Operational Base + offset (0x00034)

base address for input cr

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	addr_input_cr base address for input cr

VEPU_swreg14

Address: Operational Base + offset (0x00038)

enc control

Bit	Attr	Reset Value	Description
31	RW	0x0	int_timeout_en enable interrupt for timeout
30	RW	0x0	mv_sad_wren enable writing MV and SAD of each MB to BaseMvWrite
29	RW	0x0	nal_mode NAL size output to base control
28	RW	0x0	slice_rdyint_en enable interrupt for slice ready
27:19	RW	0x000	enc_width encoder width. lumwidth (macroblocks) H264: [9...255] JPEG: [6...511]

Bit	Attr	Reset Value	Description
18:10	RW	0x000	enc_height encoderd height, lumHeight (macroblocks) H264: [6..255] JPEG: [6..511]
9:7	RO	0x0	reserved
6	RW	0x0	rocon_write_dis disable writing of reconstructed image. recWriteDisable
5	RO	0x0	reserved
4:3	RW	0x0	enc_pic_type encoder picture type. frame type 0: INTER 1: INTRA(IDR) 2: MVC-INTER
2:1	RW	0x0	enc_mode encoding mode. stream type , 1=VP8, 2=JPEG,3=H264
0	RW	0x0	enc_en encoder enable

VEPU_swreg15

Address: Operational Base + offset (0x0003c)

input image control

Bit	Attr	Reset Value	Description
31:29	RW	0x0	input_chroma_offset input chrominance offset (bytes)
28:26	RW	0x0	input_lum_offset input luminance offset(bytes)
25:12	RW	0x0000	input_row_len input luminance row length
11:10	RW	0x0	overfill_right overfill pixels on right edge of image div4[0...3]
9:6	RW	0x0	overfill_bot overfill pixels on bottom edge of image. YFill [0..15]
5:2	RW	0x0	input_format input image format. YUV420P/YUV420SP/YUV422/UYVY422/RGB5 65/RGB444/RGB888/RGB101010
1:0	RW	0x0	imagein_rotmode input image rotation 0: disabled 1: 90 degress rigth 2: 90 degress left

VEPU_swreg16

Address: Operational Base + offset (0x00040)
encoder control register 0

Bit	Attr	Reset Value	Description
31:26	RW	0x00	init_qp H.264 pic init qp in PPS[0...51]
25:22	RW	0x0	slice_alpha H.264 slice filter alpha c0 offset div2 [-66]
21:18	RW	0x0	slice_beta h.264 slice filter beta offset div2 [-6 ...6]
17:13	RW	0x00	chroma_qp_offset H264 chroma qp index offset [-12...12]
12:9	RO	0x0	reserved
8	RW	0x0	sw_qpass jpeg enc quant bypass
7:5	RO	0x0	reserved
4:1	RW	0x0	idr_picid IDR pic ID
0	RW	0x0	constr_intra_pred constrained intra prediction

VEPU_swreg16_reuse

Address: Operational Base + offset (0x00040)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	luma_sec_ref_addr Base address for second reference luma

VEPU_swreg17_reuse

Address: Operational Base + offset (0x00044)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	chroma_sec_ref_addr Base address for second reference chroma

VEPU_swreg17

Address: Operational Base + offset (0x00044)
encoder control register 1

Bit	Attr	Reset Value	Description
31:24	RW	0x00	pic_parameter_set_id H.264 pic_parameter_set_id
23:16	RW	0x00	intra_pred_mode H.264 intra prediction previous 4x4 mode favor

Bit	Attr	Reset Value	Description
15:0	RW	0x0000	frame_num H.264 frame number

VEPU_swreg18

Address: Operational Base + offset (0x00048)

encoder control register 2

Bit	Attr	Reset Value	Description
31:30	RW	0x0	deblocking_filter_mode Deblocking filter mode. 0=enabled. 1=disabled (vp8=simple). 2=disabled on slice
29:23	RW	0x00	h264_slice_size H.264 Slice size. mbRowPerSlice (mb rows) [0..127] 0=one slice per picture
22	RW	0x0	disable_quarter_pixmv H.264 Disable quarter pixel MVs. disableQuarterPixelMv
21	RW	0x0	transform8x8_mode_en H.264 Transform 8x8 enable. High Profile H.264. transform8x8Mode
20:19	RW	0x0	cabac_int_idc H.264 CABAC initial IDC. [0..2]
18	RW	0x0	entropy_coding_mode H.264 CABAC / VP8 boolenc enable. entropyCodingMode. 0=CAVLC (Baseline Profile H.264). 1=CABAC (Main Profile H.264)
17	RW	0x0	h264_inter4x4_mode H.264 Inter 4x4 mode restriction. restricted4x4Mode
16	RW	0x0	h264_stream_mode H.264 Stream mode. 0=NAL unit stream. 1=Byte stream
15:0	RW	0x0000	intra16x16_mode Intra prediction intra 16x16 mode favor

VEPU_swreg19

Address: Operational Base + offset (0x0004c)

encoder control register 3

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved

Bit	Attr	Reset Value	Description
30	RW	0x0	mutimv_en Enable using more than 1 MV per macroblock.
29:20	RW	0x000	mv_penalty_1_4p Differential MV penalty for 1/4p ME. DMVPenaltyQp
19:10	RW	0x000	mv_penalty_4p Differential MV penalty for 4p ME. DMVPenalty4p
9:0	RW	0x000	mv_penalty_1p differential MV penalty for 1p

VEPU_swreg20

Address: Operational Base + offset (0x00050)

JPEG control register

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x000	mv_penalty_16x8_8x16 Penalty for using 16x8 or 8x16 MV.
19:10	RW	0x000	mv_penalty_8x8 Penalty for using 8x8 MV
9:0	RW	0x000	mv_penalty_8x4_4x8 Penalty for using 8x4 or 4x8 MV.

VEPU_swreg20_reuse

Address: Operational Base + offset (0x00050)

JPEG control register

Bit	Attr	Reset Value	Description
31:26	RO	0x0	reserved
25	RW	0x0	jpeg_mode JPEG mode. 0=4:2:0 (4lum+2chr blocks/MCU). 1=4:2:2 (2lum+2chr blocks/MCU)
24	RW	0x0	jpeg_slic_en Field0000 Abstract JPEG slice enable. 0=picture ends with EOI. 1=slice ends with RST
23:16	RW	0x00	jpeg_RST_mark_inter Field0001 Abstract JPEG restart marker interval when slices are disabled (mb)
15:0	RW	0x0000	jpeg_RST_mark_1 rows) [0..255] JPEG restart marker for first RST. incremented by HW for next RST

VEPU_swreg21

Address: Operational Base + offset (0x00054)

encoder control register 4

Bit	Attr	Reset Value	Description
31:24	RW	0x00	macroblock_penalty H.264 SKIP macroblock mode / VP8 zero/nearest/near mode penalty
23:16	RW	0x00	completed_slices H.264 amount of completed slices.
15:0	RW	0x0000	inter_mode inter MB mode favor in intra/inter selection

VEPU_swreg22

Address: Operational Base + offset (0x00058)

stream header remainder bits MSB

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	strm_hdr_rem stream header remainder bits MSB stream header remainder bits MSB

VEPU_swreg23

Address: Operational Base + offset (0x0005c)

stream header remainder bits LSB

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	strm_hdr_rem2 stream header remainder bits LSB

VEPU_swreg24

Address: Operational Base + offset (0x00060)

stream buffer limit

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	strm_buffer_limit stream buffer limit

VEPU_swreg25

Address: Operational Base + offset (0x00064)

MAD control register

Bit	Attr	Reset Value	Description
31:28	RW	0x0	QP_adjust MAD based QP adjustment. madQpChange [-8..7]
27:22	RW	0x00	MAD_threshold MAD threshold div256
21	RO	0x0	reserved

Bit	Attr	Reset Value	Description
20:0	RW	0x0000000	qp_sum_div2 QP sum div2 output

VEPU_swreg26

Address: Operational Base + offset (0x00068)

Bit	Attr	Reset Value	Description
31:0	RW	0x000000000	intra_slice_bitmap Field0000 Abstract Intra slice bitmap for slices 64..95. LSB=slice64. MSB=slice95. 1=intra.

VEPU_swreg26_vp8

Address: Operational Base + offset (0x00068)

Bit	Attr	Reset Value	Description
31:0	RW	0x000000000	vp8_pro_update_cnt_addr Field0000 Abstract Base address for VP8 counters for probability updates

VEPU_swreg27

Address: Operational Base + offset (0x0006c)

QP register

Bit	Attr	Reset Value	Description
31:26	RW	0x00	qp_lum H.264 Initial QP. qpLum [0..51]
25:20	RW	0x00	qp_max H.264 Minimum QP. qpMax [0..51]
19:14	RW	0x00	qp_min H.264 Minimum QP. qpMin [0..51]
13	RO	0x0	reserved
12:0	RW	0x0000	checkpoint_distan checkpoint distance checkpoint distance

VEPU_swreg27_vp8

Address: Operational Base + offset (0x0006c)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:23	RW	0x00	vp8_y1_round_dc VP8 qpY1RoundDc 8b

Bit	Attr	Reset Value	Description
22:14	RW	0x000	vp8_y1_zbin_dc VP8 qpY1ZbinDc
13:0	RW	0x0000	vp8_y1_quant_dc checkpoint distance VP8 qpY1QuantDc

VEPU_swreg28

Address: Operational Base + offset (0x00070)
checkpoint 1 and 2

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	checkp_1 checkpoint 1 word target/usage
15:0	RW	0x0000	checkp_2 checkpoint 2 word target/usage

VEPU_swreg28_vp8

Address: Operational Base + offset (0x00070)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:23	RW	0x00	vp8_y1_round_ac VP8 qpY1RoundAc
22:14	RW	0x000	vp8_y1_zbin_ac VP8 qpY1ZbinAc
13:0	RW	0x0000	vp8_y1_quant_ac checkpoint distance VP8 qpY1QuantAc

VEPU_swreg29_vp8

Address: Operational Base + offset (0x00074)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:23	RW	0x00	vp8_y2_round_dc VP8 qpY2RoundDc
22:14	RW	0x000	vp8_y2_zbin_dc VP8 qpY2ZbinDc
13:0	RW	0x0000	vp8_y2_quant_dc checkpoint distance VP8 qpY2QuantDc

VEPU_swreg29

Address: Operational Base + offset (0x00074)
checkpoint 3 and 4

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	checkp_3 checkpoint 3 word target/usage
15:0	RW	0x0000	checkp_4 checkpoint 4 word target/usage checkpoint 4 word target/usage

VEPU_swreg30_vp8

Address: Operational Base + offset (0x00078)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:23	RW	0x00	vp8_y2_round_ac VP8 qpY2RoundAc
22:14	RW	0x000	vp8_y2_zbin_ac VP8 qpY2ZbinAc
13:0	RW	0x0000	vp8_y2_quant_ac checkpoint distance VP8 qpY2QuantAc

VEPU_swreg30

Address: Operational Base + offset (0x00078)

checkpoint 5 and 6

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	checkp_5 checkpoint 5 word target/usage
15:0	RW	0x0000	checkp_6 checkpoint 6 word target/usage checkpoint 6 word target/usage

VEPU_swreg31_vp8

Address: Operational Base + offset (0x0007c)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:23	RW	0x00	vp8_ch_round_dc VP8 qpChRoundDc
22:14	RW	0x000	vp8_ch_zbin_dc VP8 qpChZbinDc
13:0	RW	0x0000	vp8_ch_quant_dc checkpoint distance VP8 qpChQuantDc

VEPU_swreg31

Address: Operational Base + offset (0x0007c)

checkpoint 7 and 8

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	checkp_7 checkpoint 7 word target/usage
15:0	RW	0x0000	checkp_8 checkpoint 8 word target/usage checkpoint 8 word target/usage

VEPU_swreg32

Address: Operational Base + offset (0x00080)

checkpoint 9 and 10

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	checkp_9 checkpoint 9 word target/usage
15:0	RW	0x0000	checkp_10 checkpoint 10 word target/usage checkpoint 10 word target/usage

VEPU_swreg32_vp8

Address: Operational Base + offset (0x00080)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:23	RW	0x00	vp8_ch_round_ac VP8 qpChRoundAc
22:14	RW	0x000	vp8_ch_zbin_ac VP8 qpChZbinAc
13:0	RW	0x0000	vp8_ch_quant_ac checkpoint distance VP8 qpChQuantAc

VEPU_swreg33

Address: Operational Base + offset (0x00084)

checkpoint word error 1 and 2

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	checkp_error1 checkpoint word error 1
15:0	RW	0x0000	checkp_error2 checkpoint word error 2

VEPU_swreg33_vp8

Address: Operational Base + offset (0x00084)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved

Bit	Attr	Reset Value	Description
27:26	RW	0x0	vp8_1st_reffme_mvrefidx VP8 mvRefIdx for first reference frame. 0=ipf. 1=grf. 2=arf.
25:17	RW	0x000	vp8_y2_dequant_dc VP8 qpY2DequantDc
16:8	RW	0x000	vp8_y1_dequant_ac VP8 qpY1DequantAc
7:0	RW	0x00	vp8_y1_dequant_dc checkpoint distance VP8 qpY1DequantDc

VEPU_swreg34_vp8

Address: Operational Base + offset (0x00088)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30	RW	0x0	vp8_seg_update_en Field0000 Abstract VP8 enable for segmentation map update. Map is different from previous frame and is written in stream.
29	RW	0x0	vp8_seg_en Field0000 Abstract VP8 enable for segmentation. Segmentation map is stored in BaseVp8SegmentMap.
28	RW	0x0	vp8_2st_reffme_en Field0000 Abstract VP8 enable for second reference frame.
27:26	RW	0x0	vp8_2st_reffme_mvrefidx VP8 mvRefIdx for second reference frame. 0=ipf. 1=grf. 2=arf.
25:17	RW	0x000	vp8_ch_dequant_ac VP8 qpChDequantAc
16:9	RW	0x00	vp8_ch_dequant_dc VP8 qpChDequantDc
8:0	RW	0x000	vp8_y2_dequant_ac checkpoint distance VP8 qpY2DequantAc

VEPU_swreg34

Address: Operational Base + offset (0x00088)

checkpoint word error 1 and 2

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	checkp_error3 checkpoint word error 3
15:0	RW	0x0000	checkp_error4 checkpoint word error 4

VEPU_swreg35

Address: Operational Base + offset (0x0008c)

checkpoint word error 1 and 2

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	checkp_error5 checkpoint word error 5
15:0	RW	0x0000	checkp_error6 checkpoint word error 6

VEPU_swreg35_vp8

Address: Operational Base + offset (0x0008c)

checkpoint word error 1 and 2

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	vp8_bool_value VP8 boolEncValue VP8 Penalty value for second reference frame zero-mv [0..255]

VEPU_swreg36

Address: Operational Base + offset (0x00090)

checkpoint delta QP register

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:24	RW	0x0	checkp_qp_1 checkpoint delta QP 1
23:20	RW	0x0	checkp_qp_2 checkpoint delta QP 2
19:16	RW	0x0	checkp_qp_3 checkpoint delta QP 3
15:12	RW	0x0	checkp_qp_4 checkpoint delta QP 4
11:8	RW	0x0	checkp_qp_5 checkpoint delta QP 5
7:4	RW	0x0	checkp_qp_6 checkpoint delta QP 6
3:0	RW	0x0	checkp_qp_7 checkpoint delta QP 7

VEPU_swreg36_vp8

Address: Operational Base + offset (0x00090)

checkpoint delta QP register

Bit	Attr	Reset Value	Description
31:24	RW	0x00	vp8_2st_reffme_pena Field0000 Abstract VP8 Penalty value for second reference frame zero-mv [0..255]
23:21	RW	0x0	vp8_dblk_fil_shps Field0000 Abstract VP8 Deblocking filter sharpness [0..7]
20:15	RW	0x00	vp8_dblk_fil_lev Field0000 Abstract VP8 Deblocking filter level [0..63]
14:13	RW	0x0	vp8_dct_ptton_cnt Field0000 Abstract VP8 DCT partition count. 0=1. 1=2 [0..1]
12:8	RW	0x00	vp8_bool_bits_minus8 Field0000 Abstract VP8 boolEncValueBitsMinus8 [0..23]
7:0	RW	0x00	vp8_bool_range VP8 boolEncRange [0..255]

VEPU_swreg37

Address: Operational Base + offset (0x00094)

rlc control

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:23	RW	0x00	stream_st_offset Field0000 Description
22	RO	0x0	reserved
21:0	RW	0x000000	rlc_sum rlc sum rlc sum

VEPU_swreg38

Address: Operational Base + offset (0x00098)

mb control register

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	macroblock_count Field0000 Description

Bit	Attr	Reset Value	Description
15:0	RW	0x0000	mb_count_out Field0000 Description

VEPU_swreg39

Address: Operational Base + offset (0x0009c)

Base address for next pic

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	next_pic_addr Base address for next pic Base address for next pic luminance

VEPU_swreg40

Address: Operational Base + offset (0x000a0)

Stabilization minimum value

Bit	Attr	Reset Value	Description
31:30	RW	0x0	stab_mode Stabilization mode. 0=disabled. 1=stab only. 2=stab+encode
29:24	RO	0x0	reserved
23:0	RW	0x000000	stab_min_value Stabilization minimum value output. max 253*253*255

VEPU_swreg41

Address: Operational Base + offset (0x000a4)

Stabilization motion sum

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	stab_motion_sum Stabilization motion sum div8 output. max 53*253*255*1089/8

VEPU_swreg42

Address: Operational Base + offset (0x000a8)

stab_matrix1 and stab_gmv_hor

Bit	Attr	Reset Value	Description
31:26	RW	0x00	stab_gmv_hor Stabilization GMV horizontal output [-16..16]
25:24	RO	0x0	reserved
23:0	RW	0x000000	stab_matrix1 Stabilization matrix 1 (up-left position) output

VEPU_swreg43

Address: Operational Base + offset (0x000ac)

stab_matrix2 and stab_gmv_ver

Bit	Attr	Reset Value	Description
31:26	RW	0x00	stab_gmv_ver Stabilization GMV vertical output [-16..16]
25:24	RO	0x0	reserved
23:0	RW	0x000000	stab_matrix2 Stabilization matrix 2 (up position) output

VEPU_swreg44

Address: Operational Base + offset (0x000b0)

stab_matrix3

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23:0	RW	0x000000	stab_matrix3 Stabilization matrix 3 (up-right position) output

VEPU_swreg45

Address: Operational Base + offset (0x000b4)

stab_matrix4

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23:0	RW	0x000000	stab_matrix4 Stabilization matrix 4 (left position) output

VEPU_swreg46

Address: Operational Base + offset (0x000b8)

stab_matrix5

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23:0	RW	0x000000	stab_matrix5 Stabilization matrix 5 (GMV position) output

VEPU_swreg47

Address: Operational Base + offset (0x000bc)

stab_matrix6

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23:0	RW	0x000000	stab_matrix6 Stabilization matrix 6 (right position) output

VEPU_swreg48

Address: Operational Base + offset (0x000c0)

stab_matrix7

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23:0	RW	0x0000000	stab_matrix7 Stabilization matrix 7 (down-left position) output

VEPU_swreg49

Address: Operational Base + offset (0x000c4)

stab_matrix8

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23:0	RW	0x0000000	stab_matrix8 Stabilization matrix 8 (down position) output

VEPU_swreg50

Address: Operational Base + offset (0x000c8)

stab_matrix9

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23:0	RW	0x0000000	stab_matrix9 Stabilization matrix 9 (down-right position) output

VEPU_swreg51

Address: Operational Base + offset (0x000cc)

cabac_table_addr

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	cabac_table_addr Base address for cabac context tables (H264) or probability tables (VP8)

VEPU_swreg52

Address: Operational Base + offset (0x000d0)

Base address for MV output

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	mv_out_addr Base address for MV output writing

VEPU_swreg53

Address: Operational Base + offset (0x000d4)

RGB to YUV conversion coefficient A and B

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	coeffB_RGB2YUV RGB to YUV conversion B RGB to YUV conversion coefficient B
15:0	RW	0x0000	coeffA_RGB2YUV RGB to YUV conversion coefficient A

VEPU_swreg54

Address: Operational Base + offset (0x000d8)

RGB to YUV conversion coefficient C and E

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	coeffE_RGB2YUV RGB to YUV conversion coefficient E
15:0	RW	0x0000	coeffC_RGB2YUV RGB to YUV conversion coefficient C

VEPU_swreg55

Address: Operational Base + offset (0x000dc)

RGB mask MSB bit

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:26	RW	0x00	Bmask_MST RGB B-component mask MSB bit position [0..31]
25:21	RW	0x00	Gmask_MST RGB G-component mask MSB bit position [0..31]
20:16	RW	0x00	Rmask_MST RGB R-component mask MSB bit position [0..31]
15:0	RW	0x0000	coeffF_RGB2YUV RGB to YUV conversion coefficient F

VEPU_swreg56

Address: Operational Base + offset (0x000e0)

intra area control register

Bit	Attr	Reset Value	Description
31:24	RW	0x00	intra_left_mb Intra area left mb column (inside area) [0..255]
23:16	RW	0x00	intra_right_mb Intra area right mb column (inside area) [0..255]
15:8	RW	0x00	intra_top_mb Intra area top mb row (inside area) [0..255]

Bit	Attr	Reset Value	Description
7:0	RW	0x00	intra_bot_mb Intra area bottom mb row (inside area) [0..255]

VEPU_swreg57

Address: Operational Base + offset (0x000e4)

CIR intra control reg

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	CIR_first_intra CIR first intra mb. 0=disabled [0..65535]
15:0	RW	0x0000	CIR_intra_mbinterval CIR intra mb interval. 0=disabled [0..65535]

VEPU_swreg58_vp8

Address: Operational Base + offset (0x000e8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	vp8_1st_dct_pa_addr Base address for VP8 1st DCT partition

VEPU_swreg58

Address: Operational Base + offset (0x000e8)

Intra slice bitmap for slices 0..31

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	intra_slice_bitmap Intra slice bitmap for slices 0..31. LSB=slice0. MSB=slice31. 1=intra.

VEPU_swreg59_vp8

Address: Operational Base + offset (0x000ec)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	vp8_2st_dct_pa_addr Base address for VP8 2st DCT partition

VEPU_swreg59

Address: Operational Base + offset (0x000ec)

Intra slice bitmap for slices32..63

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	intra_slice_bitmap Intra slice bitmap for slices32..63. LSB=slice32. MSB=slice63. 1=intra.

VEPU_swreg60

Address: Operational Base + offset (0x000f0)

1st ROI area register

Bit	Attr	Reset Value	Description
31:24	RW	0x00	ROI_1st_leftmb 1st ROI area left mb column (inside area) qp+=Roi1DeltaQp
23:16	RW	0x00	ROI_1st_rightmb 1st ROI area right mb column (outside area) qp-=Roi1DeltaQp
15:8	RW	0x00	ROI_1st_topmb 1st ROI area top mb row (inside area)
7:0	RW	0x00	ROI_1st_botmb 1st ROI area bottom mb row (outside area)

VEPU_swreg61

Address: Operational Base + offset (0x000f4)

Register0061 Abstract

Bit	Attr	Reset Value	Description
31:24	RW	0x00	ROI_2st_leftmb 2st ROI area left mb column (inside area) qp+=Roi1DeltaQp
23:16	RW	0x00	ROI_2st_rightmb 2st ROI area top mb row (inside area)
15:8	RW	0x00	ROI_2st_topmb 2st ROI area right mb column (outside area) qp-=Roi1DeltaQp
7:0	RW	0x00	ROI_2st_botmb 2st ROI area bottom mb row (outside area)

VEPU_swreg62

Address: Operational Base + offset (0x000f8)

MVC control reg

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:28	RW	0x0	mv16x16_favor Zero 16x16 MV favor div2.
27:19	RW	0x000	penalty_4x4mv Penalty for using 4x4 MV.
18:16	RW	0x0	mvc_priority_id MVC priority_id [0..7]
15:13	RW	0x0	mvc_view_id MVC view_id [0..7]
12:10	RW	0x0	mvc_temporal_id MVC temporal_id [0..7]
9	RW	0x0	mvc_anchor_pic_flag MVC anchor_pic_flag. Specifies that the picture is part of an anchor access unit.
8	RW	0x0	mvc_inter_view_flag MVC inter_view_flag. Specifies that the picture is used for inter-view prediction.
7:4	RW	0x0	delta_qp_1st Field0000 Abstract 1st ROI area delta QP. qp = Qp - Roi1DeltaQp [0..15]
3:0	RW	0x0	delta_qp_2st Field0000 Abstract 2nd ROI area delta QP. qp = Qp - Roi2DeltaQp [0..15]

VEPU_swreg63

Address: Operational Base + offset (0x000fc)

Register0063 Abstract

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30	RW	0x0	flag_tile_4x4 Field0000 Abstract Tiled 4x4 input mode supported by HW. 0=not supported. 1=supported
29	RW	0x0	search_area_h Field0000 Abstract HW search area height. 0=5 MB rows. 1=3 MB rows

Bit	Attr	Reset Value	Description
28	RW	0x0	flag_rgb2yuv_cov Field0000 Abstract RGB to YUV conversion supported by HW. 0=not supported. 1=supported
27	RW	0x0	flag_h264_enc Field0000 Abstract H.264 encoding supported by HW. 0=not supported. 1=supported
26	RW	0x0	flag_vp8_enc Field0000 Abstract VP8 encoding supported by HW. 0=not supported. 1=supported
25	RW	0x0	flag_jpeg_enc Field0000 Abstract JPEG encoding supported by HW. 0=not supported. 1=supported
24:16	RO	0x0	reserved
15:12	RW	0x0	bus_width Field0000 Abstract Bus width of HW. 0=32b. 1=64b. 2=128b
11:0	RO	0x780	MAX_VID_WIDTH Field0000 Description

VEPU_swreg64

Address: Operational Base + offset (0x00100)

JPEG luma quantization 1

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	jpeg_lum_qua1 JPEG luma quantization 1

VEPU_swreg64_vp8

Address: Operational Base + offset (0x00100)

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23:12	RW	0x000	vp8_intra16_mode1 VP8 intra 16x16 mode 1 penalty
11:0	RW	0x000	vp8_intra16_mode0 VP8 intra 16x16 mode 0 penalty

VEPU_swreg65_vp8

Address: Operational Base + offset (0x00104)

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23:12	RW	0x000	vp8_intra16_mode3 VP8 intra 16x16 mode 3 penalty
11:0	RW	0x000	vp8_intra16_mode2 VP8 intra 16x16 mode 2 penalty

VEPU_swreg65

Address: Operational Base + offset (0x00104)

JPEG luma quantization 2

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	jpeg_lum_qua2 JPEG luma quantization 2

VEPU_swreg66_vp8

Address: Operational Base + offset (0x00108)

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23:12	RW	0x000	vp8_intra4_mode1 VP8 intra 4x4 mode 1 penalty
11:0	RW	0x000	vp8_intra4_mode0 VP8 intra 4x4 mode 0 penalty

VEPU_swreg66

Address: Operational Base + offset (0x00108)

JPEG luma quantization 3

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	jpeg_lum_qua3 JPEG luma quantization 3

VEPU_swreg67_vp8

Address: Operational Base + offset (0x0010c)

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23:12	RW	0x000	vp8_intra4_mode3 VP8 intra 4x4 mode 3 penalty
11:0	RW	0x000	vp8_intra4_mode2 VP8 intra 4x4 mode 2 penalty

VEPU_swreg67

Address: Operational Base + offset (0x0010c)

JPEG luma quantization 4

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	jpeg_lum_qua4 JPEG luma quantization 4

VEPU_swreg68_vp8

Address: Operational Base + offset (0x00110)

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23:12	RW	0x000	vp8_intra4_mode5 VP8 intra 4x4 mode 5 penalty
11:0	RW	0x000	vp8_intra4_mode4 VP8 intra 4x4 mode 4 penalty

VEPU_swreg68

Address: Operational Base + offset (0x00110)

JPEG luma quantization 5

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	jpeg_lum_qua5 JPEG luma quantization 5

VEPU_swreg69_vp8

Address: Operational Base + offset (0x00114)

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23:12	RW	0x000	vp8_intra4_mode7 VP8 intra 4x4 mode 7 penalty
11:0	RW	0x000	vp8_intra4_mode6 VP8 intra 4x4 mode 6 penalty

VEPU_swreg69

Address: Operational Base + offset (0x00114)

JPEG luma quantization 6

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	jpeg_lum_qua6 JPEG luma quantization 6 JPEG luma quantization 6

VEPU_swreg70_vp8

Address: Operational Base + offset (0x00118)

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23:12	RW	0x000	vp8_intra4_mode9 VP8 intra 4x4 mode 9 penalty
11:0	RW	0x000	vp8_intra4_mode8 VP8 intra 4x4 mode 8 penalty

VEPU_swreg70

Address: Operational Base + offset (0x00118)

JPEG luma quantization 7

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	jpeg_lum_qua7 JPEG luma quantization 7

VEPU_swreg71_vp8

Address: Operational Base + offset (0x0011c)

JPEG luma quantization 7

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	vp8_seg_addr Base address for VP8 segmentation map, segmentId 2-bits/macroblock

VEPU_swreg71

Address: Operational Base + offset (0x0011c)

JPEG luma quantization 8

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	jpeg_lum_qua8 JPEG luma quantization 8

VEPU_swreg72

Address: Operational Base + offset (0x00120)

JPEG luma quantization 9

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	jpeg_lum_qua9 JPEG luma quantization 9

VEPU_swreg72_vp8

Address: Operational Base + offset (0x00120)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:23	RW	0x00	vp8_seg1_y1_round_dc VP8 segment1 qpY1RoundDc

Bit	Attr	Reset Value	Description
22:14	RW	0x000	vp8_seg1_y1_zbin_dc VP8 segment1 qpY1ZbinDc
13:0	RW	0x0000	vp8_seg1_y1_quant_dc checkpoint distance VP8 segment1 qpY1QuantDc

VEPU_swreg73

Address: Operational Base + offset (0x00124)

Register0073 Abstract

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	jpeg_lum_qua10 JPEG luma quantization 10 JPEG luma quantization 10

VEPU_swreg73_vp8

Address: Operational Base + offset (0x00124)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:23	RW	0x00	vp8_seg1_y1_round_ac VP8 segment1 qpY1RoundAc
22:14	RW	0x000	vp8_seg1_y1_zbin_ac VP8 segment1 qpY1ZbinAc
13:0	RW	0x0000	vp8_seg1_y1_quant_ac checkpoint distance VP8 segment1 qpY1QuantAc

VEPU_swreg74_vp8

Address: Operational Base + offset (0x00128)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:23	RW	0x00	vp8_seg1_y2_round_dc VP8 segment1 qpY2RoundDc
22:14	RW	0x000	vp8_seg1_y2_zbin_dc VP8 segment1 qpY2ZbinDc
13:0	RW	0x0000	vp8_seg1_y2_quant_dc checkpoint distance VP8 segment1 qpY2QuantDc

VEPU_swreg74

Address: Operational Base + offset (0x00128)

JPEG luma quantization 11

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	jpeg_lum_qua11 JPEG luma quantization 11

VEPU_swreg75

Address: Operational Base + offset (0x0012c)

JPEG luma quantization 12

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	jpeg_lum_qua12 JPEG luma quantization 12

VEPU_swreg75_vp8

Address: Operational Base + offset (0x0012c)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:23	RW	0x00	vp8_seg1_y1_round_ac VP8 segment1 qpY2RoundAc
22:14	RW	0x000	vp8_seg1_y2_zbin_ac VP8 segment1 qpY2ZbinAc
13:0	RW	0x0000	vp8_seg1_y2_quant_ac checkpoint distance VP8 segment1 qpY2QuantAc

VEPU_swreg76_vp8

Address: Operational Base + offset (0x00130)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:23	RW	0x00	vp8_seg1_ch_round_dc VP8 segment1 qpchRoundDc
22:14	RW	0x000	vp8_seg1_ch_zbin_dc VP8 segment1 qpchZbinDc
13:0	RW	0x0000	vp8_seg1_ch_quant_dc checkpoint distance VP8 segment1 qpchQuantDc

VEPU_swreg76

Address: Operational Base + offset (0x00130)

JPEG luma quantization 13

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	jpeg_lum_qua13 JPEG luma quantization 13

VEPU_swreg77_vp8

Address: Operational Base + offset (0x00134)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:23	RW	0x00	vp8_seg1_ch_round_ac VP8 segment1 qpchRoundAc
22:14	RW	0x000	vp8_seg1_ch_zbin_ac VP8 segment1 qpchZbinAc
13:0	RW	0x0000	vp8_seg1_ch_quant_ac checkpoint distance VP8 segment1 qpchQuantAc

VEPU_swreg77

Address: Operational Base + offset (0x00134)

JPEG luma quantization 14

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	jpeg_lum_qua14 JPEG luma quantization 14

VEPU_swreg78_vp8

Address: Operational Base + offset (0x00138)

Bit	Attr	Reset Value	Description
31:26	RO	0x0	reserved
25:17	RW	0x000	vp8_seg1_y2_dequant_dc VP8 segment1 qpY2DequantDc
16:8	RW	0x000	vp8_seg1_y1_dequant_ac VP8 segment1 qpY1DequantAc
7:0	RW	0x00	vp8_seg1_y1_dequant_dc checkpoint distance VP8 segment1 qpY1DequantDc

VEPU_swreg78

Address: Operational Base + offset (0x00138)

JPEG luma quantization 15

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	jpeg_lum_qua15 JPEG luma quantization 15

VEPU_swreg79

Address: Operational Base + offset (0x0013c)

JPEG luma quantization 16

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	jpeg_lum_qua16 JPEG luma quantization 16

VEPU_swreg79_vp8

Address: Operational Base + offset (0x0013c)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	vp8_seg1_fil_lev Field0000 Abstract VP8 segment1 filter level
25:17	RW	0x000	vp8_seg1_ch_dequant_ac VP8 segment1 qpChDequantAc
16:9	RW	0x00	vp8_seg1_ch_dequant_dc VP8 segment1 qpChDequantDc
8:0	RW	0x000	vp8_seg1_y2_dequant_ac checkpoint distance VP8 segment1 qpY2DequantAc

VEPU_swreg80_vp8

Address: Operational Base + offset (0x00140)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:23	RW	0x00	vp8_seg2_y1_round_dc VP8 segment2 qpY1RoundDc
22:14	RW	0x000	vp8_seg2_y1_zbin_dc VP8 segment2 qpY1ZbinDc
13:0	RW	0x0000	vp8_seg2_y1_quant_dc checkpoint distance VP8 segment2 qpY1QuantDc

VEPU_swreg80

Address: Operational Base + offset (0x00140)

JPEG chroma quantization 1

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	jpeg_chrom_qua1 JPEG chroma quantization 1

VEPU_swreg81

Address: Operational Base + offset (0x00144)

JPEG chroma quantization 2

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	jpeg_chrom_qua2 JPEG chroma quantization 2

VEPU_swreg81_vp8

Address: Operational Base + offset (0x00144)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:23	RW	0x00	vp8_seg2_y1_round_ac VP8 segment2 qpY1RoundAc
22:14	RW	0x000	vp8_seg2_y1_zbin_ac VP8 segment2 qpY1ZbinAc
13:0	RW	0x0000	vp8_seg2_y1_quant_ac checkpoint distance VP8 segment2 qpY1QuantAc

VEPU_swreg82_vp8

Address: Operational Base + offset (0x00148)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:23	RW	0x00	vp8_seg2_y2_round_dc VP8 segment2 qpY2RoundDc
22:14	RW	0x000	vp8_seg2_y2_zbin_dc VP8 segment2 qpY2ZbinDc
13:0	RW	0x0000	vp8_seg2_y2_quant_dc checkpoint distance VP8 segment2 qpY2QuantDc

VEPU_swreg82

Address: Operational Base + offset (0x00148)

JPEG chroma quantization 3

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	jpeg_chrom_qua3 JPEG chroma quantization 3

VEPU_swreg83

Address: Operational Base + offset (0x0014c)

JPEG chroma quantization 4

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	jpeg_chrom_qua4 JPEG chroma quantization 4

VEPU_swreg83_vp8

Address: Operational Base + offset (0x0014c)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:23	RW	0x00	vp8_seg2_y1_round_ac VP8 segment2 qpY1RoundAc

Bit	Attr	Reset Value	Description
22:14	RW	0x000	vp8_seg2_y2_zbin_ac VP8 segment2 qpY2ZbinAc
13:0	RW	0x0000	vp8_seg2_y2_quant_ac checkpoint distance VP8 segment2 qpY2QuantAc

VEPU_swreg84_vp8

Address: Operational Base + offset (0x00150)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:23	RW	0x00	vp8_seg2_ch_round_dc VP8 segment2 qpchRoundDc
22:14	RW	0x000	vp8_seg2_ch_zbin_dc VP8 segment2 qpchZbinDc
13:0	RW	0x0000	vp8_seg2_ch_quant_dc checkpoint distance VP8 segment2 qpchQuantDc

VEPU_swreg84

Address: Operational Base + offset (0x00150)

JPEG chroma quantization 5

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	jpeg_chrom_qua5 JPEG chroma quantization 5

VEPU_swreg85

Address: Operational Base + offset (0x00154)

JPEG chroma quantization 6

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	jpeg_chrom_qua6 JPEG chroma quantization 6

VEPU_swreg85_vp8

Address: Operational Base + offset (0x00154)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:23	RW	0x00	vp8_seg2_ch_round_ac VP8 segment2 qpchRoundAc
22:14	RW	0x000	vp8_seg2_ch_zbin_ac VP8 segment2 qpchZbinAc

Bit	Attr	Reset Value	Description
13:0	RW	0x0000	vp8_seg2_ch_quant_ac checkpoint distance VP8 segment2 qpchQuantAc

VEPU_swreg86_vp8

Address: Operational Base + offset (0x00158)

Bit	Attr	Reset Value	Description
31:26	RO	0x0	reserved
25:17	RW	0x000	vp8_seg2_y2_dequant_dc VP8 segment2 qpY2DequantDc
16:8	RW	0x000	vp8_seg2_y1_dequant_ac VP8 segment2 qpY1DequantAc
7:0	RW	0x00	vp8_seg2_y1_dequant_dc checkpoint distance VP8 segment2 qpY2DequantDc

VEPU_swreg86

Address: Operational Base + offset (0x00158)

JPEG chroma quantization 7

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	jpeg_chrom_qua7 JPEG chroma quantization 7

VEPU_swreg87

Address: Operational Base + offset (0x0015c)

JPEG chroma quantization 8

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	jpeg_chrom_qua8 JPEG chroma quantization 8

VEPU_swreg87_vp8

Address: Operational Base + offset (0x0015c)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	vp8_seg2_fil_lev Field0000 Abstract VP8 segment2 filter level
25:17	RW	0x000	vp8_seg2_ch_dequant_ac VP8 segment2 qpChDequantAc
16:9	RW	0x00	vp8_seg2_ch_dequant_dc VP8 segment2 qpChDequantDc

Bit	Attr	Reset Value	Description
8:0	RW	0x000	vp8_seg2_y2_dequant_ac checkpoint distance VP8 segment2qpY2DequantAc

VEPU_swreg88_vp8

Address: Operational Base + offset (0x00160)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:23	RW	0x00	vp8_seg3_y1_round_dc VP8 segment3 qpY1RoundDc
22:14	RW	0x000	vp8_seg3_y1_zbin_dc VP8 segment3 qpY1ZbinDc
13:0	RW	0x0000	vp8_seg3_y1_quant_dc checkpoint distance VP8 segment3 qpY1QuantDc

VEPU_swreg88

Address: Operational Base + offset (0x00160)

JPEG chroma quantization 9

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	jpeg_chrom_qua9 JPEG chroma quantization 9

VEPU_swreg89_vp8

Address: Operational Base + offset (0x00164)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:23	RW	0x00	vp8_seg3_y1_round_ac VP8 segment3 qpY1RoundAc
22:14	RW	0x000	vp8_seg3_y1_zbin_ac VP8 segment3 qpY1ZbinAc
13:0	RW	0x0000	vp8_seg3_y1_quant_ac checkpoint distance VP8 segment3 qpY1QuantAc

VEPU_swreg89

Address: Operational Base + offset (0x00164)

JPEG chroma quantization 10

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	jpeg_chrom_qua10 JPEG chroma quantization 10

VEPU_swreg90_vp8

Address: Operational Base + offset (0x00168)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:23	RW	0x00	vp8_seg3_y2_round_dc VP8 segment3 qpY2RoundDc
22:14	RW	0x000	vp8_seg3_y2_zbin_dc VP8 segment3 qpY2ZbinDc
13:0	RW	0x0000	vp8_seg3_y2_quant_dc checkpoint distance VP8 segment3 qpY2QuantDc

VEPU_swreg90

Address: Operational Base + offset (0x00168)

JPEG chroma quantization 11

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	jpeg_chrom_qua11 JPEG chroma quantization 11

VEPU_swreg91_vp8

Address: Operational Base + offset (0x0016c)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:23	RW	0x00	vp8_seg3_y1_round_ac VP8 segment3 qpY2RoundAc
22:14	RW	0x000	vp8_seg3_y2_zbin_ac VP8 segment3 qpY2ZbinAc
13:0	RW	0x0000	vp8_seg3_y2_quant_ac checkpoint distance VP8 segment3 qpY2QuantAc

VEPU_swreg91

Address: Operational Base + offset (0x0016c)

JPEG chroma quantization 12

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	jpeg_chrom_qua12 JPEG chroma quantization 12

VEPU_swreg92_vp8

Address: Operational Base + offset (0x00170)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved

Bit	Attr	Reset Value	Description
30:23	RW	0x00	vp8_seg3_ch_round_dc VP8 segment3 qpchRoundDc
22:14	RW	0x000	vp8_seg3_ch_zbin_dc VP8 segment3 qpchZbinDc
13:0	RW	0x0000	vp8_seg3_ch_quant_dc checkpoint distance VP8 segment3 qpchQuantDc

VEPU_swreg92

Address: Operational Base + offset (0x00170)

JPEG chroma quantization 13

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	jpeg_chrom_qua13 JPEG chroma quantization 13

VEPU_swreg93_vp8

Address: Operational Base + offset (0x00174)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:23	RW	0x00	vp8_seg3_ch_round_ac VP8 segment3 qpchRoundAc
22:14	RW	0x000	vp8_seg3_ch_zbin_ac VP8 segment3 qpchZbinAc
13:0	RW	0x0000	vp8_seg3_ch_quant_ac checkpoint distance VP8 segment3 qpchQuantAc

VEPU_swreg93

Address: Operational Base + offset (0x00174)

JPEG chroma quantization 14

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	jpeg_chrom_qua14 JPEG chroma quantization 14

VEPU_swreg94_vp8

Address: Operational Base + offset (0x00178)

Bit	Attr	Reset Value	Description
31:26	RO	0x0	reserved
25:17	RW	0x000	vp8_seg3_y2_dequant_dc VP8 segment3 qpY2DequantDc
16:8	RW	0x000	vp8_seg3_y1_dequant_ac VP8 segment3 qpY1DequantAc

Bit	Attr	Reset Value	Description
7:0	RW	0x00	vp8_seg3_y1_dequant_dc checkpoint distance VP8 segment3 qpY2DequantDc

VEPU_swreg94

Address: Operational Base + offset (0x00178)

JPEG chroma quantization 15

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	jpeg_chrom_qua15 JPEG chroma quantization 15

VEPU_swreg95_vp8

Address: Operational Base + offset (0x0017c)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	vp8_seg3_fil_lev Field0000 Abstract VP8 segment3 filter level
25:17	RW	0x000	vp8_seg3_ch_dequant_ac VP8 segment3 qpChDequantAc
16:9	RW	0x00	vp8_seg3_ch_dequant_dc VP8 segment3 qpChDequantDc
8:0	RW	0x000	vp8_seg3_y2_dequant_ac checkpoint distance VP8 segment3qpY2DequantAc

VEPU_swreg95

Address: Operational Base + offset (0x0017c)

JPEG chroma quantization 16

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	jpeg_chrom_qua16 JPEG chroma quantization 16

VEPU_swreg96

Address: Operational Base + offset (0x00180)

DMV 4p/1p penalty values 0-3

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	DMV_4p_1p_penalty DMV 4p/1p penalty values 0-3

VEPU_swreg97

Address: Operational Base + offset (0x00184)

DMV 4p/1p penalty values 4-7

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	DMV_4p_1p_penalty DMV 4p/1p penalty values 4-7

VEPU_swreg98

Address: Operational Base + offset (0x00188)

DMV 4p/1p penalty values

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	DMV_4p_1p_penalty DMV 4p/1p penalty values

VEPU_swreg99

Address: Operational Base + offset (0x0018c)

DMV 4p/1p penalty values

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	DMV_4p_1p_penalty DMV 4p/1p penalty values

VEPU_swreg100

Address: Operational Base + offset (0x00190)

DMV 4p/1p penalty values

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	DMV_4p_1p_penalty DMV 4p/1p penalty values

VEPU_swreg101

Address: Operational Base + offset (0x00194)

DMV 4p/1p penalty values

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	DMV_4p_1p_penalty DMV 4p/1p penalty values

VEPU_swreg102

Address: Operational Base + offset (0x00198)

DMV 4p/1p penalty values

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	DMV_4p_1p_penalty DMV 4p/1p penalty values

VEPU_swreg103

Address: Operational Base + offset (0x0019c)

DMV 4p/1p penalty values

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	DMV_4p_1p_penalty DMV 4p/1p penalty values

VEPU_swreg104

Address: Operational Base + offset (0x001a0)

DMV 4p/1p penalty values

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	DMV_4p_1p_penalty DMV 4p/1p penalty values

VEPU_swreg105

Address: Operational Base + offset (0x001a4)

DMV 4p/1p penalty values

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	DMV_4p_1p_penalty DMV 4p/1p penalty values

VEPU_swreg106

Address: Operational Base + offset (0x001a8)

DMV 4p/1p penalty values

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	DMV_4p_1p_penalty DMV 4p/1p penalty values

VEPU_swreg107

Address: Operational Base + offset (0x001ac)

DMV 4p/1p penalty values

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	DMV_4p_1p_penalty DMV 4p/1p penalty values

VEPU_swreg108

Address: Operational Base + offset (0x001b0)

DMV 4p/1p penalty values

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	DMV_4p_1p_penalty DMV 4p/1p penalty values

VEPU_swreg109

Address: Operational Base + offset (0x001b4)

DMV 4p/1p penalty values

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	DMV_4p_1p_penalty DMV 4p/1p penalty values

VEPU_swreg110

Address: Operational Base + offset (0x001b8)

DMV 4p/1p penalty values

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	DMV_4p_1p_penalty DMV 4p/1p penalty values

VEPU_swreg111

Address: Operational Base + offset (0x001bc)

DMV 4p/1p penalty values

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	DMV_4p_1p_penalty DMV 4p/1p penalty values

VEPU_swreg112

Address: Operational Base + offset (0x001c0)

DMV 4p/1p penalty values

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	DMV_4p_1p_penalty DMV 4p/1p penalty values

VEPU_swreg113

Address: Operational Base + offset (0x001c4)

DMV 4p/1p penalty values

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	DMV_4p_1p_penalty DMV 4p/1p penalty values

VEPU_swreg114

Address: Operational Base + offset (0x001c8)

DMV 4p/1p penalty values

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	DMV_4p_1p_penalty DMV 4p/1p penalty values

VEPU_swreg115

Address: Operational Base + offset (0x001cc)

DMV 4p/1p penalty values

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	DMV_4p_1p_penalty DMV 4p/1p penalty values

VEPU_swreg116

Address: Operational Base + offset (0x001d0)

DMV 4p/1p penalty values

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	DMV_4p_1p_penalty DMV 4p/1p penalty values

VEPU_swreg117

Address: Operational Base + offset (0x001d4)

DMV 4p/1p penalty values

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	DMV_4p_1p_penalty DMV 4p/1p penalty values

VEPU_swreg118

Address: Operational Base + offset (0x001d8)

DMV 4p/1p penalty values

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	DMV_4p_1p_penalty DMV 4p/1p penalty values

VEPU_swreg119

Address: Operational Base + offset (0x001dc)

DMV 4p/1p penalty values

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	DMV_4p_1p_penalty DMV 4p/1p penalty values

VEPU_swreg120

Address: Operational Base + offset (0x001e0)

DMV 4p/1p penalty values

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	DMV_4p_1p_penalty DMV 4p/1p penalty values

VEPU_swreg121

Address: Operational Base + offset (0x001e4)

DMV 4p/1p penalty values

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	DMV_4p_1p_penalty DMV 4p/1p penalty values

VEPU_swreg122

Address: Operational Base + offset (0x001e8)

DMV 4p/1p penalty values

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	DMV_4p_1p_penalty DMV 4p/1p penalty values

VEPU_swreg123

Address: Operational Base + offset (0x001ec)

DMV 4p/1p penalty values

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	DMV_4p_1p_penalty DMV 4p/1p penalty values

VEPU_swreg124

Address: Operational Base + offset (0x001f0)

DMV 4p/1p penalty values

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	DMV_4p_1p_penalty DMV 4p/1p penalty values

VEPU_swreg125

Address: Operational Base + offset (0x001f4)

DMV 4p/1p penalty values

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	DMV_4p_1p_penalty DMV 4p/1p penalty values

VEPU_swreg126

Address: Operational Base + offset (0x001f8)

DMV 4p/1p penalty values

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	DMV_4p_1p_penalty DMV 4p/1p penalty values

VEPU_swreg127

Address: Operational Base + offset (0x001fc)

DMV 4p/1p penalty values

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	DMV_4p_1p_penalty DMV 4p/1p penalty values

VEPU_swreg128

Address: Operational Base + offset (0x00200)

DMV 4p/1p penalty values

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	DMV_4p_1p_penalty DMV 4p/1p penalty values

VEPU_swreg129

Address: Operational Base + offset (0x00204)

DMV 4p/1p penalty values

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	DMV_4p_1p_penalty DMV 4p/1p penalty values

VEPU_swreg130

Address: Operational Base + offset (0x00208)

DMV 4p/1p penalty values

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	DMV_4p_1p_penalty DMV 4p/1p penalty values

VEPU_swreg131

Address: Operational Base + offset (0x0020c)

DMV 4p/1p penalty values

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	DMV_4p_1p_penalty DMV 4p/1p penalty values

VEPU_swreg132

Address: Operational Base + offset (0x00210)

DMV 4p/1p penalty values

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	DMV_4p_1p_penalty DMV 4p/1p penalty values

VEPU_swreg133

Address: Operational Base + offset (0x00214)

DMV 4p/1p penalty values

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	DMV_4p_1p_penalty DMV 4p/1p penalty values

VEPU_swreg134

Address: Operational Base + offset (0x00218)

DMV 4p/1p penalty values

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	DMV_4p_1p_penalty DMV 4p/1p penalty values

VEPU_swreg135

Address: Operational Base + offset (0x0021c)

DMV 4p/1p penalty values

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	DMV_4p_1p_penalty DMV 4p/1p penalty values

VEPU_swreg136

Address: Operational Base + offset (0x00220)

DMV 4p/1p penalty values

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	DMV_4p_1p_penalty DMV 4p/1p penalty values

VEPU_swreg137

Address: Operational Base + offset (0x00224)

DMV 4p/1p penalty values

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	DMV_4p_1p_penalty DMV 4p/1p penalty values

VEPU_swreg138

Address: Operational Base + offset (0x00228)

DMV 4p/1p penalty values

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	DMV_4p_1p_penalty DMV 4p/1p penalty values

VEPU_swreg139

Address: Operational Base + offset (0x0022c)

DMV 4p/1p penalty values

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	DMV_4p_1p_penalty DMV 4p/1p penalty values

VEPU_swreg140

Address: Operational Base + offset (0x00230)

DMV 4p/1p penalty values

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	DMV_4p_1p_penalty DMV 4p/1p penalty values

VEPU_swreg141

Address: Operational Base + offset (0x00234)

DMV 4p/1p penalty values

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	DMV_4p_1p_penalty DMV 4p/1p penalty values

VEPU_swreg142

Address: Operational Base + offset (0x00238)

DMV 4p/1p penalty values

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	DMV_4p_1p_penalty DMV 4p/1p penalty values

VEPU_swreg143

Address: Operational Base + offset (0x0023c)

DMV 4p/1p penalty values

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	DMV_4p_1p_penalty DMV 4p/1p penalty values

VEPU_swreg144

Address: Operational Base + offset (0x00240)

DMV 4p/1p penalty values

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	DMV_4p_1p_penalty DMV 4p/1p penalty values

VEPU_swreg145

Address: Operational Base + offset (0x00244)

DMV 4p/1p penalty values

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	DMV_4p_1p_penalty DMV 4p/1p penalty values

VEPU_swreg146

Address: Operational Base + offset (0x00248)

DMV 4p/1p penalty values

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	DMV_4p_1p_penalty DMV 4p/1p penalty values

VEPU_swreg147

Address: Operational Base + offset (0x0024c)

DMV 4p/1p penalty values

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	DMV_4p_1p_penalty DMV 4p/1p penalty values

VEPU_swreg148

Address: Operational Base + offset (0x00250)

DMV 4p/1p penalty values

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	DMV_4p_1p_penalty DMV 4p/1p penalty values

VEPU_swreg149

Address: Operational Base + offset (0x00254)

DMV 4p/1p penalty values

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	DMV_4p_1p_penalty DMV 4p/1p penalty values

VEPU_swreg150

Address: Operational Base + offset (0x00258)

DMV 4p/1p penalty values

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	DMV_4p_1p_penalty DMV 4p/1p penalty values

VEPU_swreg151

Address: Operational Base + offset (0x0025c)

DMV 4p/1p penalty values

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	DMV_4p_1p_penalty DMV 4p/1p penalty values

VEPU_swreg152

Address: Operational Base + offset (0x00260)

DMV 4p/1p penalty values

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	DMV_4p_1p_penalty DMV 4p/1p penalty values

VEPU_swreg153

Address: Operational Base + offset (0x00264)

DMV 4p/1p penalty values

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	DMV_4p_1p_penalty DMV 4p/1p penalty values

VEPU_swreg154

Address: Operational Base + offset (0x00268)

DMV 4p/1p penalty values

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	DMV_4p_1p_penalty DMV 4p/1p penalty values

VEPU_swreg155

Address: Operational Base + offset (0x0026c)

DMV 4p/1p penalty values

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	DMV_4p_1p_penalty DMV 4p/1p penalty values

VEPU_swreg156

Address: Operational Base + offset (0x00270)

DMV 4p/1p penalty values

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	DMV_4p_1p_penalty DMV 4p/1p penalty values

VEPU_swreg157

Address: Operational Base + offset (0x00274)

DMV 4p/1p penalty values

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	DMV_4p_1p_penalty DMV 4p/1p penalty values

VEPU_swreg158

Address: Operational Base + offset (0x00278)

DMV 4p/1p penalty values

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	DMV_4p_1p_penalty DMV 4p/1p penalty values

VEPU_swreg159

Address: Operational Base + offset (0x0027c)

DMV 4p/1p penalty values

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	DMV_4p_1p_penalty DMV 4p/1p penalty values 124-127

VEPU_swreg160

Address: Operational Base + offset (0x00280)

vp8 control

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved

Bit	Attr	Reset Value	Description
23:12	RW	0x000	vp8_coeff_dmv_penalty VP8 coeff for dmv penalty for intra/inter selection
11:0	RW	0x000	vp8_inter_type VP8 bit cost of inter type

VEPU_swreg161

Address: Operational Base + offset (0x00284)

VP8 bit cost of golden ref frame

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:0	RW	0x000	vp8_ref_frame VP8 bit cost of golden ref frame

VEPU_swreg162

Address: Operational Base + offset (0x00288)

vp8 loop filter delta registers

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:21	RW	0x00	vp8_loopfilter_altref VP8 loop filter delta for alt ref
20:14	RW	0x00	vp8_loopfilter_goldenref VP8 loop filter delta for golden ref
13:7	RW	0x00	vp8_loopfilter_lastref VP8 loop filter delta for last ref
6:0	RW	0x00	vp8_loopfilter_intra VP8 loop filter delta for intra mb

VEPU_swreg163

Address: Operational Base + offset (0x0028c)

vp8 loop filter delta register

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:21	RW	0x00	vp8_loopfilter_splitmv VP8 loop filter delta for SPLITMV
20:14	RW	0x00	vp8_loopfilter_newmv VP8 loop filter delta for NEWMV
13:7	RW	0x00	vp8_loopfilter_zeromv VP8 loop filter delta for ZEROMV
6:0	RW	0x00	vp8_loopfilter_bpred VP8 loop filter delta for BPRED

16.4.9 VDPU Register Summary

Name	Offset	Size	Reset Value	Description
VDPU_SWREG0	0x00000	W	0x00000000	Register0000 Abstract
VDPU_SWREG1	0x00004	W	0x00000000	interrupt register decoder
VDPU_SWREG2	0x00008	W	0x01000400	device configuration register decoder
VDPU_SWREG3	0x0000c	W	0x00000001	Device control register 0(deemode, picture type etc)
VDPU_SWREG4_H264	0x00010	W	0x00000000	decoder control register 1(picture parameters)
VDPU_SWREG4	0x00010	W	0x00000000	decoder control register 1(picture parameters)
VDPU_SWREG5	0x00014	W	0x00000000	decoder control register2 (stream decoding table selects)
VDPU_SWREG5_H264	0x00014	W	0x00000000	decoder control register2 (stream decoding table selects)
VDPU_SWREG5_VP8	0x00014	W	0x00000000	decoder control register2 (stream decoding table selects)
VDPU_SWREG6	0x00018	W	0x00000000	decoder control register 3(stream buffer information)
VDPU_SWREG7	0x0001c	W	0x00000000	decoder control register 4(H264, VC-1 control)
VDPU_SWREG7_VP8	0x0001c	W	0x00000000	decoder control register 4(H264, VC-1 control)
VDPU_SWREG8	0x00020	W	0x00000000	decoder control register 5(H264, VC-1)
VDPU_SWREG8_VP8	0x00020	W	0x00000000	decoder control register 5(H264, VC-1)
VDPU_SWREG9	0x00024	W	0x00000000	decoder control register 6
VDPU_SWREG9_VP8	0x00024	W	0x00000000	decoder control register 6
VDPU_SREG10_H264_RLC	0x00028	W	0x00000000	Base address for differential motion vector base address
VDPU_SREG10_H264	0x00028	W	0x00000000	Base address for differential motion vector base address
VDPU_SREG10_VP8	0x00028	W	0x00000000	Base address for differential motion vector base address
VDPU_SWREG11_H264_RLC	0x0002c	W	0x00000000	decoder control register 7
VDPU_SWREG11_H264	0x0002c	W	0x00000000	decoder control register 7
VDPU_SWREG11_VP8	0x0002c	W	0x00000000	
VDPU_SWREG12	0x00030	W	0x00000000	Base address for RLC data (RLC) / stream start address/decoded
VDPU_SWREG13	0x00034	W	0x00000000	Base address for decoded picture / base address for JPEG deco

Name	Offset	Size	Reset Value	Description
VDPU_SWREG14	0x00038	W	0x00000000	Base address for reference picture index 0 / base address for J
VDPU_SWREG14_VP8	0x00038	W	0x00000000	Base address for reference picture index 0 / base address for J
VDPU_SWREG15_JPEG_ROI	0x0003c	W	0x00000000	JPEG roi control
VDPU_SWREG15	0x0003c	W	0x00000000	Base address for reference picture index 1 / JPEG control
VDPU_SWREG15_VP8	0x0003c	W	0x00000000	Base address for reference picture index 1 / JPEG control
VDPU_SWREG16	0x00040	W	0x00000000	base address for reference picture index 2 / List of VLC code len
VDPU_SWREG17	0x00044	W	0x00000000	Base address for reference picture index 3 / List of VLC code le
VDPU_SWREG18	0x00048	W	0x00000000	Base address for reference picture index 4 / VC1 control / MPE
VDPU_SWREG18_VP8	0x00048	W	0x00000000	Base address for reference picture index 4 / VC1 control / MPE
VDPU_SWREG19	0x0004c	W	0x00000000	Base address for reference picture index 5
VDPU_SWREG19_VP8	0x0004c	W	0x00000000	Base address for reference picture index 5
VDPU_SWREG20	0x00050	W	0x00000000	Base address for reference picture index 6
VDPU_SWREG21	0x00054	W	0x00000000	Base address for reference picture index 7
VDPU_SWREG22	0x00058	W	0x00000000	Base address for reference picture index 8
VDPU_SWREG22_VP8	0x00058	W	0x00000000	Base address for reference picture index 8
VDPU_SWREG23	0x0005c	W	0x00000000	Base address for reference picture index 9
VDPU_SWREG23_VP8	0x0005c	W	0x00000000	Base address for reference picture index 9
VDPU_SWREG24	0x00060	W	0x00000000	Base address for reference picture index 10
VDPU_SWREG24_VP8	0x00060	W	0x00000000	Base address for reference picture index 10
VDPU_SWREG25_VP8	0x00064	W	0x00000000	Base address for reference picture index 10
VDPU_SWREG25	0x00064	W	0x00000000	Base address for reference picture index 11
VDPU_SWREG26_VP8	0x00068	W	0x00000000	Base address for reference picture index 10
VDPU_SWREG26	0x00068	W	0x00000000	Base address for reference picture index 12
VDPU_SWREG27_VP8	0x0006c	W	0x00000000	Base address for reference picture index 13
VDPU_SWREG27	0x0006c	W	0x00000000	Base address for reference picture index 13
VDPU_SWREG28_VP8	0x00070	W	0x00000000	Base address for reference picture index 10
VDPU_SWREG28	0x00070	W	0x00000000	Base address for reference picture index14

Name	Offset	Size	Reset Value	Description
VDPU_SWREG29_VP8	0x00074	W	0x00000000	Base address for reference picture index 10
VDPU_SWREG29	0x00074	W	0x00000000	Base address for reference picture index15
VDPU_SWREG30	0x00078	W	0x00000000	Reference picture numbers for index 0 and 1 (H264 VLC)
VDPU_SWREG30_VP8	0x00078	W	0x00000000	Reference picture numbers for index 0 and 1 (H264 VLC)
VDPU_SWREG31	0x0007c	W	0x00000000	Reference picture numbers for index 2 and 3 (H264 VLC) /
VDPU_SWREG31_VP8	0x0007c	W	0x00000000	Reference picture numbers for index 2 and 3 (H264 VLC) /
VDPU_SWREG32	0x00080	W	0x00000000	Reference picture numbers for index 4 and 5 (H264 VLC)
VDPU_SWREG32_VP8	0x00080	W	0x00000000	Reference picture numbers for index 4 and 5 (H264 VLC)
VDPU_SWREG33	0x00084	W	0x00000000	Reference picture numbers for index 6 and 7 (H264 VLC)
VDPU_SWREG33_VP8	0x00084	W	0x00000000	Reference picture numbers for index 6 and 7 (H264 VLC)
VDPU_SWREG34	0x00088	W	0x00000000	Reference picture numbers for index 8 and 9 (H264 VLC)
VDPU_SWREG34_VP8	0x00088	W	0x00000000	Reference picture numbers for index 8 and 9 (H264 VLC)
VDPU_SWREG35_JPEG_ROI	0x0008c	W	0x00000000	JPEG roi offset/dc base address
VDPU_SWREG35	0x0008c	W	0x00000000	Reference picture numbers for index 10 and 11 (H264 VLC)
VDPU_SWREG35_VP8	0x0008c	W	0x00000000	Reference picture numbers for index 10 and 11 (H264 VLC)
VDPU_SWREG36	0x00090	W	0x00000000	Reference picture numbers for index 12 and 13 (H264 VLC)
VDPU_SWREG36_JPEG_ROI	0x00090	W	0x00000000	JPEG roi offset/dc length
VDPU_SWREG36_VP8	0x00090	W	0x00000000	Reference picture numbers for index 12 and 13 (H264 VLC)
VDPU_SWREG37_VP8	0x00094	W	0x00000000	Reference picture numbers for index 12 and 13 (H264 VLC)
VDPU_SWREG37	0x00094	W	0x00000000	Reference picture numbers for index 14 and 15 (H264 VLC)
VDPU_SWREG38	0x00098	W	0x00000000	Reference picture long term flags (H264 VLC) / VPx prediction filt
VDPU_SWREG38_H264	0x00098	W	0x00000000	Reference picture numbers for index 12 and 13 (H264 VLC)

Name	Offset	Size	Reset Value	Description
VDPU_SWREG39	0x0009c	W	0x00000000	Reference picture valid flags (H264 VLC) /VPx prediction filter ta
VDPU_SWREG39_H264	0x0009c	W	0x00000000	Reference picture numbers for index 12 and 13 (H264 VLC)
VDPU_SWREG40	0x000a0	W	0x00000000	Base address for standard dependent tables
VDPU_SWREG41	0x000a4	W	0x00000000	Base address for direct mode motion vectors
VDPU_SWREG42_VP8	0x000a8	W	0x00000000	
VDPU_SWREG42	0x000a8	W	0x00000000	bi_dir initial ref pic list register (0-2)
VDPU_SWREG43_VP8	0x000ac	W	0x00000000	
VDPU_SWREG43	0x000ac	W	0x00000000	bi-dir initial ref pic list register (3-5)
VDPU_SWREG44_VP8	0x000b0	W	0x00000000	
VDPU_SWREG44	0x000b0	W	0x00000000	bi-dir initial ref pic list register (6-8)
VDPU_SWREG45_VP8	0x000b4	W	0x00000000	
VDPU_SWREG45	0x000b4	W	0x00000000	bi-dir initial ref pic list register (9- 11)
VDPU_SWREG46	0x000b8	W	0x00000000	bi-dir initial ref pic list register (12- 14) / VP7,VP8 quantization v
VDPU_SWREG46_VP8	0x000b8	W	0x00000000	bi-dir initial ref pic list register (12- 14) / VP7,VP8 quantization v
VDPU_SWREG47	0x000bc	W	0x00000000	bi-dir and P fwd initial ref pic list register (15 and P 0-3) / VP7,V
VDPU_SWREG47_VP8	0x000bc	W	0x00000000	bi-dir and P fwd initial ref pic list register (15 and P 0-3) / VP7,V
VDPU_SWREG48	0x000c0	W	0x00000000	Error concealment register
VDPU_SWREG49	0x000c4	W	0x00000000	Prediction filter tap register for H264, MPEG4, VC1
VDPU_SWREG50	0x000c8	W	0xfb56f80	Synthesis configuration register decoder 0 (read only)
VDPU_SWREG51	0x000cc	W	0x00000000	Reference picture buffer control register
VDPU_SWREG52	0x000d0	W	0x00000000	Reference picture buffer information register 1 (read only)
VDPU_SWREG53	0x000d4	W	0x00000000	Reference picture buffer information register 2 (read only)
VDPU_SWREG54	0x000d8	W	0xe5da0000	Synthesis configuration register decoder 1 (read only)
VDPU_SWREG55	0x000dc	W	0x00000000	Reference picture buffer 2 / Advanced prefetch control register
VDPU_SWREG56	0x000e0	W	0x00000000	Reference buffer information register 3 (read only)
VDPU_SWREG57_INTRA_INTER	0x000e4	W	0x00000000	intra_dli3t,intra_dblspeed,inter_dblspeed,stream_len_hi

Name	Offset	Size	Reset Value	Description
VDPU_SWREG57	0x000e4	W	0x00000000	intra_dli3t,intra_dblspeed,inter_dblspeed,stream_len_hi
VDPU_SWREG58	0x000e8	W	0x00000000	Decoder debug register 0 (read only)
VDPU_SWREG59	0x000ec	W	0x00000000	H264 Chrominance 8 pixel interleaved data base
VDPU_SWREG60	0x000f0	W	0x00000000	Interrupt register post-processor
VDPU_SWREG61	0x000f4	W	0x01010100	Device configuration register post-processor
VDPU_SWREG62	0x000f8	W	0x00000000	Deinterlace control register
VDPU_SWREG63	0x000fc	W	0x00000000	base address for reading post-processing input picture uminan
VDPU_SWREG64	0x00100	W	0x00000000	Base address for reading post-processing input picture Cb/Ch
VDPU_SWREG65	0x00104	W	0x00000000	Base address for reading post-processing input picture Cr
VDPU_SWREG66	0x00108	W	0x00000000	Base address for writing post-processed picture luminance/RGB
VDPU_SWREG67	0x0010c	W	0x00000000	Base address for writing post-processed picture Ch
VDPU_SWREG68	0x00110	W	0x00000000	Register for contrast adjusting
VDPU_SWREG69	0x00114	W	0x00000000	Register for colour conversion and contrast adjusting
VDPU_SWREG70	0x00118	W	0x00000000	Register for colour conversion 0
VDPU_SWREG71	0x0011c	W	0x00000000	Register for colour conversion 1 + rotation mode
VDPU_SWREG72	0x00120	W	0x00000000	PP input size and -cropping register
VDPU_SWREG73	0x00124	W	0x00000000	PP input picture base address for Y bottom field
VDPU_SWREG74	0x00128	W	0x00000000	PP input picture base for Ch bottom field
VDPU_SWREG79	0x0013c	W	0x00000000	Scaling ratio register 1 & padding for B
VDPU_SWREG80	0x00140	W	0x00000000	Scaling register 0 ratio & padding for R and G
VDPU_SWREG81	0x00144	W	0x00000000	Scaling ratio register 2
VDPU_SWREG82	0x00148	W	0x00000000	Rmask register
VDPU_SWREG83	0x0014c	W	0x00000000	Gmask register
VDPU_SWREG84	0x00150	W	0x00000000	Bmask register
VDPU_SWREG85	0x00154	W	0x00000000	Post-processor control register
VDPU_SWREG86	0x00158	W	0x00000000	Mask 1 start coordinate register
VDPU_SWREG87	0x0015c	W	0x00000000	Mask 2 start coordinate register
VDPU_SWREG88	0x00160	W	0x00000000	Mask 1 size and PP original width register
VDPU_SWREG89	0x00164	W	0x00000000	Mask 2 size register
VDPU_SWREG90	0x00168	W	0x00000000	PiP register 0
VDPU_SWREG91	0x0016c	W	0x00000000	PiP register 1 and dithering control
VDPU_SWREG92	0x00170	W	0x00000000	Display width and PP input size extension register

Name	Offset	Size	Reset Value	Description
VDPU_SWREG93	0x00174	W	0x00000000	Display width and PP input size extension register
VDPU_SWREG94	0x00178	W	0x00000000	Base address for alpha blend 2 gui component
VDPU_SWREG95	0x0017c	W	0x00000000	Base address for alpha blend 2 gui component
VDPU_SWREG98	0x00188	W	0x00000000	PP output width/height extension
VDPU_SWREG99	0x0018c	W	0xe000f000	PP fuse register (read only)
VDPU_SWREG100	0x00190	W	0xff874780	Synthesis configuration register post-processor (read only)
VDPU_SWREG101	0x00194	W	0x00000000	soft reset signals
VDPU_SWREG102	0x00198	W	0x00000000	vpu performance cycle
VDPU_SWREG103	0x0019c	W	0x00000000	AXI DDR READ DATA NUM
VDPU_SWREG104	0x001a0	W	0x00000000	Register0000 Abstract
VDPU_SWREG105	0x001a4	W	0x00000000	
VDPU_SWREG106	0x001a8	W	0x00000000	
VDPU_SWREG107	0x001ac	W	0x00000000	

Notes: Size : **B** - Byte (8 bits) access, **HW** - Half WORD (16 bits) access, **W** - WORD (32 bits) access

16.4.10 Detail Register Description

VDPU_SWREG0

Address: Operational Base + offset (0x000000)

Register0000 Abstract

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	pro_num product number
15:12	RW	0x0	major_version major_version major_version
11:4	RW	0x00	minor_version minor_version minor_version
3	RW	0x0	ID_ASCII_EN ASCII type product ID enable ASCII type product ID enable

Bit	Attr	Reset Value	Description
2:0	RW	0x0	build_version build_version build_version

VDPU_SWREG1

Address: Operational Base + offset (0x00004)

interrupt register decoder

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24	RW	0x0	reserved
23:19	RO	0x0	reserved
18	RW	0x0	sw_dec_timeout Interrupt status bit decoder timeout. When high the decoder 0 has been idling for too long. HW will self reset. Possible only if timeout interrupt is enabled [note]:the h264 and vp8 decoder will use these bits.
17	RW	0x0	sw_dec_slice_int Interrupt status bit dec_slice_decoded. When high SW must set new base addresses for sw_dec_out_base and sw_jpg_ch_out_base before resetting this status bit. Used for JPEG and VP8 snapshot modes [note]:the JPEG decoder will use these bits.
16	RW	0x0	sw_dec_error_int Interrupt status bit input stream error. When high, an error is found in input data stream decoding. HW will self reset. [note]:the h264 and vp8 decoder will use these bits.
15	RW	0x0	sw_dec_aso_int Interrupt status bit ASO (Arbitrary Slice Ordering) detected. When high, ASO detected in input data stream decoding. HW will self reset. [note]:the h264 decoder will use these bits.
14	RW	0x0	sw_dec_buffer_int Interrupt status bit input buffer empty. When high, input stream buffer is empty but picture is not ready. HW will not self reset. [note]:the h264 and vp8 decoder will use these bits.

Bit	Attr	Reset Value	Description
13	RW	0x0	sw_dec_bus_int Interrupt status bit bus. Error response from bus. HW will self reset. [note]:the h264 and vp8 decoder will use these bits.
12	RW	0x0	sw_dec_rdy_int Interrupt status bit decoder. When this bit is high decoder has decoded a picture. HW will self reset. [note]:the h264 and vp8 decoder will use these bits.
11:9	RO	0x0	reserved
8	RW	0x0	sw_dec_irq Decoder IRQ. When high, decoder requests an interrupt. SW will reset this after interrupt is handled. [note]:the h264 and vp8 decoder will use these bits.
7:5	RO	0x0	reserved
4	RW	0x0	sw_dec_irq_dis Decoder IRQ disable. When high, there are no interrupts concerning decoder from HW. Polling must be used to see the interrupt statuses. [note]:the h264 and vp8 decoder will use these bits.
3:1	RO	0x0	reserved
0	RW	0x0	sw_dec_en decoder enable. Decoder enable. Setting this bit high will start the decoding operation. HW will reset this when picture is processed or ASO or stream error is detected or bus error or timeout interrupt is given. [note]:the h264 and vp8 decoder will use these bits.

VDPU_SWREG2

Address: Operational Base + offset (0x000008)
 device configuration register decoder

Bit	Attr	Reset Value	Description
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Bit	Attr	Reset Value	Description
31:24	RW	0x01	<p>sw_dec_axi_rd_id Read ID used for decoder reading services in AXI bus (if connected to AXI) [note]:the h264 and vp8 decoder will use these bits.</p>
23	RW	0x0	<p>sw_dec_timeout_e Timeout interrupt enable. If enabled HW may return timeout interrupt in case HW gets stucked while decoding picture. [note]:the h264 and vp8 decoder will use these bits.</p>
22	RW	0x0	<p>sw_dec_strswap32_e Decoder input 32bit data swap for stream data (may be used for 64 bit environment): 0 = no swapping of 32 bit words 1 = 32 bit data words are swapped (needed in 64 bit environment to achieve 7-6-5-4-3-2-1-0 byte order(also little endian should be enabled)) [note]:the h264 and vp8 decoder will use these bits.</p>
21	RW	0x0	<p>sw_dec_strendian_e Decoder input endian mode for stream data: 0 = Big endian (0-1-2-3 order) 1 = Little endian (3-2-1-0 order) [note]:the h264 and vp8 decoder will use these bits.</p>
20	RW	0x0	<p>sw_dec_inswap32_e Decoder input 32bit data swap for other than stream data (may be used for 64 bit environment): 0 = no swapping of 32 bit words 1 = 32 bit data words are swapped (needed in 64 bit environment to achieve 7-6-5-4-3-2-1-0 byte order(also little endian should be enabled)) [note]:the h264 and vp8 decoder will use these bits.</p>

Bit	Attr	Reset Value	Description
19	RW	0x0	<p>sw_dec_outswap32_e Decoder output 32bit data swap (may be used for 64 bit environment): 0 = no swapping of 32 bit words 1 = 32 bit data words are swapped (needed in 64 bit environment to achieve 7-6-5-4-3-2-1-0 byte order(also little endian should be enabled)) [note]:the h264 and vp8 decoder will use these bits.</p>
18	RW	0x0	<p>sw_dec_data_disc_e Data discard enable. Precise burst lengths are used with reading services. Extra data is discarded internally. [note]:the h264 and vp8 decoder will use these bits.</p>
17	RW	0x0	<p>sw_tiled_mode_msb Tiled mode msb. Concatenated to Tiled mode lsb which form 2 bit tiled mode. Definition of tiledmode: 0 = Tiled mode not enabled 1 = Tiled mode enabled for 8x4 tile size 2,3 Reserved [note]:the h264 and vp8 decoder will use these bits.</p>
16:11	RW	0x00	<p>sw_dec_latency Decoder master interface additional latency. Can be used to slow down decoder HW between services in steps of 8 clock cycles: 0 = no latency 1 = minimum 8 cycles of IDLE between services 2 = minimum 16 cycles of IDLE between services ... 63 = minimum latency of 504 cycles of IDLE between services [note]:the h264 and vp8 decoder will use these bits.</p>

Bit	Attr	Reset Value	Description
10	RW	0x1	<p>sw_dec_clk_gate_e Decoder dynamic clock gating enable: 0 = Clock is running for all structures 1 = Clock is gated for decoder structures that are not used Note: Clock gating value can be changed only when decoder is disabled</p>
9	RW	0x0	<p>sw_dec_in_endian Decoder input endian mode for other than stream data: 0 = Big endian (0-1-2-3 order) 1 = Little endian (3-2-1-0 order) [note]:the h264 and vp8 decoder will use these bits.</p>
8	RW	0x0	<p>sw_dec_out_endian Decoder output endian mode: 0 = Big endian (0-1-2-3 order) 1 = Little endian (3-2-1-0 order) [note]:the h264 and vp8 decoder will use these bits.</p>
7	RW	0x0	<p>sw_tiled_mode_lsb Tiled mode lsb. Concatenated to Tiled mode msb which form 2 bit tiled mode. Defined in tiled_mode_msb [note]:the h264 and vp8 decoder will use these bits.</p>
6	RW	0x0	<p>sw_dec_adv_pre_dis Advanced PREFETCH mode disable (advanced reference picture reading mode for video) [note]:the h264 and vp8 decoder will use these bits.</p>
5	RW	0x0	<p>sw_dec_scmd_dis AXI Single Command Multiple Data 0 disable. (where only the first addresses of the burst are given from address generator). This bit is used to disable the feature (possible SW workaround if something is not working correctly) [note]:the h264 and vp8 decoder will use these bits.</p>

Bit	Attr	Reset Value	Description
4:0	RW	0x00	<p>sw_dec_max_burst Maximum burst length for decoder bus transactions. Valid values: AXI: 1-16 [note]:the h264 and vp8 decoder will use these bits.</p>

VDPU_SWREG3

Address: Operational Base + offset (0x0000c)
Device control register 0(decmode, picture type etc)

Bit	Attr	Reset Value	Description
31:28	RW	0x0	<p>sw_dec_mode Decoding mode: 0 = H.264, 1 = MPEG-4, 2 = H.263, 3 = JPEG, 4 = VC-1, 5 = MPEG-2, 6 = MPEG-1, 7 = Reserved, 8 = Reserved, 9 = VP7, 10 = VP8, 11 = AVS, others = reserved [note]:all the decoder mode will use these bits.</p>
27	RW	0x0	<p>sw_rlc_mode_e RLC mode enable: 1 = HW decodes video from RLC input data + side information (Differential MV's, separate DC coeffs, Intra 4x4 modes, MB control). Valid only for H.264 Baseline and MPEG- 4 SP. 0 = HW decodes video from bit stream (VLC mode) + side information (bitplane data in VC-1) [note]:the h264 and MPEG4 decoder will use these bits.</p>

Bit	Attr	Reset Value	Description
26	RW	0x0	sw_skip_mode AVS: 0: special MB type code indicates skipped mbs 1 means that skipped mbs are indicated using skip_run -syntax element like in VP8: 0 : HW decodes mb_coeff_skip -flag 1 : HW does not decode mb_coeff_skip -flag [note]:the vp8 decoder will use these bits.
25	RW	0x0	Reserved
24	RW	0x0	sw_pjpeg_e Progressive JPEG enable: 0 = baseline JPEG 1 = progressive JPEG
23	RW	0x0	sw_pic_interlace_e Coding mode of the current picture: 0 = progressive 1 = interlaced [note]:the h264 decoder will use these bits.
22	RW	0x0	sw_pic_fieldmode_e Structure of the current picture (residual structure) 0 = frame structure, this means MBAFF structured picture for interlaced sequence 1 = field structure [note]:the h264 decoder will use these bits.
21	RW	0x0	sw_pic_b_e B picture enable for current picture: 0=picture type is I or P depending on sw_pic_inter_e 1=picture type is BI (vc1)/D (mpeg1) or B depending on sw_pic_inter_e (not valid for H264 since its slice based information)
20	RW	0x0	sw_pic_inter_e Picture type. 1= Inter type (P) 0= Intra type (I) See also sw_pic_b_e [note]:the vp8 decoder will use these bits.
19	RW	0x0	sw_pic_topfield_e If field structure is enabled this bit informs which one of the fields is being decoded: 0 = bottom field 1 = top field [note]:the h264 decoder will use these bits.

Bit	Attr	Reset Value	Description
18	RW	0x0	<p>sw_fwd_interlace_e Coding mode of forward reference picture: 0 = progressive 1 = interlaced Note: for backward reference picture the coding mode is always same as for current picture.</p>
17	RW	0x0	<p>sw_sorenson_e Sorenson Sparc enable (possible if sw_dec_mode is MPEG- 4) 0 = disabled 1 = H.263 compatible stream with Sorenson escape coding</p>
16	RW	0x0	<p>sw_ref_topfield_e Indicates which field should be used as reference if sw_ref_frames = 0 : 0 = bottom field 1 = top field used only in VC-1 mode</p>
15	RW	0x0	<p>sw_dec_out_dis Disable decoder output picture writing: 0 = Decoder output picture is written to external memory 1 = Decoder output picture is not written to external memory [note]:the h264 and vp8 decoder will use these bits.</p>
14	RW	0x0	<p>sw_filtering_dis De-block filtering disable 1 = filtering is disabled for current picture 0 = filtering is enabled for current picture [note]:the h264 decoder will use these bits.</p>
13	RW	0x0	<p>sw_pic_fixed_quant sw_pic_fixed_quant (DEC mode is VC-1 and AVS) 0 = Quantization parameter can vary inside picture 1 = Quantization parameter is fixed (pquant) sw_mvc_e(DEC mode is H264) multi view coding enable. Possible for H264 only [note]:the h264 decoder will use these bits.</p>

Bit	Attr	Reset Value	Description
12	RW	0x0	<p>sw_write_mvs_e Direct mode motion vector write enable for current picture / MPEG2 motion vector write enable for error concealment purposes: 0 = writing disabled for current picture 1 = the direct mode motion vectors are written to external memory. H264 direct mode motion vectors are written to DPB aside with the corresponding reference picture. Other decoding mode dir mode mvs are written to external memory starting from sw_dir_mv_base [note]:the h264 decoder will use these bits.</p>
11	RW	0x0	<p>sw_reftopfirst_e Indicates which FWD reference field has been decoded first. 0 = FWD reference bottom field 1 = FWD reference top field [note]:the h264 decoder will use these bits.</p>
10	RW	0x0	<p>sw_seq_mbaff_e Sequence includes MBAFF coded pictures [note]:the h264 decoder will use these bits.</p>
9	RW	0x0	<p>sw_picord_count_e h264_high config: Picture order count table read enable. If enabled HW will read picture order counts from memory in the beginning of picture [note]:the h264 decoder will use these bits.</p>
8	RW	0x0	<p>sw_dec_timeout_mode dec timeout mode selset when 1'b0 , timeout cycle is 181'b1 when 1'b1, timeout cycle is 221'b1 [note]:the h264 and vp8 decoder will use these bits.</p>
7:0	RW	0x01	<p>sw_dec_axi_wr_id Write ID used for decoder writing services in AXI bus (if connected to AXI) [note]:the h264 and vp8 decoder will use these bits.</p>

VDPU_SWREG4_H264

Address: Operational Base + offset (0x00010)
decoder control register 1(picture parameters)

Bit	Attr	Reset Value	Description
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Bit	Attr	Reset Value	Description
31:23	RW	0x000	sw_pic_mb_width Picture width in macroblocks = ((width in pixels + 15) /16) [note]:the h264 decoder will use these bits.
22:19	RO	0x0	reserved
18:11	RW	0x00	sw_pic_mb_height_p Picture height in macroblocks =((height in pixels+15)/16). Picture height is informed as size of the (progressive) frame also for single field (of interlaced content) is being decoded [note]:the h264 decoder will use these bits.
10:5	RO	0x0	reserved
4:0	RW	0x00	sw_ref_frames 264: num_ref_frames, maximum number of short and long term reference frames in decoded picture buffer.

VDPU_SWREG4

Address: Operational Base + offset (0x00010)
decoder control register 1(picture parameters)

Bit	Attr	Reset Value	Description
31:23	RW	0x000	sw_pic_mb_width Picture width in macroblocks = ((width in pixels + 15) /16) [note]:the vp8 decoder will use these bits.
22:19	RW	0x0	sw_mb_width_off The amount of meaningfull horizontal pixels in last MB (width offset) 0 if exactly 16 pixels multiple picture and all the horizontal pixels in last MB are meaningfull
18:11	RW	0x00	sw_pic_mb_height_p Picture height in macroblocks =((height in pixels+15)/16). Picture height is informed as size of the (progressive) frame also for single field (of interlaced content) is being decoded [note]:the vp8 decoder will use these bits.
10:7	RW	0x0	sw_mb_height_off The amount of menaingfull vertical pixels in last MB (height offset 0 if exactly 16 pixels multiple picture and all the vertical pixels in last MB are meaningfull

Bit	Attr	Reset Value	Description
6	RW	0x0	sw_alt_scan_e indicates alternative vertical scan method used for interlaced frames
5:3	RW	0x0	sw_pic_mb_w_ext Picture mb width extension. If sw_pic_mb_width does not fit to 9 bits then these bits are used to increase the range upto 11 bits (used as 3 msb)
2:0	RW	0x0	sw_pic_mb_h_ext Picture mb height extension. If sw_pic_mb_height_p does not fit to 9 bits then these bits are used to increase the range upto 11 bits (used as 3 msb)

VDPU_SWREG5

Address: Operational Base + offset (0x00014)
decoder control register2 (stream decoding table selects)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	sw_strm_start_bit Exact bit of stream start word where decoding can be started (associates with sw_rlc_vlc_base)
25	RW	0x0	sw_sync_marker_e Sync markers enable: '0' = synch markers are not used, '1' = synch markers are used. For progressive JPEG this indicates that there are restart markers in the stream after restart interval steps
24	RW	0x0	sw_type1_quant_e MPEG4: Type 1 quantization enable '0' = type 2 inverse Q method '1' = type 1 inverse Q method (Q-tables used) H264 (h264_high config): scaling matrix enable: '0' = normal transform '1' = use scaling matrix for transform (read from external)
23:19	RW	0x00	sw_ch_qp_offset Chroma Qp filter offset. (For H.264 this offset concerns Cb only)
18:14	RW	0x00	sw_ch_qp_offset2 Chroma Qp filter offset for cr type
13:1	RO	0x0	reserved

Bit	Attr	Reset Value	Description
0	RW	0x0	sw_fieldpic_flag_e Flag for streamd that field_pic_flag exists in stream

VDPU_SWREG5_H264

Address: Operational Base + offset (0x00014)
decoder control register2 (stream decoding table selects)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	sw_strm_start_bit Exact bit of stream start word where decoding can be started (associates with sw_rlc_vlc_base)
25	RO	0x0	reserved
24	RW	0x0	sw_type1_quant_e MPEG4: Type 1 quantization enable '0' = type 2 inverse Q method '1' = type 1 inverse Q method (Q-tables used) H264 (h264_high config): scaling matrix enable: '0' = normal transform '1' = use scaling matrix for transform (read from external)
23:19	RW	0x00	sw_ch_qp_offset Chroma Qp filter offset. (For H.264 this offset concerns Cb only)
18:14	RW	0x00	sw_ch_qp_offset2 Chroma Qp filter offset for cr type
13:1	RO	0x0	reserved
0	RW	0x0	sw_fieldpic_flag_e Flag for streamd that field_pic_flag exists in stream

VDPU_SWREG5_VP8

Address: Operational Base + offset (0x00014)
decoder control register2 (stream decoding table selects)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	sw_strm_start_bit Exact bit of stream start word where decoding can be started (associates with sw_rlc_vlc_base)
25:24	RO	0x0	reserved
23:18	RW	0x00	sw_strm1_start_bit it for ctrl-stream (needed if multistream is enabled, associates with sw_bitpl_ctrl_base)

Bit	Attr	Reset Value	Description
17:16	RO	0x0	reserved
15:8	RW	0x00	sw_boolean_value initial value for boolean dec 0
7:0	RW	0x00	sw_boolean_range initial range for boolean dec 0

VDPU_SWREG6

Address: Operational Base + offset (0x00018)
 decoder control register 3(stream buffer information)

Bit	Attr	Reset Value	Description
31	RW	0x0	sw_start_code_e Bit for indicating stream start code existence: '0' = stream doesn't contain start codes '1' = stream contains start codes [note]:the h264 decoder will use these bits.
30:25	RW	0x00	sw_init_qp Initial value for quantization parameter (picture quantizer). [note]:the h264 decoder will use these bits.
24	RW	0x0	sw_ch_8pix_ileav_e Enable for additional chrominance data format writing where decoder writes chrominance in group of 8 pixels of Cb and then corresponding 8 pixels of Cr. Data is written to sw_dec_ch8pix_base. Cannot be used if tiled mode is enabled [note]:the h264 decoder will use these bits.
23:0	RW	0x000000	sw_stream_len Amount of stream data bytes in input buffer. If the given buffer size is not enough for finishing the picture the corresponding interrupt is given and new stream buffer base address and stream buffer size information should be given (associates with sw_rlc_vlc_base). For VC-1 the buffer must include data for one picture/slice of the picture For H264/MPEG4/H263/MPEG2/MPEG1 the buffer must include at least data for one slice/VP of the picture For JPEG the buffer size must be a multiple of 256 bytes or the amount of data for one picture. [note]:the h264 and vp8 decoder will use these bits.

VDPU_SWREG7

Address: Operational Base + offset (0x0001c)
 decoder control register 4(H264, VC-1 control)

Bit	Attr	Reset Value	Description
31	RW	0x0	sw_cabac_e CABAC enable [note]:the h264 decoder will use these bits.
30	RW	0x0	sw_blackwhite_e '0' = 4:2:0 sampling format '1' = 4:0:0 sampling format (H264 monochroma) [note]:the h264 decoder will use these bits.
29	RW	0x0	sw_dir_8x8_infer_e Specifies the method to use to derive luma motion vectors in B_skip, B_Direct_16x16 and B_direct_8x8_inference_flag (see direct_8x8_inference_flag) [note]:the h264 decoder will use these bits.
28	RW	0x0	sw_weight_pred_e Weighted prediction enable for P slices [note]:the h264 decoder will use these bits.
27:26	RW	0x0	sw_weight_bipr_idc weighted prediction specification for B slices: "00" = default weighted prediction is applied to B slices "01" = explicit weighted prediction shall be applied to B slices "10" = implicit weighted prediction shall be applied to B slices [note]:the h264 decoder will use these bits.
25:21	RO	0x0	reserved
20:16	RW	0x00	sw_framenum_len H.264: Bit length of frame_num in data stream RV: frame size length. Informs how many bits in stream are used for frame size (HW discards these bits) [note]:the h264 decoder will use these bits.
15:0	RW	0x0000	sw_framenum current frame_num, used to identify short-term reference frames. Used in reference picture reordering [note]:the h264 decoder will use these bits.

VDPU_SWREG7_VP8

Address: Operational Base + offset (0x0001c)

decoder control register 4(H264, VC-1 control)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	sw_dct1_start_bit start bits for VP7/VP8 DCT stream partition index 1
25:20	RW	0x00	sw_dct2_start_bit start bits for VP7/VP8 DCT stream partition index 2
19:14	RO	0x0	reserved
13	RW	0x0	sw_ch_mv_res VP7/VP8 Chrominance motion vector resolution: '0' = Full pixel '1' = 1/8 pixel
12	RW	0x0	sw_bilin_mc_e bilinear motion compensation enable: '0' = Bicubic interpolation used '1' = Bilinear interpolation used
11:9	RW	0x0	sw_init_dc_match0 initial DC prediction match count 0. After HW has decoded a picture HW returns the final match count0 information which is read by SW
8:6	RW	0x0	sw_init_dc_match1 initial DC prediction match count 1. After HW has decoded a picture HW returns the final match count1 information which is read by SW
5	RW	0x0	sw_vp7_version VP7 version information to streamd: '0'= vp7 version 7.0 '1'= vp7 version 7.1 or better
4:0	RO	0x0	reserved

VDPU_SWREG8

Address: Operational Base + offset (0x000020)

decoder control register 5(H264, VC-1)

Bit	Attr	Reset Value	Description
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Bit	Attr	Reset Value	Description
31	RW	0x0	sw_const_intra_e constrained_intra_pred_flag equal to 1 specifies that intra prediction uses only neighbouring intra macroblocks in prediction. When equal to 0 also neighbouring inter macroblocks are used in intra prediction process. [note]:the h264 decoder will use these bits.
30	RW	0x0	sw_filt_ctrl_pres deblocking_filter_control_present_flag indicates whether extra variables controlling characteristics of the deblocking filter are present in the slice header. [note]:the h264 decoder will use these bits.
29	RW	0x0	sw_rdpic_cnt_pres redundant_pic_cnt_present_flag specifies whether redundant_pic_cnt syntax elements [note]:the h264 decoder will use these bits.
28	RW	0x0	sw_8x8trans_flag_e 8x8 transform flag enable for stream decoding [note]:the h264 decoder will use these bits.
27:17	RW	0x000	sw_refpic_mk_len Length of decoded reference picture marking bits [note]:the h264 decoder will use these bits.
16	RW	0x0	sw_idr_pic_e IDR (instantaneous decoding refresh) picture flag. [note]:the h264 decoder will use these bits.
15:0	RW	0x0000	sw_idr_pic_id idr_pic_id, identifies IDR (instantaneous decoding refresh) picture [note]:the h264 decoder will use these bits.

VDPU_SWREG8_VP8

Address: Operational Base + offset (0x00020)
decoder control register 5(H264, VC-1)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	sw_init_dc_comp0 initial DC predictor value 0. After HW has decoded a picture HW returns the final predictor value information which is read by SW

Bit	Attr	Reset Value	Description
15:0	RW	0x0000	sw_init_dc_comp1 initial DC predictor value 1. After HW has decoded a picture HW returns the final predictor value information which is read by SW

VDPU_SWREG9

Address: Operational Base + offset (0x00024)

decoder control register 6

Bit	Attr	Reset Value	Description
31:24	RW	0x00	sw_pps_id pic_parameter_set_id, identifies the picture parameter set that is referred to in the slice header. [note]:the h264 decoder will use these bits.
23:19	RW	0x00	sw_refidx1_active Specifies the maximum reference index that can be used while decoding inter predicted macro blocks. [note]:the h264 decoder will use these bits.
18:14	RW	0x00	sw_refidx0_active Specifies the maximum reference index that can be used while decoding inter predicted macro blocks. This is same as in previous decoders (width increased with q bit) [note]:the h264 decoder will use these bits.
13:8	RO	0x0	reserved
7:0	RW	0x00	sw_poc_length Length of picture order count field in stream [note]:the h264 decoder will use these bits.

VDPU_SWREG9_VP8

Address: Operational Base + offset (0x00024)

decoder control register 6

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:24	RW	0x0	sw_coeffs_part_am VP7/VP8 number of coefficient partitions (should it be number of additional DCT partitions with range 0)

Bit	Attr	Reset Value	Description
23:0	RW	0x000000	sw_stream1_len amount of CTRL stream data bytes in input buffer. (needed if multistream is enabled or VP7/VP8 format, assosiates with sw_bitpl_ctrl_base)

VDPU_SREG10_H264_RLC

Address: Operational Base + offset (0x00028)
 Base address for differential motion vector base address

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	sw_diff_mv_base for H264 and MPEG4, RLC mode: Differential motion vector base address.
1:0	RO	0x0	reserved

VDPU_SREG10_H264

Address: Operational Base + offset (0x00028)
 Base address for differential motion vector base address

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:25	RW	0x00	sw_pinit_rlist_f9 initial reference picture list for P forward picid 9
24:20	RW	0x00	sw_pinit_rlist_f8 initial reference picture list for P forward picid 8
19:15	RW	0x00	sw_pinit_rlist_f7 initial reference picture list for P forward picid 7
14:10	RW	0x00	sw_pinit_rlist_f6 initial reference picture list for P forward picid 6
9:5	RW	0x00	sw_pinit_rlist_f5 initial reference picture list for P forward picid 5
4:0	RW	0x00	sw_pinit_rlist_f4 initial reference picture list for P forward picid 4

VDPU_SREG10_VP8

Address: Operational Base + offset (0x00028)
 Base address for differential motion vector base address

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	sw_segment_base VP7/VP8: base address for segmentation map values 0

Bit	Attr	Reset Value	Description
1	RW	0x0	sw_segment_upd_e VP7/VP8 Segmentation map update enable: '0': segmentation values are read from external memory (from segment_base) '1': segmentation update is included in stream
0	RW	0x0	sw_segment_e segmentation enable: '0': segmentation is not enabled '1': segmentation is enabled (sw_segment_upd_e value is used)

VDPU_SWREG11_H264_RLC

Address: Operational Base + offset (0x0002c)
decoder control register 7

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	sw_i4x4_or_dc_base RLC mode: H.264: Intra prediction 4x4 mode base address. RLC mode: MPEG-4: DC component base address.
1:0	RO	0x0	reserved

VDPU_SWREG11_H264

Address: Operational Base + offset (0x0002c)
decoder control register 7

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:25	RW	0x00	sw_pinit_rlist_f15 Initial reference picture list for P forward picid 15
24:20	RW	0x00	sw_pinit_rlist_f14 Initial reference picture list for P forward picid 14
19:15	RW	0x00	sw_pinit_rlist_f13 Initial reference picture list for P forward picid 13
14:10	RW	0x00	sw_pint_rlist_f12 Initial reference picture list for P forward picid 12
9:5	RW	0x00	sw_pint_rlist_f11 Initial reference picture list for P forward picid 11

Bit	Attr	Reset Value	Description
4:0	RW	0x00	sw_pint_rlist_f10 Initial reference picture list for P forward picid 10

VDPU_SWREG11_VP8

Address: Operational Base + offset (0x0002c)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:24	RW	0x00	sw_dct3_start_bit Start for VP7/VP8 DCT stream partition index 3
23:18	RW	0x00	sw_dct4_start_bit Start for VP7/VP8 DCT stream partition index 4
17:12	RW	0x00	sw_dct5_start_bit Start for VP7/VP8 DCT stream partition index 5
11:6	RW	0x00	sw_dct6_start_bit Start for VP7/VP8 DCT stream partition index 6
5:0	RW	0x00	sw_dct7_start_bit Start for VP7/VP8 DCT stream partition index 7

VDPU_SWREG12

Address: Operational Base + offset (0x00030)

Base address for RLC data (RLC) / stream start address/decoded

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	sw_rlc_vlc_base RLC mode: Base address for RLC data (swreg3.sw_rlc_mode_e = 1). VLC mode: Stream start address / end addr+I288ess with byte precision (swreg4.rlc_mode_en = 0), start bit number in swreg5.stream_start_bit. When sw_dec_buffer_int is high or sw_dec_e is low this register contains HW return value of last_byte_address (not valid for jpeg) where stream has been read (and used) in accuracy of byte. For debug purposes the last_byte_address is also written when stream error/ASO is detected even though it may not be accurate. VP7/VP8: This base address is used as sw_dct_strm0_base including DCT stream for MB rows 0,2n [note]:the h264 and vp8 decoder will use these bits.
1:0	RO	0x0	reserved

VDPU_SWREG13

Address: Operational Base + offset (0x00034)

Base address for decoded picture / base address for JPEG deco

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	sw_dec_out_base Video: Base address for decoder output picture. Points directly to start of decoder output picture or field. JPEG/VP8 snapshot: Base address for decoder output luminance picture [note]:the h264 and vp8 decoder will use these bits.
1:0	RO	0x0	reserved

VDPU_SWREG14

Address: Operational Base + offset (0x00038)

Base address for reference picture index 0 / base address for J

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	sw_refer0_base Base address for reference picture index 0. See picture index definition from toplevel_sp [note]:the h264 decoder will use these bits.
1	RW	0x0	sw_refer0_field_e Refer picture consist of single fields or frame: '0' = reference picture consists of frame '1' = reference picture consists of fields [note]:the h264 decoder will use these bits.
0	RW	0x0	sw_refer0_topc_e Which field of reference picture is closer to current picture: '0' = bottom field is closer to current picture '1' = top field is closer to current picture [note]:the h264 decoder will use these bits.

VDPU_SWREG14_VP8

Address: Operational Base + offset (0x00038)

Base address for reference picture index 0 / base address for J

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	sw_ch_out_base base address for decoder output chrominance picture. Used in JPEG and VP8 intra picture mode (not needed if decoder output is not written)
1:0	RO	0x0	reserved

VDPU_SWREG15_JPEG_ROI

Address: Operational Base + offset (0x0003c)

JPEG roi control

Bit	Attr	Reset Value	Description
31:20	RO	0x0	reserved
19	RW	0x0	sw_jpegroi_in_endian jpeg offset input endian sw_jpegroi_in_endian 0 = big endian (0-1-2-3 order) 1 = little endian (3-2-1-0 order)
18	RW	0x0	sw_jpegroi_in_swap32 jpeg offset input 32-bit swap sw_jpegroi_in_swap32 0: no swapping of 32 bit words 1: 32bit data words are swapped (needed in 64 bit environment to achieve 7-6-5-4-3-2-1 byte order (also little endian should be enabled))
17:16	RW	0x0	sw_roi_sample_size ROI MB num sample each time ROI MB num sample each time 00 01 10 11
15:12	RW	0x0	sw_roi_distance roi distance The distance between the sample MB and ROI start MB
11:10	RW	0x0	sw_roi_out_sel roi output selection ROI output selection 00: output offset/dc 01: output picture 10: output offset/dc and picture 11: output offset/dc
9	RW	0x0	sw_roi_decode roi decode JPEG ROI decode 0: build offset/dc table 1: ROI decode

Bit	Attr	Reset Value	Description
8	RW	0x0	sw_roi_en roi enable JPEG roi mode enable 0: normal jpeg decode mode 1: JPEG roi mode
7:0	RO	0x0	reserved

VDPU_SWREG15

Address: Operational Base + offset (0x0003c)
Base address for reference picture index 1 / JPEG control

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	sw_refer1_base Base address for reference picture index 1. See picture index definition from toplevel_sp [note]:the h264 and vp8 decoder will use these bits.
1	RW	0x0	sw_refer1_field_e Refer picture consist of single fields or frame: '0' = reference picture consists of frame '1' = reference picture consists of fields
0	RW	0x0	sw_refer1_topc_e Which field of reference picture is closer to current picture: '0' = bottom field is closer to current picture '1' = top field is closer to current picture

VDPU_SWREG15_VP8

Address: Operational Base + offset (0x0003c)
Base address for reference picture index 1 / JPEG control

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RW	0x00	sw_slice_h Slice mode must be used if picture size is more than 16 Mpixels. However for bigger than 4096 MBs the slice mode usage is recommended

VDPU_SWREG16

Address: Operational Base + offset (0x00040)
base address for reference picture index 2 / List of VLC code len

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	sw_refer2_base Base address for reference picture index 2. See picture index definition from toplevel_sp [note]:the h264 decoder will use these bits.

Bit	Attr	Reset Value	Description
1	RW	0x0	sw_refer2_field_e Refer picture consist of single fields or frame: '0' = reference picture consists of frame '1' = reference picture consists of fields [note]:the h264 decoder will use these bits.
0	RW	0x0	sw_refer2_topc_e Which field of reference picture is closer to current picture: '0' = bottom field is closer to current picture '1' = top field is closer to current picture [note]:the h264 decoder will use these bits.

VDPU_SWREG17

Address: Operational Base + offset (0x00044)

Base address for reference picture index 3 / List of VLC code ie

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	sw_refer3_base Base address for reference picture index 3. See picture index definition from toplevel_sp [note]:the h264 decoder will use these bits.
1	RW	0x0	sw_refer3_field_e Refer picture consist of single fields or frame: '0' = reference picture consists of frame '1' = reference picture consists of fields [note]:the h264 decoder will use these bits.
0	RW	0x0	sw_refer3_topc_e Which field of reference picture is closer to current picture: '0' = bottom field is closer to current picture '1' = top field is closer to current picture [note]:the h264 decoder will use these bits.

VDPU_SWREG18

Address: Operational Base + offset (0x00048)

Base address for reference picture index 4 / VC1 control / MPE

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	sw_refer4_base Base address for reference picture index 4. See picture index definition from toplevel_sp [note]:the h264 and vp8 decoder will use these bits.

Bit	Attr	Reset Value	Description
1	RW	0x0	sw_refer4_field_e Refer picture consist of single fields or frame: '0' = reference picture consists of frame '1' = reference picture consists of fields [note]:the h264 decoder will use these bits.
0	RW	0x0	sw_refer4_topc_e Which field of reference picture is closer to current picture: '0' = bottom field is closer to current picture '1' = top field is closer to current picture [note]:the h264 decoder will use these bits.

VDPU_SWREG18_VP8

Address: Operational Base + offset (0x00048)

Base address for reference picture index 4 / VC1 control / MPE

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	sw_refer4_base Base address for reference picture index 4. See picture index definition from toplevel_sp
1	RO	0x0	reserved
0	RW	0x0	sw_gref_sign_bias reference picture sign bias for Golden reference frame 0

VDPU_SWREG19

Address: Operational Base + offset (0x0004c)

Base address for reference picture index 5

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	sw_refer5_base Base address for reference picture index 5. See picture index definition from toplevel_sp [note]:the h264 decoder will use these bits.
1	RW	0x0	sw_refer5_field_e Refer picture consist of single fields or frame: '0' = reference picture consists of frame '1' = reference picture consists of fields [note]:the h264 decoder will use these bits.
0	RW	0x0	sw_refer5_topc_e Which field of reference picture is closer to current picture: '0' = bottom field is closer to current picture '1' = top field is closer to current picture [note]:the h264 decoder will use these bits.

VDPU_SWREG19_VP8

Address: Operational Base + offset (0x0004c)

Base address for reference picture index 5

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	sw_refer5_base Base address for reference picture index 5. See picture index definition from toplevel_sp [note]:the h264 decoder will use these bits.
1	RO	0x0	reserved
0	RW	0x0	sw_aref_sign_bias Reference picture sign bias for Alternate reference frame

VDPU_SWREG20

Address: Operational Base + offset (0x00050)

Base address for reference picture index 6

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	sw_refer6_base Base address for reference picture index 6. See picture index definition from toplevel_sp [note]:the h264 decoder will use these bits.
1	RW	0x0	sw_refer6_field_e Refer picture consist of single fields or frame: '0' = reference picture consists of frame '1' = reference picture consists of fields [note]:the h264 decoder will use these bits.
0	RW	0x0	sw_refer6_topc_e Which field of reference picture is closer to current picture: '0' = bottom field is closer to current picture '1' = top field is closer to current picture [note]:the h264 decoder will use these bits.

VDPU_SWREG21

Address: Operational Base + offset (0x00054)

Base address for reference picture index 7

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	sw_refer7_base Base address for reference picture index 7. See picture index definition from toplevel_sp [note]:the h264 decoder will use these bits.

Bit	Attr	Reset Value	Description
1	RW	0x0	sw_refer7_field_e Refer picture consist of single fields or frame: '0' = reference picture consists of frame '1' = reference picture consists of fields [note]:the h264 decoder will use these bits.
0	RW	0x0	sw_refer7_topc_e Which field of reference picture is closer to current picture: '0' = bottom field is closer to current picture '1' = top field is closer to current picture [note]:the h264 decoder will use these bits.

VDPU_SWREG22

Address: Operational Base + offset (0x000058)

Base address for reference picture index 8

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	sw_refer8_base Base address for reference picture index 8. See picture index definition from toplevel_sp
1	RW	0x0	sw_refer8_field_e Refer picture consist of single fields or frame: '0' = reference picture consists of frame '1' = reference picture consists of fields
0	RW	0x0	sw_refer8_topc_e Which field of reference picture is closer to current picture: '0' = bottom field is closer to current picture '1' = top field is closer to current picture

VDPU_SWREG22_VP8

Address: Operational Base + offset (0x000058)

Base address for reference picture index 8

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	sw_dct_strm1_base base address for VP7/VP8 DCT stream MB row 1,2n+1 0 30 R/
1:0	RO	0x0	reserved

VDPU_SWREG23

Address: Operational Base + offset (0x00005c)

Base address for reference picture index 9

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	sw_refer9_base Base address for reference picture index 9. See picture index definition from toplevel_sp

Bit	Attr	Reset Value	Description
1	RW	0x0	sw_refer9_field_e Refer picture consist of single fields or frame: '0' = reference picture consists of frame '1' = reference picture consists of fields
0	RW	0x0	sw_refer9_topc_e Which field of reference picture is closer to current picture: '0' = bottom field is closer to current picture '1' = top field is closer to current picture

VDPU_SWREG23_VP8

Address: Operational Base + offset (0x0005c)

Base address for reference picture index 9

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	sw_dct_strm2_base base address for VP7/VP8 DCT stream MB row 2,2n+2 0 30 R/
1:0	RO	0x0	reserved

VDPU_SWREG24

Address: Operational Base + offset (0x00060)

Base address for reference picture index 10

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	sw_refer10_base Base address for reference picture index 10. See picture index definition from toplevel_sp
1	RW	0x0	sw_refer10_field_e Refer picture consist of single fields or frame: '0' = reference picture consists of frame '1' = reference picture consists of fields
0	RW	0x0	sw_refer10_top_e Which field of reference picture is closer to current picture: '0' = bottom field is closer to current picture '1' = top field is closer to current picture

VDPU_SWREG24_VP8

Address: Operational Base + offset (0x00060)

Base address for reference picture index 10

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	sw_dct_strm3_base base address for VP7/VP8 DCT stream MB row 3,2n+3 0 30 R/W
1:0	RO	0x0	reserved

VDPU_SWREG25_VP8

Address: Operational Base + offset (0x000064)

Base address for reference picture index 10

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	sw_dct_strm4_base base address for VP7/VP8 DCT stream MB row 4,2n+4
1:0	RO	0x0	reserved

VDPU_SWREG25

Address: Operational Base + offset (0x000064)

Base address for reference picture index 11

Bit	Attr	Reset Value	Description
31:3	RO	0x0	reserved
2	RW	0x0	sw_refer11_base Base address for reference picture index 11. See picture index definition from toplevel_sp
1	RW	0x0	sw_refer11_field_e Refer picture consist of single fields or frame: '0' = reference picture consists of frame '1' = reference picture consists of fields
0	RW	0x0	sw_refer11_topc_e Which field of reference picture is closer to current picture: '0' = bottom field is closer to current picture '1' = top field is closer to current picture

VDPU_SWREG26_VP8

Address: Operational Base + offset (0x000068)

Base address for reference picture index 10

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	sw_dct_strm5_base base address for VP7/VP8 DCT stream MB row 5,2n+5
1:0	RO	0x0	reserved

VDPU_SWREG26

Address: Operational Base + offset (0x000068)

Base address for reference picture index 12

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	sw_refer12_base Base address for reference picture index 12. See picture index definition from toplevel_sp

Bit	Attr	Reset Value	Description
1	RW	0x0	sw_refer12_field_e Refer picture consist of single fields or frame: '0' = reference picture consists of frame '1' = reference picture consists of fields
0	RW	0x0	sw_refer12_topc_e Which field of reference picture is closer to current picture: '0' = bottom field is closer to current picture '1' = top field is closer to current picture

VDPU_SWREG27_VP8

Address: Operational Base + offset (0x00006c)

Base address for reference picture index 13

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	sw_bitpl_ctrl_base Base address for ctrl data stream. Used if multistream is enabled
1:0	RO	0x0	reserved

VDPU_SWREG27

Address: Operational Base + offset (0x00006c)

Base address for reference picture index 13

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	sw_refer13_base Base address for reference picture index 13. See picture index definition from toplevel_sp
1	RW	0x0	sw_refer13_field_e Refer picture consist of single fields or frame: '0' = reference picture consists of frame '1' = reference picture consists of fields
0	RW	0x0	sw_refer13_topc_e Which field of reference picture is closer to current picture: '0' = bottom field is closer to current picture '1' = top field is closer to current picture

VDPU_SWREG28_VP8

Address: Operational Base + offset (0x000070)

Base address for reference picture index 10

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	sw_dct_strm6_base base address for VP7/VP8 DCT stream MB row 6,2n+6
1:0	RO	0x0	reserved

VDPU_SWREG28

Address: Operational Base + offset (0x000070)

Base address for reference picture index14

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	sw_refer14_base Base address for reference picture index 14. See picture index definition from toplevel_sp
1	RW	0x0	sw_refer14_field_e Refer picture consist of single fields or frame: '0' = reference picture consists of frame '1' = reference picture consists of fields
0	RW	0x0	sw_refer14_topc_e Which field of reference picture is closer to current picture: '0' = bottom field is closer to current picture '1' = top field is closer to current picture

VDPU_SWREG29_VP8

Address: Operational Base + offset (0x000074)

Base address for reference picture index 10

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	sw_dct_strm7_base base address for VP7/VP8 DCT stream MB row 7,2n+7
1:0	RO	0x0	reserved

VDPU_SWREG29

Address: Operational Base + offset (0x000074)

Base address for reference picture index15

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	sw_refer15_base Base address for reference picture index 15. See picture index definition from toplevel_sp
1	RW	0x0	sw_refer15_field_e Refer picture consist of single fields or frame: '0' = reference picture consists of frame '1' = reference picture consists of fields
0	RW	0x0	sw_refer15_topc_e Which field of reference picture is closer to current picture: '0' = bottom field is closer to current picture '1' = top field is closer to current picture

VDPU_SWREG30

Address: Operational Base + offset (0x000078)

Reference picture numbers for index 0 and 1 (H264 VLC)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	sw_refer1_nbr Number for reference picture index 1
15:0	RW	0x0000	sw_refer0_nbr Number for reference picture index 0

VDPU_SWREG30_VP8

Address: Operational Base + offset (0x00078)

Reference picture numbers for index 0 and 1 (H264 VLC)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:21	RW	0x00	sw_filt_mb_adj_0 filter level adjustment for MB type 0
20:14	RW	0x00	sw_filt_mb_adj_1 filter level adjustment for MB type 1
13:7	RW	0x00	sw_filt_mb_adj_2 filter level adjustment for MB type 2
6:0	RW	0x00	sw_filt_mb_adj_3 filter level adjustment for MB type 3

VDPU_SWREG31

Address: Operational Base + offset (0x0007c)

Reference picture numbers for index 2 and 3 (H264 VLC) /

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	sw_refer3_nbr Number for reference picture index 3
15:0	RW	0x0000	sw_refer2_nbr Number for reference picture index 2

VDPU_SWREG31_VP8

Address: Operational Base + offset (0x0007c)

Reference picture numbers for index 2 and 3 (H264 VLC) /

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:21	RW	0x00	sw_filt_ref_adj_0 filter level adjustment for reference frame type 0
20:14	RW	0x00	sw_filt_ref_adj_1 filter level adjustment for reference frame type 1
13:7	RW	0x00	sw_filt_ref_adj_2 filter level adjustment for reference frame type 2

Bit	Attr	Reset Value	Description
6:0	RW	0x00	sw_filt_ref_adj_3 filter level adjustment for reference frame type 3

VDPU_SWREG32

Address: Operational Base + offset (0x00080)

Reference picture numbers for index 4 and 5 (H264 VLC)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	sw_refer5_nbr Number for reference picture index 5
15:0	RW	0x0000	sw_refer4_nbr Number for reference picture index 4

VDPU_SWREG32_VP8

Address: Operational Base + offset (0x00080)

Reference picture numbers for index 4 and 5 (H264 VLC)

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23:18	RW	0x00	sw_filt_level_0 filter level value for reference frame type 0
17:12	RW	0x00	sw_filt_level_1 filter level value for reference frame type 1
11:6	RW	0x00	sw_filt_level_2 filter level value for reference frame type 2
5:0	RW	0x00	sw_filt_level_3 filter level value for reference frame type 3

VDPU_SWREG33

Address: Operational Base + offset (0x00084)

Reference picture numbers for index 6 and 7 (H264 VLC)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	sw_refer7_nbr Number for reference picture index 7
15:0	RW	0x0000	sw_refer6_nbr Number for reference picture index 6

VDPU_SWREG33_VP8

Address: Operational Base + offset (0x00084)

Reference picture numbers for index 6 and 7 (H264 VLC)

Bit	Attr	Reset Value	Description
31:27	RW	0x00	sw_quant_delta_0 quantisizer delta 0 0
26:22	RW	0x00	sw_quant_delta_1 quantisizer delta 1 0

Bit	Attr	Reset Value	Description
21:11	RW	0x000	sw_quant_0 quantisizer value for LUT (7 bit)
10:0	RW	0x000	sw_quant_1 quantisizer value for LUT (7 bit)

VDPU_SWREG34

Address: Operational Base + offset (0x00088)

Reference picture numbers for index 8 and 9 (H264 VLC)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	sw_refer9_nbr Number for reference picture index 9
15:0	RW	0x0000	sw_refer8_nbr Number for reference picture index 8

VDPU_SWREG34_VP8

Address: Operational Base + offset (0x00088)

Reference picture numbers for index 8 and 9 (H264 VLC)

Bit	Attr	Reset Value	Description
31:22	RW	0x000	sw_pred_bc_tap_0_3 Field0000 Abstract Prediction filter set 0, tap 3
21:12	RW	0x000	sw_pred_bc_tap_1_0 Prediction filter set 1, tap 0
11:2	RW	0x000	sw_pred_bc_tap_1_1 Prediction filter set 1, tap 1
1:0	RO	0x0	reserved

VDPU_SWREG35_JPEG_ROI

Address: Operational Base + offset (0x0008c)

JPEG roi offest/dc base address

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	sw_jpegdcoff_base JPEG roi offest/dc base address JPEG roi offest/dc base address
1:0	RO	0x0	reserved

VDPU_SWREG35

Address: Operational Base + offset (0x0008c)

Reference picture numbers for index 10 and 11 (H264 VLC)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	sw_refer11_nbr Number for reference picture index 11
15:0	RW	0x0000	sw_refer10_nbr Number for reference picture index 10

VDPU_SWREG35_VP8

Address: Operational Base + offset (0x0008c)

Reference picture numbers for index 10 and 11 (H264 VLC)

Bit	Attr	Reset Value	Description
31:22	RW	0x000	sw_pred_bc_tap_1_2 precision filter set 1, tap 2
21:12	RW	0x000	sw_pred_bc_tap_1_3 precision filter set 1, tap 3
11:2	RW	0x000	sw_pred_bc_tap_2_0 precision filter set 2, tap 0
1:0	RO	0x0	reserved

VDPU_SWREG36

Address: Operational Base + offset (0x00090)

Reference picture numbers for index 12 and 13 (H264 VLC)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	sw_refer13_nbr Number for reference picture index 13
15:0	RW	0x0000	sw_refer12_nbr Number for reference picture index 12

VDPU_SWREG36_JPEG_ROI

Address: Operational Base + offset (0x00090)

JPEG roi offset/dc length

Bit	Attr	Reset Value	Description
31:17	RO	0x0	reserved
16:0	RW	0x00000	sw_jpegdcoff_len sw_jpegdcoff_len The number of 64bit jpegdcoff, it can be used both when sw_roi_decode is 1'b0 or 1'b1

VDPU_SWREG36_VP8

Address: Operational Base + offset (0x00090)

Reference picture numbers for index 12 and 13 (H264 VLC)

Bit	Attr	Reset Value	Description
31:22	RW	0x000	sw_pred_bc_tap_2_1 precision filter set 2, tap 1
21:12	RW	0x000	sw_pred_bc_tap_2_2 precision filter set 2, tap 2
11:2	RW	0x000	sw_pred_bc_tap_2_3 precision filter set 2, tap 3
1:0	RO	0x0	reserved

VDPU_SWREG37_VP8

Address: Operational Base + offset (0x00094)

Reference picture numbers for index 12 and 13 (H264 VLC)

Bit	Attr	Reset Value	Description
31:22	RW	0x000	sw_pred_bc_tap_3_2 prediction filter set 3, tap 2
21:12	RW	0x000	sw_pred_bc_tap_3_1 prediction filter set 3, tap 1
11:2	RW	0x000	sw_pred_bc_tap_3_0 prediction filter set 3, tap 0
1:0	RO	0x0	reserved

VDPU_SWREG37

Address: Operational Base + offset (0x00094)

Reference picture numbers for index 14 and 15 (H264 VLC)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	sw_refer15_nbr Number for reference picture index 15
15:0	RW	0x0000	sw_refer14_nbr Number for reference picture index 14

VDPU_SWREG38

Address: Operational Base + offset (0x00098)

Reference picture long term flags (H264 VLC) / VPx prediction filt

Bit	Attr	Reset Value	Description
31:22	RW	0x000	sw_pred_bc_tap_3_3 Prediction filter set 3, tap 3
21:12	RW	0x000	sw_pred_bc_tap_4_0 Prediction filter set 4, tap 0
11:2	RW	0x000	sw_perd_bc_tap_4_1 Prediction filter set 4, tap 1
1:0	RO	0x0	reserved

VDPU_SWREG38_H264

Address: Operational Base + offset (0x00098)

Reference picture numbers for index 12 and 13 (H264 VLC)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_refer_lterm_e long term flag for reference picture index [31:0]

VDPU_SWREG39

Address: Operational Base + offset (0x0009c)

Reference picture valid flags (H264 VLC) / VPx prediction filter ta

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:22	RW	0x000	sw_pred_bc_tap_4_2 Prediction filter set 4, tap 2
21:12	RW	0x000	sw_pred_bc_tap_4_3 Prediction filter set 4, tap 3
11:2	RW	0x000	sw_pred_bc_tap_5_0 Prediction filter set 5, tap 0
1:0	RO	0x0	reserved

VDPU_SWREG39_H264

Address: Operational Base + offset (0x0009c)

Reference picture numbers for index 12 and 13 (H264 VLC)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_refer_valid_e valid flag for reference picture index [31:0]

VDPU_SWREG40

Address: Operational Base + offset (0x000a0)

Base address for standard dependent tables

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	sw_qtable_base Base address for standard dependent tables: JPEG= AC,DC, QP tables MPEG4=QP table base address if type 1 quantization is used MPEG2=QP table base address H.264=base address for various tables VP7,VP8=base address for stream decoding tables [note]:the h264 and vp8 decoder will use these bits.
1:0	RO	0x0	reserved

VDPU_SWREG41

Address: Operational Base + offset (0x000a4)

Base address for direct mode motion vectors

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	sw_dir_mv_base Direct mode motion vector write/read base address. For H264 this is used only for direct mode motion vector write base. Progressive JPEG: ACDC coefficient read/write base address. If current round is for DC components this base address is pointing to luminance (separate base addresses for chrominances), for AC component rounds this base is used for current type
1:0	RO	0x0	reserved

VDPU_SWREG42_VP8

Address: Operational Base + offset (0x000a8)

Bit	Attr	Reset Value	Description
31:22	RW	0x000	sw_pred_bc_tap_5_1 prediction filter set 5, tap 1
21:12	RW	0x000	sw_pred_bc_tap_5_2 prediction filter set 5, tap 2
11:2	RW	0x000	sw_pred_bc_tap_5_3 prediction filter set 5, tap 3
1:0	RO	0x0	reserved

VDPU_SWREG42

Address: Operational Base + offset (0x000a8)

bi_dir initial ref pic list register (0-2)/

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:25	RW	0x00	sw_binit_rlist_b2 Initial reference picture list for bi- direct backward picid 2
24:20	RW	0x00	sw_binit_rlist_f2 Initial reference picture list for bi- direct forward picid 2
19:15	RW	0x00	sw_binit_rlist_b1 Initial reference picture list for bi- direct backward picid 1
14:10	RW	0x00	sw_binit_rlist_f1 Initial reference picture list for bi- direct forward picid 1
9:5	RW	0x00	sw_binit_rlist_b0 Initial reference picture list for bi- direct backward picid 0

Bit	Attr	Reset Value	Description
4:0	RW	0x00	sw_binit_rlist_f0 Initial reference picture list for bi- direct forward picid 0

VDPU_SWREG43_VP8

Address: Operational Base + offset (0x000ac)

Bit	Attr	Reset Value	Description
31:22	RW	0x000	sw_pred_bc_tap_6_0 prediction filter set 6, tap 0
21:12	RW	0x000	sw_pred_bc_tap_6_1 prediction filter set 6, tap 1
11:2	RW	0x000	sw_pred_bc_tap_6_2 prediction filter set 6, tap 2
1:0	RO	0x0	reserved

VDPU_SWREG43

Address: Operational Base + offset (0x000ac)

bi-dir initial ref pic list register (3-5)/

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:25	RW	0x00	sw_binit_rlist_b5 Initial reference picture list for bi- direct backward picid 5
24:20	RW	0x00	sw_binit_rlist_f5 Initial reference picture list for bi- direct forward picid 5
19:15	RW	0x00	sw_binit_rlist_b4 Initial reference picture list for bi- direct backward picid 4
14:10	RW	0x00	sw_binit_rlist_f4 Initial reference picture list for bi- direct forward picid 4
9:5	RW	0x00	sw_binit_rlist_b3 Initial reference picture list for bi- direct backward picid 3
4:0	RW	0x00	sw_binit_rlist_f3 Initial reference picture list for bi- direct forward picid 3

VDPU_SWREG44_VP8

Address: Operational Base + offset (0x000b0)

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:22	RW	0x000	sw_pred_bc_tap_6_3 prediction filter set 6, tap 3
21:12	RW	0x000	sw_pred_bc_tap_7_0 prediction filter set 7, tap 0
11:2	RW	0x000	sw_pred_bc_tap_7_1 prediction filter set 7, tap 1
1:0	RO	0x0	reserved

VDPU_SWREG44

Address: Operational Base + offset (0x000b0)

bi-dir initial ref pic list register (6-8)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:25	RW	0x00	sw_binit_rlist_b8 Initial reference picture list for bi- direct backward picid 8
24:20	RW	0x00	sw_binit_rlist_f8 Initial reference picture list for bi- direct forward picid 8
19:15	RW	0x00	sw_binit_rlist_b7 Initial reference picture list for bi- direct backward picid 7
14:10	RW	0x00	sw_binit_rlist_f7 Initial reference picture list for bi- direct forward picid 7
9:5	RW	0x00	sw_binit_rlist_b6 Initial reference picture list for bi- direct backward picid 6
4:0	RW	0x00	sw_binit_rlist_f6 Initial reference picture list for bi- direct forward picid 6

VDPU_SWREG45_VP8

Address: Operational Base + offset (0x000b4)

Bit	Attr	Reset Value	Description
31:22	RW	0x000	sw_pred_bc_tap_7_2 prediction filter set 7, tap 2
21:12	RW	0x000	sw_pred_bc_tap_7_3 prediction filter set 7, tap 3
11:10	RW	0x0	sw_pred_tap_2_m1 additional Prediction filter tap -1 for set 2

Bit	Attr	Reset Value	Description
9:8	RW	0x0	sw_pred_tap_2_4 Field0000 Abstract additional Prediction filter tap 4 for set 2
7:6	RW	0x0	sw_pred_tap_4_m1 additional Prediction filter tap -1 for set 4
5:4	RW	0x0	sw_pred_tap_4_4 Field0000 Abstract additional Prediction filter tap 4 for set 4
3:2	RW	0x0	sw_pred_tap_6_m1 additional Prediction filter tap -1 for set 6
1:0	RW	0x0	sw_pred_tap_6_4 Field0000 Abstract additional Prediction filter tap 4 for set 6

VDPU_SWREG45

Address: Operational Base + offset (0x000b4)

bi-dir initial ref pic list register (9- 11)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:25	RW	0x00	sw_binit_rlist_b11 Initial reference picture list for bi- direct backward picid 11
24:20	RW	0x00	sw_binit_rlist_f11 Initial reference picture list for bi- direct forward picid 11
19:15	RW	0x00	sw_binit_rlist_b10 Initial reference picture list for bi- direct backward picid 10
14:10	RW	0x00	sw_binit_rlist_f10 Initial reference picture list for bi- direct forward picid 10
9:5	RW	0x00	sw_binit_rlist_b9 Initial reference picture list for bi- direct backward picid 9
4:0	RW	0x00	sw_binit_rlist_f9 Initial reference picture list for bi- direct forward picid 9

VDPU_SWREG46

Address: Operational Base + offset (0x000b8)

bi-dir initial ref pic list register (12- 14) / VP7,VP8 quantization v

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved

Bit	Attr	Reset Value	Description
29:25	RW	0x00	sw_binit_rlist_b14 Initial reference picture list for bi- direct backward picid 14
24:20	RW	0x00	sw_binit_rlist_f14 Initial reference picture list for bi- direct forward picid 14
19:15	RW	0x00	sw_binit_rlist_b13 Initial reference picture list for bi- direct backward picid 13
14:10	RW	0x00	sw_binit_rlist_f13 Initial reference picture list for bi- direct forward picid 13
9:5	RW	0x00	sw_binit_rlist_b12 Initial reference picture list for bi- direct backward picid 12
4:0	RW	0x00	sw_binit_rlist_f12 Initial reference picture list for bi- direct forward picid 12

VDPU_SWREG46_VP8

Address: Operational Base + offset (0x000b8)

bi-dir initial ref pic list register (12- 14) / VP7,VP8 quantization v

Bit	Attr	Reset Value	Description
31:27	RW	0x00	sw_quant_delta_2 quantisizer delta 2
26:22	RW	0x00	sw_quant_delta_3 quantisizer delta 3
21:11	RW	0x000	sw_quant_2 quantisizer value for LUT (7 bit)
10:0	RW	0x000	sw_quant_3 quantisizer value for LUT (7 bit)

VDPU_SWREG47

Address: Operational Base + offset (0x000bc)

bi-dir and P fwd initial ref pic list register (15 and P 0-3) / VP7,V

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:25	RW	0x00	sw_pinit_rlist_f3 Initial reference picture list for P forward picid 3
24:20	RW	0x00	sw_pinit_rlist_f2 Initial reference picture list for P forward picid 2

Bit	Attr	Reset Value	Description
19:15	RW	0x00	sw_pinit_rlist_f1 Initial reference picture list for P forward picid 1
14:10	RW	0x00	sw_pinit_rlist_f0 Initial reference picture list for P forward picid 0
9:5	RW	0x00	sw_binit_rlist_b15 Initial reference picture list for bi- direct backward picid 15
4:0	RW	0x00	sw_binit_rlist_f15 Initial reference picture list for bi- direct forward picid 15

VDPU_SWREG47_VP8

Address: Operational Base + offset (0x000bc)
 bi-dir and P fwd initial ref pic list register (15 and P 0-3) / VP7,V

Bit	Attr	Reset Value	Description
31:27	RW	0x00	sw_quant_delta_4 quantisizer delta 4
26:0	RO	0x0	reserved

VDPU_SWREG48

Address: Operational Base + offset (0x000c0)
 Error concealment register

Bit	Attr	Reset Value	Description
31:23	RW	0x000	sw_startmb_x Start MB from SW for X dimension. Used in error concealment case [note]:the h264 and vp8 decoder will use these bits.
22:15	RW	0x00	sw_startmb_y Start MB from SW for Y dimension. Used in error concealment case [note]:the h264 and vp8 decoder will use these bits.
14:0	RO	0x0	reserved

VDPU_SWREG49

Address: Operational Base + offset (0x000c4)
 Prediction filter tap register for H264, MPEG4, VC1

Bit	Attr	Reset Value	Description
31:22	RW	0x000	sw_pred_bc_tap_0_0 Prediction filter set 0, tap 0 [note]:the h264 decoder will use these bits.

Bit	Attr	Reset Value	Description
21:12	RW	0x000	sw_pred_bc_tap_0_1 Prediction filter set 0, tap 1 [note]:the h264 decoder will use these bits.
11:2	RW	0x000	sw_pred_bc_tap_0_2 Prediction filter set 0, tap 2 [note]:the h264 decoder will use these bits.
1:0	RO	0x0	reserved

VDPU_SWREG50

Address: Operational Base + offset (0x000c8)

Synthesis configuration register decoder 0 (read only)

Bit	Attr	Reset Value	Description
31	RO	0x1	SW_DEC_MPEG2_PROF Decoding format support, MPEG-2 / MPEG-1 '0' = not supported '1' = supported
30:29	RO	0x3	SW_DEC_VC1_PROF Decoding format support, VC-1 0 = not supported 1 = supported up to simple profile 2 = supported up to main profile 3 = supported up to advanced profile
28	RO	0x1	SW_DEC_JPEG_PROF Decoding format support, JPEG 0 = not supported 1 = supported
27:26	RO	0x2	SW_DEC_MPEG4_PROF Decoding format support, MPEG-4 / H.263 0 = not supported 1 = supported up to simple profile 2 = supported up to advanced simple profile
25:24	RO	0x3	SW_DEC_H264_PROF Decoding format support, H.264 0 = not supported 1 = supported up to baseline profile 2 = supported up to high profile labeled stream with restricted high profile tools [note]:the h264 decoder will use these bits.
23	RO	0x1	Reserved
22	RO	0x0	SW_DEC_PJEPAGE_EXIT Progressive JPEG support: '0' = Not supported '1' = supported

Bit	Attr	Reset Value	Description
21	RO	0x1	SW_DEC_OBUFF_LEVEL Decoder output buffer level: '0' = 1 MB buffering is used '1' = 4 MB buffering is used [note]:the h264 and vp8 decoder will use these bits.
20	RO	0x1	SW_REF_BUFF_EXIST [note]:the h264 and vp8 decoder will use these bits.
19:16	RO	0x5	SW_DEC_BUS_STRD [note]:the h264 and vp8 decoder will use these bits.
15:14	RO	0x1	SW_DEC_SYNTH_LAN [note]:the h264 and vp8 decoder will use these bits.
13:12	RO	0x2	SW_DEC_BUS_WIDTH 0 = error 1 = 32 bit bus 2 = 64 bit bus 3 = 128 bit bus [note]:the h264 and vp8 decoder will use these bits.
11	RO	0x1	SW_DEC_SOREN_PRO Decoding format support, Sorenson '0' = not supported '1' = supported
10:0	RO	0x780	SW_DEC_MAX_OWIDTH Max configured decoder video resolution that can be decoded. Informed as width of the picture in pixels [note]:the h264 and vp8 decoder will use these bits.

VDPU_SWREG51

Address: Operational Base + offset (0x000cc)

Reference picture buffer control register

Bit	Attr	Reset Value	Description
31	RW	0x0	sw_refbu_e Refer picture buffer enable: '0' = refer picture buffer disabled '1' = refer picture buffer enabled. Valid if picture size is QVGA or more [note]:the h264 and vp8 decoder will use these bits.

Bit	Attr	Reset Value	Description
30:19	RW	0x000	sw_refbu_thr Reference buffer disable threshold value (cache miss amount). Used to buffer shut down (if more misses than allowed) [note]:the h264 and vp8 decoder will use these bits.
18:14	RW	0x00	sw_refbu_picid The used reference picture ID for reference buffer usage [note]:the h264 and vp8 decoder will use these bits.
13	RW	0x0	sw_refbu_eval_e Enable for HW internal reference ID calculation. If given threshold level is reached by any picture_id after first MB row, that picture_id is used for reference buffer fill for rest of the picture [note]:the h264 and vp8 decoder will use these bits.
12	RW	0x0	sw_refbu_fparmod_e Field parity mode enable. Used in rebufferd evaluation mode '0' = use the result field of the evaluation '1' = use the parity mode field [note]:the h264 and vp8 decoder will use these bits.
11:9	RO	0x0	reserved
8:0	RW	0x000	sw_refbu_y_offset Y offset for rebufferd. This coordinate is used to compensate the global motion of the video for better buffer hit rate [note]:the h264 and vp8 decoder will use these bits.

VDPU_SWREG52

Address: Operational Base + offset (0x000d0)

Reference picture buffer information register 1 (read only)

Bit	Attr	Reset Value	Description
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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	sw_refbu_hit_sum The sum of the refbufferd hits of the picture. Determined for each 8x8 luminance partition of the picture. The proceeding of the HW calculation can be read during HW decoding [note]:the h264 and vp8 decoder will use these bits.
15:0	RW	0x0000	sw_refbu_intra_sum The sum of the luminance 8x8 intra partitons of the picture. The proceeding of the HW calculation can be read during HW decoding [note]:the h264 and vp8 decoder will use these bits.

VDPU_SWREG53

Address: Operational Base + offset (0x000d4)

Reference picture buffer information register 2 (read only)

Bit	Attr	Reset Value	Description
31:22	RO	0x0	reserved
21:0	RW	0x000000	sw_refbu_y_mv_sum The sum of the decoded motion vector y-components of the picture. The first luminance motion vector of each MB is used in calculation. Other motion vectors of the MB are discarded. Each motion vector is saturated between -256 - 255 before calculation. The proceeding of the HW calculation can be read during HW decoding [note]:the h264 and vp8 decoder will use these bits.

VDPU_SWREG54

Address: Operational Base + offset (0x000d8)

Synthesis configuration register decoder 1 (read only)

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31	RO	0x1	SW_DEC_JPEG_EXTENS JPEG sampling support extension for 411 and 444 samplings and support for bigger max resolution than 16 Mpix (up to 67Mpixels): '0' = not supported '1' = supported
30	RO	0x1	SW_DEC_REFBU_ILACE Refbufferd support for interlaced content: '0' = not supported '1' = supported [note]:the h264 decoder will use these bits.
29	RO	0x1	Reserved
28	RO	0x0	SW_REF_BUFF2_EXIST Reference picture buffer 2 usage: '0' = not supported '1' = reference buffer 2 is used [note]:the h264 and vp8 decoder will use these bits.
27:26	RO	0x1	SW_DEC_RV_PROF Decoding format support, RV 0 = not supported 1 = supported up to 2 = NA
25	RO	0x0	SW_DECRTL_ROM ROM implementation type (If design includes ROMs) '0': ROMs are implemented from actual ROM units '1': ROMs are impelemted from RTL
24	RO	0x1	SW_DEC_VP7_PROF Decoding format support, VP7 0 = not supported 1 = supported
23	RO	0x1	SW_DEC_VP8_PROF Decoding format support, VP8 0 = not supported 1 = supported [note]:the vp8 decoder will use these bits.
22	RO	0x1	SW_DEC_AVSPROF Decoding format support, AVS 0 = not supported 1 = supported

Bit	Attr	Reset Value	Description
21:20	RO	0x1	SW_DEC_MVC_PROF Decoding format support, MVC 0 = not supported 1 = supported
19	RO	0x1	SW_DEC_VP8SNAP_E Decoding format support, VP8 snapshot 0 = not supported bigger than 1080p resolution 1 = supported upto 16kx16k pixel resolution (defined max) [note]:the vp8 decoder will use these bits.
18:17	RO	0x1	SW_DEC_TILED_L Tiled mode support level 0 = not supported 1 = supported with 8x4 tile size 2,3 = reserved [note]:the h264 and vp8 decoder will use these bits.
16:0	RO	0x0	reserved

VDPU_SWREG55

Address: Operational Base + offset (0x000dc)

Reference picture buffer 2 / Advanced prefetch control register

Bit	Attr	Reset Value	Description
31	RW	0x0	sw_refbu2_buf_e Refer picture buffer 2 enable: '0' = refer picture buffer disabled '1' = refer picture buffer enabled. Valid if picture size is QVGA or more (can be turned off by HW if threshold value reached) [note]:the h264 and vp8 decoder will use these bits.
30:19	RW	0x000	sw_refbu2_thr Reference buffer disable threshold value (buffer miss amount). Used to buffer shut down (if more misses than allowed) [note]:the h264 and vp8 decoder will use these bits.

Bit	Attr	Reset Value	Description
18:14	RW	0x00	sw_refbu2_picid The used reference picture ID for reference buffer usage [note]:the h264 and vp8 decoder will use these bits.
13:0	RW	0x0000	sw_apf_threshold Advanced prefetch threshold value. If current MB exceeds the threshold the advanced mode is not used. Value 0 disables threshold usage and advanced prefetch usage is restricted by internal memory limitation only [note]:the h264 and vp8 decoder will use these bits.

VDPU_SWREG56

Address: Operational Base + offset (0x000e0)
Reference buffer information register 3 (read only)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	sw_refbu_top_sum The sum of the top partitions of the picture [note]:the h264 and vp8 decoder will use these bits.
15:0	RW	0x0000	sw_refbu_bot_sum The sum of the bottom partitions of the picture [note]:the h264 and vp8 decoder will use these bits.

VDPU_SWREG57_INTRA_INTER

Address: Operational Base + offset (0x000e4)
intra_dll3t,intra_dblspeed,inter_dblspeed,stream_len_hi

Bit	Attr	Reset Value	Description
31:15	RO	0x0	reserved
14:8	RO	0x00	debug_service debug_service signals service_wr[2:0], service_rd[3:0]
7	RW	0x0	sw_cache_en cache enable 1'b1: cache enable 1'b0: cache disable when sw_cache_en is 1'b1, sw_pref_sigchan should also be 1'b1

Bit	Attr	Reset Value	Description
6	RW	0x0	sw_pref_sigchan prefetch single channel enable 1'b1: prefetch single channel enable
5	RW	0x0	sw_axiwr_sel axi write master select 1'b0: auto sel encoder axi signals and decoder axi signals 1'b1: sel decoder axi signals (it only use to set bu_dec_e to 1'b0 in the middle of a frame)
4	RW	0x0	sw_paral_bus paral_bus enable when it is set to 1'b1, the axi support read and write service parallel; when it is set to 1'b0, the axi only support read and write serial
3	RW	0x0	sw_intra_dbl3t sw_intra_dbl3t In chroma dc intra prediction, when this bit is enable, there will 3 cycle enhance for every block
2	RW	0x0	sw_intra_dblspeed intra double speed enable Intra double speed enable
1	RW	0x0	sw_inter_dblspeed inter double speed enable Inter double speed enable
0	RW	0x0	sw_stream_len_hi stream length high bit The extension bit of sw_stream_len

VDPU_SWREG57

Address: Operational Base + offset (0x000e4)

intra_dbl3t,intra_dblspeed,inter_dblspeed,stream_len_hi

Bit	Attr	Reset Value	Description
31	RW	0x0	fuse_dec_h264 1 = H.264 enabled
30	RW	0x0	fuse_dec_mpeg4 1= MPEG-4/H.263 enabled
29	RW	0x0	fuse_dec_mpeg2 1 = MPEG-2/MPEG-1 enabled N
28	RW	0x0	fuse_dec_sorenson 1= sorenson enabled (requires also MPEG4 to be enabled) NA 1 R
27	RW	0x0	fuse_dec_jpeg Field0000 Abstract 1= JPEG enabled

Bit	Attr	Reset Value	Description
26	RW	0x0	Reserved
25	RW	0x0	fuse_dec_vc1 1 = VC1 enabled
24	RW	0x0	fuse_dec_pjpeg 1 = Progressive JPEG enabled (Requires also JPEG to be enabled)
23	RW	0x0	Reserved
22	RW	0x0	Reserved
21	RW	0x0	fuse_dec_vp7 1= VP7 enabled
20	RW	0x0	fuse_dec_vp8 1= VP8 enabled
19	RW	0x0	fuse_dec_avs 1 = AVS eanbled
18	RW	0x0	fuse_dec_mvc enabled (requires also H264 to be enabled)
17:16	RO	0x0	reserved
15	RW	0x0	fuse_dec_maxw_1920 1 = Max video width up to 1920 pixels enabled. Priority coded with priority 1.
14	RW	0x0	fuse_dec_maxw_1280 1 = Max video width up to 1280 pixels enabled. Priority coded with priority 2.
13	RW	0x0	fuse_dec_maxw_720 1 = Max video width up to 720 pixels enabled. Priority coded with priority 3.
12	RW	0x0	fuse_dec_maxw_352 1 = Max video width up to 352 pixels enabled. Priority coded with priority 4
11:8	RO	0x0	reserved
7	RW	0x0	fuse_dec_refbuffer 1 = reference buffer used
6:0	RO	0x0	reserved

VDPU_SWREG58

Address: Operational Base + offset (0x000e8)

Decoder debug register 0 (read only)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved

Bit	Attr	Reset Value	Description
30	RO	0x0	debug_mv_req mvst_mv_req signal value
29	RO	0x0	debug_rlc_req prtr_res_y_req signal value
28	RO	0x0	debug_res_y_req prtr_res_y_req signal value
27	RO	0x0	debug_res_c_req prtr_res_c_req signal value
26	RO	0x0	debug_strm_da_e strm_da_e signal value
25	RO	0x0	debug_framerdy dfbu_framerdy signal value
24	RO	0x0	debug_filter_req dfbu_req_e signal value
23	RO	0x0	debug_referreq0 prbu_referreq0 signal value
22	RO	0x0	debug_referreq1 prbu_referreq1 signal value
21	RO	0x0	reserved
20:0	RO	0x000000	debug_dec_mb_count HW internal MB counter value

VDPU_SWREG59

Address: Operational Base + offset (0x000ec)
H264 Chrominance 8 pixel interleaved data base

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	sw_dec_ch8pix_base Base address for additional chrominance data format where chrominance is interleaved in group of 8 pixels. The usage is enabled by sw_ch_8pix_ilav_e [note]:the h264 decoder will use these bits.
1:0	RO	0x0	reserved

VDPU_SWREG60

Address: Operational Base + offset (0x000f0)
Interrupt register post-processor

Bit	Attr	Reset Value	Description
31:14	RO	0x0	reserved
13	RW	0x0	sw_pp_bus_int Interrupt status bit bus. Error response from bus. In pipeline mode this bit is not used

Bit	Attr	Reset Value	Description
12	RW	0x0	sw_pp_rdy_int Interrupt status bit pp. When this bit is high post processor has processed a picture in external mode. In pipeline mode this bit is not used.
11:9	RO	0x0	reserved
8	RW	0x0	sw_pp_irq Post-processor IRQ. SW will reset this after interrupt is handled. HINTpp is not used for pp if IRQ disable pp is high (sw_pp_irq_n_e = 1). In pipeline mode this bit is not used
7:5	RO	0x0	reserved
4	RW	0x0	sw_pp_irq_dis Post-processor IRQ disable. When high, there are no interrupts from HW concerning post processing. Polling must be used to see the interrupt
3:2	RO	0x0	reserved
1	RW	0x0	sw_pp_pipeline_e Decoder –post-processing pipeline enable: 0 = Post-processing is processing different picture than decoder or is disabled 1 = Post-processing is performed in pipeline with decoder
0	RW	0x0	sw_pp_e External mode post-processing enable. This bit will start the post-processing operation. Not to be used if PP is in pipeline with decoder (sw_pp_pipeline_e = 1). HW will reset this when picture is post-processed.

VDPU_SWREG61

Address: Operational Base + offset (0x000f4)

Device configuration register post-processor

Bit	Attr	Reset Value	Description
31:24	RW	0x01	sw_pp_axi_rd_id Read ID used for AXI PP read services (if connected to AXI)
23:16	RW	0x01	sw_pp_axi_wr_id Write ID used for AXI PP write services (if connected to AXI)
15	RO	0x0	reserved
14	RW	0x0	sw_pp_scmd_dis AXI Single Command Multiple Data disable.

Bit	Attr	Reset Value	Description
13	RW	0x0	sw_pp_in_a2_endsel Endian/swap select for Alpha blend input source 2: '0' = Use PP in endian/swap definitions (sw_pp_in_endian, sw_pp_in_swap) '1' = Use Ablend source 1 endian/swap definitions
12	RW	0x0	sw_pp_in_a1_swap32 Alpha blend source 1 input 32bit data swap (may be used for 64 bit environment): 0 = no swapping of 32 bit words 1 = 32 bit data words are swapped (needed in 64 bit environment to achieve 7-6-5-4-3-2-1-0 byte order(also little endian should be enabled))
11	RW	0x0	sw_pp_in_a1_endian Alpha blend source 1 input data byte endian mode. 0 = Big endian (0-1-2-3 order) 1 = Little endian (3-2-1-0 order)
10	RW	0x0	sw_pp_in_swap32_e PP input 32bit data swap (may be used for 64 bit environment): 0 = no swapping of 32 bit words 1 = 32 bit data words are swapped (needed in 64 bit environment to achieve 7-6-5-4-3-2-1-0 byte order(also little endian should be enabled))
9	RW	0x0	sw_pp_data_disc_e PP data discard enable. Precise burst lengths are used with reading services. Extra data is discarded internally.
8	RW	0x1	sw_pp_clkgate_e PP dynamic clock gating enable: 1 = Clock is gated from PP structures that are not used 0 = Clock is running for all PP structures Note: Clock gating value can be changed only when PP is not enabled

Bit	Attr	Reset Value	Description
7	RW	0x0	<p>sw_pp_in_endian PP input picture byte endian mode. Used only if PP is in standalone mode. If PP is running pipelined with the decoder, this bit has no effect.</p> <p>0 = Big endian (0-1-2-3 order) 1 = Little endian (3-2-1-0 order)</p>
6	RW	0x0	<p>sw_pp_out_endian PP output picture endian mode for YCbCr data or for any data if config value SW_PP_OEN_VERSION=1</p> <p>0 = Big endian (0-1-2-3 order) 1 = Little endian (3-2-1-0 order)</p> <p>(NOTE: For SW_PP_OEN_VERSION=0 16 bit RGB data this bit works as pixel swapping bit. For 32 bit RGB this bit has no meaning)</p>
5	RW	0x0	<p>sw_pp_out_swap32_e PP output data word swap (may be used for 64 bit environment):</p> <p>0 = no swapping of 32 bit words 1 = 32 bit data words are swapped (needed in 64 bit environment to achieve 7-6-5-4-3-2-1-0 byte order (also little endian should be enabled))</p>
4:0	RW	0x00	<p>sw_pp_max_burst Maximum burst length for PP bus transactions. 1-16</p>

VDPU_SWREG62

Address: Operational Base + offset (0x000f8)

Deinterlace control register

Bit	Attr	Reset Value	Description
31	RW	0x0	<p>sw_deint_e De-interlace enable. Input data is in interlaced format and deinterlacing needs to be performed</p>
30	RO	0x0	reserved
29:16	RW	0x0000	<p>sw_deint_threshold Threshold value used in deinterlacing</p>
15	RW	0x0	<p>sw_deint_blend_e Blend enable for de-interlacing</p>
14:0	RW	0x0000	<p>sw_deint_edge_det Edge detect value used for deinterlacing</p>

VDPU_SWREG63

Address: Operational Base + offset (0x000fc)

base address for reading post-processing input picture luminance

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	sw_pp_in_lu_base Base address for post-processing input luminance picture. If PP input picture is fetched from fields this base address is used to point to topfield of the picture. Used in external mode only.
1:0	RO	0x0	reserved

VDPU_SWREG64

Address: Operational Base + offset (0x00100)

Base address for reading post-processing input picture Cb/Cb

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	sw_pp_in_cb_base Base address for post-processing input Cb picture or for both chrominance pictures (if chrominances interleaved). If PP input picture is fetched from fields this base address is used to point to topfield of the picture. Used in external mode only
1:0	RO	0x0	reserved

VDPU_SWREG65

Address: Operational Base + offset (0x00104)

Base address for reading post-processing input picture Cr

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	sw_pp_in_cr_base Base address for post-processing input cr picture. Used in external mode only
1:0	RO	0x0	reserved

VDPU_SWREG66

Address: Operational Base + offset (0x00108)

Base address for writing post-processed picture luminance/RGB

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_pp_out_lu_base Base address for post-processing output picture (luminance/YUYV/RGB).

VDPU_SWREG67

Address: Operational Base + offset (0x0010c)

Base address for writing post-processed picture Ch

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_pp_out_ch_base Base address for post-processing output chrominance picture (interleaved chrominance).

VDPU_SWREG68

Address: Operational Base + offset (0x00110)

Register for contrast adjusting

Bit	Attr	Reset Value	Description
31:24	RW	0x00	sw_contrast_thr1 Threshold value 1, used with contrast adjusting
23:20	RO	0x0	reserved
19:10	RW	0x000	sw_contrast_off2 Offset value 2, used with contrast adjusting
9:0	RW	0x000	sw_contrast_off1 Offset value 1, used with contrast adjusting

VDPU_SWREG69

Address: Operational Base + offset (0x00114)

Register for colour conversion and contrast adjusting

Bit	Attr	Reset Value	Description
31	RW	0x0	sw_pp_in_start_ch For YUYV 422 input format. Enable for start_with_chrominance. '0' =the order is Y0CbY0Cr or Y0CrY0Cb '1'= the order is CbY0CrY0 or CrY0CbY0
30	RW	0x0	sw_pp_in_cr_first For YUYV 422 input format and YCbCr 420 semiplanar format. Enable for Cr first (before Cb) '0' =the order is Y0CbY0Cr or CbY0CrY0 (if 420 semiplanar chrominance: CbCrCbCr) '1'= the order is Y0CrY0Cb or CrY0CbY0 (if 420 semiplanar chrominance: CrCbCrCb)
29	RW	0x0	sw_pp_out_start_ch For YUYV 422 output format. Enable for start_with_chrominance. '0' =the order is Y0CbY0Cr or Y0CrY0Cb '1'= the order is CbY0CrY0 or CrY0CbY0
28	RW	0x0	sw_pp_out_cr_first For YUYV 422 output format. Enable for Cr first (beforeCb) '0' =the order is Y0CbY0Cr or CbY0CrY0 '1'= the order is Y0CrY0Cb or CrY0CbY0

Bit	Attr	Reset Value	Description
27:18	RW	0x000	sw_color_coeffa2 Coefficient a2, used with Y pixel to calculate all color components
17:8	RW	0x000	sw_color_coeffa1 Coefficient a1, used with Y pixel to calculate all color components
7:0	RW	0x00	sw_contrast_thr2 Threshold value 2, used with contrast adjusting

VDPU_SWREG70

Address: Operational Base + offset (0x00118)

Register for colour conversion 0

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x000	sw_color_coeffd Coefficient d, used with Cb to calculate green component value
19:10	RW	0x000	sw_color_coeffc Coefficient c, used with Cr to calculate green component value
9:0	RW	0x000	sw_color_coeffb Coefficient b, used with Cr to calculate red component value

VDPU_SWREG71

Address: Operational Base + offset (0x0011c)

Register for colour conversion 1 + rotation mode

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:21	RW	0x000	sw_crop_startx Start coordinate x for the cropped area in macroblocks.
20:18	RW	0x0	sw_rotation_mode Rotation mode: 000 = rotation disabled 001 = rotate + 90 010 = rotate -90 011 = horizontal flip (mirror) 100 = vertical flip 101 = rotate 180
17:10	RW	0x00	sw_color_coefff Coefficient f, used with Y to adjust brightness

Bit	Attr	Reset Value	Description
9:0	RW	0x000	sw_color_coeffe Coefficient e, used with Cb to calculate blue component value

VDPU_SWREG72

Address: Operational Base + offset (0x00120)

PP input size and -cropping register

Bit	Attr	Reset Value	Description
31:24	RW	0x00	sw_crop_starty Start coordinate y for the cropped area in macroblocks.
23	RO	0x0	reserved
22:18	RW	0x00	sw_rangemap_coef_y Range map value for Y component (RANGE_MAPY+9 in VC-1 standard)
17	RO	0x0	reserved
16:9	RW	0x00	sw_pp_in_height PP input picture height in MBs. Can be cropped from a bigger input picture in external mode
8:0	RW	0x000	sw_pp_in_width PP input picture width in MBs. Can be cropped from a bigger input picture in external mode

VDPU_SWREG73

Address: Operational Base + offset (0x00124)

PP input picture base address for Y bottom field

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	sw_pp_bot_yin_base PP input Y base for bottom field
1:0	RO	0x0	reserved

VDPU_SWREG74

Address: Operational Base + offset (0x00128)

PP input picture base for Ch bottom field

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	sw_pp_bot_cin_base PP input C base for bottom field (mixed chrominance)
1:0	RO	0x0	reserved

VDPU_SWREG79

Address: Operational Base + offset (0x0013c)

Scaling ratio register 1 & padding for B

Bit	Attr	Reset Value	Description
31	RW	0x0	sw_rangemap_y_e Range map enable for Y component (RANGE_MAPY_FLAG in VC-1 standard). For VC1 main profile this bit is used as range expansion enable
30	RW	0x0	sw_rangemap_c_e Range map enable for chrominance component RANGE_MAPUV_FLAG in VC-1 standard)
29	RW	0x0	sw_ycbcr_range Defines the YCbCr range in RGB conversion: 0 = 16-255 for Y, 16-240 for Chrominance 1 = 0-255 for all components
28	RW	0x0	sw_rgb_pix_in32 RGB pixel amount/ 32 bit word 0 = 1 RGB pixel/32 bit 1 = 2 RGB pixels/32 bit
27:23	RW	0x00	sw_rgb_r_padd Amount of ones that will be padded in front of the R- component
22:18	RW	0x00	sw_rgb_g_padd Amount of ones that will be padded in front of the G- component
17:0	RW	0x00000	sw_scale_wratio Scaling ratio for width (outputw-1/inputw-1)

VDPU_SWREG80

Address: Operational Base + offset (0x00140)

Scaling register 0 ratio & padding for R and G

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30	RW	0x0	sw_pp_fast_scale_e 0 = fast downscaling is not enabled 1 = fast downscaling is enabled. The quality of the picture is decreased but performance is improved

Bit	Attr	Reset Value	Description
29:27	RW	0x0	<p>sw_pp_in_struct PP input data picture structure: 0 = Top field / progressive frame structure: Read input data from top field base address /frame base address and read every line 1 = Bottom field structure: Read input data from bottom field base address and read every line. 2 = Interlaced field structure: Read input data from both top and bottom field base address and take every line from each field. 3 = Interlaced frame structure: Read input data from both top and bottom field base address and take every second line from each field. 4 = Ripped top field structure: Read input data from top field base address and read every second line. 5 = Ripped bottom field structure: Read input data from bottom field base address and read every second line</p>
26:25	RW	0x0	<p>sw_hor_scale_mode Horizontal scaling mode: 00 = Off 01 = Upscale 10 = Downscale</p>
24:23	RW	0x0	<p>sw_ver_scale_mode Vertical scaling mode: 00 = Off 01 = Upscale 10 = Downscale</p>
22:18	RW	0x00	<p>sw_rgb_b_padd Amount of ones that will be padded in front of the B- component</p>
17:0	RW	0x00000	<p>sw_scale_hratio Scaling ratio for height (outputh-1/inputh-1)</p>

VDPU_SWREG81

Address: Operational Base + offset (0x00144)

Scaling ratio register 2

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	sw_wscale_invra Inverse scaling ratio for width, or ch (inputw-1 / outputw-1)
15:0	RW	0x0000	sw_hscale_invra Inverse scaling ratio for height or cv (inpush-1 / outputh-1)

VDPU_SWREG82

Address: Operational Base + offset (0x00148)

Rmask register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_r_mask Bit mask for R component (and alpha channel)

VDPU_SWREG83

Address: Operational Base + offset (0x0014c)

Gmask register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_g_mask Bit mask for G component (and alpha channel)

VDPU_SWREG84

Address: Operational Base + offset (0x00150)

Bmask register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_b_mask Bit mask for B component (and alpha channel)

VDPU_SWREG85

Address: Operational Base + offset (0x00154)

Post-processor control register

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:29	RW	0x0	<p>sw_pp_in_format PP input picture data format</p> <ul style="list-style-type: none"> 0 = YUYV 4:2:2 interleaved (supported only in external mode) 1 = YCbCr 4:2:0 Semi-planar in linear raster-scan format 2 = YCbCr 4:2:0 planar (supported only in external mode) 3 = YCbCr 4:0:0 (supported only in pipelined mode) 4 = YCbCr 4:2:2 Semi-planar (supported only in pipelined mode) 5 = YCbCr 4:2:0 Semi-planar in tiled format (supported only in external mode (8170 decoder only)) 6 = YCbCr 4:4:0 Semi-planar (supported only in pipelined mode, possible for jpeg only) 7 = Escape pp input data format. Defined in swreg86
28:26	RW	0x0	<p>sw_pp_out_format PP output picture data format:</p> <ul style="list-style-type: none"> 0 = RGB 1 = YCbCr 4:2:0 planar (Not supported) 2 = YCbCr 4:2:2 planar (Not supported) 3 = YUYV 4:2:2 interleaved 4 = YCbCr 4:4:4 planar (Not supported) 5 = YCh 4:2:0 chrominance interleaved 6 = YCh 4:2:2 (Not supported) 7 = YCh 4:4:4 (Not supported)
25:15	RW	0x000	<p>sw_pp_out_height Scaled picture height in pixels (Must be dividable by 2 or by any if Pixel Accurate PP output configuration is enabled)</p> <p>Max scaled picture height is 1920 pixels or maximum three times the input source height minus 8 pixels</p>
14:4	RW	0x000	<p>sw_pp_out_width Scaled picture width in pixels. Must be dividable by 8 or by any if Pixel Accurate PP output configuration is enabled.</p> <p>Max scaled picture width is 1920 pixels or maximum three times the input source width minus 8 pixels</p>

Bit	Attr	Reset Value	Description
3	RW	0x0	sw_pp_out_tiled_e Tiled mode enable for PP output. Can be used only for YCbYCr 422 output format. Can be used only if correpongind configuration supports this feature. Tile size is 4x4 pixels.
2	RW	0x0	sw_pp_out_swap16_e PP output swap 16 swaps 16 bit halfs inside of 32 bit word. Can be used for 16 bit RGB to change pixel orders but is valid also for any output format NOTE: requires that configuration of SW_PPD_OEN_VERSION=1
1	RW	0x0	sw_pp_crop8_r_e PP input picture width is not 16 pixels multiple. Only 8 pixels of the most right MB of the unrotated input picture is used for PP input.
0	RW	0x0	sw_pp_crop8_d_e PP input picture height is not 16 pixels multiple. Only 8 pixel rows of the most down MB of the unrotated input picture is used for PP input.

VDPU_SWREG86

Address: Operational Base + offset (0x00158)

Mask 1 start coordinate register

Bit	Attr	Reset Value	Description
31:29	RW	0x0	sw_pp_in_format_es Escape PP in format. Used if sw_pp_in_format is defined to 7: 0 0 = YCbCr 4:4:4 1 = YCbCr 4:1:1
28	RO	0x0	reserved
27:23	RW	0x00	sw_rangemap_coef_c Range map value for chrominance component (RANGE_MAPUV+9 in VC-1 standard)

Bit	Attr	Reset Value	Description
22	RW	0x0	sw_mask1_ablend_e Mask 1 alpha blending enable. Instead of masking the output picture the alpha blending is performed. Alpha blending source can be found from alpha blend 1 base address. Alpha blending can be enabled only for RGB/ YUYV 422 data.
21:11	RW	0x000	sw_mask1_starty Vertical start pixel for mask area 1. Defines the y coordinate. Coordinate 0,0 means the up-left corner in PP output luminance picture. See Table 47 for restrictions
10:0	RW	0x000	sw_mask1_startix Horizontal start pixel for mask area 1. Defines the x coordinate. Coordinate 0,0 means the up-left corner in PP output luminance picture. See Table 47 for restrictions

VDPU_SWREG87

Address: Operational Base + offset (0x0015c)

Mask 2 start coordinate register

Bit	Attr	Reset Value	Description
31:23	RO	0x0	reserved
22	RW	0x0	sw_mask2_ablend_e Mask 2 alpha blending enable. Instead of masking the output picture the alpha blending is performed. Alpha blending source can be found from alpha blend 2 base address. Alpha blending can be enabled only for RGB/YUYV 422 data.
21:11	RW	0x000	sw_mask_starty Vertical start pixel for mask area 2. Defines the y coordinate. Coordinate 0,0 means the up-left corner in PP output Y picture. See Table 47 for restrictions
10:0	RW	0x000	sw_mask2_startx Horizontal start pixel for mask area 2. Defines the x coordinate. Coordinate 0,0 means the up-left corner in PP output Y picture. See Table 47 for restrictions

VDPU_SWREG88

Address: Operational Base + offset (0x00160)

Mask 1 size and PP original width register

Bit	Attr	Reset Value	Description
31:23	RW	0x000	sw_ext_orig_width PP input picture original width in macro blocks.
22	RW	0x0	sw_mask1_e Mask 1 enable. If mask 1 is used this bit is high
21:11	RW	0x000	sw_mask1_endy Mask 1 end coordinate y in pixels (inside of PPD output picture). Range must be between [Mask1StartCoordinateY, ScaledHeight].
10:0	RW	0x000	sw_mask1_endx Mask 1 end coordinate x in pixels (inside of PPD output picture). Range must be between [Mask1StartCoordinateX, ScaledWidth]

VDPU_SWREG89

Address: Operational Base + offset (0x00164)

Mask 2 size register

Bit	Attr	Reset Value	Description
31:23	RO	0x0	reserved
22	RW	0x0	sw_mask2_e Mask 2 enable. If mask 1 is used this bit is high
21:11	RW	0x000	sw_mask2_endy Mask 2 end coordinate y in pixels (inside of PP output picture). Range must be between [Mask2StartCoordinateY, ScaledHeight].
10:0	RW	0x000	sw_mask2_endx Mask 2 end coordinate x in pixels (inside of PP output picture). Range must be between [Mask2StartCoordinateX, ScaledWidth].

VDPU_SWREG90

Address: Operational Base + offset (0x00168)

PiP register 0

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved

Bit	Attr	Reset Value	Description
29	RW	0x0	sw_right_cross_e Right side overcross enable. 0 = No right side overcross, 1 =right side overcross
28	RW	0x0	sw_left_cross_e Left side overcross enable. 0 = No left side overcross, 1 = left side overcross
27	RW	0x0	sw_up_cross_e Upward overcross enable. 0 = No upward overcross, 1 = upward overcross
26	RW	0x0	sw_down_cross_e Downward overcross enable. 0 = No downward overcross, 1 = downward overcross
25:15	RW	0x000	sw_up_cross Amount of upward overcross (vertical pixels outside of display from the upper side). Range must be between [0, ScaledHeight].
14:11	RO	0x0	reserved
10:0	RW	0x000	sw_down_cross Amount of downward overcross (vertical pixels outside of displayfrom the down side). Range must be between [0, ScaledHeight].

VDPU_SWREG91

Address: Operational Base + offset (0x0016c)

PiP register 1 and dithering control

Bit	Attr	Reset Value	Description
31:30	RW	0x0	sw_dither_select_r Dithering control for R channel: 00 = dithering disabled 01 = use four-bit dither matrix 10 = use five-bit dither matrix 11 = use six-bit dither matrix
29:28	RW	0x0	sw_dither_select_g Dithering control for G channel: 00 = dithering disabled 01 = use four-bit dither matrix 10 = use five-bit dither matrix 11 = use six-bit dither matrix

Bit	Attr	Reset Value	Description
27:26	RW	0x0	sw_dither_select_b Dithering control for B channel: 00 = dithering disabled 01 = use four-bit dither matrix 10 = use five-bit dither matrix 11 = use six-bit dither matrix
25:24	RO	0x0	reserved
23:22	RW	0x0	sw_pp_tiled_mode Input data is in tiled mode (at the moment valid only for YCbCr 420 data, pipeline or external mode): 0 = Tiled mode not used 1 = Tiled mode enabled for 8x4 sized tiles 2,3 = reserved
21:11	RW	0x000	sw_right_cross Amount of right side overcross (Horizontal pixels outside of display from the right side). Range must be between [0, ScaledWidth].
10:0	RW	0x000	sw_left_cross Amount of left side overcross (Horizontal pixels outside of display from the left side). Range must be between [0, ScaledWidth].

VDPU_SWREG92

Address: Operational Base + offset (0x00170)

Display width and PP input size extension register

Bit	Attr	Reset Value	Description
31:29	RW	0x0	sw_pp_in_h_ext Extended PP input height. Used with JPEG
28:26	RW	0x0	sw_pp_in_w_ext Extended PP input width. Used with JPEG
25:23	RW	0x0	sw_crop_starty_ext Extended PP input crop start coordinate x. Used with JPEG
22:20	RW	0x0	sw_crop_start_ext Extended PP input crop start coordinate y. Used with JPEG
19:12	RO	0x0	reserved
11:0	RW	0x000	sw_display_width Width of the display in pixels. Max HDTV (1920)

VDPU_SWREG93

Address: Operational Base + offset (0x00174)
 Display width and PP input size extension register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_abledn1_base Base address for alpha blending input 1 (if mask1 is used in alpha blending mode). Format of data is 24 bit RGB/ YCbCr and endian/swap -mode is as in PP input. Amount of data is informed with mask 1 size or with ablend1_scanline if ablend cropping is supported in configuration.

VDPU_SWREG94

Address: Operational Base + offset (0x00178)
 Base address for alpha blend 2 gui component

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_ablend2_base Base address for alpha blending input 2 (if mask2 is used in alpha blending mode). Format of data is 24 bit RGB/ YCbCr and endian/swap -mode is as in PP input. Amount of data is informed with mask 2 size or with ablend2_scanline if ablend cropping is supported in configuration.

VDPU_SWREG95

Address: Operational Base + offset (0x0017c)
 Base address for alpha blend 2 gui component

Bit	Attr	Reset Value	Description
31:26	RO	0x0	reserved
25:13	RW	0x0000	sw_ablend2_scan Scanline width in pixels for Ablend 2. Usage enabled if corresponding configuration bit is enabled
12:0	RW	0x0000	sw_ablend1_scan Scanline width in pixels for Ablend 1. Usage enabled if corresponding configuration bit is enabled

VDPU_SWREG98

Address: Operational Base + offset (0x00188)

PP output width/height extension

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	RW	0x0	sw_pp_out_h_ext sw_pp_out_h_ext PP output heightextension
0	RW	0x0	sw_pp_out_w_ext sw_pp_out_w_ext PP output widthextension

VDPU_SWREG99

Address: Operational Base + offset (0x0018c)

PP fuse register (read only)

Bit	Attr	Reset Value	Description
31	RO	0x1	fuse_pp_pp 1 = PP enabled
30	RO	0x1	fuse_pp_deint 1 = Deinterlacing enabled
29	RO	0x1	fuse_pp_ablend 1 = Alpha Blending enabled
28:16	RO	0x0	reserved
15	RO	0x1	fuse_pp_maxw_1920 1 = Max PP output width up to 1920 pixels enabled. Priority coded with priority 1
14	RO	0x1	fuse_pp_maxw_1280 1 = Max PP output width up to 1280 pixels enabled. Priority coded with priority 2
13	RO	0x1	fuse_pp_maxw_720 1 = Max PP output width up to 720 pixels enabled. Priority coded with priority 3
12	RO	0x1	fuse_pp_maxw_352 1 = Max PP output width up to 352 pixels enabled. Priority coded with priority 4
11:0	RO	0x0	reserved

VDPU_SWREG100

Address: Operational Base + offset (0x00190)

Synthesis configuration register post-processor (read only)

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31	RO	0x1	SW_ABLEND_CROP_E Alpha blending support for input cropping: '0': Not supported. External memory must include the exact image of the area being alpha blended '1' Supported. External memory can include a picture from blended area can be cropped. Requires usage of swreg95
30	RO	0x1	SW_PPD_PIXAC_E Pixel Accurate PP output mode exists: '0'= PIP, Scaling and masks can be adjusted by steps of 8 pixels (width) or 2 pixels (height) '1' = PIP, Scaling and masks can be adjusted by steps of 1 pixel for RGB and 2 pixels for subsampled chroma formats (by using bus specific write strobe functionality)
29	RO	0x1	SW_PPD_TILED_EXIST PP output YCbYCr 422 tiled support (4x4 pixel tiles) '0'=Not supported '1'=Supported
28	RO	0x1	SW_PPD_DITH_EXIST Dithering exists: '0' = no '1' = yes
27:26	RO	0x3	SW_PPD_SCALE_LEVEL Scaling support: 00 = No scaling 01 = Scaling with lo perfomance architecture 10 = Scaling with high performance architecture 11 = Scaling with high performance architecture + fast
25	RO	0x1	SW_PPD_DEINT_EXIST De-interlacing exists: '0' = no '1' = yes
24	RO	0x1	SW_PPD_BLEND_EXIST Alpha blending exists: '0' = no '1' = yes

Bit	Attr	Reset Value	Description
23	RO	0x1	SW_PPD_IBUFF_LEVEL PP input buffering level: '0' = 1 MB input buffering is used '1' = 4 MB input buffering is used
22:19	RO	0x0	reserved
18	RO	0x1	SW_PPD_OEN_VERSION PP output endian version: '0' = Endian mode supported for other than RGB '1' = Endian mode supported for any output format
17	RO	0x1	SW_PPD_OBUFF_LEVEL PP output buffering level: '0' = 1 unit output buffering is used '1' = 4 unit output buffering is used
16	RO	0x1	SW_PPD_PP_EXIST PPD exists: '0'=no '1'=yes
15:14	RO	0x1	SW_PPD_IN_TILED_L PPD input tiled mode support level 0 = not supported 1 = 8x4 tile size supported
13:11	RO	0x0	reserved
10:0	RO	0x780	SW_PPD_MAX_OWIDTH Max supported PP output width in pixels

VDPU_SWREG101

Address: Operational Base + offset (0x00194)

soft reset signals

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	sw_soft_reset softreset pulse signal softreset pulse signal write to 1'b1, valid; write to 1'b0, invalid;

VDPU_SWREG102

Address: Operational Base + offset (0x00198)

vpu performance cycle

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	vpu_work_cycle vpu working cycle number write initial/reset value in the begin of frame start,then will auto count base this value.

VDPU_SWREG103

Address: Operational Base + offset (0x0019c)

AXI DDR READ DATA NUM

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_axi_ddr_rdata axi ddr rdata num axi ddr rdata num, the unit is byte

VDPU_SWREG104

Address: Operational Base + offset (0x001a0)

Register0000 Abstract

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	sw_axi_ddr_wdata vdpu write data byte num vdpu write data byte num

VDPU_SWREG105

Address: Operational Base + offset (0x001a4)

Bit	Attr	Reset Value	Description
31:20	RO	0x0	reserved
19:16	RW	0x0	mon_sig_sel1 monitor signal selected for cnt1 select the counter be used for which to calculate cycle num 4'b0000: don't work 4'b0001:mv buffer hold back stream decode working cycles 4'b0010:the output fifo of cabac keep full cycles 4'b0011:the Code stream parsing block working cycles 4'b0100:scd block can't write data to scd buffer cycles 4'b0101:The speed of reconsititution and interpolation fast than reference frames feach cycles 4'b0110:The speed of reconsititution and interpolation slow than reference frames feach cycles 4'b0111:the cycles filter block hold back pred block 4'b1000:the cycles of pred block waiting for Residual data 4'b1001:the cycles of bus Related modules working
15:4	RO	0x0	reserved

Bit	Attr	Reset Value	Description
3:0	RW	0x0	<p>mon_sig_sel0 monitor signal selected for cnt0 select the counter be used for which to calculate cycle num 4'b0000: don't work 4'b0001:mv buffer hold back stream decode working cycles 4'b0010:the output fifo of cabac keep full cycles 4'b0011:the Code stream parsing block working cycles 4'b0100:scd block can't write data to scd buffer cycles 4'b0101:The speed of reconsituton and interpolation fast than reference frames feach cycles 4'b0110:The speed of reconsituton and interpolation slow than reference frames feach cycles 4'b0111:the cycles filter block hold back pred block 4'b1000:the cycles of pred block waiting for Residual data 4'b1001:the cycles of bus Related modules working</p>

VDPU_SWREG106

Address: Operational Base + offset (0x001a8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	<p>performance_mon_cnt0 the counter for the seected signal valid cycles whic describe in swreg105[3:0] write initial/reset value</p>

VDPU_SWREG107

Address: Operational Base + offset (0x001ac)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	<p>performance_mon_cnt1 Field0000 Abstract the counter for the seected signal valid cycles whic describe in swreg105[19:16] write initial/reset value</p>

16.4.11 VPU MMU Register Summary

Name	Offset	Size	Reset Value	Description
VCODEC_MMU_DTE_ADDR	0x00000	W	0x00000000	MMU current page Table address
VCODEC_MMU_STATUS	0x00004	W	0x00000000	MMU status register
VCODEC_MMU_COMMAND	0x00008	W	0x00000000	MMU command register

Name	Offset	Size	Reset Value	Description
V_CODEC_MMU_PAGE_FAULT_ADDR	0x0000c	W	0x00000000	MMU logical address of last page fault
V_CODEC_MMU_ZAP_ONE_LINE	0x00010	W	0x00000000	MMU Zap cache line register
V_CODEC_MMU_INT_RAWSTAT	0x00014	W	0x00000000	MMU raw interrupt status register
V_CODEC_MMU_INT_CLEAR	0x00018	W	0x00000000	MMU raw interrupt status register
V_CODEC_MMU_INT_MASK	0x0001c	W	0x00000000	MMU raw interrupt status register
V_CODEC_MMU_INT_STATUS	0x00020	W	0x00000000	MMU raw interrupt status register
V_CODEC_MMU_AUTO_GATING	0x00024	W	0x00000001	mmu auto gating

Notes:Size: **B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access

16.4.12 VPU MMU Detail Register Description

V_CODEC_MMU_DTE_ADDR

Address: Operational Base + offset (0x00000)

MMU current page Table address

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	MMU_DTE_ADDR MMU_DTE_ADDR MMU current page Table address

V_CODEC_MMU_STATUS

Address: Operational Base + offset (0x00004)

MMU status register

Bit	Attr	Reset Value	Description
31:11	RO	0x0	reserved
10:6	RO	0x00	PAGEFAULT_BUS_ID page fault bus id Index of master responsible for last page fault
5	RO	0x0	PAGEFAULT_IS_WRITE page fault access The direction of access for last page fault: 0 = Read 1 = Write
4	RO	0x1	REPLAY_BUFFER_EMPTY replay buffer empty status 1'b1:The MMU replay buffer is empty

Bit	Attr	Reset Value	Description
3	RO	0x1	MMU_IDLE mmu idle status The MMU is idle when accesses are being translated and there are no unfinished translated accesses. 1'b1: MMU is idle
2	RO	0x0	STAIL_ACTIVE stall active status MMU stall mode currently enabled. The mode is enabled by command 1'b1: MMU is in stall active status
1	RO	0x0	PAGE_FAULT_ACTIVE page fault active status MMU page fault mode currently enabled . The mode is enabled by command. 1'b1: page fault is active
0	RO	0x0	PAGING_ENABLED Paging enabled status 1'b0: paging is disabled 1'b1: Paging is enabled

VCODEC_MMU_COMMAND

Address: Operational Base + offset (0x00008)

MMU command register

Bit	Attr	Reset Value	Description
31:3	RO	0x0	reserved
2:0	WO	0x0	MMU_CMD mmu cmd MMU_CMD. This can be: 0: MMU_ENABLE_PAGING 1: MMU_DISABLE_PAGING 2: MMU_ENABLE_STALL 3: MMU_DISABLE_STALL 4: MMU_ZAP_CACHE 5: MMU_PAGE_FAULT_DONE 6: MMU_FORCE_RESET

VCODEC_MMU_PAGE_FAULT_ADDR

Address: Operational Base + offset (0x0000c)

MMU logical address of last page fault

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	PAGE_FAULT_ADDR page fault addr address of last page fault

VCODEC_MMU_ZAP_ONE_LINE

Address: Operational Base + offset (0x00010)

MMU Zap cache line register

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	MMU_ZAP_ONE_LINE zap one line address to be invalidated from the page table cache

VCODEC_MMU_INT_RAWSTAT

Address: Operational Base + offset (0x00014)

MMU raw interrupt status register

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	RW	0x0	READ_BUS_ERROR read bus error read bus error status
0	RW	0x0	PAGE_FAULT page fault page fault status

VCODEC_MMU_INT_CLEAR

Address: Operational Base + offset (0x00018)

MMU raw interrupt status register

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	WO	0x0	READ_BUS_ERROR read bus error write 1 to clear read bus error
0	WO	0x0	PAGE_FAULT page fault clear write 1 to page fault clear

VCODEC_MMU_INT_MASK

Address: Operational Base + offset (0x0001c)

MMU raw interrupt status register

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	RW	0x0	READ_BUS_ERROR read bus error enable the read bus interrupt source when this bit is set to 1'b1

Bit	Attr	Reset Value	Description
0	RW	0x0	PAGE_FAULT page fault mask enable the page fault interrupt source when this bit is set to 1'b1

VCODEC_MMU_INT_STATUS

Address: Operational Base + offset (0x00020)

MMU raw interrupt status register

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	RO	0x0	READ_BUS_ERROR read bus error status 1'b1: read bus error
0	RO	0x0	PAGE_FAULT page fault status 1'b1:page fault

VCODEC_MMU_AUTO_GATING

Address: Operational Base + offset (0x00024)

mmu auto gating

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x1	mmu_auto_clkgating mmu_auto_clkgating when it is 1'b1, the mmu will auto gating it self

16.4.13 VDPU Pref_cacheRegister Summary

Name	Offset	Size	Reset Value	Description
pref_cache_VERSION	0x00000	W	0xcac20101	VERSION register
pref_cache_SIZE	0x00004	W	0x06170206	L2 cache SIZE
pref_cache_STATUS	0x00008	W	0x00000000	Status register
pref_cache_COMMAND	0x00010	W	0x00000000	Command setting register
pref_cache_CLEAR_PAGE	0x00014	W	0x00000000	clear page register
pref_cache_MAX_READS	0x00018	W	0x0000001c	maximum read register
pref_cache_PERFCNT_SRC0	0x00020	W	0x00000000	performance counter 0 source register
pref_cache_PERFCNT_VAL0	0x00024	W	0x00000000	performance counter 0 value register
pref_cache_PERFCNT_SRC1	0x00028	W	0x00000000	performance counter 0 source register
pref_cache_PERFCNT_VAL1	0x0002c	W	0x00000000	performance counter 1 value register

Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access

16.4.14 VDPU_Pref_cache Detail Register Description

pref_cache_VERSION

Address: Operational Base + offset (0x00000)

VERSION register

Bit	Attr	Reset Value	Description
31:16	RO	0xcac2	PRODUCT_ID Field0000 Abstract Field0000 Description
15:8	RO	0x01	VERSION_MAJOR Field0000 Abstract Field0000 Description
7:0	RO	0x01	VERSION_MINOR Field0000 Abstract Field0000 Description

pref_cache_SIZE

Address: Operational Base + offset (0x00004)

L2 cache SIZE

Bit	Attr	Reset Value	Description
31:24	RO	0x06	External_bus_width Field0000 Abstract Log2 external bus width in bits
23:16	RO	0x17	CACHE_SIZE Field0000 Abstract Log2 cache size in bytes
15:8	RO	0x02	ASSOCIATIVITY Field0000 Abstract Log2 associativity
7:0	RO	0x06	LINE_SIZE Field0000 Abstract Log2 line size in bytes

pref_cache_STATUS

Address: Operational Base + offset (0x00008)

Status register

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	RW	0x0	DATA_BUSY Field0000 Abstract set when the cache is busy handling data
0	RW	0x0	CMD_BUSY Field0000 Abstract set when the cache is busy handling commands

pref_cache_COMMAND

Address: Operational Base + offset (0x00010)

Command setting register

Bit	Attr	Reset Value	Description
31:6	RO	0x0	reserved
5:4	RW	0x0	sw_addrb_sel Field0000 Abstract 2'b00: to sel b[14:6] 2'b01: to sel b[15:9], b[7:6] 2'b10: to sel b[16:10], b[7:6] 2'b11: to sel b[17:11], b[7:6]
3	RO	0x0	reserved
2:0	RW	0x0	COMMAND Field0000 Abstract The possible command is 1 = Clear entire cache

pref_cache_CLEAR_PAGE

Address: Operational Base + offset (0x00014)

clear page register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	CLEAR_PAGE Field0000 Abstract writing an address, invalidates all lines in that page from the cache

pref_cache_MAX_READS

Address: Operational Base + offset (0x00018)

maximum read register

Bit	Attr	Reset Value	Description
31:5	RO	0x0	reserved
4:0	RW	0x1c	MAX_READS Field0000 Abstract Limit the number of outstanding read transactions to this amount

pref_cache_PERFCNT_SRC0

Address: Operational Base + offset (0x00020)

performance counter 0 source register

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved

Bit	Attr	Reset Value	Description
3:0	RW	0x0	PERFCNT_SRC0 Field0000 Abstract This register holds all the possible source values for Performance Counter 0 0: total clock cycles 1: active clock cycles 2: read transactions, master 3: word reads, master 4: read transactions, slave 5: word reads, slave 6: read hit, slave 7: read misses, slave 8: read invalidates, slave 9: cacheable read transactions, slave 10: bad hit nmber, slave

pref_cache_PERFCNT_VAL0

Address: Operational Base + offset (0x000024)
 performance counter 0 value register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PERFCNT_VAL0 Field0000 Abstract Performance counter 0 value

pref_cache_PERFCNT_SRC1

Address: Operational Base + offset (0x000028)
 performance counter 0 source register

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved
3:0	RW	0x0	PERFCNT_SRC1 Field0000 Abstract This register holds all the possible source values for Performance Counter 1 0: total clock cycles 1: active clock cycles 2: read transactions, master 3: word reads, master 4: read transactions, slave 5: word reads, slave 6: read hit, slave 7: read misses, slave 8: read invalidates, slave 9: cacheable read transactions, slave 10: bad hit nmber, slave

pref_cache_PERFCNT_VAL1

Address: Operational Base + offset (0x0002c)
 performance counter 1 value register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PERFCNT_VAL1 Field0000 Abstract Performance counter 1 value

16.5 Application Notes

16.5.1 HEVC Configuration flow

1. Prepare the data in the DDR.
2. Set the HEVC general system configuration in HEVC.swreg2, such as working mode, in/out endian.
3. Set the picture parameters with HEVC.swreg3.
4. Set the input and output data base address and HEVC reference configuration with HEVC.swreg4~HEVC.swreg43.
5. If CABAC error detection is desired, set the HEVC.swreg44 to enable the corresponding error detection.
6. Set the interrupt configuration and start the HEVC with HEVC.swreg1.
7. Wait for the frame interrupt, and then get the processed results in the target DDR
8. Clear all the interrupts, and repeat Process2~Process8 to start a new frame decoding if the decoding is not finished yet.

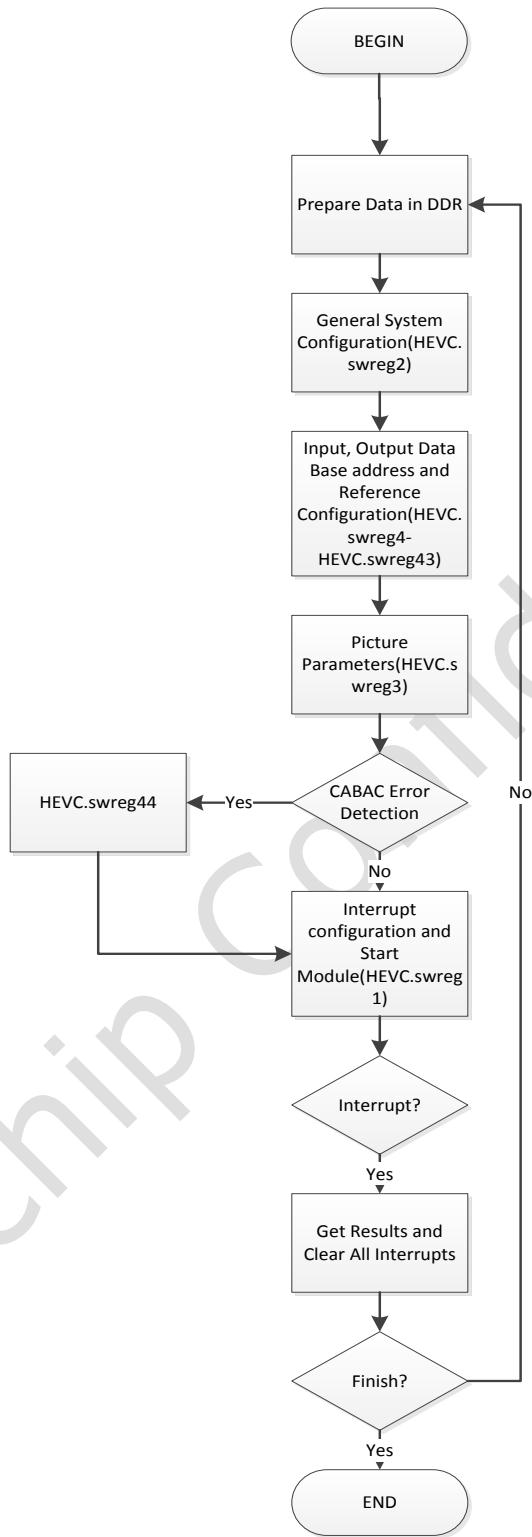


Fig. 16-6 HEVC Common Configuration Flow

16.5.2 VPU Configuration flow

1. Prepare the decoder data in the DDR memory, And in decoder other than JPEG decoder, the input stream buffer should at least contain a slice or a frame data, otherwise the decoder will produce an interrupt and show error and then reset itself.
2. Config all the registers will be used. and please notice that which be list as follows:

- In encoder---- We can configure the registers to control the input picture data format (such as endian and swap), but some input data format are fixed, such as cabac_table data. And the register VEPU_SWREG64~95 are JPEG quantization registers. They are write only registers. When you want to write these registers, you should first set VEPU_SWREG14[0] to 1'b0 and VEPU_SWREG14[2:1] to 2'b10(select JPEG mode).
 - In decoder---- The decoder can support ref buffer mode or cacheable mode, but they can't be both enabled. We can config the swreg57[6],swreg57[7] to enable cache and config the swreg51 to control the ref buffer.
3. You should config VDPU_SWREG1[0] as 1'b1 to enable video decoder. And config VDPU_SWREG60[0] as 1'b1 to enable pp. If pp performed in pipeline with decoder, you should config VDPU_SWREG60[1] as 1'b1 and then config VDPU_SWREG1[0] as 1'b1 to enable decoder and pp. VEPU_SWREG14[0] set to 1'b1 to enable encoder.
 4. Wait for the frame interrupt, and then check if the frame decoder ready interrupt is right or not, after that, you can get the processed results in the target DDR
 5. Clear all the interrupts, repeat step 2~5 to start a new frame decoder or encoder.

Chapter 17 Image Enhancement Processor (IEP)

17.1 Overview

The Image Enhancement Processor (IEP) receives data from and transmits data to system main memory by AXI bus, or output the data to LCD controller directly.

The features of IEP are as follow:

Image format

- Input data: XRGB/RGB565/YUV420/YUV422
- Output data: ARGB/RGB565/YUV420/YUV422
- ARGB/XRGB/RGB565/YUV swap
- YUV semi-planar/planar
- BT601_I/BT601_f/BT709_I/BT709_f color space conversion
- RGB dither up/down conversion
- YUV up/down sampling conversion
- Max source image resolution: 8192x8192
- Max scaled image resolution: 4096x4096

Enhancement

- Gamma adjustment with programmable mapping table
- Hue/Saturation/Brightness/Contrast enhancement
- Color enhancement with programmable coefficient
- Detail enhancement with filter matrix up to 9x9
- Edge enhancement with filter matrix up to 9x9
- Programmable difference table for detail enhancement
- Programmable distance table for detail and edge enhancement

Noise reduction

- Compression noise reduction with filter matrix up to 9x9
- Programmable difference table for compression noise reduction
- Programmable distance table for compression noise reduction
- Spatial sampling noise reduction
- Temporal sampling noise reduction
- Optional coefficient for sampling noise reduction

High quality scaling

- Horizontal down-scaling with vertical down-scaling
- Horizontal down-scaling with vertical up-scaling
- Horizontal up-scaling with vertical down-scaling
- Horizontal up-scaling with vertical up-scaling
- Arbitrary non-integer scaling ratio, from 1/16 to 16

De-interlace

- Input 4 fields, output 2 frames mode
- Input 4 fields, output 1 frames mode
- Input 2 fields, output 1 frames mode
- Programmable motion detection coefficient
- Programmable high frequency factor
- Programmable edge interpolation parameter
- Source width up to 1920

Interface

- Programmable direct path to VOP

- 32bit AHB bus slave
- 64bit AXI bus master
- Combined interrupt output

17.2 Block Diagram

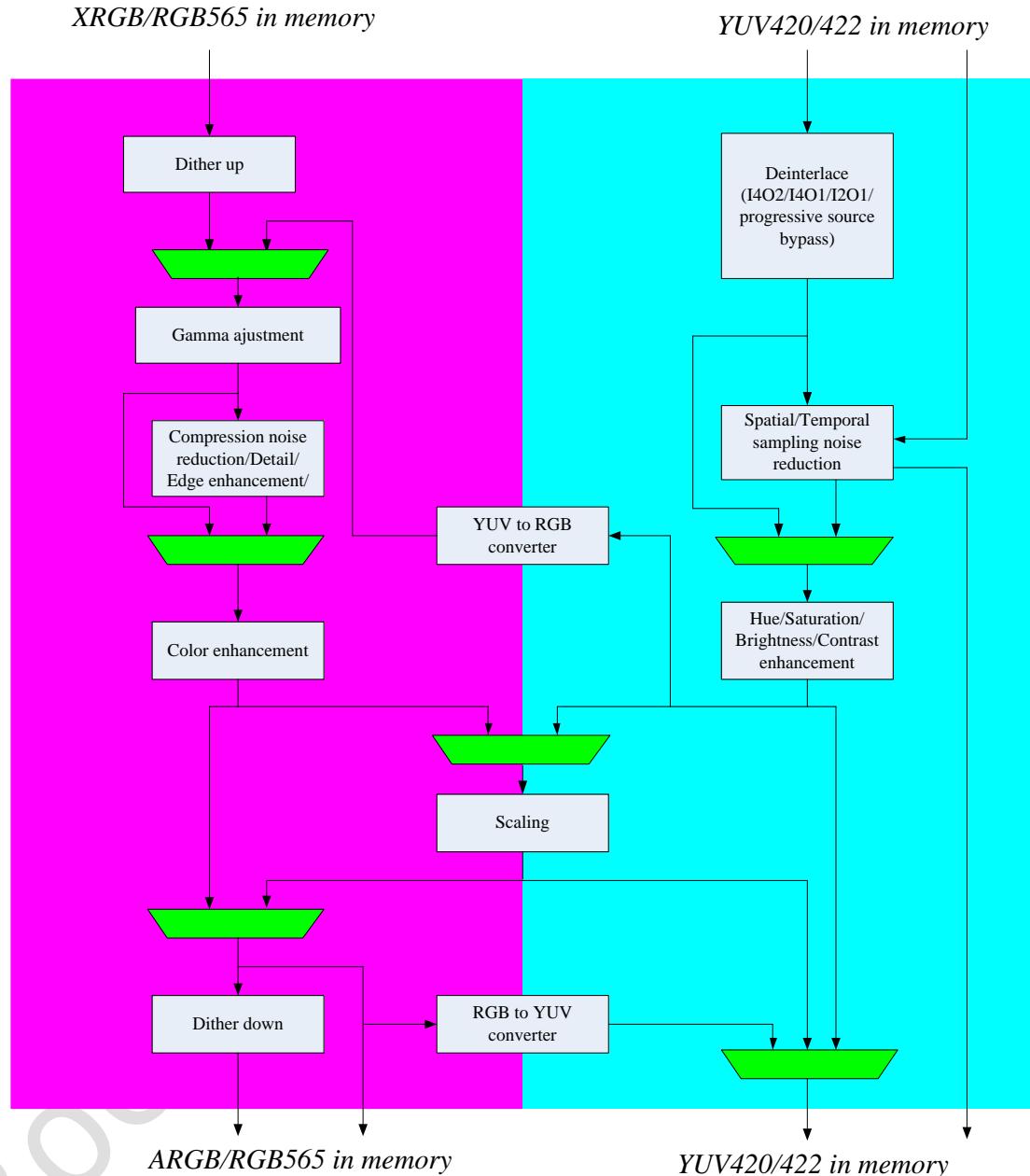


Fig. 17-1 IEP block diagram

The data path in IEP is in the previously diagram. The IEP comprises with:

Deinterlace

There are five deinterlace mode including I4O2 (input 4 fields and output 2 frames once), I4O1B, I4O1T, I2O1B, I2O1T in the deinterlace block. YUV bypass is also supported.

Enhancement

Not only hue, saturation, brightness, contrast enhancement, but also blue screen, black screen and color bar are supported in YUV domain enhancement block. Gamma adjustment, edge enhancement, detail enhancement and color enhancement are supported in RGB domain enhancement block.

Noise Reduction

Spatial and temporal sampling noise can be reduced in YUV domain noise reduction block. Compression noise can be reduced in RGB domain noise reduction block.

Scaling

There are four types of scaling modes.

Horizontal down-scaling with vertical down-scaling

Horizontal down-scaling with vertical up-scaling

Horizontal up-scaling with vertical down-scaling

Horizontal up-scaling with vertical up-scaling

17.3 Function description

17.3.1 Deinterlace

There are five deinterlace mode including I4O2, I4O1B, I4O1T, I2O1B and I2O1T in the deinterlace block. The I4O2 mode represents for 4 fields of input images and 2 frames of output images, so all of the two groups of source address registers and two groups of destination address registers need to be configured. For example, if source and destination format are both YUV420, the source address register IEP_SRC_ADDR_YRGB, IEP_SRC_ADDR_CBCR are used for source field0 and field 1, the source address register IEP_SRC_ADDR_Y1, IEP_SRC_ADDR_CBCR1 are used for source field2 and field3. The I4O1B and I4O1T mode have the same input images as the I4O2 mode, but only one frame output is generated once. The I2O1B and I2O1T mode have the same output as I4O1B and I4O1T mode, but only two fields input are needed. If bypass mode is selected, there are not any deinterlace operations. The parameter dil_ei_sel, dil_ei_radius, dil_ei_smooth, dil_ei_mode, dil_hf_en and dil_hf_fct in register IEP_CONFIG0 and registers IEP_DIL_MTN_TAB0~7 may have different influence in deinterlace effect depend on the type of the image source.

17.3.2 Noise reduction

Both of spatial and temporal sampling noise reduction are enabled when the 3D denoise bit is set. This function is used for reducing the noise generated at video or picture capturing in the camera sensor. There are four groups of optional noise reduction effect coefficients for luminance and chrominance in spatial and temporal segment.

Compression noise reduction is used for reducing the noise after the decompression of picture or video. Before the compression noise reduction is enabled, the IEP_ENH_DDE_COE0/1 from address 0x400 to 0x5FC for difference and distance coefficients must be written firstly. The filter matrix can be selected from 3x3/5x5/7x7/9x9 and the filter weight can be programmed by configuring IEP_ENH_RGB_CNFG.

17.3.3 Enhancement

Not only hue, saturation, brightness, contrast enhancement, but also blue screen, black screen and color bar are supported in this block. IEP_ENH_YUV_CNFG_0/1/2 registers can be configured to modify the YUV enhance parameters to satisfied with the requirement.

Before the gamma adjustment or contrast enhancement is enabled in RGB domain, the IEP_ENH_CG_TAB from address 0x100 to 0x3FC for B, G, R mapping must be written firstly. If the color enhancement is enabled, the IEP_ENH_C_COE must be written the required value. Before the edge or detail enhancement is enabled, the IEP_ENH_DDE_COE0/1 from address 0x400 to 0x5FC for difference and distance coefficients must be written firstly. The filter matrix can be selected from 3x3/5x5/7x7/9x9 and the filter weight can be programmed by configuring IEP_ENH_RGB_CNFG.

17.3.4 Scaling

There are four types of scaling modes: horizontal down & vertical down-scaling, horizontal down & vertical up-scaling, horizontal up & vertical down-scaling, horizontal up & vertical up-scaling. The down-scaling and up-scaling factor can be got from different way. The detail calculated method is the following:

- $vrt_up_scl_fct = \text{floor}(\text{src_image_height}/\text{dst_image_height})$

- $vrt_dn_scl_fct = \text{ceiling}((\text{dst_image_height}+1)/(\text{src_image_height}+1))$

- hz_up_scl_fct=floor(src_image_width/dst_image_width)
- hz_dn_scl_fct=ceiling((dst_image_width+1)/(src_image_width+1))

There are four up-scaling type (Hermite, Spline, Catrom and Mitchell) can be selected for difference requirement.

17.3.5 Format conversion

The color space conversion either from RGB to YUV or from YUV to RGB has the selections including BT601/709_L/F mode, and the input can be clipped or not.

If the source format is RGB565, dither up must be enabled. In contrary to the destination format is RGB565, dither down must be enabled.

17.3.6 Shadow registers

The configuration registers can be configured at any time, but they cannot have any effect immediately unless config_done is available and a new frame_start is enabled. The registers IEP_RAW_CONFIG0/1, IEP_RAW_VIR_IMG_WIDTH, IEP_RAW_IMG_SCL_FCT, IEP_RAW_SRC_IMG_SIZE, IEP_RAW_ENH_YUV_CNFG_0/1/2 corresponding to the registers have the similar names but without letters _RAW. They are used for raw register value reading before the configurations really have effect on the new frame.

17.3.7 VOP direct path

The IEP_DST_ADDR for DMA writing is useless if vop_path_en bit is set, because all RGB or YUV data is supplied for VOP directly from local bus via VOP and IEP.

17.4 Register description

17.4.1 Register Summary

Name	Offset	Size	Reset Value	Description
IEP_CONFIG0	0x00000	W	0x00000000	configuration register0
IEP_CONFIG1	0x00004	W	0x00000000	configuration register1
IEP_STATUS	0x00008	W	0x00000000	status register
IEP_INT	0x0000c	W	0x00000000	interrupt register
IEP_FRM_START	0x00010	W	0x00000000	frame start
IEP_CONFIG_DONE	0x00018	W	0x00000000	configuration done
IEP_FRM_CNT	0x0001c	W	0x00000000	frame counter
IEP_VIR_IMG_WIDTH	0x00020	W	0x01400140	Image virtual width
IEP_IMG_SCL_FCT	0x00024	W	0x20002000	scaling factor
IEP_SRC_IMG_SIZE	0x00028	W	0x00f00140	Source image width/height
IEP_DST_IMG_SIZE	0x0002c	W	0x00f00140	Destination image width/height
IEP_DST_IMG_WIDTH_TILE0	0x00030	W	0x00000000	Destination image tile0 width
IEP_DST_IMG_WIDTH_TILE1	0x00034	W	0x00000000	Destination image tile1 width
IEP_DST_IMG_WIDTH_TILE2	0x00038	W	0x00000000	Destination image tile2 width
IEP_DST_IMG_WIDTH_TILE3	0x0003c	W	0x00000000	Destination image tile3 width
IEP_ENH_YUV_CNFG_0	0x00040	W	0x00000000	brightness,contrast,saturation adjustment
IEP_ENH_YUV_CNFG_1	0x00044	W	0x00000000	Hue configuration
IEP_ENH_YUV_CNFG_2	0x00048	W	0x00000000	color bar configuration
IEP_ENH_RGB_CNFG	0x0004c	W	0x00000000	enhancement RGB configuration
IEP_ENH_C_COE	0x00050	W	0x00000000	rgb color enhancement coefficient

Name	Offset	Size	Reset Value	Description
IEP_RAW_CONFIG0	0x00058	W	0x00000000	configuration register0
IEP_RAW_CONFIG1	0x0005c	W	0x00000000	configuration register1
IEP_RAW_VIR_IMG_WIDTH	0x00060	W	0x01400140	Image virtual width
IEP_RAW_IMG_SCL_FCT	0x00064	W	0x20002000	scaling factor
IEP_RAW_SRC_IMG_SIZE	0x00068	W	0x00f00140	Source image width/height
IEP_RAW_DST_IMG_SIZE	0x0006c	W	0x00f00140	Destination image width/height
IEP_RAW_ENH_YUV_CNFG_0	0x00070	W	0x00000000	brightness,contrast,saturation adjustment
IEP_RAW_ENH_YUV_CNFG_1	0x00074	W	0x00000000	Hue configuration
IEP_RAW_ENH_YUV_CNFG_2	0x00078	W	0x00000000	color bar configuration
IEP_RAW_ENH_RGB_CNFG	0x0007c	W	0x00000000	enhancement RGB configuration
IEP_SRC_ADDR_YRGB	0x00080	W	0x00000000	Start address of source image(Y/RGB)
IEP_SRC_ADDR_CBCR	0x00084	W	0x00000000	Start address of source image(Cb/Cr)
IEP_SRC_ADDR_CR	0x00088	W	0x00000000	Start address of source image(Cr)
IEP_SRC_ADDR_Y1	0x0008c	W	0x00000000	Start address of source image(Y)
IEP_SRC_ADDR_CBCR1	0x00090	W	0x00000000	Start address of source image(Cb/Cr)
IEP_SRC_ADDR_CR1	0x00094	W	0x00000000	Start address of source image(Cr)
IEP_SRC_ADDR_Y_ITEMP	0x00098	W	0x00000000	Start address of source image(Y integer part)
IEP_SRC_ADDR_CBCR_ITEMP	0x0009c	W	0x00000000	Start address of source image(CBCR integer part)
IEP_SRC_ADDR_CR_ITEMP	0x000a0	W	0x00000000	Start address of source image(CR integer part)
IEP_SRC_ADDR_Y_FTEMP	0x000a4	W	0x00000000	Start address of source image(Y fraction part)
IEP_SRC_ADDR_CBCR_FTEMP	0x000a8	W	0x00000000	Start address of source image(CBCR fraction part)
IEP_SRC_ADDR_CR_FTEMP	0x000ac	W	0x00000000	Start address of source image(CR fraction part)
IEP_DST_ADDR_YRGB	0x000b0	W	0x00000000	Start address of destination image(Y/RGB)
IEP_DST_ADDR_CBCR	0x000b4	W	0x00000000	Start address of destination image(Cb/Cr)
IEP_DST_ADDR_CR	0x000b8	W	0x00000000	Start address of destination image(Cr)

Name	Offset	Size	Reset Value	Description
IEP_DST_ADDR_Y1	0x000bc	W	0x00000000	Start address of destination image(Y)
IEP_DST_ADDR_CBCR1	0x000c0	W	0x00000000	Start address of destination image(Cb/Cr)
IEP_DST_ADDR_CR1	0x000c4	W	0x00000000	Start address of destination image(Cr)
IEP_DST_ADDR_Y_ITEMP	0x000c8	W	0x00000000	Start address of destination image(Y integer part)
IEP_DST_ADDR_CBCR_ITEMP	0x000cc	W	0x00000000	Start address of destination image(CBCR integer part)
IEP_DST_ADDR_CR_ITEMP	0x000d0	W	0x00000000	Start address of destination image(CR integer part)
IEP_DST_ADDR_Y_FTEMP	0x000d4	W	0x00000000	Start address of destination image(Y fraction part)
IEP_DST_ADDR_CBCR_FTEMP	0x000d8	W	0x00000000	Start address of destination image(CBCR fraction part)
IEP_DST_ADDR_CR_FTEMP	0x000dc	W	0x00000000	Start address of destination image(CR fraction part)
IEP_DIL_MTN_TAB0	0x000e0	W	0x00000000	Deinterlace motion table0
IEP_DIL_MTN_TAB1	0x000e4	W	0x00000000	Deinterlace motion table1
IEP_DIL_MTN_TAB2	0x000e8	W	0x00000000	Deinterlace motion table2
IEP_DIL_MTN_TAB3	0x000ec	W	0x00000000	Deinterlace motion table3
IEP_DIL_MTN_TAB4	0x000f0	W	0x00000000	Deinterlace motion table4
IEP_DIL_MTN_TAB5	0x000f4	W	0x00000000	Deinterlace motion table5
IEP_DIL_MTN_TAB6	0x000f8	W	0x00000000	Deinterlace motion table6
IEP_DIL_MTN_TAB7	0x000fc	W	0x00000000	Deinterlace motion table7
IEP_ENH(CG)_TAB	0x00100	W	0x00000000	contrast and gamma enhancement table
IEP_ENH(DDE)_COE0	0x00400	W	0x00000000	denoise,detail and edge enhancement coefficient
IEP_ENH(DDE)_COE1	0x00500	W	0x00000000	denoise,detail and edge enhancement coefficient
IEP_MMU_DTE_ADDR	0x00800	W	0x00000000	MMU current page table address
IEP_MMU_STATUS	0x00804	W	0x00000018	MMU status register
IEP_MMU_CMD	0x00808	W	0x00000000	MMU command register
IEP_MMU_PAGE_FAULT_ADDR	0x0080c	W	0x00000000	MMU logic address of last page fault
IEP_MMU_ZAP_ONE_LINE	0x00810	W	0x00000000	MMU zap cache line register
IEP_MMU_INT_RAWSTAT	0x00814	W	0x00000000	MMU raw interrupt status register
IEP_MMU_INT_CLEAR	0x00818	W	0x00000000	MMU interrupt clear register
IEP_MMU_INT_MASK	0x0081c	W	0x00000000	MMU interrupt mask register
IEP_MMU_INT_STATUS	0x00820	W	0x00000000	MMU interrupt status register

Name	Offset	Size	Reset Value	Description
IEP_MMU_AUTO_GATING	0x00824	W	0x00000001	MMU clock auto gating register

Notes: Size : **B** - Byte (8 bits) access, **HW** - Half WORD (16 bits) access, **W** -WORD (32 bits) access

17.4.2 Detail Register Description

IEP_CONFIG0

Address: Operational Base + offset (0x000000)
configuration register0

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28	RW	0x0	scl_en image scaling enable 0:disable 1:enable
27:26	RW	0x0	scl_sel Scaling select 00: horizontal down-scaling & vertical down-scaling; 01: horizontal down-scaling & vertical up-scaling; 10: horizontal up-scaling & vertical down-scaling; 11: horizontal up-scaling & vertical up-scaling;
25:24	RW	0x0	scl_up_coe_sel scale up coefficient select 00:hermite 01:spline 10:catrom 11:mitchell
23	RW	0x0	dil_ei_sel deinterlace edge interpolation select
22:21	RW	0x0	dil_ei_radius deinterlace edge interpolation radius
20	RW	0x0	rgb_con_gam_order RGB contrast enhancement and gamma adjustment operation order select. 0:CG prior to DDE 1:DDE prior to CG (CG represent for contrast & gamma operation, and DDE represent for denoise, detail or edge enhancement operation)

Bit	Attr	Reset Value	Description
19:18	RW	0x0	rgb_enh_sel RGB enhancement select 00: no operation 01: denoise 10: detail enhancement 11: edge enhancement
17	RW	0x0	rgb_con_gam_en RGB contrast enhancement and gamma adjustment enable 0:disable 1:enable
16	RW	0x0	rgb_color_enh_en RGB color enhancement enable 0:disable 1:enable
15	RW	0x0	dil_ei_smooth deinterlace edge interpolation for smooth effect 0: disable 1: enable
14	RW	0x0	yuv_enh_en yuv enhancement enable 0:disable 1:enable
13	RW	0x0	yuv_dns_en YUV 3D denoise enable 0:disable 1:enable
12	RW	0x0	dil_ei_mode deinterlace edge interpolation 0: disable 1: enable
11	RW	0x0	dil_hf_en deinterlace high frequency calculation enable 0: disable 1: enable

Bit	Attr	Reset Value	Description
10:8	RW	0x0	dil_mode Deinterlace mode select: 000: YUV deinterlace and bypass path disable; 001: I4O2 mode 010: I4O1B mode 011: I4O1T mode 100: I2O1B mode 101: I2O1T mode 110: bypass mode
7:1	RW	0x00	dil_hf_fct deinterlace high frequency factor
0	RW	0x0	vop_path_en VOP direct path enable 0:disable 1:enable

IEP_CONFIG1

Address: Operational Base + offset (0x00004)
configuration register1

Bit	Attr	Reset Value	Description
31:24	RW	0x00	glb_alpha global alpha value only valid when destination format is ARGB
23	RW	0x0	rgb2yuv_input_clip RGB to YUV input range 0:R/G/B=[0,255] 1:R/G/B=[16,235]
22	RW	0x0	yuv2rgb_input_clip YUV to RGB input range 0:Y/U/V=[0,255] 1:Y=[16,235],U/V=[16,240]
21	RW	0x0	rgb_to_yuv_en RGB to YUV conversion enable 0: disable 1: enable
20	RW	0x0	yuv_to_rgb_en YUV to RGB conversion enable 0: disable 1: enable

Bit	Attr	Reset Value	Description
19:18	RW	0x0	rgb2yuv_coe_sel rgb2yuv coefficient select 00:bt601_1 01:bt601_f 10:bt709_1 11:bt709_f
17:16	RW	0x0	yuv2rgb_coe_sel yuv2rgb coefficient select 00:bt601_1 01:bt601_f 10:bt709_1 11:bt709_f
15	RW	0x0	dthr_down_en dither down enable 0: disable 1: enable
14	RW	0x0	dthr_up_en dither up enable 0: disable 1: enable
13:12	RW	0x0	dst_yuv_swap destination YUV swap 00:SP UV 01:SP VU 10, 11:P
11:10	RW	0x0	dst_rgb_swap destination RGB swap ARGB destination 00:ARGB 01:ABGR 10:RGBA 11:BGRA RGB565 destination 00,10:RGB 01,11:BGR
9:8	RW	0x0	dst_fmt Output image Format 00 : ARGB 01 : RGB565 10 : YUV422 11 : YUV420
7:6	RO	0x0	reserved

Bit	Attr	Reset Value	Description
5:4	RW	0x0	src_yuv_swap source YUV swap 00:SP UV 01:SP VU 10, 11:P
3:2	RW	0x0	src_rgb_swap source RGB swap XRGB source 00:XRGB 01:XBGR 10:RGBX 11:BGRX RGB565 source 00,10:RGB 01,11:BGR
1:0	RW	0x0	src_fmt Input image Format 00 : XRGB 01 : RGB565 10 : YUV422 11 : YUV420

IEP_STATUS

Address: Operational Base + offset (0x00008)

status register

Bit	Attr	Reset Value	Description
31:20	RO	0x0	reserved
19	RW	0x0	rrgb_idle_ack RGB read DMA idle acknowlege
18	RW	0x0	wrgb_idle_ack RGB write DMA idle acknowlege
17	RW	0x0	ryuv_idle_ack YUV read DMA idle acknowlege
16	RW	0x0	wyuv_idle_ack YUV write DMA idle acknowlege
15:9	RO	0x0	reserved
8	RO	0x0	voi_sts vop direct path status 00:idle 01:working
7	RO	0x0	rrgb_sts RGB DMA read status 00:idle 01:working

Bit	Attr	Reset Value	Description
6	RO	0x0	wrgb_sts RGB DMA write status 00:idle 01:working
5	RO	0x0	ryuv_sts YUV DMA read status 00:idle 01:working
4	RO	0x0	wyuv_sts YUV DMA write status 00:idle 01:working
3	RO	0x0	dde_sts RGB denoise/enhancement status 00:idle 01:working
2	RO	0x0	dil_sts de-interlace or yuv bypass status 00:idle 01:working
1	RO	0x0	scl_sts scaling status 00:idle 01:working
0	RO	0x0	dns_sts YUV 3D denoise status 00:idle 01:working

IEP_INT

Address: Operational Base + offset (0x0000c)

interrupt register

Bit	Attr	Reset Value	Description
31:17	RO	0x0	reserved
16	W1C	0x0	frm_done_int_clr Frame process done interrupt clear After be set to 1, this bit will be clear automatically.
15:9	RO	0x0	reserved
8	RW	0x0	frm_done_int_en Frame process done interrupt enable: 0: disable; 1: enable;
7:1	RO	0x0	reserved

Bit	Attr	Reset Value	Description
0	RO	0x0	frm_done_int Frame process done interrupt 0: inactive; 1: active;

IEP_FRM_START

Address: Operational Base + offset (0x00010)
frame start

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	W1C	0x0	frm_start frame start Write 1, self clear.

IEP_CONFIG_DONE

Address: Operational Base + offset (0x00018)
configuration done

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	config_done configuration done Wait for frame start to update raw register configuration to really used registers.

IEP_FRM_CNT

Address: Operational Base + offset (0x0001c)
frame counter

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	frm_cnt frame counter Self increase one after a frame operation is finished. Write arbitrary value to clear to zero.

IEP_VIR_IMG_WIDTH

Address: Operational Base + offset (0x00020)
Image virtual width

Bit	Attr	Reset Value	Description
31:16	RW	0x0140	dst_vir_image_width Destination virtual image width
15:0	RW	0x0140	src_vir_image_width Source virtual image width

IEP_IMG_SCL_FCT

Address: Operational Base + offset (0x00024)

scaling factor

Bit	Attr	Reset Value	Description
31:16	RW	0x2000	<p>vrt_scl_fct Vertical scale factor up scaling: $vrt_scl_fct = \text{floor}(\text{src_image_height}/\text{dst_image_height})$; down scaling: $vrt_scl_fct = \text{ceiling}((\text{dst_image_height}+1)/(\text{src_image_height}+1))$;</p>
15:0	RW	0x2000	<p>hrz_scl_fct Horizontal scale factor up scaling: $hrz_scl_fct = \text{floor}(\text{src_image_width}/\text{dst_image_width})$; down scaling: $hrz_scl_fct = \text{ceiling}((\text{dst_image_width}+1)/(\text{src_image_width}+1))$;</p>

IEP_SRC_IMG_SIZE

Address: Operational Base + offset (0x00028)

Source image width/height

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x00f0	src_image_height source image height
15:13	RO	0x0	reserved
12:0	RW	0x0140	src_image_width source image width

IEP_DST_IMG_SIZE

Address: Operational Base + offset (0x0002c)

Destination image width/height

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x00f0	dst_image_height Destination image height
15:13	RO	0x0	reserved
12:0	RW	0x0140	dst_image_width Destination image width

IEP_DST_IMG_WIDTH_TILE0

Address: Operational Base + offset (0x00030)

Destination image tile0 width

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved

Bit	Attr	Reset Value	Description
11:0	RW	0x000	dst_image_width_tile0 Destination image tile0 width

IEP_DST_IMG_WIDTH_TILE1

Address: Operational Base + offset (0x00034)

Destination image tile1 width

Bit	Attr	Reset Value	Description
31:11	RO	0x0	reserved
10:0	RW	0x000	dst_image_width_tile1 Destination image tile1 width

IEP_DST_IMG_WIDTH_TILE2

Address: Operational Base + offset (0x00038)

Destination image tile2 width

Bit	Attr	Reset Value	Description
31:11	RO	0x0	reserved
10:0	RW	0x000	dst_image_width_tile2 Destination image tile2 width

IEP_DST_IMG_WIDTH_TILE3

Address: Operational Base + offset (0x0003c)

Destination image tile3 width

Bit	Attr	Reset Value	Description
31:11	RO	0x0	reserved
10:0	RW	0x000	dst_image_width_tile3 Destination image tile3 width

IEP_ENH_YUV_CNFG_0

Address: Operational Base + offset (0x00040)

brightness,contrast,saturation adjustment

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24:16	RW	0x000	sat_con YUV saturation and contrast adjustment saturation * contrast range from 0 to 1.992*1.992, and this value is saturation* contrast * 128
15:8	RW	0x00	contrast YUV contrast adjustment contrast value range from 0 to 1.992, and this value is contrast*128.
7:6	RO	0x0	reserved

Bit	Attr	Reset Value	Description
5:0	RW	0x00	brightness YUV brightness adjustment range from -32 to 31 000000:0; 000001:1; 011111:31; 100000:-32; 100001:-31; 111110:-2; 111111:-1;

IEP_ENH_YUV_CNFG_1

Address: Operational Base + offset (0x00044)

Hue configuration

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:8	RW	0x00	cos_hue the cos function value for hue adjustment sin function value range from 0.866 to 1 ,and this value is cos * 128 ,no sign bit
7:0	RW	0x00	sin_hue the sin function value for hue adjustment sin function value range from -0.5 to 0.5 ,and this value is sin * 128 ,and the high bit is sign bit

IEP_ENH_YUV_CNFG_2

Address: Operational Base + offset (0x00048)

color bar configuration

Bit	Attr	Reset Value	Description
31:26	RO	0x0	reserved
25:24	RW	0x0	video_mode video mode 00:black screen 01:blue screen 10:color bars 11:normal video
23:16	RW	0x00	color_bar_v color bar v value
15:8	RW	0x00	color_bar_u color bar u value
7:0	RW	0x00	color_bar_y color bar y value

IEP_ENH_RGB_CNFG

Address: Operational Base + offset (0x0004c)

enhancement RGB configuration

Bit	Attr	Reset Value	Description
31:30	RW	0x0	luma_spat_sel 3D denoise luma spatial coefficient select
29:28	RW	0x0	luma_temp_sel 3D denoise luma temporal coefficient select
27:26	RW	0x0	chroma_spat_sel 3D denoise chroma spatial coefficient select
25:24	RW	0x0	chroma_temp_sel 3D denoise chroma temporal coefficient select
23:16	RW	0x00	enh_threshold enhancement threshold In denoise and detail enhancement operation, more than the threshold, considering as detail; but if less than the threshold, considering as noise, need to be filtered.
15	RO	0x0	reserved
14:8	RW	0x00	enh_alpha enhancement alpha value 0000000:0 0000001:1/16 0000010:2/16 0001111:15/16 0010000:1 0010001:1+1/16; 0010010:1+2/16; 0010011:1+3/16; 0100000:2; 0110000:3; 1000000:4; 1010000:5; 1100000:6; other : reserved
7:2	RO	0x0	reserved

Bit	Attr	Reset Value	Description
1:0	RW	0x0	enh_radius enhancement radius 00:R=1 01:R=2 10:R=3 11:R=4

IEP_ENH_C_COE

Address: Operational Base + offset (0x00050)

rgb color enhancement coefficient

Bit	Attr	Reset Value	Description
31:7	RO	0x0	reserved
6:5	RW	0x0	c_int_coe color enhancement integer coefficient
4:0	RW	0x00	c_frac_coe color enhancement fraction coefficient

IEP_RAW_CONFIG0

Address: Operational Base + offset (0x00058)

configuration register0

Bit	Attr	Reset Value	Description
31	RW	0x0	vrt_inv vertical inverse display 0: normal display 1: inverse display
30	RW	0x0	hrz_inv horizontal inverse display 0: normal display 1: inverse display
29	RO	0x0	reserved
28	RW	0x0	scl_en image scaling enable 0: disable 1: enable
27:26	RW	0x0	scl_sel Scaling select 00: horizontal down-scaling & vertical down-scaling; 01: horizontal down-scaling & vertical up-scaling; 10: horizontal up-scaling & vertical down-scaling; 11: horizontal up-scaling & vertical up-scaling;

Bit	Attr	Reset Value	Description
25:24	RW	0x0	scl_up_coe_sel scale up coefficient select 00:hermite 01:spline 10:catrom 11:mitchell
23	RW	0x0	dil_ei_sel deinterlace edge interpolation select
22:21	RW	0x0	dil_ei_radius deinterlace edge interpolation radius
20	RW	0x0	rgb_con_gam_order RGB contrast enhancement and gamma adjustment operation order select. 0:CG prior to DDE 1:DDE prior to CG (CG represent for contrast & gamma operation, and DDE represent for denoise, detail or edge enhancement operation)
19:18	RW	0x0	rgb_enh_sel RGB enhancement select 00: no operation 01: denoise 10: detail enhancement 11: edge enhancement
17	RW	0x0	rgb_con_gam_en RGB contrast enhancement and gamma adjustment enable 0:disable 1:enable
16	RW	0x0	rgb_color_enh_en RGB color enhancement enable 0:disable 1:enable
15	RW	0x0	dil_ei_smooth deinterlace edge interpolation for smooth effect 0: disable 1: enable
14	RW	0x0	yuv_enh_en yuv enhancement enable 0:disable 1:enable

Bit	Attr	Reset Value	Description
13	RW	0x0	yuv_dns_en YUV 3D denoise enable 0:disable 1:enable
12	RW	0x0	dil_ei_mode deinterlace edge interpolation 0: disable 1: enable
11	RW	0x0	dil_hf_en deinterlace high frequency calculation enable 0: disable 1: enable
10:8	RW	0x0	dil_mode Deinterlace mode select: 000: YUV deinterlace and bypass path disable; 001: I4O2 mode 010: I4O1B mode 011: I4O1T mode 100: I2O1B mode 101: I2O1T mode 110: bypass mode
7:1	RW	0x00	dil_hf_fct deinterlace high frequency factor
0	RW	0x0	vop_path_en VOP direct path enable 0:disable 1:enable

IEP_RAW_CONFIG1

Address: Operational Base + offset (0x0005c)

configuration register1

Bit	Attr	Reset Value	Description
31:24	RO	0x00	glb_alpha global alpha value only valid when destination format is ARGB
23	RO	0x0	rgb2yuv_input_clip RGB to YUV input range 0:R/G/B=[0,255] 1:R/G/B=[16,235]
22	RO	0x0	yuv2rgb_input_clip YUV to RGB input range 0:Y/U/V=[0,255] 1:Y=[16,235],U/V=[16,240]

Bit	Attr	Reset Value	Description
21	RO	0x0	rgb_to_yuv_en RGB to YUV conversion enable 0: disable 1: enable
20	RO	0x0	yuv_to_rgb_en YUV to RGB conversion enable 0: disable 1: enable
19:18	RO	0x0	rgb2yuv_coe_sel rgb2yuv coefficient select 00:bt601_1 01:bt601_f 10:bt709_1 11:bt709_f
17:16	RO	0x0	yuv2rgb_coe_sel yuv2rgb coefficient select 00:bt601_1 01:bt601_f 10:bt709_1 11:bt709_f
15	RO	0x0	dthr_down_en dither down enable 0: disable 1: enable
14	RO	0x0	dthr_up_en dither up enable 0: disable 1: enable
13:12	RO	0x0	dst_yuv_swap destination YUV swap 00:SP UV 01:SP VU 10, 11:P
11:10	RO	0x0	dst_rgb_swap destination RGB swap ARGB destination 00:ARGB 01:ABGR 10:RGBA 11:BGRA RGB565 destination 00,10:RGB 01,11:BGR

Bit	Attr	Reset Value	Description
9:8	RO	0x0	dst_fmt Output image Format 00 : ARGB 01 : RGB565 10 : YUV422 11 : YUV420
7:6	RO	0x0	reserved
5:4	RO	0x0	src_yuv_swap source YUV swap 00:SP UV 01:SP VU 10, 11:P
3:2	RO	0x0	src_rgb_swap source RGB swap XRGB source 00:XRGB 01:XBGR 10:RGBX 11:BGRX RGB565 source 00,10:RGB 01,11:BGR
1:0	RO	0x0	src_fmt Input image Format 00 : XRGB 01 : RGB565 10 : YUV422 11 : YUV420

IEP_RAW_VIR_IMG_WIDTH

Address: Operational Base + offset (0x00060)

Image virtual width

Bit	Attr	Reset Value	Description
31:16	RO	0x0140	dst_vir_image_width Destination virtual image width
15:0	RO	0x0140	src_vir_image_width Source virtual image width

IEP_RAW_IMG_SCL_FCT

Address: Operational Base + offset (0x00064)

scaling factor

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	RO	0x2000	vrt_scl_fct Vertical scale factor up scaling: $vrt_scl_fct=floor(src_image_height/dst_image_height);$ down scaling: $vrt_scl_fct=ceiling((dst_image_height+1)/(src_image_height+1));$
15:0	RO	0x2000	hrz_scl_fct Horizontal scale factor up scaling: $hrz_scl_fct=floor(src_image_width/dst_image_width);$ down scaling: $hrz_scl_fct=ceiling((dst_image_width+1)/(src_image_width+1));$

IEP_RAW_SRC_IMG_SIZE

Address: Operational Base + offset (0x00068)

Source image width/height

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RO	0x00f0	src_image_height source image height
15:13	RO	0x0	reserved
12:0	RO	0x0140	src_image_width source image width

IEP_RAW_DST_IMG_SIZE

Address: Operational Base + offset (0x0006c)

Destination image width/height

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RO	0x00f0	dst_image_height Destination image height
15:13	RO	0x0	reserved
12:0	RO	0x0140	dst_image_width Destination image width

IEP_RAW_ENH_YUV_CNFG_0

Address: Operational Base + offset (0x00070)

brightness,contrast,saturation adjustment

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved

Bit	Attr	Reset Value	Description
24:16	RO	0x000	sat_con YUV saturation and contrast adjustment saturation * contrast range from 0 to 1.992*1.992, and this value is saturation* contrast * 128
15:8	RO	0x00	contrast YUV contrast adjustment contrast value range from 0 to 1.992, and this value is contrast*128.
7:6	RO	0x0	reserved
5:0	RO	0x00	brightness YUV brightness adjustment range from -32 to 31 000000:0; 000001:1; 011111:31; 100000:-32; 100001:-31; 111110:-2; 111111:-1;

IEP_RAW_ENH_YUV_CNFG_1

Address: Operational Base + offset (0x00074)

Hue configuration

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:8	RO	0x00	cos_hue the cos function value for hue adjustment sin function value range from 0.866 to 1 ,and this value is cos * 128 ,no sign bit
7:0	RO	0x00	sin_hue the sin function value for hue adjustment sin function value range from -0.5 to 0.5 ,and this value is sin * 128 ,and the high bit is sign bit

IEP_RAW_ENH_YUV_CNFG_2

Address: Operational Base + offset (0x00078)

color bar configuration

Bit	Attr	Reset Value	Description
31:26	RO	0x0	reserved

Bit	Attr	Reset Value	Description
25:24	RO	0x0	video_mode video mode 00:black screen 01:blue screen 10:color bars 11:normal video
23:16	RO	0x00	color_bar_v color bar v value
15:8	RO	0x00	color_bar_u color bar u value
7:0	RO	0x00	color_bar_y color bar y value

IEP_RAW_ENH_RGB_CNFG

Address: Operational Base + offset (0x0007c)

enhancement RGB configuration

Bit	Attr	Reset Value	Description
31:30	RW	0x0	luma_spat_sel 3D denoise luma spatial coefficient select
29:28	RW	0x0	luma_temp_sel 3D denoise luma temporal coefficient select
27:26	RW	0x0	chroma_spat_sel 3D denoise chroma spatial coefficient select
25:24	RW	0x0	chroma_temp_sel 3D denoise chroma temporal coefficient select
23:16	RW	0x00	enh_threshold enhancement threshold In denoise and detail enhancement operation, more than the threshold, considering as detail; but if less than the threshold, considering as noise, need to be filtered.
15	RO	0x0	reserved

Bit	Attr	Reset Value	Description
14:8	RW	0x00	enh_alpha enhancement alpha value 0000000:0 0000001:1/16 0000010:2/16 0001111:15/16 0010000:1 0010001:1+1/16; 0010010:1+2/16; 0010011:1+3/16; 0100000:2; 0110000:3; 1000000:4; 1010000:5; 1100000:6; other : reserved
7:2	RO	0x0	reserved
1:0	RW	0x0	enh_radius enhancement radius 00:R=1 01:R=2 10:R=3 11:R=4

IEP_SRC_ADDR_YRGB

Address: Operational Base + offset (0x00080)

Start address of source image(Y/RGB)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	src_image_yrgb_mst Source image data YRGB start address in Memory

IEP_SRC_ADDR_CBCR

Address: Operational Base + offset (0x00084)

Start address of source image(Cb/Cr)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	src_image_cbcr_mst Source image data CbCr start address in Memory

IEP_SRC_ADDR_CR

Address: Operational Base + offset (0x00088)

Start address of source image(Cr)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	src_image_cr_mst Source image data Cr start address in Memory

IEP_SRC_ADDR_Y1

Address: Operational Base + offset (0x0008c)

Start address of source image(Y)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	src_image_y_mst Source image data Y start address in Memory

IEP_SRC_ADDR_CBCR1

Address: Operational Base + offset (0x00090)

Start address of source image(Cb/Cr)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	src_image_cbcr_mst Source image data CbCr start address in Memory

IEP_SRC_ADDR_CR1

Address: Operational Base + offset (0x00094)

Start address of source image(Cr)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	src_image_cr_mst Source image data Cr start address in Memory

IEP_SRC_ADDR_Y_ITEMP

Address: Operational Base + offset (0x00098)

Start address of source image(Y integer part)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	src_image_y_mst_itemp Interger part source image data Y start address in Memory

IEP_SRC_ADDR_CBCR_ITEMP

Address: Operational Base + offset (0x0009c)

Start address of source image(CBCR integer part)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	src_image_cbcr_mst_cbcr_itemp Interger part source image data CBCR start address in Memory

IEP_SRC_ADDR_CR_IITEMP

Address: Operational Base + offset (0x000a0)

Start address of source image(CR integer part)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	src_image_cr_mst_cr_iitemp Integer part source image data CR start address in Memory

IEP_SRC_ADDR_Y_FTEMP

Address: Operational Base + offset (0x000a4)

Start address of source image(Y fraction part)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	src_image_y_mst_ftemp Fraction part source image data Y start address in Memory

IEP_SRC_ADDR_CBCR_FTEMP

Address: Operational Base + offset (0x000a8)

Start address of source image(CBCR fraction part)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	src_image_cbcr_mst_ftemp Fraction part source image data CBCR start address in Memory

IEP_SRC_ADDR_CR_FTEMP

Address: Operational Base + offset (0x000ac)

Start address of source image(CR fraction part)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	src_image_cr_mst_ftemp Fraction part source image data CR start address in Memory

IEP_DST_ADDR_YRGB

Address: Operational Base + offset (0x000b0)

Start address of destination image(Y/RGB)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	dst_image_yrgb_mst Destination image data YRGB start address in Memory

IEP_DST_ADDR_CBCR

Address: Operational Base + offset (0x000b4)

Start address of destination image(Cb/Cr)

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	dst_image_cbcr_mst Destination image data CBCR start address in Memory

IEP_DST_ADDR_CR

Address: Operational Base + offset (0x000b8)

Start address of destination image(Cr)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	dst_image_cr_mst Destination image data CR start address in Memory

IEP_DST_ADDR_Y1

Address: Operational Base + offset (0x000bc)

Start address of destination image(Y)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	dst_image_y_mst Destination image data Y start address in Memory

IEP_DST_ADDR_CBCR1

Address: Operational Base + offset (0x000c0)

Start address of destination image(Cb/Cr)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	dst_image_cbcr_mst Destination image data CbCr start address in Memory

IEP_DST_ADDR_CR1

Address: Operational Base + offset (0x000c4)

Start address of destination image(Cr)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	dst_image_cr_mst Destination image data Cr start address in Memory

IEP_DST_ADDR_Y_ITEMP

Address: Operational Base + offset (0x000c8)

Start address of destination image(Y integer part)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	dst_image_y_mst_itemp Interger part destination image data Y start address in Memory

IEP_DST_ADDR_CBCR_ITEMP

Address: Operational Base + offset (0x000cc)

Start address of destination image(CBCR integer part)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	dst_image_cbcr_mst_itemp Int part destination image data CBCR start address in Memory

IEP_DST_ADDR_CR_ITEMP

Address: Operational Base + offset (0x000d0)

Start address of destination image(CR integer part)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	dst_image_cr_mst_itemp Interger part destination image data CR start address in Memory

IEP_DST_ADDR_Y_FTEMP

Address: Operational Base + offset (0x000d4)

Start address of destination image(Y fraction part)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	dst_image_y_mst_ftemp Fraction part destination image data Y start address in Memory

IEP_DST_ADDR_CBCR_FTEMP

Address: Operational Base + offset (0x000d8)

Start address of destination image(CBCR fraction part)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	dst_image_cbcr_mst_ftemp Fraction part destination image data CBCR start address in Mem

IEP_DST_ADDR_CR_FTEMP

Address: Operational Base + offset (0x000dc)

Start address of destination image(CR fraction part)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	dst_image_cr_mst_ftemp Fraction part destination image data CR start address

IEP_DIL_MTN_TAB0

Address: Operational Base + offset (0x000e0)

Deinterlace motion table0

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved

Bit	Attr	Reset Value	Description
30:24	RW	0x00	mtn_sub_tab3 motion sub table3
23	RO	0x0	reserved
22:16	RW	0x00	mtn_sub_tab2 motion sub table2
15	RO	0x0	reserved
14:8	RW	0x00	mtn_sub_tab1 motion sub table1
7	RO	0x0	reserved
6:0	RW	0x00	mtn_sub_tab0 motion sub table0

IEP_DIL_MTN_TAB1

Address: Operational Base + offset (0x000e4)

Deinterlace motion table1

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x00	mtn_sub_tab3 motion sub table3
23	RO	0x0	reserved
22:16	RW	0x00	mtn_sub_tab2 motion sub table2
15	RO	0x0	reserved
14:8	RW	0x00	mtn_sub_tab1 motion sub table1
7	RO	0x0	reserved
6:0	RW	0x00	mtn_sub_tab0 motion sub table0

IEP_DIL_MTN_TAB2

Address: Operational Base + offset (0x000e8)

Deinterlace motion table2

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x00	mtn_sub_tab3 motion sub table3
23	RO	0x0	reserved
22:16	RW	0x00	mtn_sub_tab2 motion sub table2
15	RO	0x0	reserved
14:8	RW	0x00	mtn_sub_tab1 motion sub table1
7	RO	0x0	reserved

Bit	Attr	Reset Value	Description
6:0	RW	0x00	mtn_sub_tab0 motion sub table0

IEP_DIL_MTN_TAB3

Address: Operational Base + offset (0x000ec)

Deinterlace motion table3

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x00	mtn_sub_tab3 motion sub table3
23	RO	0x0	reserved
22:16	RW	0x00	mtn_sub_tab2 motion sub table2
15	RO	0x0	reserved
14:8	RW	0x00	mtn_sub_tab1 motion sub table1
7	RO	0x0	reserved
6:0	RW	0x00	mtn_sub_tab0 motion sub table0

IEP_DIL_MTN_TAB4

Address: Operational Base + offset (0x000f0)

Deinterlace motion table4

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x00	mtn_sub_tab3 motion sub table3
23	RO	0x0	reserved
22:16	RW	0x00	mtn_sub_tab2 motion sub table2
15	RO	0x0	reserved
14:8	RW	0x00	mtn_sub_tab1 motion sub table1
7	RO	0x0	reserved
6:0	RW	0x00	mtn_sub_tab0 motion sub table0

IEP_DIL_MTN_TAB5

Address: Operational Base + offset (0x000f4)

Deinterlace motion table5

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x00	mtn_sub_tab3 motion sub table3

Bit	Attr	Reset Value	Description
23	RO	0x0	reserved
22:16	RW	0x00	mtn_sub_tab2 motion sub table2
15	RO	0x0	reserved
14:8	RW	0x00	mtn_sub_tab1 motion sub table1
7	RO	0x0	reserved
6:0	RW	0x00	mtn_sub_tab0 motion sub table0

IEP_DIL_MTN_TAB6

Address: Operational Base + offset (0x000f8)

Deinterlace motion table6

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x00	mtn_sub_tab3 motion sub table3
23	RO	0x0	reserved
22:16	RW	0x00	mtn_sub_tab2 motion sub table2
15	RO	0x0	reserved
14:8	RW	0x00	mtn_sub_tab1 motion sub table1
7	RO	0x0	reserved
6:0	RW	0x00	mtn_sub_tab0 motion sub table0

IEP_DIL_MTN_TAB7

Address: Operational Base + offset (0x000fc)

Deinterlace motion table7

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x00	mtn_sub_tab3 motion sub table3
23	RO	0x0	reserved
22:16	RW	0x00	mtn_sub_tab2 motion sub table2
15	RO	0x0	reserved
14:8	RW	0x00	mtn_sub_tab1 motion sub table1
7	RO	0x0	reserved
6:0	RW	0x00	mtn_sub_tab0 motion sub table0

IEP_ENH(CG)_TAB

Address: Operational Base + offset (0x00100)
 contrast and gamma enhancement table

Bit	Attr	Reset Value	Description
31:24	RW	0x00	cg_tab_3 cg table 3 pixel value 3,7,11,15,.....mapping
23:16	RW	0x00	cg_tab_2 cg table 2 pixel value 2,6,10,14,.....mapping
15:8	RW	0x00	cg_tab_1 cg table 1 pixel value 1,5,9,13,.....mapping
7:0	RW	0x00	cg_tab_0 cg table 0 256x8bit contrast & gamma mapping table pixel value 0,4,8,12,.....mapping

IEP_ENH(DDE_COE0)

Address: Operational Base + offset (0x00400)
 denoise,detail and edge enhancement coefficient

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:24	RW	0x00	dde_coe_3 dde coefficient 3 coefficient number 3,7,11,15,.....
23:22	RO	0x0	reserved
21:16	RW	0x00	dde_coe_2 dde coefficient 2 coefficient number 2,6,10,14,.....
15:14	RO	0x0	reserved
13:8	RW	0x00	dde_coe_1 dde coefficient 1 coefficient number 1,5,9,13,.....
7:6	RO	0x0	reserved
5:0	RW	0x00	dde_coe_0 dde coefficient 0 256x6bit coefficient for denoise and detail enhancement coefficient number 0,4,8,12,.....

IEP_ENH(DDE_COE1)

Address: Operational Base + offset (0x00500)
 denoise,detail and edge enhancement coefficient

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:24	RW	0x00	dde_coe_3 dde coefficient 3 coefficient number 3,7,11,15,.....
23:22	RO	0x0	reserved
21:16	RW	0x00	dde_coe_2 dde coefficient 3 coefficient number 2,6,10,14,.....
15:14	RO	0x0	reserved
13:8	RW	0x00	dde_coe_1 dde coefficient 1 coefficient number 1,5,9,13,.....
7:6	RO	0x0	reserved
5:0	RW	0x00	dde_coe_0 dde coefficient 1 81x6bit coefficient for denoise and detail enhancement coefficient number 0,4,8,12,.....

IEP_MMU_DTE_ADDR

Address: Operational Base + offset (0x00800)

MMU current page table address

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	mmu_dte_addr page table address

IEP_MMU_STATUS

Address: Operational Base + offset (0x00804)

MMU status register

Bit	Attr	Reset Value	Description
31:11	RO	0x0	reserved
10:6	RW	0x00	mmu_page_fault_bus_id Index of master responsible for the last page fault
5	RW	0x0	mmu_page_fault_is_write The direction of access for last page fault: 0: read 1:write
4	RW	0x1	mmu_replay_buffer_empty The MMU replay buffer is empty.

Bit	Attr	Reset Value	Description
3	RW	0x1	mmu_idle the MMU is idle when accesses are being translated and there are no unfinished translated access. The MMU_IDLE signal only reports idle when the MMU processor is idle and accesses are active on the external bus. Note: the MMU can be idle in page fault mode.
2	RW	0x0	mmu_stall_active MMU stall mode currently enabled. The mode is enabled by command.
1	RW	0x0	mmu_page_fault_active MMU page fault mode currently enabled. The mode is enabled by command
0	RW	0x0	mmu_paging_enabled mmu paging is enabled

IEP_MMU_CMD

Address: Operational Base + offset (0x00808)

MMU command register

Bit	Attr	Reset Value	Description
31:3	RO	0x0	reserved
2:0	RW	0x0	mmu_cmd 0: MMU_ENABLE_PAGING. enable paging. 1: MMU_DISABLE_PAGING. disable paging. 2: MMU_ENABLE_STALL. turn on stall mode. 3: MMU_DISABLE_STALL. turn off stall mode. 4: MMU_ZAP_CACHE. zap the entire page table cache. 5: MMU_PAGE_FAULT_DONE. leave page fault mode. 6: MMU_FORCE_RESET. reset the mmu. The MMU_ENABLE_STALL command can always be issued. Other commands are ignored unless the MMU is idle or stalled.

IEP_MMU_PAGE_FAULT_ADDR

Address: Operational Base + offset (0x0080c)

MMU logic address of last page fault

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	mmu_page_fault_addr address of last page fault

IEP_MMU_ZAP_ONE_LINE

Address: Operational Base + offset (0x00810)

MMU zap cache line register

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	mmu_zap_one_line address to be invalidated from the page table cache.

IEP_MMU_INT_RAWSTAT

Address: Operational Base + offset (0x00814)

MMU raw interrupt status register

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	RW	0x0	read_bus_error read bus error
0	RW	0x0	page_fault page fault

IEP_MMU_INT_CLEAR

Address: Operational Base + offset (0x00818)

MMU interrupt clear register

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	RW	0x0	read_bus_error_clear read bus error interrupt clear. write 1 to this register can clear read bus error interrupt.
0	RW	0x0	page_fault_clear page fault interrupt clear, write 1 to this register can clear page fault interrupt.

IEP_MMU_INT_MASK

Address: Operational Base + offset (0x0081c)

MMU interrupt mask register

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	RW	0x0	read_bus_error_int_en read bus error interrupt enable
0	RW	0x0	page_fault_int_en page fault interrupt enable

IEP_MMU_INT_STATUS

Address: Operational Base + offset (0x00820)

MMU interrupt status register

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	RW	0x0	read_bus_error read bus error interrupt
0	RW	0x0	page_fault page fault interrupt

IEP_MMU_AUTO_GATING

Address: Operational Base + offset (0x00824)

MMU clock auto gating register

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x1	mmu_auto_gating mmu clock auto gating when it is 1, the mmu will auto gating itself

17.5 Application Notes

17.5.1 VOP path disabled configure flow

1. Keep IEP direct path disabled.
2. Configure all registers which are needed at any time.
3. Configure IEP_CONFIG_DONE.
4. Configure IEP_FRM_START.

17.5.2 VOP path enabled configure flow

1. Keep IEP direct path enabled.
2. Configure all IEP registers which are needed.
3. Configure VOP related registers which are needed.
4. Configure CONFIG_DONE register in VOP only.
5. Wait for frame start from VOP and IEP direct path.

17.5.3 VOP path turn on flow

1. Configure all IEP registers which are needed.
2. Configure VOP related registers which are needed.
3. Enable IEP direct path.
4. Enable VOP direct path.
5. Configure CONFIG_DONE register in VOP only.
6. Wait for frame start from VOP and IEP direct path.

17.5.4 VOP path turn off flow

1. Disable VOP direct path.
2. Disable IEP direct path, so IEP do not receive any other CONFIG_DONE and frame start from VOP immediately.
3. Configure CONFIG_DONE register in VOP.
4. Wait for frame start from VOP and IEP direct path, so VOP quit direct path mode completely.
5. Configure IEP registers which are needed at any time.
6. Configure IEP_CONFIG_DONE.
7. Configure IEP_FRM_START, IEP is working at write back mode now.

Chapter 18 Video Input Processor (VIP)

18.1 Overview

The Video Input Processor, receives the data from Camera or CCIR656 encoder, and transfers the data into system main memory by AXI bus.

The Video Input Processor supports following features:

- Support YCbCr422 input
- Support Raw8bit input
- Support CCIR656(PAL/NTSC) input
- Support JPEG input
- Support YCbCr422/420 output
- Support UYVY/VYUY/YUYV/YVYU configurable
- Support up to 8192x8192 resolution source
- Support picture in picture
- Support arbitrary size window crop
- Support error/terminate interrupt and combined interrupt output
- Support clk/vsync/href polarity configurable
- Support one frame stop/ping-pong mode

18.2 Block Diagram

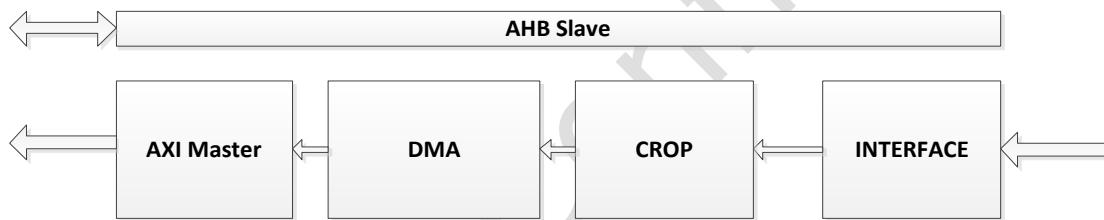


Fig. 18-1 VIP block diagram

The VIP comprises with:

- AHB Slave
Host configure the registers via the AHB Slave
- AXI Master
Transmit the data to chip memory via the AXI Master
- INTERFACE
Translate the input video data into the requisite data format
- CROP
Bypass or crop the source video data to a smaller size destination
- DMA
Control the operation of AXI Master

18.3 Function description

This chapter is used to illustrate the operational behavior of how VIP works. If YUV422 or ccir656 signal is received from external devices, VIP translate it into YUV422/420 data, and separate the data to Y and UV data, then store them to different memory via AXI bus separately. But if raw data is received, there are not any translations happened, the 8 data is considered as 16bit data and write directly to memory.

18.3.1 Support Vsync high active or low active

Vsync Low active as below

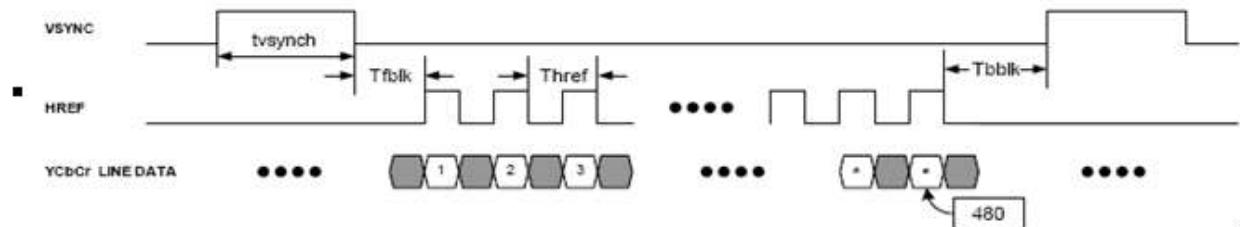
Vertical sensor timing (line by line)

Fig. 18-2 Timing diagram for VIP when vsync low active

Vsync High active

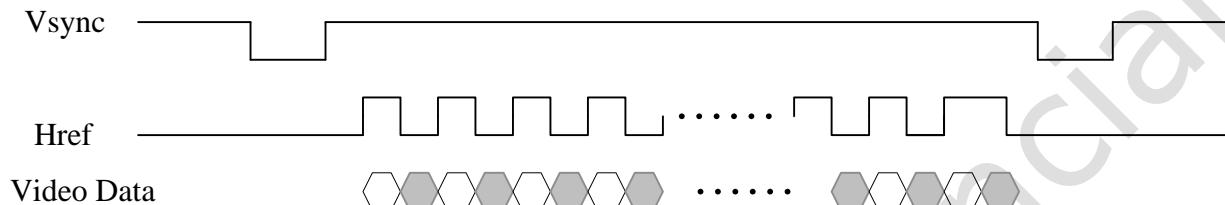


Fig. 18-3 Timing diagram for VIP when vsync high active

18.3.2 Support href high active or low active

Href high active

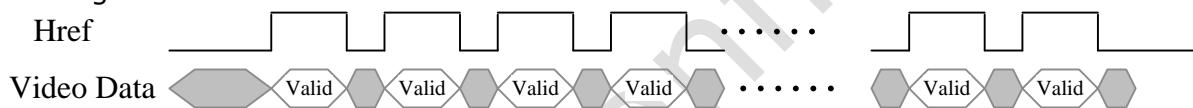


Fig. 18-4 Timing diagram for VIP when href high active

Href Low active

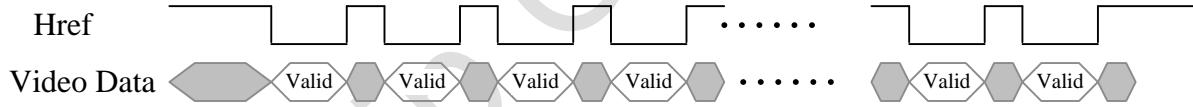


Fig. 18-5 Timing diagram for VIP when href low active

Y first

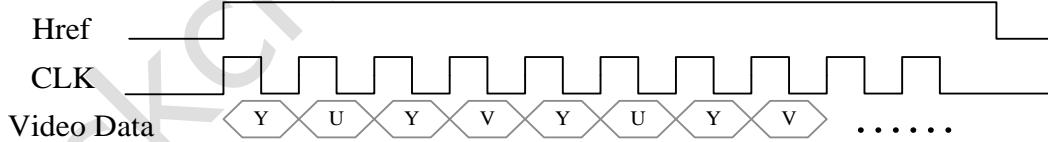


Fig. 18-6 Timing diagram for VIP when Y data first

U first

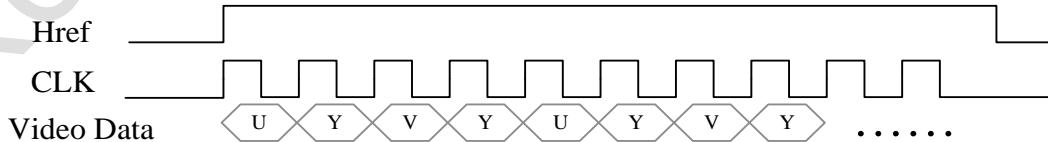


Fig. 18-7 Timing diagram for VIP when U data first

18.3.3 Support CCIR656 (NTSC and PAL)

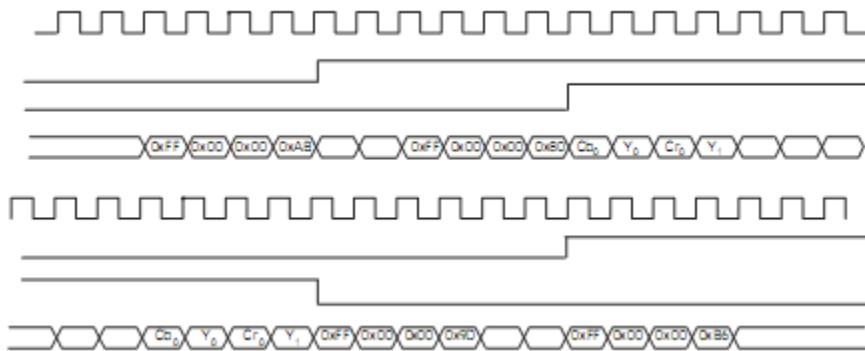


Fig. 18-8 CCIR656 timing

18.3.4 Support Raw data (8-bit) or JPEG

Pixel Data Timing Example

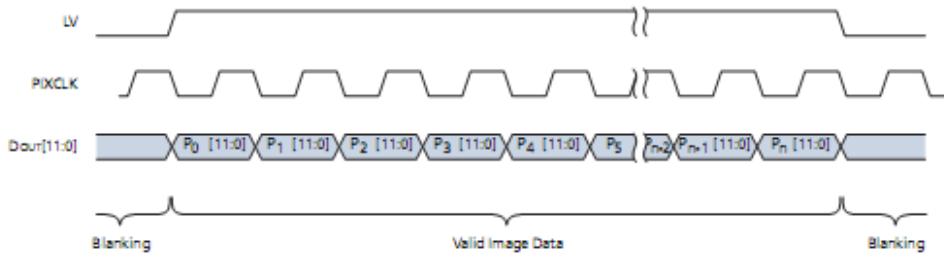


Fig. 18-9 Raw Data or JPEG Timing

VIP module can work in three modes: one frame stop mode, ping-pong mode.

One frame stop mode

In this mode, configure the parameter WORK_MODE to one frame stop mode. After one frame captured, VIP will automatic stop. After capturing, the image Y, UV data will be stored at main memory location defined by VIP_FRM0_ADDR_Y, FRM0_ADDR_UV separately.

Ping-Pong mode

After one frame(F1) captured, VIP will start to capture the next frame(F2) automatically, and host must assign new address pointer of frame1 and clear the frame1 status, thus VIP will capture the third frame automatically(by new F1 address) without any stop and so on for the following frames. But if host did not update the frame buffer address, the VIP will cover the pre-frame data stored in the memory with the following frame data.

Storage

Difference between the YUV mode and raw mode is that in the YUV mode or ccir656 mode, data will be storage in the Y data buffer and UV data buffer; but in the raw or jpeg mode, RGB data will be storage in the same buffer. In addition, in the yuv mode, the width of Y, U or V data is a byte in memory; in Raw or JPEG mode, the width is a halfword no matter the data source is 8 bit.

CROP

The parameter START_Y and START_X defines the coordinate of crop start point. And the frame size after cropping is following the value of SET_WIDTH and SET_HEIGHT.

18.4 Register description

18.4.1 Register Summary

Name	Offset	Size	Reset Value	Description
VIP_CTRL	0x00000	W	0x00007000	VIP control

Name	Offset	Size	Reset Value	Description
VIP_INTEN	0x00004	W	0x00000000	VIP interrupt status
VIP_INTSTAT	0x00008	W	0x00000000	VIP interrupt status
VIP_FOR	0x0000c	W	0x00000000	VIP format
VIP_FRM0_ADDR_Y	0x00014	W	0x00000000	VIP frame0 y address
VIP_FRM0_ADDR_UV	0x00018	W	0x00000000	VIP frame0 uv address
VIP_FRM1_ADDR_Y	0x0001c	W	0x00000000	VIP frame1 y address
VIP_FRM1_ADDR_UV	0x00020	W	0x00000000	VIP frame1 uv address
VIP_VIR_LINE_WIDTH	0x00024	W	0x00000000	VIP virtual line width
VIP_SET_SIZE	0x00028	W	0x01e002d0	VIP frame set size
VIP_CROP	0x00044	W	0x00000000	VIP crop start point
VIP_SCL_CTRL	0x00048	W	0x00000000	VIP scale control
VIP_FIFO_ENTRY	0x00054	W	0x00000000	VIP FIFO entry
VIP_FRAME_STATUS	0x00060	W	0x00000000	VIP frame status
VIP_CUR_DST	0x00064	W	0x00000000	VIP current destination address
VIP_LAST_LINE	0x00068	W	0x00000000	VIP last frame line number
VIP_LAST_PIX	0x0006c	W	0x00000000	VIP last line pixel number

Notes: **S**ize : **B** - Byte (8 bits) access, **HW** - Half WORD (16 bits) access, **W**-WORD (32 bits) access

18.4.2 Detail Register Description

VIP_CTRL

Address: Operational Base + offset (0x00000)

VIP control

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:12	RW	0x7	AXI_BURST_TYPE axi master burst type 0-15 : burst1~16
11:3	RO	0x0	reserved
2:1	RW	0x0	WORK_MODE Working Mode 00 : one frame stop mode 01 : ping-pong mode 02 : line loop mode 03 : reserved
0	RW	0x0	CAP_EN capture enable 0 : disable 1 : enable

VIP_INTEN

Address: Operational Base + offset (0x00004)

VIP interrupt status

Bit	Attr	Reset Value	Description
31:10	RO	0x0	reserved

Bit	Attr	Reset Value	Description
9	RW	0x0	PST_INF_FRAME_END_EN frame end after interface FIFO interrupt enable 0 : disable 1 : enable
8	RW	0x0	PRE_INF_FRAME_END_EN frame end before interface FIFO interrupt enable 0 : disable 1 : enable
7	RO	0x0	reserved
6	W1C	0x0	BUS_ERR_EN axi master or ahb slave response error interrupt enable 0 : disable 1 : enable
5	RW	0x0	DFIFO_OF_EN DMA FIFO overflow interrupt enable 0 : disable 1 : enable
4	RW	0x0	IFIFO_OF_EN interface FIFO overflow interrupt enable 0 : disable 1 : enable
3	W1C	0x0	PIX_ERR_EN the pixel number of last line not equal to the set height interrupt enable 0 : disable 1 : enable
2	W1C	0x0	LINE_ERR_EN the line number of last frame not equal to the set height interrupt enable 0 : disable 1 : enable
1	W1C	0x0	LINE_END_EN line end interrupt enable 0 : disable 1 : enable
0	W1C	0x0	DMA_FRAME_END_EN dma frame end interrupt enable 0 : disable 1 : enable

VIP_INTSTAT

Address: Operational Base + offset (0x000008)

VIP interrupt status

Bit	Attr	Reset Value	Description
31:10	RO	0x0	reserved
9	RW	0x0	PST_INF_FRAME_END frame end after interface FIFO interrupt 0 : no interrupt 1 : interrupt
8	RW	0x0	PRE_INF_FRAME_END frame end before interface FIFO interrupt 0 : no interrupt 1 : interrupt
7	RO	0x0	reserved
6	W1C	0x0	BUS_ERR axi master or ahb slave response error interrupt 0 : no interrupt 1 : interrupt
5	RW	0x0	DFIFO_OF DMA FIFO overflow interrupt 0 : no interrupt 1 : interrupt
4	RW	0x0	IFIFO_OF interface FIFO overflow interrupt 0 : no interrupt 1 : interrupt
3	W1C	0x0	PIX_ERR the pixel number of last line not equal to the set height interrupt 0 : no interrupt 1 : interrupt
2	W1C	0x0	LINE_ERR the line number of last frame not equal to the set height interrupt 0 : no interrupt 1 : interrupt
1	W1C	0x0	LINE_END line end interrupt 0 : no interrupt 1 : interrupt
0	W1C	0x0	DMA_FRAME_END dma frame end interrupt 0 : no interrupt 1 : interrupt

VIP_FOR

Address: Operational Base + offset (0x0000c)

VIP format

Bit	Attr	Reset Value	Description
31:20	RO	0x0	reserved
19	RW	0x0	UV_STORE_ORDER UV storage order 0 : UVUV 1 : VUVU
18	RW	0x0	RAW_END raw data endian 0 : little end 1 : big end
17	RW	0x0	OUT_420_ORDER output 420 order 0 : UV in the even line 1 : UV in the odd line Note: The first line is even line(line 0).
16	RW	0x0	OUTPUT_420 output 420 or 422 0 : output is 422 1 : output is 420
15	RO	0x0	reserved
14:13	RW	0x0	MIPI_MODE mipi mode 00 : 32 bit bypass mode; 01 : rgb mode; 10 : yuv mode; 11 : reserve;
12:11	RW	0x0	RAW_WIDTH raw data width 00 : 8bit raw data; 01 : 10bit raw data; 10 : 12bit raw data; 11 : reserve;
10	RW	0x0	JPEG_MODE JPEG mode 0 : other mode 1 : mode1
9	RW	0x0	FIELD_ORDER ccir input order 0 : odd field first 1 : even field first
8	RW	0x0	IN_420_ORDER 420 input order 0 : UV in the even line 1 : UV in the odd line Note: The first line is even line(line 0).

Bit	Attr	Reset Value	Description
7	RW	0x0	INPUT_420 input 420 or 422 0 : 422 1 : 420
6:5	RW	0x0	YUV_IN_ORDER YUV input order 00 : UYVY 01 : YVYU 10 : VYUY 11 : YUYV
4:2	RW	0x0	INPUT_MODE input mode 000 : YUV 010 : PAL 011 : NTSC 100 : RAW 101 : JPEG 110 : MIPI Other : invalid
1	RW	0x0	HREF_POL href input polarity 0 : high active 1 : low active
0	RW	0x0	VSYNC_POL vsync input polarity 0 : low active 1 : high active

VIP_FRM0_ADDR_Y

Address: Operational Base + offset (0x00014)

VIP frame0 y address

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	FRM0_ADDR_Y frame0 y address

VIP_FRM0_ADDR_UV

Address: Operational Base + offset (0x00018)

VIP frame0 uv address

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	FRM0_ADDR_UV frame0 uv address

VIP_FRM1_ADDR_Y

Address: Operational Base + offset (0x0001c)

VIP frame1 y address

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	FRM1_ADDR_Y frame1 y address

VIP_FRM1_ADDR_UV

Address: Operational Base + offset (0x00020)

VIP frame1 uv address

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	FRM1_ADDR_UV frame1 uv address

VIP_VIR_LINE_WIDTH

Address: Operational Base + offset (0x00024)

VIP virtual line width

Bit	Attr	Reset Value	Description
31:15	RO	0x0	reserved
14:0	RW	0x0000	VIR_LINE_WIDTH virtual line width

VIP_SET_SIZE

Address: Operational Base + offset (0x00028)

VIP frame set size

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x01e0	SET_HEIGHT set height
15:13	RO	0x0	reserved
12:0	RW	0x02d0	SET_WIDTH set width

VIP_CROP

Address: Operational Base + offset (0x00044)

VIP crop start point

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	START_Y start y point
15:13	RO	0x0	reserved
12:0	RW	0x0000	START_X start x point

VIP_SCL_CTRL

Address: Operational Base + offset (0x00048)

VIP scale control

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:7	RO	0x0	reserved
6	RW	0x0	MIPI_32B_BP mipi 32 bit bypass 0 : no bypass 1 : bypass
5	RW	0x0	RAW_16B_BP raw 16 bit bypass 0 : no bypass 1 : bypass
4	RW	0x0	YUV_16B_BP YUV 16 bit bypass 0 : no bypass 1 : bypass
3:0	RO	0x0	reserved

VIP_FIFO_ENTRY

Address: Operational Base + offset (0x00054)

VIP FIFO entry

Bit	Attr	Reset Value	Description
31:18	RO	0x0	reserved
17:9	RW	0x000	UV_FIFO_ENTRY valid UV double word in FIFO write 0 clear
8:0	RO	0x000	Y_FIFO_ENTRY valid Y double word in FIFO write 0 clear

VIP_FRAME_STATUS

Address: Operational Base + offset (0x00060)

VIP frame status

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	FRAME_NUM complete frame number write 0 to clear
15:2	RO	0x0	reserved
1	RO	0x0	F1_STS frame 0 status 0 : frame 1 not ready 1 : frame 1 ready write 0 clear
0	RO	0x0	F0_STS frame 0 status 0 : frame 0 not ready 1 : frame 0 ready write 0 clear

VIP_CUR_DST

Address: Operational Base + offset (0x00064)

VIP current destination address

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	CUR_DST current destination address maybe not the current, because the clock synchronization.

VIP_LAST_LINE

Address: Operational Base + offset (0x00068)

VIP last frame line number

Bit	Attr	Reset Value	Description
31:13	RO	0x0	reserved
12:0	RO	0x0000	LAST_LINE_NUM line number of last frame

VIP_LAST_PIX

Address: Operational Base + offset (0x0006c)

VIP last line pixel number

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	LAST_UV_NUM y number of last line
15:13	RO	0x0	reserved
12:0	RO	0x0000	LAST_Y_NUM y number of last line

18.5 Interface description

Module Pin	Direction	Pad Name	IOMUX Setting
vip_clko ut	O	IO_CIFclkin_HOSTwkack_GPSclk_HSADCc Ikout_DVPgpio2b2	GRF_GPIO2B_MUX[5:4]==2'b1
vip_clki n	I	IO_CIFclkout_HOSTwkreq_HSADCTSfail_DVPgpio2b3	GRF_GPIO2B_MUX[7:6]==2'b1
vip_href	I	IO_CIFhref_HOSTdin7_HSADCTSvalid_DV Pgpio2b1	GRF_GPIO2B_MUX[3:2]==2'b1
vip_vsyn c	I	IO_CIFvsync_HOSTdin6_HSADCTSsync_D VPgpio2b0	GRF_GPIO2B_MUX[1:0]==2'b1
vip_dat a0	I	IO_CIFdata0_DVPgpio2b4	GRF_GPIO2B_MUX[9:8]==2'b1
vip_dat a1	I	IO_CIFdata1_DVPgpio2b5	GRF_GPIO2B_MUX[11:10]==2'b1
vip_dat a2	I	IO_CIFdata2_HOSTdin0_HSADCdata0_DV Pgpio2a0	GRF_GPIO2A_MUX[1:0]==2'b1
vip_dat a3	I	IO_CIFdata3_HOSTdin1_HSADCdata1_DV Pgpio2a1	GRF_GPIO2A_MUX[3:2]==2'b1

vip_dat_a4	I	IO_CIFdata4_HOSTdin2_HSADCdata2_DV Pgpio2a2	GRF_GPIO2A_MUX[5:4]==2'b1
vip_dat_a5	I	IO_CIFdata5_HOSTdin3_HSADCdata3_DV Pgpio2a3	GRF_GPIO2A_MUX[7:6]==2'b1
vip_dat_a6	I	IO_CIFdata6_HOSTckinp_HSADCdata4_D VPgpio2a4	GRF_GPIO2A_MUX[9:8]==2'b1
vip_dat_a7	I	IO_CIFdata7_HOSTckinn_HSADCdata5_D VPgpio2a5	GRF_GPIO2A_MUX[11:10]==2'b1
vip_dat_a8	I	IO_CIFdata8_HOSTdin4_HSADCdata6_DV Pgpio2a6	GRF_GPIO2A_MUX[13:12]==2'b1
vip_dat_a9	I	IO_CIFdata9_HOSTdin5_HSADCdata7_DV Pgpio2a7	GRF_GPIO2A_MUX[15:14]==2'b1
vip_dat_a10	I	IO_CIFdata10_DVPgpio2b6	GRF_GPIO2B_MUX[13:12]==2'b1
vip_dat_a11	I	IO_CIFdata11_DVPgpio2b7	GRF_GPIO2B_MUX[15:14]==2'b1

18.6 Application Notes

The biggest configuration requirement of all operations is the CAP_EN bit must be set after all the mode selection is ready. The configuration order of the input/output data format, YUV order, the address, frame size/width, AXI burst length and other options do not need to care.

There are many debug registers to make it easy to read the internal operation information of VIP. The valid pixel number of scale result in FIFO can be known by read VIP_SCL_VALID_NUM. The line number of last frame and the pixel number of last line can be also known by read the VIP_LAST_LINE and VIP_LAST_PIX.

Chapter 19 Encryption and Decryption (Crypto)

19.1 Overview

Crypto is a hardware accelerator of encrypting or decrypting. It supports the most commonly used algorithm: DES/3DES, AES, SHA1, SHA256, MD5 and RSA.

The Crypto supports following features:

- Support AES 128/192/256 bits key mode, ECB/CBC/CTR chain mode, Slave/FIFO mode
- Support DES/3DES (ECB and CBC chain mode), 3DES (EDE/ EEE key mode), Slave/FIFO mode

- Support SHA1/SHA256/MD5 (with hardware padding) HASH function, FIFO mode only

- Support 160 bit Pseudo Random Number Generator (PRNG)

- Support PKA 512/1024/2048 bit Exp Modulator

- Support up to 150M clock frequency

19.2 Block Diagram

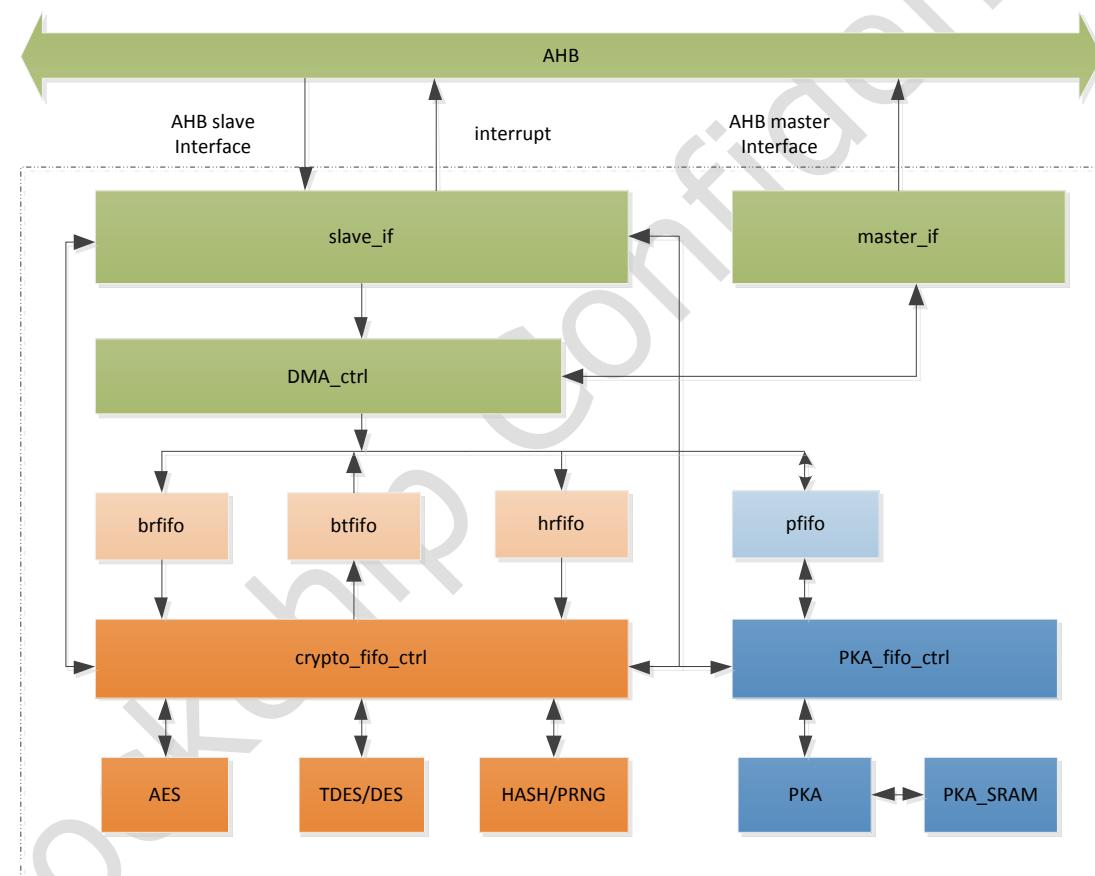


Fig. 19-1 Crypto Architecture

Figure above shows the architecture of Crypto.

19.3 Register description

19.3.1 Register Summary

Name	Offset	Size	Reset Value	Description
CRYPTO_INTSTS	0x0000	W	0x00000000	Interrupt Status Register

Name	Offset	Size	Reset Value	Description
CRYPTO_INTENA	0x0004	W	0x00000000	Interrupt Set Register
CRYPTO_CTRL	0x0008	W	0x00000000	Control Register
CRYPTO_CONF	0x000c	W	0x00000000	
CRYPTO_BRDMAS	0x0010	W	0x00000000	Block Receiving DMA Start Address Register
CRYPTO_BTDMAS	0x0014	W	0x00000000	Block Transmiting DMA Start Address Register
CRYPTO_BRDMAL	0x0018	W	0x00000000	Block Receiving DMA Length Register
CRYPTO_HRDMAS	0x001c	W	0x00000000	Hash Receiving DMA Start Address Register
CRYPTO_HRDMAL	0x0020	W	0x00000000	Hash Receiving DMA Length Register
CRYPTO_AES_CTRL	0x0080	W	0x00000000	AES Control Register
CRYPTO_AES_STS	0x0084	W	0x00000000	Status Register
CRYPTO_AES_DIN_0	0x0088	W	0x00000000	AES Input Data 0 Register
CRYPTO_AES_DIN_1	0x008c	W	0x00000000	AES Input Data 1 Register
CRYPTO_AES_DIN_2	0x0090	W	0x00000000	AES Input Data 2 Register
CRYPTO_AES_DIN_3	0x0094	W	0x00000000	AES Input Data 3 Register
CRYPTO_AES_DOUT_0	0x0098	W	0x00000000	AES Output Data 0 Register
CRYPTO_AES_DOUT_1	0x009c	W	0x00000000	AES Output Data 1 Register
CRYPTO_AES_DOUT_2	0x00a0	W	0x00000000	AES Output Data 2 Register
CRYPTO_AES_DOUT_3	0x00a4	W	0x00000000	AES Output Data 3 Register
CRYPTO_AES_IV_0	0x00a8	W	0x00000000	AES IV data 0 Register
CRYPTO_AES_IV_1	0x00ac	W	0x00000000	AES IV data 1 Register
CRYPTO_AES_IV_2	0x00b0	W	0x00000000	AES IV data 2 Register
CRYPTO_AES_IV_3	0x00b4	W	0x00000000	AES IV data 3 Register
CRYPTO_AES_KEY_0	0x00b8	W	0x00000000	AES Key data 0 Register
CRYPTO_AES_KEY_1	0x00bc	W	0x00000000	AES Key data 1 Register
CRYPTO_AES_KEY_2	0x00c0	W	0x00000000	AES Key data 2 Register
CRYPTO_AES_KEY_3	0x00c4	W	0x00000000	AES Key data 3 Register
CRYPTO_AES_KEY_4	0x00c8	W	0x00000000	AES Key data 4 Register
CRYPTO_AES_KEY_5	0x00cc	W	0x00000000	AES Key data 5 Register
CRYPTO_AES_KEY_6	0x00d0	W	0x00000000	AES Key data 6 Register
CRYPTO_AES_KEY_7	0x00d4	W	0x00000000	AES Key data 7 Register
CRYPTO_AES_CNT_0	0x00d8	W	0x00000000	AES Input Counter 0 Register
CRYPTO_AES_CNT_1	0x00dc	W	0x00000000	AES Input Counter 1 Register
CRYPTO_AES_CNT_2	0x00e0	W	0x00000000	AES Input Counter 2 Register
CRYPTO_AES_CNT_3	0x00e4	W	0x00000000	AES Input Counter 3 Register
CRYPTO_TDES_CTRL	0x0100	W	0x00000000	TDES Control Register
CRYPTO_TDES_STS	0x0104	W	0x00000000	Status Register
CRYPTO_TDES_DIN_0	0x0108	W	0x00000000	TDES Input Data 0 Register
CRYPTO_TDES_DIN_1	0x010c	W	0x00000000	TDES Input Data 1 Register
CRYPTO_TDES_DOUT_0	0x0110	W	0x00000000	TDES Output Data 0 Register

Name	Offset	Size	Reset Value	Description
CRYPTO_TDES_DOUT_1	0x0114	W	0x00000000	TDES Output Data 1 Register
CRYPTO_TDES_IV_0	0x0118	W	0x00000000	TDES IV data 0 Register
CRYPTO_TDES_IV_1	0x011c	W	0x00000000	TDES IV data 1 Register
CRYPTO_TDES_KEY1_0	0x0120	W	0x00000000	TDES Key1 data 1 Register
CRYPTO_TDES_KEY1_1	0x0124	W	0x00000000	TDES Key1 data 1 Register
CRYPTO_TDES_KEY2_0	0x0128	W	0x00000000	TDES Key2 data 0 Register
CRYPTO_TDES_KEY2_1	0x012c	W	0x00000000	TDES Key2 data 1 Register
CRYPTO_TDES_KEY3_0	0x0130	W	0x00000000	TDES Key3 data 0 Register
CRYPTO_TDES_KEY3_1	0x0134	W	0x00000000	TDES Key3 data 1 Register
CRYPTO_HASH_CTRL	0x0180	W	0x00000000	Hash Control Register
CRYPTO_HASH_STS	0x0184	W	0x00000000	Hash Status Register
CRYPTO_HASH_MSG_LEN	0x0188	W	0x00000000	Hash Message Len
CRYPTO_HASH_DOUT_0	0x018c	W	0x00000000	Hash Result Register 0
CRYPTO_HASH_DOUT_1	0x0190	W	0x00000000	Hash Result Register 1
CRYPTO_HASH_DOUT_2	0x0194	W	0x00000000	Hash Result Register 2
CRYPTO_HASH_DOUT_3	0x0198	W	0x00000000	Hash Result Register 3
CRYPTO_HASH_DOUT_4	0x019c	W	0x00000000	Hash Result Register 4
CRYPTO_HASH_DOUT_5	0x01a0	W	0x00000000	Hash Result Register 4
CRYPTO_HASH_DOUT_6	0x01a4	W	0x00000000	Hash Result Register 6
CRYPTO_HASH_DOUT_7	0x01a8	W	0x00000000	Hash Result Register 7
CRYPTO_HASH_SEED_0	0x01ac	W	0x00000000	PRNG Seed/HMAC Key Register 0
CRYPTO_HASH_SEED_1	0x01b0	W	0x00000000	PRNG Seed/HMAC Key Register 1
CRYPTO_HASH_SEED_2	0x01b4	W	0x00000000	PRNG Seed/HMAC Key Register 2
CRYPTO_HASH_SEED_3	0x01b8	W	0x00000000	PRNG Seed/HMAC Key Register 3
CRYPTO_HASH_SEED_4	0x01bc	W	0x00000000	PRNG Seed/HMAC Key Register 4
CRYPTO_TRNG_CTRL	0x0200	W	0x00000000	TRNG Control
CRYPTO_TRNG_DOUT_0	0x0204	W	0x00000000	TRNG Output Data 0
CRYPTO_TRNG_DOUT_1	0x0208	W	0x00000000	TRNG Output Data 1
CRYPTO_TRNG_DOUT_2	0x020c	W	0x00000000	TRNG Output Data 2
CRYPTO_TRNG_DOUT_3	0x0210	W	0x00000000	TRNG Output Data 3
CRYPTO_TRNG_DOUT_4	0x0214	W	0x00000000	TRNG Output Data 4
CRYPTO_TRNG_DOUT_5	0x0218	W	0x00000000	TRNG Output Data 5
CRYPTO_TRNG_DOUT_6	0x021c	W	0x00000000	TRNG Output Data 6
CRYPTO_TRNG_DOUT_7	0x0220	W	0x00000000	TRNG Output Data 7
CRYPTO_PKA_CTRL	0x0280	W	0x00000000	PKA Control Register
CRYPTO_PKA_M	0x0400	W	0x00000000	
CRYPTO_PKA_C	0x0500	W	0x00000000	
CRYPTO_PKA_N	0x0600	W	0x00000000	
CRYPTO_PKA_E	0x0700	W	0x00000000	

Notes: Size : **B** - Byte (8 bits) access, **HW** - Half WORD (16 bits) access, **W** -WORD (32 bits) access

19.3.2 Detail Register Description

CRYPTO_INTSTS

Address: Operational Base + offset (0x0000)

Interrupt Status Register

Bit	Attr	Reset Value	Description
31:6	RO	0x0	reserved
5	RW	0x0	PKA_DONE_INT PKA Done Interrupt
4	W1C	0x0	HASH_DONE_INT Hash Done Interrupt
3	W1C	0x0	HRDMA_ERR_INT Specifies the interrupt of hash receiving DMA Error
2	W1C	0x0	HRDMA_DONE_INT Specifies the interrupt of hash receiving DMA DONE
1	W1C	0x0	BCDMA_ERR_INT Specifies the interrupt of block cipher Error
0	W1C	0x0	BCDMA_DONE_INT Specifies the interrupt of block cipher DONE

CRYPTO_INTENA

Address: Operational Base + offset (0x0004)

Interrupt Set Register

Bit	Attr	Reset Value	Description
31:6	RO	0x0	reserved
5	RW	0x0	PKA_DONE_ENA Set the interrupt Enable of PKA done 1'b1: enable 1'b0: disable
4	RW	0x0	HASH_DONE_ENA Set the interrupt Enable of hash done 1'b1: enable 1'b0: disable
3	RW	0x0	HRDMA_ERR_ENA Set the interrupt Enable of hash receiving DMA Error 1'b1: enable 1'b0: disable
2	RW	0x0	HRDMA_DONE_ENA Set the interrupt Enable of hash receiving DMA DONE 1'b1: enable 1'b0: disable

Bit	Attr	Reset Value	Description
1	RW	0x0	BCDMA_ERR_ENA Set the interrupt Enable of block cipher DMA Error 1'b1: enable 1'b0: disable
0	RW	0x0	BCDMA_DONE_ENA Set the interrupt Enable of block cipher DMA DONE 1'b1: enable 1'b0: disable

CRYPTO_CTRL

Address: Operational Base + offset (0x0008)

Control Register

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	Write_Mask
15:10	RO	0x0	reserved
9	RW	0x0	TRNG_FLUSH FLUSH TRNG Software write 1 to start. When finishes, the core will clear it.
8	RWSC	0x0	TRNG_START Start TRNG Software write 1 to start. When finishes, the core will clear it.
7	RWSC	0x0	PKA_FLUSH Software write 1 to start Flush Process. The process will clear BRFIFO, BTFIFO, and state machine. Then Software should write 0 to end FLUSH Process
6	RW	0x0	HASH_FLUSH Software write 1 to start Flush Process. The process will clear BRFIFO, BTFIFO, and state machine. Then Software should write 0 to end FLUSH Process
5	RW	0x0	BLOCK_FLUSH Software write 1 to start Flush Process. The process will clear BRFIFO, BTFIFO, and state machine. Then Software should write 0 to end FLUSH Process. It must last for at least 20 cycles to clean registers and FSM
4	RWSC	0x0	PKA_START Starts/initializes PKA Software write 1 to start. When finishes, the core will clear it.

Bit	Attr	Reset Value	Description
3	RWSC	0x0	HASH_START Starts/initializes HASH/PRNG/HMAC Software write 1 to start. When finishes, the core will clear it.
2	RWSC	0x0	BLOCK_START Starts/initializes Block Cipher Software write 1 to start. When finishes, the core will clear it.
1	RWSC	0x0	TDES_START Starts/initializes TDES Software write 1 to start. When finishes, the core will clear it.
0	RWSC	0x0	AES_START Starts/initializes AES Software write 1 to start. When finishes, the core will clear it. Software can also write 0 to clear it.

CRYPTO_CONF

Address: Operational Base + offset (0x000c)

Bit	Attr	Reset Value	Description
31:9	RO	0x0	reserved
8	RW	0x0	HR_ADDR_MODE Hash Receive DMA Address Mode 1'b1: fix 1'b0: increment
7	RW	0x0	BT_ADDR_MODE Block Transmit DMA Address Mode 1'b1: fix 1'b0: increment
6	RW	0x0	BR_ADDR_MODE Block Receive DMA Address Mode 1'b1: fix 1'b0: increment
5	RW	0x0	Byteswap_HRFIFO If this bit is high, then the data read from the bus is byte-swapped in a word boundary. If this bit is low (default), then the data is handed over to the FIFO without byte-swap. For little endian bus, this bit should be 1'b1.

Bit	Attr	Reset Value	Description
4	RW	0x0	Byteswap_BTFIFO If this bit is high, then the data read from the bus is byte-swapped in a word boundary. If this bit is low (default), then the data is handed over to the FIFO without byte-swap. For little endian bus, this bit should be 1'b1.
3	RW	0x0	Byteswap_BRFIFO If this bit is high, then the data read from the bus is byte-swapped in a word boundary. If this bit is low (default), then the data is handed over to the FIFO without byte-swap. For little endian bus, this bit should be 1'b1.
2	RW	0x0	DESSEL Specifies the Destination block cipher of FIFO. AES(=0)/DES(=1)
1:0	RW	0x0	HASHINSEL Specifies the following Data from independent source (0) Data from block cipher input (1) Data from block cipher output (2) Reserved (3)

CRYPTO_BRDMAS

Address: Operational Base + offset (0x0010)

Block Receiving DMA Start Address Register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	STARTADDR Specifies the Start Address of DMA The address should be aligned by 32-bit.

CRYPTO_BTDMAS

Address: Operational Base + offset (0x0014)

Block Transmitting DMA Start Address Register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	STARTADDR Specifies the Start Address of DMA The address needs to be aligned by 32-bit.

CRYPTO_BRDMAL

Address: Operational Base + offset (0x0018)

Block Receiving DMA Length Register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	LENGTH Specifies the Block length of DMA. The length unit is WORD.

CRYPTO_HRDMAS

Address: Operational Base + offset (0x001c)

Hash Receiving DMA Start Address Register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	STARTADDR Specifies the Start Address of DMA The address needs to be aligned by 32-bit.

CRYPTO_HRDMAL

Address: Operational Base + offset (0x0020)

Hash Receiving DMA Length Register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	LENGTH Specifies the Block length of DMA. The length unit is BYTE.

CRYPTO_AES_CTRL

Address: Operational Base + offset (0x0080)

AES Control Register

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11	RW	0x0	AES_BitSwap_CNT Change the Big-endian and Little-endian by swapping the byte order. 0 = Disables Counter data byte swap 1 = Enables Counter data byte swap
10	RW	0x0	AES_BitSwap_Key Change the Big-endian and Little-endian by swapping the byte order. 0 = Disables Key byte swap 1 = Enables Key byte swap
9	RW	0x0	AES_BitSwap_IV Change the Big-endian and Little-endian by swapping the byte order. 0 = Disables Initial value byte swap 1 = Enables Initial value byte swap
8	RW	0x0	AES_BitSwap_DO Change the Big-endian and Little-endian by swapping the byte order. 0 = Disables Output data byte swap 1 = Enables Output data byte swap

Bit	Attr	Reset Value	Description
7	RW	0x0	AES_BitSwap_DI Change the Big-endian and Little-endian by swapping the byte order. 0 = Disables Input data byte swap 1 = Enables Input data byte swap
6	RW	0x0	AES_KeyChange Specifies the AES key change mode selection signal. When the bit is asserted, it will not do key-expansion function to calculate new sub-key. So it is a faster way, when several times of calculation use the same key. But if the keys are different, asserting this bit will have the wrong result. 0 = Key is not changed 1 = Key is changed
5:4	RW	0x0	AES_ChainMode Specifies AES chain mode selection 00 = ECB mode 01 = CBC mode 10 = CTR mode
3:2	RW	0x0	AES_KeySize Specifies the AES key size selection signal 00 : 128-bit key 01 : 192-bit key 10 : 256-bit key
1	RW	0x0	AES_FifoMode Specify AES Fifo Mode 1'b0: Slave mode 1'b1: fifo mode
0	RW	0x0	AES_Enc Specifies the Encryption/ Decryption mode selection signal 0 : Encryption 1 : Decryption

CRYPTO_AES_STS

Address: Operational Base + offset (0x0084)

Status Register

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved

Bit	Attr	Reset Value	Description
0	RW	0x0	AES_DONE When AES finish, it will be HIGH, And it will not be LOW until it restart . 1: done 0: not done

CRYPTO_AES_DIN_0

Address: Operational Base + offset (0x0088)

AES Input Data 0 Register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	AES_DIN_0 Specifies AES Input data [127:96].

CRYPTO_AES_DIN_1

Address: Operational Base + offset (0x008c)

AES Input Data 1 Register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	AES_DIN_1 Specifies AES Input data [95:64].

CRYPTO_AES_DIN_2

Address: Operational Base + offset (0x0090)

AES Input Data 2 Register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	AES_DIN_2 Specifies AES Input data [63:32]

CRYPTO_AES_DIN_3

Address: Operational Base + offset (0x0094)

AES Input Data 3 Register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	AES_DIN_3 Specifies AES Input data [31:0]

CRYPTO_AES_DOUT_0

Address: Operational Base + offset (0x0098)

AES Output Data 0 Register

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	AES_DOUT_0 Specifies AES Output data [127:96].

CRYPTO_AES_DOUT_1

Address: Operational Base + offset (0x009c)

AES Output Data 1 Register

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	AES_DOUT_1 Specifies the Output data [95:64].

CRYPTO_AES_DOUT_2

Address: Operational Base + offset (0x00a0)

AES Output Data 2 Register

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	AES_DOUT_2 Specifies AES Output data [63:32].

CRYPTO_AES_DOUT_3

Address: Operational Base + offset (0x00a4)

AES Output Data 3 Register

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	AES_DOUT_3 Specifies AES Output data [31:0].

CRYPTO_AES_IV_0

Address: Operational Base + offset (0x00a8)

AES IV data 0 Register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	AES_IV_0 Specifies AES Initialization vector [127:96]

CRYPTO_AES_IV_1

Address: Operational Base + offset (0x00ac)

AES IV data 1 Register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	AES_IV_1 Specifies AES Initialization vector [95:64]

CRYPTO_AES_IV_2

Address: Operational Base + offset (0x00b0)

AES IV data 2 Register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	AES_IV_2 Specifies AES Initialization vector [63:32]

CRYPTO_AES_IV_3

Address: Operational Base + offset (0x00b4)

AES IV data 3 Register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	AES_IV_3 Specifies AES Initialization vector [31:0]

CRYPTO_AES_KEY_0

Address: Operational Base + offset (0x00b8)

AES Key data 0 Register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	AES_KEY_0 Specifies AES key data [255:224]

CRYPTO_AES_KEY_1

Address: Operational Base + offset (0x00bc)

AES Key data 1 Register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	AES_KEY_1 Specifies AES key data [223:192]

CRYPTO_AES_KEY_2

Address: Operational Base + offset (0x00c0)

AES Key data 2 Register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	AES_KEY_2 Specifies AES key data [191:160]

CRYPTO_AES_KEY_3

Address: Operational Base + offset (0x00c4)

AES Key data 3 Register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	AES_KEY_3 Specifies AES key data [159:128]

CRYPTO_AES_KEY_4

Address: Operational Base + offset (0x00c8)

AES Key data 4 Register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	AES_KEY_4 Specifies AES key data [127:96]

CRYPTO_AES_KEY_5

Address: Operational Base + offset (0x00cc)

AES Key data 5 Register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	AES_KEY_5 Specifies the key data [95:64]

CRYPTO_AES_KEY_6

Address: Operational Base + offset (0x00d0)

AES Key data 6 Register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	AES_KEY_6 Specifies AES key data [63:32]

CRYPTO_AES_KEY_7

Address: Operational Base + offset (0x00d4)

AES Key data 7 Register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	AES_KEY_7 Specifies the key data [31:0]

CRYPTO_AES_CNT_0

Address: Operational Base + offset (0x00d8)

AES Input Counter 0 Register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	AES_CNT_0 Specifies AES Input Counter [127:96].

CRYPTO_AES_CNT_1

Address: Operational Base + offset (0x00dc)

AES Input Counter 1 Register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	AES_CNT_1 Specifies AES Input Counter [95:64].

CRYPTO_AES_CNT_2

Address: Operational Base + offset (0x00e0)

AES Input Counter 2 Register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	AES_CNT_2 Specifies AES Input Counter[63:32]

CRYPTO_AES_CNT_3

Address: Operational Base + offset (0x00e4)

AES Input Counter 3 Register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	AES_CNT_3 Specifies AES Input Counter [31:0]

CRYPTO_TDES_CTRL

Address: Operational Base + offset (0x0100)

TDES Control Register

Bit	Attr	Reset Value	Description
31:9	RO	0x0	reserved

Bit	Attr	Reset Value	Description
8	RW	0x0	TDES_ByteSwap_Key 0 = Disables Key byte swap 1 = Enables Key byte swap
7	RW	0x0	TDES_ByteSwap_IV 0 = Disables Initial value byte swap 1 = Enables Initial value byte swap
6	RW	0x0	TDES_ByteSwap_DO 0 = Disables Output data byte swap 1 = Enables Output data byte swap
5	RW	0x0	TDES_ByteSwap_DI 0 = Disables Input data byte swap 1 = Enables Input data byte swap
4	RW	0x0	TDES_ChainMode Specifies TDES chain mode selection 0 : ECB mode 1 : CBC mode
3	RW	0x0	TDES_EEE Specifies the TDES key mode selection 1'b0 : EDE 1'b1 : EEE
2	RW	0x0	TDES_Select Specify DES or TDES cipher 1'b0 : DES 1'b1 : TDES
1	RW	0x0	TDES_FifoMode Specify TDES Fifo Mode 1'b0: Slave mode 1'b1: Fifo mode
0	RW	0x0	TDES_Enc Specifies the Encryption/ Decryption mode selection signal 0 : Encryption 1 : Decryption

CRYPTO_TDES_STS

Address: Operational Base + offset (0x0104)

Status Register

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	TDES_DONE When DES/TDES finishes, it will be HIGH, And it will not be LOW until it restart . 1: done 0: not done

CRYPTO_TDES_DIN_0

Address: Operational Base + offset (0x0108)

TDES Input Data 0 Register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	TDES_DIN_0 Specifies TDES Input data [63:32].

CRYPTO_TDES_DIN_1

Address: Operational Base + offset (0x010c)

TDES Input Data 1 Register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	TDES_DIN_1 Specifies TDES Input data [31:0].

CRYPTO_TDES_DOUT_0

Address: Operational Base + offset (0x0110)

TDES Output Data 0 Register

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	TDES_DOUT_0 Specifies TDES Output data [63:32].

CRYPTO_TDES_DOUT_1

Address: Operational Base + offset (0x0114)

TDES Output Data 1 Register

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	TDES_DOUT_1 Specifies TDES Output data [31:0].

CRYPTO_TDES_IV_0

Address: Operational Base + offset (0x0118)

TDES IV data 0 Register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	TDES_IV_0 Specifies TDES Initialization vector [63:32]

CRYPTO_TDES_IV_1

Address: Operational Base + offset (0x011c)

TDES IV data 1 Register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	TDES_IV_1 Specifies TDES Initialization vector [31:0]

CRYPTO_TDES_KEY1_0

Address: Operational Base + offset (0x0120)

TDES Key1 data 1 Register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	TDES_KEY1_0 Specifies TDES key1 data [63:32]

CRYPTO_TDES_KEY1_1

Address: Operational Base + offset (0x0124)

TDES Key1 data 1 Register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	TDES_KEY1_1 Specifies TDES key1 data [31:0]

CRYPTO_TDES_KEY2_0

Address: Operational Base + offset (0x0128)

TDES Key2 data 0 Register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	TDES_KEY2_0 Specifies TDES key2 data [63:32]

CRYPTO_TDES_KEY2_1

Address: Operational Base + offset (0x012c)

TDES Key2 data 1 Register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	TDES_KEY2_1 Specifies TDES key data [31:0]

CRYPTO_TDES_KEY3_0

Address: Operational Base + offset (0x0130)

TDES Key3 data 0 Register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	TDES_KEY3_0 Specifies TDES key3 data [63:32]

CRYPTO_TDES_KEY3_1

Address: Operational Base + offset (0x0134)

TDES Key3 data 1 Register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	AES_KEY3_1 Specifies TDES key3 data [31:0]

CRYPTO_HASH_CTRL

Address: Operational Base + offset (0x0180)

Hash Control Register

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved

Bit	Attr	Reset Value	Description
3	RW	0x0	HASH_SWAP_DO Specifies the Byte swap of data output (hash result) 0 = Does not swap (default) 1 = Swap
2	RW	0x0	HASH_SWAP_DI Specifies the Byte swap of data input. 0 = Does not swap (default) 1 = Swap
1:0	RW	0x0	Engine_Selection 2'b00: SHA1_HASH 2'b01: MD5_HASH 2'b10: SHA256_HASH 2'b11: PRNG

CRYPTO_HASH_STS

Address: Operational Base + offset (0x0184)

Hash Status Register

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	HASH_DONE Hash Done Signal When HASH finishes, it will be HIGH, And it will not be LOW until it restart 1'b1 : done 1'b0 : not done

CRYPTO_HASH_MSG_LEN

Address: Operational Base + offset (0x0188)

Hash Message Len

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Msg_size Hash total byte.

CRYPTO_HASH_DOUT_0

Address: Operational Base + offset (0x018c)

Hash Result Register 0

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	HASH_RESULT_0 Specifies the HASH Result [159:128]

CRYPTO_HASH_DOUT_1

Address: Operational Base + offset (0x0190)

Hash Result Register 1

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	HASH_RESULT_1 Specifies the HASH Result [127:96]

CRYPTO_HASH_DOUT_2

Address: Operational Base + offset (0x0194)

Hash Result Register 2

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	HASH_RESULT_2 Specifies the HASH Result [95:64]

CRYPTO_HASH_DOUT_3

Address: Operational Base + offset (0x0198)

Hash Result Register 3

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	HASH_RESULT_3 Specifies the HASH Result [63:32]

CRYPTO_HASH_DOUT_4

Address: Operational Base + offset (0x019c)

Hash Result Register 4

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	HASH_RESULT_4 Specifies the HASH Result [31:0]

CRYPTO_HASH_DOUT_5

Address: Operational Base + offset (0x01a0)

Hash Result Register 4

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	HASH_RESULT_5 Specifies the HASH Result [31:0]

CRYPTO_HASH_DOUT_6

Address: Operational Base + offset (0x01a4)

Hash Result Register 6

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	HASH_RESULT_6 Specifies the HASH Result [31:0]

CRYPTO_HASH_DOUT_7

Address: Operational Base + offset (0x01a8)

Hash Result Register 7

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	HASH_RESULT_7 Specifies the HASH Result [31:0]

CRYPTO_HASH_SEED_0

Address: Operational Base + offset (0x01ac)

PRNG Seed/HMAC Key Register 0

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	HASH_SEED_0 Specifies PRNG Seed/HMAC Key buffer [159:128]

CRYPTO_HASH_SEED_1

Address: Operational Base + offset (0x01b0)

PRNG Seed/HMAC Key Register 1

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	HASH_SEED_1 Specifies PRNG Seed/HMAC Key buffer [127:96]

CRYPTO_HASH_SEED_2

Address: Operational Base + offset (0x01b4)

PRNG Seed/HMAC Key Register 2

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	HASH_SEED_2 Specifies PRNG Seed/HMAC Key buffer [95:64]

CRYPTO_HASH_SEED_3

Address: Operational Base + offset (0x01b8)

PRNG Seed/HMAC Key Register 3

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	HASH_SEED_3 Specifies PRNG Seed/HMAC Key buffer [63:32]

CRYPTO_HASH_SEED_4

Address: Operational Base + offset (0x01bc)

PRNG Seed/HMAC Key Register 4

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	HASH_SEED_4 Specifies PRNG Seed/HMAC Key buffer [31:0]

CRYPTO_TRNG_CTRL

Address: Operational Base + offset (0x0200)

TRNG Control

Bit	Attr	Reset Value	Description
31:17	RO	0x0	reserved

Bit	Attr	Reset Value	Description
16	RW	0x0	osc_enable osc_ring enable It control the running of osc_ring. And it is independent of clock and flush signal. This means that it can run even when clock is gating or flush is asserted as long as osc_enable is asserted. Before it is used to get TRNG result, please run osc_ring first to get enough entropy. 1'b1: Enable ; 1'b0: Disable ;
15:0	RW	0x0000	period sample period TRNG use clock_crypto to sample ring osc output, this parameter is specify how many cycles to generate 1 bit random data.

CRYPTO_TRNG_DOUT_0

Address: Operational Base + offset (0x0204)

TRNG Output Data 0

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	TRNG_DOUT_0

CRYPTO_TRNG_DOUT_1

Address: Operational Base + offset (0x0208)

TRNG Output Data 1

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	TRNG_DOUT_1

CRYPTO_TRNG_DOUT_2

Address: Operational Base + offset (0x020c)

TRNG Output Data 2

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	TRNG_DOUT_2

CRYPTO_TRNG_DOUT_3

Address: Operational Base + offset (0x0210)

TRNG Output Data 3

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	TRNG_DOUT_3

CRYPTO_TRNG_DOUT_4

Address: Operational Base + offset (0x0214)

TRNG Output Data 4

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	TRNG_DOUT_4

CRYPTO_TRNG_DOUT_5

Address: Operational Base + offset (0x0218)

TRNG Output Data 5

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	TRNG_DOUT_5

CRYPTO_TRNG_DOUT_6

Address: Operational Base + offset (0x021c)

TRNG Output Data 6

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	TRNG_DOUT_6

CRYPTO_TRNG_DOUT_7

Address: Operational Base + offset (0x0220)

TRNG Output Data 7

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	TRNG_DOUT_7

CRYPTO_PKA_CTRL

Address: Operational Base + offset (0x0280)

PKA Control Register

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1:0	RW	0x0	block_size PKA Size It specifies the bits of N in PKA calculation. 2'b00: 512 bit 2'b01: 1024 bit 2'b10: 2048 bit

CRYPTO_PKA_M

Address: Operational Base + offset (0x0400)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	m PKA input or output data. PKA result = (M ^ E) mod N. When it finishes, the result data is in M position. Start from PKA_M base address, and may contain 512/1024/2048 bits data.

CRYPTO_PKA_C

Address: Operational Base + offset (0x0500)

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	c PKA pre-calculate data, C = 2 ^ (2n+2) mod N

CRYPTO_PKA_N

Address: Operational Base + offset (0x0600)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	n PKA modular

CRYPTO_PKA_E

Address: Operational Base + offset (0x0700)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	e PKA exponent.

19.4 Application Note

19.4.1 Reset a port

CRU_SOFTRST3_CON.crypto_srstn_req is used to do a soft reset to crypto . Please refer to "Chapter CRU" for more details.

19.4.2 Overall Performance

Use CLKSEL24_CON.crypto_div_con to select crypto frequency: $F_{crypto} = F_{clock} / (div + 1)$. Make sure F_{crypto} do not exceed 150M.

The performance of crypto FIFO mode is list below.

algorithm	cycle	block size	frequency	throughput rate
DES	17	64 bit	100M	376 M bps
TDES	51	64 bit	100M	125 M bps
AES	11/13/15	128 bit	100M	1160/984/853Mbps
SHA-1	81	512 bit	100M	632 Mbps
MD5	65	512 bit	100M	787 Mbps

19.4.3 Usage

1. Symmetric algorithm

DES/3DES, AES are symmetric algorithms. There are two ways of using these algorithms: Slave mode and FIFO mode.

In Slave mode, you can calculate 1 block size of data by starting the engine. Take AES-128 for example, you should

Program Input 128 bit Data to AES_DIN_0~AES_DIN_3

Program Input 128 bit Key to AES_KEY_0~AES_KEY_3

Program control mode to AES_CTRL to run in different mode

Program CTRL.AES_START to run
wait AES_STS.DONE High
Read AES_DOUT_0 ~ AES_DOUT_3 to get result.

In FIFO mode,

Program the source address to BRDMAS, the destination address to BTDMAS, program the length in word unit to BRDMAL;
Program Input 128 bit Key to AES_KEY_0~AES_KEY_3;
Program control mode to AES_CTRL to run in different mode;
Program INTENA to enable interrupt;
Program CTRL.BLOCK_START to start;
wait interrupt asserted;
Program INTSTS to clear interrupt status;
Read the destination address which BTDMA points to.

FIFO mode get much higher throughput rate.

2. HASH

HASH is used to get digest of data. Only support FIFO mode.

There are three source: (1) hr_fifo; (2) br_fifo; (3) bt_fifo.

Take hr_fifo for example

Program CTRL.HASH_FLUSH 1'b1 to clear, wait several cycle (≥ 10 cycles), and Program CTRL.HASH_FLUSH 1'b0
Program data source address to HRDMAS, program 1 time data length in word unit to HRDMAL, program total length in byte unit to HASH_MSG_LEN
Program HASH_CTRL to choose algorithm, for example SHA-256
Program INTENA to enable interrupt;
Program CTRL.HASH_START 1'b1 to start;
Wait interrupt asserted; Only if HRDMAL length meets can this interrupt be asserted
If you have another section of data to hash, then go to (2), HASH_MSG_LEN need not to be programmed;
else go to (8)
wait HASH_STS.done asserted. Only if Hash_MSG_LEN meet can this bit status register asserted.
Read HASH_DOUT_0 – HASH_DOUT_7 to get result.

3. Asymmetric Algorithm

Support 512/1024/2048 bit RSA calculation. It provide the big number calculation. Result = $M^E \bmod N$

Program CTRL.PKA_FLUSH 1'b1 to flush RSA module;
Wait CTRL.PKA_FLUSH to be LOW. It is self-cleared;
Program input_data(M) to PKA_M; Program pre_caculated C to PKA_C; Program Key(N) to PKA_N; Program Key(E) to PKA_E. $C = 2^{(2n+2)} \bmod N$. n is the required bit of N. For example 2048 bit N, n = 2048;
Program PKA_CTRL to select RSA size: 512/1024/2048
Program INTENA to enable interrupt;
Program CTRL.PKA_START to start;
Wait interrupt asserted.
Read PKA_M to get results.

Chapter 20 Process Voltage Temperature Monitor (PVTM)

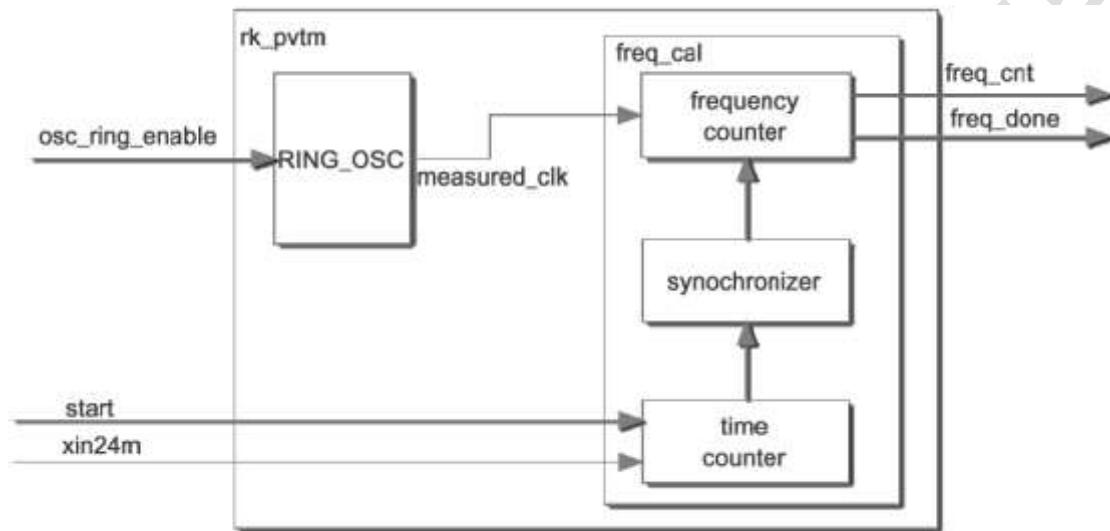
20.1 Overview

The Process-Voltage-Temperature Monitor (PVTM) is used to monitor the chip performance variance caused by chip process, voltage and temperature.

PVTM supports the following features:

- a clock oscillation ring is integrated and used to generate a clock like signal, the frequency of this clock is determined by the cell delay value of clock oscillation ring circuit
- a frequency counter is used to measure the frequency of the clock oscillation ring.

20.2 Block Diagram



The PVTM include two main blocks

RING_OSC, it is composed with inverters with odd number, which is used to generate a clock

Freq_cal, it is used to measure the frequency of clock which generated from the RING_SOC block

Frequency Calculation

A frequency fixed clock(24MH) is used to calculate the clock cycles of RING_OSC generated clock. Suppose the time period is 1s, then the clock period of RING_OSC clock is $T = 1/2 * \text{clock_counter}(\text{s})$