Computer Engineering 431, Spring 2018 Exam 3, Tuesday, April 19th

Exam time: 5 pre + 70 minutes exam

Test Value: 16 **pts. Total possible points:** 20 **(max score =** 125 **%)**

Total = /16	P1: /8	P2: /4	P3: /8

Front Left Neighbor # _____	**Front Neighbor #** _____	**Front Right Neighbor #** _____
Left Neighbor # _____	**Your Name (print clearly):** _____	**Right Neighbor #** _____
Rear Left Neighbor # _____	**Rear Neighbor #** _____	**Rear Right Neighbor #** _____

1. *(8pts) Coherence simulation*

Assume a four-core system, each core with two SMT threads, wherein each core has a private L1 followed by a shared bus to main memory. Assume that all cache lines are initially invalid. Assume that there exist two lines FOO and BAR that map to different sets in the cache.

Using the MESI protocol, simulate the coherence state of cache lines FOO and BAR under the following thread to core and variable to cache line mappings:
Thread to core – T0:Core 0, T1: Core 1, T2: Core 1, T3: Core 2, T4: Core 3, T5: Core 3
Variable to cache line – A and C in FOO, B and D in BAR

OPERATION	CORE 0		CORE 1		CORE 2		CORE 3	
<Initial>	FOO	BAR	FOO	BAR	FOO	BAR	FOO	BAR
	I	I	I	I	I	I	I	I
T0: Load A								
T1: Load B								
T2: Store C								
T0: Store A								
T3: Load C								
T3: Store A								
T4: Load B								
T5: Load D								
T0: Load B								
T1: Store B								
T5: Store D								
T0: Store B								
T3: Store C								
T5: Load D								
T2: Load A								

2. (4 pts) *Protocols*
For each of the following < current state-in-cache, action > pairs in MESI, note whether the local cache controller must initiate a bus transaction, and why.

i. < I, remote store>

ii. < S, local load >

iii. <M, remote load >

iv. <E, local store>

3. (8 pts) *Protocol-Behavior interactions*
Assume that two cores are about to run the same spin-lock protected code, with assumptions given in comments, and that they execute no instructions beyond OP13 and the cache is initially empty:

```
Check:  ADDI    $1, $0, 1       #OP1- set $1 to 1 (1 locked, 0 unlocked)
        LL      $2, 0($3)       #OP2- $3 contains pointer to lock
        BNE     $2, $0, Check   #OP3- repeat if locked
        SC      $1, 0($3)       #OP4- attempt to lock
        BEQ     $1, $0, Check   #OP5- repeat if failed
        LW      $1, 0($4)       #OP6- critical section – assume that the pointers stored
        LW      $2, 0($5)       #OP7- in $3, $4, and $5 point to separate cache blocks
        ADDU    $1, $2, $1      #OP8- and that the associativity of the cache is > 3
        ADDU    $1, $1, $6      #OP9- where the value of $6 may differ per thread
        ADDU    $2, $2, $7      #OP10- where the value of $7 may differ per thread
        SW      $1, 0($4)       #OP11- update protected value
        SW      $2, 0($5)       #OP12- update protected value
        SW      $0, 0($3)       #OP13- release lock
```

Assume that each core can execute 1 instruction per cycle, including (uncontended) bus transactions, that core 0 always wins when two bus operations are requested in the same cycle, and core 0 first executes OP1 in cycle 0 and core 1 first executes OP1 in cycle 1. Assume MSI coherence.

i. (2) In what cycle will core 1 execute op13?

ii. (3) Would MESI improve performance? Why/why not? What if there were more than two threads?

iii. (3) Would VI hurt performance? Why/why not? What if there were more than two threads?