Quiz 4 Solutions

Q1) Explain the difference between internal and external fragmentation. What is the most internal fragmentation if 4kB <= address space <= 8kB, and page size = 4kB.

A1) Internal fragmentation is within a page – if much of the page is unused. External fragmentation is found when there is memory to store, but it is scattered, and the application requires contiguous allocation.

Q2) Consider a paging system with the page table stored in memory.

- If a memory ref. takes 200 nsec, how long does a paged memory ref. take?
- If we add TLBs, and TLB hit ratio is 90%, what is the effective mem. ref. time? TLB access takes 0 time.

A2) First part is 400 nsec.
E.M.R.T. = (.90)(200) + (.10)(400) = 220   <first part is TLB hit, then TLB miss)

Q3) How much memory is needed to store an entire page table for 32-bit address space if

- Page size = 4kB, single level page table?
- Page size = 4kB, 2-level page table, p1=10, p2=10, p3=12?

A3) 20 bits for entry, 12 for offset (to represent 4kB). So memory needed is:
(2^20 * 20 bits)
First level page table is: (2^10 *32 bits) each points to table of size (2^10 *10).
Total is: (2^10 *32) + (2^10 * 2^10 *10)

Q4) Consider a demand paging system with the following time-measured utilizations: CPU = 20%, paging disk = 97.7%, other IO devices = 5%.

A4) Install a faster CPU => doesn't help, decreases CPU utilization.
Install a bigger swap device => no change, bandwidth is problem, not size.
Increase the degree of multi-programming => worse. Swap util increases, CPU utilization decreases.
Decrease the degree of multi-programming => better. Swap util decreases, CPU utilization increases.
Install more main memory => CPU increases, swap decreases.
Install a faster hard disk => CPU increases, swap decreases.
Increase the page size => tradeoff between improving bandwidth by getting fewer pages and wasting RAM because of internal fragmentation.

Q5) Which of the two computers would you buy: CPU=1GHZ, RAM=500 pages or CPU=2GHZ, RAM = 400 pages? Based on a curve found in the lecture slides.

A5) Calculate PFR. For 500 pages = (500)^2/(1000)^2
For 400 pages = (600)^2/(1000)^2
Assume memory access time of 100 cycles and swap access time of 100,000 cycles. Ignore memory needed to store page table, ignore the TLB. Assume all instructions are load/stores.

E.A.T. = (1-PFR)*100 + PFR*100000

For 1GHZ, 500 page machine:

E.A.T. = (.75)(100) + (.25)(100000) = 25075
Runs 10^9 cycles/sec => 10^9/25075 = 39880.36 instructions in a second.

For 2GHZ, 400 page machine:

E.A.T. = (.64)(100) + (.36)(100000) = 36064
Runs 2*10^9 cycles/sec => (2*10^9)/36064 = 55456.97 instructions in a second.

So the faster machine would be the better choice.