Operating Systems/Computer Architecture Candidacy Exam Spring 2021

Name:

Instructions: This exam has two sections: operating systems and computer architecture. Each section has 100 points worth of questions. You have 3 hours to answer 50 points worth of questions from each section. Only the first 50 points-worth of questions starting from the beginning of the section will be graded. Therefore, try to answer only the questions whose answers you are confident about. Good luck!

Operating Systems

Virtual Memory

1. **(5 points)** Describe one benefit of virtual memory.

2. **(5 points)** What causes a page fault? Describe what happens during a page fault.

3. **(5 points)** All processes running in the operating system share the same page table. True or False? Explain your answer.

4. **(5 points)** What is the purpose of a TLB?

5. **(5 points)** What is the page size in modern operating systems?

Kernel

1. **(5 points)** What is the difference between a program and a process?

2. **(5 points)** What is a system call? How does it differ from an ordinary function call?

3. **(5 points)** What is a context switch? Describe one cause of a context switch.

4. **(5 points)** Two primary types of multitasking are preemptive and cooperative. Describe how each works. Which one do mainstream operating systems use?

5. **(5 points)** Why do we need an operating system at all? Why don't we write our programs to run directly on raw hardware?

Storage

1. **(5 points)** What is an inode? List three pieces of information stored in an inode.

2. **(5 points)** What is RAID? Choose any of the RAID levels and explain how it works.

3. **(5 points)** Modern file systems provide only metadata consistency by default. What does metadata consistency mean and what are the implications of this for the users.

4. **(5 points)** Some file systems can provide data consistency as well if configured to do so. What is data consistency and why do these file systems not provide data consistency by default?

5. **(5 pointts)** Two decades ago, operating systems took a long time to boot after a power failure: they had to run a file system checker, which analyzed all on-disk file system data structures to ensure the metadata consistency of the file system. Today, however, operating systems boot quickly even after a power failure because modern file systems use a technique that obviates the need to perform

full disk analysis for ensuring metadata consistency. What is the name of the technique used by modern file systems?

Concurrency

1. **(5 points)** What is a data race?

2. **(5 points)** Write a piece of pseudocode that has a data race and describe how it can be prevented using a lock.

3. **(5 points)** What is a readers-writer lock? Describe a scenario where a readers-writer lock is preferable to a regular lock.

4. **(5 pointts)** What problem does a condition variable solve? Describe a scenario where using a condition variable is necessary.

5. **(5 points)** What is a deadlock? Describe a scenario where a deadlock occurs and show how to prevent it.

Computer Architecture

Potpourri

1. **(5 points)** Describe 4 software level techniques for improving instruction level parallelism.

2. **(5 points)** Describe the difference between snooping and directory-based coherency protocols.

3. **(5 points)** Describe the difference between write-though and write-back policies.

4. **(5 points)** Describe how speculation can improve performance compared to dynamic scheduling.

5. **(5 points)** What is the difference between interrupt and exception/trap?

Pipelining and hazards

1. Consider the following sequence of instructions being processed on a **pipelined** 5-stage RISC processor:

```
Load R4, #50(R2)
Add R5, R2, R3
Subtract R6, R4, R5
Or R7, R2, R5
```

(a) **(6 points)** Identify all the data dependencies in the above instruction sequence indicating the instructions and the registers involved.

(b) **(4 points)** Assuming that the pipeline does not use operand forwarding and that the only sources of pipeline stalls are the data hazards, draw a diagram to show instruction flow through the pipeline during each clock cycle.

(c) **(2 points)** How long does it take for the instruction sequence to complete in (b)?

(d) **(6 points)** Assuming that the pipeline now uses operand forwarding, draw a diagram to show the flow of instructions through the pipeline during each clock cycle. Indicate operand forwarding by arrows.

(e) **(4 points)** Memory latency is a problem for processors so the architect modified the pipeline. The new microarchitecture implements MEM stage before the EX stage. Make minimal changes in the instructions so that it fits in the new pipeline. Do not attempt to aggressively reschedule the instructions.

(f) **(3 points)** Write one pro and one con of the new pipeline presented in part (e).

Performance analysis

1. A computer M has the following CPIs for instruction types A through D:
Type A $CPI_A = 1.8$
Type B $CPI_B = 2.2$
Type C $CPI_C = 2.6$
Type D $CPI_D = 2.5$

And a program has the following mix of instructions:
Type A = 25%
Type B = 30%
Type C = 15%
Type D = remaining %

(a) **(5 points)** Calculate the average CPI of the machine.

(b) **(5 points)** Calculate the runtime of program on the machine if Instruction Count = 22,000 and clock rate is 3 GHz.

2. On a different machine, the clock rate is 3.2 GHz. A program has 30% Type A instructions and the remainder are Type B instructions. A hardware accelerator can make Type A instructions 5 times faster.

(a) **(5 points)** How much speed up will be gained by the program via this accelerator?

(b) **(5 points)** Use Amdahl's Law to determine how much **maximum** speed up can be gained by using this accelerator? You can make the accelerator as fast as possible.

3. **(5 points)** Power consumption is given by CV^2f where C is switching capacitance, V is operating voltage and f is operating frequency. Power consumption gives rise to heat therefore we need to reduce the power under overheating conditions. One approach to reduce power is to scale down the clock frequency (DVF) while another approach is to scale down both the voltage and frequency (DVFS). If you have the capability to scale the voltage by ½ and clock frequency by ½, which approach will you prefer to reduce power? How much power can be reduced?

Cache

1. **(3 points)** Explain how caches improve performance.

2. **(3 points)** A special cache has the block size equal to the word length. What property of program behavior, which usually contributes to higher performance if we use a cache, does not help the performance if we use this special cache?

3. **(6 points)** Suppose we have a byte addressable memory of size 4GB (2^{32} bytes). We are given a cache of size 1MB (2^{20} bytes, not including tag bits) and a cache block size of 256 (2^8) bytes. Compute for a 8-way associative cache the length in number of bits for the tag, index and offset fields of a 32-bit memory address.

4. **(5 points)** Explain the purpose of the index of an address and why it does not need to be stored in the cache.

5. Suppose we have a cache / memory system with the following parameters:

- L1 cache with a 5% miss rate, cache hits require 1 clock cycle
- Clock rate of 1 GHz (1 clock cycle = 1 nanosecond)
- Memory system accesses require 25 nanoseconds

(a) **(4 points)** What is the average memory access time for a system with only a L1 cache?

(b) **(4 points)** We decide to add a second L2 cache that will be accessed only when accesses miss the L1 cache. If the L2 cache has a miss rate of 2%, what percentage of memory accesses will miss both caches and actually access memory?