## *32,768 WORD x 8 Bit CMOS Static RAM*

### FEATURES

- **Fast Access Time: 70, 85, 100, 120ns (Max.)**
- **Low Power Dissipation**
  - **Standby (CMOS): 10μW (Typ.) L-Version**
  - **5μW (Typ.) LL-Version**
  - **Operating : 35mW/1MHz (Max.)**
- **Single 5V ± 10% Power Supply**
- **TTL Compatible Inputs and Outputs**
- **Fully Static Operation**
  - **No clock or refresh required**
- **Three State Outputs**
- **Low Data Retention Voltage: 2V (Min.)**
- **Standard Pin Configuration**
  - **KM62256BLP/BLP-L : 28-DIP-600B**
  - **KM62256BLG/BLG-L : 28-SOP-450**
  - **KM62256BLS/BLS-L : 28-DIP-300**
  - **KM62256BLTG/BLTG-L : 28-TSOP1-0813.4F**
  - **KM62256BLRG/BLRG-L : 28-TSOP1-0813.4R**

### GENERAL DESCRIPTION

The KM62256BL/BL-L is a 262,144-bit high-speed Static Random Access Memory organized as 32,768 words by 8 bits.

The device is fabricated using Samsung's advanced CMOS process with polyresistors.

The KM62256BL/BL-L has an output enable input for precise control of the data outputs.

It also has a chip enable input for the minimum current power down mode.

The KM62256BL/BL-L has been designed for high speed and low power application. It is particularly well suited for battery back-up nonvolatile memory application.

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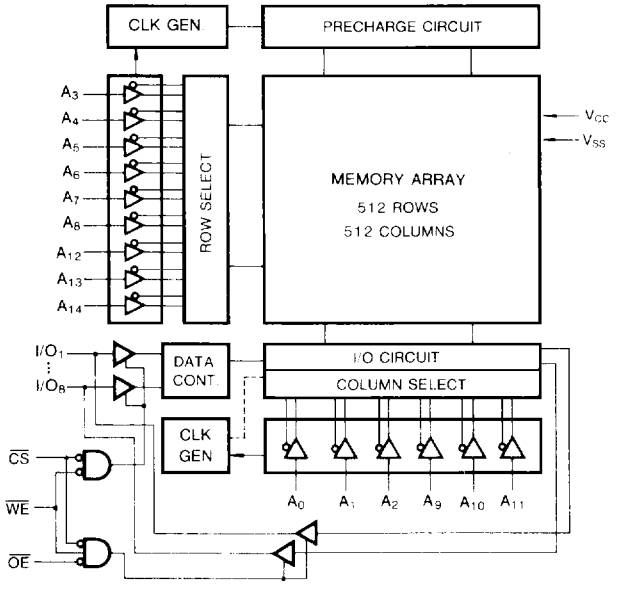
### FUNCTIONAL BLOCK DIAGRAM

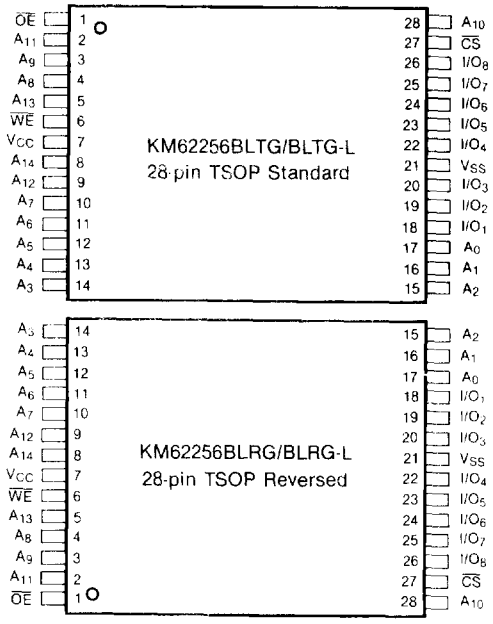


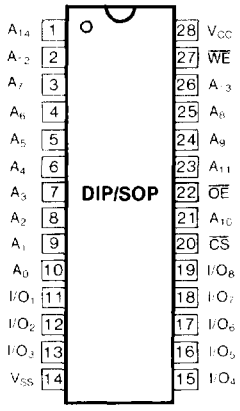

### PIN CONFIGURATIONS

| Pin Name | Pin Function |
|---|---|
| $A_0$-$A_{14}$ | Address Inputs |
| $\overline{WE}$ | Write Enable Input |
| $\overline{CS}$ | Chip Select Input |
| $\overline{OE}$ | Output Enable Input |
| $I/O_1$-$I/O_8$ | Data Inputs/Outputs |
| $V_{CC}$ | Power (+5V) |
| $V_{SS}$ | Ground |
| N.C. | No Connection (32-TSOP only) |

## PIN CONFIGURATIONS (Top View)

**28-pin TSOP (0813.4)**



## ABSOLUTE MAXIMUM RATINGS*

| Item | Symbol | Rating | Unit |
|---|---|---|---|
| Voltage on Any Pin Relative to $V_{SS}$ | $V_{IN}$, $V_{OUT}$ | -0.5 to $V_{CC}$ +5.5 | V |
| Voltage on $V_{CC}$ Supply Relative to $V_{SS}$ | $V_{CC}$ | -0.5 to 7.0 | V |
| Power Dissipation | $P_D$ | 1.0 | W |
| Storage Temperature | $T_{STG}$ | -65 to 150 | °C |
| Operating Temperature | $T_A$ | 0 to 70 | °C |
| Soldering Temperature and Time | $T_{solder}$ | 260° C, 10 sec(Lead only) | — |

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

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## RECOMMENDED OPERATING CONDITIONS ($T_A$=0 to 70°C)

| Item | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Supply Voltage | $V_{CC}$ | 4.5 | 5.0 | 5.5 | V |
| Ground | $V_{SS}$ | 0 | 0 | 0 | V |
| Input High Voltage | $V_{IH}$ | 2.2 | — | $V_{CC}$+0.5 | V |
| Input Low Voltage | $V_{IL}$ | -0.5* | — | 0.8 | V |

* $V_{IL}$(min)=-3.0V for ≤ 50ns pulse

## DC AND OPERATING CHARACTERISTICS

($T_A$=0 to 70°C, $V_{CC}$=5V±10%, unless otherwise specified)

| Item | Symbol | Test Condition | | Min | Typ* | Max | Unit |
|---|---|---|---|---|---|---|---|
| Input Leakage Current | $I_{LI}$ | $V_{IN}$=$V_{SS}$ to $V_{CC}$ | | -1 | — | 1 | μA |
| Output Leakage Current | $I_{LO}$ | $\overline{CS}$=$V_{IN}$ or $\overline{OE}$=$V_{IH}$ or $\overline{WE}$=$V_{IL}$, $V_{I/O}$=$V_{SS}$ to $V_{CC}$ | | -1 | — | 1 | μA |
| Operation Power Supply Current | $I_{CC}$ | $\overline{CS}$=$V_{IL}$, $V_{IN}$=$V_{IH}$ or $V_{IL}$<br>$I_{I/O}$=0mA | | — | 7 | 15 | mA |
| Average Operating Current | $I_{CC1}$ | Cycle Time=1μS, 100% Duty $\overline{CS}$≤0.2V, $V_{IL}$≤0.2V<br>$V_{IH}$≥$V_{CC}$-0.2V, $I_{I/O}$=0mA | | — | — | 7 | mA |
| | $I_{CC2}$ | Min Cycle. 100% Duty $\overline{CS}$=$V_{IL}$,<br>$V_{IN}$=$V_{IL}$ or $V_{IH}$ $I_{I/O}$=0mA | | — | 45 | 70 | mA |
| Standby Power Supply Current | $I_{SB}$ | $\overline{CS}$=$V_{IH}$ | | — | — | 1 | mA |
| | $I_{SB1}$ | $\overline{CS}$≥$V_{CC}$-0.2V, $V_{IN}$≥$V_{CC}$-0.2 or<br>$V_{IN}$≤0.2V | L-Ver | — | 2 | 100 | μA |
| | | | LL-Ver | — | 1 | 20 | μA |
| Output Low Voltage | $V_{OL}$ | $I_{OL}$=2.1mA | | — | — | 0.4 | V |
| Output High Voltage | $V_{OH}$ | $I_{OH}$=-1.0mA | | 2.4 | — | — | V |

*Typ: $V_{CC}$=5V, $T_A$=25° C

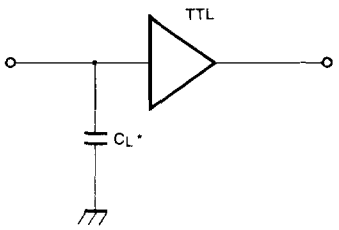
## CAPACITANCE ($f = 1MHz$, $T_A = 25°C$)

| Item | Symbol | Test Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| Input Capacitance | $C_{IN}$ | $V_{IN} = 0V$ | — | 6 | pF |
| Input/Output Capacitance | $C_{I/O}$ | $V_{I/O} = 0V$ | — | 8 | pF |

Note: Capacitance is sampled and not 100% tested.

## TEST CONDITIONS ($T_A = 0$ to $70°C$, $V_{CC} = 5V \pm 10\%$, unless otherwise specified)

| Parameter | Value |
|---|---|
| Input Pulse Level | 0.8 to 2.4V |
| Input Rise and Fall Times | 5ns |
| Input and Output Timing Reference Levels | 1.5V |
| Output Loads | $C_L = 100pF + 1$ TTL |




* Including Scope and Jig Capacitance

## READ CYCLE

| Parameter | Symbol | KM62256BL-7 KM62256BL-7L | | KM62256BL-8 KM62256BL-8L | | KM62256BL-10 KM62256BL-10L | | KM62256BL-12 KM62256BL-12L | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| Read Cycle Time | $t_{RC}$ | 70 | | 85 | | 100 | | 120 | | ns |
| Address Access Time | $t_{AA}$ | | 70 | | 85 | | 100 | | 120 | ns |
| Chip Select to Output | $t_{CO}$ | | 70 | | 85 | | 100 | | 120 | ns |
| Output Enable to Valid Output | $t_{OE}$ | | 35 | | 45 | | 50 | | 60 | ns |
| Chip Select to Low-Z Output | $t_{LZ}$ | 10 | | 10 | | 10 | | 10 | | ns |
| Output Enable to Low-Z Output | $t_{OLZ}$ | 5 | | 5 | | 5 | | 5 | | ns |
| Chip Disselect to High-Z Output | $t_{HZ}$ | 0 | 30 | 0 | 30 | 0 | 35 | 0 | 40 | ns |
| Output Disable to High-Z Output | $t_{OHZ}$ | 0 | 30 | 0 | 30 | 0 | 35 | 0 | 40 | ns |
| Output Hold from Address Change | $t_{OH}$ | 5 | | 5 | | 10 | | 10 | | ns |

## WRITE CYCLE

| Parameter | Symbol | KM62256BL-7 KM62256BL-7L | | KM62256BL-8 KM62256BL-8L | | KM62256BL-10 KM62256BL-10L | | KM62256BL-12 KM62256BL-12L | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| Write Cycle Time | $t_{WC}$ | 70 | | 85 | | 100 | | 120 | | ns |
| Chip Select to End of Write | $t_{CW}$ | 60 | | 75 | | 80 | | 85 | | ns |
| Address Valid to End of Write | $t_{AW}$ | 60 | | 75 | | 80 | | 85 | | ns |
| Address Set-up Time | $t_{AS}$ | 0 | | 0 | | 0 | | 0 | | ns |
| Write Pulse Width | $t_{WP}$ | 50 | | 60 | | 60 | | 70 | | ns |
| Write Recovery Time | $t_{WR}$ | 0 | | 0 | | 0 | | 0 | | ns |
| Write to Output High-Z | $t_{WHZ}$ | 0 | 25 | 0 | 30 | 0 | 30 | 0 | 40 | ns |
| Data to Write Time Overlap | $t_{DW}$ | 30 | | 40 | | 40 | | 50 | | ns |
| Data Hold from Write Time | $t_{DH}$ | 0 | | 0 | | 0 | | 0 | | ns |
| End Write to Output Low-Z | $t_{OW}$ | 5 | | 5 | | 5 | | 5 | | ns |

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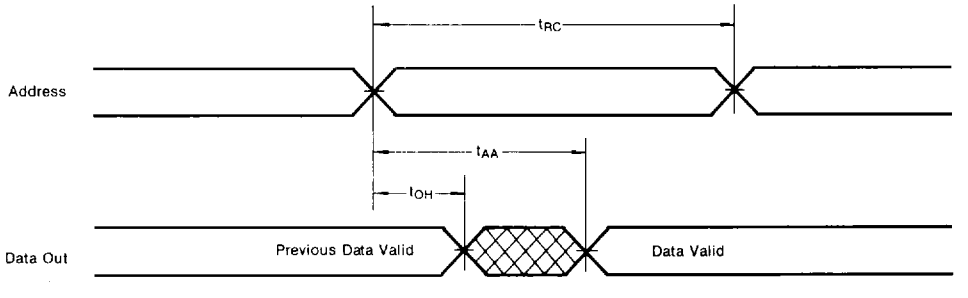
# TIMING DIAGRAMS

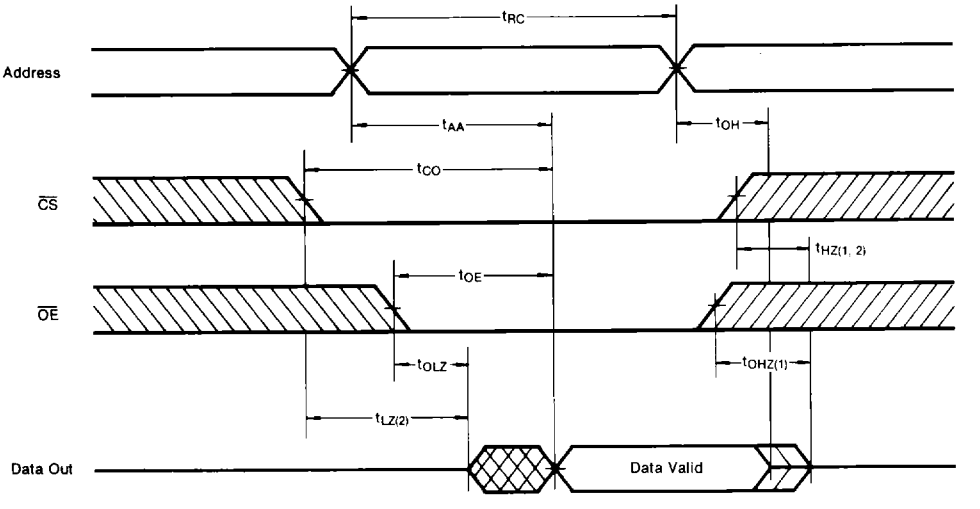
### TIMING WAVEFORM OF READ CYCLE (1) (Address Controlled)

($\overline{CS} = \overline{OE} = V_{IL}$, $\overline{WE} = V_{IH}$)



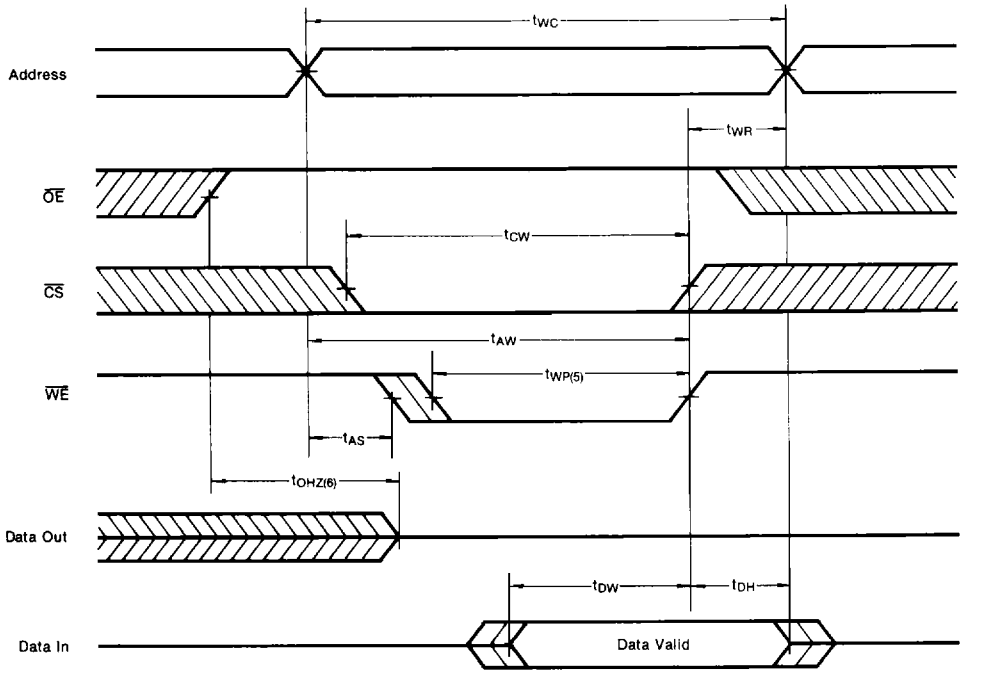
## TIMING WAVEFORM OF READ CYCLE (2)

($\overline{WE}$ = $V_{IH}$) (Note 1, 2, 3, 4)



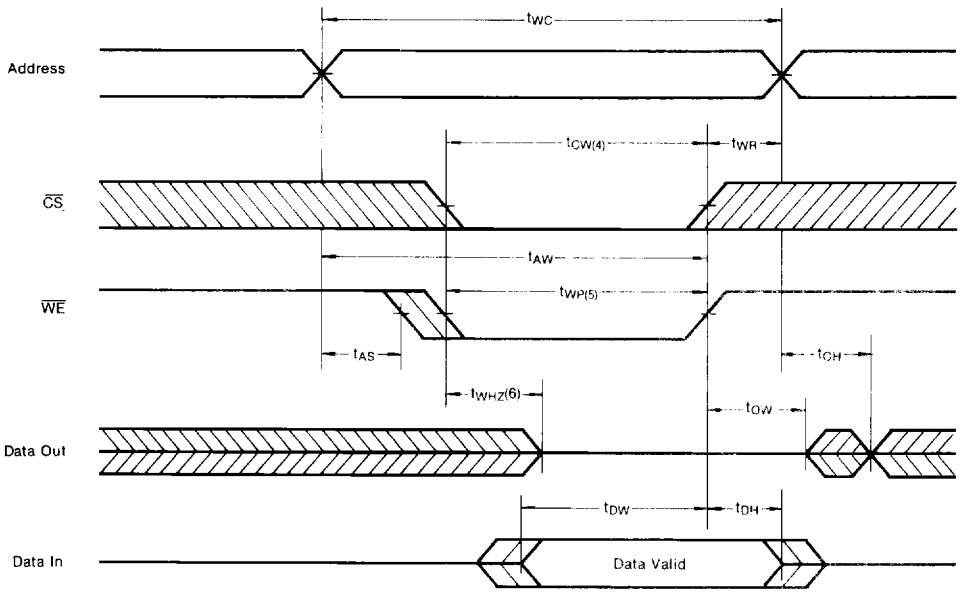

## TIMING WAVEFORM OF WRITE CYCLE (3)

($\overline{OE}$ Clocked) (Note 5, 6, 7, 8)



## TIMING WAVEFORM OF WRITE CYCLE (4)

($\overline{OE}$ Low Fixed) (Note 5, 6, 7, 8, 9)




### Notes

1. $t_{HZ}$ and $t_{OHZ}$ are defined as the time at which the outputs achieve the open circuit condition and are not referenced to the $V_{OH}$ or $V_{OL}$ level.
2. At any given temperature and voltage condition $t_{HZ}$ (max.) is less than $t_{LZ}$ (min.) both for a given device and from device to device.
3. $\overline{WE}$ is high for read cycle.
4. Address valid prior to or coincident with $\overline{CS}$ transition Low.
5. A write occurs during the overlap ($t_{WP}$) of a low $\overline{CS}$ and $\overline{WE}$.
6. During this period, I/O pins are in the output state. The input signals out of phase must not applied.
7. $\overline{CS}$ or $\overline{WE}$ must be high during address transition state.
8. If $\overline{OE}$ is high, I/O pins remain in a high-impedance state.
9. $\overline{OE}$ is continuously low ($\overline{OE} = V_{IL}$).

## FUNCTIONAL DESCRIPTION

| $\overline{CS}$ | $\overline{WE}$ | $\overline{OE}$ | Mode | I/O Pin | $V_{CC}$ Current |
|---|---|---|---|---|---|
| H | X* | X | Power Down | High-Z | $I_{SB}$, $I_{SB1}$ |
| L | H | H | Output Disable | High-Z | $I_{CC}$ |
| L | H | L | Read | $D_{OUT}$ | $I_{CC}$ |
| L | L | X | Write | $D_{IN}$ | $I_{CC}$ |

* X means Don't Care.

## DATA RETENTION CHARACTERISTICS ($T_A$ = 0 to 70°C)

| Parameter | Symbol | Test Condition | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $V_{CC}$ for Data Retention | $V_{DR}$ | $\overline{CS} \geq V_{CC} - 0.2V$ | | 2.0 | | 5.5 | V |
| Data Retention Current | $I_{DR}$ | $V_{CC}$ = 3.0V<br>$\overline{CS} \geq V_{CC} - 0.2V$ | L | | 1 | 50* | μA |
| | | | L-L | | 0.5 | 10** | μA |
| Data Retention Set-up Time | $t_{SDR}$ | See Data Retention Waveforms (below) | | 0 | | | ns |
| Recovery Time | $t_{RDR}$ | | | $t_{RC}$*** | | | ns |

* 20μA (Max.) at 0°C ~ 40°C
** 3μA (Max.) at 0°C ~ 40°C
*** $t_{RC}$: Read Cycle Time

## DATA RETENTION WAVEFORM ($\overline{CS}$ Controlled)