- To activate a UART you will need to turn on the UART clock in the **RCGC1** register.

- You should also turn on the clock for the digital port in the **RCGC2** register.

- You need to enable the transmit and receive pins as digital signals.

- The alternative function for these pins must also be selected.

In particular we set bits in both the **AFSEL** and **PCTL** registers.

- The OE, BE, PE, and FE are error flags associated with the receiver. You can see these flags in two places: associated with each data byte in **UART0\_DR\_R** or as a separate error register **in UART0\_RSR\_R**.

- The software can clear these four error flags by writing any value to UART0\_RSR\_R.

- The status of the two FIFOs can be seen in the **UART0\_FR\_R** register.

- The status of the two FIFOs can be seen in the **UART0\_FR\_R** register. The BUSY flag is set while the transmitter still has unsent bits, even if the transmitter is disabled. It will become zero when the transmit FIFO is empty and the last stop bit has been sent. If you implement busy-wait output by first outputting then waiting for BUSY to become 0 (right flowchart of Figure 11.10), then the routine will write new data and return after that particular data has been completely transmitted.

- The **UART0\_CTL\_R** control register contains the bits that turn on the UART. **TXE** is the Transmitter Enable bit, and **RXE** is the Receiver Enable bit. We set **TXE**, **RXE**, and UARTEN equal to 1 in order to activate the UART device. However, we should clear **UARTEN** during the initialization sequence.

- The **IBRD** and **FBRD** registers specify the baud rate. The baud rate divider is a 22-bit binary fixed-point value with a resolution of 2-6.

- The three registers **LCRH**, **IBRD**, and **FBRD** form an internal 30-bit register. This internal register is only updated when a write operation to **LCRH** is performed, so any changes to the baud-rate divisor must be followed by a write to the **LCRH** register for the changes to take effect. Out of reset, both FIFOs are disabled and act as 1-byte-deep holding registers. The FIFOs are enabled by setting the **FEN** bit in **LCRH**.