Design Note — C16QS Carrier Board (v1)

1. Functional Overview

This board is a minimal-component carrier for the Cavli C16QS LTE Cat-1 bis module. It provides regulated power, level-shifted UART, SIM card interface, RF antenna connection, hardware control signals, and basic debug access.

The design follows Cavli's reference hardware requirements for power, RF routing, SIM connectivity, and control interfaces.

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2. Power Architecture

The board is powered from a 5 V external supply connected at J1. A synchronous buck regulator (AP62250WU) generates the module supply voltage VBAT.

The regulator output is set using the resistor divider R3 and R4 to approximately 3.8 V, which lies safely within the C16QS operating range.

The inductor L1 and capacitors C6 and C7 form the switching and output filter network recommended in the regulator datasheet. Additional local decoupling capacitors (C1–C4) are placed directly at the module's VBAT pins to handle high-frequency current transients during LTE transmission.

The regulator is sized to handle the module's peak current during transmit bursts, providing sufficient margin above the expected maximum load.

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3. UART Level Shifting

The C16QS uses 1.8 V logic levels, while the external host operates at 3.3 V. A TXS0104ED bidirectional level translator is used to safely interface between these voltage domains.

VCCA is connected to the module's 1.8 V domain and VCCB is connected to the 3.3 V host supply. Series resistors on the UART lines reduce ringing and EMI. The UART interface is brought out to J_UART1 for external connection and debugging.

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4. USIM Interface

The SIM interface connects the C16QS to a nano-SIM socket. The clock, reset, and data lines include small series resistors for signal integrity. TVS diodes protect the SIM lines from ESD events caused by user insertion or removal.

Local decoupling is placed close to the SIM socket to stabilize the SIM supply and suppress noise.

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5. RF and Antenna Layout

The RF output from the module is routed directly to a u.FL connector for an external LTE antenna.

The RF trace is kept short, straight, and free of stubs or vias. It is routed on the top layer over a continuous ground plane to maintain controlled impedance. Ground stitching vias surround the RF area and the connector shield pads to provide a low-inductance return path and reduce radiation.

Copper keep-out is enforced around the RF trace to prevent coupling from digital or switching signals.

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6. Control, Reset, and Status

The power-key and reset signals are accessible through a header to allow external control and debugging.

A NET_STATUS output drives a transistor that switches a visible LED. This allows network status indication without loading or stressing the module's GPIO.

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7. Mechanical and Manufacturing

The PCB uses a simple two-layer construction to reduce cost and complexity. All components are surface-mount and compatible with standard automated assembly.

Mounting holes provide mechanical support. Silkscreen includes board identification and reference markings.

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8. Compliance Summary

The design meets the C16QS hardware requirements for supply voltage range, peak current capability, SIM interface protection, RF impedance control, logic-level compatibility, and required control signals.

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9. Conclusion

This carrier board provides a stable, electrically compliant, and manufacturable platform for integrating the C16QS LTE module into host systems. The design emphasizes power integrity, RF signal quality, and interface protection while keeping the BOM and layout simple.