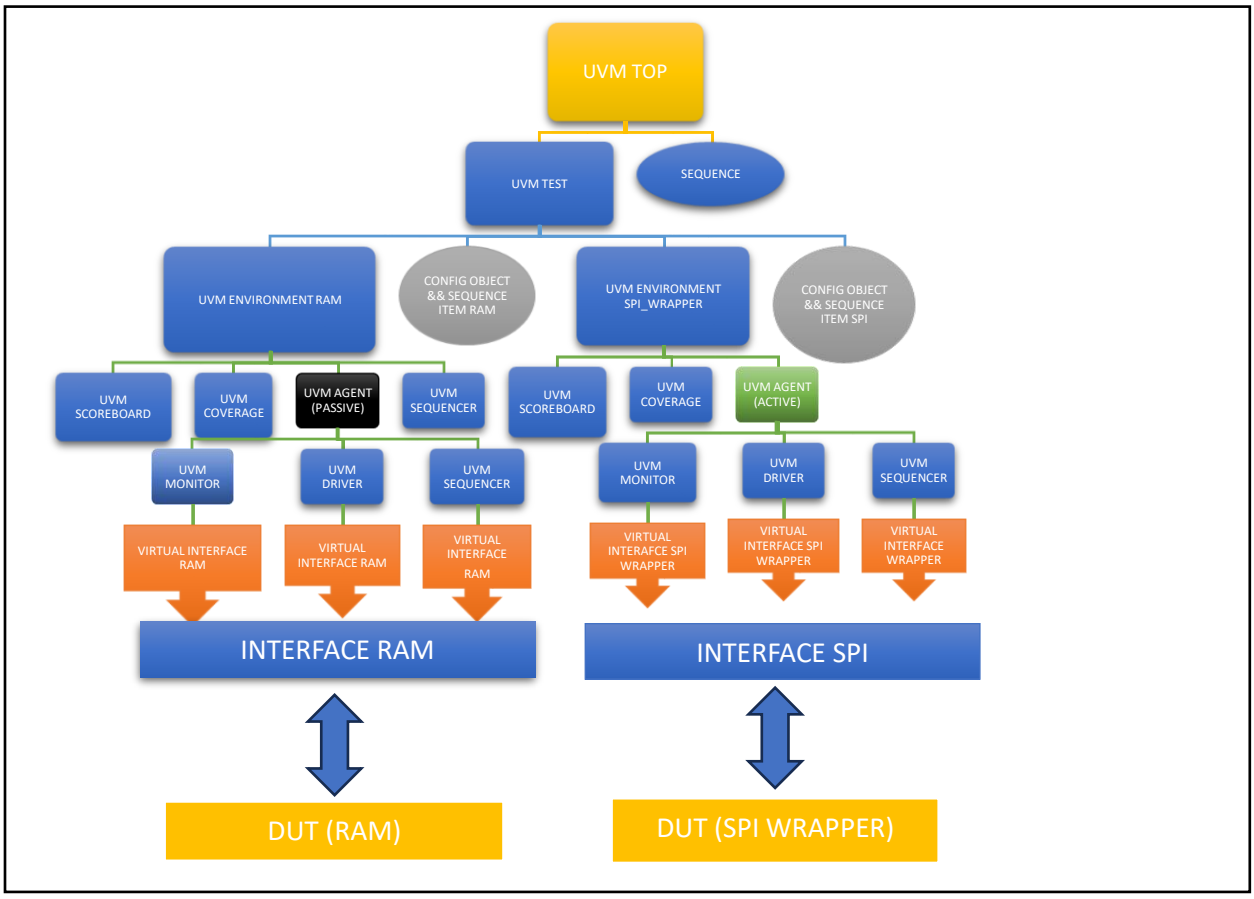
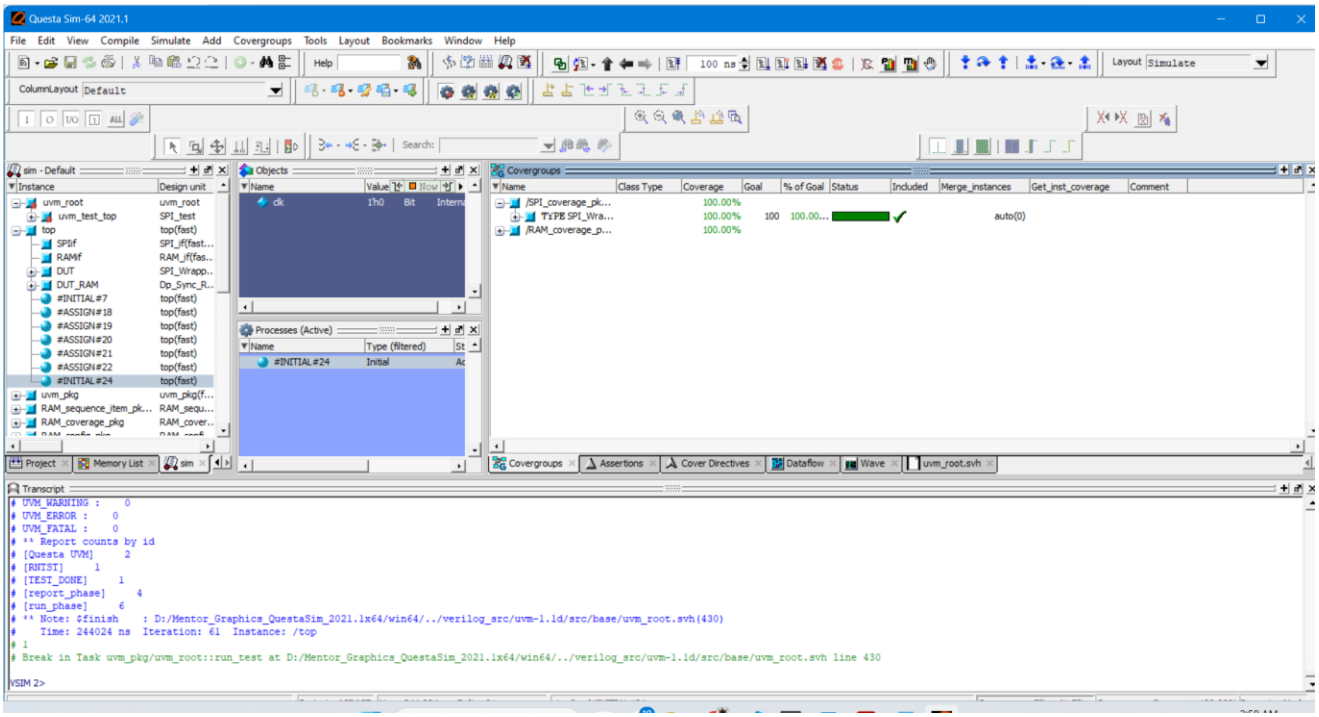
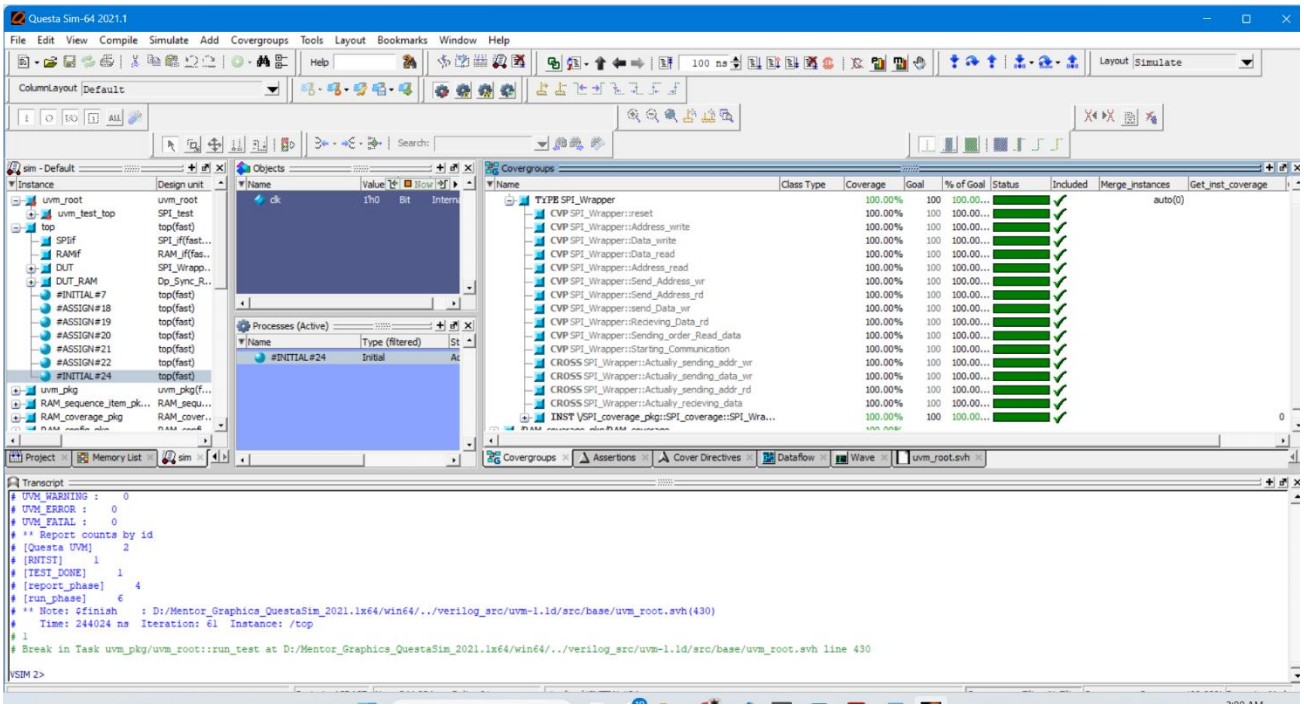
UVM Project


UVM TOP
UVM TEST
SEQUENCE
UVM ENVIRONMENT RAM
CONFIG OBJECT && SEQUENCE ITEM RAM
UVM ENVIRONMENT SPI_WRAPPER
CONFIG OBJECT && SEQUENCE ITEM SPI
UVM SCOREBOARD
UVM COVERAGE
UVM AGENT (PASSIVE)
UVM SEQUENCER
UVM SCOREBOARD
UVM COVERAGE
UVM AGENT (ACTIVE)
UVM MONITOR
UVM DRIVER
UVM SEQUENCER
UVM MONITOR
UVM DRIVER
UVM SEQUENCER
VIRTUAL INTERFACE RAM
VIRTUAL INTERFACE RAM
VIRTUAL INTERFACE RAM
VIRTUAL INTERAFCE SPI WRAPPER
VIRTUAL INTERFACE SPI WRAPPER
VIRTUAL INTERFACE WRAPPER
INTERFACE RAM
INTERFACE SPI
DUT (RAM)
DUT (SPI WRAPPER)

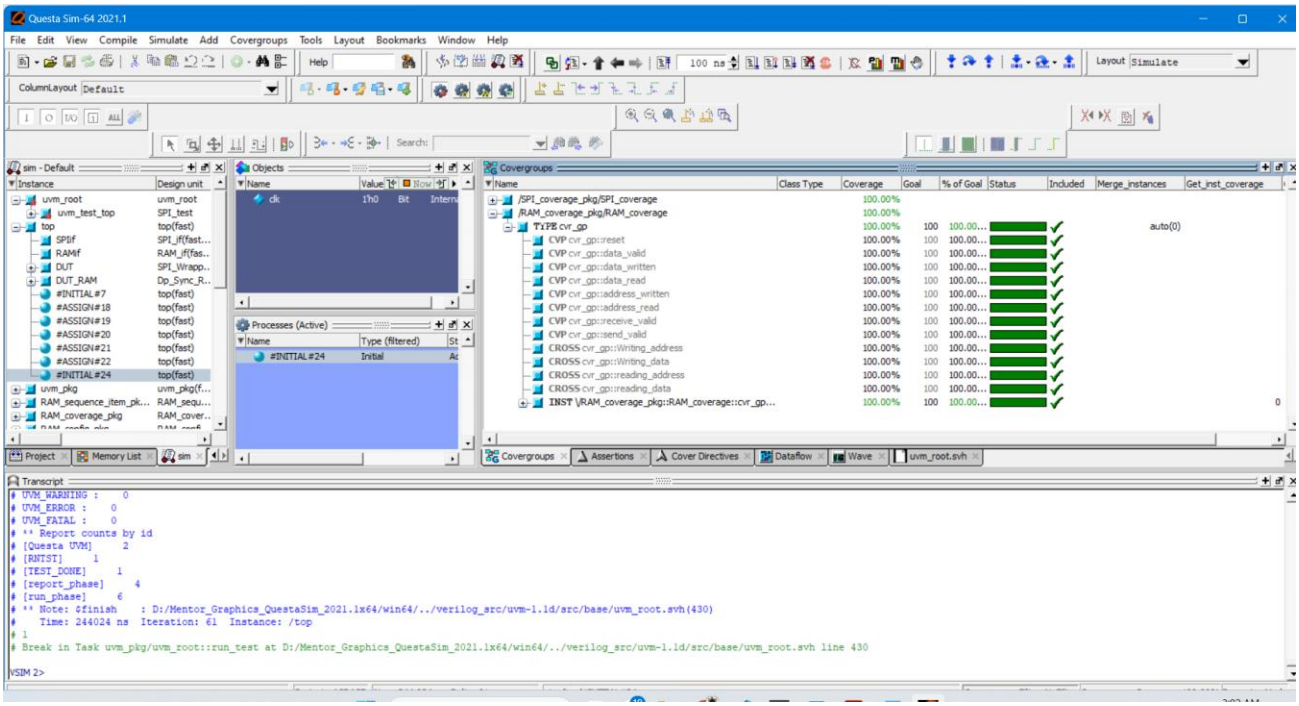
F_Coverage:



SPI F_Coverage:



RAM Coverage:



Do file

```
vlib work
vlog -f slc_file.txt -sv +cover
vsim -voptargs=+acc work.top -classdebug -uvmcontrol=all -coverage
run 0
coverage save RAM_CV.ucdb -onexit -du Dp_Sync_RAM_wrapper
run -all
quit -sim
vcover report RAM_CV.ucdb -all -annotate -details -output code_coverage_RAM.txt
vlib work
vlog -f slc_file.txt -sv +cover
vsim -voptargs=+acc work.top -classdebug -uvmcontrol=all -coverage
run 0
coverage save SPI_Wrapper_CV.ucdb -onexit -du SPI_Wrapper
run -all
quit -sim
vcover report SPI_Wrapper_CV.ucdb -all -annotate -details -output code_coverage_SPI_Wrapper.txt
vlib work
vlog -f slc_file.txt -sv +cover
vsim -voptargs=+acc work.top -classdebug -uvmcontrol=all -coverage
run 0
run -all
coverage report -detail -cvg -comments -output fcover_report.txt {}
quit -sim
```

RAM bugs from previous project:

- RAM bugs:

```
15      integer i;
16      always @(posedge clk or negedge rst_n) begin
17          if (!rst_n) begin
18             dout <= 0;
19             for(i=0; i<MEM_DEPTH; i=i+1)
20              mem[i] <= 0;
21          end
22          else if (rx_valid) begin
23             tx_valid <= 0;
24             case (din[9:8])
25              2'b00: addr_wr <= din[7:0];
26              2'b01: mem[addr_wr] <= din[7:0];
27              2'b10: addr_rd <= din[7:0];
28              2'b11: {dout, tx_valid} <= {mem[addr_rd], 1'b1};
29             endcase
30          end
31      end
32
```

1) rst_n must be Async.
2) rst_n doesn't clear the RAM.
3) When rest asserted the internal signals (addr_rd,addr_wr) and output signal (dout and tx_valid) must equal zeros.

Handling:

```
19      always @(posedge clk ) begin // first bug : rst must be syncrouns no Ashync
20          if (!rst_n) begin
21             dout <= 0;
22             tx_valid <= 0; //second bug : tx must take zero when rst_n is asserted
23             wr_addr <= 0 ;
24             rd_addr <= 0 ;//3th bug : when rst_n asserted , addr and not 2 internal signals it only one
25          end
26          else if (rx_valid) begin
27             tx_valid <= 0;
28              case (din[9:8])
29              2'b00:  wr_addr  <= din[7:0];
30              2'b01: mem[wr_addr] <= din[7:0];
31              2'b10: rd_addr <= din[7:0];
32              default: {dout, tx_valid} <= {mem[rd_addr], 1'b1};
33             endcase
34          end
35          else begin
36              tx_valid  <= 0 ;
37          end
38           //4th bug : when rx_valid not asserted then tx_valid must down to zero
39      end
```

SPI bugs also from previous project:

- SPI bugs:

```
12      reg [2:0] cs, ns;
13      reg [9:0] PO;
14      wire [7:0] temp;
15      reg SO, flag_rd = 0;
16      integer state_count = 0, final_count = 0;
17
18      assign temp = (tx_valid)? tx_data: temp;
19      assign MISO = SO;
20
21      always @(posedge clk or negedge rst_n) begin
22          if (!rst_n)
23              cs <= IDLE;
24          else
25              cs <= ns;
26      end
```

4) rst_n must be Async.
5) When reset is asserted the flags and counters must flush and data_out signals must also zeros.

Handling:

```
28      always @(cs) begin
29          case (cs)
30                IDLE: rx_valid = 0;
31                WRITE: rx_valid = 1;
32                READ_ADD: rx_valid = 1;
33                READ_DATA: rx_valid = 1;
34                default: rx_valid = 0;
35          endcase
36      end
37
38      always @(posedge clk or negedge SS_n) begin
39          if ((cs == WRITE) || (cs == READ_ADD) || (cs == READ_DATA)) begin
40              PO <= {PO[8:0], MOSI}; state_count <= state_count + 1;
41              if (state_count == 10) begin
42              rx_data <= PO; state_count <= 0;
43              end
44          end
45          if (rx_data[9:8] == 2'b11 && temp) begin
46              SO <= temp[7-final_count];
47              final_count <= final_count + 1;
48              if (final_count == 10)
49              final_count <= 0;
50          end
51      end
```

- **Current state bugs:**

```
28      always @(cs) begin
29          case (cs)
30                IDLE: rx_valid = 0;
31                WRITE: rx_valid = 1;
32                READ_ADD: rx_valid = 1;
33                READ_DATA: rx_valid = 1;
34                default: rx_valid = 0;
35          endcase
36      end
```

Handle:

```
52  always @(posedge clk) begin//* bug
53
54      case (cs)
55          IDLE : begin
56
57              rx_valid = 0 ;
58              PO  = 0 ;
59              state_count = 0 ;
60              final_count = 0 ;
61              SO = 0 ;
62              Act_input_output = 0;
63                  end
64          WRITE: begin //done
65
66              if (state_count < 10 )begin //0 ,
67                  PO = {PO[8:0] , MOSI} ;
68                  state_count = state_count + 1 ;
69                  if (PO[9] ==1'b0 && state_count ==10)begin
70                      rx_valid = 1 ;
71                  end
72                  else
73                      rx_valid = 0 ;
74              end
75              else
76                  rx_valid = 0 ;
77
78                  end
```

```
            READ_ADD: begin // done

              if (state_count<10 )begin
                  PO = {PO[8:0] , MOSI} ;
                  state_count = state_count + 1 ;
                  rx_valid = 0 ;
              end
              if (PO[9:8]==2'b10 && state_count==10)begin
                  rx_valid = 1 ;
                  flag_rd = 1;
              end
              else
                  rx_valid = 0 ;
                  end
            READ_DATA: begin // done

              if (Act_input_output == 0)begin
                  if (state_count<9 )begin
                      PO = {PO[8:0] , MOSI} ;
                      state_count = state_count + 1 ;
                      rx_valid = 0 ;
                  end
                  else begin
                      PO = {PO[8:0] , MOSI} ;
                      state_count = state_count + 1 ;
                      rx_valid = 0 ;
                  end

                  if (PO[9:8]==2'b11 && state_count== 10 )begin
                      rx_valid = 1 ;
                      Act_input_output = 1;
                      flag_rd = 0;
                  end
              end
              else begin
                  state_count = state_count + 1 ;
                  rx_valid = 0 ;
                  if (tx_valid && state_count == 12 )begin
                      temp = tx_data ;
                  end
                  if (state_count >= 12 && final_count <= 7)begin
                      SO = temp [7 - final_count ];
                      rx_valid =0 ;
                      final_count = final_count + 1 ;
                  end
              end
                  end
              default: begin
                rx_valid = 0 ;
                PO  = 0 ;
                state_count = 0 ;
                final_count = 0 ;
                SO = 0 ;
                Act_input_output = 0;

                  end
              endcase
    end
```

- **Bugs flag of read operation:**

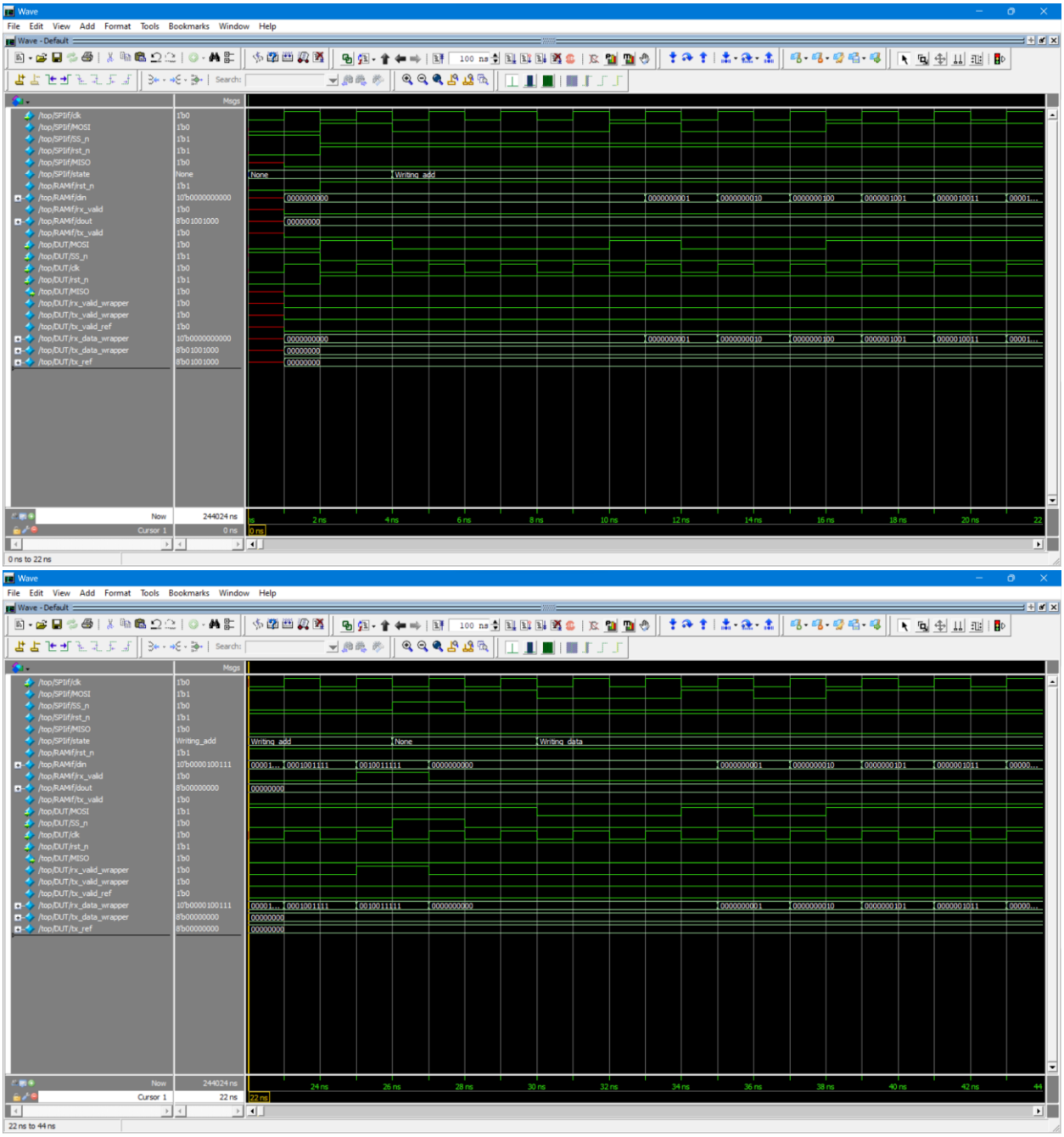
```
    always @(MOSI, SS_n, cs) begin
        case (cs)
              IDLE:
            if (SS_n)
                ns = IDLE;
            else
                ns = CHK_CMD;
              CHK_CMD:
            if (SS_n)
                ns = IDLE;
            else begin
                if (!MOSI)
                ns = WRITE;
                else begin
                if (!flag_rd)
                    ns = READ_ADD;
                else
                    ns = READ_DATA;
                end
            end
              WRITE:
            if (SS_n)
                ns = IDLE;
            else
                ns = WRITE;
              READ_ADD:
            if (SS_n)
                ns = IDLE;
            else begin
                ns = READ_ADD; flag_rd = 1;
            end
              READ_DATA:
            if (SS_n)
                ns = IDLE;
            else begin
                ns = READ_DATA; flag_rd = 0;
            end
              default: ns = IDLE;
        endcase
    end
```

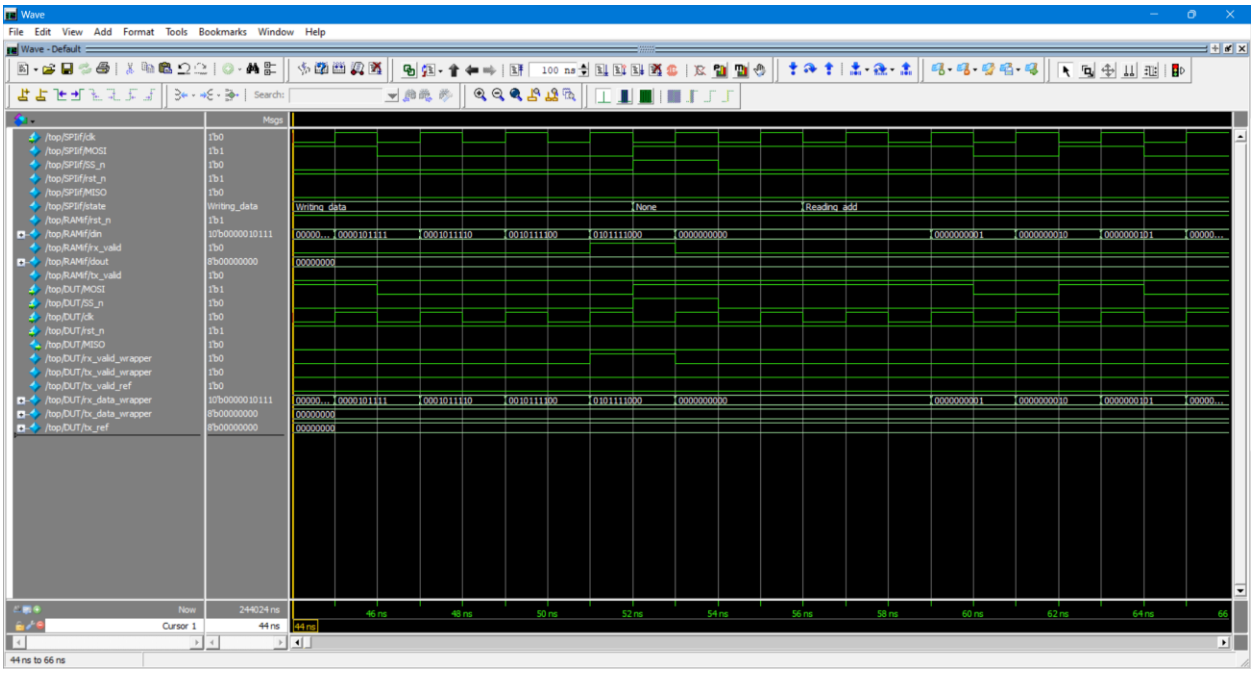
Handle:

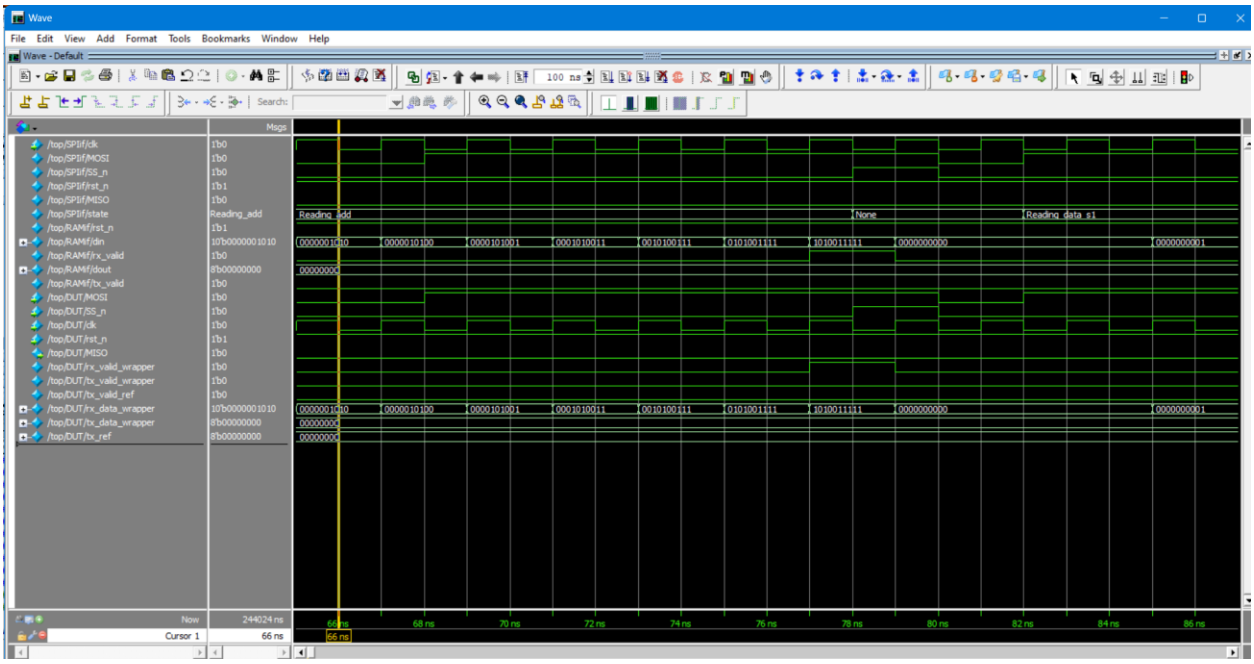
The value of the flag changed in current state (reading data or address) block not here.

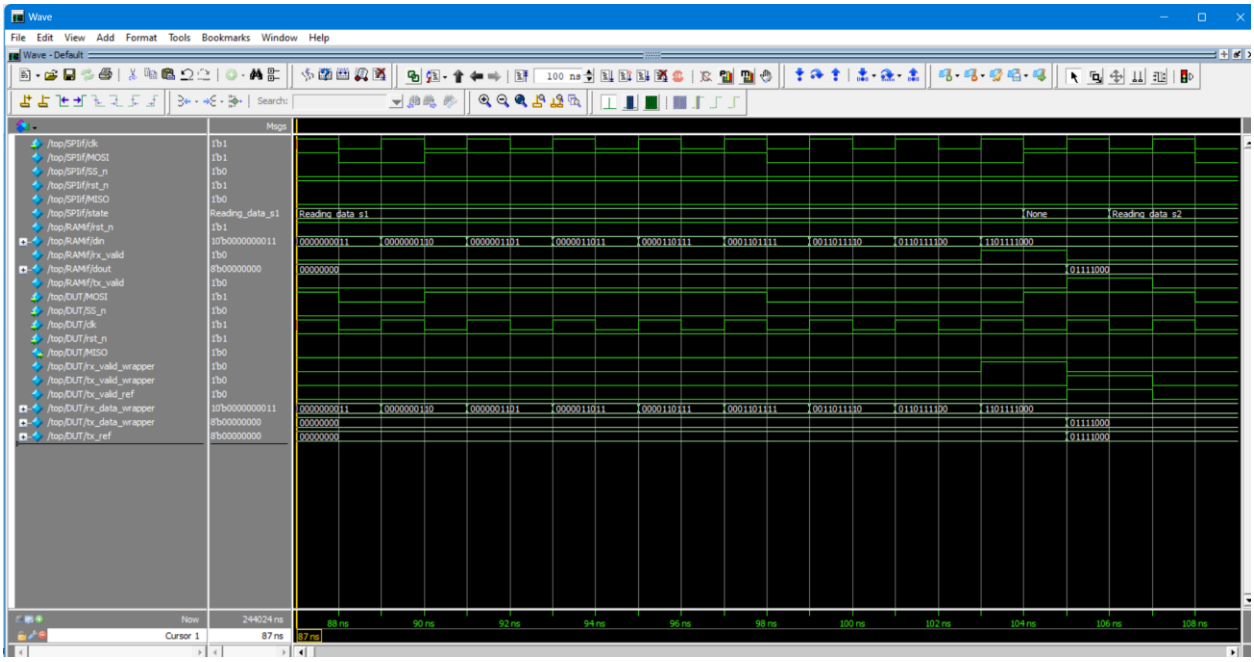
```
138     always @(*) begin
139
140         case (cs)
141             IDLE:
142                 if (SS_n)
143                     ns = IDLE;
144                 else
145                     ns = CHK_CMD;
146             CHK_CMD:
147                 if (SS_n)
148                     ns = IDLE;
149                 else begin//SS_n = 0
150                     if (MOSI==0) //MOSI = 0
151                         ns = WRITE;
152                     else  begin //MOSI = 1
153                         if (!flag_rd) //flag_rd = 0
154                             ns = READ_ADD;
155                         else  //flag_rd = 1
156                             ns = READ_DATA;
157                     end
158                 end
159             WRITE:
160                 if (SS_n)
161                     ns = IDLE;
162                 else
163                     ns = WRITE;
164             READ_ADD:
165                 if (SS_n)
166                     ns = IDLE;
167                 else begin
168                     ns = READ_ADD;
169                     // flag_rd = 1;
170                 end
171             READ_DATA:
172                 if (SS_n)
173                     ns = IDLE;
174                 else begin
175                     ns = READ_DATA;
176                     // flag_rd = 0;
177                 end
178
179             default: ns = IDLE;
180         endcase
181     end
182
```

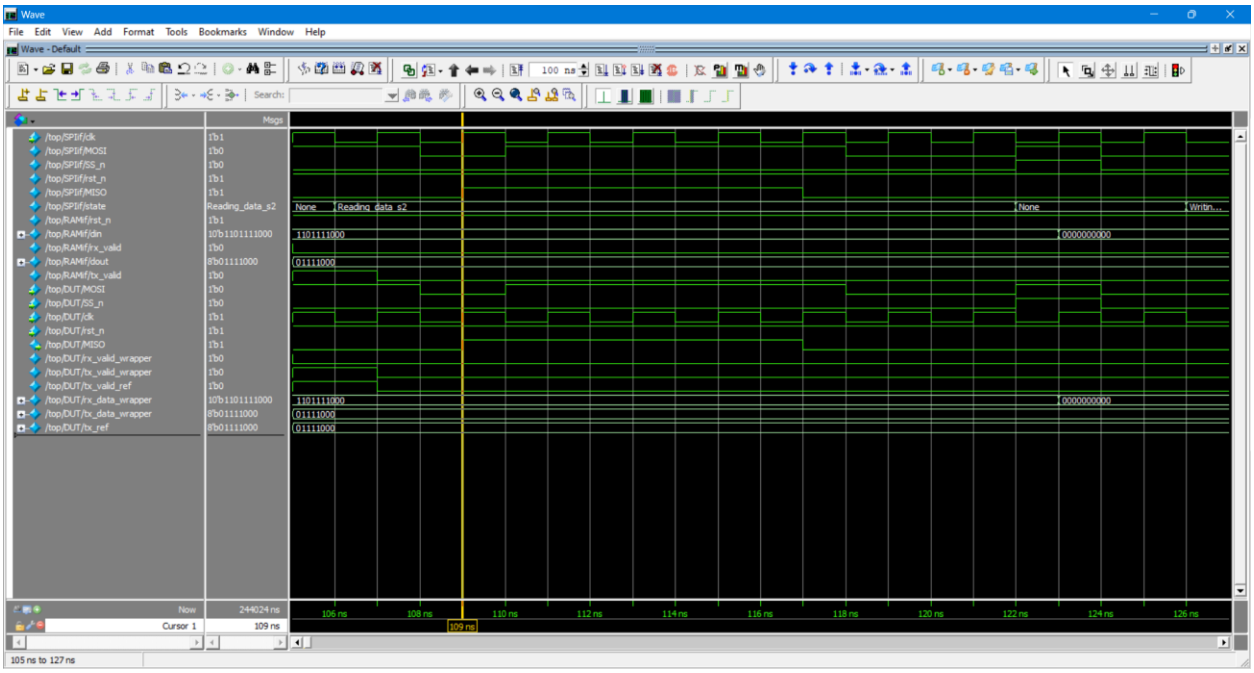
Questa snippets from part 3 :(for one cycle of first sequence):

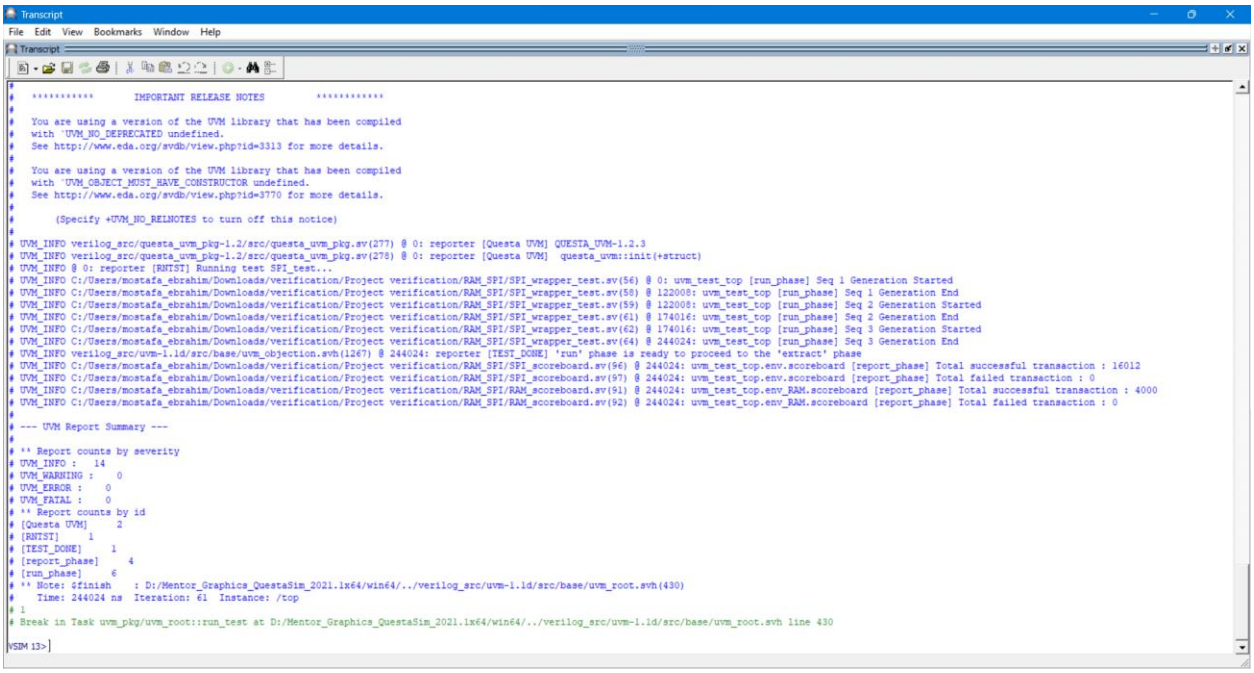



Wave
File Edit View Add Format Tools Bookmarks Window Help
Wave - Default
Msgs
/top/SPIf/clk
/top/SPIf/MOSI
/top/SPIf/SS_n
/top/SPIf/rst_n
/top/SPIf/MISO
/top/SPIf/state
/top/RAMf/rst_n
/top/RAMf/din
/top/RAMf/rx_valid
/top/RAMf/dout
/top/RAMf/tx_valid
/top/DUT/MOSI
/top/DUT/SS_n
/top/DUT/clk
/top/DUT/rst_n
/top/DUT/MISO
/top/DUT/rx_valid_wrapper
/top/DUT/tx_valid_wrapper
/top/DUT/tx_valid_ref
/top/DUT/rx_data_wrapper
/top/DUT/tx_data_wrapper
/top/DUT/tx_ref
Writing_data
None
Reading_add
Now
244024 ns
Cursor 1
44 ns
44 ns to 66 ns


Wave
File Edit View Add Format Tools Bookmarks Window Help
Wave - Default
Msgs
/top/SPIf/clk
/top/SPIf/MOSI
/top/SPIf/SS_n
/top/SPIf/rst_n
/top/SPIf/MISO
/top/SPIf/state
/top/RAMf/rst_n
/top/RAMf/din
/top/RAMf/rx_valid
/top/RAMf/dout
/top/RAMf/tx_valid
/top/DUT/MOSI
/top/DUT/SS_n
/top/DUT/clk
/top/DUT/rst_n
/top/DUT/MISO
/top/DUT/rx_valid_wrapper
/top/DUT/tx_valid_wrapper
/top/DUT/tx_valid_ref
/top/DUT/rx_data_wrapper
/top/DUT/tx_data_wrapper
/top/DUT/tx_ref
Reading_add
None
Reading_data_s1
Now
244024 ns
Cursor 1
66 ns


Wave
File Edit View Add Format Tools Bookmarks Window Help
Wave - Default
/top/SPIif/clk
/top/SPIif/MOSI
/top/SPIif/SS_n
/top/SPIif/rst_n
/top/SPIif/MISO
/top/SPIif/state
/top/RAMif/rst_n
/top/RAMif/din
/top/RAMif/rx_valid
/top/RAMif/dout
/top/RAMif/tx_valid
/top/DUT/MOSI
/top/DUT/SS_n
/top/DUT/clk
/top/DUT/rst_n
/top/DUT/MISO
/top/DUT/rx_valid_wrapper
/top/DUT/tx_valid_wrapper
/top/DUT/tx_valid_ref
/top/DUT/rx_data_wrapper
/top/DUT/tx_data_wrapper
/top/DUT/tx_ref
Reading_data_s1
None
Reading_data_s2
01111000
Now
Cursor 1
87 ns


Wave
File Edit View Add Format Tools Bookmarks Window Help
Wave - Default
/top/SPIif/clk
/top/SPIif/MOSI
/top/SPIif/SS_n
/top/SPIif/rst_n
/top/SPIif/MISO
/top/SPIif/state
/top/RAMif/rst_n
/top/RAMif/din
/top/RAMif/rx_valid
/top/RAMif/dout
/top/RAMif/tx_valid
/top/DUT/MOSI
/top/DUT/SS_n
/top/DUT/clk
/top/DUT/rst_n
/top/DUT/MISO
/top/DUT/rx_valid_wrapper
/top/DUT/tx_valid_wrapper
/top/DUT/tx_valid_ref
/top/DUT/rx_data_wrapper
/top/DUT/tx_data_wrapper
/top/DUT/tx_ref
None
Reading_data_s2
Writin...
01111000
Now
Cursor 1
109 ns
105 ns to 127 ns



- **The following will be:**
  1. **RAM code coverage.**
  2. **Wrapper code coverage.**
  3. **Assertion (that I didn't do it)**
  4. **Functional coverage for RAM**
  5. **Functional coverage for wrapper**

Code Coverage reports:

RAM code coverage

Coverage Report by instance with details

```
================================================================================
=== Instance: /\top#DUT_RAM
=== Design Unit: work.Dp_Sync_RAM_wrapper
================================================================================
```

Branch Coverage:

Enabled Coverage	Bins	Hits	Misses	Coverage
Branches	7	7	0	100.00%

```
================================Branch Details================================

Branch Coverage for instance /\top#DUT_RAM

    Line       Item                 Count     Source
    ----       ----                 -----     ------
  File Dp_Sync_RAM.sv
-----------------------------------IF Branch-----------------------------------
    16                              122012     Count coming in to IF
    16         1                    12                                    if (!rst_n) begin
    22         1                    8000                          else if (rx_valid) begin
    31         1                    114000                        else begin
Branch totals: 3 hits of 3 branches = 100.00%

---------------------------------CASE Branch-----------------------------------
    24                              8000     Count coming in to CASE
    25         1                    2000                                  2'b00:  wr_addr  <= din[7:0];
    26         1                    2000                                  2'b01: mem[wr_addr] <= din[7:0];
    27         1                    2000                                  2'b10: rd_addr <= din[7:0];
    28         1                    2000                                  default: {dout, tx_valid} <=
{mem[rd_addr], 1'b1};
Branch totals: 4 hits of 4 branches = 100.00%
```

Statement Coverage:

Enabled Coverage	Bins	Hits	Misses	Coverage
Statements	13	13	0	100.00%

```
================================Statement Details================================

Statement Coverage for instance /\top#DUT_RAM  --

    Line       Item                 Count     Source
    ----       ----                 -----     ------
  File Dp_Sync_RAM.sv
    1                               module Dp_Sync_RAM_wrapper(rst_n, din, rx_valid, dout, tx_valid);
    2                                   parameter MEM_DEPTH = 256;
    3                                   parameter ADDR_SIZE = 8;
    4
    5                                   input rst_n, rx_valid;
    6                                   input [9:0] din;
    7                                   output reg tx_valid;
    8                                   output reg [7:0] dout;
    9
```

```
   10                                   reg [7:0] mem [MEM_DEPTH-1:0];
   11                                   reg [ADDR_SIZE-1:0] rd_addr,wr_addr ;
   12
   13                                   initial begin // first bug : rst must be syncrouns no Ashync
   14          1            1                   #1
   15          1            1                   forever begin
   16                                                   if (!rst_n) begin
   17          1            12                      dout <= 0;
   18          1            12                      tx_valid <= 0; //second bug : tx must take
zero when rst_n is asserted
   19          1            12                      wr_addr <= 0 ;
   20          1            12                      rd_addr <= 0 ;//3th bug : when rst_n
asserted , addr and not 2 internal signals it only one
   21                                               end
   22                                               else if (rx_valid) begin
   23          1            8000                    tx_valid <= 0;
   24                                               case (din[9:8])
   25          1            2000                            2'b00:  wr_addr  <= din[7:0];
   26          1            2000                            2'b01: mem[wr_addr] <= din[7:0];
   27          1            2000                            2'b10: rd_addr <= din[7:0];
   28          1            2000                            default: {dout, tx_valid} <=
{mem[rd_addr], 1'b1};
   29                                               endcase
   30                                               end
   31                                               else begin
   32          1            114000                          tx_valid  <= 0 ;
   33                                               end
   34                                               //4th bug : when rx_valid not asserted then
tx_valid must down to zero
   35          1            122012                  #2;
```

Toggle Coverage:

Enabled Coverage	Bins	Hits	Misses	Coverage
Toggles	74	74	0	100.00%

==========Toggle Details==========

Toggle Coverage for instance /\top#DUT_RAM --

Node	1H->0L	0L->1H	"Coverage"
din[0-9]	1	1	100.00
dout[7-0]	1	1	100.00
rd_addr[7-0]	1	1	100.00
rst_n	1	1	100.00
rx_valid	1	1	100.00
tx_valid	1	1	100.00
wr_addr[7-0]	1	1	100.00

Total Node Count = 37
Toggled Node Count = 37
Untoggled Node Count = 0

Toggle Coverage = 100.00% (74 of 74 bins)

	Total Coverage By Instance (filtered view): 100.00%
SPI_wrapper code coverage (SPI_slave code coverage)	Coverage Report by instance with details ========== === Instance: /\top#DUT /DUT_2 === Design Unit: work.SPI_Slave_wrapper ========== **Branch Coverage:** **Enabled Coverage Bins Hits Misses Coverage** **---------- ---- ---- ------ --------** **Branches 47 46 1 97.87%** ==========Branch Details========== Branch Coverage for instance /\top#DUT /DUT_2 Line Item Count Source ---- ---- ----- ------ File SPI_Slave.sv ----------IF Branch---------- 25 122012 Count coming in to IF 25 1 12 if (!rst_n)begin 32 1 122000 else Branch totals: 2 hits of 2 branches = 100.00% ----------IF Branch---------- 36 24001 Count coming in to IF 36 1 8001 if (cs == IDLE)begin 16000 All False Count Branch totals: 2 hits of 2 branches = 100.00% ----------CASE Branch---------- 48 122012 Count coming in to CASE 49 1 8011 IDLE : begin 58 1 44000 WRITE: begin //done 73 1 22000 READ_ADD: begin // done 87 1 40000 READ_DATA: begin // done 120 1 8001 default: begin Branch totals: 5 hits of 5 branches = 100.00% ----------IF Branch---------- 60 44000 Count coming in to IF 60 1 40000 if (state_count < 10)begin //0 , 69 1 4000 else Branch totals: 2 hits of 2 branches = 100.00% ----------IF Branch---------- 63 40000 Count coming in to IF 63 1 4000 if (PO[9] ==1'b0 && state_count ==10)begin 66 1 36000 else Branch totals: 2 hits of 2 branches = 100.00% ----------IF Branch---------- 75 22000 Count coming in to IF 75 1 20000 if (state_count<10)begin 2000 All False Count Branch totals: 2 hits of 2 branches = 100.00% ----------IF Branch---------- 80 22000 Count coming in to IF

```
   80          1                4000                                  if (PO[9:8]==2'b10 &&
state_count==10)begin
   84          1                18000                                 else
Branch totals: 2 hits of 2 branches = 100.00%

----------------------------------------IF Branch----------------------------------------
   89                           40000    Count coming in to IF
   89          1                20000                                 if (Act_input_output == 0)begin
   107         1                 20000                                else begin
Branch totals: 2 hits of 2 branches = 100.00%

----------------------------------------IF Branch----------------------------------------
   90                           20000    Count coming in to IF
   90          1                18000                                         if (state_count<9 )begin
   95          1                 2000                                    else begin
Branch totals: 2 hits of 2 branches = 100.00%

----------------------------------------IF Branch----------------------------------------
   101                          20000    Count coming in to IF
   101         1                 2000                                    if (PO[9:8]==2'b11 && state_count==
10 )begin
                                18000    All False Count
Branch totals: 2 hits of 2 branches = 100.00%

----------------------------------------IF Branch----------------------------------------
   110                          20000    Count coming in to IF
   110         1                 2000                                          if (tx_valid && state_count ==
12 )begin
                                18000    All False Count
Branch totals: 2 hits of 2 branches = 100.00%

----------------------------------------IF Branch----------------------------------------
   113                          20000    Count coming in to IF
   113         1                16000                                         if (state_count >= 12 &&
final_count <= 7)begin
                                 4000    All False Count
Branch totals: 2 hits of 2 branches = 100.00%

----------------------------------------CASE Branch----------------------------------------
   134                          92914    Count coming in to CASE
   135         1                16006                          IDLE:
   140         1                11967                          CHK_CMD:
   153         1                25982                          WRITE:
   158         1                15981                          READ_ADD:
   165         1                22977                          READ_DATA:
   173         1                   1                 default: ns = IDLE;
Branch totals: 6 hits of 6 branches = 100.00%

----------------------------------------IF Branch----------------------------------------
   136                          16006    Count coming in to IF
   136         1                 8006                                    if (SS_n)
   138         1                 8000                                    else
Branch totals: 2 hits of 2 branches = 100.00%

----------------------------------------IF Branch----------------------------------------
   141                          11967    Count coming in to IF
   141         1                ***0***                                 if (SS_n)
   143         1                 11967                                  else begin//SS_n = 0
Branch totals: 1 hit of 2 branches = 50.00%

----------------------------------------IF Branch----------------------------------------
   144                          11967    Count coming in to IF
   144         1                 5954                                      if (MOSI==0) //MOSI = 0
   146         1                 6013                                      else  begin //MOSI = 1
Branch totals: 2 hits of 2 branches = 100.00%
```

```
------------------------------------IF Branch------------------------------------
    147                  6013    Count coming in to IF
    147         1        4013                                        if (!flag_rd) //flag_rd = 0
    149         1        2000                                        else  //flag_rd = 1
Branch totals: 2 hits of 2 branches = 100.00%

------------------------------------IF Branch------------------------------------
    154                 25982    Count coming in to IF
    154         1        4000                                   if (SS_n)
    156         1       21982                                   else
Branch totals: 2 hits of 2 branches = 100.00%

------------------------------------IF Branch------------------------------------
    159                 15981    Count coming in to IF
    159         1        2000                                   if (SS_n)
    161         1       13981                                   else begin
Branch totals: 2 hits of 2 branches = 100.00%

------------------------------------IF Branch------------------------------------
    166                 22977    Count coming in to IF
    166         1        2000                                   if (SS_n)
    168         1       20977                                   else begin
Branch totals: 2 hits of 2 branches = 100.00%
```

Condition Coverage:

Enabled Coverage	Bins	Covered	Misses	Coverage
Conditions	14	10	4	71.42%

```
================================Condition Details================================

Condition Coverage for instance /\top#DUT /DUT_2 --

  File SPI_Slave.sv
----------------Focused Condition View-------------------
Line       36 Item    1  (cs == 0)
Condition totals: 1 of 1 input term covered = 100.00%

  Input Term   Covered  Reason for no coverage   Hint
 -----------  --------  -----------------------  --------------
  (cs == 0)        Y

    Rows:       Hits  FEC Target           Non-masking condition(s)
 ---------  ---------  --------------------  -------------------------
  Row   1:          1  (cs == 0)_0          -
  Row   2:          1  (cs == 0)_1          -

----------------Focused Condition View-------------------
Line       60 Item    1  (state_count < 10)
Condition totals: 1 of 1 input term covered = 100.00%

        Input Term   Covered  Reason for no coverage   Hint
       -----------  --------  -----------------------  --------------
  (state_count < 10)        Y

    Rows:       Hits  FEC Target           Non-masking condition(s)
 ---------  ---------  --------------------  -------------------------
  Row   1:          1  (state_count < 10)_0  -
  Row   2:          1  (state_count < 10)_1  -

----------------Focused Condition View-------------------
Line       63 Item    1  (~PO[9] && (state_count == 10))
Condition totals: 1 of 2 input terms covered = 50.00%
```

```
        Input Term   Covered  Reason for no coverage   Hint
        ----------- --------  ----------------------  --------------
             PO[9]        N  '_1' not hit           Hit '_1'
 (state_count == 10)        Y

    Rows:      Hits  FEC Target           Non-masking condition(s)
 --------- ---------  -------------------  -------------------------
 Row   1:         1  PO[9]_0              (state_count == 10)
 Row   2:    ***0***  PO[9]_1              -
 Row   3:         1  (state_count == 10)_0  ~PO[9]
 Row   4:         1  (state_count == 10)_1  ~PO[9]

----------------Focused Condition View--------------------
Line      75 Item    1  (state_count < 10)
Condition totals: 1 of 1 input term covered = 100.00%

       Input Term   Covered  Reason for no coverage   Hint
       ----------- --------  ----------------------  --------------
 (state_count < 10)        Y

    Rows:      Hits  FEC Target           Non-masking condition(s)
 --------- ---------  -------------------  -------------------------
 Row   1:         1  (state_count < 10)_0  -
 Row   2:         1  (state_count < 10)_1  -

----------------Focused Condition View--------------------
Line      80 Item    1  ((PO[9:8] == 2) && (state_count == 10))
Condition totals: 1 of 2 input terms covered = 50.00%

        Input Term   Covered  Reason for no coverage   Hint
        ----------- --------  ----------------------  --------------
     (PO[9:8] == 2)        Y
 (state_count == 10)        N  '_0' not hit           Hit '_0'

    Rows:      Hits  FEC Target           Non-masking condition(s)
 --------- ---------  -------------------  -------------------------
 Row   1:         1  (PO[9:8] == 2)_0      -
 Row   2:         1  (PO[9:8] == 2)_1      (state_count == 10)
 Row   3:    ***0***  (state_count == 10)_0  (PO[9:8] == 2)
 Row   4:         1  (state_count == 10)_1  (PO[9:8] == 2)

----------------Focused Condition View--------------------
Line      90 Item    1  (state_count < 9)
Condition totals: 1 of 1 input term covered = 100.00%

       Input Term   Covered  Reason for no coverage   Hint
       ----------- --------  ----------------------  --------------
 (state_count < 9)        Y

    Rows:      Hits  FEC Target           Non-masking condition(s)
 --------- ---------  -------------------  -------------------------
 Row   1:         1  (state_count < 9)_0   -
 Row   2:         1  (state_count < 9)_1   -

----------------Focused Condition View--------------------
Line      101 Item    1  ((PO[9:8] == 3) && (state_count == 10))
Condition totals: 1 of 2 input terms covered = 50.00%

        Input Term   Covered  Reason for no coverage   Hint
        ----------- --------  ----------------------  --------------
     (PO[9:8] == 3)        Y
 (state_count == 10)        N  '_0' not hit           Hit '_0'

    Rows:      Hits  FEC Target           Non-masking condition(s)
 --------- ---------  -------------------  -------------------------
 Row   1:         1  (PO[9:8] == 3)_0      -
```

```
 Row   2:        1  (PO[9:8] == 3)_1      (state_count == 10)
 Row   3:   ***0***  (state_count == 10)_0  (PO[9:8] == 3)
 Row   4:        1  (state_count == 10)_1  (PO[9:8] == 3)

----------------Focused Condition View-------------------
Line      110 Item    1  (tx_valid && (state_count == 12))
Condition totals: 1 of 2 input terms covered = 50.00%

        Input Term   Covered  Reason for no coverage   Hint
       -----------  --------  ----------------------  --------------
         tx_valid        Y
 (state_count == 12)       N  '_0' not hit           Hit '_0'

    Rows:      Hits  FEC Target           Non-masking condition(s)
 ---------  ---------  -------------------  --------------------------
 Row   1:        1  tx_valid_0           -
 Row   2:        1  tx_valid_1           (state_count == 12)
 Row   3:   ***0***  (state_count == 12)_0  tx_valid
 Row   4:        1  (state_count == 12)_1  tx_valid

----------------Focused Condition View-------------------
Line      113 Item    1  ((state_count >= 12) && (final_count <= 7))
Condition totals: 2 of 2 input terms covered = 100.00%

        Input Term   Covered  Reason for no coverage   Hint
       -----------  --------  ----------------------  --------------
 (state_count >= 12)       Y
  (final_count <= 7)       Y

    Rows:      Hits  FEC Target           Non-masking condition(s)
 ---------  ---------  -------------------  --------------------------
 Row   1:        1  (state_count >= 12)_0  -
 Row   2:        1  (state_count >= 12)_1  (final_count <= 7)
 Row   3:        1  (final_count <= 7)_0   (state_count >= 12)
 Row   4:        1  (final_count <= 7)_1   (state_count >= 12)


FSM Coverage:
   Enabled Coverage            Bins     Hits    Misses  Coverage
   ----------------           ----     ----   ------  --------
   FSM States                    5        5        0   100.00%
   FSM Transitions               8        7        1    87.50%

================================FSM Details================================

FSM Coverage for instance /\top#DUT /DUT_2 --

FSM_ID: cs
   Current State Object : cs
   ----------------------
   State Value MapInfo :
   ----------------------
Line         State Name             Value
----        ----------            -----
 135              IDLE                0
 140           CHK_CMD                1
 165         READ_DATA                4
 158          READ_ADD                3
 153             WRITE                2
   Covered States :
   ----------------
              State         Hit_count
              -----        ---------
               IDLE             8012
            CHK_CMD             8000
          READ_DATA            40000
```

```
            READ_ADD            22000
               WRITE            44000
   Covered Transitions :
   ---------------------
Line         Trans_ID        Hit_count        Transition
----         --------        ---------        ----------
 139              0             8000        IDLE -> CHK_CMD
 150              1             2000        CHK_CMD -> READ_DATA
 148              2             2000        CHK_CMD -> READ_ADD
 145              3             4000        CHK_CMD -> WRITE
 167              5             2000        READ_DATA -> IDLE
 160              6             2000        READ_ADD -> IDLE
 155              7             4000        WRITE -> IDLE
   Uncovered Transitions :
   -----------------------
Line         Trans_ID        Transition
----         --------        ----------
 142              4        CHK_CMD -> IDLE


   Summary                  Bins     Hits    Misses  Coverage
   -------                  ----     ----    ------  --------
      FSM States              5        5         0   100.00%
      FSM Transitions         8        7         1    87.50%
Statement Coverage:
   Enabled Coverage           Bins     Hits    Misses  Coverage
   ----------------           ----     ----    ------  --------
   Statements                 67       66         1    98.50%

================================Statement Details================================

Statement Coverage for instance /\top#DUT /DUT_2 --

   Line       Item                 Count     Source
   ----       ----                 -----     ------
 File SPI_Slave.sv
   1                                    module SPI_Slave_wrapper (MOSI, SS_n, clk, rst_n, tx_data, tx_valid, MISO,
rx_data, rx_valid);
   2                                        parameter IDLE = 0;
   3                                        parameter CHK_CMD = 1;
   4                                        parameter WRITE = 2;
   5                                        parameter READ_ADD = 3;
   6                                         parameter READ_DATA = 4;
   7
   8                                        input MOSI, SS_n, clk, rst_n, tx_valid;
   9                                        input [7:0] tx_data;
   10                                       output MISO;
   11                                       output reg rx_valid;
   12                                       output  [9:0] rx_data;
   13
   14                                       reg [2:0] cs, ns;//current state and next state
   15                                       reg [9:0] PO;
   16                                       reg [7:0] temp;
   17                                       reg SO, flag_rd ;
   18                                       integer state_count = 0, final_count = 0;
   19                                       reg Act_input_output;
   20
   21                                       assign MISO = SO; // output of reading
   22                                       assign rx_data   = PO ;
   23                                     // state Memory
   24          1              122012                always @(posedge clk ) begin //bug : reset must be syncrouns not
Async
   25                                                   if (!rst_n)begin
   26          1                 12                            cs <= IDLE;
   27          1                 12                       flag_rd<=0;
   28          1                 12                       final_count <=32'hFFFF_FFFF;
```

```
   29        1              12              state_count <=32'hFFFF_FFFF;
   30        1              12              temp <= 0 ;
   31                                     end
   32                                     else
   33        1          122000                      cs <= ns;
   34                             end
   35        1           24001              always @ (cs)begin
   36                                     if (cs == IDLE)begin
   37        1            8001                          rx_valid = 0 ;
   38        1            8001                      PO  = 0 ;
   39        1            8001                      state_count = 0 ;
   40        1            8001                      final_count = 0 ;
   41        1            8001                      SO = 0 ;
   42        1            8001                      Act_input_output = 0;
   43                                     end
   44                             end
   45
   46        1          122012              always @(posedge clk) begin//* bug
   47
   48                                     case (cs)
   49                                         IDLE : begin
   50
   51        1            8011                          rx_valid = 0 ;
   52        1            8011                    PO  = 0 ;
   53        1            8011                    state_count = 0 ;
   54        1            8011                    final_count = 0 ;
   55        1            8011                    SO = 0 ;
   56        1            8011                    Act_input_output = 0;
   57                                         end
   58                                     WRITE: begin //done
   59
   60                                                 if (state_count < 10 )begin //0 ,
   61        1           40000                                     PO = {PO[8:0] , MOSI} ;
   62        1           40000                                     state_count =
state_count + 1 ;
   63                                                                 if (PO[9] ==1'b0 && state_count
==10)begin
   64        1            4000                                       rx_valid = 1 ;
   65                                                    end
   66                                                    else
   67        1           36000                                     rx_valid = 0 ;
   68                                                 end
   69                                                 else
   70        1            4000                                     rx_valid = 0 ;
   71
   72                                             end
   73                                     READ_ADD: begin // done
   74
   75                                         if (state_count<10 )begin
   76        1           20000                         PO = {PO[8:0] , MOSI} ;
   77        1           20000                         state_count = state_count + 1 ;
   78        1           20000                         rx_valid = 0 ;
   79                                         end
   80                                         if (PO[9:8]==2'b10 && state_count==10)begin
   81        1            4000                         rx_valid = 1 ;
   82        1            4000                         flag_rd = 1;
   83                                         end
   84                                         else
   85        1           18000                                     rx_valid = 0 ;
   86                                                 end
   87                                     READ_DATA: begin // done
   88
   89                                         if (Act_input_output == 0)begin
   90                                                 if (state_count<9 )begin
   91        1           18000                           PO = {PO[8:0] , MOSI} ;
   92        1           18000                           state_count = state_count + 1 ;
```

```
   93          1              18000                                                  rx_valid = 0 ;
   94                                                                    end
   95                                                                    else begin
   96          1              2000                                                   PO = {PO[8:0] , MOSI} ;
   97          1              2000                                                     state_count = state_count + 1 ;
   98          1              2000                                                     rx_valid = 0 ;
   99                                                                    end
   100
   101                                                                   if (PO[9:8]==2'b11 && state_count== 10 )begin
   102         1              2000                                                     rx_valid = 1 ;
   103         1              2000                                                     Act_input_output = 1;
   104         1              2000                                                     flag_rd = 0;
   105                                                                   end
   106                                                                 end
   107                                                                 else begin
   108         1              20000                                                  state_count = state_count + 1 ;
   109         1              20000                                                  rx_valid = 0 ;
   110                                                                       if (tx_valid && state_count == 12 )begin
   111         1              2000                                                       temp = tx_data ;
   112                                                                       end
   113                                                                       if (state_count >= 12 && final_count <=
7)begin
   114         1              16000                                                        SO = temp [7 -
final_count ];
   115         1              16000                                                        rx_valid =0 ;
   116         1              16000                                                        final_count =
final_count + 1 ;
   117                                                                         end
   118                                                                       end
   119                                                                  end
   120                                                    default: begin
   121         1              8001                                       rx_valid = 0 ;
   122         1              8001                                    PO  = 0 ;
   123         1              8001                                    state_count = 0 ;
   124         1              8001                                    final_count = 0 ;
   125         1              8001                                    SO = 0 ;
   126         1              8001                                    Act_input_output = 0;
   127
   128                                                       end
   129                                                    endcase
   130                                 end
   131
   132         1              92914              always @(*) begin
   133
   134                                            case (cs)
   135                                              IDLE:
   136                                                       if (SS_n)
   137         1              8006                                ns = IDLE;
   138                                                       else
   139         1              8000                                ns = CHK_CMD;
   140                                              CHK_CMD:
   141                                                       if (SS_n)
   142         1              ***0***                             ns = IDLE;
   143                                                       else begin//SS_n = 0
   144                                                         if (MOSI==0) //MOSI = 0
   145         1              5954                                        ns = WRITE;
   146                                                         else  begin //MOSI = 1
   147                                                                 if (!flag_rd) //flag_rd = 0
   148         1              4013                                          ns = READ_ADD;
   149                                                                 else  //flag_rd = 1
   150         1              2000                                          ns = READ_DATA;
   151                                                         end
   152                                                       end
   153                                              WRITE:
   154                                                       if (SS_n)
   155         1              4000                                ns = IDLE;
```

```
156                                                 else
157         1           21982                               ns = WRITE;
158                                         READ_ADD:
159                                                 if (SS_n)
160         1           2000                                ns = IDLE;
161                                                 else begin
162         1           13981                               ns = READ_ADD;
163                                                   // flag_rd = 1;
164                                                 end
165                                         READ_DATA:
166                                                 if (SS_n)
167         1           2000                                ns = IDLE;
168                                                 else begin
169         1           20977                               ns = READ_DATA;
170                                                   // flag_rd = 0;
171                                                 end
172
173         1           1                   default: ns = IDLE;
```

Toggle Coverage:

Enabled Coverage	Bins	Hits	Misses	Coverage
Toggles	232	232	0	100.00%

==========Toggle Details==========

Toggle Coverage for instance /\top#DUT /DUT_2 --

Node	1H->0L	0L->1H	"Coverage"
Act_input_output	1	1	100.00
MISO	1	1	100.00
MOSI	1	1	100.00
PO[9-0]	1	1	100.00
SO	1	1	100.00
SS_n	1	1	100.00
clk	1	1	100.00
cs[2-0]	1	1	100.00
final_count[31-0]	1	1	100.00
flag_rd	1	1	100.00
ns[2-0]	1	1	100.00
rst_n	1	1	100.00
rx_data[0-9]	1	1	100.00
rx_valid	1	1	100.00
state_count[31-0]	1	1	100.00
temp[7-0]	1	1	100.00
tx_data[0-7]	1	1	100.00
tx_valid	1	1	100.00

Total Node Count = 116
Toggled Node Count = 116
Untoggled Node Count = 0

Toggle Coverage = 100.00% (232 of 232 bins)

==========

=== Instance: /\top#DUT
=== Design Unit: work.SPI_Wrapper

==========

Toggle Coverage:

Enabled Coverage	Bins	Hits	Misses	Coverage
Toggles	68	68	0	100.00%

==========Toggle Details==========

	Toggle Coverage for instance /\top#DUT -- Node 1H->0L 0L->1H "Coverage" --- MISO 1 1 100.00 MOSI 1 1 100.00 SS_n 1 1 100.00 clk 1 1 100.00 rst_n 1 1 100.00 rx_data_wrapper[9-0] 1 1 100.00 rx_valid_wrapper 1 1 100.00 tx_data_wrapper[7-0] 1 1 100.00 tx_ref[7-0] 1 1 100.00 tx_valid_ref 1 1 100.00 tx_valid_wrapper 1 1 100.00 Total Node Count = 34 Toggled Node Count = 34 Untoggled Node Count = 0 **Toggle Coverage = 100.00% (68 of 68 bins)** **Total Coverage By Instance (filtered view): 92.55%**
Assertions	I saw that I didn't need to use assertion because I got what I want in checking with scoreboard……

Function coverage report For RAM and wrapper

Coverage Report by instance with details

==========

=== Instance: /RAM_coverage_pkg
=== Design Unit: work.RAM_coverage_pkg
==========

Covergroup Coverage:
Covergroups 1 na na 100.00%
Coverpoints/Crosses 12 na na na
Covergroup Bins 655 655 0 100.00%

Covergroup Metric Goal Bins Status

TYPE /RAM_coverage_pkg/RAM_coverage/cvr_gp 100.00% 100 - Covered
covered/total bins: 655 655 -
missing/total bins: 0 655 -
% Hit: 100.00% 100 -
Coverpoint reset 100.00% 100 - Covered

```
    covered/total bins:                    2         2         -
    missing/total bins:                    0         2         -
    % Hit:                           100.00%       100         -
  Coverpoint data_valid                100.00%       100         -    Covered
    covered/total bins:                    9         9         -
    missing/total bins:                    0         9         -
    % Hit:                           100.00%       100         -
  Coverpoint data_written              100.00%       100         -    Covered
    covered/total bins:                   64        64         -
    missing/total bins:                    0        64         -
    % Hit:                           100.00%       100         -
  Coverpoint data_read                 100.00%       100         -    Covered
    covered/total bins:                   64        64         -
    missing/total bins:                    0        64         -
    % Hit:                           100.00%       100         -
  Coverpoint address_written           100.00%       100         -    Covered
    covered/total bins:                   64        64         -
    missing/total bins:                    0        64         -
    % Hit:                           100.00%       100         -
  Coverpoint address_read              100.00%       100         -    Covered
    covered/total bins:                   64        64         -
    missing/total bins:                    0        64         -
    % Hit:                           100.00%       100         -
  Coverpoint receive_valid             100.00%       100         -    Covered
    covered/total bins:                    2         2         -
    missing/total bins:                    0         2         -
    % Hit:                           100.00%       100         -
  Coverpoint send_valid                100.00%       100         -    Covered
    covered/total bins:                    2         2         -
    missing/total bins:                    0         2         -
    % Hit:                           100.00%       100         -
  Cross Writing_address                100.00%       100         -    Covered
    covered/total bins:                  128       128         -
    missing/total bins:                    0       128         -
    % Hit:                           100.00%       100         -
  Cross Writing_data                   100.00%       100         -    Covered
    covered/total bins:                  128       128         -
    missing/total bins:                    0       128         -
    % Hit:                           100.00%       100         -
  Cross reading_address                100.00%       100         -    Covered
    covered/total bins:                   64        64         -
    missing/total bins:                    0        64         -
    % Hit:                           100.00%       100         -
  Cross reading_data                   100.00%       100         -    Covered
    covered/total bins:                   64        64         -
    missing/total bins:                    0        64         -
    % Hit:                           100.00%       100         -
Covergroup instance \/RAM_coverage_pkg::RAM_coverage::cvr_gp
                                     100.00%       100         -    Covered
  covered/total bins:                    655       655         -
  missing/total bins:                      0       655         -
  % Hit:                           100.00%       100         -
  Coverpoint reset                   100.00%       100         -    Covered
    covered/total bins:                    2         2         -
    missing/total bins:                    0         2         -
    % Hit:                           100.00%       100         -
    bin reset_asserted                    12         1         -    Covered
    bin reset_disable                 122000         1         -    Covered
  Coverpoint data_valid                100.00%       100         -    Covered
    covered/total bins:                    9         9         -
    missing/total bins:                    0         9         -
    % Hit:                           100.00%       100         -
    bin writing_complete                6000         1         -    Covered
    bin writing                        94012         1         -    Covered
    bin reading                         2000         1         -    Covered
    bin change_wr_rd                    2000         1         -    Covered
```

bin change_rd_wr	2000	1	-	Covered
bin default_values[0]	94012	1	-	Covered
bin default_values[1]	6000	1	-	Covered
bin default_values[2]	2000	1	-	Covered
bin default_values[3]	20000	1	-	Covered
Coverpoint data_written	100.00%	100	-	Covered
covered/total bins:	64	64	-	
missing/total bins:	0	64	-	
% Hit:	100.00%	100	-	
bin auto[0:3]	116107	1	-	Covered
bin auto[4:7]	94	1	-	Covered
bin auto[8:11]	95	1	-	Covered
bin auto[12:15]	95	1	-	Covered
bin auto[16:19]	95	1	-	Covered
bin auto[20:23]	95	1	-	Covered
bin auto[24:27]	93	1	-	Covered
bin auto[28:31]	93	1	-	Covered
bin auto[32:35]	93	1	-	Covered
bin auto[36:39]	94	1	-	Covered
bin auto[40:43]	95	1	-	Covered
bin auto[44:47]	96	1	-	Covered
bin auto[48:51]	95	1	-	Covered
bin auto[52:55]	94	1	-	Covered
bin auto[56:59]	93	1	-	Covered
bin auto[60:63]	95	1	-	Covered
bin auto[64:67]	92	1	-	Covered
bin auto[68:71]	94	1	-	Covered
bin auto[72:75]	92	1	-	Covered
bin auto[76:79]	92	1	-	Covered
bin auto[80:83]	95	1	-	Covered
bin auto[84:87]	91	1	-	Covered
bin auto[88:91]	96	1	-	Covered
bin auto[92:95]	92	1	-	Covered
bin auto[96:99]	93	1	-	Covered
bin auto[100:103]	95	1	-	Covered
bin auto[104:107]	91	1	-	Covered
bin auto[108:111]	94	1	-	Covered
bin auto[112:115]	93	1	-	Covered
bin auto[116:119]	94	1	-	Covered
bin auto[120:123]	90	1	-	Covered
bin auto[124:127]	95	1	-	Covered
bin auto[128:131]	91	1	-	Covered
bin auto[132:135]	94	1	-	Covered
bin auto[136:139]	93	1	-	Covered
bin auto[140:143]	91	1	-	Covered
bin auto[144:147]	91	1	-	Covered
bin auto[148:151]	95	1	-	Covered
bin auto[152:155]	94	1	-	Covered
bin auto[156:159]	95	1	-	Covered
bin auto[160:163]	93	1	-	Covered
bin auto[164:167]	92	1	-	Covered
bin auto[168:171]	95	1	-	Covered
bin auto[172:175]	95	1	-	Covered
bin auto[176:179]	95	1	-	Covered
bin auto[180:183]	93	1	-	Covered
bin auto[184:187]	93	1	-	Covered
bin auto[188:191]	92	1	-	Covered
bin auto[192:195]	93	1	-	Covered
bin auto[196:199]	93	1	-	Covered
bin auto[200:203]	94	1	-	Covered
bin auto[204:207]	95	1	-	Covered
bin auto[208:211]	94	1	-	Covered
bin auto[212:215]	92	1	-	Covered
bin auto[216:219]	94	1	-	Covered
bin auto[220:223]	95	1	-	Covered
bin auto[224:227]	96	1	-	Covered

bin auto[228:231]	96	1	-	Covered
bin auto[232:235]	93	1	-	Covered
bin auto[236:239]	95	1	-	Covered
bin auto[240:243]	96	1	-	Covered
bin auto[244:247]	94	1	-	Covered
bin auto[248:251]	95	1	-	Covered
bin auto[252:255]	94	1	-	Covered
Coverpoint data_read	100.00%	100	-	Covered
covered/total bins:	64	64	-	
missing/total bins:	0	64	-	
% Hit:	100.00%	100	-	
bin auto[0:3]	27817	1	-	Covered
bin auto[4:7]	1361	1	-	Covered
bin auto[8:11]	1475	1	-	Covered
bin auto[12:15]	1536	1	-	Covered
bin auto[16:19]	1536	1	-	Covered
bin auto[20:23]	1536	1	-	Covered
bin auto[24:27]	1536	1	-	Covered
bin auto[28:31]	1440	1	-	Covered
bin auto[32:35]	1475	1	-	Covered
bin auto[36:39]	1501	1	-	Covered
bin auto[40:43]	1536	1	-	Covered
bin auto[44:47]	1536	1	-	Covered
bin auto[48:51]	1536	1	-	Covered
bin auto[52:55]	1536	1	-	Covered
bin auto[56:59]	1485	1	-	Covered
bin auto[60:63]	1389	1	-	Covered
bin auto[64:67]	1274	1	-	Covered
bin auto[68:71]	1501	1	-	Covered
bin auto[72:75]	1590	1	-	Covered
bin auto[76:79]	1335	1	-	Covered
bin auto[80:83]	1536	1	-	Covered
bin auto[84:87]	1536	1	-	Covered
bin auto[88:91]	1536	1	-	Covered
bin auto[92:95]	1536	1	-	Covered
bin auto[96:99]	1256	1	-	Covered
bin auto[100:103]	1536	1	-	Covered
bin auto[104:107]	1536	1	-	Covered
bin auto[108:111]	1501	1	-	Covered
bin auto[112:115]	1536	1	-	Covered
bin auto[116:119]	1424	1	-	Covered
bin auto[120:123]	1493	1	-	Covered
bin auto[124:127]	1536	1	-	Covered
bin auto[128:131]	1475	1	-	Covered
bin auto[132:135]	1475	1	-	Covered
bin auto[136:139]	1676	1	-	Covered
bin auto[140:143]	1344	1	-	Covered
bin auto[144:147]	1440	1	-	Covered
bin auto[148:151]	1536	1	-	Covered
bin auto[152:155]	1354	1	-	Covered
bin auto[156:159]	1536	1	-	Covered
bin auto[160:163]	1475	1	-	Covered
bin auto[164:167]	1641	1	-	Covered
bin auto[168:171]	1536	1	-	Covered
bin auto[172:175]	1501	1	-	Covered
bin auto[176:179]	1536	1	-	Covered
bin auto[180:183]	1440	1	-	Covered
bin auto[184:187]	1501	1	-	Covered
bin auto[188:191]	1536	1	-	Covered
bin auto[192:195]	1616	1	-	Covered
bin auto[196:199]	1536	1	-	Covered
bin auto[200:203]	1641	1	-	Covered
bin auto[204:207]	1451	1	-	Covered
bin auto[208:211]	1536	1	-	Covered
bin auto[212:215]	1353	1	-	Covered
bin auto[216:219]	1396	1	-	Covered

bin auto[220:223]	1501	1	-	Covered
bin auto[224:227]	1536	1	-	Covered
bin auto[228:231]	1536	1	-	Covered
bin auto[232:235]	1536	1	-	Covered
bin auto[236:239]	1440	1	-	Covered
bin auto[240:243]	1536	1	-	Covered
bin auto[244:247]	1536	1	-	Covered
bin auto[248:251]	1501	1	-	Covered
bin auto[252:255]	1466	1	-	Covered
Coverpoint address_written	100.00%	100	-	Covered
covered/total bins:	64	64	-	
missing/total bins:	0	64	-	
% Hit:	100.00%	100	-	
bin auto[0:3]	75986	1	-	Covered
bin auto[4:7]	7969	1	-	Covered
bin auto[8:11]	3969	1	-	Covered
bin auto[12:15]	3969	1	-	Covered
bin auto[16:19]	1980	1	-	Covered
bin auto[20:23]	1957	1	-	Covered
bin auto[24:27]	1959	1	-	Covered
bin auto[28:31]	1979	1	-	Covered
bin auto[32:35]	976	1	-	Covered
bin auto[36:39]	972	1	-	Covered
bin auto[40:43]	962	1	-	Covered
bin auto[44:47]	964	1	-	Covered
bin auto[48:51]	963	1	-	Covered
bin auto[52:55]	964	1	-	Covered
bin auto[56:59]	969	1	-	Covered
bin auto[60:63]	978	1	-	Covered
bin auto[64:67]	473	1	-	Covered
bin auto[68:71]	471	1	-	Covered
bin auto[72:75]	468	1	-	Covered
bin auto[76:79]	472	1	-	Covered
bin auto[80:83]	464	1	-	Covered
bin auto[84:87]	468	1	-	Covered
bin auto[88:91]	468	1	-	Covered
bin auto[92:95]	464	1	-	Covered
bin auto[96:99]	463	1	-	Covered
bin auto[100:103]	468	1	-	Covered
bin auto[104:107]	469	1	-	Covered
bin auto[108:111]	465	1	-	Covered
bin auto[112:115]	468	1	-	Covered
bin auto[116:119]	469	1	-	Covered
bin auto[120:123]	474	1	-	Covered
bin auto[124:127]	473	1	-	Covered
bin auto[128:131]	220	1	-	Covered
bin auto[132:135]	222	1	-	Covered
bin auto[136:139]	221	1	-	Covered
bin auto[140:143]	218	1	-	Covered
bin auto[144:147]	219	1	-	Covered
bin auto[148:151]	220	1	-	Covered
bin auto[152:155]	221	1	-	Covered
bin auto[156:159]	219	1	-	Covered
bin auto[160:163]	217	1	-	Covered
bin auto[164:167]	216	1	-	Covered
bin auto[168:171]	218	1	-	Covered
bin auto[172:175]	218	1	-	Covered
bin auto[176:179]	220	1	-	Covered
bin auto[180:183]	217	1	-	Covered
bin auto[184:187]	217	1	-	Covered
bin auto[188:191]	215	1	-	Covered
bin auto[192:195]	216	1	-	Covered
bin auto[196:199]	216	1	-	Covered
bin auto[200:203]	218	1	-	Covered
bin auto[204:207]	219	1	-	Covered
bin auto[208:211]	215	1	-	Covered

bin auto[212:215]	222	1	-	Covered
bin auto[216:219]	219	1	-	Covered
bin auto[220:223]	216	1	-	Covered
bin auto[224:227]	216	1	-	Covered
bin auto[228:231]	221	1	-	Covered
bin auto[232:235]	217	1	-	Covered
bin auto[236:239]	221	1	-	Covered
bin auto[240:243]	222	1	-	Covered
bin auto[244:247]	220	1	-	Covered
bin auto[248:251]	222	1	-	Covered
bin auto[252:255]	221	1	-	Covered
Coverpoint address_read	100.00%	100	-	Covered
covered/total bins:	64	64	-	
missing/total bins:	0	64	-	
% Hit:	100.00%	100	-	
bin auto[0:3]	120043	1	-	Covered
bin auto[4:7]	32	1	-	Covered
bin auto[8:11]	32	1	-	Covered
bin auto[12:15]	31	1	-	Covered
bin auto[16:19]	32	1	-	Covered
bin auto[20:23]	32	1	-	Covered
bin auto[24:27]	32	1	-	Covered
bin auto[28:31]	32	1	-	Covered
bin auto[32:35]	32	1	-	Covered
bin auto[36:39]	31	1	-	Covered
bin auto[40:43]	32	1	-	Covered
bin auto[44:47]	31	1	-	Covered
bin auto[48:51]	32	1	-	Covered
bin auto[52:55]	29	1	-	Covered
bin auto[56:59]	32	1	-	Covered
bin auto[60:63]	31	1	-	Covered
bin auto[64:67]	32	1	-	Covered
bin auto[68:71]	30	1	-	Covered
bin auto[72:75]	30	1	-	Covered
bin auto[76:79]	32	1	-	Covered
bin auto[80:83]	31	1	-	Covered
bin auto[84:87]	32	1	-	Covered
bin auto[88:91]	32	1	-	Covered
bin auto[92:95]	32	1	-	Covered
bin auto[96:99]	32	1	-	Covered
bin auto[100:103]	31	1	-	Covered
bin auto[104:107]	32	1	-	Covered
bin auto[108:111]	30	1	-	Covered
bin auto[112:115]	31	1	-	Covered
bin auto[116:119]	31	1	-	Covered
bin auto[120:123]	32	1	-	Covered
bin auto[124:127]	32	1	-	Covered
bin auto[128:131]	31	1	-	Covered
bin auto[132:135]	32	1	-	Covered
bin auto[136:139]	31	1	-	Covered
bin auto[140:143]	31	1	-	Covered
bin auto[144:147]	31	1	-	Covered
bin auto[148:151]	30	1	-	Covered
bin auto[152:155]	31	1	-	Covered
bin auto[156:159]	31	1	-	Covered
bin auto[160:163]	32	1	-	Covered
bin auto[164:167]	32	1	-	Covered
bin auto[168:171]	30	1	-	Covered
bin auto[172:175]	30	1	-	Covered
bin auto[176:179]	32	1	-	Covered
bin auto[180:183]	32	1	-	Covered
bin auto[184:187]	30	1	-	Covered
bin auto[188:191]	31	1	-	Covered
bin auto[192:195]	31	1	-	Covered
bin auto[196:199]	32	1	-	Covered
bin auto[200:203]	32	1	-	Covered

```
    bin auto[204:207]                    31        1        -    Covered
    bin auto[208:211]                    28        1        -    Covered
    bin auto[212:215]                    31        1        -    Covered
    bin auto[216:219]                    32        1        -    Covered
    bin auto[220:223]                    30        1        -    Covered
    bin auto[224:227]                    31        1        -    Covered
    bin auto[228:231]                    31        1        -    Covered
    bin auto[232:235]                    31        1        -    Covered
    bin auto[236:239]                    32        1        -    Covered
    bin auto[240:243]                    30        1        -    Covered
    bin auto[244:247]                    32        1        -    Covered
    bin auto[248:251]                    32        1        -    Covered
    bin auto[252:255]                    31        1        -    Covered
  Coverpoint receive_valid               100.00%   100      -    Covered
    covered/total bins:                  2         2        -
    missing/total bins:                  0         2        -
    % Hit:                               100.00%   100      -
    bin receive_asserted                 8000      1        -    Covered
    bin receive_disable                  114012    1        -    Covered
  Coverpoint send_valid                  100.00%   100      -    Covered
    covered/total bins:                  2         2        -
    missing/total bins:                  0         2        -
    % Hit:                               100.00%   100      -
    bin send_asserted                    2000      1        -    Covered
    bin send_disable                     120012    1        -    Covered
  Cross Writing_address                  100.00%   100      -    Covered
    covered/total bins:                  128       128      -
    missing/total bins:                  0         128      -
    % Hit:                               100.00%   100      -
    Auto, Default and User Defined Bins:
      bin <auto[252:255],receive_disable>    189     1        -    Covered
      bin <auto[248:251],receive_disable>    190     1        -    Covered
      bin <auto[244:247],receive_disable>    188     1        -    Covered
      bin <auto[240:243],receive_disable>    192     1        -    Covered
      bin <auto[236:239],receive_disable>    189     1        -    Covered
      bin <auto[232:235],receive_disable>    186     1        -    Covered
      bin <auto[228:231],receive_disable>    189     1        -    Covered
      bin <auto[224:227],receive_disable>    186     1        -    Covered
      bin <auto[220:223],receive_disable>    185     1        -    Covered
      bin <auto[216:219],receive_disable>    188     1        -    Covered
      bin <auto[212:215],receive_disable>    190     1        -    Covered
      bin <auto[208:211],receive_disable>    185     1        -    Covered
      bin <auto[204:207],receive_disable>    189     1        -    Covered
      bin <auto[200:203],receive_disable>    186     1        -    Covered
      bin <auto[196:199],receive_disable>    184     1        -    Covered
      bin <auto[192:195],receive_disable>    185     1        -    Covered
      bin <auto[188:191],receive_disable>    185     1        -    Covered
      bin <auto[184:187],receive_disable>    187     1        -    Covered
      bin <auto[180:183],receive_disable>    185     1        -    Covered
      bin <auto[176:179],receive_disable>    188     1        -    Covered
      bin <auto[172:175],receive_disable>    188     1        -    Covered
      bin <auto[168:171],receive_disable>    186     1        -    Covered
      bin <auto[164:167],receive_disable>    184     1        -    Covered
      bin <auto[160:163],receive_disable>    186     1        -    Covered
      bin <auto[156:159],receive_disable>    188     1        -    Covered
      bin <auto[152:155],receive_disable>    189     1        -    Covered
      bin <auto[148:151],receive_disable>    191     1        -    Covered
      bin <auto[144:147],receive_disable>    187     1        -    Covered
      bin <auto[140:143],receive_disable>    186     1        -    Covered
      bin <auto[136:139],receive_disable>    190     1        -    Covered
      bin <auto[132:135],receive_disable>    190     1        -    Covered
      bin <auto[128:131],receive_disable>    189     1        -    Covered
      bin <auto[124:127],receive_disable>    443     1        -    Covered
      bin <auto[120:123],receive_disable>    442     1        -    Covered
      bin <auto[116:119],receive_disable>    438     1        -    Covered
      bin <auto[112:115],receive_disable>    437     1        -    Covered
```

bin <auto[108:111],receive_disable>	435	1	-	Covered
bin <auto[104:107],receive_disable>	437	1	-	Covered
bin <auto[100:103],receive_disable>	437	1	-	Covered
bin <auto[96:99],receive_disable>	432	1	-	Covered
bin <auto[92:95],receive_disable>	432	1	-	Covered
bin <auto[88:91],receive_disable>	437	1	-	Covered
bin <auto[84:87],receive_disable>	436	1	-	Covered
bin <auto[80:83],receive_disable>	433	1	-	Covered
bin <auto[76:79],receive_disable>	440	1	-	Covered
bin <auto[72:75],receive_disable>	439	1	-	Covered
bin <auto[68:71],receive_disable>	439	1	-	Covered
bin <auto[64:67],receive_disable>	442	1	-	Covered
bin <auto[60:63],receive_disable>	947	1	-	Covered
bin <auto[56:59],receive_disable>	937	1	-	Covered
bin <auto[52:55],receive_disable>	934	1	-	Covered
bin <auto[48:51],receive_disable>	931	1	-	Covered
bin <auto[44:47],receive_disable>	932	1	-	Covered
bin <auto[40:43],receive_disable>	932	1	-	Covered
bin <auto[36:39],receive_disable>	940	1	-	Covered
bin <auto[32:35],receive_disable>	944	1	-	Covered
bin <auto[28:31],receive_disable>	1947	1	-	Covered
bin <auto[24:27],receive_disable>	1927	1	-	Covered
bin <auto[20:23],receive_disable>	1926	1	-	Covered
bin <auto[16:19],receive_disable>	1948	1	-	Covered
bin <auto[12:15],receive_disable>	3938	1	-	Covered
bin <auto[8:11],receive_disable>	3937	1	-	Covered
bin <auto[4:7],receive_disable>	7938	1	-	Covered
bin <auto[0:3],receive_disable>	69955	1	-	Covered
bin <auto[252:255],receive_asserted>	32	1	-	Covered
bin <auto[248:251],receive_asserted>	32	1	-	Covered
bin <auto[244:247],receive_asserted>	32	1	-	Covered
bin <auto[240:243],receive_asserted>	30	1	-	Covered
bin <auto[236:239],receive_asserted>	32	1	-	Covered
bin <auto[232:235],receive_asserted>	31	1	-	Covered
bin <auto[228:231],receive_asserted>	32	1	-	Covered
bin <auto[224:227],receive_asserted>	30	1	-	Covered
bin <auto[220:223],receive_asserted>	31	1	-	Covered
bin <auto[216:219],receive_asserted>	31	1	-	Covered
bin <auto[212:215],receive_asserted>	32	1	-	Covered
bin <auto[208:211],receive_asserted>	30	1	-	Covered
bin <auto[204:207],receive_asserted>	30	1	-	Covered
bin <auto[200:203],receive_asserted>	32	1	-	Covered
bin <auto[196:199],receive_asserted>	32	1	-	Covered
bin <auto[192:195],receive_asserted>	31	1	-	Covered
bin <auto[188:191],receive_asserted>	30	1	-	Covered
bin <auto[184:187],receive_asserted>	30	1	-	Covered
bin <auto[180:183],receive_asserted>	32	1	-	Covered
bin <auto[176:179],receive_asserted>	32	1	-	Covered
bin <auto[172:175],receive_asserted>	30	1	-	Covered
bin <auto[168:171],receive_asserted>	32	1	-	Covered
bin <auto[164:167],receive_asserted>	32	1	-	Covered
bin <auto[160:163],receive_asserted>	31	1	-	Covered
bin <auto[156:159],receive_asserted>	31	1	-	Covered
bin <auto[152:155],receive_asserted>	32	1	-	Covered
bin <auto[148:151],receive_asserted>	29	1	-	Covered
bin <auto[144:147],receive_asserted>	32	1	-	Covered
bin <auto[140:143],receive_asserted>	32	1	-	Covered
bin <auto[136:139],receive_asserted>	31	1	-	Covered
bin <auto[132:135],receive_asserted>	32	1	-	Covered
bin <auto[128:131],receive_asserted>	31	1	-	Covered
bin <auto[124:127],receive_asserted>	30	1	-	Covered
bin <auto[120:123],receive_asserted>	32	1	-	Covered
bin <auto[116:119],receive_asserted>	31	1	-	Covered
bin <auto[112:115],receive_asserted>	31	1	-	Covered
bin <auto[108:111],receive_asserted>	30	1	-	Covered
bin <auto[104:107],receive_asserted>	32	1	-	Covered

bin <auto[100:103],receive_asserted>	31	1	-	Covered
bin <auto[96:99],receive_asserted>	31	1	-	Covered
bin <auto[92:95],receive_asserted>	32	1	-	Covered
bin <auto[88:91],receive_asserted>	31	1	-	Covered
bin <auto[84:87],receive_asserted>	32	1	-	Covered
bin <auto[80:83],receive_asserted>	31	1	-	Covered
bin <auto[76:79],receive_asserted>	32	1	-	Covered
bin <auto[72:75],receive_asserted>	29	1	-	Covered
bin <auto[68:71],receive_asserted>	32	1	-	Covered
bin <auto[64:67],receive_asserted>	31	1	-	Covered
bin <auto[60:63],receive_asserted>	31	1	-	Covered
bin <auto[56:59],receive_asserted>	32	1	-	Covered
bin <auto[52:55],receive_asserted>	30	1	-	Covered
bin <auto[48:51],receive_asserted>	32	1	-	Covered
bin <auto[44:47],receive_asserted>	32	1	-	Covered
bin <auto[40:43],receive_asserted>	30	1	-	Covered
bin <auto[36:39],receive_asserted>	32	1	-	Covered
bin <auto[32:35],receive_asserted>	32	1	-	Covered
bin <auto[28:31],receive_asserted>	32	1	-	Covered
bin <auto[24:27],receive_asserted>	32	1	-	Covered
bin <auto[20:23],receive_asserted>	31	1	-	Covered
bin <auto[16:19],receive_asserted>	32	1	-	Covered
bin <auto[12:15],receive_asserted>	31	1	-	Covered
bin <auto[8:11],receive_asserted>	32	1	-	Covered
bin <auto[4:7],receive_asserted>	31	1	-	Covered
bin <auto[0:3],receive_asserted>	6031	1	-	Covered
Cross Writing_data	100.00%	100	-	Covered
covered/total bins:	128	128	-	
missing/total bins:	0	128	-	
% Hit:	100.00%	100	-	
Auto, Default and User Defined Bins:				
bin <auto[252:255],receive_disable>	62	1	-	Covered
bin <auto[248:251],receive_disable>	63	1	-	Covered
bin <auto[244:247],receive_disable>	62	1	-	Covered
bin <auto[240:243],receive_disable>	64	1	-	Covered
bin <auto[236:239],receive_disable>	64	1	-	Covered
bin <auto[232:235],receive_disable>	61	1	-	Covered
bin <auto[228:231],receive_disable>	64	1	-	Covered
bin <auto[224:227],receive_disable>	64	1	-	Covered
bin <auto[220:223],receive_disable>	64	1	-	Covered
bin <auto[216:219],receive_disable>	63	1	-	Covered
bin <auto[212:215],receive_disable>	63	1	-	Covered
bin <auto[208:211],receive_disable>	63	1	-	Covered
bin <auto[204:207],receive_disable>	63	1	-	Covered
bin <auto[200:203],receive_disable>	63	1	-	Covered
bin <auto[196:199],receive_disable>	61	1	-	Covered
bin <auto[192:195],receive_disable>	62	1	-	Covered
bin <auto[188:191],receive_disable>	60	1	-	Covered
bin <auto[184:187],receive_disable>	61	1	-	Covered
bin <auto[180:183],receive_disable>	62	1	-	Covered
bin <auto[176:179],receive_disable>	64	1	-	Covered
bin <auto[172:175],receive_disable>	63	1	-	Covered
bin <auto[168:171],receive_disable>	63	1	-	Covered
bin <auto[164:167],receive_disable>	61	1	-	Covered
bin <auto[160:163],receive_disable>	62	1	-	Covered
bin <auto[156:159],receive_disable>	63	1	-	Covered
bin <auto[152:155],receive_disable>	63	1	-	Covered
bin <auto[148:151],receive_disable>	63	1	-	Covered
bin <auto[144:147],receive_disable>	61	1	-	Covered
bin <auto[140:143],receive_disable>	62	1	-	Covered
bin <auto[136:139],receive_disable>	62	1	-	Covered
bin <auto[132:135],receive_disable>	63	1	-	Covered
bin <auto[128:131],receive_disable>	61	1	-	Covered
bin <auto[124:127],receive_disable>	63	1	-	Covered
bin <auto[120:123],receive_disable>	62	1	-	Covered
bin <auto[116:119],receive_disable>	63	1	-	Covered

bin <auto[112:115],receive_disable>	62	1	-	Covered
bin <auto[108:111],receive_disable>	62	1	-	Covered
bin <auto[104:107],receive_disable>	59	1	-	Covered
bin <auto[100:103],receive_disable>	63	1	-	Covered
bin <auto[96:99],receive_disable>	63	1	-	Covered
bin <auto[92:95],receive_disable>	61	1	-	Covered
bin <auto[88:91],receive_disable>	64	1	-	Covered
bin <auto[84:87],receive_disable>	60	1	-	Covered
bin <auto[80:83],receive_disable>	64	1	-	Covered
bin <auto[76:79],receive_disable>	62	1	-	Covered
bin <auto[72:75],receive_disable>	61	1	-	Covered
bin <auto[68:71],receive_disable>	62	1	-	Covered
bin <auto[64:67],receive_disable>	63	1	-	Covered
bin <auto[60:63],receive_disable>	64	1	-	Covered
bin <auto[56:59],receive_disable>	62	1	-	Covered
bin <auto[52:55],receive_disable>	62	1	-	Covered
bin <auto[48:51],receive_disable>	63	1	-	Covered
bin <auto[44:47],receive_disable>	64	1	-	Covered
bin <auto[40:43],receive_disable>	63	1	-	Covered
bin <auto[36:39],receive_disable>	62	1	-	Covered
bin <auto[32:35],receive_disable>	62	1	-	Covered
bin <auto[28:31],receive_disable>	63	1	-	Covered
bin <auto[24:27],receive_disable>	61	1	-	Covered
bin <auto[20:23],receive_disable>	63	1	-	Covered
bin <auto[16:19],receive_disable>	63	1	-	Covered
bin <auto[12:15],receive_disable>	64	1	-	Covered
bin <auto[8:11],receive_disable>	64	1	-	Covered
bin <auto[4:7],receive_disable>	63	1	-	Covered
bin <auto[0:3],receive_disable>	110075	1	-	Covered
bin <auto[252:255],receive_asserted>	32	1	-	Covered
bin <auto[248:251],receive_asserted>	32	1	-	Covered
bin <auto[244:247],receive_asserted>	32	1	-	Covered
bin <auto[240:243],receive_asserted>	32	1	-	Covered
bin <auto[236:239],receive_asserted>	31	1	-	Covered
bin <auto[232:235],receive_asserted>	32	1	-	Covered
bin <auto[228:231],receive_asserted>	32	1	-	Covered
bin <auto[224:227],receive_asserted>	32	1	-	Covered
bin <auto[220:223],receive_asserted>	31	1	-	Covered
bin <auto[216:219],receive_asserted>	31	1	-	Covered
bin <auto[212:215],receive_asserted>	29	1	-	Covered
bin <auto[208:211],receive_asserted>	31	1	-	Covered
bin <auto[204:207],receive_asserted>	32	1	-	Covered
bin <auto[200:203],receive_asserted>	31	1	-	Covered
bin <auto[196:199],receive_asserted>	32	1	-	Covered
bin <auto[192:195],receive_asserted>	31	1	-	Covered
bin <auto[188:191],receive_asserted>	32	1	-	Covered
bin <auto[184:187],receive_asserted>	32	1	-	Covered
bin <auto[180:183],receive_asserted>	31	1	-	Covered
bin <auto[176:179],receive_asserted>	31	1	-	Covered
bin <auto[172:175],receive_asserted>	32	1	-	Covered
bin <auto[168:171],receive_asserted>	32	1	-	Covered
bin <auto[164:167],receive_asserted>	31	1	-	Covered
bin <auto[160:163],receive_asserted>	31	1	-	Covered
bin <auto[156:159],receive_asserted>	32	1	-	Covered
bin <auto[152:155],receive_asserted>	31	1	-	Covered
bin <auto[148:151],receive_asserted>	32	1	-	Covered
bin <auto[144:147],receive_asserted>	30	1	-	Covered
bin <auto[140:143],receive_asserted>	29	1	-	Covered
bin <auto[136:139],receive_asserted>	31	1	-	Covered
bin <auto[132:135],receive_asserted>	31	1	-	Covered
bin <auto[128:131],receive_asserted>	30	1	-	Covered
bin <auto[124:127],receive_asserted>	32	1	-	Covered
bin <auto[120:123],receive_asserted>	28	1	-	Covered
bin <auto[116:119],receive_asserted>	31	1	-	Covered
bin <auto[112:115],receive_asserted>	31	1	-	Covered
bin <auto[108:111],receive_asserted>	32	1	-	Covered

bin <auto[104:107],receive_asserted>	32	1	-	Covered
bin <auto[100:103],receive_asserted>	32	1	-	Covered
bin <auto[96:99],receive_asserted>	30	1	-	Covered
bin <auto[92:95],receive_asserted>	31	1	-	Covered
bin <auto[88:91],receive_asserted>	32	1	-	Covered
bin <auto[84:87],receive_asserted>	31	1	-	Covered
bin <auto[80:83],receive_asserted>	31	1	-	Covered
bin <auto[76:79],receive_asserted>	30	1	-	Covered
bin <auto[72:75],receive_asserted>	31	1	-	Covered
bin <auto[68:71],receive_asserted>	32	1	-	Covered
bin <auto[64:67],receive_asserted>	29	1	-	Covered
bin <auto[60:63],receive_asserted>	31	1	-	Covered
bin <auto[56:59],receive_asserted>	31	1	-	Covered
bin <auto[52:55],receive_asserted>	32	1	-	Covered
bin <auto[48:51],receive_asserted>	32	1	-	Covered
bin <auto[44:47],receive_asserted>	32	1	-	Covered
bin <auto[40:43],receive_asserted>	32	1	-	Covered
bin <auto[36:39],receive_asserted>	32	1	-	Covered
bin <auto[32:35],receive_asserted>	31	1	-	Covered
bin <auto[28:31],receive_asserted>	30	1	-	Covered
bin <auto[24:27],receive_asserted>	32	1	-	Covered
bin <auto[20:23],receive_asserted>	32	1	-	Covered
bin <auto[16:19],receive_asserted>	32	1	-	Covered
bin <auto[12:15],receive_asserted>	31	1	-	Covered
bin <auto[8:11],receive_asserted>	31	1	-	Covered
bin <auto[4:7],receive_asserted>	31	1	-	Covered
bin <auto[0:3],receive_asserted>	6032	1	-	Covered
Cross reading_address	100.00%	100	-	Covered
covered/total bins:	64	64	-	
missing/total bins:	0	64	-	
% Hit:	100.00%	100	-	
Auto, Default and User Defined Bins:				
bin <auto[252:255],receive_asserted>	31	1	-	Covered
bin <auto[124:127],receive_asserted>	32	1	-	Covered
bin <auto[188:191],receive_asserted>	31	1	-	Covered
bin <auto[60:63],receive_asserted>	31	1	-	Covered
bin <auto[220:223],receive_asserted>	30	1	-	Covered
bin <auto[92:95],receive_asserted>	32	1	-	Covered
bin <auto[156:159],receive_asserted>	31	1	-	Covered
bin <auto[28:31],receive_asserted>	32	1	-	Covered
bin <auto[236:239],receive_asserted>	32	1	-	Covered
bin <auto[108:111],receive_asserted>	30	1	-	Covered
bin <auto[172:175],receive_asserted>	30	1	-	Covered
bin <auto[44:47],receive_asserted>	31	1	-	Covered
bin <auto[204:207],receive_asserted>	31	1	-	Covered
bin <auto[76:79],receive_asserted>	32	1	-	Covered
bin <auto[140:143],receive_asserted>	31	1	-	Covered
bin <auto[12:15],receive_asserted>	31	1	-	Covered
bin <auto[244:247],receive_asserted>	32	1	-	Covered
bin <auto[116:119],receive_asserted>	31	1	-	Covered
bin <auto[180:183],receive_asserted>	32	1	-	Covered
bin <auto[52:55],receive_asserted>	29	1	-	Covered
bin <auto[212:215],receive_asserted>	31	1	-	Covered
bin <auto[84:87],receive_asserted>	32	1	-	Covered
bin <auto[148:151],receive_asserted>	30	1	-	Covered
bin <auto[20:23],receive_asserted>	32	1	-	Covered
bin <auto[228:231],receive_asserted>	31	1	-	Covered
bin <auto[100:103],receive_asserted>	31	1	-	Covered
bin <auto[164:167],receive_asserted>	32	1	-	Covered
bin <auto[36:39],receive_asserted>	31	1	-	Covered
bin <auto[196:199],receive_asserted>	32	1	-	Covered
bin <auto[68:71],receive_asserted>	30	1	-	Covered
bin <auto[132:135],receive_asserted>	32	1	-	Covered
bin <auto[4:7],receive_asserted>	32	1	-	Covered
bin <auto[248:251],receive_asserted>	32	1	-	Covered
bin <auto[120:123],receive_asserted>	32	1	-	Covered

```
        bin <auto[184:187],receive_asserted>          30       1       -   Covered
        bin <auto[56:59],receive_asserted>          32       1       -   Covered
        bin <auto[216:219],receive_asserted>          32       1       -   Covered
        bin <auto[88:91],receive_asserted>          32       1       -   Covered
        bin <auto[152:155],receive_asserted>          31       1       -   Covered
        bin <auto[24:27],receive_asserted>          32       1       -   Covered
        bin <auto[232:235],receive_asserted>          31       1       -   Covered
        bin <auto[104:107],receive_asserted>          32       1       -   Covered
        bin <auto[168:171],receive_asserted>          30       1       -   Covered
        bin <auto[40:43],receive_asserted>          32       1       -   Covered
        bin <auto[200:203],receive_asserted>          32       1       -   Covered
        bin <auto[72:75],receive_asserted>          30       1       -   Covered
        bin <auto[136:139],receive_asserted>          31       1       -   Covered
        bin <auto[8:11],receive_asserted>          32       1       -   Covered
        bin <auto[240:243],receive_asserted>          30       1       -   Covered
        bin <auto[112:115],receive_asserted>          31       1       -   Covered
        bin <auto[176:179],receive_asserted>          32       1       -   Covered
        bin <auto[48:51],receive_asserted>          32       1       -   Covered
        bin <auto[208:211],receive_asserted>          28       1       -   Covered
        bin <auto[80:83],receive_asserted>          31       1       -   Covered
        bin <auto[144:147],receive_asserted>          31       1       -   Covered
        bin <auto[16:19],receive_asserted>          32       1       -   Covered
        bin <auto[224:227],receive_asserted>          31       1       -   Covered
        bin <auto[96:99],receive_asserted>          32       1       -   Covered
        bin <auto[160:163],receive_asserted>          32       1       -   Covered
        bin <auto[32:35],receive_asserted>          32       1       -   Covered
        bin <auto[192:195],receive_asserted>          31       1       -   Covered
        bin <auto[64:67],receive_asserted>          32       1       -   Covered
        bin <auto[128:131],receive_asserted>          31       1       -   Covered
        bin <auto[0:3],receive_asserted>          6031       1       -   Covered
      Illegal and Ignore Bins:
        ignore_bin ignore_bin1                 114012                 -   Occurred
    Cross reading_data                         100.00%      100       -   Covered
      covered/total bins:                          64       64       -
      missing/total bins:                          0        64       -
      % Hit:                                 100.00%      100       -
      Auto, Default and User Defined Bins:
        bin <auto[252:255],receive_asserted>          92       1       -   Covered
        bin <auto[124:127],receive_asserted>          96       1       -   Covered
        bin <auto[188:191],receive_asserted>          96       1       -   Covered
        bin <auto[60:63],receive_asserted>          86       1       -   Covered
        bin <auto[220:223],receive_asserted>          94       1       -   Covered
        bin <auto[92:95],receive_asserted>          96       1       -   Covered
        bin <auto[156:159],receive_asserted>          96       1       -   Covered
        bin <auto[28:31],receive_asserted>          90       1       -   Covered
        bin <auto[236:239],receive_asserted>          90       1       -   Covered
        bin <auto[108:111],receive_asserted>          94       1       -   Covered
        bin <auto[172:175],receive_asserted>          94       1       -   Covered
        bin <auto[44:47],receive_asserted>          96       1       -   Covered
        bin <auto[204:207],receive_asserted>          90       1       -   Covered
        bin <auto[76:79],receive_asserted>          84       1       -   Covered
        bin <auto[140:143],receive_asserted>          84       1       -   Covered
        bin <auto[12:15],receive_asserted>          96       1       -   Covered
        bin <auto[244:247],receive_asserted>          96       1       -   Covered
        bin <auto[116:119],receive_asserted>          88       1       -   Covered
        bin <auto[180:183],receive_asserted>          90       1       -   Covered
        bin <auto[52:55],receive_asserted>          96       1       -   Covered
        bin <auto[212:215],receive_asserted>          84       1       -   Covered
        bin <auto[84:87],receive_asserted>          96       1       -   Covered
        bin <auto[148:151],receive_asserted>          96       1       -   Covered
        bin <auto[20:23],receive_asserted>          96       1       -   Covered
        bin <auto[228:231],receive_asserted>          96       1       -   Covered
        bin <auto[100:103],receive_asserted>          96       1       -   Covered
        bin <auto[164:167],receive_asserted>          102       1       -   Covered
        bin <auto[36:39],receive_asserted>          94       1       -   Covered
        bin <auto[196:199],receive_asserted>          96       1       -   Covered
```

```
        bin <auto[68:71],receive_asserted>          94       1       -   Covered
        bin <auto[132:135],receive_asserted>        92       1       -   Covered
        bin <auto[4:7],receive_asserted>            86       1       -   Covered
        bin <auto[248:251],receive_asserted>        94       1       -   Covered
        bin <auto[120:123],receive_asserted>        92       1       -   Covered
        bin <auto[184:187],receive_asserted>        94       1       -   Covered
        bin <auto[56:59],receive_asserted>          92       1       -   Covered
        bin <auto[216:219],receive_asserted>        88       1       -   Covered
        bin <auto[88:91],receive_asserted>          96       1       -   Covered
        bin <auto[152:155],receive_asserted>        84       1       -   Covered
        bin <auto[24:27],receive_asserted>          96       1       -   Covered
        bin <auto[232:235],receive_asserted>        96       1       -   Covered
        bin <auto[104:107],receive_asserted>        96       1       -   Covered
        bin <auto[168:171],receive_asserted>        96       1       -   Covered
        bin <auto[40:43],receive_asserted>          96       1       -   Covered
        bin <auto[200:203],receive_asserted>       102       1       -   Covered
        bin <auto[72:75],receive_asserted>          98       1       -   Covered
        bin <auto[136:139],receive_asserted>       104       1       -   Covered
        bin <auto[8:11],receive_asserted>           92       1       -   Covered
        bin <auto[240:243],receive_asserted>        96       1       -   Covered
        bin <auto[112:115],receive_asserted>        96       1       -   Covered
        bin <auto[176:179],receive_asserted>        96       1       -   Covered
        bin <auto[48:51],receive_asserted>          96       1       -   Covered
        bin <auto[208:211],receive_asserted>        96       1       -   Covered
        bin <auto[80:83],receive_asserted>          96       1       -   Covered
        bin <auto[144:147],receive_asserted>        90       1       -   Covered
        bin <auto[16:19],receive_asserted>          96       1       -   Covered
        bin <auto[224:227],receive_asserted>        96       1       -   Covered
        bin <auto[96:99],receive_asserted>          80       1       -   Covered
        bin <auto[160:163],receive_asserted>        92       1       -   Covered
        bin <auto[32:35],receive_asserted>          92       1       -   Covered
        bin <auto[192:195],receive_asserted>       100       1       -   Covered
        bin <auto[64:67],receive_asserted>          80       1       -   Covered
        bin <auto[128:131],receive_asserted>        92       1       -   Covered
        bin <auto[0:3],receive_asserted>          2118       1       -   Covered
    Illegal and Ignore Bins:
        ignore_bin ignore_bin1                  114012               -   Occurred

================================================================================
=== Instance: /SPI_coverage_pkg
=== Design Unit: work.SPI_coverage_pkg
================================================================================

Covergroup Coverage:
    Covergroups                 1        na        na   100.00%
        Coverpoints/Crosses    15        na        na        na
            Covergroup Bins   522       522         0   100.00%
----------------------------------------------------------------------------------------------------
Covergroup                              Metric     Goal     Bins    Status

----------------------------------------------------------------------------------------------------
 TYPE /SPI_coverage_pkg/SPI_coverage/SPI_Wrapper     100.00%      100        -   Covered
    covered/total bins:                               522      522        -
    missing/total bins:                               0        522        -
    % Hit:                                 100.00%    100        -
    Coverpoint reset                       100.00%    100        -   Covered
        covered/total bins:                   2        2        -
        missing/total bins:                   0        2        -
        % Hit:                             100.00%    100        -
    Coverpoint Address_write               100.00%    100        -   Covered
        covered/total bins:                  64       64        -
        missing/total bins:                   0       64        -
        % Hit:                             100.00%    100        -
```

```
    Coverpoint Data_write                    100.00%      100         -    Covered
      covered/total bins:                      64         64          -
      missing/total bins:                       0         64          -
      % Hit:                             100.00%      100         -
    Coverpoint Data_read                     100.00%      100         -    Covered
      covered/total bins:                      64         64          -
      missing/total bins:                       0         64          -
      % Hit:                             100.00%      100         -
    Coverpoint Address_read                  100.00%      100         -    Covered
      covered/total bins:                      64         64          -
      missing/total bins:                       0         64          -
      % Hit:                             100.00%      100         -
    Coverpoint Send_Address_wr               100.00%      100         -    Covered
      covered/total bins:                       1          1          -
      missing/total bins:                       0          1          -
      % Hit:                             100.00%      100         -
    Coverpoint Send_Address_rd               100.00%      100         -    Covered
      covered/total bins:                       1          1          -
      missing/total bins:                       0          1          -
      % Hit:                             100.00%      100         -
    Coverpoint send_Data_wr                  100.00%      100         -    Covered
      covered/total bins:                       1          1          -
      missing/total bins:                       0          1          -
      % Hit:                             100.00%      100         -
    Coverpoint Recieving_Data_rd             100.00%      100         -    Covered
      covered/total bins:                       1          1          -
      missing/total bins:                       0          1          -
      % Hit:                             100.00%      100         -
    Coverpoint Sending_order_Read_data       100.00%      100         -    Covered
      covered/total bins:                       1          1          -
      missing/total bins:                       0          1          -
      % Hit:                             100.00%      100         -
    Coverpoint Starting_Communication        100.00%      100         -    Covered
      covered/total bins:                       3          3          -
      missing/total bins:                       0          3          -
      % Hit:                             100.00%      100         -
    Cross Actualiy_sending_addr_wr           100.00%      100         -    Covered
      covered/total bins:                      64         64          -
      missing/total bins:                       0         64          -
      % Hit:                             100.00%      100         -
    Cross Actualiy_sending_data_wr           100.00%      100         -    Covered
      covered/total bins:                      64         64          -
      missing/total bins:                       0         64          -
      % Hit:                             100.00%      100         -
    Cross Actualiy_sending_addr_rd           100.00%      100         -    Covered
      covered/total bins:                      64         64          -
      missing/total bins:                       0         64          -
      % Hit:                             100.00%      100         -
    Cross Actualiy_recieving_data            100.00%      100         -    Covered
      covered/total bins:                      64         64          -
      missing/total bins:                       0         64          -
      % Hit:                             100.00%      100         -
  Covergroup instance \/SPI_coverage_pkg::SPI_coverage::SPI_Wrapper
                                         100.00%      100         -    Covered
    covered/total bins:                       522        522          -
    missing/total bins:                         0        522          -
    % Hit:                               100.00%      100         -
    Coverpoint reset                     100.00%      100         -    Covered
      covered/total bins:                       2          2          -
      missing/total bins:                       0          2          -
      % Hit:                             100.00%      100         -
      bin reset_asserted                       12          1          -    Covered
      bin reset_disable                    122000          1          -    Covered
    Coverpoint Address_write                 100.00%      100         -    Covered
      covered/total bins:                      64         64          -
      missing/total bins:                       0         64          -
```

% Hit:	100.00%	100	-	
bin auto[0:3]	121028	1	-	Covered
bin auto[4:7]	16	1	-	Covered
bin auto[8:11]	16	1	-	Covered
bin auto[12:15]	15	1	-	Covered
bin auto[16:19]	16	1	-	Covered
bin auto[20:23]	16	1	-	Covered
bin auto[24:27]	16	1	-	Covered
bin auto[28:31]	16	1	-	Covered
bin auto[32:35]	16	1	-	Covered
bin auto[36:39]	16	1	-	Covered
bin auto[40:43]	16	1	-	Covered
bin auto[44:47]	16	1	-	Covered
bin auto[48:51]	16	1	-	Covered
bin auto[52:55]	14	1	-	Covered
bin auto[56:59]	16	1	-	Covered
bin auto[60:63]	15	1	-	Covered
bin auto[64:67]	16	1	-	Covered
bin auto[68:71]	16	1	-	Covered
bin auto[72:75]	15	1	-	Covered
bin auto[76:79]	16	1	-	Covered
bin auto[80:83]	15	1	-	Covered
bin auto[84:87]	16	1	-	Covered
bin auto[88:91]	16	1	-	Covered
bin auto[92:95]	16	1	-	Covered
bin auto[96:99]	16	1	-	Covered
bin auto[100:103]	15	1	-	Covered
bin auto[104:107]	16	1	-	Covered
bin auto[108:111]	16	1	-	Covered
bin auto[112:115]	15	1	-	Covered
bin auto[116:119]	15	1	-	Covered
bin auto[120:123]	16	1	-	Covered
bin auto[124:127]	16	1	-	Covered
bin auto[128:131]	15	1	-	Covered
bin auto[132:135]	16	1	-	Covered
bin auto[136:139]	15	1	-	Covered
bin auto[140:143]	16	1	-	Covered
bin auto[144:147]	16	1	-	Covered
bin auto[148:151]	16	1	-	Covered
bin auto[152:155]	16	1	-	Covered
bin auto[156:159]	15	1	-	Covered
bin auto[160:163]	16	1	-	Covered
bin auto[164:167]	16	1	-	Covered
bin auto[168:171]	16	1	-	Covered
bin auto[172:175]	14	1	-	Covered
bin auto[176:179]	16	1	-	Covered
bin auto[180:183]	16	1	-	Covered
bin auto[184:187]	14	1	-	Covered
bin auto[188:191]	15	1	-	Covered
bin auto[192:195]	15	1	-	Covered
bin auto[196:199]	16	1	-	Covered
bin auto[200:203]	16	1	-	Covered
bin auto[204:207]	15	1	-	Covered
bin auto[208:211]	14	1	-	Covered
bin auto[212:215]	16	1	-	Covered
bin auto[216:219]	16	1	-	Covered
bin auto[220:223]	15	1	-	Covered
bin auto[224:227]	15	1	-	Covered
bin auto[228:231]	16	1	-	Covered
bin auto[232:235]	16	1	-	Covered
bin auto[236:239]	16	1	-	Covered
bin auto[240:243]	15	1	-	Covered
bin auto[244:247]	16	1	-	Covered
bin auto[248:251]	16	1	-	Covered
bin auto[252:255]	16	1	-	Covered
Coverpoint Data_write	100.00%	100	-	Covered

covered/total bins:	64	64	-	
missing/total bins:	0	64	-	
% Hit:	100.00%	100	-	
bin auto[0:3]	121028	1	-	Covered
bin auto[4:7]	16	1	-	Covered
bin auto[8:11]	15	1	-	Covered
bin auto[12:15]	16	1	-	Covered
bin auto[16:19]	16	1	-	Covered
bin auto[20:23]	16	1	-	Covered
bin auto[24:27]	16	1	-	Covered
bin auto[28:31]	15	1	-	Covered
bin auto[32:35]	15	1	-	Covered
bin auto[36:39]	16	1	-	Covered
bin auto[40:43]	16	1	-	Covered
bin auto[44:47]	16	1	-	Covered
bin auto[48:51]	16	1	-	Covered
bin auto[52:55]	16	1	-	Covered
bin auto[56:59]	16	1	-	Covered
bin auto[60:63]	15	1	-	Covered
bin auto[64:67]	14	1	-	Covered
bin auto[68:71]	16	1	-	Covered
bin auto[72:75]	15	1	-	Covered
bin auto[76:79]	15	1	-	Covered
bin auto[80:83]	16	1	-	Covered
bin auto[84:87]	16	1	-	Covered
bin auto[88:91]	16	1	-	Covered
bin auto[92:95]	16	1	-	Covered
bin auto[96:99]	16	1	-	Covered
bin auto[100:103]	16	1	-	Covered
bin auto[104:107]	16	1	-	Covered
bin auto[108:111]	16	1	-	Covered
bin auto[112:115]	16	1	-	Covered
bin auto[116:119]	15	1	-	Covered
bin auto[120:123]	13	1	-	Covered
bin auto[124:127]	16	1	-	Covered
bin auto[128:131]	15	1	-	Covered
bin auto[132:135]	15	1	-	Covered
bin auto[136:139]	16	1	-	Covered
bin auto[140:143]	14	1	-	Covered
bin auto[144:147]	15	1	-	Covered
bin auto[148:151]	16	1	-	Covered
bin auto[152:155]	15	1	-	Covered
bin auto[156:159]	16	1	-	Covered
bin auto[160:163]	15	1	-	Covered
bin auto[164:167]	16	1	-	Covered
bin auto[168:171]	16	1	-	Covered
bin auto[172:175]	16	1	-	Covered
bin auto[176:179]	16	1	-	Covered
bin auto[180:183]	15	1	-	Covered
bin auto[184:187]	16	1	-	Covered
bin auto[188:191]	16	1	-	Covered
bin auto[192:195]	16	1	-	Covered
bin auto[196:199]	16	1	-	Covered
bin auto[200:203]	16	1	-	Covered
bin auto[204:207]	16	1	-	Covered
bin auto[208:211]	16	1	-	Covered
bin auto[212:215]	13	1	-	Covered
bin auto[216:219]	16	1	-	Covered
bin auto[220:223]	16	1	-	Covered
bin auto[224:227]	16	1	-	Covered
bin auto[228:231]	16	1	-	Covered
bin auto[232:235]	16	1	-	Covered
bin auto[236:239]	15	1	-	Covered
bin auto[240:243]	16	1	-	Covered
bin auto[244:247]	16	1	-	Covered
bin auto[248:251]	16	1	-	Covered

bin auto[252:255]	16	1	-	Covered
Coverpoint Data_read	100.00%	100	-	Covered
covered/total bins:	64	64	-	
missing/total bins:	0	64	-	
% Hit:	100.00%	100	-	
bin auto[0:3]	121028	1	-	Covered
bin auto[4:7]	16	1	-	Covered
bin auto[8:11]	15	1	-	Covered
bin auto[12:15]	16	1	-	Covered
bin auto[16:19]	16	1	-	Covered
bin auto[20:23]	16	1	-	Covered
bin auto[24:27]	16	1	-	Covered
bin auto[28:31]	15	1	-	Covered
bin auto[32:35]	15	1	-	Covered
bin auto[36:39]	16	1	-	Covered
bin auto[40:43]	16	1	-	Covered
bin auto[44:47]	16	1	-	Covered
bin auto[48:51]	16	1	-	Covered
bin auto[52:55]	16	1	-	Covered
bin auto[56:59]	16	1	-	Covered
bin auto[60:63]	15	1	-	Covered
bin auto[64:67]	14	1	-	Covered
bin auto[68:71]	16	1	-	Covered
bin auto[72:75]	15	1	-	Covered
bin auto[76:79]	15	1	-	Covered
bin auto[80:83]	16	1	-	Covered
bin auto[84:87]	16	1	-	Covered
bin auto[88:91]	16	1	-	Covered
bin auto[92:95]	16	1	-	Covered
bin auto[96:99]	16	1	-	Covered
bin auto[100:103]	16	1	-	Covered
bin auto[104:107]	16	1	-	Covered
bin auto[108:111]	16	1	-	Covered
bin auto[112:115]	16	1	-	Covered
bin auto[116:119]	15	1	-	Covered
bin auto[120:123]	13	1	-	Covered
bin auto[124:127]	16	1	-	Covered
bin auto[128:131]	15	1	-	Covered
bin auto[132:135]	15	1	-	Covered
bin auto[136:139]	16	1	-	Covered
bin auto[140:143]	14	1	-	Covered
bin auto[144:147]	15	1	-	Covered
bin auto[148:151]	16	1	-	Covered
bin auto[152:155]	15	1	-	Covered
bin auto[156:159]	16	1	-	Covered
bin auto[160:163]	15	1	-	Covered
bin auto[164:167]	16	1	-	Covered
bin auto[168:171]	16	1	-	Covered
bin auto[172:175]	16	1	-	Covered
bin auto[176:179]	16	1	-	Covered
bin auto[180:183]	15	1	-	Covered
bin auto[184:187]	16	1	-	Covered
bin auto[188:191]	16	1	-	Covered
bin auto[192:195]	16	1	-	Covered
bin auto[196:199]	16	1	-	Covered
bin auto[200:203]	16	1	-	Covered
bin auto[204:207]	16	1	-	Covered
bin auto[208:211]	16	1	-	Covered
bin auto[212:215]	13	1	-	Covered
bin auto[216:219]	16	1	-	Covered
bin auto[220:223]	16	1	-	Covered
bin auto[224:227]	16	1	-	Covered
bin auto[228:231]	16	1	-	Covered
bin auto[232:235]	16	1	-	Covered
bin auto[236:239]	15	1	-	Covered
bin auto[240:243]	16	1	-	Covered

bin auto[244:247]	16	1	-	Covered	
bin auto[248:251]	16	1	-	Covered	
bin auto[252:255]	16	1	-	Covered	
Coverpoint Address_read	100.00%	100	-	Covered	
covered/total bins:	64	64	-		
missing/total bins:	0	64	-		
% Hit:	100.00%	100	-		
bin auto[0:3]	121028	1	-	Covered	
bin auto[4:7]	16	1	-	Covered	
bin auto[8:11]	16	1	-	Covered	
bin auto[12:15]	15	1	-	Covered	
bin auto[16:19]	16	1	-	Covered	
bin auto[20:23]	16	1	-	Covered	
bin auto[24:27]	16	1	-	Covered	
bin auto[28:31]	16	1	-	Covered	
bin auto[32:35]	16	1	-	Covered	
bin auto[36:39]	16	1	-	Covered	
bin auto[40:43]	16	1	-	Covered	
bin auto[44:47]	16	1	-	Covered	
bin auto[48:51]	16	1	-	Covered	
bin auto[52:55]	14	1	-	Covered	
bin auto[56:59]	16	1	-	Covered	
bin auto[60:63]	15	1	-	Covered	
bin auto[64:67]	16	1	-	Covered	
bin auto[68:71]	16	1	-	Covered	
bin auto[72:75]	15	1	-	Covered	
bin auto[76:79]	16	1	-	Covered	
bin auto[80:83]	15	1	-	Covered	
bin auto[84:87]	16	1	-	Covered	
bin auto[88:91]	16	1	-	Covered	
bin auto[92:95]	16	1	-	Covered	
bin auto[96:99]	16	1	-	Covered	
bin auto[100:103]	15	1	-	Covered	
bin auto[104:107]	16	1	-	Covered	
bin auto[108:111]	16	1	-	Covered	
bin auto[112:115]	15	1	-	Covered	
bin auto[116:119]	15	1	-	Covered	
bin auto[120:123]	16	1	-	Covered	
bin auto[124:127]	16	1	-	Covered	
bin auto[128:131]	15	1	-	Covered	
bin auto[132:135]	16	1	-	Covered	
bin auto[136:139]	15	1	-	Covered	
bin auto[140:143]	16	1	-	Covered	
bin auto[144:147]	16	1	-	Covered	
bin auto[148:151]	16	1	-	Covered	
bin auto[152:155]	16	1	-	Covered	
bin auto[156:159]	15	1	-	Covered	
bin auto[160:163]	16	1	-	Covered	
bin auto[164:167]	16	1	-	Covered	
bin auto[168:171]	16	1	-	Covered	
bin auto[172:175]	14	1	-	Covered	
bin auto[176:179]	16	1	-	Covered	
bin auto[180:183]	16	1	-	Covered	
bin auto[184:187]	14	1	-	Covered	
bin auto[188:191]	15	1	-	Covered	
bin auto[192:195]	15	1	-	Covered	
bin auto[196:199]	16	1	-	Covered	
bin auto[200:203]	16	1	-	Covered	
bin auto[204:207]	15	1	-	Covered	
bin auto[208:211]	14	1	-	Covered	
bin auto[212:215]	16	1	-	Covered	
bin auto[216:219]	16	1	-	Covered	
bin auto[220:223]	15	1	-	Covered	
bin auto[224:227]	15	1	-	Covered	
bin auto[228:231]	16	1	-	Covered	
bin auto[232:235]	16	1	-	Covered	

```
    bin auto[236:239]                    16        1        -    Covered
    bin auto[240:243]                    15        1        -    Covered
    bin auto[244:247]                    16        1        -    Covered
    bin auto[248:251]                    16        1        -    Covered
    bin auto[252:255]                    16        1        -    Covered
  Coverpoint Send_Address_wr          100.00%      100        -    Covered
    covered/total bins:                   1        1        -
    missing/total bins:                   0        1        -
    % Hit:                          100.00%      100        -
    bin writing_add                   11000        1        -    Covered
  Coverpoint Send_Address_rd          100.00%      100        -    Covered
    covered/total bins:                   1        1        -
    missing/total bins:                   0        1        -
    % Hit:                          100.00%      100        -
    bin reading_add                   11000        1        -    Covered
  Coverpoint send_Data_wr             100.00%      100        -    Covered
    covered/total bins:                   1        1        -
    missing/total bins:                   0        1        -
    % Hit:                          100.00%      100        -
    bin writing_data                  11000        1        -    Covered
  Coverpoint Recieving_Data_rd        100.00%      100        -    Covered
    covered/total bins:                   1        1        -
    missing/total bins:                   0        1        -
    % Hit:                          100.00%      100        -
    bin reading_data                   8000        1        -    Covered
  Coverpoint Sending_order_Read_data  100.00%      100        -    Covered
    covered/total bins:                   1        1        -
    missing/total bins:                   0        1        -
    % Hit:                          100.00%      100        -
    bin order_reading_data            11000        1        -    Covered
  Coverpoint Starting_Communication   100.00%      100        -    Covered
    covered/total bins:                   3        3        -
    missing/total bins:                   0        3        -
    % Hit:                          100.00%      100        -
    bin Start                        114000        1        -    Covered
    bin End                            8012        1        -    Covered
    bin transaction_back               7988        1        -    Covered
  Cross Actualiy_sending_addr_wr      100.00%      100        -    Covered
    covered/total bins:                  64       64        -
    missing/total bins:                   0       64        -
    % Hit:                          100.00%      100        -
    Auto, Default and User Defined Bins:
      bin <writing_add,auto[252:255]>          16        1        -    Covered
      bin <writing_add,auto[248:251]>          16        1        -    Covered
      bin <writing_add,auto[244:247]>          16        1        -    Covered
      bin <writing_add,auto[240:243]>          15        1        -    Covered
      bin <writing_add,auto[236:239]>          16        1        -    Covered
      bin <writing_add,auto[232:235]>          16        1        -    Covered
      bin <writing_add,auto[228:231]>          16        1        -    Covered
      bin <writing_add,auto[224:227]>          15        1        -    Covered
      bin <writing_add,auto[220:223]>          15        1        -    Covered
      bin <writing_add,auto[216:219]>          16        1        -    Covered
      bin <writing_add,auto[212:215]>          16        1        -    Covered
      bin <writing_add,auto[208:211]>          14        1        -    Covered
      bin <writing_add,auto[204:207]>          15        1        -    Covered
      bin <writing_add,auto[200:203]>          16        1        -    Covered
      bin <writing_add,auto[196:199]>          16        1        -    Covered
      bin <writing_add,auto[192:195]>          15        1        -    Covered
      bin <writing_add,auto[188:191]>          15        1        -    Covered
      bin <writing_add,auto[184:187]>          14        1        -    Covered
      bin <writing_add,auto[180:183]>          16        1        -    Covered
      bin <writing_add,auto[176:179]>          16        1        -    Covered
      bin <writing_add,auto[172:175]>          14        1        -    Covered
      bin <writing_add,auto[168:171]>          16        1        -    Covered
      bin <writing_add,auto[164:167]>          16        1        -    Covered
      bin <writing_add,auto[160:163]>          16        1        -    Covered
```

bin <writing_add,auto[156:159]>	15	1	-	Covered
bin <writing_add,auto[152:155]>	16	1	-	Covered
bin <writing_add,auto[148:151]>	16	1	-	Covered
bin <writing_add,auto[144:147]>	16	1	-	Covered
bin <writing_add,auto[140:143]>	16	1	-	Covered
bin <writing_add,auto[136:139]>	15	1	-	Covered
bin <writing_add,auto[132:135]>	16	1	-	Covered
bin <writing_add,auto[128:131]>	15	1	-	Covered
bin <writing_add,auto[124:127]>	16	1	-	Covered
bin <writing_add,auto[120:123]>	16	1	-	Covered
bin <writing_add,auto[116:119]>	15	1	-	Covered
bin <writing_add,auto[112:115]>	15	1	-	Covered
bin <writing_add,auto[108:111]>	16	1	-	Covered
bin <writing_add,auto[104:107]>	16	1	-	Covered
bin <writing_add,auto[100:103]>	15	1	-	Covered
bin <writing_add,auto[96:99]>	16	1	-	Covered
bin <writing_add,auto[92:95]>	16	1	-	Covered
bin <writing_add,auto[88:91]>	16	1	-	Covered
bin <writing_add,auto[84:87]>	16	1	-	Covered
bin <writing_add,auto[80:83]>	15	1	-	Covered
bin <writing_add,auto[76:79]>	16	1	-	Covered
bin <writing_add,auto[72:75]>	15	1	-	Covered
bin <writing_add,auto[68:71]>	16	1	-	Covered
bin <writing_add,auto[64:67]>	16	1	-	Covered
bin <writing_add,auto[60:63]>	15	1	-	Covered
bin <writing_add,auto[56:59]>	16	1	-	Covered
bin <writing_add,auto[52:55]>	14	1	-	Covered
bin <writing_add,auto[48:51]>	16	1	-	Covered
bin <writing_add,auto[44:47]>	16	1	-	Covered
bin <writing_add,auto[40:43]>	16	1	-	Covered
bin <writing_add,auto[36:39]>	16	1	-	Covered
bin <writing_add,auto[32:35]>	16	1	-	Covered
bin <writing_add,auto[28:31]>	16	1	-	Covered
bin <writing_add,auto[24:27]>	16	1	-	Covered
bin <writing_add,auto[20:23]>	16	1	-	Covered
bin <writing_add,auto[16:19]>	16	1	-	Covered
bin <writing_add,auto[12:15]>	15	1	-	Covered
bin <writing_add,auto[8:11]>	16	1	-	Covered
bin <writing_add,auto[4:7]>	16	1	-	Covered
bin <writing_add,auto[0:3]>	10016	1	-	Covered
Cross Actualiy_sending_data_wr	100.00%	100	-	Covered
covered/total bins:	64	64	-	
missing/total bins:	0	64	-	
% Hit:	100.00%	100	-	
Auto, Default and User Defined Bins:				
bin <writing_data,auto[252:255]>	16	1	-	Covered
bin <writing_data,auto[248:251]>	16	1	-	Covered
bin <writing_data,auto[244:247]>	16	1	-	Covered
bin <writing_data,auto[240:243]>	16	1	-	Covered
bin <writing_data,auto[236:239]>	15	1	-	Covered
bin <writing_data,auto[232:235]>	16	1	-	Covered
bin <writing_data,auto[228:231]>	16	1	-	Covered
bin <writing_data,auto[224:227]>	16	1	-	Covered
bin <writing_data,auto[220:223]>	16	1	-	Covered
bin <writing_data,auto[216:219]>	16	1	-	Covered
bin <writing_data,auto[212:215]>	13	1	-	Covered
bin <writing_data,auto[208:211]>	16	1	-	Covered
bin <writing_data,auto[204:207]>	16	1	-	Covered
bin <writing_data,auto[200:203]>	16	1	-	Covered
bin <writing_data,auto[196:199]>	16	1	-	Covered
bin <writing_data,auto[192:195]>	16	1	-	Covered
bin <writing_data,auto[188:191]>	16	1	-	Covered
bin <writing_data,auto[184:187]>	16	1	-	Covered
bin <writing_data,auto[180:183]>	15	1	-	Covered
bin <writing_data,auto[176:179]>	16	1	-	Covered
bin <writing_data,auto[172:175]>	16	1	-	Covered

```
        bin <writing_data,auto[168:171]>          16       1       -   Covered
        bin <writing_data,auto[164:167]>          16       1       -   Covered
        bin <writing_data,auto[160:163]>          15       1       -   Covered
        bin <writing_data,auto[156:159]>          16       1       -   Covered
        bin <writing_data,auto[152:155]>          15       1       -   Covered
        bin <writing_data,auto[148:151]>          16       1       -   Covered
        bin <writing_data,auto[144:147]>          15       1       -   Covered
        bin <writing_data,auto[140:143]>          14       1       -   Covered
        bin <writing_data,auto[136:139]>          16       1       -   Covered
        bin <writing_data,auto[132:135]>          15       1       -   Covered
        bin <writing_data,auto[128:131]>          15       1       -   Covered
        bin <writing_data,auto[124:127]>          16       1       -   Covered
        bin <writing_data,auto[120:123]>          13       1       -   Covered
        bin <writing_data,auto[116:119]>          15       1       -   Covered
        bin <writing_data,auto[112:115]>          16       1       -   Covered
        bin <writing_data,auto[108:111]>          16       1       -   Covered
        bin <writing_data,auto[104:107]>          16       1       -   Covered
        bin <writing_data,auto[100:103]>          16       1       -   Covered
        bin <writing_data,auto[96:99]>            16       1       -   Covered
        bin <writing_data,auto[92:95]>            16       1       -   Covered
        bin <writing_data,auto[88:91]>            16       1       -   Covered
        bin <writing_data,auto[84:87]>            16       1       -   Covered
        bin <writing_data,auto[80:83]>            16       1       -   Covered
        bin <writing_data,auto[76:79]>            15       1       -   Covered
        bin <writing_data,auto[72:75]>            15       1       -   Covered
        bin <writing_data,auto[68:71]>            16       1       -   Covered
        bin <writing_data,auto[64:67]>            14       1       -   Covered
        bin <writing_data,auto[60:63]>            15       1       -   Covered
        bin <writing_data,auto[56:59]>            16       1       -   Covered
        bin <writing_data,auto[52:55]>            16       1       -   Covered
        bin <writing_data,auto[48:51]>            16       1       -   Covered
        bin <writing_data,auto[44:47]>            16       1       -   Covered
        bin <writing_data,auto[40:43]>            16       1       -   Covered
        bin <writing_data,auto[36:39]>            16       1       -   Covered
        bin <writing_data,auto[32:35]>            15       1       -   Covered
        bin <writing_data,auto[28:31]>            15       1       -   Covered
        bin <writing_data,auto[24:27]>            16       1       -   Covered
        bin <writing_data,auto[20:23]>            16       1       -   Covered
        bin <writing_data,auto[16:19]>            16       1       -   Covered
        bin <writing_data,auto[12:15]>            16       1       -   Covered
        bin <writing_data,auto[8:11]>             15       1       -   Covered
        bin <writing_data,auto[4:7]>              16       1       -   Covered
        bin <writing_data,auto[0:3]>           10016       1       -   Covered
    Cross Actualiy_sending_addr_rd                100.00%      100       -   Covered
      covered/total bins:                    64       64       -
      missing/total bins:                    0        64       -
      % Hit:                          100.00%       100       -
      Auto, Default and User Defined Bins:
        bin <reading_add,auto[252:255]>           16       1       -   Covered
        bin <reading_add,auto[248:251]>           16       1       -   Covered
        bin <reading_add,auto[244:247]>           16       1       -   Covered
        bin <reading_add,auto[240:243]>           15       1       -   Covered
        bin <reading_add,auto[236:239]>           16       1       -   Covered
        bin <reading_add,auto[232:235]>           16       1       -   Covered
        bin <reading_add,auto[228:231]>           16       1       -   Covered
        bin <reading_add,auto[224:227]>           15       1       -   Covered
        bin <reading_add,auto[220:223]>           15       1       -   Covered
        bin <reading_add,auto[216:219]>           16       1       -   Covered
        bin <reading_add,auto[212:215]>           16       1       -   Covered
        bin <reading_add,auto[208:211]>           14       1       -   Covered
        bin <reading_add,auto[204:207]>           15       1       -   Covered
        bin <reading_add,auto[200:203]>           16       1       -   Covered
        bin <reading_add,auto[196:199]>           16       1       -   Covered
        bin <reading_add,auto[192:195]>           15       1       -   Covered
        bin <reading_add,auto[188:191]>           15       1       -   Covered
        bin <reading_add,auto[184:187]>           14       1       -   Covered
```

bin <reading_add,auto[180:183]>	16	1	-	Covered
bin <reading_add,auto[176:179]>	16	1	-	Covered
bin <reading_add,auto[172:175]>	14	1	-	Covered
bin <reading_add,auto[168:171]>	16	1	-	Covered
bin <reading_add,auto[164:167]>	16	1	-	Covered
bin <reading_add,auto[160:163]>	16	1	-	Covered
bin <reading_add,auto[156:159]>	15	1	-	Covered
bin <reading_add,auto[152:155]>	16	1	-	Covered
bin <reading_add,auto[148:151]>	16	1	-	Covered
bin <reading_add,auto[144:147]>	16	1	-	Covered
bin <reading_add,auto[140:143]>	16	1	-	Covered
bin <reading_add,auto[136:139]>	15	1	-	Covered
bin <reading_add,auto[132:135]>	16	1	-	Covered
bin <reading_add,auto[128:131]>	15	1	-	Covered
bin <reading_add,auto[124:127]>	16	1	-	Covered
bin <reading_add,auto[120:123]>	16	1	-	Covered
bin <reading_add,auto[116:119]>	15	1	-	Covered
bin <reading_add,auto[112:115]>	15	1	-	Covered
bin <reading_add,auto[108:111]>	16	1	-	Covered
bin <reading_add,auto[104:107]>	16	1	-	Covered
bin <reading_add,auto[100:103]>	15	1	-	Covered
bin <reading_add,auto[96:99]>	16	1	-	Covered
bin <reading_add,auto[92:95]>	16	1	-	Covered
bin <reading_add,auto[88:91]>	16	1	-	Covered
bin <reading_add,auto[84:87]>	16	1	-	Covered
bin <reading_add,auto[80:83]>	15	1	-	Covered
bin <reading_add,auto[76:79]>	16	1	-	Covered
bin <reading_add,auto[72:75]>	15	1	-	Covered
bin <reading_add,auto[68:71]>	16	1	-	Covered
bin <reading_add,auto[64:67]>	16	1	-	Covered
bin <reading_add,auto[60:63]>	15	1	-	Covered
bin <reading_add,auto[56:59]>	16	1	-	Covered
bin <reading_add,auto[52:55]>	14	1	-	Covered
bin <reading_add,auto[48:51]>	16	1	-	Covered
bin <reading_add,auto[44:47]>	16	1	-	Covered
bin <reading_add,auto[40:43]>	16	1	-	Covered
bin <reading_add,auto[36:39]>	16	1	-	Covered
bin <reading_add,auto[32:35]>	16	1	-	Covered
bin <reading_add,auto[28:31]>	16	1	-	Covered
bin <reading_add,auto[24:27]>	16	1	-	Covered
bin <reading_add,auto[20:23]>	16	1	-	Covered
bin <reading_add,auto[16:19]>	16	1	-	Covered
bin <reading_add,auto[12:15]>	15	1	-	Covered
bin <reading_add,auto[8:11]>	16	1	-	Covered
bin <reading_add,auto[4:7]>	16	1	-	Covered
bin <reading_add,auto[0:3]>	10016	1	-	Covered
Cross Actualiy_recieving_data	100.00%	100	-	Covered
covered/total bins:	64	64	-	
missing/total bins:	0	64	-	
% Hit:	100.00%	100	-	
Auto, Default and User Defined Bins:				
bin <reading_data,auto[252:255]>	16	1	-	Covered
bin <reading_data,auto[248:251]>	16	1	-	Covered
bin <reading_data,auto[244:247]>	16	1	-	Covered
bin <reading_data,auto[240:243]>	16	1	-	Covered
bin <reading_data,auto[236:239]>	15	1	-	Covered
bin <reading_data,auto[232:235]>	16	1	-	Covered
bin <reading_data,auto[228:231]>	16	1	-	Covered
bin <reading_data,auto[224:227]>	16	1	-	Covered
bin <reading_data,auto[220:223]>	16	1	-	Covered
bin <reading_data,auto[216:219]>	16	1	-	Covered
bin <reading_data,auto[212:215]>	13	1	-	Covered
bin <reading_data,auto[208:211]>	16	1	-	Covered
bin <reading_data,auto[204:207]>	16	1	-	Covered
bin <reading_data,auto[200:203]>	16	1	-	Covered
bin <reading_data,auto[196:199]>	16	1	-	Covered

```
        bin <reading_data,auto[192:195]>          16       1       -   Covered
        bin <reading_data,auto[188:191]>          16       1       -   Covered
        bin <reading_data,auto[184:187]>          16       1       -   Covered
        bin <reading_data,auto[180:183]>          15       1       -   Covered
        bin <reading_data,auto[176:179]>          16       1       -   Covered
        bin <reading_data,auto[172:175]>          16       1       -   Covered
        bin <reading_data,auto[168:171]>          16       1       -   Covered
        bin <reading_data,auto[164:167]>          16       1       -   Covered
        bin <reading_data,auto[160:163]>          15       1       -   Covered
        bin <reading_data,auto[156:159]>          16       1       -   Covered
        bin <reading_data,auto[152:155]>          15       1       -   Covered
        bin <reading_data,auto[148:151]>          16       1       -   Covered
        bin <reading_data,auto[144:147]>          15       1       -   Covered
        bin <reading_data,auto[140:143]>          14       1       -   Covered
        bin <reading_data,auto[136:139]>          16       1       -   Covered
        bin <reading_data,auto[132:135]>          15       1       -   Covered
        bin <reading_data,auto[128:131]>          15       1       -   Covered
        bin <reading_data,auto[124:127]>          16       1       -   Covered
        bin <reading_data,auto[120:123]>          13       1       -   Covered
        bin <reading_data,auto[116:119]>          15       1       -   Covered
        bin <reading_data,auto[112:115]>          16       1       -   Covered
        bin <reading_data,auto[108:111]>          16       1       -   Covered
        bin <reading_data,auto[104:107]>          16       1       -   Covered
        bin <reading_data,auto[100:103]>          16       1       -   Covered
        bin <reading_data,auto[96:99]>            16       1       -   Covered
        bin <reading_data,auto[92:95]>            16       1       -   Covered
        bin <reading_data,auto[88:91]>            16       1       -   Covered
        bin <reading_data,auto[84:87]>            16       1       -   Covered
        bin <reading_data,auto[80:83]>            16       1       -   Covered
        bin <reading_data,auto[76:79]>            15       1       -   Covered
        bin <reading_data,auto[72:75]>            15       1       -   Covered
        bin <reading_data,auto[68:71]>            16       1       -   Covered
        bin <reading_data,auto[64:67]>            14       1       -   Covered
        bin <reading_data,auto[60:63]>            15       1       -   Covered
        bin <reading_data,auto[56:59]>            16       1       -   Covered
        bin <reading_data,auto[52:55]>            16       1       -   Covered
        bin <reading_data,auto[48:51]>            16       1       -   Covered
        bin <reading_data,auto[44:47]>            16       1       -   Covered
        bin <reading_data,auto[40:43]>            16       1       -   Covered
        bin <reading_data,auto[36:39]>            16       1       -   Covered
        bin <reading_data,auto[32:35]>            15       1       -   Covered
        bin <reading_data,auto[28:31]>            15       1       -   Covered
        bin <reading_data,auto[24:27]>            16       1       -   Covered
        bin <reading_data,auto[20:23]>            16       1       -   Covered
        bin <reading_data,auto[16:19]>            16       1       -   Covered
        bin <reading_data,auto[12:15]>            16       1       -   Covered
        bin <reading_data,auto[8:11]>             15       1       -   Covered
        bin <reading_data,auto[4:7]>              16       1       -   Covered
        bin <reading_data,auto[0:3]>            7016       1       -   Covered

COVERGROUP COVERAGE:
----------------------------------------------------------------------------------------------------
Covergroup                                Metric      Goal      Bins    Status

----------------------------------------------------------------------------------------------------
 TYPE /RAM_coverage_pkg/RAM_coverage/cvr_gp          100.00%       100         -   Covered
   covered/total bins:                              655       655         -
   missing/total bins:                                0       655         -
   % Hit:                                       100.00%       100         -
   Coverpoint reset                             100.00%       100         -   Covered
     covered/total bins:                              2         2         -
     missing/total bins:                              0         2         -
     % Hit:                                     100.00%       100         -
   Coverpoint data_valid                        100.00%       100         -   Covered
     covered/total bins:                              9         9         -
     missing/total bins:                              0         9         -
```

```
    % Hit:                    100.00%      100        -
  Coverpoint data_written     100.00%      100        -    Covered
    covered/total bins:          64        64        -
    missing/total bins:           0        64        -
    % Hit:                    100.00%      100        -
  Coverpoint data_read        100.00%      100        -    Covered
    covered/total bins:          64        64        -
    missing/total bins:           0        64        -
    % Hit:                    100.00%      100        -
  Coverpoint address_written  100.00%      100        -    Covered
    covered/total bins:          64        64        -
    missing/total bins:           0        64        -
    % Hit:                    100.00%      100        -
  Coverpoint address_read     100.00%      100        -    Covered
    covered/total bins:          64        64        -
    missing/total bins:           0        64        -
    % Hit:                    100.00%      100        -
  Coverpoint receive_valid    100.00%      100        -    Covered
    covered/total bins:           2         2        -
    missing/total bins:           0         2        -
    % Hit:                    100.00%      100        -
  Coverpoint send_valid       100.00%      100        -    Covered
    covered/total bins:           2         2        -
    missing/total bins:           0         2        -
    % Hit:                    100.00%      100        -
  Cross Writing_address       100.00%      100        -    Covered
    covered/total bins:         128       128        -
    missing/total bins:           0       128        -
    % Hit:                    100.00%      100        -
  Cross Writing_data          100.00%      100        -    Covered
    covered/total bins:         128       128        -
    missing/total bins:           0       128        -
    % Hit:                    100.00%      100        -
  Cross reading_address       100.00%      100        -    Covered
    covered/total bins:          64        64        -
    missing/total bins:           0        64        -
    % Hit:                    100.00%      100        -
  Cross reading_data          100.00%      100        -    Covered
    covered/total bins:          64        64        -
    missing/total bins:           0        64        -
    % Hit:                    100.00%      100        -
Covergroup instance \/RAM_coverage_pkg::RAM_coverage::cvr_gp
                              100.00%      100        -    Covered
  covered/total bins:           655       655        -
  missing/total bins:             0       655        -
  % Hit:                      100.00%      100        -
  Coverpoint reset            100.00%      100        -    Covered
    covered/total bins:           2         2        -
    missing/total bins:           0         2        -
    % Hit:                    100.00%      100        -
    bin reset_asserted           12         1        -    Covered
    bin reset_disable        122000         1        -    Covered
  Coverpoint data_valid       100.00%      100        -    Covered
    covered/total bins:           9         9        -
    missing/total bins:           0         9        -
    % Hit:                    100.00%      100        -
    bin writing_complete        6000         1        -    Covered
    bin writing                94012         1        -    Covered
    bin reading                 2000         1        -    Covered
    bin change_wr_rd            2000         1        -    Covered
    bin change_rd_wr            2000         1        -    Covered
    bin default_values[0]      94012         1        -    Covered
    bin default_values[1]       6000         1        -    Covered
    bin default_values[2]       2000         1        -    Covered
    bin default_values[3]      20000         1        -    Covered
  Coverpoint data_written     100.00%      100        -    Covered
```

covered/total bins:	64	64	-	
missing/total bins:	0	64	-	
% Hit:	100.00%	100	-	
bin auto[0:3]	116107	1	-	Covered
bin auto[4:7]	94	1	-	Covered
bin auto[8:11]	95	1	-	Covered
bin auto[12:15]	95	1	-	Covered
bin auto[16:19]	95	1	-	Covered
bin auto[20:23]	95	1	-	Covered
bin auto[24:27]	93	1	-	Covered
bin auto[28:31]	93	1	-	Covered
bin auto[32:35]	93	1	-	Covered
bin auto[36:39]	94	1	-	Covered
bin auto[40:43]	95	1	-	Covered
bin auto[44:47]	96	1	-	Covered
bin auto[48:51]	95	1	-	Covered
bin auto[52:55]	94	1	-	Covered
bin auto[56:59]	93	1	-	Covered
bin auto[60:63]	95	1	-	Covered
bin auto[64:67]	92	1	-	Covered
bin auto[68:71]	94	1	-	Covered
bin auto[72:75]	92	1	-	Covered
bin auto[76:79]	92	1	-	Covered
bin auto[80:83]	95	1	-	Covered
bin auto[84:87]	91	1	-	Covered
bin auto[88:91]	96	1	-	Covered
bin auto[92:95]	92	1	-	Covered
bin auto[96:99]	93	1	-	Covered
bin auto[100:103]	95	1	-	Covered
bin auto[104:107]	91	1	-	Covered
bin auto[108:111]	94	1	-	Covered
bin auto[112:115]	93	1	-	Covered
bin auto[116:119]	94	1	-	Covered
bin auto[120:123]	90	1	-	Covered
bin auto[124:127]	95	1	-	Covered
bin auto[128:131]	91	1	-	Covered
bin auto[132:135]	94	1	-	Covered
bin auto[136:139]	93	1	-	Covered
bin auto[140:143]	91	1	-	Covered
bin auto[144:147]	91	1	-	Covered
bin auto[148:151]	95	1	-	Covered
bin auto[152:155]	94	1	-	Covered
bin auto[156:159]	95	1	-	Covered
bin auto[160:163]	93	1	-	Covered
bin auto[164:167]	92	1	-	Covered
bin auto[168:171]	95	1	-	Covered
bin auto[172:175]	95	1	-	Covered
bin auto[176:179]	95	1	-	Covered
bin auto[180:183]	93	1	-	Covered
bin auto[184:187]	93	1	-	Covered
bin auto[188:191]	92	1	-	Covered
bin auto[192:195]	93	1	-	Covered
bin auto[196:199]	93	1	-	Covered
bin auto[200:203]	94	1	-	Covered
bin auto[204:207]	95	1	-	Covered
bin auto[208:211]	94	1	-	Covered
bin auto[212:215]	92	1	-	Covered
bin auto[216:219]	94	1	-	Covered
bin auto[220:223]	95	1	-	Covered
bin auto[224:227]	96	1	-	Covered
bin auto[228:231]	96	1	-	Covered
bin auto[232:235]	93	1	-	Covered
bin auto[236:239]	95	1	-	Covered
bin auto[240:243]	96	1	-	Covered
bin auto[244:247]	94	1	-	Covered
bin auto[248:251]	95	1	-	Covered

bin auto[252:255]	94	1	-	Covered
Coverpoint data_read	100.00%	100	-	Covered
covered/total bins:	64	64	-	
missing/total bins:	0	64	-	
% Hit:	100.00%	100	-	
bin auto[0:3]	27817	1	-	Covered
bin auto[4:7]	1361	1	-	Covered
bin auto[8:11]	1475	1	-	Covered
bin auto[12:15]	1536	1	-	Covered
bin auto[16:19]	1536	1	-	Covered
bin auto[20:23]	1536	1	-	Covered
bin auto[24:27]	1536	1	-	Covered
bin auto[28:31]	1440	1	-	Covered
bin auto[32:35]	1475	1	-	Covered
bin auto[36:39]	1501	1	-	Covered
bin auto[40:43]	1536	1	-	Covered
bin auto[44:47]	1536	1	-	Covered
bin auto[48:51]	1536	1	-	Covered
bin auto[52:55]	1536	1	-	Covered
bin auto[56:59]	1485	1	-	Covered
bin auto[60:63]	1389	1	-	Covered
bin auto[64:67]	1274	1	-	Covered
bin auto[68:71]	1501	1	-	Covered
bin auto[72:75]	1590	1	-	Covered
bin auto[76:79]	1335	1	-	Covered
bin auto[80:83]	1536	1	-	Covered
bin auto[84:87]	1536	1	-	Covered
bin auto[88:91]	1536	1	-	Covered
bin auto[92:95]	1536	1	-	Covered
bin auto[96:99]	1256	1	-	Covered
bin auto[100:103]	1536	1	-	Covered
bin auto[104:107]	1536	1	-	Covered
bin auto[108:111]	1501	1	-	Covered
bin auto[112:115]	1536	1	-	Covered
bin auto[116:119]	1424	1	-	Covered
bin auto[120:123]	1493	1	-	Covered
bin auto[124:127]	1536	1	-	Covered
bin auto[128:131]	1475	1	-	Covered
bin auto[132:135]	1475	1	-	Covered
bin auto[136:139]	1676	1	-	Covered
bin auto[140:143]	1344	1	-	Covered
bin auto[144:147]	1440	1	-	Covered
bin auto[148:151]	1536	1	-	Covered
bin auto[152:155]	1354	1	-	Covered
bin auto[156:159]	1536	1	-	Covered
bin auto[160:163]	1475	1	-	Covered
bin auto[164:167]	1641	1	-	Covered
bin auto[168:171]	1536	1	-	Covered
bin auto[172:175]	1501	1	-	Covered
bin auto[176:179]	1536	1	-	Covered
bin auto[180:183]	1440	1	-	Covered
bin auto[184:187]	1501	1	-	Covered
bin auto[188:191]	1536	1	-	Covered
bin auto[192:195]	1616	1	-	Covered
bin auto[196:199]	1536	1	-	Covered
bin auto[200:203]	1641	1	-	Covered
bin auto[204:207]	1451	1	-	Covered
bin auto[208:211]	1536	1	-	Covered
bin auto[212:215]	1353	1	-	Covered
bin auto[216:219]	1396	1	-	Covered
bin auto[220:223]	1501	1	-	Covered
bin auto[224:227]	1536	1	-	Covered
bin auto[228:231]	1536	1	-	Covered
bin auto[232:235]	1536	1	-	Covered
bin auto[236:239]	1440	1	-	Covered
bin auto[240:243]	1536	1	-	Covered

bin auto[244:247]	1536	1	-	Covered	
bin auto[248:251]	1501	1	-	Covered	
bin auto[252:255]	1466	1	-	Covered	
Coverpoint address_written	100.00%	100	-	Covered	
covered/total bins:	64	64	-		
missing/total bins:	0	64	-		
% Hit:	100.00%	100	-		
bin auto[0:3]	75986	1	-	Covered	
bin auto[4:7]	7969	1	-	Covered	
bin auto[8:11]	3969	1	-	Covered	
bin auto[12:15]	3969	1	-	Covered	
bin auto[16:19]	1980	1	-	Covered	
bin auto[20:23]	1957	1	-	Covered	
bin auto[24:27]	1959	1	-	Covered	
bin auto[28:31]	1979	1	-	Covered	
bin auto[32:35]	976	1	-	Covered	
bin auto[36:39]	972	1	-	Covered	
bin auto[40:43]	962	1	-	Covered	
bin auto[44:47]	964	1	-	Covered	
bin auto[48:51]	963	1	-	Covered	
bin auto[52:55]	964	1	-	Covered	
bin auto[56:59]	969	1	-	Covered	
bin auto[60:63]	978	1	-	Covered	
bin auto[64:67]	473	1	-	Covered	
bin auto[68:71]	471	1	-	Covered	
bin auto[72:75]	468	1	-	Covered	
bin auto[76:79]	472	1	-	Covered	
bin auto[80:83]	464	1	-	Covered	
bin auto[84:87]	468	1	-	Covered	
bin auto[88:91]	468	1	-	Covered	
bin auto[92:95]	464	1	-	Covered	
bin auto[96:99]	463	1	-	Covered	
bin auto[100:103]	468	1	-	Covered	
bin auto[104:107]	469	1	-	Covered	
bin auto[108:111]	465	1	-	Covered	
bin auto[112:115]	468	1	-	Covered	
bin auto[116:119]	469	1	-	Covered	
bin auto[120:123]	474	1	-	Covered	
bin auto[124:127]	473	1	-	Covered	
bin auto[128:131]	220	1	-	Covered	
bin auto[132:135]	222	1	-	Covered	
bin auto[136:139]	221	1	-	Covered	
bin auto[140:143]	218	1	-	Covered	
bin auto[144:147]	219	1	-	Covered	
bin auto[148:151]	220	1	-	Covered	
bin auto[152:155]	221	1	-	Covered	
bin auto[156:159]	219	1	-	Covered	
bin auto[160:163]	217	1	-	Covered	
bin auto[164:167]	216	1	-	Covered	
bin auto[168:171]	218	1	-	Covered	
bin auto[172:175]	218	1	-	Covered	
bin auto[176:179]	220	1	-	Covered	
bin auto[180:183]	217	1	-	Covered	
bin auto[184:187]	217	1	-	Covered	
bin auto[188:191]	215	1	-	Covered	
bin auto[192:195]	216	1	-	Covered	
bin auto[196:199]	216	1	-	Covered	
bin auto[200:203]	218	1	-	Covered	
bin auto[204:207]	219	1	-	Covered	
bin auto[208:211]	215	1	-	Covered	
bin auto[212:215]	222	1	-	Covered	
bin auto[216:219]	219	1	-	Covered	
bin auto[220:223]	216	1	-	Covered	
bin auto[224:227]	216	1	-	Covered	
bin auto[228:231]	221	1	-	Covered	
bin auto[232:235]	217	1	-	Covered	

bin auto[236:239]	221	1	-	Covered
bin auto[240:243]	222	1	-	Covered
bin auto[244:247]	220	1	-	Covered
bin auto[248:251]	222	1	-	Covered
bin auto[252:255]	221	1	-	Covered
Coverpoint address_read	100.00%	100	-	Covered
covered/total bins:	64	64	-	
missing/total bins:	0	64	-	
% Hit:	100.00%	100	-	
bin auto[0:3]	120043	1	-	Covered
bin auto[4:7]	32	1	-	Covered
bin auto[8:11]	32	1	-	Covered
bin auto[12:15]	31	1	-	Covered
bin auto[16:19]	32	1	-	Covered
bin auto[20:23]	32	1	-	Covered
bin auto[24:27]	32	1	-	Covered
bin auto[28:31]	32	1	-	Covered
bin auto[32:35]	32	1	-	Covered
bin auto[36:39]	31	1	-	Covered
bin auto[40:43]	32	1	-	Covered
bin auto[44:47]	31	1	-	Covered
bin auto[48:51]	32	1	-	Covered
bin auto[52:55]	29	1	-	Covered
bin auto[56:59]	32	1	-	Covered
bin auto[60:63]	31	1	-	Covered
bin auto[64:67]	32	1	-	Covered
bin auto[68:71]	30	1	-	Covered
bin auto[72:75]	30	1	-	Covered
bin auto[76:79]	32	1	-	Covered
bin auto[80:83]	31	1	-	Covered
bin auto[84:87]	32	1	-	Covered
bin auto[88:91]	32	1	-	Covered
bin auto[92:95]	32	1	-	Covered
bin auto[96:99]	32	1	-	Covered
bin auto[100:103]	31	1	-	Covered
bin auto[104:107]	32	1	-	Covered
bin auto[108:111]	30	1	-	Covered
bin auto[112:115]	31	1	-	Covered
bin auto[116:119]	31	1	-	Covered
bin auto[120:123]	32	1	-	Covered
bin auto[124:127]	32	1	-	Covered
bin auto[128:131]	31	1	-	Covered
bin auto[132:135]	32	1	-	Covered
bin auto[136:139]	31	1	-	Covered
bin auto[140:143]	31	1	-	Covered
bin auto[144:147]	31	1	-	Covered
bin auto[148:151]	30	1	-	Covered
bin auto[152:155]	31	1	-	Covered
bin auto[156:159]	31	1	-	Covered
bin auto[160:163]	32	1	-	Covered
bin auto[164:167]	32	1	-	Covered
bin auto[168:171]	30	1	-	Covered
bin auto[172:175]	30	1	-	Covered
bin auto[176:179]	32	1	-	Covered
bin auto[180:183]	32	1	-	Covered
bin auto[184:187]	30	1	-	Covered
bin auto[188:191]	31	1	-	Covered
bin auto[192:195]	31	1	-	Covered
bin auto[196:199]	32	1	-	Covered
bin auto[200:203]	32	1	-	Covered
bin auto[204:207]	31	1	-	Covered
bin auto[208:211]	28	1	-	Covered
bin auto[212:215]	31	1	-	Covered
bin auto[216:219]	32	1	-	Covered
bin auto[220:223]	30	1	-	Covered
bin auto[224:227]	31	1	-	Covered

```
    bin auto[228:231]                    31        1        -    Covered
    bin auto[232:235]                    31        1        -    Covered
    bin auto[236:239]                    32        1        -    Covered
    bin auto[240:243]                    30        1        -    Covered
    bin auto[244:247]                    32        1        -    Covered
    bin auto[248:251]                    32        1        -    Covered
    bin auto[252:255]                    31        1        -    Covered
  Coverpoint receive_valid               100.00%   100      -    Covered
    covered/total bins:                  2         2        -
    missing/total bins:                  0         2        -
    % Hit:                               100.00%   100      -
    bin receive_asserted                 8000      1        -    Covered
    bin receive_disable                  114012    1        -    Covered
  Coverpoint send_valid                  100.00%   100      -    Covered
    covered/total bins:                  2         2        -
    missing/total bins:                  0         2        -
    % Hit:                               100.00%   100      -
    bin send_asserted                    2000      1        -    Covered
    bin send_disable                     120012    1        -    Covered
  Cross Writing_address                  100.00%   100      -    Covered
    covered/total bins:                  128       128      -
    missing/total bins:                  0         128      -
    % Hit:                               100.00%   100      -
    Auto, Default and User Defined Bins:
      bin <auto[252:255],receive_disable>    189       1        -    Covered
      bin <auto[248:251],receive_disable>    190       1        -    Covered
      bin <auto[244:247],receive_disable>    188       1        -    Covered
      bin <auto[240:243],receive_disable>    192       1        -    Covered
      bin <auto[236:239],receive_disable>    189       1        -    Covered
      bin <auto[232:235],receive_disable>    186       1        -    Covered
      bin <auto[228:231],receive_disable>    189       1        -    Covered
      bin <auto[224:227],receive_disable>    186       1        -    Covered
      bin <auto[220:223],receive_disable>    185       1        -    Covered
      bin <auto[216:219],receive_disable>    188       1        -    Covered
      bin <auto[212:215],receive_disable>    190       1        -    Covered
      bin <auto[208:211],receive_disable>    185       1        -    Covered
      bin <auto[204:207],receive_disable>    189       1        -    Covered
      bin <auto[200:203],receive_disable>    186       1        -    Covered
      bin <auto[196:199],receive_disable>    184       1        -    Covered
      bin <auto[192:195],receive_disable>    185       1        -    Covered
      bin <auto[188:191],receive_disable>    185       1        -    Covered
      bin <auto[184:187],receive_disable>    187       1        -    Covered
      bin <auto[180:183],receive_disable>    185       1        -    Covered
      bin <auto[176:179],receive_disable>    188       1        -    Covered
      bin <auto[172:175],receive_disable>    188       1        -    Covered
      bin <auto[168:171],receive_disable>    186       1        -    Covered
      bin <auto[164:167],receive_disable>    184       1        -    Covered
      bin <auto[160:163],receive_disable>    186       1        -    Covered
      bin <auto[156:159],receive_disable>    188       1        -    Covered
      bin <auto[152:155],receive_disable>    189       1        -    Covered
      bin <auto[148:151],receive_disable>    191       1        -    Covered
      bin <auto[144:147],receive_disable>    187       1        -    Covered
      bin <auto[140:143],receive_disable>    186       1        -    Covered
      bin <auto[136:139],receive_disable>    190       1        -    Covered
      bin <auto[132:135],receive_disable>    190       1        -    Covered
      bin <auto[128:131],receive_disable>    189       1        -    Covered
      bin <auto[124:127],receive_disable>    443       1        -    Covered
      bin <auto[120:123],receive_disable>    442       1        -    Covered
      bin <auto[116:119],receive_disable>    438       1        -    Covered
      bin <auto[112:115],receive_disable>    437       1        -    Covered
      bin <auto[108:111],receive_disable>    435       1        -    Covered
      bin <auto[104:107],receive_disable>    437       1        -    Covered
      bin <auto[100:103],receive_disable>    437       1        -    Covered
      bin <auto[96:99],receive_disable>      432       1        -    Covered
      bin <auto[92:95],receive_disable>      432       1        -    Covered
      bin <auto[88:91],receive_disable>      437       1        -    Covered
```

bin <auto[84:87],receive_disable>	436	1	-	Covered
bin <auto[80:83],receive_disable>	433	1	-	Covered
bin <auto[76:79],receive_disable>	440	1	-	Covered
bin <auto[72:75],receive_disable>	439	1	-	Covered
bin <auto[68:71],receive_disable>	439	1	-	Covered
bin <auto[64:67],receive_disable>	442	1	-	Covered
bin <auto[60:63],receive_disable>	947	1	-	Covered
bin <auto[56:59],receive_disable>	937	1	-	Covered
bin <auto[52:55],receive_disable>	934	1	-	Covered
bin <auto[48:51],receive_disable>	931	1	-	Covered
bin <auto[44:47],receive_disable>	932	1	-	Covered
bin <auto[40:43],receive_disable>	932	1	-	Covered
bin <auto[36:39],receive_disable>	940	1	-	Covered
bin <auto[32:35],receive_disable>	944	1	-	Covered
bin <auto[28:31],receive_disable>	1947	1	-	Covered
bin <auto[24:27],receive_disable>	1927	1	-	Covered
bin <auto[20:23],receive_disable>	1926	1	-	Covered
bin <auto[16:19],receive_disable>	1948	1	-	Covered
bin <auto[12:15],receive_disable>	3938	1	-	Covered
bin <auto[8:11],receive_disable>	3937	1	-	Covered
bin <auto[4:7],receive_disable>	7938	1	-	Covered
bin <auto[0:3],receive_disable>	69955	1	-	Covered
bin <auto[252:255],receive_asserted>	32	1	-	Covered
bin <auto[248:251],receive_asserted>	32	1	-	Covered
bin <auto[244:247],receive_asserted>	32	1	-	Covered
bin <auto[240:243],receive_asserted>	30	1	-	Covered
bin <auto[236:239],receive_asserted>	32	1	-	Covered
bin <auto[232:235],receive_asserted>	31	1	-	Covered
bin <auto[228:231],receive_asserted>	32	1	-	Covered
bin <auto[224:227],receive_asserted>	30	1	-	Covered
bin <auto[220:223],receive_asserted>	31	1	-	Covered
bin <auto[216:219],receive_asserted>	31	1	-	Covered
bin <auto[212:215],receive_asserted>	32	1	-	Covered
bin <auto[208:211],receive_asserted>	30	1	-	Covered
bin <auto[204:207],receive_asserted>	30	1	-	Covered
bin <auto[200:203],receive_asserted>	32	1	-	Covered
bin <auto[196:199],receive_asserted>	32	1	-	Covered
bin <auto[192:195],receive_asserted>	31	1	-	Covered
bin <auto[188:191],receive_asserted>	30	1	-	Covered
bin <auto[184:187],receive_asserted>	30	1	-	Covered
bin <auto[180:183],receive_asserted>	32	1	-	Covered
bin <auto[176:179],receive_asserted>	32	1	-	Covered
bin <auto[172:175],receive_asserted>	30	1	-	Covered
bin <auto[168:171],receive_asserted>	32	1	-	Covered
bin <auto[164:167],receive_asserted>	32	1	-	Covered
bin <auto[160:163],receive_asserted>	31	1	-	Covered
bin <auto[156:159],receive_asserted>	31	1	-	Covered
bin <auto[152:155],receive_asserted>	32	1	-	Covered
bin <auto[148:151],receive_asserted>	29	1	-	Covered
bin <auto[144:147],receive_asserted>	32	1	-	Covered
bin <auto[140:143],receive_asserted>	32	1	-	Covered
bin <auto[136:139],receive_asserted>	31	1	-	Covered
bin <auto[132:135],receive_asserted>	32	1	-	Covered
bin <auto[128:131],receive_asserted>	31	1	-	Covered
bin <auto[124:127],receive_asserted>	30	1	-	Covered
bin <auto[120:123],receive_asserted>	32	1	-	Covered
bin <auto[116:119],receive_asserted>	31	1	-	Covered
bin <auto[112:115],receive_asserted>	31	1	-	Covered
bin <auto[108:111],receive_asserted>	30	1	-	Covered
bin <auto[104:107],receive_asserted>	32	1	-	Covered
bin <auto[100:103],receive_asserted>	31	1	-	Covered
bin <auto[96:99],receive_asserted>	31	1	-	Covered
bin <auto[92:95],receive_asserted>	32	1	-	Covered
bin <auto[88:91],receive_asserted>	31	1	-	Covered
bin <auto[84:87],receive_asserted>	32	1	-	Covered
bin <auto[80:83],receive_asserted>	31	1	-	Covered

```
        bin <auto[76:79],receive_asserted>          32       1       -    Covered
        bin <auto[72:75],receive_asserted>          29       1       -    Covered
        bin <auto[68:71],receive_asserted>          32       1       -    Covered
        bin <auto[64:67],receive_asserted>          31       1       -    Covered
        bin <auto[60:63],receive_asserted>          31       1       -    Covered
        bin <auto[56:59],receive_asserted>          32       1       -    Covered
        bin <auto[52:55],receive_asserted>          30       1       -    Covered
        bin <auto[48:51],receive_asserted>          32       1       -    Covered
        bin <auto[44:47],receive_asserted>          32       1       -    Covered
        bin <auto[40:43],receive_asserted>          30       1       -    Covered
        bin <auto[36:39],receive_asserted>          32       1       -    Covered
        bin <auto[32:35],receive_asserted>          32       1       -    Covered
        bin <auto[28:31],receive_asserted>          32       1       -    Covered
        bin <auto[24:27],receive_asserted>          32       1       -    Covered
        bin <auto[20:23],receive_asserted>          31       1       -    Covered
        bin <auto[16:19],receive_asserted>          32       1       -    Covered
        bin <auto[12:15],receive_asserted>          31       1       -    Covered
        bin <auto[8:11],receive_asserted>           32       1       -    Covered
        bin <auto[4:7],receive_asserted>            31       1       -    Covered
        bin <auto[0:3],receive_asserted>          6031       1       -    Covered
    Cross Writing_data                      100.00%      100       -    Covered
      covered/total bins:                       128      128       -
      missing/total bins:                         0      128       -
      % Hit:                                100.00%      100       -
      Auto, Default and User Defined Bins:
        bin <auto[252:255],receive_disable>        62       1       -    Covered
        bin <auto[248:251],receive_disable>        63       1       -    Covered
        bin <auto[244:247],receive_disable>        62       1       -    Covered
        bin <auto[240:243],receive_disable>        64       1       -    Covered
        bin <auto[236:239],receive_disable>        64       1       -    Covered
        bin <auto[232:235],receive_disable>        61       1       -    Covered
        bin <auto[228:231],receive_disable>        64       1       -    Covered
        bin <auto[224:227],receive_disable>        64       1       -    Covered
        bin <auto[220:223],receive_disable>        64       1       -    Covered
        bin <auto[216:219],receive_disable>        63       1       -    Covered
        bin <auto[212:215],receive_disable>        63       1       -    Covered
        bin <auto[208:211],receive_disable>        63       1       -    Covered
        bin <auto[204:207],receive_disable>        63       1       -    Covered
        bin <auto[200:203],receive_disable>        63       1       -    Covered
        bin <auto[196:199],receive_disable>        61       1       -    Covered
        bin <auto[192:195],receive_disable>        62       1       -    Covered
        bin <auto[188:191],receive_disable>        60       1       -    Covered
        bin <auto[184:187],receive_disable>        61       1       -    Covered
        bin <auto[180:183],receive_disable>        62       1       -    Covered
        bin <auto[176:179],receive_disable>        64       1       -    Covered
        bin <auto[172:175],receive_disable>        63       1       -    Covered
        bin <auto[168:171],receive_disable>        63       1       -    Covered
        bin <auto[164:167],receive_disable>        61       1       -    Covered
        bin <auto[160:163],receive_disable>        62       1       -    Covered
        bin <auto[156:159],receive_disable>        63       1       -    Covered
        bin <auto[152:155],receive_disable>        63       1       -    Covered
        bin <auto[148:151],receive_disable>        63       1       -    Covered
        bin <auto[144:147],receive_disable>        61       1       -    Covered
        bin <auto[140:143],receive_disable>        62       1       -    Covered
        bin <auto[136:139],receive_disable>        62       1       -    Covered
        bin <auto[132:135],receive_disable>        63       1       -    Covered
        bin <auto[128:131],receive_disable>        61       1       -    Covered
        bin <auto[124:127],receive_disable>        63       1       -    Covered
        bin <auto[120:123],receive_disable>        62       1       -    Covered
        bin <auto[116:119],receive_disable>        63       1       -    Covered
        bin <auto[112:115],receive_disable>        62       1       -    Covered
        bin <auto[108:111],receive_disable>        62       1       -    Covered
        bin <auto[104:107],receive_disable>        59       1       -    Covered
        bin <auto[100:103],receive_disable>        63       1       -    Covered
        bin <auto[96:99],receive_disable>          63       1       -    Covered
        bin <auto[92:95],receive_disable>          61       1       -    Covered
```

bin <auto[88:91],receive_disable>	64	1	-	Covered
bin <auto[84:87],receive_disable>	60	1	-	Covered
bin <auto[80:83],receive_disable>	64	1	-	Covered
bin <auto[76:79],receive_disable>	62	1	-	Covered
bin <auto[72:75],receive_disable>	61	1	-	Covered
bin <auto[68:71],receive_disable>	62	1	-	Covered
bin <auto[64:67],receive_disable>	63	1	-	Covered
bin <auto[60:63],receive_disable>	64	1	-	Covered
bin <auto[56:59],receive_disable>	62	1	-	Covered
bin <auto[52:55],receive_disable>	62	1	-	Covered
bin <auto[48:51],receive_disable>	63	1	-	Covered
bin <auto[44:47],receive_disable>	64	1	-	Covered
bin <auto[40:43],receive_disable>	63	1	-	Covered
bin <auto[36:39],receive_disable>	62	1	-	Covered
bin <auto[32:35],receive_disable>	62	1	-	Covered
bin <auto[28:31],receive_disable>	63	1	-	Covered
bin <auto[24:27],receive_disable>	61	1	-	Covered
bin <auto[20:23],receive_disable>	63	1	-	Covered
bin <auto[16:19],receive_disable>	63	1	-	Covered
bin <auto[12:15],receive_disable>	64	1	-	Covered
bin <auto[8:11],receive_disable>	64	1	-	Covered
bin <auto[4:7],receive_disable>	63	1	-	Covered
bin <auto[0:3],receive_disable>	110075	1	-	Covered
bin <auto[252:255],receive_asserted>	32	1	-	Covered
bin <auto[248:251],receive_asserted>	32	1	-	Covered
bin <auto[244:247],receive_asserted>	32	1	-	Covered
bin <auto[240:243],receive_asserted>	32	1	-	Covered
bin <auto[236:239],receive_asserted>	31	1	-	Covered
bin <auto[232:235],receive_asserted>	32	1	-	Covered
bin <auto[228:231],receive_asserted>	32	1	-	Covered
bin <auto[224:227],receive_asserted>	32	1	-	Covered
bin <auto[220:223],receive_asserted>	31	1	-	Covered
bin <auto[216:219],receive_asserted>	31	1	-	Covered
bin <auto[212:215],receive_asserted>	29	1	-	Covered
bin <auto[208:211],receive_asserted>	31	1	-	Covered
bin <auto[204:207],receive_asserted>	32	1	-	Covered
bin <auto[200:203],receive_asserted>	31	1	-	Covered
bin <auto[196:199],receive_asserted>	32	1	-	Covered
bin <auto[192:195],receive_asserted>	31	1	-	Covered
bin <auto[188:191],receive_asserted>	32	1	-	Covered
bin <auto[184:187],receive_asserted>	32	1	-	Covered
bin <auto[180:183],receive_asserted>	31	1	-	Covered
bin <auto[176:179],receive_asserted>	31	1	-	Covered
bin <auto[172:175],receive_asserted>	32	1	-	Covered
bin <auto[168:171],receive_asserted>	32	1	-	Covered
bin <auto[164:167],receive_asserted>	31	1	-	Covered
bin <auto[160:163],receive_asserted>	31	1	-	Covered
bin <auto[156:159],receive_asserted>	32	1	-	Covered
bin <auto[152:155],receive_asserted>	31	1	-	Covered
bin <auto[148:151],receive_asserted>	32	1	-	Covered
bin <auto[144:147],receive_asserted>	30	1	-	Covered
bin <auto[140:143],receive_asserted>	29	1	-	Covered
bin <auto[136:139],receive_asserted>	31	1	-	Covered
bin <auto[132:135],receive_asserted>	31	1	-	Covered
bin <auto[128:131],receive_asserted>	30	1	-	Covered
bin <auto[124:127],receive_asserted>	32	1	-	Covered
bin <auto[120:123],receive_asserted>	28	1	-	Covered
bin <auto[116:119],receive_asserted>	31	1	-	Covered
bin <auto[112:115],receive_asserted>	31	1	-	Covered
bin <auto[108:111],receive_asserted>	32	1	-	Covered
bin <auto[104:107],receive_asserted>	32	1	-	Covered
bin <auto[100:103],receive_asserted>	32	1	-	Covered
bin <auto[96:99],receive_asserted>	30	1	-	Covered
bin <auto[92:95],receive_asserted>	31	1	-	Covered
bin <auto[88:91],receive_asserted>	32	1	-	Covered
bin <auto[84:87],receive_asserted>	31	1	-	Covered

```
        bin <auto[80:83],receive_asserted>          31       1       -   Covered
        bin <auto[76:79],receive_asserted>          30       1       -   Covered
        bin <auto[72:75],receive_asserted>          31       1       -   Covered
        bin <auto[68:71],receive_asserted>          32       1       -   Covered
        bin <auto[64:67],receive_asserted>          29       1       -   Covered
        bin <auto[60:63],receive_asserted>          31       1       -   Covered
        bin <auto[56:59],receive_asserted>          31       1       -   Covered
        bin <auto[52:55],receive_asserted>          32       1       -   Covered
        bin <auto[48:51],receive_asserted>          32       1       -   Covered
        bin <auto[44:47],receive_asserted>          32       1       -   Covered
        bin <auto[40:43],receive_asserted>          32       1       -   Covered
        bin <auto[36:39],receive_asserted>          32       1       -   Covered
        bin <auto[32:35],receive_asserted>          31       1       -   Covered
        bin <auto[28:31],receive_asserted>          30       1       -   Covered
        bin <auto[24:27],receive_asserted>          32       1       -   Covered
        bin <auto[20:23],receive_asserted>          32       1       -   Covered
        bin <auto[16:19],receive_asserted>          32       1       -   Covered
        bin <auto[12:15],receive_asserted>          31       1       -   Covered
        bin <auto[8:11],receive_asserted>           31       1       -   Covered
        bin <auto[4:7],receive_asserted>            31       1       -   Covered
        bin <auto[0:3],receive_asserted>            6032     1       -   Covered
    Cross reading_address                   100.00%      100       -   Covered
      covered/total bins:                   64           64        -
      missing/total bins:                   0            64        -
      % Hit:                                100.00%      100       -
      Auto, Default and User Defined Bins:
        bin <auto[252:255],receive_asserted>        31       1       -   Covered
        bin <auto[124:127],receive_asserted>        32       1       -   Covered
        bin <auto[188:191],receive_asserted>        31       1       -   Covered
        bin <auto[60:63],receive_asserted>          31       1       -   Covered
        bin <auto[220:223],receive_asserted>        30       1       -   Covered
        bin <auto[92:95],receive_asserted>          32       1       -   Covered
        bin <auto[156:159],receive_asserted>        31       1       -   Covered
        bin <auto[28:31],receive_asserted>          32       1       -   Covered
        bin <auto[236:239],receive_asserted>        32       1       -   Covered
        bin <auto[108:111],receive_asserted>        30       1       -   Covered
        bin <auto[172:175],receive_asserted>        30       1       -   Covered
        bin <auto[44:47],receive_asserted>          31       1       -   Covered
        bin <auto[204:207],receive_asserted>        31       1       -   Covered
        bin <auto[76:79],receive_asserted>          32       1       -   Covered
        bin <auto[140:143],receive_asserted>        31       1       -   Covered
        bin <auto[12:15],receive_asserted>          31       1       -   Covered
        bin <auto[244:247],receive_asserted>        32       1       -   Covered
        bin <auto[116:119],receive_asserted>        31       1       -   Covered
        bin <auto[180:183],receive_asserted>        32       1       -   Covered
        bin <auto[52:55],receive_asserted>          29       1       -   Covered
        bin <auto[212:215],receive_asserted>        31       1       -   Covered
        bin <auto[84:87],receive_asserted>          32       1       -   Covered
        bin <auto[148:151],receive_asserted>        30       1       -   Covered
        bin <auto[20:23],receive_asserted>          32       1       -   Covered
        bin <auto[228:231],receive_asserted>        31       1       -   Covered
        bin <auto[100:103],receive_asserted>        31       1       -   Covered
        bin <auto[164:167],receive_asserted>        32       1       -   Covered
        bin <auto[36:39],receive_asserted>          31       1       -   Covered
        bin <auto[196:199],receive_asserted>        32       1       -   Covered
        bin <auto[68:71],receive_asserted>          30       1       -   Covered
        bin <auto[132:135],receive_asserted>        32       1       -   Covered
        bin <auto[4:7],receive_asserted>            32       1       -   Covered
        bin <auto[248:251],receive_asserted>        32       1       -   Covered
        bin <auto[120:123],receive_asserted>        32       1       -   Covered
        bin <auto[184:187],receive_asserted>        30       1       -   Covered
        bin <auto[56:59],receive_asserted>          32       1       -   Covered
        bin <auto[216:219],receive_asserted>        32       1       -   Covered
        bin <auto[88:91],receive_asserted>          32       1       -   Covered
        bin <auto[152:155],receive_asserted>        31       1       -   Covered
        bin <auto[24:27],receive_asserted>          32       1       -   Covered
```

```
        bin <auto[232:235],receive_asserted>          31       1       -    Covered
        bin <auto[104:107],receive_asserted>          32       1       -    Covered
        bin <auto[168:171],receive_asserted>          30       1       -    Covered
        bin <auto[40:43],receive_asserted>            32       1       -    Covered
        bin <auto[200:203],receive_asserted>          32       1       -    Covered
        bin <auto[72:75],receive_asserted>            30       1       -    Covered
        bin <auto[136:139],receive_asserted>          31       1       -    Covered
        bin <auto[8:11],receive_asserted>             32       1       -    Covered
        bin <auto[240:243],receive_asserted>          30       1       -    Covered
        bin <auto[112:115],receive_asserted>          31       1       -    Covered
        bin <auto[176:179],receive_asserted>          32       1       -    Covered
        bin <auto[48:51],receive_asserted>            32       1       -    Covered
        bin <auto[208:211],receive_asserted>          28       1       -    Covered
        bin <auto[80:83],receive_asserted>            31       1       -    Covered
        bin <auto[144:147],receive_asserted>          31       1       -    Covered
        bin <auto[16:19],receive_asserted>            32       1       -    Covered
        bin <auto[224:227],receive_asserted>          31       1       -    Covered
        bin <auto[96:99],receive_asserted>            32       1       -    Covered
        bin <auto[160:163],receive_asserted>          32       1       -    Covered
        bin <auto[32:35],receive_asserted>            32       1       -    Covered
        bin <auto[192:195],receive_asserted>          31       1       -    Covered
        bin <auto[64:67],receive_asserted>            32       1       -    Covered
        bin <auto[128:131],receive_asserted>          31       1       -    Covered
        bin <auto[0:3],receive_asserted>            6031       1       -    Covered
      Illegal and Ignore Bins:
        ignore_bin ignore_bin1                    114012                 -    Occurred
    Cross reading_data                            100.00%     100       -    Covered
      covered/total bins:                             64      64       -
      missing/total bins:                             0       64       -
      % Hit:                                    100.00%     100       -
      Auto, Default and User Defined Bins:
        bin <auto[252:255],receive_asserted>          92       1       -    Covered
        bin <auto[124:127],receive_asserted>          96       1       -    Covered
        bin <auto[188:191],receive_asserted>          96       1       -    Covered
        bin <auto[60:63],receive_asserted>            86       1       -    Covered
        bin <auto[220:223],receive_asserted>          94       1       -    Covered
        bin <auto[92:95],receive_asserted>            96       1       -    Covered
        bin <auto[156:159],receive_asserted>          96       1       -    Covered
        bin <auto[28:31],receive_asserted>            90       1       -    Covered
        bin <auto[236:239],receive_asserted>          90       1       -    Covered
        bin <auto[108:111],receive_asserted>          94       1       -    Covered
        bin <auto[172:175],receive_asserted>          94       1       -    Covered
        bin <auto[44:47],receive_asserted>            96       1       -    Covered
        bin <auto[204:207],receive_asserted>          90       1       -    Covered
        bin <auto[76:79],receive_asserted>            84       1       -    Covered
        bin <auto[140:143],receive_asserted>          84       1       -    Covered
        bin <auto[12:15],receive_asserted>            96       1       -    Covered
        bin <auto[244:247],receive_asserted>          96       1       -    Covered
        bin <auto[116:119],receive_asserted>          88       1       -    Covered
        bin <auto[180:183],receive_asserted>          90       1       -    Covered
        bin <auto[52:55],receive_asserted>            96       1       -    Covered
        bin <auto[212:215],receive_asserted>          84       1       -    Covered
        bin <auto[84:87],receive_asserted>            96       1       -    Covered
        bin <auto[148:151],receive_asserted>          96       1       -    Covered
        bin <auto[20:23],receive_asserted>            96       1       -    Covered
        bin <auto[228:231],receive_asserted>          96       1       -    Covered
        bin <auto[100:103],receive_asserted>          96       1       -    Covered
        bin <auto[164:167],receive_asserted>         102       1       -    Covered
        bin <auto[36:39],receive_asserted>            94       1       -    Covered
        bin <auto[196:199],receive_asserted>          96       1       -    Covered
        bin <auto[68:71],receive_asserted>            94       1       -    Covered
        bin <auto[132:135],receive_asserted>          92       1       -    Covered
        bin <auto[4:7],receive_asserted>              86       1       -    Covered
        bin <auto[248:251],receive_asserted>          94       1       -    Covered
        bin <auto[120:123],receive_asserted>          92       1       -    Covered
        bin <auto[184:187],receive_asserted>          94       1       -    Covered
```

```
        bin <auto[56:59],receive_asserted>          92       1       -    Covered
        bin <auto[216:219],receive_asserted>        88       1       -    Covered
        bin <auto[88:91],receive_asserted>          96       1       -    Covered
        bin <auto[152:155],receive_asserted>        84       1       -    Covered
        bin <auto[24:27],receive_asserted>          96       1       -    Covered
        bin <auto[232:235],receive_asserted>        96       1       -    Covered
        bin <auto[104:107],receive_asserted>        96       1       -    Covered
        bin <auto[168:171],receive_asserted>        96       1       -    Covered
        bin <auto[40:43],receive_asserted>          96       1       -    Covered
        bin <auto[200:203],receive_asserted>        102      1       -    Covered
        bin <auto[72:75],receive_asserted>          98       1       -    Covered
        bin <auto[136:139],receive_asserted>        104      1       -    Covered
        bin <auto[8:11],receive_asserted>           92       1       -    Covered
        bin <auto[240:243],receive_asserted>        96       1       -    Covered
        bin <auto[112:115],receive_asserted>        96       1       -    Covered
        bin <auto[176:179],receive_asserted>        96       1       -    Covered
        bin <auto[48:51],receive_asserted>          96       1       -    Covered
        bin <auto[208:211],receive_asserted>        96       1       -    Covered
        bin <auto[80:83],receive_asserted>          96       1       -    Covered
        bin <auto[144:147],receive_asserted>        90       1       -    Covered
        bin <auto[16:19],receive_asserted>          96       1       -    Covered
        bin <auto[224:227],receive_asserted>        96       1       -    Covered
        bin <auto[96:99],receive_asserted>          80       1       -    Covered
        bin <auto[160:163],receive_asserted>        92       1       -    Covered
        bin <auto[32:35],receive_asserted>          92       1       -    Covered
        bin <auto[192:195],receive_asserted>        100      1       -    Covered
        bin <auto[64:67],receive_asserted>          80       1       -    Covered
        bin <auto[128:131],receive_asserted>        92       1       -    Covered
        bin <auto[0:3],receive_asserted>            2118     1       -    Covered
      Illegal and Ignore Bins:
        ignore_bin ignore_bin1                      114012               -    Occurred
TYPE /SPI_coverage_pkg/SPI_coverage/SPI_Wrapper     100.00%  100     -    Covered
  covered/total bins:                               522      522     -
  missing/total bins:                               0        522     -
  % Hit:                                            100.00%  100     -
  Coverpoint reset                                  100.00%  100     -    Covered
    covered/total bins:                             2        2       -
    missing/total bins:                             0        2       -
    % Hit:                                          100.00%  100     -
  Coverpoint Address_write                          100.00%  100     -    Covered
    covered/total bins:                             64       64      -
    missing/total bins:                             0        64      -
    % Hit:                                          100.00%  100     -
  Coverpoint Data_write                             100.00%  100     -    Covered
    covered/total bins:                             64       64      -
    missing/total bins:                             0        64      -
    % Hit:                                          100.00%  100     -
  Coverpoint Data_read                              100.00%  100     -    Covered
    covered/total bins:                             64       64      -
    missing/total bins:                             0        64      -
    % Hit:                                          100.00%  100     -
  Coverpoint Address_read                           100.00%  100     -    Covered
    covered/total bins:                             64       64      -
    missing/total bins:                             0        64      -
    % Hit:                                          100.00%  100     -
  Coverpoint Send_Address_wr                        100.00%  100     -    Covered
    covered/total bins:                             1        1       -
    missing/total bins:                             0        1       -
    % Hit:                                          100.00%  100     -
  Coverpoint Send_Address_rd                        100.00%  100     -    Covered
    covered/total bins:                             1        1       -
    missing/total bins:                             0        1       -
    % Hit:                                          100.00%  100     -
  Coverpoint send_Data_wr                           100.00%  100     -    Covered
    covered/total bins:                             1        1       -
    missing/total bins:                             0        1       -
```

```
    % Hit:                          100.00%      100        -
  Coverpoint Recieving_Data_rd                   100.00%      100        -    Covered
    covered/total bins:                    1        1        -
    missing/total bins:                    0        1        -
    % Hit:                          100.00%      100        -
  Coverpoint Sending_order_Read_data             100.00%      100        -    Covered
    covered/total bins:                    1        1        -
    missing/total bins:                    0        1        -
    % Hit:                          100.00%      100        -
  Coverpoint Starting_Communication              100.00%      100        -    Covered
    covered/total bins:                    3        3        -
    missing/total bins:                    0        3        -
    % Hit:                          100.00%      100        -
  Cross Actualiy_sending_addr_wr                 100.00%      100        -    Covered
    covered/total bins:                   64       64        -
    missing/total bins:                    0       64        -
    % Hit:                          100.00%      100        -
  Cross Actualiy_sending_data_wr                 100.00%      100        -    Covered
    covered/total bins:                   64       64        -
    missing/total bins:                    0       64        -
    % Hit:                          100.00%      100        -
  Cross Actualiy_sending_addr_rd                 100.00%      100        -    Covered
    covered/total bins:                   64       64        -
    missing/total bins:                    0       64        -
    % Hit:                          100.00%      100        -
  Cross Actualiy_recieving_data                  100.00%      100        -    Covered
    covered/total bins:                   64       64        -
    missing/total bins:                    0       64        -
    % Hit:                          100.00%      100        -
Covergroup instance \/SPI_coverage_pkg::SPI_coverage::SPI_Wrapper
                                   100.00%      100        -    Covered
  covered/total bins:                     522      522        -
  missing/total bins:                       0      522        -
  % Hit:                          100.00%      100        -
  Coverpoint reset                          100.00%      100        -    Covered
    covered/total bins:                     2        2        -
    missing/total bins:                     0        2        -
    % Hit:                          100.00%      100        -
    bin reset_asserted                     12        1        -    Covered
    bin reset_disable                  122000        1        -    Covered
  Coverpoint Address_write                  100.00%      100        -    Covered
    covered/total bins:                    64       64        -
    missing/total bins:                     0       64        -
    % Hit:                          100.00%      100        -
    bin auto[0:3]                      121028        1        -    Covered
    bin auto[4:7]                          16        1        -    Covered
    bin auto[8:11]                         16        1        -    Covered
    bin auto[12:15]                        15        1        -    Covered
    bin auto[16:19]                        16        1        -    Covered
    bin auto[20:23]                        16        1        -    Covered
    bin auto[24:27]                        16        1        -    Covered
    bin auto[28:31]                        16        1        -    Covered
    bin auto[32:35]                        16        1        -    Covered
    bin auto[36:39]                        16        1        -    Covered
    bin auto[40:43]                        16        1        -    Covered
    bin auto[44:47]                        16        1        -    Covered
    bin auto[48:51]                        16        1        -    Covered
    bin auto[52:55]                        14        1        -    Covered
    bin auto[56:59]                        16        1        -    Covered
    bin auto[60:63]                        15        1        -    Covered
    bin auto[64:67]                        16        1        -    Covered
    bin auto[68:71]                        16        1        -    Covered
    bin auto[72:75]                        15        1        -    Covered
    bin auto[76:79]                        16        1        -    Covered
    bin auto[80:83]                        15        1        -    Covered
    bin auto[84:87]                        16        1        -    Covered
```

bin auto[88:91]	16	1	-	Covered
bin auto[92:95]	16	1	-	Covered
bin auto[96:99]	16	1	-	Covered
bin auto[100:103]	15	1	-	Covered
bin auto[104:107]	16	1	-	Covered
bin auto[108:111]	16	1	-	Covered
bin auto[112:115]	15	1	-	Covered
bin auto[116:119]	15	1	-	Covered
bin auto[120:123]	16	1	-	Covered
bin auto[124:127]	16	1	-	Covered
bin auto[128:131]	15	1	-	Covered
bin auto[132:135]	16	1	-	Covered
bin auto[136:139]	15	1	-	Covered
bin auto[140:143]	16	1	-	Covered
bin auto[144:147]	16	1	-	Covered
bin auto[148:151]	16	1	-	Covered
bin auto[152:155]	16	1	-	Covered
bin auto[156:159]	15	1	-	Covered
bin auto[160:163]	16	1	-	Covered
bin auto[164:167]	16	1	-	Covered
bin auto[168:171]	16	1	-	Covered
bin auto[172:175]	14	1	-	Covered
bin auto[176:179]	16	1	-	Covered
bin auto[180:183]	16	1	-	Covered
bin auto[184:187]	14	1	-	Covered
bin auto[188:191]	15	1	-	Covered
bin auto[192:195]	15	1	-	Covered
bin auto[196:199]	16	1	-	Covered
bin auto[200:203]	16	1	-	Covered
bin auto[204:207]	15	1	-	Covered
bin auto[208:211]	14	1	-	Covered
bin auto[212:215]	16	1	-	Covered
bin auto[216:219]	16	1	-	Covered
bin auto[220:223]	15	1	-	Covered
bin auto[224:227]	15	1	-	Covered
bin auto[228:231]	16	1	-	Covered
bin auto[232:235]	16	1	-	Covered
bin auto[236:239]	16	1	-	Covered
bin auto[240:243]	15	1	-	Covered
bin auto[244:247]	16	1	-	Covered
bin auto[248:251]	16	1	-	Covered
bin auto[252:255]	16	1	-	Covered
Coverpoint Data_write	100.00%	100	-	Covered
covered/total bins:	64	64	-	
missing/total bins:	0	64	-	
% Hit:	100.00%	100	-	
bin auto[0:3]	121028	1	-	Covered
bin auto[4:7]	16	1	-	Covered
bin auto[8:11]	15	1	-	Covered
bin auto[12:15]	16	1	-	Covered
bin auto[16:19]	16	1	-	Covered
bin auto[20:23]	16	1	-	Covered
bin auto[24:27]	16	1	-	Covered
bin auto[28:31]	15	1	-	Covered
bin auto[32:35]	15	1	-	Covered
bin auto[36:39]	16	1	-	Covered
bin auto[40:43]	16	1	-	Covered
bin auto[44:47]	16	1	-	Covered
bin auto[48:51]	16	1	-	Covered
bin auto[52:55]	16	1	-	Covered
bin auto[56:59]	16	1	-	Covered
bin auto[60:63]	15	1	-	Covered
bin auto[64:67]	14	1	-	Covered
bin auto[68:71]	16	1	-	Covered
bin auto[72:75]	15	1	-	Covered
bin auto[76:79]	15	1	-	Covered

bin auto[80:83]	16	1	-	Covered
bin auto[84:87]	16	1	-	Covered
bin auto[88:91]	16	1	-	Covered
bin auto[92:95]	16	1	-	Covered
bin auto[96:99]	16	1	-	Covered
bin auto[100:103]	16	1	-	Covered
bin auto[104:107]	16	1	-	Covered
bin auto[108:111]	16	1	-	Covered
bin auto[112:115]	16	1	-	Covered
bin auto[116:119]	15	1	-	Covered
bin auto[120:123]	13	1	-	Covered
bin auto[124:127]	16	1	-	Covered
bin auto[128:131]	15	1	-	Covered
bin auto[132:135]	15	1	-	Covered
bin auto[136:139]	16	1	-	Covered
bin auto[140:143]	14	1	-	Covered
bin auto[144:147]	15	1	-	Covered
bin auto[148:151]	16	1	-	Covered
bin auto[152:155]	15	1	-	Covered
bin auto[156:159]	16	1	-	Covered
bin auto[160:163]	15	1	-	Covered
bin auto[164:167]	16	1	-	Covered
bin auto[168:171]	16	1	-	Covered
bin auto[172:175]	16	1	-	Covered
bin auto[176:179]	16	1	-	Covered
bin auto[180:183]	15	1	-	Covered
bin auto[184:187]	16	1	-	Covered
bin auto[188:191]	16	1	-	Covered
bin auto[192:195]	16	1	-	Covered
bin auto[196:199]	16	1	-	Covered
bin auto[200:203]	16	1	-	Covered
bin auto[204:207]	16	1	-	Covered
bin auto[208:211]	16	1	-	Covered
bin auto[212:215]	13	1	-	Covered
bin auto[216:219]	16	1	-	Covered
bin auto[220:223]	16	1	-	Covered
bin auto[224:227]	16	1	-	Covered
bin auto[228:231]	16	1	-	Covered
bin auto[232:235]	16	1	-	Covered
bin auto[236:239]	15	1	-	Covered
bin auto[240:243]	16	1	-	Covered
bin auto[244:247]	16	1	-	Covered
bin auto[248:251]	16	1	-	Covered
bin auto[252:255]	16	1	-	Covered
Coverpoint Data_read	100.00%	100	-	Covered
covered/total bins:	64	64	-	
missing/total bins:	0	64	-	
% Hit:	100.00%	100	-	
bin auto[0:3]	121028	1	-	Covered
bin auto[4:7]	16	1	-	Covered
bin auto[8:11]	15	1	-	Covered
bin auto[12:15]	16	1	-	Covered
bin auto[16:19]	16	1	-	Covered
bin auto[20:23]	16	1	-	Covered
bin auto[24:27]	16	1	-	Covered
bin auto[28:31]	15	1	-	Covered
bin auto[32:35]	15	1	-	Covered
bin auto[36:39]	16	1	-	Covered
bin auto[40:43]	16	1	-	Covered
bin auto[44:47]	16	1	-	Covered
bin auto[48:51]	16	1	-	Covered
bin auto[52:55]	16	1	-	Covered
bin auto[56:59]	16	1	-	Covered
bin auto[60:63]	15	1	-	Covered
bin auto[64:67]	14	1	-	Covered
bin auto[68:71]	16	1	-	Covered

bin auto[72:75]	15	1	-	Covered
bin auto[76:79]	15	1	-	Covered
bin auto[80:83]	16	1	-	Covered
bin auto[84:87]	16	1	-	Covered
bin auto[88:91]	16	1	-	Covered
bin auto[92:95]	16	1	-	Covered
bin auto[96:99]	16	1	-	Covered
bin auto[100:103]	16	1	-	Covered
bin auto[104:107]	16	1	-	Covered
bin auto[108:111]	16	1	-	Covered
bin auto[112:115]	16	1	-	Covered
bin auto[116:119]	15	1	-	Covered
bin auto[120:123]	13	1	-	Covered
bin auto[124:127]	16	1	-	Covered
bin auto[128:131]	15	1	-	Covered
bin auto[132:135]	15	1	-	Covered
bin auto[136:139]	16	1	-	Covered
bin auto[140:143]	14	1	-	Covered
bin auto[144:147]	15	1	-	Covered
bin auto[148:151]	16	1	-	Covered
bin auto[152:155]	15	1	-	Covered
bin auto[156:159]	16	1	-	Covered
bin auto[160:163]	15	1	-	Covered
bin auto[164:167]	16	1	-	Covered
bin auto[168:171]	16	1	-	Covered
bin auto[172:175]	16	1	-	Covered
bin auto[176:179]	16	1	-	Covered
bin auto[180:183]	15	1	-	Covered
bin auto[184:187]	16	1	-	Covered
bin auto[188:191]	16	1	-	Covered
bin auto[192:195]	16	1	-	Covered
bin auto[196:199]	16	1	-	Covered
bin auto[200:203]	16	1	-	Covered
bin auto[204:207]	16	1	-	Covered
bin auto[208:211]	16	1	-	Covered
bin auto[212:215]	13	1	-	Covered
bin auto[216:219]	16	1	-	Covered
bin auto[220:223]	16	1	-	Covered
bin auto[224:227]	16	1	-	Covered
bin auto[228:231]	16	1	-	Covered
bin auto[232:235]	16	1	-	Covered
bin auto[236:239]	15	1	-	Covered
bin auto[240:243]	16	1	-	Covered
bin auto[244:247]	16	1	-	Covered
bin auto[248:251]	16	1	-	Covered
bin auto[252:255]	16	1	-	Covered
Coverpoint Address_read	100.00%	100	-	Covered
covered/total bins:	64	64	-	
missing/total bins:	0	64	-	
% Hit:	100.00%	100	-	
bin auto[0:3]	121028	1	-	Covered
bin auto[4:7]	16	1	-	Covered
bin auto[8:11]	16	1	-	Covered
bin auto[12:15]	15	1	-	Covered
bin auto[16:19]	16	1	-	Covered
bin auto[20:23]	16	1	-	Covered
bin auto[24:27]	16	1	-	Covered
bin auto[28:31]	16	1	-	Covered
bin auto[32:35]	16	1	-	Covered
bin auto[36:39]	16	1	-	Covered
bin auto[40:43]	16	1	-	Covered
bin auto[44:47]	16	1	-	Covered
bin auto[48:51]	16	1	-	Covered
bin auto[52:55]	14	1	-	Covered
bin auto[56:59]	16	1	-	Covered
bin auto[60:63]	15	1	-	Covered

```
    bin auto[64:67]                          16        1        -    Covered
    bin auto[68:71]                          16        1        -    Covered
    bin auto[72:75]                          15        1        -    Covered
    bin auto[76:79]                          16        1        -    Covered
    bin auto[80:83]                          15        1        -    Covered
    bin auto[84:87]                          16        1        -    Covered
    bin auto[88:91]                          16        1        -    Covered
    bin auto[92:95]                          16        1        -    Covered
    bin auto[96:99]                          16        1        -    Covered
    bin auto[100:103]                        15        1        -    Covered
    bin auto[104:107]                        16        1        -    Covered
    bin auto[108:111]                        16        1        -    Covered
    bin auto[112:115]                        15        1        -    Covered
    bin auto[116:119]                        15        1        -    Covered
    bin auto[120:123]                        16        1        -    Covered
    bin auto[124:127]                        16        1        -    Covered
    bin auto[128:131]                        15        1        -    Covered
    bin auto[132:135]                        16        1        -    Covered
    bin auto[136:139]                        15        1        -    Covered
    bin auto[140:143]                        16        1        -    Covered
    bin auto[144:147]                        16        1        -    Covered
    bin auto[148:151]                        16        1        -    Covered
    bin auto[152:155]                        16        1        -    Covered
    bin auto[156:159]                        15        1        -    Covered
    bin auto[160:163]                        16        1        -    Covered
    bin auto[164:167]                        16        1        -    Covered
    bin auto[168:171]                        16        1        -    Covered
    bin auto[172:175]                        14        1        -    Covered
    bin auto[176:179]                        16        1        -    Covered
    bin auto[180:183]                        16        1        -    Covered
    bin auto[184:187]                        14        1        -    Covered
    bin auto[188:191]                        15        1        -    Covered
    bin auto[192:195]                        15        1        -    Covered
    bin auto[196:199]                        16        1        -    Covered
    bin auto[200:203]                        16        1        -    Covered
    bin auto[204:207]                        15        1        -    Covered
    bin auto[208:211]                        14        1        -    Covered
    bin auto[212:215]                        16        1        -    Covered
    bin auto[216:219]                        16        1        -    Covered
    bin auto[220:223]                        15        1        -    Covered
    bin auto[224:227]                        15        1        -    Covered
    bin auto[228:231]                        16        1        -    Covered
    bin auto[232:235]                        16        1        -    Covered
    bin auto[236:239]                        16        1        -    Covered
    bin auto[240:243]                        15        1        -    Covered
    bin auto[244:247]                        16        1        -    Covered
    bin auto[248:251]                        16        1        -    Covered
    bin auto[252:255]                        16        1        -    Covered
  Coverpoint Send_Address_wr                 100.00%   100      -    Covered
    covered/total bins:                      1         1        -
    missing/total bins:                      0         1        -
    % Hit:                                   100.00%   100      -
    bin writing_add                          11000     1        -    Covered
  Coverpoint Send_Address_rd                 100.00%   100      -    Covered
    covered/total bins:                      1         1        -
    missing/total bins:                      0         1        -
    % Hit:                                   100.00%   100      -
    bin reading_add                          11000     1        -    Covered
  Coverpoint send_Data_wr                    100.00%   100      -    Covered
    covered/total bins:                      1         1        -
    missing/total bins:                      0         1        -
    % Hit:                                   100.00%   100      -
    bin writing_data                         11000     1        -    Covered
  Coverpoint Recieving_Data_rd               100.00%   100      -    Covered
    covered/total bins:                      1         1        -
    missing/total bins:                      0         1        -
```

```
    % Hit:                    100.00%      100        -
    bin reading_data          8000         1        -    Covered
  Coverpoint Sending_order_Read_data        100.00%      100        -    Covered
    covered/total bins:       1            1        -
    missing/total bins:       0            1        -
    % Hit:                    100.00%      100        -
    bin order_reading_data    11000        1        -    Covered
  Coverpoint Starting_Communication         100.00%      100        -    Covered
    covered/total bins:       3            3        -
    missing/total bins:       0            3        -
    % Hit:                    100.00%      100        -
    bin Start                 114000       1        -    Covered
    bin End                   8012         1        -    Covered
    bin transaction_back      7988         1        -    Covered
  Cross Actualiy_sending_addr_wr            100.00%      100        -    Covered
    covered/total bins:       64           64       -
    missing/total bins:       0            64       -
    % Hit:                    100.00%      100        -
    Auto, Default and User Defined Bins:
      bin <writing_add,auto[252:255]>       16           1        -    Covered
      bin <writing_add,auto[248:251]>       16           1        -    Covered
      bin <writing_add,auto[244:247]>       16           1        -    Covered
      bin <writing_add,auto[240:243]>       15           1        -    Covered
      bin <writing_add,auto[236:239]>       16           1        -    Covered
      bin <writing_add,auto[232:235]>       16           1        -    Covered
      bin <writing_add,auto[228:231]>       16           1        -    Covered
      bin <writing_add,auto[224:227]>       15           1        -    Covered
      bin <writing_add,auto[220:223]>       15           1        -    Covered
      bin <writing_add,auto[216:219]>       16           1        -    Covered
      bin <writing_add,auto[212:215]>       16           1        -    Covered
      bin <writing_add,auto[208:211]>       14           1        -    Covered
      bin <writing_add,auto[204:207]>       15           1        -    Covered
      bin <writing_add,auto[200:203]>       16           1        -    Covered
      bin <writing_add,auto[196:199]>       16           1        -    Covered
      bin <writing_add,auto[192:195]>       15           1        -    Covered
      bin <writing_add,auto[188:191]>       15           1        -    Covered
      bin <writing_add,auto[184:187]>       14           1        -    Covered
      bin <writing_add,auto[180:183]>       16           1        -    Covered
      bin <writing_add,auto[176:179]>       16           1        -    Covered
      bin <writing_add,auto[172:175]>       14           1        -    Covered
      bin <writing_add,auto[168:171]>       16           1        -    Covered
      bin <writing_add,auto[164:167]>       16           1        -    Covered
      bin <writing_add,auto[160:163]>       16           1        -    Covered
      bin <writing_add,auto[156:159]>       15           1        -    Covered
      bin <writing_add,auto[152:155]>       16           1        -    Covered
      bin <writing_add,auto[148:151]>       16           1        -    Covered
      bin <writing_add,auto[144:147]>       16           1        -    Covered
      bin <writing_add,auto[140:143]>       16           1        -    Covered
      bin <writing_add,auto[136:139]>       15           1        -    Covered
      bin <writing_add,auto[132:135]>       16           1        -    Covered
      bin <writing_add,auto[128:131]>       15           1        -    Covered
      bin <writing_add,auto[124:127]>       16           1        -    Covered
      bin <writing_add,auto[120:123]>       16           1        -    Covered
      bin <writing_add,auto[116:119]>       15           1        -    Covered
      bin <writing_add,auto[112:115]>       15           1        -    Covered
      bin <writing_add,auto[108:111]>       16           1        -    Covered
      bin <writing_add,auto[104:107]>       16           1        -    Covered
      bin <writing_add,auto[100:103]>       15           1        -    Covered
      bin <writing_add,auto[96:99]>         16           1        -    Covered
      bin <writing_add,auto[92:95]>         16           1        -    Covered
      bin <writing_add,auto[88:91]>         16           1        -    Covered
      bin <writing_add,auto[84:87]>         16           1        -    Covered
      bin <writing_add,auto[80:83]>         15           1        -    Covered
      bin <writing_add,auto[76:79]>         16           1        -    Covered
      bin <writing_add,auto[72:75]>         15           1        -    Covered
      bin <writing_add,auto[68:71]>         16           1        -    Covered
```

```
        bin <writing_add,auto[64:67]>              16        1        -    Covered
        bin <writing_add,auto[60:63]>              15        1        -    Covered
        bin <writing_add,auto[56:59]>              16        1        -    Covered
        bin <writing_add,auto[52:55]>              14        1        -    Covered
        bin <writing_add,auto[48:51]>              16        1        -    Covered
        bin <writing_add,auto[44:47]>              16        1        -    Covered
        bin <writing_add,auto[40:43]>              16        1        -    Covered
        bin <writing_add,auto[36:39]>              16        1        -    Covered
        bin <writing_add,auto[32:35]>              16        1        -    Covered
        bin <writing_add,auto[28:31]>              16        1        -    Covered
        bin <writing_add,auto[24:27]>              16        1        -    Covered
        bin <writing_add,auto[20:23]>              16        1        -    Covered
        bin <writing_add,auto[16:19]>              16        1        -    Covered
        bin <writing_add,auto[12:15]>              15        1        -    Covered
        bin <writing_add,auto[8:11]>               16        1        -    Covered
        bin <writing_add,auto[4:7]>                16        1        -    Covered
        bin <writing_add,auto[0:3]>                10016     1        -    Covered
    Cross Actualiy_sending_data_wr                 100.00%   100      -    Covered
      covered/total bins:                          64        64       -
      missing/total bins:                          0         64       -
      % Hit:                                       100.00%   100      -
      Auto, Default and User Defined Bins:
        bin <writing_data,auto[252:255]>           16        1        -    Covered
        bin <writing_data,auto[248:251]>           16        1        -    Covered
        bin <writing_data,auto[244:247]>           16        1        -    Covered
        bin <writing_data,auto[240:243]>           16        1        -    Covered
        bin <writing_data,auto[236:239]>           15        1        -    Covered
        bin <writing_data,auto[232:235]>           16        1        -    Covered
        bin <writing_data,auto[228:231]>           16        1        -    Covered
        bin <writing_data,auto[224:227]>           16        1        -    Covered
        bin <writing_data,auto[220:223]>           16        1        -    Covered
        bin <writing_data,auto[216:219]>           16        1        -    Covered
        bin <writing_data,auto[212:215]>           13        1        -    Covered
        bin <writing_data,auto[208:211]>           16        1        -    Covered
        bin <writing_data,auto[204:207]>           16        1        -    Covered
        bin <writing_data,auto[200:203]>           16        1        -    Covered
        bin <writing_data,auto[196:199]>           16        1        -    Covered
        bin <writing_data,auto[192:195]>           16        1        -    Covered
        bin <writing_data,auto[188:191]>           16        1        -    Covered
        bin <writing_data,auto[184:187]>           16        1        -    Covered
        bin <writing_data,auto[180:183]>           15        1        -    Covered
        bin <writing_data,auto[176:179]>           16        1        -    Covered
        bin <writing_data,auto[172:175]>           16        1        -    Covered
        bin <writing_data,auto[168:171]>           16        1        -    Covered
        bin <writing_data,auto[164:167]>           16        1        -    Covered
        bin <writing_data,auto[160:163]>           15        1        -    Covered
        bin <writing_data,auto[156:159]>           16        1        -    Covered
        bin <writing_data,auto[152:155]>           15        1        -    Covered
        bin <writing_data,auto[148:151]>           16        1        -    Covered
        bin <writing_data,auto[144:147]>           15        1        -    Covered
        bin <writing_data,auto[140:143]>           14        1        -    Covered
        bin <writing_data,auto[136:139]>           16        1        -    Covered
        bin <writing_data,auto[132:135]>           15        1        -    Covered
        bin <writing_data,auto[128:131]>           15        1        -    Covered
        bin <writing_data,auto[124:127]>           16        1        -    Covered
        bin <writing_data,auto[120:123]>           13        1        -    Covered
        bin <writing_data,auto[116:119]>           15        1        -    Covered
        bin <writing_data,auto[112:115]>           16        1        -    Covered
        bin <writing_data,auto[108:111]>           16        1        -    Covered
        bin <writing_data,auto[104:107]>           16        1        -    Covered
        bin <writing_data,auto[100:103]>           16        1        -    Covered
        bin <writing_data,auto[96:99]>             16        1        -    Covered
        bin <writing_data,auto[92:95]>             16        1        -    Covered
        bin <writing_data,auto[88:91]>             16        1        -    Covered
        bin <writing_data,auto[84:87]>             16        1        -    Covered
        bin <writing_data,auto[80:83]>             16        1        -    Covered
```

```
        bin <writing_data,auto[76:79]>              15        1        -    Covered
        bin <writing_data,auto[72:75]>              15        1        -    Covered
        bin <writing_data,auto[68:71]>              16        1        -    Covered
        bin <writing_data,auto[64:67]>              14        1        -    Covered
        bin <writing_data,auto[60:63]>              15        1        -    Covered
        bin <writing_data,auto[56:59]>              16        1        -    Covered
        bin <writing_data,auto[52:55]>              16        1        -    Covered
        bin <writing_data,auto[48:51]>              16        1        -    Covered
        bin <writing_data,auto[44:47]>              16        1        -    Covered
        bin <writing_data,auto[40:43]>              16        1        -    Covered
        bin <writing_data,auto[36:39]>              16        1        -    Covered
        bin <writing_data,auto[32:35]>              15        1        -    Covered
        bin <writing_data,auto[28:31]>              15        1        -    Covered
        bin <writing_data,auto[24:27]>              16        1        -    Covered
        bin <writing_data,auto[20:23]>              16        1        -    Covered
        bin <writing_data,auto[16:19]>              16        1        -    Covered
        bin <writing_data,auto[12:15]>              16        1        -    Covered
        bin <writing_data,auto[8:11]>               15        1        -    Covered
        bin <writing_data,auto[4:7]>                16        1        -    Covered
        bin <writing_data,auto[0:3]>             10016        1        -    Covered
    Cross Actualiy_sending_addr_rd                  100.00%      100        -    Covered
      covered/total bins:                       64        64        -
      missing/total bins:                       0         64        -
      % Hit:                                    100.00%   100       -
      Auto, Default and User Defined Bins:
        bin <reading_add,auto[252:255]>             16        1        -    Covered
        bin <reading_add,auto[248:251]>             16        1        -    Covered
        bin <reading_add,auto[244:247]>             16        1        -    Covered
        bin <reading_add,auto[240:243]>             15        1        -    Covered
        bin <reading_add,auto[236:239]>             16        1        -    Covered
        bin <reading_add,auto[232:235]>             16        1        -    Covered
        bin <reading_add,auto[228:231]>             16        1        -    Covered
        bin <reading_add,auto[224:227]>             15        1        -    Covered
        bin <reading_add,auto[220:223]>             15        1        -    Covered
        bin <reading_add,auto[216:219]>             16        1        -    Covered
        bin <reading_add,auto[212:215]>             16        1        -    Covered
        bin <reading_add,auto[208:211]>             14        1        -    Covered
        bin <reading_add,auto[204:207]>             15        1        -    Covered
        bin <reading_add,auto[200:203]>             16        1        -    Covered
        bin <reading_add,auto[196:199]>             16        1        -    Covered
        bin <reading_add,auto[192:195]>             15        1        -    Covered
        bin <reading_add,auto[188:191]>             15        1        -    Covered
        bin <reading_add,auto[184:187]>             14        1        -    Covered
        bin <reading_add,auto[180:183]>             16        1        -    Covered
        bin <reading_add,auto[176:179]>             16        1        -    Covered
        bin <reading_add,auto[172:175]>             14        1        -    Covered
        bin <reading_add,auto[168:171]>             16        1        -    Covered
        bin <reading_add,auto[164:167]>             16        1        -    Covered
        bin <reading_add,auto[160:163]>             16        1        -    Covered
        bin <reading_add,auto[156:159]>             15        1        -    Covered
        bin <reading_add,auto[152:155]>             16        1        -    Covered
        bin <reading_add,auto[148:151]>             16        1        -    Covered
        bin <reading_add,auto[144:147]>             16        1        -    Covered
        bin <reading_add,auto[140:143]>             16        1        -    Covered
        bin <reading_add,auto[136:139]>             15        1        -    Covered
        bin <reading_add,auto[132:135]>             16        1        -    Covered
        bin <reading_add,auto[128:131]>             15        1        -    Covered
        bin <reading_add,auto[124:127]>             16        1        -    Covered
        bin <reading_add,auto[120:123]>             16        1        -    Covered
        bin <reading_add,auto[116:119]>             15        1        -    Covered
        bin <reading_add,auto[112:115]>             15        1        -    Covered
        bin <reading_add,auto[108:111]>             16        1        -    Covered
        bin <reading_add,auto[104:107]>             16        1        -    Covered
        bin <reading_add,auto[100:103]>             15        1        -    Covered
        bin <reading_add,auto[96:99]>               16        1        -    Covered
        bin <reading_add,auto[92:95]>               16        1        -    Covered
```

```
        bin <reading_add,auto[88:91]>              16        1        -    Covered
        bin <reading_add,auto[84:87]>              16        1        -    Covered
        bin <reading_add,auto[80:83]>              15        1        -    Covered
        bin <reading_add,auto[76:79]>              16        1        -    Covered
        bin <reading_add,auto[72:75]>              15        1        -    Covered
        bin <reading_add,auto[68:71]>              16        1        -    Covered
        bin <reading_add,auto[64:67]>              16        1        -    Covered
        bin <reading_add,auto[60:63]>              15        1        -    Covered
        bin <reading_add,auto[56:59]>              16        1        -    Covered
        bin <reading_add,auto[52:55]>              14        1        -    Covered
        bin <reading_add,auto[48:51]>              16        1        -    Covered
        bin <reading_add,auto[44:47]>              16        1        -    Covered
        bin <reading_add,auto[40:43]>              16        1        -    Covered
        bin <reading_add,auto[36:39]>              16        1        -    Covered
        bin <reading_add,auto[32:35]>              16        1        -    Covered
        bin <reading_add,auto[28:31]>              16        1        -    Covered
        bin <reading_add,auto[24:27]>              16        1        -    Covered
        bin <reading_add,auto[20:23]>              16        1        -    Covered
        bin <reading_add,auto[16:19]>              16        1        -    Covered
        bin <reading_add,auto[12:15]>              15        1        -    Covered
        bin <reading_add,auto[8:11]>               16        1        -    Covered
        bin <reading_add,auto[4:7]>                16        1        -    Covered
        bin <reading_add,auto[0:3]>             10016        1        -    Covered
    Cross Actualiy_recieving_data                 100.00%    100        -    Covered
      covered/total bins:                    64        64       -
      missing/total bins:                    0         64       -
      % Hit:                                 100.00%   100      -
      Auto, Default and User Defined Bins:
        bin <reading_data,auto[252:255]>           16        1        -    Covered
        bin <reading_data,auto[248:251]>           16        1        -    Covered
        bin <reading_data,auto[244:247]>           16        1        -    Covered
        bin <reading_data,auto[240:243]>           16        1        -    Covered
        bin <reading_data,auto[236:239]>           15        1        -    Covered
        bin <reading_data,auto[232:235]>           16        1        -    Covered
        bin <reading_data,auto[228:231]>           16        1        -    Covered
        bin <reading_data,auto[224:227]>           16        1        -    Covered
        bin <reading_data,auto[220:223]>           16        1        -    Covered
        bin <reading_data,auto[216:219]>           16        1        -    Covered
        bin <reading_data,auto[212:215]>           13        1        -    Covered
        bin <reading_data,auto[208:211]>           16        1        -    Covered
        bin <reading_data,auto[204:207]>           16        1        -    Covered
        bin <reading_data,auto[200:203]>           16        1        -    Covered
        bin <reading_data,auto[196:199]>           16        1        -    Covered
        bin <reading_data,auto[192:195]>           16        1        -    Covered
        bin <reading_data,auto[188:191]>           16        1        -    Covered
        bin <reading_data,auto[184:187]>           16        1        -    Covered
        bin <reading_data,auto[180:183]>           15        1        -    Covered
        bin <reading_data,auto[176:179]>           16        1        -    Covered
        bin <reading_data,auto[172:175]>           16        1        -    Covered
        bin <reading_data,auto[168:171]>           16        1        -    Covered
        bin <reading_data,auto[164:167]>           16        1        -    Covered
        bin <reading_data,auto[160:163]>           15        1        -    Covered
        bin <reading_data,auto[156:159]>           16        1        -    Covered
        bin <reading_data,auto[152:155]>           15        1        -    Covered
        bin <reading_data,auto[148:151]>           16        1        -    Covered
        bin <reading_data,auto[144:147]>           15        1        -    Covered
        bin <reading_data,auto[140:143]>           14        1        -    Covered
        bin <reading_data,auto[136:139]>           16        1        -    Covered
        bin <reading_data,auto[132:135]>           15        1        -    Covered
        bin <reading_data,auto[128:131]>           15        1        -    Covered
        bin <reading_data,auto[124:127]>           16        1        -    Covered
        bin <reading_data,auto[120:123]>           13        1        -    Covered
        bin <reading_data,auto[116:119]>           15        1        -    Covered
        bin <reading_data,auto[112:115]>           16        1        -    Covered
        bin <reading_data,auto[108:111]>           16        1        -    Covered
        bin <reading_data,auto[104:107]>           16        1        -    Covered
```

bin <reading_data,auto[100:103]>	16	1	-	Covered
bin <reading_data,auto[96:99]>	16	1	-	Covered
bin <reading_data,auto[92:95]>	16	1	-	Covered
bin <reading_data,auto[88:91]>	16	1	-	Covered
bin <reading_data,auto[84:87]>	16	1	-	Covered
bin <reading_data,auto[80:83]>	16	1	-	Covered
bin <reading_data,auto[76:79]>	15	1	-	Covered
bin <reading_data,auto[72:75]>	15	1	-	Covered
bin <reading_data,auto[68:71]>	16	1	-	Covered
bin <reading_data,auto[64:67]>	14	1	-	Covered
bin <reading_data,auto[60:63]>	15	1	-	Covered
bin <reading_data,auto[56:59]>	16	1	-	Covered
bin <reading_data,auto[52:55]>	16	1	-	Covered
bin <reading_data,auto[48:51]>	16	1	-	Covered
bin <reading_data,auto[44:47]>	16	1	-	Covered
bin <reading_data,auto[40:43]>	16	1	-	Covered
bin <reading_data,auto[36:39]>	16	1	-	Covered
bin <reading_data,auto[32:35]>	15	1	-	Covered
bin <reading_data,auto[28:31]>	15	1	-	Covered
bin <reading_data,auto[24:27]>	16	1	-	Covered
bin <reading_data,auto[20:23]>	16	1	-	Covered
bin <reading_data,auto[16:19]>	16	1	-	Covered
bin <reading_data,auto[12:15]>	16	1	-	Covered
bin <reading_data,auto[8:11]>	15	1	-	Covered
bin <reading_data,auto[4:7]>	16	1	-	Covered
bin <reading_data,auto[0:3]>	7016	1	-	Covered

TOTAL COVERGROUP COVERAGE: 100.00% COVERGROUP TYPES: 2

Total Coverage By Instance (filtered view): 100.00%