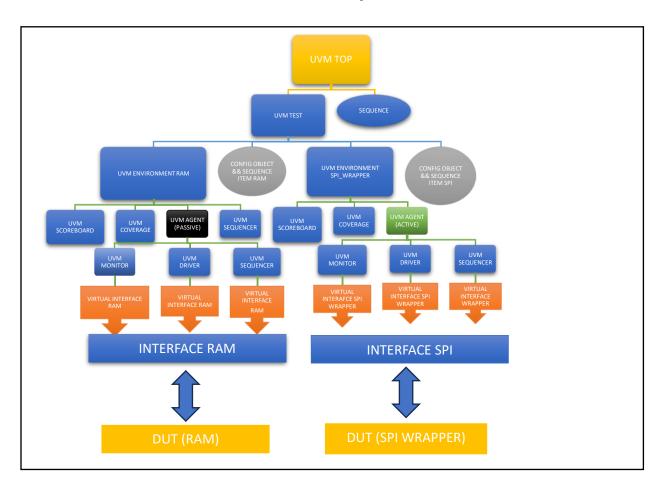
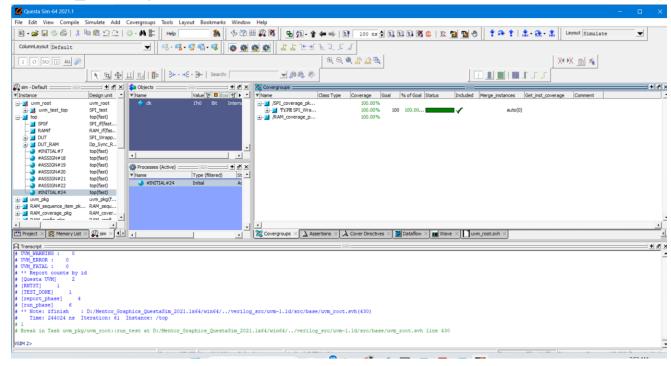
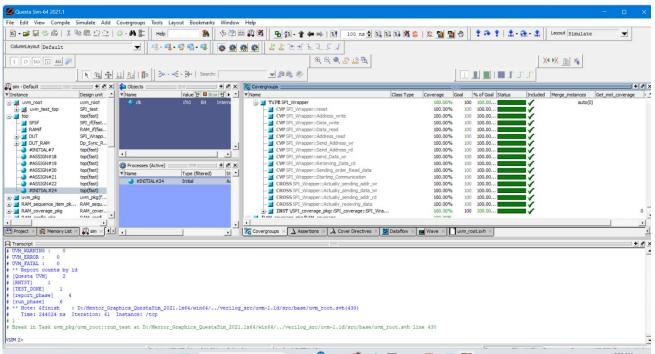
UVM Project



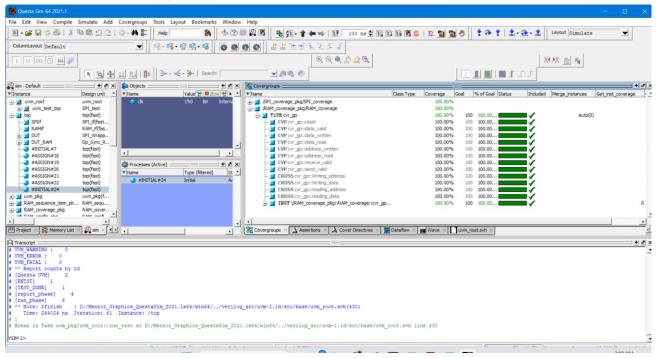
♣ F_Coverage:



♣ SPI F_Coverage:



♣ RAM Coverage:



♣ Do file

```
vlib work
vlog -f slc_file.txt -sv +cover
vsim -voptargs=+acc work.top -classdebug -uvmcontrol=all -coverage
run 0
coverage save RAM_CV.ucdb -onexit -du Dp_Sync_RAM_wrapper
run -all
quit -sim
vcover report RAM CV.ucdb -all -annotate -details -output code coverage RAM.txt
vlib work
vlog -f slc file.txt -sv +cover
vsim -voptargs=+acc work.top -classdebug -uvmcontrol=all -coverage
coverage save SPI_Wrapper_CV.ucdb -onexit -du SPI_Wrapper
run -all
quit -sim
vcover report SPI_Wrapper_CV.ucdb -all -annotate -details -output code_coverage_SPI_Wrapper.txt
vlib work
vlog -f slc file.txt -sv +cover
vsim -voptargs=+acc work.top -classdebug -uvmcontrol=all -coverage
run 0
run -all
coverage report -detail -cvg -comments -output fcover report.txt {}
quit -sim
```

4 RAM bugs from previous project:

```
RAM bugs:
     15
              integer i;
              always @(posedge \ clk \ or \ negedge \ rst_n) begin
     17
                  if (!rst_n) begin
     18
                    dout <= 0;
                     for(i=0; i<MEM_DEPTH; i=i+1)</pre>
     20
                      mem[i] \leftarrow 0;
     21
                 end
                 else if (rx_valid) begin
     22
                    tx_valid <= 0;
     24
                     case (din[9:8])
     25
                      2'b00: addr_wr <= din[7:0];
                      2'b01: mem[addr_wr] <= din[7:0];
     26
     27
                      2'b10: addr_rd <= din[7:0];
     28
                      2'b11: {dout, tx_valid} <= {mem[addr_rd], 1'b1};</pre>
     29
                     endcase
                 end
     30
     31
              end
```

- rst_n must be Async.
- 2) rst n doesn't clear the RAM.
- 3) When rest asserted the internal signals (addr_rd,addr_wr) and output signal (dout and tx_valid) must equal zeros.

Handling:

```
always @(posedge clk ) begin // first bug : rst must be syncrouns no Ashync
if (!rst_n) begin
19
20
21
                dout <= 0;
                tx_valid <= 0; //second bug : tx must take zero when rst_n is asserted</pre>
                rd\_addr \leftarrow 0;//3th bug : when rst_n asserted , addr and not 2 internal signals it only one
25
            else if (rx_valid) begin
26
               tx_valid <= 0;
                case (din[9:8])
28
                 2'b00: wr_addr
                                   <= din[7:0];
                2'b01: mem[wr_addr] <= din[7:0];
31
                 2'b10: rd_addr <= din[7:0];
32
                default: {dout, tx_valid} <= {mem[rd_addr], 1'b1};</pre>
               endcase
            end
34
35
            else begin
                 tx_valid <= 0;
             //4th bug : when rx_valid not asserted then tx_valid must down to zero
39
10
```

♣ SPI bugs also from previous project:

```
SPI bugs:
     12
             reg [2:0] cs, ns;
     13
             reg [9:0] PO;
             wire [7:0] temp;
     14
     15
             reg SO, flag_rd = 0;
     16
             integer state_count = 0, final_count = 0;
     17
             assign temp = (tx_valid)? tx_data: temp;
     18
     19
             assign MISO = SO;
     21
             always @(posedge clk or negedge rst_n) begin
                if (!rst_n)
     22
     23
                    cs <= IDLE;
     24
                 else
     25
                     cs <= ns;
```

- 4) rst_n must be Async.
- 5) When reset is asserted the flags and counters must flush and data_out signals must also zeros.

Handling:

Current state bugs:

Handle:

Bugs flag of read operation:

```
always @(MOSI, SS_n, cs) begin case (cs)
  53
54
55
                                 if (SS_n)
                                ns = IDLE;
else
                                 ns = CHK_CMD;
CHK_CMD:
  59
60
                                CHK_CMD:
if (SS_n)
    ns = IDLE;
else begin
    if (!MOSI)
    ns = WRITE;
else begin
    if (!flag_rd)
        ns = READ_ADD;
else
  64
  65
67
                                      ns = READ_DATA;
end
  69
                            end
WRITE:
if (SS_n)
ns = IDLE;

WRITE
  73
74
75
76
77
78
79
                                ns = WRITE;
READ ADD:
                                if (SS_n)
  80
81
                                      ns = IDLE;
                                ns = IDLE;
else begin
    ns = READ_ADD; flag_rd = 1;
end
    READ_DATA:
  83
                                if (SS_n)
ns = IDLE;
  85
86
                                ns = IDLE;
else begin
ns = READ_DATA; flag_rd = 0;
end
  87
  88
                                   default: ns = IDLE;
  90
                         endcase
  92
93
```

Handle:

The value of the flag changed in current state (reading data or address) block not here.

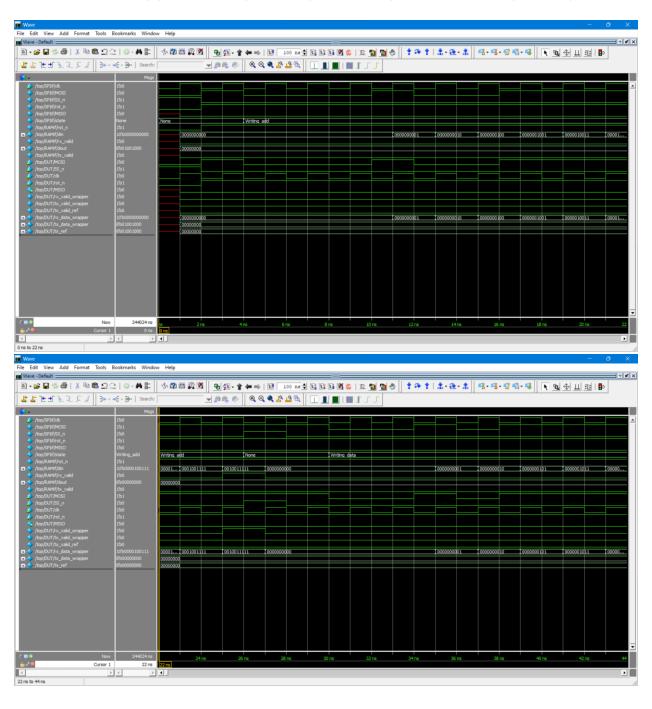
```
138
139
                   always @(*) begin
                          case (cs)
140
141
                                        if (SS_n)
ns = IDLE;
else
142
                                 ns = CHK_CMD;
145
146
                                        if (SS_n)
                                        in (35_n)
| ns = IDLE;
| else begin//SS_n = 0
| if (MOSI==0) //MOSI = 0
| ns = WRTTF-
148
149
150
                                                ns = WRITE;
else begin //MOSI = 1
if (!flag_rd) //flag_rd = 0
ns = READ_ADD;
else //flag_rd = 1
151
152
153
154
155
156
157
158
                                        end
end
                                 write:
if (SS_n)
ns = IDLE;
else
160
161
162
                                 ns = WRITE;
READ_ADD:
163
164
165
166
167
                                        if (SS_n)

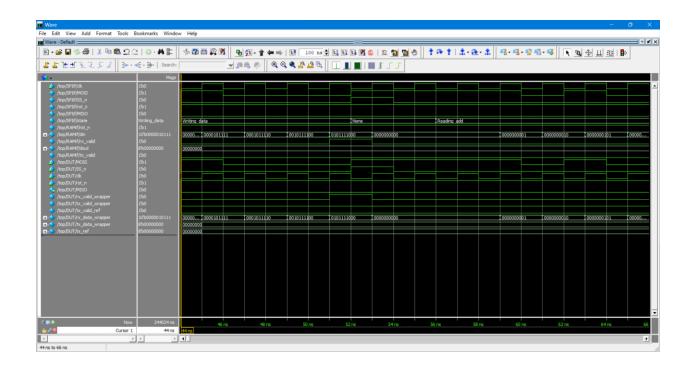
ns = IDLE;
else begin
                                        ns = READ_ADD;

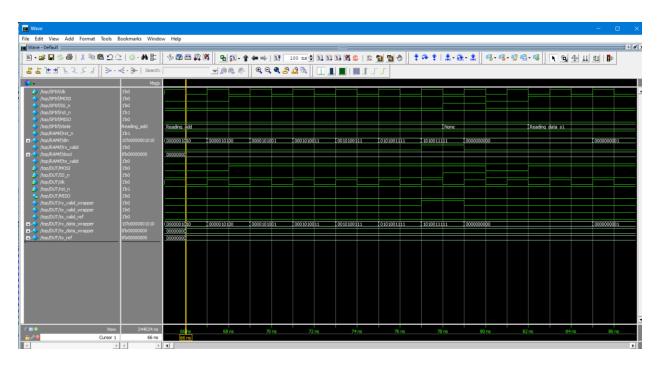
// flag_rd = 1;

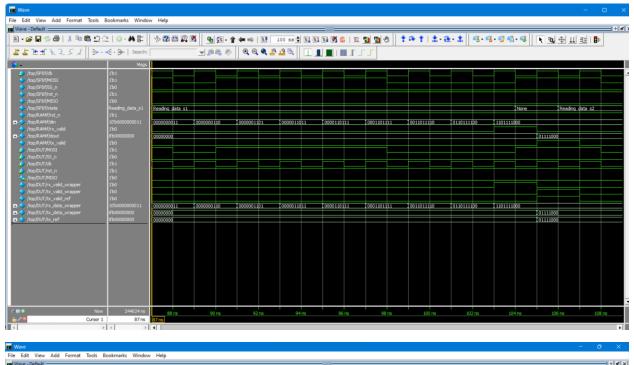
end
168
169
170
                                READ_DATA:
                                 READ_DATA:
   if (SS_n)
        ns = IDLE;
   else begin
        ns = READ_DATA;
        // flag_rd = 0;
}
174
175
                                         end
177
178
                                  default: ns = IDLE;
180
181
182
                          endcase
```

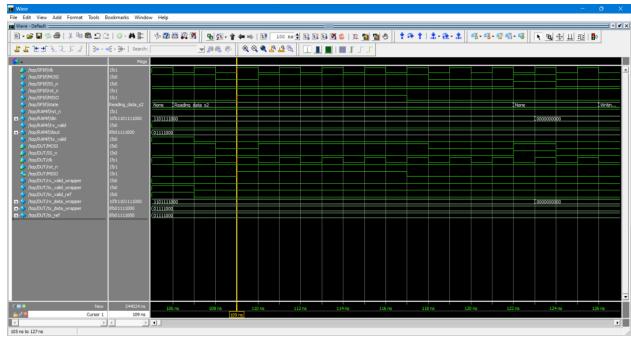
♣ Questa snippets from part 3 :(for one cycle of first sequence):











```
The fact Wave Reclaments Window Help

The fact Wave Reclaments W
```

- The following will be:
 - 1. RAM code coverage.
 - 2. Wrapper code coverage.
 - 3. Assertion (that I didn't do it)
 - 4. Functional coverage for RAM
 - 5. Functional coverage for wrapper



+ code cov	3146	10001001											
RAM code coverage		e Report by inst											
				======	=====	======							
	=== Desi	ance: /\top#DU gn Unit: work.[Dp_Sync_R		•								
		coverage:	=======		=====	:======							
	Enab	led Coverage	Bi	ns Hit	s IV	lisses Cov	verage verage						
	Branc		7	7 (100	0.00%							
	======	========	======	====Bra	nch D	etails====							
	Branch (Coverage for ins	tance /\to	p#DUT_R	AM								
	Line	Item	Count	Source	e								
		_Sync_RAM.sv	IF Bran	ıch									
	16		122012										
		1	12				if (!rst_n) begin						
	22	1	8000				x_valid) begin						
	31	1				else beg	gin						
	Branch t	otals: 3 hits of 3	3 branches	= 100.00)%								
			CASE B	ranch									
	24					n to CASE							
	25	1	2000		_		2'b00: wr_addr <= din[7:0];						
		1					2'b01: mem[wr_addr] <= din[7:0];						
		1					2'b10: rd_addr <= din[7:0];						
	28	1	2000				default: {dout, tx_valid} <=						
		l_addr], 1'b1}; otals: 4 hits of 4	4 branches	= 100.00	1%								
	Statement Coverage:												
				ns Hit	·s M	lisses Cov	uerage						
	Enabled Coverage Bins Hits Misses Coverage												
	Statements 13 13 0 100.00%												
	======	=======	======	====Stat	emen	t Details==							
	Stateme	nt Coverage for	instance /	\top#DU	T_RAN	И							
	Line 	Item	Count	Source	e								
	File Dp	_Sync_RAM.sv											
	1		mod	dule Dp_9	Sync_I	RAM_wrap	per(rst_n, din, rx_valid, dout, tx_valid);						
	2				parameter MEM_DEPTH = 256;								
	3			par	amete	er ADDR_SI	ZE = 8;						
	4			:	+ ~~+	النامين بم م							
	5 6					n, rx_valid	,						
	6 input [9:0] din; 7 output reg tx_valid;												
	8					g [7:0] dou	ıt;						
	9				_		<u></u>						
			_	_		_							

```
reg [7:0] mem [MEM_DEPTH-1:0];
  10
  11
                                    reg [ADDR SIZE-1:0] rd addr,wr addr;
  12
  13
                                    initial begin // first bug : rst must be syncrouns no Ashync
  14
                          1
           1
                          1
                                             forever begin
  15
           1
  16
                                                      if (!rst_n) begin
  17
           1
                         12
                                                 dout \le 0;
 18
           1
                         12
                                                 tx valid <= 0; //second bug : tx must take
zero when rst n is asserted
 19
           1
                         12
                                                 wr addr \leq 0;
                         12
                                                 rd_addr <= 0 ;//3th bug : when rst_n
 20
           1
asserted, addr and not 2 internal signals it only one
  22
                                               else if (rx_valid) begin
  23
                        8000
                                                 tx_valid <= 0;
  24
                                                 case (din[9:8])
  25
                        2000
                                                           2'b00: wr_addr <= din[7:0];
           1
  26
                        2000
                                                           2'b01: mem[wr_addr] <= din[7:0];
           1
                                                           2'b10: rd addr <= din[7:0];
  27
           1
                        2000
  28
           1
                        2000
                                                           default: {dout, tx_valid} <=</pre>
{mem[rd_addr], 1'b1};
  29
                                                 endcase
  30
                                               end
  31
                                               else begin
  32
                       114000
           1
                                                        tx valid <= 0;
  33
                                               end
  34
                                              //4th bug : when rx_valid not asserted then
tx valid must down to zero
 35
           1
                       122012
                                              #2;
Toggle Coverage:
  Enabled Coverage
                             Bins
                                    Hits Misses Coverage
                        74
                               74
                                       0 100.00%
  Toggles
             =============Toggle Details======================
Toggle Coverage for instance /\top#DUT_RAM --
                       Node 1H->0L 0L->1H
                                                             "Coverage"
                     din[0-9]
                                  1
                                         1
                                                          100.00
                     dout[7-0]
                                                           100.00
                                          1
                   rd_addr[7-0]
                                                            100.00
                                        1
                                                         100.00
                       rst_n
                     rx_valid
                                         1
                                                          100.00
                                  1
                                                          100.00
                     tx_valid
                                  1
                                         1
                   wr_addr[7-0]
                                                             100.00
Total Node Count =
Toggled Node Count =
                          37
Untoggled Node Count =
Toggle Coverage = 100.00% (74 of 74 bins)
```

	Total Coverage By Instance (filtered view): 100.00%	
SPI_wrapper	Coverage Report by instance with details	
code coverage		
(SPI_slave code	=== Instance: /\top#DUT /DUT_2	
coverage)	=== Design Unit: work.SPI_Slave_wrapper	
22.2.2.804	Branch Coverage:	
	Enabled Coverage Bins Hits Misses Coverage	
	Branches 47 46 1 97.87%	
	======================================	========
	Branch Coverage for instance /\top#DUT /DUT_2	
	Line Item Count Source	
	File SPI_Slave.sv	
	25 122012 Count coming in to IF	
	25 122012 Count coming in to IF 25 1 12 if (!rst_n)begin	
	32 1 122000 else	
	Branch totals: 2 hits of 2 branches = 100.00%	
	IF Branch	
	36 24001 Count coming in to IF	
	36 1 8001 if (cs == IDLE)begin	
	16000 All False Count Branch totals: 2 hits of 2 branches = 100.00%	
	CASE Branch	
	48 122012 Count coming in to CASE 49 1 8011 IDLE : begi	'n
	58 1 44000 WRITE: begin //dor	
	73 1 22000 READ_ADD: begin /	•
		// done
	120 1 8001 default: begin Branch totals: 5 hits of 5 branches = 100.00%	
	IF Branch	
	60 44000 Count coming in to IF 60 1 40000 i	if (state_count < 10)begin //0 ,
		else
	Branch totals: 2 hits of 2 branches = 100.00%	
	IF Branch	
	63 40000 Count coming in to IF	15 (0.10.1) 4110.00
	63 1 4000 state_count ==10)begin	if (PO[9] ==1'b0 &&
	66 1 36000	else
	Branch totals: 2 hits of 2 branches = 100.00%	
	IF Branch	
	75 22000 Count coming in to IF	
	· · · · · · · · · · · · · · · · · · ·	unt<10)begin
	2000 All False Count Branch totals: 2 hits of 2 branches = 100.00%	
	IE Pranch	
	80 22000 Count coming in to IF	

80			
	1	4000	if (PO[9:8]==2'b10 &&
	ınt==10)be		ala-
84	1	18000	else
Branch to	tais: 2 hits	s of 2 branches = 100.00%	
		IE Branch	
		IF Branch	
89 80	1	40000 Count comi	
			if (Act_input_output == 0)begin
	1 tals: 2 hits		else begin
DI ADIIBIO	itais: Z NIts	s of 2 branches = 100.00%	
		IF Branch	
90		20000 Count comi	
90	1	18000	if (state count<9)begin
95	1		else begin
		s of 2 branches = 100.00%	eise begiii
Dianei to	Z 11113	, 5. 2 branches - 100.00/6	
		IF Branch	
101		20000 Count comi	
	1	2000	if (PO[9:8]==2'b11 && state_count==
10)begin			, , ,
, 0		18000 All False Cour	nt
Branch to	tals: 2 hits	of 2 branches = 100.00%	
		IF Branch	
110		20000 Count comi	ing in to IF
110	1	2000	if (tx_valid && state_count ==
12)begin			
		18000 All False Cour	nt
Branch to	tals: 2 hits	of 2 branches = 100.00%	
		IF Branch	
44-		20000 -	
113		20000 Count comi	ing in to IF
113	1	16000	
113	1 nt <= 7)be	16000 gin	ing in to IF if (state_count >= 12 &&
113 final_cou	nt <= 7)be	16000 gin 4000 All False Coun	ing in to IF if (state_count >= 12 &&
113 final_cou	nt <= 7)be	16000 gin	ing in to IF if (state_count >= 12 &&
113 final_cou Branch to	nt <= 7)be	16000 gin 4000 All False Coun s of 2 branches = 100.00%	ing in to IF if (state_count >= 12 && t
113 final_coul Branch to	nt <= 7)be	16000 gin 4000 All False Coun s of 2 branches = 100.00%CASE Branch	ing in to IF if (state_count >= 12 && t
113 final_cour	nt <= 7)be	16000 gin 4000 All False Coun s of 2 branches = 100.00%CASE Branch 92914 Count comi	ing in to IF if (state_count >= 12 && t ing in to CASE
113 final_countries of the second sec	nt <= 7)be tals: 2 hits 1 1	16000 gin 4000 All False Coun s of 2 branches = 100.00%CASE Branch 92914 Count comi 16006 11967	ing in to IF if (state_count >= 12 && t ing in to CASE IDLE:
113 final_cour Branch to 134 135 140	nt <= 7)be tals: 2 hits 1 1	16000 gin 4000 All False Coun s of 2 branches = 100.00%CASE Branch 92914 Count comi 16006 11967	ing in to IF if (state_count >= 12 && t ing in to CASE IDLE: CHK_CMD:
113 final_cour Branch to 	nt <= 7)be tals: 2 hits 	16000 gin 4000 All False Coun s of 2 branches = 100.00%CASE Branch 92914 Count comi 16006 11967 25982	ing in to IF if (state_count >= 12 && t ing in to CASE IDLE: CHK_CMD: WRITE:
113 final_could branch to 134 135 140 153 158	nt <= 7)be stals: 2 hits 	16000 gin 4000 All False Coun s of 2 branches = 100.00%CASE Branch 92914 Count comi 16006 11967 25982 15981	ing in to IF if (state_count >= 12 && t ing in to CASE
113 final_could branch to 134 135 140 153 158 165	nt <= 7)be stals: 2 hits 	16000 gin 4000 All False Coun s of 2 branches = 100.00%	ing in to IF if (state_count >= 12 && t ing in to CASE
113 final_countries final_coun	nt <= 7)be	16000 gin 4000 All False Coun s of 2 branches = 100.00%	ing in to IF if (state_count >= 12 && t ing in to CASE IDLE: CHK_CMD: WRITE: READ_ADD:
113 final_countries final_coun	nt <= 7)be	16000 gin 4000 All False Coun s of 2 branches = 100.00%	ing in to IF if (state_count >= 12 && t ing in to CASE
113 final_countries final_coun	nt <= 7)be tals: 2 hits 	16000 gin 4000 All False Coun s of 2 branches = 100.00%	ing in to IF if (state_count >= 12 && t ing in to CASE IDLE: CHK_CMD: WRITE: READ_ADD: READ_DATA: default: ns = IDLE;
113 final_could Branch to 134 135 140 153 158 165 173 Branch to 155 175 Branch to 15	nt <= 7)be tals: 2 hits 	16000 gin 4000 All False Coun s of 2 branches = 100.00%	ing in to IF if (state_count >= 12 && t ing in to CASE IDLE: CHK_CMD: WRITE: READ_ADD: READ_DATA: default: ns = IDLE;
113 final_could Branch to	nt <= 7)be	16000 gin 4000 All False Coun s of 2 branches = 100.00%	ing in to IF if (state_count >= 12 && t ing in to CASE IDLE: CHK_CMD: WRITE: READ_ADD: READ_DATA: default: ns = IDLE; ing in to IF
113 final_countries final_coun	nt <= 7)be tals: 2 hits 	16000 gin 4000 All False Coun of 2 branches = 100.00%	ing in to IF if (state_count >= 12 && t ing in to CASE IDLE: CHK_CMD: WRITE: READ_ADD: READ_DATA: default: ns = IDLE; ing in to IF if (SS_n)
113 final_countries final_coun	nt <= 7)be	16000 gin 4000 All False Coun s of 2 branches = 100.00%	ing in to IF if (state_count >= 12 && t ing in to CASE IDLE: CHK_CMD: WRITE: READ_ADD: READ_DATA: default: ns = IDLE; ing in to IF
113 final_countries final_coun	nt <= 7)be	16000 gin 4000 All False Coun of 2 branches = 100.00%	ing in to IF if (state_count >= 12 && t ing in to CASE IDLE: CHK_CMD: WRITE: READ_ADD: READ_DATA: default: ns = IDLE; ing in to IF if (SS_n)
113 final_countries final_coun	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	16000 gin 4000 All False Coun of 2 branches = 100.00%	ing in to IF if (state_count >= 12 && t ing in to CASE IDLE: CHK_CMD: WRITE: READ_ADD: READ_DATA: default: ns = IDLE; ing in to IF if (SS_n) else
113 final_countries final_coun	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	16000 gin 4000 All False Coun s of 2 branches = 100.00%	ing in to IF if (state_count >= 12 && t ing in to CASE IDLE: CHK_CMD: WRITE: READ_ADD: READ_DATA: default: ns = IDLE; ing in to IF if (SS_n) else
113 final_countries final_coun	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	16000 gin 4000 All False Coun of 2 branches = 100.00%	ing in to IF if (state_count >= 12 && t ing in to CASE IDLE: CHK_CMD: WRITE: READ_ADD: READ_DATA: default: ns = IDLE; ing in to IF if (SS_n) else
113 final_countries final_coun	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	16000 gin 4000 All False Couns of 2 branches = 100.00%	ing in to IF if (state_count >= 12 && t ing in to CASE IDLE: CHK_CMD: WRITE: READ_ADD: READ_DATA: default: ns = IDLE; ing in to IF if (SS_n) else
113 final_countries final_coun	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	16000 gin 4000 All False Counts of 2 branches = 100.00% CASE Branch 92914 Count coming 16006 11967 25982 15981 22977 1 s of 6 branches = 100.00% IF Branch	ing in to IF if (state_count >= 12 && t if (state_count >= 12 && if (state_count >=
113 final_countries final_coun	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	16000 gin 4000 All False Couns of 2 branches = 100.00%	ing in to IF if (state_count >= 12 && t ing in to CASE IDLE: CHK_CMD: WRITE: READ_ADD: READ_DATA: default: ns = IDLE; ing in to IF if (SS_n) else
113 final_countries final_coun	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	16000 gin 4000 All False Coun s of 2 branches = 100.00% CASE Branch 92914 Count comi 16006 11967 25982 15981 22977 1 s of 6 branches = 100.00% IF Branch 16006 Count comi 8006 8000 s of 2 branches = 100.00% IF Branch	ing in to IF if (state_count >= 12 && t if (state_count >= 12 && if (state_count
113 final_countries final_coun	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	16000 gin 4000 All False Coun s of 2 branches = 100.00% CASE Branch 92914 Count comi 16006 11967 25982 15981 22977 1 s of 6 branches = 100.00% IF Branch 16006 Count comi 8006 8000 s of 2 branches = 100.00% IF Branch	ing in to IF if (state_count >= 12 && t ing in to CASE IDLE: CHK_CMD: WRITE: READ_ADD: READ_DATA: default: ns = IDLE; if (SS_n) else ing in to IF if (SS_n) else begin//SS_n = 0
113 final_countries final_coun	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	16000 gin 4000 All False Counts of 2 branches = 100.00% CASE Branch 92914 Count coming 16006 11967 25982 15981 22977 1 stof 6 branches = 100.00% IF Branch	ing in to IF if (state_count >= 12 && t ing in to CASE IDLE: CHK_CMD: WRITE: READ_ADD: READ_DATA: default: ns = IDLE; if (SS_n) else ing in to IF if (SS_n) else begin//SS_n = 0
113 final_countries final_coun	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	16000 gin 4000 All False Coun s of 2 branches = 100.00% CASE Branch 92914 Count comi 16006 11967 25982 15981 22977 1 s of 6 branches = 100.00% IF Branch 16006 Count comi 8006 8000 s of 2 branches = 100.00% IF Branch	ing in to IF if (state_count >= 12 && t ing in to CASE IDLE: CHK_CMD: WRITE: READ_ADD: READ_DATA: default: ns = IDLE; ing in to IF if (SS_n) else else begin//SS_n = 0

```
-----IF Branch-----
                 6013 Count coming in to IF
 147
 147
                   4013
                                                            if (!flag_rd) //flag_rd = 0
 149
       1
                   2000
                                                            else //flag_rd = 1
Branch totals: 2 hits of 2 branches = 100.00%
      -----IF Branch-----
                25982 Count coming in to IF
 154
 154 1 4000
156 1 21982
                                                  if (SS n)
                                                  else
Branch totals: 2 hits of 2 branches = 100.00%
         -----IF Branch-----
                15981 Count coming in to IF
 159
 159 1
                  2000
                                                  if (SS_n)
 161 1 13981
                                                  else begin
Branch totals: 2 hits of 2 branches = 100.00%
      -----IF Branch-----
 166
            22977 Count coming in to IF
      1 2000
1 20977
 166
                                                  if (SS_n)
 168 1
                                                  else begin
Branch totals: 2 hits of 2 branches = 100.00%
Condition Coverage:
  Enabled Coverage
                         Bins Covered Misses Coverage
  Conditions
                     14 10 4 71.42%
Condition Coverage for instance /\top#DUT /DUT_2 --
File SPI_Slave.sv
-----Focused Condition View-----
Line 36 Item 1 (cs == 0)
Condition totals: 1 of 1 input term covered = 100.00%
Input Term Covered Reason for no coverage Hint
 (cs == 0) Y
 Rows: Hits FEC Target Non-masking condition(s)
Row 1: 1 (cs == 0)_0
Row 2: 1 (cs == 0)_1
-----Focused Condition View-----
Line 60 Item 1 (state_count < 10)
Condition totals: 1 of 1 input term covered = 100.00%
   Input Term Covered Reason for no coverage Hint
(state_count < 10) Y
  Rows: Hits FEC Target Non-masking condition(s)
Row 1: 1 (state_count < 10)_0 -
Row 2: 1 (state_count < 10)_1 -
-----Focused Condition View------
Line 63 Item 1 (~PO[9] && (state_count == 10))
Condition totals: 1 of 2 input terms covered = 50.00%
```

```
Input Term Covered Reason for no coverage Hint
     PO[9] N '_1' not hit Hit '_1'
(state_count == 10) Y
  Rows: Hits FEC Target
                           Non-masking condition(s)
Row 1: 1 PO[9]_0 (state_count == 10)
Row 2: ***0*** PO[9] 1
Row 3: 1 (state_count == 10)_0 ~PO[9]
Row 4: 1 (state_count == 10)_1 ~PO[9]
-----Focused Condition View------
Line 75 Item 1 (state_count < 10)
Condition totals: 1 of 1 input term covered = 100.00%
    Input Term Covered Reason for no coverage Hint
(state_count < 10) Y
  Rows: Hits FEC Target Non-masking condition(s)
Row 1: 1 (state_count < 10)_0 -
Row 2: 1 (state_count < 10)_1 -
-----Focused Condition View------
Line 80 Item 1 ((PO[9:8] == 2) && (state_count == 10))
Condition totals: 1 of 2 input terms covered = 50.00%
    Input Term Covered Reason for no coverage Hint
   (PO[9:8] == 2) Y
(state_count == 10) N '_0' not hit Hit '_0'
  Rows: Hits FEC Target Non-masking condition(s)
Row 1: 1 (PO[9:8] == 2)_0 -
Row 2: 1 (PO[9:8] == 2)_1 (state_count == 10)
Row 3: ***0*** (state_count == 10)_0 (PO[9:8] == 2)
Row 4: 1 (state_count == 10)_1 (PO[9:8] == 2)
------Focused Condition View------
Line 90 Item 1 (state_count < 9)
Condition totals: 1 of 1 input term covered = 100.00%
   Input Term Covered Reason for no coverage Hint
(state_count < 9) Y
  Rows: Hits FEC Target Non-masking condition(s)
Row 1: 1 (state count < 9) 0 -
Row 2: 1 (state_count < 9)_1 -
-----Focused Condition View-----
Line 101 Item 1 ((PO[9:8] == 3) && (state_count == 10))
Condition totals: 1 of 2 input terms covered = 50.00%
    Input Term Covered Reason for no coverage Hint
   (PO[9:8] == 3) Y
(state_count == 10) N '_0' not hit Hit '_0'
  Rows: Hits FEC Target Non-masking condition(s)
Row 1: 1 (PO[9:8] == 3)_0 -
```

```
Row 2: 1 (PO[9:8] == 3)_1 (state_count == 10)
 Row 3: ***0*** (state count == 10) 0 (PO[9:8] == 3)
Row 4: 1 (state_count == 10)_1 (PO[9:8] == 3)
-----Focused Condition View-----
Line 110 Item 1 (tx_valid && (state_count == 12))
Condition totals: 1 of 2 input terms covered = 50.00%
    Input Term Covered Reason for no coverage Hint
     tx_valid Y
 (state_count == 12) N '_0' not hit
                                Hit ' 0'
  Rows: Hits FEC Target
                         Non-masking condition(s)
Row 1: 1 tx_valid_0 -
Row 2: 1 tx_valid_1 (state_count == 12)
 Row 3: ***0*** (state_count == 12)_0 tx_valid
 Row 4: 1 (state_count == 12)_1 tx_valid
------Focused Condition View------
Line 113 Item 1 ((state count >= 12) && (final count <= 7))
Condition totals: 2 of 2 input terms covered = 100.00%
    Input Term Covered Reason for no coverage Hint
 (state_count >= 12) Y
 (final_count <= 7)
  Rows: Hits FEC Target Non-masking condition(s)
 Row 1:
         1 (state_count >= 12)_0 -
 Row 2:
           1 (state_count >= 12)_1 (final_count <= 7)
          1 (final_count <= 7)_0 (state_count >= 12)
 Row 3:
         1 (final_count <= 7)_1 (state_count >= 12)
 Row 4:
FSM Coverage:
 Enabled Coverage Bins Hits Misses Coverage
 -----
 FSM States
                   5 5 0 100.00%
                    8 7 1 87.50%
 FSM Transitions
FSM Coverage for instance /\top#DUT /DUT_2 --
FSM ID: cs
 Current State Object : cs
 State Value MapInfo:
                    Value
Line State Name
      -----
       IDLE
135
140 CHK_CMD 1
165 READ_DATA 4
158
      READ_ADD
                         3
153
         WRITE
 Covered States :
        State
                Hit count
                   8012
        IDLE
                  8000
       CHK_CMD
      READ_DATA
```

```
READ_ADD
                                                       22000
                    WRITE
                                                  44000
   Covered Transitions:
                    Trans_ID
                                                 Hit_count
                                                                                Transition
Line
                                                8000
                                                                  IDLE -> CHK_CMD
139
                            O
                                                2000
                                                                     CHK CMD -> READ DATA
150
                            1
                                                2000
                                                                     CHK CMD -> READ ADD
148
                                                                     CHK_CMD -> WRITE
                                                4000
145
                            3
                            5
                                                2000
                                                                     READ_DATA -> IDLE
167
160
                            6
                                                2000
                                                                      READ ADD -> IDLE
155
                            7
                                                4000
                                                                      WRITE -> IDLE
   Uncovered Transitions :
                   Trans_ID
                                                Transition
142
                            4
                                          CHK_CMD -> IDLE
                                                Bins Hits Misses Coverage
   Summary
       FSM States
                                                  5 5 0 100.00%
       FSM Transitions
                                                     8 7 1 87.50%
Statement Coverage:
   Enabled Coverage
                                                 Bins Hits Misses Coverage
                                                  67 66 1 98.50%
   Statements
Statement Coverage for instance /\top#DUT /DUT_2 --
   Line
                  Item
                                                      Count Source
 File SPI_Slave.sv
                                                            module \ SPI\_Slave\_wrapper \ (MOSI, SS\_n, clk, rst\_n, tx\_data, tx\_valid, MISO, table \ and table \ a
   1
rx_data, rx_valid);
                                                                  parameter IDLE = 0;
   3
                                                                  parameter CHK_CMD = 1;
   4
                                                                  parameter WRITE = 2;
   5
                                                                  parameter READ_ADD = 3;
   6
                                                                  parameter READ_DATA = 4;
   7
   8
                                                                 input MOSI, SS_n, clk, rst_n, tx_valid;
   9
                                                                  input [7:0] tx_data;
   10
                                                                  output MISO;
                                                                  output reg rx_valid;
   11
   12
                                                                  output [9:0] rx_data;
   13
   14
                                                                  reg [2:0] cs, ns;//current state and next state
   15
                                                                 reg [9:0] PO;
   16
                                                                  reg [7:0] temp;
   17
                                                                 reg SO, flag_rd;
                                                                 integer state_count = 0, final_count = 0;
   18
   19
                                                                  reg Act_input_output;
   20
   21
                                                                  assign MISO = SO; // output of reading
   22
                                                                  assign rx_data = PO;
   23
                                                            // state Memory
                                                 122012
                                                                                        always @(posedge clk ) begin //bug : reset must be syncrouns not
   24
                        1
Async
   25
                                                                                        if (!rst_n)begin
   26
                        1
                                                      12
                                                                                                              cs <= IDLE;
   27
                        1
                                                      12
                                                                                            flag_rd<=0;
    28
                                                      12
                                                                                            final_count <= 32'hFFFF_FFFF;
```

```
29
                                           state_count <=32'hFFFF_FFFF;
           1
                          12
 30
           1
                          12
                                           temp <= 0;
 31
                                         end
 32
                                         else
 33
                       122000
           1
                                                      cs <= ns;
 34
 35
           1
                        24001
                                         always @ (cs)begin
 36
                                         if (cs == IDLE)begin
 37
           1
                         8001
                                                              rx valid = 0;
                                                      PO = 0;
 38
                         8001
           1
 39
           1
                         8001
                                                      state_count = 0;
 40
           1
                         8001
                                                      final_count = 0;
                         8001
                                                      SO = 0;
 41
           1
                         8001
 42
                                                      Act_input_output = 0;
           1
 43
                                         end
 44
                               end
 45
 46
           1
                       122012
                                         always @(posedge clk) begin//* bug
 47
 48
                                         case (cs)
 49
                                                     IDLE : begin
 50
 51
           1
                         8011
                                                              rx_valid = 0;
                         8011
                                                        PO = 0;
 52
           1
 53
           1
                         8011
                                                        state_count = 0;
 54
           1
                         8011
                                                        final_count = 0;
 55
                         8011
                                                        SO = 0;
           1
 56
           1
                         8011
                                                        Act_input_output = 0;
 57
                                                end
 58
                                            WRITE: begin //done
 59
 60
                                                              if (state_count < 10 )begin //0,
                        40000
                                                                                   PO = \{PO[8:0], MOSI\};
 61
           1
                        40000
 62
           1
                                                                                   state_count =
state count + 1;
 63
                                                                         if (PO[9] ==1'b0 && state_count
==10)begin
 64
           1
                         4000
                                                                                     rx_valid = 1;
 65
                                                                end
 66
                                                                else
                                                                                   rx_valid = 0;
 67
           1
                        36000
 68
                                                              end
 69
                                                              else
                         4000
 70
           1
                                                                                   rx_valid = 0;
 71
 72
                                                        end
 73
                                            READ_ADD: begin // done
 74
 75
                                                    if (state_count<10 )begin
                        20000
 76
           1
                                                                         PO = \{PO[8:0], MOSI\};
 77
           1
                        20000
                                                                         state_count = state_count + 1;
 78
           1
                        20000
                                                                         rx_valid = 0;
 79
                                                    if (PO[9:8]==2'b10 && state_count==10)begin
 80
 81
           1
                         4000
                                                                         rx_valid = 1;
 82
           1
                         4000
                                                                         flag_rd = 1;
 83
                                                    end
 84
                                                    else
 85
           1
                        18000
                                                                                   rx_valid = 0;
 86
                                                          end
 87
                                            READ_DATA: begin // done
 88
 89
                                                    if (Act_input_output == 0)begin
 90
                                                              if (state_count<9 )begin
 91
                        18000
                                                                           PO = {PO[8:0], MOSI};
           1
 92
                        18000
                                                                           state_count = state_count + 1;
```

```
93
           1
                        18000
                                                                          rx_valid = 0;
 94
                                                     end
 95
                                                     else begin
                        2000
 96
           1
                                                                        PO = \{PO[8:0], MOSI\};
 97
           1
                        2000
                                                                          state_count = state_count + 1;
 98
           1
                        2000
                                                                          rx_valid = 0;
 99
                                                     end
 100
 101
                                                     if (PO[9:8]==2'b11 && state_count== 10 )begin
                         2000
 102
            1
                                                                          rx_valid = 1;
 103
                         2000
                                                                          Act_input_output = 1;
           1
 104
                         2000
                                                                          flag_rd = 0;
 105
                                                     end
 106
                                                   end
 107
                                                   else begin
 108
            1
                        20000
                                                                        state_count = state_count + 1;
                        20000
 109
            1
                                                                        rx_valid = 0;
 110
                                                             if (tx_valid && state_count == 12 )begin
 111
            1
                         2000
                                                                                  temp = tx_data;
                                                             end
 112
 113
                                                             if (state_count >= 12 && final_count <=
7)begin
 114
                        16000
                                                                                    SO = temp [7 -
final_count];
 115
                        16000
                                                                                    rx_valid =0;
            1
 116
                        16000
                                                                                    final_count =
final_count + 1;
 117
                                                               end
 118
                                                             end
 119
                                                         end
 120
                                            default: begin
                                                             rx_valid = 0;
 121
                         8001
            1
                         8001
 122
            1
                                                       PO = 0;
                         8001
 123
           1
                                                       state_count = 0;
                                                       final_count = 0;
                         8001
 124
           1
 125
            1
                         8001
                                                       SO = 0;
                         8001
 126
            1
                                                       Act_input_output = 0;
 127
 128
                                              end
 129
                                            endcase
 130
                              end
 131
 132
            1
                        92914
                                         always @(*) begin
 133
 134
                                         case (cs)
 135
                                           IDLE:
 136
                                                     if (SS_n)
                         8006
 137
            1
                                                                 ns = IDLE;
 138
                                                     else
                         8000
                                                                 ns = CHK\_CMD;
 139
            1
 140
                                           CHK_CMD:
 141
                                                     if (SS_n)
                       ***0***
                                                                 ns = IDLE;
 142
            1
                                                     else begin//SS_n = 0
 143
 144
                                                       if (MOSI==0) //MOSI = 0
 145
            1
                         5954
                                                                            ns = WRITE;
                                                       else begin //MOSI = 1
 146
 147
                                                                 if (!flag_rd) //flag_rd = 0
 148
            1
                         4013
                                                                              ns = READ_ADD;
 149
                                                                  else //flag_rd = 1
 150
                         2000
                                                                              ns = READ_DATA;
            1
 151
                                                       end
 152
                                                     end
                                           WRITE:
 153
 154
                                                     if (SS_n)
 155
                         4000
                                                                 ns = IDLE;
```

```
156
                                    else
 157
                21982
                                             ns = WRITE;
 158
                             READ_ADD:
                                    if (SS_n)
 159
                 2000
 160
        1
                                             ns = IDLE;
 161
                                    else begin
        1
                13981
                                             ns = READ\_ADD;
 162
 163
                                     // flag_rd = 1;
 164
                                    end
                             READ_DATA:
 165
 166
                                    if (SS_n)
 167
                 2000
                                             ns = IDLE;
        1
 168
                                    else begin
                20977
                                             ns = READ_DATA;
 169
        1
 170
                                     // flag_rd = 0;
 171
                                    end
 172
 173
        1
                  1
                             default: ns = IDLE;
Toggle Coverage:
 Enabled Coverage
                            Hits Misses Coverage
 Toggles
                  232
                        232
                               0 100.00%
Toggle Coverage for instance /\top#DUT /DUT_2 --
                Node 1H->0L 0L->1H
                                         "Coverage"
                                           100.00
            Act_input_output
                           1
                MISO
                       1
                            1
                                       100.00
                MOSI
                       1
                           1
                                       100.00
                     1
                                       100.00
               PO[9-0]
                          1
                SO
                           1
                                      100.00
                SS_n
                                      100.00
                     1
                          1
                clk
                                      100.00
                      1
                          1
               cs[2-0]
                      1
                                       100.00
                                          100.00
           final_count[31-0]
                          1
               flag_rd
                                       100.00
                     1
                           1
               ns[2-0]
                                       100.00
               rst_n
                      1
                           1
                                      100.00
             rx_data[0-9]
                        1 1
                                        100.00
                                       100.00
              rx_valid
                       1
                           1
           state_count[31-0]
                                          100.00
                                        100.00
              temp[7-0]
                        1
                             1
                           1
             tx_data[0-7]
                                        100.00
                        1
              tx valid
                                       100.00
Total Node Count = 116
Toggled Node Count = 116
Untoggled Node Count =
Toggle Coverage = 100.00% (232 of 232 bins)
______
=== Instance: /\top#DUT
=== Design Unit: work.SPI_Wrapper
______
Toggle Coverage:
                 Bins Hits Misses Coverage
 Enabled Coverage
                      0 100.00%
 Toggles
              68
                 68
```

Toggle Coverage for instance /\top#DUT --"Coverage" Node 1H->0L 0L->1H MISO MOSI 1 100.00 1 SS n 1 1 100.00 100.00 rst_n 1 1 100.00 100.00 100.00 100.00 100.00 100.00 tx_valid_wrapper 1 1 100.00 Total Node Count = 34 Toggled Node Count = Untoggled Node Count = Toggle Coverage = 100.00% (68 of 68 bins) Total Coverage By Instance (filtered view): 92.55% I saw that I didn't need to use assertion because I got what I want in checking with scoreboard....... **Assertions**



♣ Function coverage report For RAM and wrapper

```
Coverage Report by instance with details
=== Instance: /RAM_coverage_pkg
=== Design Unit: work.RAM_coverage_pkg
Covergroup Coverage:
  Covergroups
                                      na 100.00%
    Coverpoints/Crosses
                          12
                                 na
                                                 na
      Covergroup Bins
                          655
                                 655
                                          0 100.00%
Covergroup
                         Metric Goal Bins Status
TYPE /RAM_coverage_pkg/RAM_coverage/cvr_gp
                                       100.00% 100 - Covered
 covered/total bins:
                           655 655
                           0 655
 missing/total bins:
 % Hit:
                     100.00% 100
 Coverpoint reset
                         100.00% 100

    Covered
```

```
covered/total bins:
                                       2
                                             2
   missing/total bins:
                                      0
                                             2
   % Hit:
                              100.00%
                                          100
 Coverpoint data_valid
                                     100.00%
                                                  100

    Covered

   covered/total bins:
                                             9
                                      9
   missing/total bins:
                                      0
                                             9
                              100.00%
   % Hit:
                                          100
 Coverpoint data written
                                      100.00%
                                                   100
                                                            - Covered
   covered/total bins:
                                      64
                                             64
   missing/total bins:
                                      0
                                            64
                              100.00%
   % Hit:
                                          100
                                      100.00%
                                                  100
 Coverpoint data read
                                                              Covered
   covered/total bins:
                                      64
                                             64
   missing/total bins:
                                      0
                                            64
                              100.00%
   % Hit:
                                          100
 Coverpoint address_written
                                        100.00%
                                                     100
                                                                Covered
   covered/total bins:
                                      64
                                             64
   missing/total bins:
                                      0
                                            64
   % Hit:
                              100.00%
                                          100
 Coverpoint address_read
                                       100.00%
                                                    100
                                                               Covered
   covered/total bins:
                                      64
                                             64
   missing/total bins:
                                            64
   % Hit:
                              100.00%
                                          100
 Coverpoint receive_valid
                                      100.00%
                                                   100
                                                            - Covered
   covered/total bins:
                                      2
                                             2
   missing/total bins:
                                      0
                              100.00%
   % Hit:
                                          100
 Coverpoint send_valid
                                      100.00%
                                                  100
                                                           - Covered
   covered/total bins:
                                      2
   missing/total bins:
                                      0
                                             2
                              100.00%
                                          100
   % Hit:
 Cross Writing_address
                                      100.00%
                                                  100
                                                              Covered
   covered/total bins:
                                      128
                                             128
   missing/total bins:
                                      0
                                            128
   % Hit:
                              100.00%
                                          100
 Cross Writing_data
                                    100.00%
                                                100
                                                            Covered
   covered/total bins:
                                      128
                                             128
   missing/total bins:
                                      0
                                            128
   % Hit:
                              100.00%
                                          100
 Cross reading_address
                                      100.00%
                                                  100
                                                             Covered
   covered/total bins:
                                      64
                                             64
   missing/total bins:
                                      0
                                            64
   % Hit:
                              100.00%
                                          100
 Cross reading_data
                                    100.00%
                                                100
                                                            Covered
   covered/total bins:
                                      64
                                             64
   missing/total bins:
                                      0
                                            64
                              100.00%
   % Hit:
                                          100
Covergroup\ instance\ \bigvee RAM\_coverage\_pkg::RAM\_coverage::cvr\_gp
                            100.00%
                                        100
                                                   Covered
 covered/total bins:
                                      655
                                             655
 missing/total bins:
                                            655
                                      O
 % Hit:
                              100.00%
                                          100
 Coverpoint reset
                                   100.00%
                                               100
                                                           Covered
   covered/total bins:
                                      2
                                             2
   missing/total bins:
                                      0
   % Hit:
                              100.00%
                                          100
   bin reset_asserted
                                      12
                                              1
                                                       Covered
   bin reset disable
                                   122000
                                                         Covered
 Coverpoint data_valid
                                     100.00%
                                                  100
                                                             Covered
   covered/total bins:
                                       9
                                             9
   missing/total bins:
                                      O
   % Hit:
                              100.00%
                                          100
   bin writing_complete
                                       6000
                                                 1
                                                       - Covered
   bin writing
                                 94012
                                                     Covered
                                            1
   bin reading
                                  2000
                                                     Covered
                                            1
   bin change_wr_rd
                                      2000
                                                         Covered
```

```
2000
                                              1
 bin change_rd_wr
                                                       Covered
 bin default values[0]
                                    94012
                                              1
                                                        Covered
 bin default_values[1]
                                    6000
                                              1
                                                       Covered
 bin default_values[2]
                                    2000
                                              1
                                                       Covered
 bin default_values[3]
                                    20000
                                               1
                                                        Covered
Coverpoint data_written
                                     100.00%
                                                 100
                                                            Covered
 covered/total bins:
                                    64
                                           64
 missing/total bins:
                                    0
                                          64
 % Hit:
                            100.00%
                                        100
 bin auto[0:3]
                               116107
                                            1
                                                     Covered
 bin auto[4:7]
                                  94
                                                   Covered
                                         1
 bin auto[8:11]
                                  95
                                          1
                                                   Covered
 bin auto[12:15]
                                   95
                                          1
                                                    Covered
                                   95
 bin auto[16:19]
                                          1
                                                    Covered
 bin auto[20:23]
                                   95
                                                    Covered
                                           1
 bin auto[24:27]
                                   93
                                                    Covered
                                   93
 bin auto[28:31]
                                          1
                                                    Covered
 bin auto[32:35]
                                   93
                                          1
                                                    Covered
 bin auto[36:39]
                                   94
                                                    Covered
                                           1
                                   95
 bin auto[40:43]
                                          1
                                                    Covered
 bin auto[44:47]
                                   96
                                                    Covered
                                          1
                                   95
 bin auto[48:51]
                                          1
                                                    Covered
 bin auto[52:55]
                                   94
                                                    Covered
                                   93
 bin auto[56:59]
                                          1
                                                    Covered
 bin auto[60:63]
                                   95
                                                    Covered
                                           1
 bin auto[64:67]
                                   92
                                                    Covered
                                   94
 bin auto[68:71]
                                           1
                                                    Covered
                                   92
 bin auto[72:75]
                                                    Covered
                                           1
 bin auto[76:79]
                                   92
                                                    Covered
 bin auto[80:83]
                                   95
                                           1
                                                    Covered
 bin auto[84:87]
                                   91
                                           1
                                                    Covered
 bin auto[88:91]
                                   96
                                           1
                                                    Covered
 bin auto[92:95]
                                   92
                                                    Covered
 bin auto[96:99]
                                   93
                                           1
                                                    Covered
 bin auto[100:103]
                                    95
                                                     Covered
                                            1
 bin auto[104:107]
                                    91
                                                     Covered
                                    94
 bin auto[108:111]
                                            1
                                                     Covered
 bin auto[112:115]
                                    93
                                                     Covered
                                            1
 bin auto[116:119]
                                    94
                                                     Covered
 bin auto[120:123]
                                    90
                                            1
                                                     Covered
 bin auto[124:127]
                                    95
                                                     Covered
                                            1
                                    91
                                                     Covered
 bin auto[128:131]
                                            1
 bin auto[132:135]
                                    94
                                            1
                                                     Covered
 bin auto[136:139]
                                    93
                                            1
                                                     Covered
 bin auto[140:143]
                                    91
                                                     Covered
                                            1
 bin auto[144:147]
                                    91
                                                     Covered
                                    95
 bin auto[148:151]
                                            1
                                                     Covered
                                    94
 bin auto[152:155]
                                            1
                                                     Covered
 bin auto[156:159]
                                    95
                                                     Covered
 bin auto[160:163]
                                    93
                                            1
                                                     Covered
 bin auto[164:167]
                                    92
                                            1
                                                     Covered
 bin auto[168:171]
                                    95
                                            1
                                                     Covered
 bin auto[172:175]
                                    95
                                            1
                                                     Covered
 bin auto[176:179]
                                    95
                                                     Covered
                                            1
 bin auto[180:183]
                                    93
                                                     Covered
                                            1
 bin auto[184:187]
                                    93
                                                     Covered
 bin auto[188:191]
                                    92
                                            1
                                                     Covered
 bin auto[192:195]
                                    93
                                                     Covered
                                            1
 bin auto[196:199]
                                    93
                                            1
                                                     Covered
 bin auto[200:203]
                                    94
                                            1
                                                     Covered
                                    95
 bin auto[204:207]
                                            1
                                                     Covered
                                                     Covered
 bin auto[208:211]
                                    94
 bin auto[212:215]
                                    92
                                            1
                                                     Covered
                                    94
 bin auto[216:219]
                                            1
                                                     Covered
 bin auto[220:223]
                                    95
                                                     Covered
                                            1
 bin auto[224:227]
                                    96
                                                     Covered
```

```
bin auto[228:231]
                                    96
                                           1
                                                     Covered
 bin auto[232:235]
                                    93
                                           1
                                                     Covered
 bin auto[236:239]
                                    95
                                                     Covered
 bin auto[240:243]
                                    96
                                           1
                                                     Covered
 bin auto[244:247]
                                    94
                                                     Covered
                                           1
 bin auto[248:251]
                                    95
                                                     Covered
                                    94
 bin auto[252:255]
                                           1
                                                     Covered
                                   100.00%
                                                        - Covered
Coverpoint data read
                                                100
 covered/total bins:
                                    64
                                           64
 missing/total bins:
                                    0
                                          64
                            100.00%
 % Hit:
                                        100
 bin auto[0:3]
                                27817
                                           1
                                                    Covered
 bin auto[4:7]
                                1361
                                          1
                                                   Covered
 bin auto[8:11]
                                 1475
                                           1
                                                    Covered
 bin auto[12:15]
                                 1536
                                                    Covered
                                           1
 bin auto[16:19]
                                 1536
                                                     Covered
 bin auto[20:23]
                                                     Covered
                                 1536
                                           1
 bin auto[24:27]
                                 1536
                                                     Covered
                                           1
 bin auto[28:31]
                                 1440
                                                     Covered
                                           1
 bin auto[32:35]
                                 1475
                                           1
                                                     Covered
 bin auto[36:39]
                                 1501
                                                     Covered
                                           1
 bin auto[40:43]
                                 1536
                                           1
                                                     Covered
 bin auto[44:47]
                                 1536
                                                     Covered
 bin auto[48:51]
                                 1536
                                           1
                                                     Covered
 bin auto[52:55]
                                 1536
                                                     Covered
                                           1
 bin auto[56:59]
                                 1485
                                                     Covered
                                           1
 bin auto[60:63]
                                 1389
                                           1
                                                     Covered
 bin auto[64:67]
                                 1274
                                                     Covered
                                           1
 bin auto[68:71]
                                 1501
                                           1
                                                     Covered
 bin auto[72:75]
                                 1590
                                           1
                                                     Covered
                                 1335
 bin auto[76:79]
                                                     Covered
                                           1
 bin auto[80:83]
                                 1536
                                           1
                                                     Covered
 bin auto[84:87]
                                 1536
                                                     Covered
 bin auto[88:91]
                                 1536
                                           1
                                                     Covered
 bin auto[92:95]
                                 1536
                                                     Covered
                                           1
 bin auto[96:99]
                                 1256
                                                     Covered
 bin auto[100:103]
                                   1536
                                             1
                                                      Covered
 bin auto[104:107]
                                   1536
                                                      Covered
                                             1
 bin auto[108:111]
                                   1501
                                             1
                                                      Covered
 bin auto[112:115]
                                   1536
                                             1
                                                      Covered
 bin auto[116:119]
                                   1424
                                             1
                                                      Covered
 bin auto[120:123]
                                   1493
                                             1
                                                      Covered
 bin auto[124:127]
                                   1536
                                             1
                                                      Covered
 bin auto[128:131]
                                   1475
                                             1
                                                      Covered
 bin auto[132:135]
                                   1475
                                             1
                                                      Covered
 bin auto[136:139]
                                   1676
                                             1
                                                      Covered
 bin auto[140:143]
                                   1344
                                             1
                                                      Covered
                                   1440
 bin auto[144:147]
                                             1
                                                      Covered
 bin auto[148:151]
                                   1536
                                             1
                                                      Covered
 bin auto[152:155]
                                   1354
                                             1
                                                      Covered
 bin auto[156:159]
                                   1536
                                             1
                                                      Covered
 bin auto[160:163]
                                   1475
                                             1
                                                      Covered
 bin auto[164:167]
                                   1641
                                             1
                                                      Covered
 bin auto[168:171]
                                   1536
                                             1
                                                      Covered
 bin auto[172:175]
                                   1501
                                             1
                                                      Covered
 bin auto[176:179]
                                   1536
                                             1
                                                      Covered
 bin auto[180:183]
                                   1440
                                             1
                                                      Covered
 bin auto[184:187]
                                   1501
                                             1
                                                      Covered
 bin auto[188:191]
                                   1536
                                             1
                                                      Covered
 bin auto[192:195]
                                   1616
                                             1
                                                      Covered
 bin auto[196:199]
                                   1536
                                             1
                                                      Covered
 bin auto[200:203]
                                   1641
                                             1
                                                      Covered
 bin auto[204:207]
                                   1451
                                             1
                                                      Covered
 bin auto[208:211]
                                   1536
                                             1
                                                      Covered
                                   1353
                                             1
 bin auto[212:215]
                                                      Covered
 bin auto[216:219]
                                   1396
                                                      Covered
```

```
bin auto[220:223]
                                   1501
                                             1
                                                      Covered
 bin auto[224:227]
                                   1536
                                             1
                                                      Covered
 bin auto[228:231]
                                   1536
                                             1
                                                      Covered
 bin auto[232:235]
                                   1536
                                             1
                                                      Covered
 bin auto[236:239]
                                   1440
                                             1
                                                      Covered
 bin auto[240:243]
                                   1536
                                                      Covered
 bin auto[244:247]
                                   1536
                                             1
                                                      Covered
                                   1501
 bin auto[248:251]
                                             1
                                                      Covered
 bin auto[252:255]
                                   1466
                                                      Covered
Coverpoint address_written
                                      100.00%
                                                  100
                                                           - Covered
 covered/total bins:
                                    64
                                          64
                                          64
 missing/total bins:
                                    0
 % Hit:
                            100.00%
                                        100
 bin auto[0:3]
                                75986
                                           1
                                                    Covered
 bin auto[4:7]
                                 7969
                                          1
                                                   Covered
 bin auto[8:11]
                                 3969
                                                    Covered
 bin auto[12:15]
                                  3969
                                           1
                                                    Covered
 bin auto[16:19]
                                  1980
                                                     Covered
                                            1
 bin auto[20:23]
                                  1957
                                                     Covered
                                            1
 bin auto[24:27]
                                  1959
                                            1
                                                     Covered
 bin auto[28:31]
                                  1979
                                                     Covered
                                           1
                                  976
 bin auto[32:35]
                                           1
                                                    Covered
 bin auto[36:39]
                                  972
                                                    Covered
 bin auto[40:43]
                                  962
                                           1
                                                    Covered
 bin auto[44:47]
                                  964
                                                    Covered
                                           1
 bin auto[48:51]
                                  963
                                                    Covered
                                           1
                                  964
 bin auto[52:55]
                                           1
                                                    Covered
                                  969
                                                    Covered
 bin auto[56:59]
                                           1
 bin auto[60:63]
                                  978
                                                    Covered
                                           1
 bin auto[64:67]
                                  473
                                           1
                                                    Covered
 bin auto[68:71]
                                  471
                                                    Covered
                                           1
 bin auto[72:75]
                                  468
                                           1
                                                    Covered
 bin auto[76:79]
                                  472
                                           1
                                                    Covered
 bin auto[80:83]
                                  464
                                           1
                                                    Covered
 bin auto[84:87]
                                  468
                                                    Covered
                                           1
 bin auto[88:91]
                                  468
                                                    Covered
                                  464
 bin auto[92:95]
                                           1
                                                    Covered
 bin auto[96:99]
                                  463
                                                    Covered
                                           1
 bin auto[100:103]
                                   468
                                            1
                                                     Covered
 bin auto[104:107]
                                   469
                                            1
                                                     Covered
 bin auto[108:111]
                                   465
                                                     Covered
                                            1
                                   468
 bin auto[112:115]
                                            1
                                                     Covered
 bin auto[116:119]
                                   469
                                            1
                                                     Covered
 bin auto[120:123]
                                   474
                                                     Covered
                                            1
 bin auto[124:127]
                                   473
                                                     Covered
                                            1
 bin auto[128:131]
                                   220
                                                      Covered
 bin auto[132:135]
                                   222
                                            1
                                                     Covered
 bin auto[136:139]
                                   221
                                            1
                                                     Covered
 bin auto[140:143]
                                   218
                                                     Covered
 bin auto[144:147]
                                   219
                                            1
                                                     Covered
 bin auto[148:151]
                                   220
                                            1
                                                     Covered
 bin auto[152:155]
                                   221
                                            1
                                                     Covered
 bin auto[156:159]
                                   219
                                            1
                                                     Covered
 bin auto[160:163]
                                   217
                                                     Covered
                                            1
 bin auto[164:167]
                                   216
                                                     Covered
                                            1
 bin auto[168:171]
                                   218
                                                     Covered
 bin auto[172:175]
                                   218
                                            1
                                                     Covered
 bin auto[176:179]
                                   220
                                                     Covered
                                            1
 bin auto[180:183]
                                   217
                                            1
                                                      Covered
 bin auto[184:187]
                                   217
                                            1
                                                     Covered
 bin auto[188:191]
                                   215
                                            1
                                                     Covered
                                                     Covered
 bin auto[192:195]
                                   216
                                            1
 bin auto[196:199]
                                   216
                                            1
                                                     Covered
 bin auto[200:203]
                                   218
                                            1
                                                     Covered
 bin auto[204:207]
                                   219
                                                     Covered
                                            1
 bin auto[208:211]
                                    215
                                                     Covered
```

```
bin auto[212:215]
                                    222
                                                      Covered
                                            1
                                    219
 bin auto[216:219]
                                            1
                                                     Covered
 bin auto[220:223]
                                    216
                                                     Covered
 bin auto[224:227]
                                    216
                                            1
                                                     Covered
 bin auto[228:231]
                                    221
                                                      Covered
                                            1
 bin auto[232:235]
                                    217
                                                      Covered
 bin auto[236:239]
                                    221
                                            1
                                                      Covered
 bin auto[240:243]
                                    222
                                                     Covered
                                            1
 bin auto[244:247]
                                    220
                                                      Covered
 bin auto[248:251]
                                    222
                                            1
                                                     Covered
                                    221
 bin auto[252:255]
                                            1
                                                     Covered
                                     100.00%
                                                          - Covered
Coverpoint address read
                                                  100
 covered/total bins:
                                    64
                                           64
 missing/total bins:
                                    0
                                          64
                            100.00%
 % Hit:
                                        100
 bin auto[0:3]
                               120043
                                                     Covered
 bin auto[4:7]
                                  32
                                         1
                                                  Covered
 bin auto[8:11]
                                  32
                                                   Covered
                                          1
 bin auto[12:15]
                                   31
                                                    Covered
                                          1
 bin auto[16:19]
                                   32
                                           1
                                                    Covered
 bin auto[20:23]
                                   32
                                                    Covered
                                          1
                                   32
 bin auto[24:27]
                                          1
                                                    Covered
 bin auto[28:31]
                                   32
                                                    Covered
 bin auto[32:35]
                                   32
                                           1
                                                    Covered
 bin auto[36:39]
                                   31
                                                    Covered
                                           1
 bin auto[40:43]
                                   32
                                                    Covered
 bin auto[44:47]
                                   31
                                           1
                                                    Covered
 bin auto[48:51]
                                   32
                                                    Covered
                                           1
 bin auto[52:55]
                                   29
                                                    Covered
 bin auto[56:59]
                                   32
                                           1
                                                    Covered
 bin auto[60:63]
                                   31
                                          1
                                                    Covered
 bin auto[64:67]
                                   32
                                           1
                                                    Covered
 bin auto[68:71]
                                   30
                                           1
                                                    Covered
 bin auto[72:75]
                                   30
                                          1
                                                    Covered
 bin auto[76:79]
                                   32
                                                    Covered
                                           1
 bin auto[80:83]
                                   31
                                                    Covered
                                   32
 bin auto[84:87]
                                           1
                                                    Covered
 bin auto[88:91]
                                   32
                                                    Covered
                                           1
 bin auto[92:95]
                                   32
                                                    Covered
 bin auto[96:99]
                                   32
                                           1
                                                    Covered
 bin auto[100:103]
                                    31
                                            1
                                                     Covered
 bin auto[104:107]
                                                     Covered
                                    32
                                            1
 bin auto[108:111]
                                    30
                                            1
                                                     Covered
 bin auto[112:115]
                                    31
                                            1
                                                     Covered
 bin auto[116:119]
                                    31
                                                     Covered
                                            1
 bin auto[120:123]
                                    32
                                                     Covered
                                    32
 bin auto[124:127]
                                            1
                                                     Covered
 bin auto[128:131]
                                    31
                                            1
                                                     Covered
 bin auto[132:135]
                                    32
                                                     Covered
 bin auto[136:139]
                                    31
                                            1
                                                     Covered
 bin auto[140:143]
                                    31
                                            1
                                                     Covered
 bin auto[144:147]
                                    31
                                            1
                                                     Covered
 bin auto[148:151]
                                    30
                                            1
                                                     Covered
 bin auto[152:155]
                                    31
                                                     Covered
                                            1
 bin auto[156:159]
                                    31
                                                     Covered
                                            1
 bin auto[160:163]
                                    32
                                                     Covered
 bin auto[164:167]
                                    32
                                            1
                                                     Covered
 bin auto[168:171]
                                    30
                                            1
                                                     Covered
 bin auto[172:175]
                                    30
                                            1
                                                     Covered
 bin auto[176:179]
                                    32
                                            1
                                                     Covered
 bin auto[180:183]
                                    32
                                            1
                                                     Covered
 bin auto[184:187]
                                    30
                                                     Covered
 bin auto[188:191]
                                    31
                                            1
                                                     Covered
 bin auto[192:195]
                                    31
                                            1
                                                     Covered
 bin auto[196:199]
                                    32
                                                     Covered
                                            1
 bin auto[200:203]
                                    32
                                                     Covered
```

```
bin auto[204:207]
                                     31
                                            1
                                                      Covered
 bin auto[208:211]
                                     28
                                                     Covered
                                            1
 bin auto[212:215]
                                     31
                                                     Covered
 bin auto[216:219]
                                     32
                                            1
                                                     Covered
 bin auto[220:223]
                                     30
                                                     Covered
                                            1
 bin auto[224:227]
                                     31
                                                      Covered
 bin auto[228:231]
                                     31
                                            1
                                                     Covered
 bin auto[232:235]
                                     31
                                            1
                                                     Covered
 bin auto[236:239]
                                                      Covered
 bin auto[240:243]
                                     30
                                            1
                                                     Covered
 bin auto[244:247]
                                     32
                                            1
                                                      Covered
 bin auto[248:251]
                                     32
                                                      Covered
 bin auto[252:255]
                                     31
                                            1
                                                      Covered
Coverpoint receive_valid
                                     100.00%
                                                 100

    Covered

 covered/total bins:
                                     2
                                           2
 missing/total bins:
                                     0
                                           2
                            100.00%
 % Hit:
                                         100
 bin receive_asserted
                                     8000
                                                        Covered
                                              1
 bin receive_disable
                                   114012
                                               1
Coverpoint send_valid
                                    100.00%
                                                100
                                                         - Covered
 covered/total bins:
                                     2
                                           2
 missing/total bins:
 % Hit:
                            100.00%
 bin send_asserted
                                    2000
                                                       Covered
 bin send_disable
                                  120012
                                                        Covered
Cross Writing_address
                                                         - Covered
                                    100.00%
 covered/total bins:
                                    128
                                           128
                                          128
 missing/total bins:
                                     0
                            100.00%
                                         100
 Auto, Default and User Defined Bins:
   bin <auto[252:255],receive_disable>
                                            189
                                                     1
                                                              Covered
    bin <auto[248:251],receive_disable>
                                            190
                                                     1
                                                              Covered
    bin <auto[244:247],receive_disable>
                                            188
                                                     1
                                                              Covered
   bin <auto[240:243],receive_disable>
                                            192
                                                     1
                                                              Covered
   bin <auto[236:239],receive_disable>
                                            189
                                                              Covered
                                                     1
    bin <auto[232:235],receive_disable>
                                            186
                                                              Covered
                                            189
    bin <auto[228:231],receive_disable>
                                                     1
                                                              Covered
                                            186
                                                              Covered
    bin <auto[224:227],receive_disable>
                                                     1
    bin <auto[220:223],receive_disable>
                                            185
                                                     1
                                                              Covered
    bin <auto[216:219],receive_disable>
                                            188
                                                     1
                                                              Covered
                                                              Covered
    bin <auto[212:215],receive_disable>
                                            190
                                                     1
                                                              Covered
    bin <auto[208:211],receive_disable>
                                            185
                                                     1
    bin <auto[204:207],receive_disable>
                                            189
                                                     1
                                                              Covered
    bin <auto[200:203],receive_disable>
                                            186
                                                     1
                                                              Covered
    bin <auto[196:199],receive_disable>
                                            184
                                                     1
                                                              Covered
    bin <auto[192:195],receive_disable>
                                            185
                                                     1
                                                              Covered
   bin <auto[188:191],receive_disable>
                                            185
                                                     1
                                                              Covered
   bin <auto[184:187],receive_disable>
                                            187
                                                     1
                                                              Covered
   bin <auto[180:183], receive disable>
                                            185
                                                              Covered
   bin <auto[176:179],receive_disable>
                                            188
                                                     1
                                                              Covered
    bin <auto[172:175],receive_disable>
                                            188
                                                              Covered
                                                     1
    bin <auto[168:171],receive disable>
                                            186
                                                     1
                                                              Covered
   bin <auto[164:167],receive_disable>
                                            184
                                                     1
                                                              Covered
                                                              Covered
   bin <auto[160:163],receive_disable>
                                            186
                                                     1
   bin <auto[156:159],receive_disable>
                                            188
                                                              Covered
   bin <auto[152:155],receive_disable>
                                            189
                                                              Covered
   bin <auto[148:151],receive_disable>
                                            191
                                                     1
                                                              Covered
    bin <auto[144:147],receive disable>
                                            187
                                                     1
                                                              Covered
    bin <auto[140:143],receive_disable>
                                            186
                                                     1
                                                              Covered
   bin <auto[136:139],receive_disable>
                                            190
                                                     1
                                                              Covered
   bin <auto[132:135],receive_disable>
                                            190
                                                     1
                                                              Covered
    bin <auto[128:131],receive disable>
                                            189
                                                              Covered
    bin <auto[124:127],receive_disable>
                                            443
                                                              Covered
    bin <auto[120:123],receive_disable>
                                            442
                                                     1
                                                              Covered
    bin <auto[116:119],receive_disable>
                                            438
                                                              Covered
                                                     1
   bin <auto[112:115],receive_disable>
                                            437
                                                              Covered
```

bin <auto[108:111],receive_disable></auto[108:111],receive_disable>	435	1	-	
bin <auto[104:107],receive_disable></auto[104:107],receive_disable>	437	1	-	
bin <auto[100:103],receive_disable></auto[100:103],receive_disable>	437	1	-	
bin <auto[96:99],receive_disable></auto[96:99],receive_disable>	432	1	-	Covered
bin <auto[92:95],receive_disable></auto[92:95],receive_disable>	432	1	-	Covered
bin <auto[88:91],receive_disable></auto[88:91],receive_disable>	437	1	-	Covered
bin <auto[84:87],receive_disable></auto[84:87],receive_disable>	436	1	-	Covered
bin <auto[80:83],receive_disable></auto[80:83],receive_disable>	433	1	-	Covered
bin <auto[76:79],receive_disable></auto[76:79],receive_disable>	440	1	-	Covered
bin <auto[72:75],receive_disable></auto[72:75],receive_disable>	439	1	-	Covered
bin <auto[68:71],receive_disable></auto[68:71],receive_disable>	439	1	-	Covered
bin <auto[64:67],receive disable=""></auto[64:67],receive>	442	1	-	Covered
bin <auto[60:63],receive_disable></auto[60:63],receive_disable>	947	1	_	
bin <auto[66:59],receive_disable></auto[66:59],receive_disable>	937	1	_	Covered
bin <auto[50:55],receive_disable></auto[50:55],receive_disable>	934	1	_	Covered
	934	1	-	Covered
bin <auto[48:51],receive_disable></auto[48:51],receive_disable>			-	
bin <auto[44:47],receive_disable></auto[44:47],receive_disable>	932	1	-	Covered
bin <auto[40:43],receive_disable></auto[40:43],receive_disable>	932	1	-	Covered
bin <auto[36:39],receive_disable></auto[36:39],receive_disable>	940	1	-	Covered
bin <auto[32:35],receive_disable></auto[32:35],receive_disable>	944	1	-	Covered
bin <auto[28:31],receive_disable></auto[28:31],receive_disable>	1947	1	-	
bin <auto[24:27],receive_disable></auto[24:27],receive_disable>	1927	1	-	Covered
bin <auto[20:23],receive_disable></auto[20:23],receive_disable>	1926	1	-	Covered
bin <auto[16:19],receive_disable></auto[16:19],receive_disable>	1948	1	-	Covered
bin <auto[12:15],receive_disable></auto[12:15],receive_disable>	3938	1	-	Covered
bin <auto[8:11],receive_disable></auto[8:11],receive_disable>	3937	1	_	Covered
bin <auto[4:7],receive_disable></auto[4:7],receive_disable>	7938	1	_	Covered
	69955	1	_	Covered
bin <auto[0.3],receive_disable></auto[0.3],receive_disable>	32	1	٠.	
bin <auto[232.253], receive_asserted=""></auto[232.253],>	32	1	_	
			_	
bin <auto[244:247],receive_asserted></auto[244:247],receive_asserted>	32	1		00.0.00
bin <auto[240:243],receive_asserted></auto[240:243],receive_asserted>	30	1	-	
bin <auto[236:239],receive_asserted></auto[236:239],receive_asserted>	32	1	-	
bin <auto[232:235],receive_asserted></auto[232:235],receive_asserted>	31	1	-	
bin <auto[228:231],receive_asserted></auto[228:231],receive_asserted>	32	1	-	
bin <auto[224:227],receive_asserted></auto[224:227],receive_asserted>	30	1	-	0010.00
bin <auto[220:223],receive_asserted></auto[220:223],receive_asserted>	31	1	-	Covered
bin <auto[216:219],receive_asserted></auto[216:219],receive_asserted>	31	1	-	Covered
bin <auto[212:215],receive_asserted></auto[212:215],receive_asserted>	32	1	-	Covered
bin <auto[208:211],receive_asserted></auto[208:211],receive_asserted>	30	1	-	Covered
bin <auto[204:207],receive_asserted></auto[204:207],receive_asserted>	30	1	-	
bin <auto[200:203],receive_asserted></auto[200:203],receive_asserted>	32	1	-	
bin <auto[196:199],receive_asserted></auto[196:199],receive_asserted>	32	1	_	
bin <auto[192:195],receive_asserted></auto[192:195],receive_asserted>	31	1	_	Covered
	30	1	-	- Covered
bin <auto[188:191],receive_asserted> bin <auto[184:187],receive_asserted></auto[184:187],receive_asserted></auto[188:191],receive_asserted>			-	- Covered
	30	1	-	
bin <auto[180:183],receive_asserted></auto[180:183],receive_asserted>	32	1	-	Covered
bin <auto[176:179],receive_asserted></auto[176:179],receive_asserted>	32	1	-	0010.00
bin <auto[172:175],receive_asserted></auto[172:175],receive_asserted>	30	1	-	Covered
bin <auto[168:171],receive_asserted></auto[168:171],receive_asserted>	32	1	-	Covered
bin <auto[164:167],receive_asserted></auto[164:167],receive_asserted>	32	1	-	
bin <auto[160:163],receive_asserted></auto[160:163],receive_asserted>	31	1	-	Covered
bin <auto[156:159],receive_asserted></auto[156:159],receive_asserted>	31	1	-	Covered
bin <auto[152:155],receive_asserted></auto[152:155],receive_asserted>	32	1	-	Covered
bin <auto[148:151],receive_asserted></auto[148:151],receive_asserted>	29	1	-	Covered
bin <auto[144:147],receive_asserted></auto[144:147],receive_asserted>	32	1	_	
bin <auto[144:147],receive_asserted></auto[144:147],receive_asserted>	32	1	_	Covered
bin <auto[140.143],receive_asserted></auto[140.143],receive_asserted>	31	1		- Covered
	32		_	
bin <auto[132:135],receive_asserted></auto[132:135],receive_asserted>		1	-	
bin <auto[128:131],receive_asserted></auto[128:131],receive_asserted>	31	1	-	Covered
bin <auto[124:127],receive_asserted></auto[124:127],receive_asserted>	30	1	-	00.0.00
bin <auto[120:123],receive_asserted></auto[120:123],receive_asserted>	32	1	-	Covered
bin <auto[116:119],receive_asserted></auto[116:119],receive_asserted>	31	1	-	Covered
bin <auto[112:115],receive_asserted></auto[112:115],receive_asserted>	31	1	-	Covered
bin <auto[108:111],receive_asserted></auto[108:111],receive_asserted>	30	1	-	Covered
bin <auto[104:107],receive_asserted></auto[104:107],receive_asserted>	32	1	-	Covered
		_		

```
bin <auto[100:103],receive_asserted>
                                             31
                                                           - Covered
    bin <auto[96:99],receive asserted>
                                                            Covered
    bin <auto[92:95],receive_asserted>
                                                             Covered
    bin <auto[88:91],receive_asserted>
                                            31
                                                   1
                                                            Covered
    bin <auto[84:87],receive_asserted>
                                            32
                                                   1
                                                             Covered
    bin <auto[80:83],receive_asserted>
                                            31
                                                   1
                                                             Covered
    bin <auto[76:79],receive_asserted>
                                            32
                                                   1
                                                             Covered
                                                          - Covered
    bin <auto[72:75],receive asserted>
                                            29
                                                   1
    bin <auto[68:71],receive asserted>
                                                             Covered
    bin <auto[64:67],receive_asserted>
                                            31
                                                   1
                                                            Covered
    bin <auto[60:63],receive_asserted>
                                            31
                                                   1
                                                             Covered
    bin <auto[56:59],receive asserted>
                                            32
                                                   1
                                                             Covered
    bin <auto[52:55],receive_asserted>
                                            30
                                                   1
                                                             Covered
                                                          - Covered
    bin <auto[48:51],receive_asserted>
                                            32
                                                   1
    bin <auto[44:47],receive_asserted>
                                                   1
                                                          - Covered
    bin <auto[40:43],receive_asserted>
                                                          - Covered
    bin <auto[36:39],receive_asserted>
                                            32
                                                   1

    Covered

    bin <auto[32:35],receive_asserted>
                                            32
                                                   1
                                                             Covered
    bin <auto[28:31],receive_asserted>
                                            32
                                                   1
                                                             Covered
    bin <auto[24:27],receive_asserted>
                                            32
                                                   1
                                                             Covered
    bin <auto[20:23],receive_asserted>
                                                             Covered
                                            31
                                                   1
    bin <auto[16:19],receive asserted>
                                                             Covered
    bin <auto[12:15],receive_asserted>
                                                             Covered
    bin <auto[8:11],receive_asserted>
                                           32
                                                   1
                                                            Covered
                                          31
                                                           Covered
    bin <auto[4:7],receive_asserted>
                                                  1
                                          6031
    bin <auto[0:3],receive_asserted>
                                                             Covered
Cross Writing_data
                                             100
                                  100.00%
                                                         Covered
                                   128
 covered/total bins:
                                           128
 missing/total bins:
                                          128
 % Hit:
                            100.00%
                                         100
 Auto, Default and User Defined Bins:
    bin <auto[252:255],receive_disable>
                                            62
                                                    1
                                                             Covered
    bin <auto[248:251],receive_disable>
                                             63
                                                             Covered
    bin <auto[244:247],receive_disable>
                                            62
                                                    1
                                                             Covered
    bin <auto[240:243],receive_disable>
                                                             Covered
    bin <auto[236:239],receive_disable>
                                                             Covered
                                            61
    bin <auto[232:235],receive_disable>
                                                    1
                                                             Covered
    bin <auto[228:231],receive_disable>
                                                             Covered
                                            64
                                                    1
    bin <auto[224:227],receive_disable>
                                                             Covered
    bin <auto[220:223],receive_disable>
                                            64
                                                    1
                                                             Covered
    bin <auto[216:219],receive_disable>
                                            63
                                                             Covered
                                                    1
    bin <auto[212:215],receive_disable>
                                                             Covered
    bin <auto[208:211],receive_disable>
                                                    1
                                                             Covered
    bin <auto[204:207],receive_disable>
                                            63
                                                    1
                                                             Covered
    bin <auto[200:203],receive_disable>
                                            63
                                                    1
                                                             Covered
    bin <auto[196:199],receive_disable>
                                            61
                                                             Covered
    bin <auto[192:195],receive_disable>
                                            62
                                                    1
                                                             Covered
    bin <auto[188:191], receive disable>
                                            60
                                                    1
                                                             Covered
    bin <auto[184:187], receive disable>
                                                             Covered
    bin <auto[180:183],receive_disable>
                                            62
                                                             Covered
    bin <auto[176:179],receive_disable>
                                            64
                                                    1
                                                             Covered
    bin <auto[172:175],receive disable>
                                            63
                                                             Covered
    bin <auto[168:171],receive_disable>
                                            63
                                                             Covered
    bin <auto[164:167],receive_disable>
                                            61
                                                             Covered
    bin <auto[160:163], receive disable>
                                                             Covered
    bin <auto[156:159],receive_disable>
                                                             Covered
    bin <auto[152:155],receive_disable>
                                            63
                                                    1
                                                             Covered
    bin <auto[148:151],receive disable>
                                            63
                                                             Covered
                                                    1
    bin <auto[144:147],receive_disable>
                                                             Covered
    bin <auto[140:143],receive_disable>
                                            62
                                                    1
                                                             Covered
    bin <auto[136:139],receive_disable>
                                            62
                                                    1
                                                             Covered
    bin <auto[132:135],receive disable>
                                                             Covered
    bin <auto[128:131],receive_disable>
                                            61
                                                             Covered
    bin <auto[124:127],receive_disable>
                                            63
                                                    1
                                                             Covered
    bin <auto[120:123],receive_disable>
                                            62
                                                             Covered
                                                    1
    bin <auto[116:119],receive_disable>
                                                             Covered
```

```
bin <auto[112:115],receive_disable>
                                                1
                                                         Covered
bin <auto[108:111],receive disable>
                                        62
                                                         Covered
bin <auto[104:107],receive_disable>
                                        59
                                                         Covered
                                        63
bin <auto[100:103],receive_disable>
                                               1
                                                         Covered
bin <auto[96:99],receive_disable>
                                       63
                                                        Covered
                                              1
bin <auto[92:95],receive_disable>
                                       61
                                                        Covered
bin <auto[88:91],receive_disable>
                                       64
                                              1
                                                        Covered
                                                     - Covered
bin <auto[84:87],receive_disable>
                                       60
                                              1
bin <auto[80:83], receive disable>
                                                        Covered
bin <auto[76:79],receive_disable>
                                       62
                                              1
                                                        Covered
bin <auto[72:75],receive_disable>
                                       61
                                              1
                                                        Covered
bin <auto[68:71],receive disable>
                                       62
                                              1
                                                        Covered
bin <auto[64:67],receive_disable>
                                       63
                                              1
                                                        Covered
bin <auto[60:63],receive_disable>
                                       64
                                              1
                                                        Covered
bin <auto[56:59],receive_disable>
                                       62
                                                       Covered
                                              1
bin <auto[52:55],receive_disable>
                                                     - Covered
bin <auto[48:51],receive_disable>
                                       63
                                                       Covered
                                              1
bin <auto[44:47],receive_disable>
                                       64
                                                        Covered
                                              1
bin <auto[40:43],receive_disable>
                                       63
                                                        Covered
bin <auto[36:39],receive_disable>
                                       62
                                              1
                                                        Covered
bin <auto[32:35],receive_disable>
                                       62
                                                        Covered
                                              1
bin <auto[28:31],receive disable>
                                                        Covered
bin <auto[24:27],receive_disable>
                                                        Covered
bin <auto[20:23],receive_disable>
                                       63
                                              1
                                                        Covered
bin <auto[16:19],receive_disable>
                                       63
                                                        Covered
                                              1
bin <auto[12:15],receive_disable>
                                       64
                                                        Covered
                                                    - Covered
bin <auto[8:11],receive_disable>
                                      64
                                              1
bin <auto[4:7],receive_disable>
                                      63
                                                    - Covered
bin <auto[0:3],receive_disable>
                                                         Covered
bin <auto[252:255],receive_asserted>
                                                 1
                                                         Covered
                                         32
bin <auto[248:251],receive_asserted>
                                                1
                                                         Covered
bin <auto[244:247],receive_asserted>
                                         32
                                                 1
                                                          Covered
bin <auto[240:243],receive_asserted>
                                         32
                                                 1
                                                          Covered
bin <auto[236:239],receive_asserted>
                                         31
                                                 1
                                                          Covered
                                                          Covered
bin <auto[232:235],receive_asserted>
                                                1
bin <auto[228:231],receive_asserted>
                                                         Covered
                                                         Covered
bin <auto[224:227],receive_asserted>
                                         32
                                                1
                                                         Covered
bin <auto[220:223],receive_asserted>
                                         31
                                                1
bin <auto[216:219],receive_asserted>
                                                          Covered
bin <auto[212:215],receive_asserted>
                                         29
                                                 1
                                                         Covered
                                                         Covered
bin <auto[208:211],receive_asserted>
                                         31
                                                1
                                                          Covered
bin <auto[204:207],receive_asserted>
bin <auto[200:203],receive_asserted>
                                         31
                                                 1
                                                         Covered
bin <auto[196:199],receive_asserted>
                                         32
                                                1
                                                       - Covered
bin <auto[192:195],receive_asserted>
                                         31
                                                         Covered
                                                 1
bin <auto[188:191],receive_asserted>
                                         32
                                                 1
                                                          Covered
                                                         Covered
bin <auto[184:187],receive_asserted>
                                         32
                                                 1
                                                         Covered
bin <auto[180:183],receive asserted>
                                         31
                                                1
bin <auto[176:179],receive asserted>
                                                          Covered
bin <auto[172:175],receive_asserted>
                                                 1
                                                         Covered
                                         32
                                                         Covered
bin <auto[168:171],receive_asserted>
                                                1
bin <auto[164:167],receive asserted>
                                         31
                                                1
                                                          Covered
bin <auto[160:163],receive_asserted>
                                         31
                                                 1
                                                         Covered
bin <auto[156:159],receive_asserted>
                                         32
                                                         Covered
                                                1
bin <auto[152:155],receive_asserted>
                                                         Covered
bin <auto[148:151],receive_asserted>
                                                         Covered
bin <auto[144:147],receive_asserted>
                                         30
                                                1
                                                       - Covered
bin <auto[140:143],receive asserted>
                                         29
                                                         Covered
                                                1
bin <auto[136:139],receive_asserted>
                                         31
                                                          Covered
bin <auto[132:135],receive_asserted>
                                         31
                                                 1
                                                         Covered
                                                         Covered
bin <auto[128:131],receive_asserted>
                                         30
                                                1
                                                          Covered
bin <auto[124:127],receive asserted>
bin <auto[120:123],receive_asserted>
                                         28
                                                 1
                                                         Covered
bin <auto[116:119],receive_asserted>
                                         31
                                                 1
                                                          Covered
                                         31
                                                          Covered
bin <auto[112:115],receive_asserted>
                                                 1
bin <auto[108:111],receive_asserted>
                                                          Covered
```

```
bin <auto[104:107],receive_asserted>
                                             32
                                                              Covered
                                                    1
    bin <auto[100:103],receive asserted>
                                             32
                                                              Covered
    bin <auto[96:99],receive_asserted>
                                            30
                                                    1
                                                             Covered
    bin <auto[92:95],receive_asserted>
                                            31
                                                   1
                                                             Covered
    bin <auto[88:91],receive_asserted>
                                            32
                                                   1
                                                             Covered
    bin <auto[84:87],receive_asserted>
                                            31
                                                   1
                                                             Covered
   bin <auto[80:83],receive_asserted>
                                            31
                                                   1
                                                             Covered
   bin <auto[76:79],receive asserted>
                                            30
                                                   1
                                                             Covered
   bin <auto[72:75],receive asserted>
                                                             Covered
   bin <auto[68:71],receive_asserted>
                                            32
                                                   1
                                                             Covered
    bin <auto[64:67],receive_asserted>
                                            29
                                                   1
                                                             Covered
    bin <auto[60:63],receive asserted>
                                            31
                                                   1
                                                             Covered
   bin <auto[56:59],receive_asserted>
                                            31
                                                   1
                                                             Covered
   bin <auto[52:55],receive_asserted>
                                            32
                                                   1
                                                             Covered
   bin <auto[48:51],receive asserted>
                                                             Covered
                                                   1
   bin <auto[44:47],receive_asserted>
                                            32
                                                             Covered
   bin <auto[40:43],receive_asserted>
                                            32
                                                   1
                                                             Covered
    bin <auto[36:39],receive_asserted>
                                            32
                                                   1
                                                             Covered
    bin <auto[32:35],receive_asserted>
                                            31
                                                   1
                                                             Covered
   bin <auto[28:31],receive_asserted>
                                            30
                                                   1
                                                             Covered
   bin <auto[24:27],receive_asserted>
                                            32
                                                             Covered
                                                   1
   bin <auto[20:23],receive asserted>
                                                             Covered
    bin <auto[16:19],receive_asserted>
                                                             Covered
    bin <auto[12:15],receive_asserted>
                                            31
                                                   1
                                                             Covered
                                           31
                                                            Covered
    bin <auto[8:11],receive_asserted>
                                                  1
    bin <auto[4:7],receive_asserted>
                                           31
                                                           Covered
   bin <auto[0:3],receive_asserted>
                                          6032
                                                   1

    Covered

                                    100.00%
Cross reading_address
                                                100
                                                         - Covered
 covered/total bins:
                                           64
 missing/total bins:
                                    0
                                          64
 % Hit:
                            100.00%
                                        100
 Auto, Default and User Defined Bins:
   bin <auto[252:255],receive_asserted>
                                             31
                                                              Covered
   bin <auto[124:127],receive_asserted>
                                             32
                                                     1
                                                              Covered
   bin <auto[188:191],receive_asserted>
                                                              Covered
                                             31
                                                    1
    bin <auto[60:63],receive_asserted>
                                                             Covered
    bin <auto[220:223],receive_asserted>
                                             30
                                                    1

    Covered

    bin <auto[92:95],receive_asserted>
                                            32
                                                    1
                                                             Covered
    bin <auto[156:159],receive_asserted>
                                                              Covered
                                                          - Covered
   bin <auto[28:31],receive_asserted>
                                            32
    bin <auto[236:239],receive_asserted>
                                                           - Covered
                                             32
                                                    1
    bin <auto[108:111],receive_asserted>
                                                              Covered
    bin <auto[172:175],receive_asserted>
                                             30
                                                              Covered
    bin <auto[44:47],receive_asserted>
                                            31
                                                    1

    Covered

    bin <auto[204:207],receive asserted>
                                             31
                                                              Covered
                                                    1
    bin <auto[76:79],receive_asserted>
                                            32
                                                            Covered
   bin <auto[140:143],receive_asserted>
                                             31
                                                    1
                                                           - Covered
                                                          - Covered
   bin <auto[12:15],receive asserted>
                                            31
                                                   1
    bin <auto[244:247],receive asserted>
                                                              Covered
   bin <auto[116:119],receive_asserted>
                                             31
                                                    1
                                                              Covered
    bin <auto[180:183],receive_asserted>
                                             32
                                                              Covered
                                                    1
    bin <auto[52:55],receive asserted>
                                            29
                                                             Covered
   bin <auto[212:215],receive_asserted>
                                             31
                                                    1

    Covered

   bin <auto[84:87],receive_asserted>
                                                          - Covered
                                            32
                                                    1
   bin <auto[148:151], receive asserted>
                                                           - Covered
   bin <auto[20:23],receive_asserted>
                                            32
                                                          - Covered
   bin <auto[228:231],receive_asserted>
                                             31
                                                    1

    Covered

    bin <auto[100:103],receive asserted>
                                             31
                                                              Covered
                                                    1
    bin <auto[164:167],receive_asserted>
                                             32
                                                              Covered
   bin <auto[36:39],receive_asserted>
                                            31
                                                          - Covered
   bin <auto[196:199],receive_asserted>
                                             32

    Covered

    bin <auto[68:71],receive asserted>
                                                             Covered
    bin <auto[132:135],receive_asserted>
                                             32
                                                              Covered
    bin <auto[4:7],receive_asserted>
                                           32
                                                           Covered
    bin <auto[248:251],receive_asserted>
                                             32
                                                           - Covered
                                                    1
   bin <auto[120:123],receive_asserted>
                                                              Covered
```

```
bin <auto[184:187],receive_asserted>
                                             30
                                                           - Covered
    bin <auto[56:59],receive asserted>
                                            32
                                                    1
                                                            Covered
    bin <auto[216:219],receive_asserted>
                                             32
                                                              Covered
    bin <auto[88:91],receive_asserted>
                                            32
                                                    1

    Covered

    bin <auto[152:155],receive_asserted>
                                             31
                                                              Covered
                                                    1
    bin <auto[24:27],receive_asserted>
                                            32
                                                             Covered
   bin <auto[232:235],receive_asserted>
                                             31
                                                    1
                                                              Covered
   bin <auto[104:107],receive asserted>
                                             32
                                                    1
                                                              Covered
   bin <auto[168:171],receive asserted>
                                                              Covered
   bin <auto[40:43],receive_asserted>
                                            32
                                                    1
                                                          - Covered
    bin <auto[200:203],receive_asserted>
                                             32
                                                    1
                                                              Covered
    bin <auto[72:75],receive asserted>
                                            30
                                                            Covered
   bin <auto[136:139],receive_asserted>
                                             31
                                                     1
                                                              Covered
                                                         - Covered
   bin <auto[8:11],receive_asserted>
                                           32
   bin <auto[240:243],receive asserted>
                                             30
                                                           - Covered
   bin <auto[112:115],receive_asserted>
                                                              Covered
   bin <auto[176:179],receive_asserted>
                                             32
                                                    1
                                                              Covered
    bin <auto[48:51],receive_asserted>
                                            32
                                                            Covered
                                                    1
    bin <auto[208:211],receive_asserted>
                                             28
                                                              Covered
   bin <auto[80:83],receive_asserted>
                                            31
                                                    1
                                                          - Covered
   bin <auto[144:147],receive_asserted>

    Covered

                                             31
                                                    1
   bin <auto[16:19],receive asserted>
                                            32
                                                          - Covered
    bin <auto[224:227],receive_asserted>
                                                           - Covered
    bin <auto[96:99],receive_asserted>
                                            32
                                                    1
                                                            Covered
    bin <auto[160:163],receive_asserted>
                                                              Covered
                                             32
                                                    1
    bin <auto[32:35],receive_asserted>
                                                             Covered
   bin <auto[192:195],receive_asserted>
                                             31
                                                    1

    Covered

    bin <auto[64:67],receive_asserted>
                                                          - Covered
                                            32
                                                    1
    bin <auto[128:131],receive_asserted>
                                             31
                                                             Covered
   bin <auto[0:3],receive_asserted>
                                          6031
                                                    1
                                                          - Covered
 Illegal and Ignore Bins:
   ignore_bin ignore_bin1
                                    114012
                                                         Occurred
Cross reading_data
                                  100.00%
                                               100
                                                          Covered
 covered/total bins:
                                    64
                                           64
 missing/total bins:
                                    0
                                          64
 % Hit:
                            100.00%
                                        100
 Auto, Default and User Defined Bins:
    bin <auto[252:255],receive_asserted>
                                                           - Covered
                                             92
                                                     1
    bin <auto[124:127],receive_asserted>
                                                     1
                                                              Covered
   bin <auto[188:191],receive_asserted>
                                             96
                                                     1
                                                              Covered
    bin <auto[60:63],receive_asserted>
                                                            Covered
                                            86
    bin <auto[220:223],receive_asserted>
                                                              Covered
    bin <auto[92:95],receive_asserted>
                                            96
                                                          - Covered
    bin <auto[156:159],receive_asserted>
                                                              Covered
                                             96
                                                    1
    bin <auto[28:31],receive asserted>
                                            90
                                                            Covered
    bin <auto[236:239],receive_asserted>
                                             90
                                                              Covered
   bin <auto[108:111],receive_asserted>
                                             94
                                                     1
                                                              Covered
   bin <auto[172:175],receive asserted>
                                             94
                                                              Covered
                                                    1
   bin <auto[44:47],receive asserted>
                                            96
                                                            Covered
   bin <auto[204:207],receive_asserted>
                                             90
                                                    1
                                                           - Covered
    bin <auto[76:79],receive_asserted>
                                            84
                                                    1
                                                            Covered
    bin <auto[140:143],receive asserted>
                                                              Covered
   bin <auto[12:15],receive_asserted>
                                            96
                                                            Covered
   bin <auto[244:247],receive_asserted>
                                             96
                                                    1

    Covered

   bin <auto[116:119],receive asserted>
                                                              Covered
   bin <auto[180:183],receive_asserted>
                                             90
                                                              Covered
   bin <auto[52:55],receive_asserted>
                                            96
                                                          - Covered
    bin <auto[212:215],receive asserted>
                                             84
                                                              Covered
                                                    1
    bin <auto[84:87],receive_asserted>
                                            96
                                                            Covered
   bin <auto[148:151],receive_asserted>
                                             96
                                                    1
                                                              Covered
   bin <auto[20:23],receive_asserted>
                                            96
                                                    1
                                                          - Covered
    bin <auto[228:231],receive asserted>
                                                              Covered
    bin <auto[100:103],receive_asserted>
                                             96
                                                              Covered
    bin <auto[164:167],receive_asserted>
                                             102
                                                               Covered
                                            94
    bin <auto[36:39],receive_asserted>
                                                            Covered
   bin <auto[196:199],receive_asserted>
                                                              Covered
```

```
bin <auto[68:71],receive_asserted>
                                           94
                                                 1
                                                       - Covered
     bin <auto[132:135],receive asserted>
                                            92
                                                         - Covered
     bin <auto[4:7],receive_asserted>
                                                      - Covered
     bin <auto[248:251],receive_asserted>
                                            94
                                                  1

    Covered

     bin <auto[120:123],receive_asserted>
                                            92
                                                        - Covered
                                                  1
      bin <auto[184:187],receive_asserted>
                                            94
                                                           Covered
     bin <auto[56:59],receive_asserted>
                                           92
                                                  1
                                                       - Covered
     bin <auto[216:219],receive asserted>
                                           88
                                                        - Covered
                                                  1
     bin <auto[88:91],receive asserted>
                                           96
                                                       - Covered
     bin <auto[152:155],receive_asserted>
                                            84
                                                  1

    Covered

     bin <auto[24:27],receive_asserted>
                                           96
                                                 1
                                                       - Covered
      bin <auto[232:235],receive asserted>
                                            96
                                                  1
                                                        - Covered
     bin <auto[104:107],receive_asserted>
                                            96
                                                  1
                                                        - Covered
     bin <auto[168:171],receive_asserted>
                                            96
                                                  1

    Covered

     bin <auto[40:43],receive asserted>
                                           96
                                                       - Covered
     bin <auto[200:203],receive_asserted>
                                           102
                                                         - Covered
                                           98
                                                       - Covered
     bin <auto[72:75],receive_asserted>
                                                 1
     bin <auto[136:139],receive_asserted>
                                           104
                                                         - Covered
                                                   1
      bin <auto[8:11],receive_asserted>
                                                       - Covered
                                          92
     bin <auto[240:243],receive_asserted>
                                            96
                                                  1
                                                        - Covered
     bin <auto[112:115],receive_asserted>
                                           96
                                                        - Covered
                                                  1
     bin <auto[176:179],receive asserted>
                                                        - Covered
     bin <auto[48:51],receive_asserted>
                                           96
                                                       - Covered
     bin <auto[208:211],receive_asserted>
                                           96
                                                 1

    Covered

      bin <auto[80:83],receive_asserted>
                                           96
                                                  1
                                                       - Covered
      bin <auto[144:147],receive_asserted>
                                            90

    Covered

                                                       - Covered
     bin <auto[16:19],receive_asserted>
                                           96
     bin <auto[224:227],receive_asserted>
                                           96

    Covered

                                                  1
                                                       - Covered
      bin <auto[96:99],receive_asserted>
     bin <auto[160:163],receive_asserted>
                                            92
                                                  1
                                                        - Covered
      bin <auto[32:35],receive_asserted>
                                           92
                                                       - Covered
                                                 1
      bin <auto[192:195],receive_asserted>
                                           100
                                                           Covered
                                                   1
      bin <auto[64:67],receive_asserted>
                                           80
                                                       - Covered
     bin <auto[128:131],receive_asserted>
                                           92
                                                  1
                                                         - Covered
     bin <auto[0:3],receive_asserted>
                                                          Covered
                                        2118
                                                 1
    Illegal and Ignore Bins:
                                    114012
                                                     - Occurred
     ignore_bin ignore_bin1
______
=== Instance: /SPI_coverage_pkg
=== Design Unit: work.SPI_coverage_pkg
Covergroup Coverage:
  Covergroups
                                       na
                                               na 100.00%
     Coverpoints/Crosses
                                    15
                                            na
                                                     na
                                                             na
        Covergroup Bins
                                 522
                                          522
                                                     0 100.00%
Covergroup
                               Metric
                                        Goal
                                                Bins Status
TYPE /SPI_coverage_pkg/SPI_coverage/SPI_Wrapper
                                                 100.00%
                                                            100
                                                                    - Covered
  covered/total bins:
                                   522
                                          522
  missing/total bins:
                                   0
                                        522
                            100.00%
                                       100
  % Hit:
  Coverpoint reset
                                100.00%
                                            100
                                                      Covered
   covered/total bins:
                                   2
   missing/total bins:
                                   0
                                         2
                            100.00%
   % Hit:
                                       100
  Coverpoint Address_write
                                    100.00%
                                                100
                                                        - Covered
   covered/total bins:
                                   64
                                         64
   missing/total bins:
                                   0
                                         64
    % Hit:
                                       100
```

```
100.00%
                                                  100
                                                           - Covered
 Coverpoint Data_write
   covered/total bins:
                                      64
                                             64
   missing/total bins:
                                      0
                                            64
                                          100
   % Hit:
                              100.00%
 Coverpoint Data_read
                                     100.00%
                                                  100
                                                           - Covered
   covered/total bins:
                                      64
                                             64
   missing/total bins:
                                      0
                                            64
                              100.00%
   % Hit:
                                          100
 Coverpoint Address read
                                       100.00%
                                                               Covered
                                                    100
   covered/total bins:
                                      64
                                             64
   missing/total bins:
                                      O
                                            64
                              100.00%
                                          100
   % Hit:
 Coverpoint Send_Address_wr
                                          100.00%
                                                      100
                                                               - Covered
   covered/total bins:
                                      1
                                            1
   missing/total bins:
                                      0
                                            1
   % Hit:
                              100.00%
                                          100
                                         100.00%
 Coverpoint Send_Address_rd
                                                      100
                                                                 Covered
   covered/total bins:
                                      1
                                             1
   missing/total bins:
                              100.00%
   % Hit:
                                          100
 Coverpoint send_Data_wr
                                        100.00%
                                                    100
                                                                Covered
   covered/total bins:
                                      1
                                             1
   missing/total bins:
   % Hit:
                              100.00%
                                          100
 Coverpoint Recieving_Data_rd
                                                      100
                                         100.00%
                                                                 Covered
   covered/total bins:
                                      1
                                             1
   missing/total bins:
                                      0
                                            1
   % Hit:
                              100.00%
                                          100
 Coverpoint Sending_order_Read_data
                                              100.00%
                                                          100
                                                                     Covered
   covered/total bins:
                                      1
                                             1
   missing/total bins:
                                      0
                                            1
                              100.00%
   % Hit:
                                          100
 Coverpoint Starting_Communication
                                            100.00%
                                                         100
                                                                    Covered
   covered/total bins:
                                             3
   missing/total bins:
                                            3
   % Hit:
                              100.00%
                                          100
 Cross Actualiy_sending_addr_wr
                                                       100
                                          100.00%
                                                                - Covered
   covered/total bins:
                                      64
                                             64
   missing/total bins:
                                      0
                                            64
                              100.00%
   % Hit:
                                          100
 Cross Actualiy_sending_data_wr
                                                       100
                                          100.00%
                                                                - Covered
   covered/total bins:
                                             64
   missing/total bins:
                                      0
                                            64
   % Hit:
                              100.00%
                                          100
 Cross Actualiy_sending_addr_rd
                                          100.00%
                                                      100
                                                                 Covered
   covered/total bins:
   missing/total bins:
                                      0
                                            64
                              100.00%
   % Hit:
                                          100
 Cross Actually recieving data
                                        100.00%
                                                     100
                                                                Covered
   covered/total bins:
                                      64
                                             64
   missing/total bins:
                                      0
                                            64
   % Hit:
                              100.00%
                                          100
Covergroup instance \SPI_coverage_pkg::SPI_coverage::SPI_Wrapper
                           100.00%
                                       100

    Covered

 covered/total bins:
                                     522
                                             522
 missing/total bins:
                                      0
                                           522
 % Hit:
                              100.00%
                                          100
 Coverpoint reset
                                   100.00%
                                               100
                                                          Covered
   covered/total bins:
                                      2
   missing/total bins:
                                      0
                                            2
                              100.00%
   % Hit:
                                          100
   bin reset asserted
                                      12
                                                       Covered
   bin reset_disable
                                   122000
                                                         Covered
 Coverpoint Address_write
                                       100.00%
                                                    100
                                                             - Covered
   covered/total bins:
                                      64
                                             64
   missing/total bins:
                                            64
```

% Hit: 100.00% 100 - bin auto[0:3] 121028 1 - Covered bin auto[4:7] 16 1 - Covered bin auto[8:11] 16 1 - Covered bin auto[12:15] 15 1 - Covered bin auto[16:19] 16 1 - Covered bin auto[20:23] 16 1 - Covered bin auto[24:27] 16 1 - Covered bin auto[28:31] 16 1 - Covered bin auto[32:35] 16 1 - Covered bin auto[36:39] 16 1 - Covered bin auto[40:43] 16 1 - Covered bin auto[40:43] 16 1 - Covered bin auto[48:51] 16 1 - Covered bin auto[55:55] 14 1 - Covered bin auto[60:63] 15 1 - Covered	
bin auto[4:7]	
bin auto[8:11]	
bin auto[12:15]	
bin auto[16:19] 16 1 - Covered bin auto[20:23] 16 1 - Covered bin auto[24:27] 16 1 - Covered bin auto[28:31] 16 1 - Covered bin auto[32:35] 16 1 - Covered bin auto[36:39] 16 1 - Covered bin auto[40:43] 16 1 - Covered bin auto[44:47] 16 1 - Covered bin auto[48:51] 16 1 - Covered bin auto[52:55] 14 1 - Covered bin auto[56:59] 16 1 - Covered	
bin auto[20:23] 16 1 - Covered bin auto[24:27] 16 1 - Covered bin auto[28:31] 16 1 - Covered bin auto[32:35] 16 1 - Covered bin auto[36:39] 16 1 - Covered bin auto[40:43] 16 1 - Covered bin auto[44:47] 16 1 - Covered bin auto[48:51] 16 1 - Covered bin auto[52:55] 14 1 - Covered bin auto[56:59] 16 1 - Covered	
bin auto[24:27] 16 1 - Covered bin auto[28:31] 16 1 - Covered bin auto[32:35] 16 1 - Covered bin auto[36:39] 16 1 - Covered bin auto[40:43] 16 1 - Covered bin auto[44:47] 16 1 - Covered bin auto[48:51] 16 1 - Covered bin auto[52:55] 14 1 - Covered bin auto[56:59] 16 1 - Covered	
bin auto[28:31] 16 1 - Covered bin auto[32:35] 16 1 - Covered bin auto[36:39] 16 1 - Covered bin auto[40:43] 16 1 - Covered bin auto[44:47] 16 1 - Covered bin auto[48:51] 16 1 - Covered bin auto[52:55] 14 1 - Covered bin auto[56:59] 16 1 - Covered	
bin auto[32:35] 16 1 - Covered bin auto[36:39] 16 1 - Covered bin auto[40:43] 16 1 - Covered bin auto[44:47] 16 1 - Covered bin auto[48:51] 16 1 - Covered bin auto[52:55] 14 1 - Covered bin auto[56:59] 16 1 - Covered	
bin auto[36:39] 16 1 - Covered bin auto[40:43] 16 1 - Covered bin auto[44:47] 16 1 - Covered bin auto[48:51] 16 1 - Covered bin auto[52:55] 14 1 - Covered bin auto[56:59] 16 1 - Covered	
bin auto[40:43] 16 1 - Covered bin auto[44:47] 16 1 - Covered bin auto[48:51] 16 1 - Covered bin auto[52:55] 14 1 - Covered bin auto[56:59] 16 1 - Covered	
bin auto[44:47] 16 1 - Covered bin auto[48:51] 16 1 - Covered bin auto[52:55] 14 1 - Covered bin auto[56:59] 16 1 - Covered	
bin auto[48:51] 16 1 - Covered bin auto[52:55] 14 1 - Covered bin auto[56:59] 16 1 - Covered	
bin auto[52:55] 14 1 - Covered bin auto[56:59] 16 1 - Covered	
bin auto[56:59] 16 1 - Covered	
I DIN AUTO160/531 15 1 - COVERED	
bin auto[64:67] 16 1 - Covered	
bin auto[68:71] 16 1 - Covered	
bin auto[72:75] 15 1 - Covered	
bin auto[76:79] 16 1 - Covered	
bin auto[80:83] 15 1 - Covered	
bin auto[84:87] 16 1 - Covered	
bin auto[88:91] 16 1 - Covered	
bin auto[92:95] 16 1 - Covered	
bin auto[96:99] 16 1 - Covered	
bin auto[100:103] 15 1 - Covered	
bin auto[104:107] 16 1 - Covered	
bin auto[108:111] 16 1 - Covered	
bin auto[112:115] 15 1 - Covered	
bin auto[116:119] 15 1 - Covered	
bin auto[120:123] 16 1 - Covered	
bin auto[124:127] 16 1 - Covered	
bin auto[128:131] 15 1 - Covered	
bin auto[132:135] 16 1 - Covered	
bin auto[136:139] 15 1 - Covered	
bin auto[140:143] 16 1 - Covered	
bin auto[144:147] 16 1 - Covered	
bin auto [148:151] 16 1 - Covered	
bin auto[152:155] 16 1 - Covered	
bin auto[156:159] 15 1 - Covered	
bin auto[160:163] 16 1 - Covered	
bin auto[164:167] 16 1 - Covered	
bin auto[168:171] 16 1 - Covered	
bin auto[172:175] 14 1 - Covered	
bin auto[176:179] 16 1 - Covered	
bin auto[180:183] 16 1 - Covered	
bin auto[184:187] 14 1 - Covered	
bin auto[188:191] 15 1 - Covered	
bin auto[192:195] 15 1 - Covered	
bin auto[196:199] 16 1 - Covered	
bin auto[200:203] 16 1 - Covered	
bin auto[204:207] 15 1 - Covered	
bin auto[208:211] 14 1 - Covered	
bin auto[212:215] 16 1 - Covered	
bin auto[216:219] 16 1 - Covered	
bin auto[220:223] 15 1 - Covered	
bin auto[224:227] 15 1 - Covered	
bin auto[228:231] 16 1 - Covered	
bin auto[232:235] 16 1 - Covered	
bin auto[236:239] 16 1 - Covered	
bin auto[240:243] 15 1 - Covered	
bin auto[244:247] 16 1 - Covered	
bin auto[248:251] 16 1 - Covered	
bin auto[252:255] 16 1 - Covered	
Coverpoint Data_write 100.00% 100 - Covered	

covered/total bins:	64	64		_
missing/total bins:	0	64	_	
% Hit:	100.00%	100	_	
bin auto[0:3]	121028	1	_	Covered
bin auto[4:7]	16			Covered
bin auto[8:11]	15	1		Covered
bin auto[3:11]	16	1	_	Covered
bin auto[12:13]	16	1	_	Covered
bin auto[20:23]	16	1	_	Covered
bin auto[24:27]	16	1	_	Covered
bin auto[28:31]	15	1	_	Covered
bin auto[32:35]	15	1	_	Covered
bin auto[36:39]	16	1	_	Covered
				Covered
bin auto[40:43]	16 16	1	-	
bin auto[44:47]	16 16	1	-	Covered
bin auto[48:51]	16	1	-	Covered
bin auto[52:55]	16	1	-	Covered
bin auto[56:59]	16	1	-	Covered
bin auto[60:63]	15	1	-	Covered
bin auto[64:67]	14	1	-	Covered
bin auto[68:71]	16	1	-	Covered
bin auto[72:75]	15	1	-	Covered
bin auto[76:79]	15	1	-	Covered
bin auto[80:83]	16	1	-	Covered
bin auto[84:87]	16	1	-	Covered
bin auto[88:91]	16	1	_	Covered
bin auto[92:95]	16	1	_	Covered
bin auto[96:99]	16	1	_	Covered
bin auto[100:103]	16	1	٠.	
bin auto[100:103]	16	1		
bin auto[104:107]	16	1	-	Covered
			-	
bin auto[112:115]	16	1	-	Covered
bin auto[116:119]	15	1	-	Covered
bin auto[120:123]	13	1	-	0010.00
bin auto[124:127]	16	1	-	
bin auto[128:131]	15	1	-	Covered
bin auto[132:135]	15	1	-	0010.00
bin auto[136:139]	16	1	-	Covered
bin auto[140:143]	14	1	-	Covered
bin auto[144:147]	15	1	-	Covered
bin auto[148:151]	16	1	-	Covered
bin auto[152:155]	15	1	-	
bin auto[156:159]	16	1	-	
bin auto[160:163]	15	1	_	Covered
bin auto[164:167]	16	1		Covered
bin auto[168:171]	16	1	-	
			-	
bin auto[172:175]	16	1	-	Covered
bin auto[176:179]	16	1	-	0010.00
bin auto[180:183]	15	1	-	Covered
bin auto[184:187]	16	1	-	Covered
bin auto[188:191]	16	1	-	Covered
bin auto[192:195]	16	1	-	Covered
bin auto[196:199]	16	1	-	Covered
bin auto[200:203]	16	1	-	Covered
bin auto[204:207]	16	1	-	Covered
bin auto[208:211]	16	1	-	Covered
bin auto[212:215]	13	1	-	Covered
bin auto[216:219]	16	1	_	Covered
bin auto[220:223]	16	1		Covered
bin auto[224:227]	16	1	-	Covered
			-	
bin auto[228:231]	16	1	-	
bin auto[232:235]	16	1	-	
bin auto[236:239]	15	1	-	Covered
bin auto[240:243]	16	1	-	Covered
-				
bin auto[244:247] bin auto[248:251]	16	1	-	Covered

bin auto[252:255]	16	1	- Co	Covered
Coverpoint Data_read		.00%	100	- Covered
covered/total bins:	64	64	-	
missing/total bins:	0	64	-	
% Hit:	100.00%	100	-	
bin auto[0:3]	121028	1	- Co	Covered
bin auto[4:7]	16	1	- Cove	
bin auto[8:11]	15	1		overed
bin auto[12:15]	16	1		Covered
bin auto[16:19]	16	1		Covered
bin auto[20:23]	16	1		Covered
bin auto[24:27]	16	1		Covered
bin auto[28:31]	15	1		Covered
bin auto[32:35]	15	1		Covered
bin auto[36:39]	16	1		Covered
bin auto[40:43]	16	1		Covered
bin auto[44:47]	16	1		Covered
bin auto[48:51]	16	1		Covered
bin auto[52:55]	16	1		Covered
bin auto[56:59]	16	1		Covered
bin auto[60:63]	15	1		covered
bin auto[64:67]	14	1		Covered
bin auto[68:71]	16	1		covered
bin auto[72:75]	15	1		covered
bin auto[76:79]	15	1		covered
bin auto[80:83]	16	1		Covered
bin auto[84:87]	16	1		Covered
bin auto[88:91]	16	1		covered
bin auto[92:95]	16	1		covered
bin auto[96:99]	16	1		covered
bin auto[100:103]	16	1		Covered
bin auto[104:107]	16	1		Covered
bin auto[108:111]	16	1		Covered
bin auto[112:115]	16	1		Covered
bin auto[116:119]	15	1		Covered
bin auto[120:123]	13	1		Covered
bin auto[124:127]	16	1		Covered
bin auto[128:131]	15	1		Covered
bin auto[132:135]	15	1		Covered
bin auto[136:139]	16	1		Covered
bin auto[140:143]	14	1		Covered
bin auto[144:147]	15	1		Covered
bin auto[148:151]	16	1		Covered
bin auto[152:155]	15	1		Covered
bin auto[152:155] bin auto[156:159]	16	1		Covered
bin auto[150:163]	15	1		Covered
bin auto[164:167]	16	1		Covered
bin auto[168:171]	16	1		Covered
bin auto[172:175]	16	1		Covered
bin auto[172:173] bin auto[176:179]	16	1		Covered
bin auto[176.179] bin auto[180:183]	15	1		Covered
bin auto[184:187]	16	1		Covered
bin auto[188:191]	16	1		Covered
bin auto[188:191] bin auto[192:195]	16	1		Covered
bin auto[192:193] bin auto[196:199]	16	1		Covered
bin auto[200:203]	16	1		Covered
bin auto[200:203] bin auto[204:207]		1		Covered
bin auto[204:207] bin auto[208:211]	16 16	1		Covered
bin auto[208:211] bin auto[212:215]	13	1		Covered
bin auto[212:215] bin auto[216:219]	16			Covered
bin auto[216:219] bin auto[220:223]		1		Covered
bin auto[224:227]	16 16	1 1		Covered
bin auto[224:227] bin auto[228:231]	16 16	1		Covered
bin auto[228:231] bin auto[232:235]	16 16	1		Covered
	16			
bin auto[236:239] bin auto[240:243]	15 16	1		Covered
DIII AUTOT740:7431	16	1	- ((Covered

1: . [044.047]	46		
bin auto[244:247]	16 1		
bin auto[248:251]	16 1		
bin auto[252:255]	16 1		
Coverpoint Address_read	100.009		Covered
covered/total bins:	64 6	4 -	
missing/total bins:	0 64	-	
% Hit:	100.00% 100	-	
bin auto[0:3]	121028 1		d
bin auto[4:7]	16 1	- Covered	
bin auto[8:11]	16 1	- Covered	
bin auto[12:15]	15 1	- Covered	
bin auto[16:19]	16 1	- Covered	
bin auto[20:23]	16 1	- Covered	
bin auto[24:27]	16 1	- Covered	
bin auto[28:31]	16 1	- Covered	
bin auto[32:35]	16 1	- Covered	
bin auto[36:39]	16 1	- Covered	
bin auto[40:43]	16 1	- Covered	
bin auto[44:47]	16 1	- Covered	
bin auto[48:51]	16 1	- Covered	
bin auto[52:55]	14 1	- Covered	
bin auto[56:59]	16 1	- Covered	
bin auto[60:63]	15 1	- Covered	
bin auto[64:67]	16 1	 Covered 	
bin auto[68:71]	16 1	- Covered	
bin auto[72:75]	15 1	- Covered	
bin auto[76:79]	16 1	- Covered	
bin auto[80:83]	15 1	 Covered 	
bin auto[84:87]	16 1	 Covered 	
bin auto[88:91]	16 1	- Covered	
bin auto[92:95]	16 1	- Covered	
bin auto[96:99]	16 1	 Covered 	
bin auto[100:103]	15 1		
bin auto[104:107]	16 1		
bin auto[108:111]	16 1		
bin auto[112:115]	15 1		
bin auto[116:119]	15 1		
bin auto[120:123]	16 1		
bin auto[124:127]	16 1		
bin auto[128:131]	15 1		
bin auto[132:135]	16 1		
bin auto[136:139]	15 1		
bin auto[140:143]	16 1		
bin auto[144:147]	16 1		
bin auto[148:151]	16 1		
bin auto[152:155]	16 1		
bin auto[156:159]	15 1		
bin auto[160:163]	16 1		
bin auto[164:167]	16 1		
bin auto[168:171]	16 1		
bin auto[172:175]	14 1		
bin auto[176:179]	16 1		
bin auto[180:183]	16 1		
bin auto[184:187]	14 1		
bin auto[188:191]	15 1		
bin auto[192:195]	15 1		
bin auto[196:199]	16 1		
bin auto[200:203]	16 1		
bin auto[204:207]	15 1		
bin auto[208:211]	14 1		
bin auto[212:215]	16 1		
bin auto[216:219]	16 1		
bin auto[220:223]	15 1		
bin auto[224:227]	15 1	- Covered	d
bin auto[228:231]	16 1	- Covered	d
bin auto[232:235]	16 1	- Covered	d

```
bin auto[236:239]
                                    16
                                           1
                                                     Covered
 bin auto[240:243]
                                    15
                                                    Covered
 bin auto[244:247]
                                    16
                                                    Covered
 bin auto[248:251]
                                    16
                                           1
                                                    Covered
 bin auto[252:255]
                                                    Covered
                                    16
                                           1
Coverpoint Send_Address_wr
                                       100.00%
                                                            - Covered
 covered/total bins:
                                    1
                                          1
 missing/total bins:
                                    0
                                          1
 % Hit:
                            100.00%
                                        100
 bin writing_add
                                 11000
                                                     Covered
Coverpoint Send_Address_rd
                                       100.00%
                                                   100
                                                            - Covered
 covered/total bins:
                                    1
                                          1
 missing/total bins:
                                    0
                                          1
                            100.00%
                                        100
 % Hit:
 bin reading_add
                                  11000
                                                     Covered
Coverpoint send_Data_wr
                                      100.00%
                                                  100
                                                           - Covered
 covered/total bins:
                                    1
                                          1
 missing/total bins:
                                    0
                                          1
 % Hit:
                            100.00%
                                        100
 bin writing_data
                                 11000
                                                     Covered
Coverpoint Recieving_Data_rd
                                       100.00%
                                                   100
                                                            - Covered
 covered/total bins:
                                          1
 missing/total bins:
                                    0
 % Hit:
                            100.00%
                                        100
 bin reading_data
                                  8000
                                                     Covered
                                            1
Coverpoint Sending_order_Read_data
                                           100.00%
                                                       100
                                                                   Covered
 covered/total bins:
                                          1
 missing/total bins:
                                    0
                                          1
                            100.00%
 % Hit:
                                        100
 bin order_reading_data
                                     11000
                                                1
                                                       - Covered
                                          100.00%
Coverpoint Starting_Communication
                                                       100
                                                               - Covered
 covered/total bins:
                                    3
                                          3
 missing/total bins:
                                    0
                                          3
 % Hit:
                            100.00%
                                        100
 bin Start
                             114000
                                                  Covered
                                         1
                              8012
                                                 Covered
 bin End
                                    7988
 bin transaction_back
                                              1
                                                    - Covered
                                        100.00%
                                                    100
                                                             - Covered
Cross Actualiy_sending_addr_wr
 covered/total bins:
                                    64
                                          64
 missing/total bins:
                                    0
                                          64
 % Hit:
                            100.00%
                                        100
 Auto, Default and User Defined Bins:
   bin <writing_add,auto[252:255]>
                                           16
                                                  1
                                                        - Covered
   bin <writing_add,auto[248:251]>
                                           16
                                                  1
                                                           Covered
   bin <writing_add,auto[244:247]>
                                                           Covered
                                           16
                                                  1
   bin <writing_add,auto[240:243]>
                                           15
                                                           Covered
   bin <writing_add,auto[236:239]>
                                          16
                                                  1
                                                           Covered
   bin <writing add,auto[232:235]>
                                          16
                                                  1
                                                           Covered
   bin <writing add,auto[228:231]>
                                          16
                                                           Covered
   bin <writing_add,auto[224:227]>
                                           15
                                                  1
                                                           Covered
                                          15
   bin <writing_add,auto[220:223]>
                                                  1
                                                           Covered
    bin <writing add,auto[216:219]>
                                           16
                                                  1
                                                           Covered
   bin <writing_add,auto[212:215]>
                                           16
                                                  1
                                                           Covered
   bin <writing_add,auto[208:211]>
                                                           Covered
                                          14
                                                  1
   bin <writing_add,auto[204:207]>
                                          15
                                                  1
                                                           Covered
   bin <writing_add,auto[200:203]>
                                                           Covered
   bin <writing_add,auto[196:199]>
                                           16
                                                  1
                                                           Covered
                                          15
   bin <writing add,auto[192:195]>
                                                  1
                                                           Covered
    bin <writing_add,auto[188:191]>
                                           15
                                                  1
                                                           Covered
   bin <writing_add,auto[184:187]>
                                          14
                                                  1
                                                           Covered
   bin <writing_add,auto[180:183]>
                                          16
                                                  1
                                                           Covered
   bin <writing add,auto[176:179]>
                                           16
                                                  1
                                                           Covered
   bin <writing_add,auto[172:175]>
                                           14
                                                  1
                                                           Covered
    bin <writing_add,auto[168:171]>
                                           16
                                                  1
                                                           Covered
    bin <writing_add,auto[164:167]>
                                           16
                                                  1
                                                           Covered
   bin <writing_add,auto[160:163]>
                                           16
                                                           Covered
```

```
bin <writing_add,auto[156:159]>
                                            15
                                                   1
                                                            Covered
    bin <writing add,auto[152:155]>
                                                            Covered
                                           16
                                                   1
    bin <writing_add,auto[148:151]>
                                                            Covered
    bin <writing_add,auto[144:147]>
                                            16
                                                   1
                                                            Covered
    bin <writing_add,auto[140:143]>
                                            16
                                                   1
                                                            Covered
    bin < writing_add, auto[136:139]>
                                            15
                                                   1
                                                            Covered
    bin <writing_add,auto[132:135]>
                                            16
                                                   1
                                                            Covered
    bin < writing add.auto[128:131]>
                                           15
                                                   1
                                                            Covered
    bin <writing add,auto[124:127]>
                                            16
                                                            Covered
    bin <writing_add,auto[120:123]>
                                            16
                                                   1
                                                            Covered
    bin <writing_add,auto[116:119]>
                                           15
                                                   1
                                                            Covered
    bin <writing add,auto[112:115]>
                                           15
                                                   1
                                                            Covered
    bin <writing_add,auto[108:111]>
                                           16
                                                   1
                                                            Covered
    bin <writing_add,auto[104:107]>
                                           16
                                                   1
                                                            Covered
    bin <writing_add,auto[100:103]>
                                           15
                                                            Covered
    bin <writing_add,auto[96:99]>
                                          16
                                                  1
                                                        - Covered
    bin <writing_add,auto[92:95]>
                                          16
                                                  1
                                                          Covered
                                          16
    bin <writing_add,auto[88:91]>
                                                  1
                                                           Covered
    bin <writing_add,auto[84:87]>
                                          16
                                                           Covered
    bin <writing_add,auto[80:83]>
                                          15
                                                  1
                                                           Covered
    bin <writing_add,auto[76:79]>
                                          16
                                                  1
                                                           Covered
    bin <writing add,auto[72:75]>
                                          15
                                                           Covered
    bin <writing_add,auto[68:71]>
                                                           Covered
    bin <writing_add,auto[64:67]>
                                          16
                                                  1
                                                           Covered
    bin <writing_add,auto[60:63]>
                                          15
                                                  1
                                                           Covered
    bin <writing_add,auto[56:59]>
                                          16
                                                           Covered
    bin <writing_add,auto[52:55]>
                                          14
                                                  1
                                                           Covered
    bin <writing_add,auto[48:51]>
                                          16
                                                          Covered
                                                  1
    bin <writing_add,auto[44:47]>
                                          16
                                                           Covered
    bin <writing_add,auto[40:43]>
                                          16
                                                          Covered
    bin <writing_add,auto[36:39]>
                                          16
                                                 1
                                                           Covered
    bin <writing_add,auto[32:35]>
                                          16
                                                 1
                                                           Covered
    bin <writing_add,auto[28:31]>
                                          16
                                                           Covered
    bin <writing_add,auto[24:27]>
                                          16
                                                  1
                                                           Covered
                                                           Covered
    bin <writing_add,auto[20:23]>
                                          16
    bin <writing_add,auto[16:19]>
                                                           Covered
    bin <writing_add,auto[12:15]>
                                          15
                                                 1
                                                           Covered
    bin <writing_add,auto[8:11]>
                                         16
                                                          Covered
    bin <writing_add,auto[4:7]>
                                         16
                                                          Covered
    bin <writing_add,auto[0:3]>
                                        10016
                                                  1
                                                            Covered
Cross Actualiy_sending_data_wr
                                         100.00%
                                                     100
                                                              - Covered
 covered/total bins:
                                            64
  missing/total bins:
                                    0
                                          64
                            100.00%
                                         100
 % Hit:
 Auto, Default and User Defined Bins:
    bin <writing_data,auto[252:255]>
                                            16
                                                   1
                                                            Covered
    bin <writing_data,auto[248:251]>
                                            16
                                                   1
                                                            Covered
    bin <writing_data,auto[244:247]>
                                            16
                                                            Covered
                                                   1
    bin <writing data,auto[240:243]>
                                            16
                                                   1
                                                            Covered
    bin <writing_data,auto[236:239]>
                                            15
                                                   1
                                                            Covered
    bin <writing_data,auto[232:235]>
                                            16
                                                   1
                                                            Covered
    bin <writing_data,auto[228:231]>
                                            16
                                                   1
                                                            Covered
    bin <writing_data,auto[224:227]>
                                            16
                                                   1
                                                            Covered
    bin <writing_data,auto[220:223]>
                                            16
                                                   1
                                                            Covered
                                                            Covered
    bin <writing_data,auto[216:219]>
                                            16
                                                   1
                                                            Covered
    bin < writing_data, auto[212:215]>
                                            13
    bin <writing_data,auto[208:211]>
                                            16
                                                   1
                                                            Covered
    bin <writing data,auto[204:207]>
                                            16
                                                   1
                                                            Covered
    bin <writing_data,auto[200:203]>
                                            16
                                                   1
                                                             Covered
    bin <writing_data,auto[196:199]>
                                            16
                                                   1
                                                            Covered
    bin <writing_data,auto[192:195]>
                                            16
                                                            Covered
                                                   1
    bin <writing data,auto[188:191]>
                                            16
                                                   1
                                                            Covered
    bin <writing_data,auto[184:187]>
                                            16
                                                   1
                                                            Covered
                                            15
                                                   1
    bin <writing_data,auto[180:183]>
                                                            Covered
    bin <writing_data,auto[176:179]>
                                            16
                                                   1
                                                            Covered
    bin <writing_data,auto[172:175]>
                                                            Covered
```

```
bin <writing_data,auto[168:171]>
                                            16
                                                   1
                                                            Covered
    bin < writing data, auto [164:167]>
                                                            Covered
                                            16
                                                   1
    bin <writing_data,auto[160:163]>
                                            15
                                                            Covered
    bin <writing_data,auto[156:159]>
                                            16
                                                   1
                                                            Covered
                                            15
    bin <writing_data,auto[152:155]>
                                                   1
                                                            Covered
    bin < writing_data, auto[148:151]>
                                            16
                                                   1
                                                             Covered
   bin <writing_data,auto[144:147]>
                                            15
                                                   1
                                                            Covered
   bin <writing_data,auto[140:143]>
                                            14
                                                            Covered
                                                   1
   bin <writing data,auto[136:139]>
                                            16
                                                   1
                                                            Covered
   bin <writing_data,auto[132:135]>
                                            15
                                                   1
                                                            Covered
    bin <writing_data,auto[128:131]>
                                            15
                                                   1
                                                            Covered
    bin < writing data, auto [124:127]>
                                            16
                                                   1
                                                            Covered
   bin <writing_data,auto[120:123]>
                                            13
                                                   1
                                                            Covered
   bin <writing_data,auto[116:119]>
                                            15
                                                   1
                                                            Covered
                                                            Covered
   bin <writing_data,auto[112:115]>
                                            16
                                                   1
    bin <writing_data,auto[108:111]>
                                            16
                                                            Covered
                                            16
   bin <writing_data,auto[104:107]>
                                                   1
                                                            Covered
                                           16
    bin <writing_data,auto[100:103]>
                                                   1
                                                            Covered
    bin <writing_data,auto[96:99]>
                                          16
                                                  1
   bin <writing_data,auto[92:95]>
                                          16
                                                  1
                                                           Covered
   bin <writing_data,auto[88:91]>
                                                           Covered
                                          16
                                                  1
   bin <writing data,auto[84:87]>
                                          16
                                                           Covered
    bin <writing_data,auto[80:83]>
                                                           Covered
    bin <writing_data,auto[76:79]>
                                          15
                                                  1
                                                           Covered
    bin < writing_data, auto [72:75] >
                                          15
                                                           Covered
                                                  1
    bin <writing_data,auto[68:71]>
                                          16
                                                           Covered
    bin <writing_data,auto[64:67]>
                                          14
                                                  1
                                                           Covered
    bin <writing_data,auto[60:63]>
                                          15
                                                           Covered
    bin <writing_data,auto[56:59]>
                                          16
                                                           Covered
    bin < writing_data, auto [52:55] >
                                          16
                                                  1
                                                           Covered
    bin <writing_data,auto[48:51]>
                                          16
                                                 1
                                                           Covered
    bin <writing_data,auto[44:47]>
                                          16
                                                  1
                                                           Covered
    bin < writing_data, auto [40:43] >
                                          16
                                                           Covered
   bin <writing_data,auto[36:39]>
                                          16
                                                  1
                                                           Covered
    bin <writing_data,auto[32:35]>
                                          15
                                                  1
                                                           Covered
    bin <writing_data,auto[28:31]>
                                                           Covered
    bin <writing_data,auto[24:27]>
                                          16
                                                 1
                                                           Covered
    bin <writing_data,auto[20:23]>
                                          16
                                                           Covered
                                                 1
    bin <writing_data,auto[16:19]>
                                          16
                                                           Covered
    bin <writing_data,auto[12:15]>
                                          16
                                                           Covered
    bin <writing_data,auto[8:11]>
                                          15
                                                          Covered
    bin <writing_data,auto[4:7]>
                                         16
                                                          Covered
   bin <writing_data,auto[0:3]>
                                        10016
                                                  1
                                                            Covered
                                         100.00%
Cross Actualiy_sending_addr_rd
                                                     100

    Covered

 covered/total bins:
                                           64
                                    64
 missing/total bins:
                                          64
 % Hit:
                            100.00%
                                         100
 Auto, Default and User Defined Bins:
   bin <reading add,auto[252:255]>
                                            16
                                                             Covered
   bin <reading_add,auto[248:251]>
                                            16
                                                   1
                                                             Covered
   bin <reading_add,auto[244:247]>
                                            16
                                                   1
                                                             Covered
    bin <reading add,auto[240:243]>
                                            15
                                                   1
                                                             Covered
   bin <reading_add,auto[236:239]>
                                            16
                                                   1
                                                             Covered
   bin <reading_add,auto[232:235]>
                                            16
                                                   1
                                                             Covered
   bin <reading_add,auto[228:231]>
                                                             Covered
                                            16
                                                   1
                                                             Covered
   bin <reading_add,auto[224:227]>
   bin <reading_add,auto[220:223]>
                                            15
                                                   1
                                                             Covered
   bin <reading add,auto[216:219]>
                                            16
                                                   1
                                                             Covered
    bin <reading_add,auto[212:215]>
                                            16
                                                   1
                                                             Covered
   bin <reading_add,auto[208:211]>
                                            14
                                                   1
                                                             Covered
   bin <reading_add,auto[204:207]>
                                            15
                                                             Covered
                                                   1
   bin <reading add,auto[200:203]>
                                            16
                                                             Covered
   bin <reading_add,auto[196:199]>
                                            16
                                                   1
                                                             Covered
    bin <reading_add,auto[192:195]>
                                            15
                                                   1
                                                             Covered
    bin <reading_add,auto[188:191]>
                                            15
                                                   1
                                                             Covered
    bin <reading_add,auto[184:187]>
                                                             Covered
```

```
bin <reading_add,auto[180:183]>
                                           16
                                                  1
                                                            Covered
    bin <reading add,auto[176:179]>
                                           16
                                                            Covered
                                                  1
    bin <reading_add,auto[172:175]>
                                                            Covered
    bin <reading_add,auto[168:171]>
                                           16
                                                  1
                                                           Covered
                                           16
    bin <reading_add,auto[164:167]>
                                                  1
                                                            Covered
    bin <reading_add,auto[160:163]>
                                           16
                                                            Covered
   bin <reading_add,auto[156:159]>
                                           15
                                                  1
                                                            Covered
   bin <reading add,auto[152:155]>
                                           16
                                                  1
                                                            Covered
   bin <reading add,auto[148:151]>
                                           16
                                                            Covered
   bin <reading_add,auto[144:147]>
                                           16
                                                  1
                                                            Covered
    bin <reading_add,auto[140:143]>
                                           16
                                                  1
                                                            Covered
    bin <reading add,auto[136:139]>
                                           15
                                                  1
                                                            Covered
   bin <reading_add,auto[132:135]>
                                           16
                                                  1
                                                            Covered
   bin <reading_add,auto[128:131]>
                                           15
                                                  1
                                                            Covered
   bin <reading_add,auto[124:127]>
                                                            Covered
                                           16
                                                  1
    bin <reading_add,auto[120:123]>
                                                            Covered
   bin <reading_add,auto[116:119]>
                                           15
                                                           Covered
                                                  1
                                           15
    bin <reading_add,auto[112:115]>
                                                  1
                                                            Covered
    bin <reading_add,auto[108:111]>
                                           16
                                                  1
                                                            Covered
   bin <reading_add,auto[104:107]>
                                           16
                                                  1
                                                            Covered
   bin <reading_add,auto[100:103]>
                                           15
                                                            Covered
                                                  1
   bin <reading add,auto[96:99]>
                                         16
                                                          Covered
    bin <reading_add,auto[92:95]>
                                         16
                                                          Covered
    bin <reading_add,auto[88:91]>
                                         16
                                                 1
                                                          Covered
    bin <reading_add,auto[84:87]>
                                         16
                                                 1
                                                          Covered
    bin <reading_add,auto[80:83]>
                                         15
                                                          Covered
   bin <reading_add,auto[76:79]>
                                         16
                                                 1
                                                          Covered
    bin <reading_add,auto[72:75]>
                                         15
                                                          Covered
                                                 1
    bin <reading_add,auto[68:71]>
                                         16
                                                          Covered
    bin <reading_add,auto[64:67]>
                                         16
                                                 1
                                                          Covered
    bin <reading_add,auto[60:63]>
                                         15
                                                 1
                                                          Covered
    bin <reading_add,auto[56:59]>
                                         16
                                                 1
                                                          Covered
    bin <reading_add,auto[52:55]>
                                         14
                                                 1
                                                           Covered
   bin <reading_add,auto[48:51]>
                                         16
                                                 1
                                                          Covered
   bin <reading_add,auto[44:47]>
                                                          Covered
                                         16
                                                 1
    bin <reading_add,auto[40:43]>
                                                          Covered
    bin <reading_add,auto[36:39]>
                                         16
                                                 1
                                                          Covered
    bin <reading_add,auto[32:35]>
                                         16
                                                          Covered
                                                 1
    bin <reading_add,auto[28:31]>
                                         16
                                                          Covered
   bin <reading_add,auto[24:27]>
                                         16
                                                 1
                                                          Covered
    bin <reading_add,auto[20:23]>
                                         16
                                                          Covered
    bin <reading_add,auto[16:19]>
                                         16
                                                          Covered
   bin <reading_add,auto[12:15]>
                                         15
                                                          Covered
                                         16
   bin <reading_add,auto[8:11]>
                                                1
                                                         Covered
    bin <reading_add,auto[4:7]>
                                        16
                                                1
                                                         Covered
    bin <reading_add,auto[0:3]>
                                       10016
                                                  1
                                                           Covered
                                      100.00%
Cross Actualiy_recieving_data
                                                  100
                                                           - Covered
 covered/total bins:
                                    64
                                          64
 missing/total bins:
                                         64
 % Hit:
                           100.00%
                                        100
 Auto, Default and User Defined Bins:
    bin <reading data,auto[252:255]>
                                           16
                                                   1
                                                            Covered
   bin <reading_data,auto[248:251]>
                                           16
                                                  1
                                                            Covered
   bin <reading_data,auto[244:247]>
                                           16
                                                  1
                                                            Covered
   bin <reading_data,auto[240:243]>
                                                            Covered
                                           16
                                                   1
   bin <reading_data,auto[236:239]>
                                                            Covered
   bin <reading_data,auto[232:235]>
                                           16
                                                  1
                                                            Covered
   bin <reading data,auto[228:231]>
                                           16
                                                  1
                                                            Covered
    bin <reading_data,auto[224:227]>
                                           16
                                                   1
                                                            Covered
   bin <reading_data,auto[220:223]>
                                           16
                                                  1
                                                            Covered
   bin <reading_data,auto[216:219]>
                                           16
                                                  1
                                                            Covered
   bin <reading data,auto[212:215]>
                                           13
                                                            Covered
   bin <reading_data,auto[208:211]>
                                           16
                                                  1
                                                            Covered
    bin <reading_data,auto[204:207]>
                                           16
                                                  1
                                                            Covered
    bin <reading_data,auto[200:203]>
                                           16
                                                  1
                                                            Covered
   bin <reading_data,auto[196:199]>
                                                            Covered
```

```
bin <reading_data,auto[192:195]>
                                             16
                                                    1
                                                             Covered
      bin <reading data,auto[188:191]>
                                             16
                                                             Covered
                                                    1
      bin <reading_data,auto[184:187]>
                                                             Covered
      bin <reading_data,auto[180:183]>
                                             15
                                                    1

    Covered

      bin <reading_data,auto[176:179]>
                                             16
                                                    1
                                                             Covered
      bin <reading_data,auto[172:175]>
                                             16
                                                    1
                                                              Covered
      bin <reading_data,auto[168:171]>
                                             16
                                                    1
                                                             Covered
                                                          - Covered
      bin <reading data,auto[164:167]>
                                             16
                                                    1
      bin <reading data,auto[160:163]>
                                             15
                                                             Covered
      bin <reading_data,auto[156:159]>
                                             16
                                                    1
                                                             Covered
      bin <reading_data,auto[152:155]>
                                             15
                                                    1
                                                             Covered
      bin <reading data,auto[148:151]>
                                             16
                                                    1
                                                             Covered
      bin <reading_data,auto[144:147]>
                                             15
                                                    1
                                                             Covered
      bin <reading_data,auto[140:143]>
                                             14
                                                    1
                                                             Covered
      bin <reading_data,auto[136:139]>
                                                    1
                                                             Covered
                                             16
      bin <reading_data,auto[132:135]>
                                                             Covered
      bin <reading_data,auto[128:131]>
                                             15
                                                    1

    Covered

      bin <reading_data,auto[124:127]>
                                             16
                                                    1
                                                             Covered
                                             13
      bin <reading_data,auto[120:123]>
                                                    1
                                                              Covered
      bin <reading_data,auto[116:119]>
                                             15
                                                    1
                                                             Covered
      bin <reading_data,auto[112:115]>
                                                             Covered
                                             16
                                                    1
      bin <reading data,auto[108:111]>
                                             16
                                                    1
                                                             Covered
      bin <reading_data,auto[104:107]>
                                                             Covered
      bin <reading_data,auto[100:103]>
                                             16
                                                    1
                                                             Covered
      bin <reading_data,auto[96:99]>
                                            16
                                                         - Covered
                                                   1
      bin <reading_data,auto[92:95]>
                                            16
                                                            Covered
      bin <reading_data,auto[88:91]>
                                           16
                                                   1
                                                            Covered
      bin <reading_data,auto[84:87]>
                                                         - Covered
                                           16
                                                   1
                                                         - Covered
      bin <reading_data,auto[80:83]>
                                            16
      bin <reading_data,auto[76:79]>
                                            15
                                                   1
                                                         - Covered
      bin <reading_data,auto[72:75]>
                                           15
                                                   1
                                                         - Covered
      bin <reading_data,auto[68:71]>
                                            16
                                                   1
                                                            Covered
      bin <reading_data,auto[64:67]>
                                            14
                                                   1
                                                            Covered
      bin <reading_data,auto[60:63]>
                                           15
                                                   1
                                                            Covered
      bin <reading_data,auto[56:59]>
                                                            Covered
                                           16
                                                   1
      bin <reading_data,auto[52:55]>
                                                            Covered
      bin <reading_data,auto[48:51]>
                                           16
                                                   1
                                                         - Covered
      bin <reading_data,auto[44:47]>
                                           16
                                                   1
                                                         - Covered
      bin <reading_data,auto[40:43]>
                                            16
                                                            Covered
      bin <reading_data,auto[36:39]>
                                           16
                                                   1
                                                            Covered
                                                         - Covered
      bin <reading_data,auto[32:35]>
                                           15
                                                   1
      bin <reading_data,auto[28:31]>
                                            15
                                                         - Covered
      bin <reading_data,auto[24:27]>
                                           16
                                                   1
                                                         - Covered
      bin <reading_data,auto[20:23]>
                                           16
                                                   1

    Covered

      bin <reading data,auto[16:19]>
                                           16
                                                   1
                                                            Covered
      bin <reading_data,auto[12:15]>
                                           16
                                                   1
                                                            Covered
      bin <reading_data,auto[8:11]>
                                           15
                                                  1
                                                            Covered
                                                        - Covered
      bin <reading data,auto[4:7]>
                                          16
                                                  1
      bin <reading data,auto[0:3]>
                                          7016
                                                            Covered
COVERGROUP COVERAGE:
                                 Metric
                                           Goal
                                                  Bins Status
Covergroup
TYPE /RAM_coverage_pkg/RAM_coverage/cvr_gp
                                                    100.00%
                                                                100
                                                                         - Covered
  covered/total bins:
                                     655
                                             655
  missing/total bins:
                                     0
                                           655
  % Hit:
                              100.00%
                                          100
  Coverpoint reset
                                  100.00%
                                              100
                                                          Covered
    covered/total bins:
                                      2
                                            2
    missing/total bins:
                              100.00%
    % Hit:
                                          100
  Coverpoint data_valid
                                     100.00%
                                                 100
                                                          - Covered
    covered/total bins:
                                      9
                                            9
    missing/total bins:
```

```
% Hit:
                              100.00%
                                          100
                                      100.00%
 Coverpoint data written
                                                   100
                                                            - Covered
   covered/total bins:
                                             64
   missing/total bins:
                                      0
                                            64
   % Hit:
                              100.00%
                                          100
 Coverpoint data_read
                                      100.00%
                                                  100
                                                              Covered
   covered/total bins:
                                      64
                                             64
   missing/total bins:
                                      0
                                            64
   % Hit:
                              100.00%
                                          100
 Coverpoint address_written
                                        100.00%
                                                    100
                                                               Covered
   covered/total bins:
                                      64
                                            64
   missing/total bins:
                                      0
                                            64
                              100.00%
   % Hit:
                                          100
 Coverpoint address_read
                                       100.00%
                                                   100
                                                               Covered
   covered/total bins:
                                      64
                                             64
   missing/total bins:
                                      0
                                            64
                              100.00%
   % Hit:
                                          100
 Coverpoint receive_valid
                                      100.00%
                                                   100
                                                              Covered
   covered/total bins:
                                             2
   missing/total bins:
                                      0
                                            2
   % Hit:
                              100.00%
                                          100
 Coverpoint send valid
                                      100.00%
                                                  100
                                                           - Covered
   covered/total bins:
                                      2
                                             2
   missing/total bins:
                                      0
   % Hit:
                              100.00%
                                          100
 Cross Writing_address
                                      100.00%
                                                  100
                                                           - Covered
   covered/total bins:
                                      128
                                             128
   missing/total bins:
                                           128
                                      0
                              100.00%
   % Hit:
                                          100
 Cross Writing_data
                                    100.00%
                                                100
                                                            Covered
   covered/total bins:
                                      128
                                             128
   missing/total bins:
                                      0
                                           128
   % Hit:
                              100.00%
                                          100
 Cross reading_address
                                      100.00%
                                                  100

    Covered

   covered/total bins:
                                      64
                                             64
   missing/total bins:
                              100.00%
   % Hit:
                                          100
 Cross reading_data
                                    100.00%
                                                100
                                                            Covered
   covered/total bins:
                                      64
                                             64
   missing/total bins:
                                      0
                                            64
                              100.00%
   % Hit:
                                          100
Covergroup instance \( \forall RAM_coverage_pkg::RAM_coverage::cvr_gp \)
                           100.00%
                                        100
                                                   Covered
 covered/total bins:
                                     655
                                             655
 missing/total bins:
                                           655
                                      0
 % Hit:
                              100.00%
                                          100
 Coverpoint reset
                                   100.00%
                                               100
                                                           Covered
   covered/total bins:
                                      2
                                             2
   missing/total bins:
   % Hit:
                              100.00%
                                          100
   bin reset_asserted
                                      12
                                                       Covered
                                              1
   bin reset disable
                                   122000
                                                         Covered
 Coverpoint data_valid
                                     100.00%
                                                  100
                                                          - Covered
   covered/total bins:
                                      9
                                            9
   missing/total bins:
                                      0
   % Hit:
                              100.00%
                                          100
   bin writing_complete
                                       6000
                                                 1
                                                       - Covered
                                 94012
   bin writing
                                                     Covered
                                            1
   bin reading
                                  2000
                                            1
                                                     Covered
   bin change_wr_rd
                                      2000
                                                         Covered
   bin change_rd_wr
                                      2000
                                                         Covered
                                                1
   bin default values[0]
                                      94012
                                                          Covered
                                                1
   bin default_values[1]
                                      6000
                                                1
                                                         Covered
                                      2000
   bin default_values[2]
                                                1
                                                         Covered
   bin default_values[3]
                                      20000
                                                1
                                                          Covered
 Coverpoint data_written
                                      100.00%
                                                   100
                                                            - Covered
```

covered/total bins:	64	64	-
			-
missing/total bins:	100.00%	64	-
% Hit: bin auto[0:3]	100.00% 116107	100 1	- Covered
bin auto[4:7]	94	1	- Covered
bin auto[4:7]	9 4 95	1	- Covered
bin auto[3:11]	95	1	- Covered
bin auto[12:13]	95	1	- Covered
bin auto[20:23]	95 95	1	- Covered
bin auto[24:27]	93	1	- Covered
bin auto[24:27] bin auto[28:31]	93	1	- Covered
bin auto[32:35]	93	1	- Covered
bin auto[32:35]	93 94	1	- Covered
bin auto[40:43]	9 4 95	1	- Covered
bin auto[40:43] bin auto[44:47]	95 96	1	- Covered
	96 95		
bin auto[48:51]		1	
bin auto[52:55]	94	1	- Covered
bin auto[56:59]	93	1	- Covered
bin auto[60:63]	95	1	- Covered
bin auto[64:67]	92	1	- Covered
bin auto[68:71]	94	1	- Covered
bin auto[72:75]	92	1	- Covered
bin auto[76:79]	92	1	- Covered
bin auto[80:83]	95	1	 Covered
bin auto[84:87]	91	1	- Covered
bin auto[88:91]	96	1	 Covered
bin auto[92:95]	92	1	 Covered
bin auto[96:99]	93	1	 Covered
bin auto[100:103]	95	1	- Covered
bin auto[104:107]	91	1	- Covered
bin auto[108:111]	94	1	- Covered
bin auto[112:115]	93	1	- Covered
bin auto[116:119]	94	1	- Covered
bin auto[120:123]	90	1	- Covered
bin auto[124:127]	95	1	- Covered
bin auto[128:131]	91	1	- Covered
bin auto[132:135]	94	1	- Covered
bin auto[136:139]	93	1	- Covered
bin auto[140:143]	91	1	- Covered
bin auto[144:147]	91	1	- Covered
bin auto[148:151]	95	1	- Covered
bin auto[148:151]	94	1	- Covered
bin auto[152:155]	95	1	- Covered
bin auto[160:163]	93	1	- Covered
bin auto[164:167]	92	1	- Covered
bin auto[168:171]	95	1	- Covered
bin auto[172:175]	95	1	- Covered
bin auto[176:179]	95	1	- Covered
bin auto[180:183]	93	1	- Covered
bin auto[184:187]	93	1	- Covered
bin auto[188:191]	92	1	- Covered
bin auto[192:195]	93	1	- Covered
bin auto[196:199]	93	1	 Covered
bin auto[200:203]	94	1	 Covered
bin auto[204:207]	95	1	 Covered
bin auto[208:211]	94	1	- Covered
bin auto[212:215]	92	1	 Covered
bin auto[216:219]	94	1	- Covered
bin auto[220:223]	95	1	- Covered
bin auto[224:227]	96	1	- Covered
bin auto[228:231]	96	1	- Covered
bin auto[232:235]	93	1	- Covered
bin auto[236:239]	95	1	- Covered
bin auto[240:243]	96	1	- Covered
bin auto[244:247]	94	1	 Covered
bin auto[248:251]	95	1	- Covered

bin auto[252:255]	94	1	-	Covered	
Coverpoint data_read	100.0		100	- Covered	
covered/total bins:	64	64	-		
missing/total bins:	0	64	-		
% Hit:	100.00%	100	-		
bin auto[0:3]	27817	1	_	Covered	
bin auto[4:7]	1361	1		Covered	
bin auto[8:11]	1475	1		Covered	
bin auto[12:15]	1536	1	_	Covered	
bin auto[16:19]	1536	1	_	Covered	
bin auto[20:23]	1536	1	_	Covered	
bin auto[24:27]	1536	1		Covered	
bin auto[28:31]	1440	1	_	Covered	
bin auto[32:35]	1475	1	_	Covered	
bin auto[32:33] bin auto[36:39]	1501	1		Covered	
bin auto[40:43]	1536	1	_	Covered	
bin auto[44:47]	1536	1		Covered	
bin auto[48:51]	1536	1		Covered	
bin auto[52:55]	1536	1	-	Covered	
bin auto[56:59]	1485	1		Covered	
bin auto[60:63]	1389	1		Covered	
bin auto[64:67]	1274	1	-	Covered	
bin auto[68:71]	1501	1		Covered	
bin auto[72:75]	1590	1	-	Covered	
bin auto[76:79]	1335	1	-	Covered	
bin auto[80:83]	1536	1		Covered	
bin auto[84:87]	1536	1	-	Covered	
bin auto[88:91]	1536	1		Covered	
bin auto[92:95]	1536	1	-	Covered	
bin auto[96:99]	1256	1	-	Covered	
bin auto[100:103]	1536			Covered	
bin auto[104:107]	1536			Covered	
bin auto[108:111]	1501			Covered	
bin auto[112:115]	1536			Covered	
bin auto[116:119]	1424			Covered	
bin auto[120:123]	1493			Covered	
bin auto[124:127]	1536			Covered	
bin auto[128:131]	1475				
bin auto[132:135]	1475				
bin auto[136:139]	1676			Covered	
bin auto[140:143]	1344			Covered	
bin auto[144:147]	1440			Covered	
bin auto[148:151]	1536			Covered	
bin auto[152:155]	1354			Covered	
bin auto[156:159]	1536			Covered	
bin auto[160:163]	1475			Covered	
bin auto[164:167]	1641			Covered	
bin auto[168:171]	1536			Covered	
bin auto[172:175]	1501			Covered	
bin auto[176:179]	1536			Covered	
bin auto[180:183]	1440			Covered	
bin auto[184:187]	1501				
bin auto[188:191]	1536			Covered	
bin auto[192:195]	1616			Covered	
bin auto[196:199]	1536			Covered	
bin auto[200:203]	1641			Covered	
bin auto[204:207]	1451			Covered	
bin auto[208:211]	1536			Covered	
bin auto[212:215]	1353			Covered	
bin auto[216:219]	1396			Covered	
bin auto[220:223]	1501			Covered	
bin auto[224:227]	1536			Covered	
bin auto[228:231]	1536			Covered	
bin auto[232:235]	1536			Covered	
bin auto[236:239]	1440	1	-	Covered	
bin auto[240:243]	1536	1		Covered	

bin auto[244:247] 1536 1 - Covered bin auto[248:251] 1501 1 - Covered bin auto[252:255] 1466 1 - Covered Coverpoint address_written covered/total bins: 64 64 - Covered thit: 100.00% 100 - Covered bin auto[0:3] 75986 1 - Covered bin auto[8:17] 7969 1 - Covered bin auto[8:11] 3969 1 - Covered bin auto[12:15] 3969 1 - Covered bin auto[16:19] 1980 1 - Covered bin auto[20:23] 1957 1 - Covered bin auto[24:27] 1959 1 - Covered bin auto[28:31] 1979 1 - Covered bin auto[28:31] 1979 1 - Covered bin auto[28:31] 1979 1 - Covered bin auto[36:39] 972 1 - Covered bin auto[36:39] 972 1 - Covered bin auto[40:43] 962 1 - Covered bin auto[40:43] 963 1 - Covered bin auto[56:55] 964 1 - Covered bin auto[56:559] 969 1 - Covered bin auto[56:559] 969 1 - Covered bin auto[60:63] 978 1 - Covered	
bin auto[252:255]	
Coverpoint address_written covered/total bins: 64 64 - Covered cove	
covered/total bins: 64 64 - missing/total bins: 0 64 - % Hit: 100.00% 100 - bin auto[0:3] 75986 1 - Covered bin auto[8:11] 3969 1 - Covered bin auto[12:15] 3969 1 - Covered bin auto[16:19] 1980 1 - Covered bin auto[20:23] 1957 1 - Covered bin auto[24:27] 1959 1 - Covered bin auto[28:31] 1979 1 - Covered bin auto[36:39] 972 1 - Covered bin auto[40:43] 962 1 - Covered bin auto[48:51] 963 1 - Covered bin auto[52:55] 964 1 - Covered bin auto[52:59] 969 1 - Covered bin auto[60:63] 978 1 - Covered bin auto[64:67] 473 1 - Covered	
missing/total bins: 0 64 - % Hit: 100.00% 100 - bin auto[0:3] 75986 1 - Covered bin auto[4:7] 7969 1 - Covered bin auto[8:11] 3969 1 - Covered bin auto[16:19] 1980 1 - Covered bin auto[20:23] 1957 1 - Covered bin auto[28:31] 1979 1 - Covered bin auto[32:35] 976 1 - Covered bin auto[36:39] 972 1 - Covered bin auto[40:43] 962 1 - Covered bin auto[48:51] 963 1 - Covered bin auto[52:55] 964 1 - Covered bin auto[66:63] 978 1 - Covered bin auto[64:67] 473 1 - Covered	
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bin auto[16:19]	
bin auto[20:23] 1957 1 - Covered bin auto[24:27] 1959 1 - Covered bin auto[28:31] 1979 1 - Covered bin auto[32:35] 976 1 - Covered bin auto[36:39] 972 1 - Covered bin auto[40:43] 962 1 - Covered bin auto[44:47] 964 1 - Covered bin auto[48:51] 963 1 - Covered bin auto[52:55] 964 1 - Covered bin auto[56:59] 969 1 - Covered bin auto[60:63] 978 1 - Covered bin auto[64:67] 473 1 - Covered	
bin auto[24:27]	
bin auto[28:31] 1979 1 - Covered bin auto[32:35] 976 1 - Covered bin auto[36:39] 972 1 - Covered bin auto[40:43] 962 1 - Covered bin auto[44:47] 964 1 - Covered bin auto[48:51] 963 1 - Covered bin auto[52:55] 964 1 - Covered bin auto[56:59] 969 1 - Covered bin auto[60:63] 978 1 - Covered bin auto[64:67] 473 1 - Covered	
bin auto[32:35] 976 1 - Covered bin auto[36:39] 972 1 - Covered bin auto[40:43] 962 1 - Covered bin auto[44:47] 964 1 - Covered bin auto[48:51] 963 1 - Covered bin auto[52:55] 964 1 - Covered bin auto[56:59] 969 1 - Covered bin auto[60:63] 978 1 - Covered bin auto[64:67] 473 1 - Covered	
bin auto[36:39] 972 1 - Covered bin auto[40:43] 962 1 - Covered bin auto[44:47] 964 1 - Covered bin auto[48:51] 963 1 - Covered bin auto[52:55] 964 1 - Covered bin auto[56:59] 969 1 - Covered bin auto[60:63] 978 1 - Covered bin auto[64:67] 473 1 - Covered	
bin auto[40:43] 962 1 - Covered bin auto[44:47] 964 1 - Covered bin auto[48:51] 963 1 - Covered bin auto[52:55] 964 1 - Covered bin auto[56:59] 969 1 - Covered bin auto[60:63] 978 1 - Covered bin auto[64:67] 473 1 - Covered	
bin auto[44:47] 964 1 - Covered bin auto[48:51] 963 1 - Covered bin auto[52:55] 964 1 - Covered bin auto[56:59] 969 1 - Covered bin auto[60:63] 978 1 - Covered bin auto[64:67] 473 1 - Covered	
bin auto[48:51] 963 1 - Covered bin auto[52:55] 964 1 - Covered bin auto[56:59] 969 1 - Covered bin auto[60:63] 978 1 - Covered bin auto[64:67] 473 1 - Covered	
bin auto[52:55] 964 1 - Covered bin auto[56:59] 969 1 - Covered bin auto[60:63] 978 1 - Covered bin auto[64:67] 473 1 - Covered	
bin auto[56:59] 969 1 - Covered bin auto[60:63] 978 1 - Covered bin auto[64:67] 473 1 - Covered	
bin auto[56:59] 969 1 - Covered bin auto[60:63] 978 1 - Covered bin auto[64:67] 473 1 - Covered	
bin auto[60:63] 978 1 - Covered bin auto[64:67] 473 1 - Covered	
bin auto[64:67] 473 1 - Covered	
bin auto[68:71] 471 1 - Covered	
bin auto[72:75] 468 1 - Covered	
bin auto[76:79] 472 1 - Covered	
•	
bin auto[84:87] 468 1 - Covered	
bin auto[88:91] 468 1 - Covered	
bin auto[92:95] 464 1 - Covered	
bin auto[96:99] 463 1 - Covered	
bin auto[100:103] 468 1 - Covered	
bin auto[104:107] 469 1 - Covered	
bin auto[108:111] 465 1 - Covered	
bin auto[112:115] 468 1 - Covered	
bin auto[116:119] 469 1 - Covered	
bin auto[120:123] 474 1 - Covered	
bin auto[124:127] 473 1 - Covered	
bin auto[128:131] 220 1 - Covered	
bin auto[132:135] 222 1 - Covered	
bin auto[136:139] 221 1 - Covered bin auto[140:143] 218 1 - Covered	
·	
bin auto[144:147] 219 1 - Covered	
bin auto[148:151] 220 1 - Covered	
bin auto[152:155] 221 1 - Covered	
bin auto[156:159] 219 1 - Covered	
bin auto[160:163] 217 1 - Covered	
bin auto[164:167] 216 1 - Covered	
bin auto[168:171] 218 1 - Covered	
bin auto[172:175] 218 1 - Covered	
bin auto[176:179] 220 1 - Covered	
bin auto[180:183] 217 1 - Covered	
bin auto[184:187] 217 1 - Covered	
bin auto[188:191] 215 1 - Covered	
bin auto[192:195] 216 1 - Covered	
bin auto[196:199] 216 1 - Covered	
bin auto[200:203] 218 1 - Covered	
bin auto[204:207] 219 1 - Covered	
bin auto[208:211] 215 1 - Covered	
bin auto[212:215] 222 1 - Covered	
bin auto[216:219] 219 1 - Covered	
bin auto[220:223] 216 1 - Covered	
bin auto[224:227] 216 1 - Covered	
bin auto[228:231] 221 1 - Covered	
bin auto[232:235] 217 1 - Covered	

```
bin auto[236:239]
                                    221
                                                      Covered
                                            1
                                    222
 bin auto[240:243]
                                             1
                                                     Covered
 bin auto[244:247]
                                    220
                                                     Covered
                                    222
 bin auto[248:251]
                                             1
                                                     Covered
 bin auto[252:255]
                                    221
                                             1
                                                      Covered
Coverpoint address_read
                                     100.00%
                                                  100
                                                          - Covered
 covered/total bins:
                                    64
                                           64
 missing/total bins:
                                    0
                                          64
 % Hit:
                            100.00%
                                        100
 bin auto[0:3]
                               120043
                                            1
                                                     Covered
 bin auto[4:7]
                                  32
                                                  Covered
                                         1
 bin auto[8:11]
                                  32
                                                   Covered
                                          1
 bin auto[12:15]
                                   31
                                          1
                                                    Covered
 bin auto[16:19]
                                   32
                                          1
                                                    Covered
 bin auto[20:23]
                                   32
                                                    Covered
 bin auto[24:27]
                                   32
                                                    Covered
 bin auto[28:31]
                                   32
                                          1
                                                    Covered
 bin auto[32:35]
                                   32
                                          1
                                                    Covered
 bin auto[36:39]
                                   31
                                           1
                                                    Covered
                                   32
 bin auto[40:43]
                                           1
                                                    Covered
 bin auto[44:47]
                                   31
                                                    Covered
                                          1
                                   32
 bin auto[48:51]
                                                    Covered
 bin auto[52:55]
                                   29
                                                    Covered
 bin auto[56:59]
                                   32
                                          1
                                                    Covered
 bin auto[60:63]
                                   31
                                                    Covered
                                           1
 bin auto[64:67]
                                   32
                                                    Covered
 bin auto[68:71]
                                   30
                                           1
                                                    Covered
 bin auto[72:75]
                                   30
                                                    Covered
                                           1
 bin auto[76:79]
                                   32
                                                    Covered
 bin auto[80:83]
                                   31
                                           1
                                                    Covered
                                   32
 bin auto[84:87]
                                           1
                                                    Covered
 bin auto[88:91]
                                   32
                                           1
                                                    Covered
 bin auto[92:95]
                                   32
                                                    Covered
 bin auto[96:99]
                                   32
                                           1
                                                    Covered
 bin auto[100:103]
                                    31
                                                     Covered
                                            1
 bin auto[104:107]
                                    32
                                                     Covered
                                    30
 bin auto[108:111]
                                            1
                                                     Covered
 bin auto[112:115]
                                    31
                                            1
                                                     Covered
 bin auto[116:119]
                                    31
                                                     Covered
 bin auto[120:123]
                                    32
                                            1
                                                     Covered
 bin auto[124:127]
                                    32
                                                     Covered
                                            1
                                                     Covered
 bin auto[128:131]
                                    31
                                            1
 bin auto[132:135]
                                    32
                                            1
                                                     Covered
 bin auto[136:139]
                                    31
                                            1
                                                     Covered
 bin auto[140:143]
                                    31
                                            1
                                                     Covered
 bin auto[144:147]
                                    31
                                            1
                                                     Covered
                                    30
 bin auto[148:151]
                                            1
                                                     Covered
 bin auto[152:155]
                                    31
                                            1
                                                     Covered
 bin auto[156:159]
                                    31
                                                     Covered
 bin auto[160:163]
                                    32
                                            1
                                                     Covered
 bin auto[164:167]
                                    32
                                            1
                                                     Covered
 bin auto[168:171]
                                    30
                                            1
                                                     Covered
 bin auto[172:175]
                                    30
                                            1
                                                     Covered
 bin auto[176:179]
                                    32
                                                     Covered
                                            1
 bin auto[180:183]
                                    32
                                                     Covered
                                            1
 bin auto[184:187]
                                    30
                                                     Covered
 bin auto[188:191]
                                    31
                                            1
                                                     Covered
 bin auto[192:195]
                                    31
                                            1
                                                     Covered
 bin auto[196:199]
                                    32
                                            1
                                                     Covered
 bin auto[200:203]
                                    32
                                            1
                                                     Covered
 bin auto[204:207]
                                    31
                                            1
                                                     Covered
 bin auto[208:211]
                                    28
                                                     Covered
 bin auto[212:215]
                                    31
                                            1
                                                     Covered
 bin auto[216:219]
                                    32
                                            1
                                                     Covered
 bin auto[220:223]
                                    30
                                                     Covered
                                            1
 bin auto[224:227]
                                                     Covered
```

```
bin auto[228:231]
                                     31
                                            1
                                                      Covered
 bin auto[232:235]
                                     31
                                                     Covered
 bin auto[236:239]
                                     32
                                                     Covered
 bin auto[240:243]
                                     30
                                            1
                                                     Covered
 bin auto[244:247]
                                     32
                                                     Covered
                                            1
 bin auto[248:251]
                                     32
                                                      Covered
 bin auto[252:255]
                                     31
                                            1
                                                     Covered
                                     100.00%
Coverpoint receive_valid
                                                 100
                                                          - Covered
 covered/total bins:
                                     2
 missing/total bins:
                                     0
                                           2
                            100.00%
 % Hit:
                                         100
 bin receive asserted
                                    8000
                                                        Covered
 bin receive disable
                                   114012
                                               1
                                                        Covered
Coverpoint send_valid
                                    100.00%
                                                100
                                                         - Covered
 covered/total bins:
                                     2
                                           2
 missing/total bins:
                                     0
                                           2
 % Hit:
                            100.00%
                                         100
 bin send asserted
                                    2000
                                                       Covered
                                              1
 bin send_disable
                                  120012
Cross Writing_address
                                    100.00%
                                                100
                                                         - Covered
 covered/total bins:
                                    128
                                            128
 missing/total bins:
                                          128
                            100.00%
                                         100
 % Hit:
 Auto, Default and User Defined Bins:
    bin <auto[252:255],receive_disable>
                                            189
                                                              Covered
                                                     1
    bin <auto[248:251],receive_disable>
                                                              Covered
                                            190
                                                     1
   bin <auto[244:247],receive_disable>
                                            188
                                                     1
                                                              Covered
    bin <auto[240:243],receive_disable>
                                            192
                                                              Covered
                                                     1
                                                              Covered
    bin <auto[236:239],receive_disable>
                                            189
    bin <auto[232:235],receive_disable>
                                            186
                                                     1
                                                              Covered
                                            189
                                                              Covered
    bin <auto[228:231],receive_disable>
                                                     1
    bin <auto[224:227],receive_disable>
                                            186
                                                     1
                                                              Covered
    bin <auto[220:223],receive_disable>
                                            185
                                                     1
                                                              Covered
   bin <auto[216:219],receive_disable>
                                            188
                                                     1
                                                              Covered
                                            190
                                                              Covered
    bin <auto[212:215],receive_disable>
                                                     1
    bin <auto[208:211],receive_disable>
                                            185
                                                              Covered
                                            189
    bin <auto[204:207],receive_disable>
                                                     1
                                                              Covered
                                            186
                                                              Covered
    bin <auto[200:203],receive_disable>
                                                     1
    bin <auto[196:199],receive_disable>
                                            184
                                                              Covered
    bin <auto[192:195],receive_disable>
                                            185
                                                     1
                                                              Covered
                                                              Covered
    bin <auto[188:191],receive_disable>
                                            185
                                                     1
    bin <auto[184:187],receive_disable>
                                            187
                                                              Covered
    bin <auto[180:183],receive_disable>
                                            185
                                                     1
                                                              Covered
    bin <auto[176:179],receive_disable>
                                            188
                                                     1
                                                              Covered
    bin <auto[172:175],receive_disable>
                                            188
                                                     1
                                                              Covered
    bin <auto[168:171],receive_disable>
                                            186
                                                     1
                                                              Covered
   bin <auto[164:167],receive_disable>
                                            184
                                                     1
                                                              Covered
   bin <auto[160:163],receive_disable>
                                            186
                                                     1
                                                              Covered
   bin <auto[156:159], receive disable>
                                            188
                                                              Covered
   bin <auto[152:155],receive_disable>
                                            189
                                                              Covered
                                            191
                                                              Covered
    bin <auto[148:151],receive_disable>
                                                     1
    bin <auto[144:147],receive disable>
                                            187
                                                     1
                                                              Covered
   bin <auto[140:143],receive_disable>
                                            186
                                                     1
                                                              Covered
                                                              Covered
   bin <auto[136:139],receive_disable>
                                            190
                                                     1
   bin <auto[132:135],receive_disable>
                                            190
                                                              Covered
   bin <auto[128:131],receive_disable>
                                            189
                                                              Covered
   bin <auto[124:127],receive_disable>
                                            443
                                                     1
                                                              Covered
    bin <auto[120:123],receive disable>
                                            442
                                                     1
                                                              Covered
    bin <auto[116:119],receive_disable>
                                            438
                                                               Covered
   bin <auto[112:115],receive_disable>
                                            437
                                                     1
                                                              Covered
   bin <auto[108:111],receive_disable>
                                            435
                                                     1
                                                              Covered
    bin <auto[104:107],receive disable>
                                            437
                                                              Covered
    bin <auto[100:103],receive_disable>
                                            437
                                                              Covered
    bin <auto[96:99],receive_disable>
                                           432
                                                             Covered
                                                    1
    bin <auto[92:95],receive_disable>
                                           432
                                                             Covered
                                                   1
   bin <auto[88:91],receive_disable>
                                           437
                                                             Covered
```

 bin <auto[84:87],receive_disable></auto[84:87],receive_disable>	436	1	-	Covered
bin <auto[80:83],receive_disable></auto[80:83],receive_disable>	433	1	-	Covered
bin <auto[76:79],receive_disable></auto[76:79],receive_disable>	440	1	-	Covered
bin <auto[72:75],receive_disable></auto[72:75],receive_disable>	439	1	-	Covered
bin <auto[68:71],receive_disable></auto[68:71],receive_disable>	439	1	-	Covered
bin <auto[64:67],receive_disable></auto[64:67],receive_disable>	442	1	-	Covered
bin <auto[60:63],receive_disable></auto[60:63],receive_disable>	947	1		Covered
bin <auto[56:59],receive_disable></auto[56:59],receive_disable>	937	1		Covered
bin <auto[52:55],receive_disable></auto[52:55],receive_disable>	934	1		Covered
bin <auto[32:53],receive_disable></auto[32:53],receive_disable>	931	1		Covered
bin <auto[44:47],receive_disable></auto[44:47],receive_disable>	932	1		Covered
bin <auto[40:43],receive_disable></auto[40:43],receive_disable>	932	1		Covered
bin <auto[36:39],receive_disable></auto[36:39],receive_disable>	940	1		Covered
bin <auto[32:35],receive_disable></auto[32:35],receive_disable>	944	1		Covered
bin <auto[28:31],receive_disable></auto[28:31],receive_disable>	1947	1	-	Covered
bin <auto[24:27],receive_disable></auto[24:27],receive_disable>	1927	1	-	Covered
bin <auto[20:23],receive_disable></auto[20:23],receive_disable>	1926	1	-	Covered
bin <auto[16:19],receive_disable></auto[16:19],receive_disable>	1948	1	-	Covered
bin <auto[12:15],receive_disable></auto[12:15],receive_disable>	3938	1	-	Covered
bin <auto[8:11],receive_disable></auto[8:11],receive_disable>	3937	1	-	Covered
bin <auto[4:7],receive_disable></auto[4:7],receive_disable>	7938	1	- (Covered
	69955	1		Covered
bin <auto[252:255],receive_asserted></auto[252:255],receive_asserted>	32	1	_	Covered
bin <auto[232.253], receive_asserted=""></auto[232.253],>	32	1	-	Covered
	32	1		
bin <auto[244:247],receive_asserted></auto[244:247],receive_asserted>			-	Covered
bin <auto[240:243],receive_asserted></auto[240:243],receive_asserted>	30	1	-	Covered
bin <auto[236:239],receive_asserted></auto[236:239],receive_asserted>	32	1	-	Covered
bin <auto[232:235],receive_asserted></auto[232:235],receive_asserted>	31	1	-	Covered
bin <auto[228:231],receive_asserted></auto[228:231],receive_asserted>	32	1	-	Covered
bin <auto[224:227],receive_asserted></auto[224:227],receive_asserted>	30	1	-	Covered
bin <auto[220:223],receive_asserted></auto[220:223],receive_asserted>	31	1	-	Covered
bin <auto[216:219],receive_asserted></auto[216:219],receive_asserted>	31	1	-	Covered
bin <auto[212:215],receive_asserted></auto[212:215],receive_asserted>	32	1	-	Covered
bin <auto[208:211],receive_asserted></auto[208:211],receive_asserted>	30	1	-	Covered
bin <auto[204:207],receive_asserted></auto[204:207],receive_asserted>	30	1	_	Covered
bin <auto[200:203],receive_asserted></auto[200:203],receive_asserted>	32	1	_	Covered
bin <auto[196:199],receive_asserted></auto[196:199],receive_asserted>	32	1	_	Covered
bin <auto[190:195],receive_asserted></auto[190:195],receive_asserted>	31	1	_	
	30	1		Covered
bin <auto[188:191],receive_asserted></auto[188:191],receive_asserted>			-	
bin <auto[184:187],receive_asserted></auto[184:187],receive_asserted>	30	1	-	Covered
bin <auto[180:183],receive_asserted></auto[180:183],receive_asserted>	32	1	-	Covered
bin <auto[176:179],receive_asserted></auto[176:179],receive_asserted>	32	1	-	Covered
bin <auto[172:175],receive_asserted></auto[172:175],receive_asserted>	30	1	-	Covered
bin <auto[168:171],receive_asserted></auto[168:171],receive_asserted>	32	1	-	Covered
bin <auto[164:167],receive_asserted></auto[164:167],receive_asserted>	32	1	-	Covered
bin <auto[160:163],receive_asserted></auto[160:163],receive_asserted>	31	1	-	Covered
bin <auto[156:159],receive_asserted></auto[156:159],receive_asserted>	31	1	-	Covered
bin <auto[152:155],receive_asserted></auto[152:155],receive_asserted>	32	1	-	Covered
bin <auto[148:151],receive_asserted></auto[148:151],receive_asserted>	29	1	-	Covered
bin <auto[144:147],receive asserted=""></auto[144:147],receive>	32	1	_	Covered
bin <auto[144:147],receive_asserted></auto[144:147],receive_asserted>	32	1	_	Covered
bin <auto[140.143],receive_asserted></auto[140.143],receive_asserted>	31	1	_	Covered
			-	
bin <auto[132:135],receive_asserted></auto[132:135],receive_asserted>	32	1	-	Covered
bin <auto[128:131],receive_asserted></auto[128:131],receive_asserted>	31	1	-	Covered
bin <auto[124:127],receive_asserted></auto[124:127],receive_asserted>	30	1	-	Covered
bin <auto[120:123],receive_asserted></auto[120:123],receive_asserted>	32	1	-	Covered
bin <auto[116:119],receive_asserted></auto[116:119],receive_asserted>	31	1	-	Covered
bin <auto[112:115],receive_asserted></auto[112:115],receive_asserted>	31	1	-	Covered
bin <auto[108:111],receive_asserted></auto[108:111],receive_asserted>	30	1	-	Covered
bin <auto[104:107],receive_asserted></auto[104:107],receive_asserted>	32	1	-	Covered
bin <auto[100:103],receive_asserted></auto[100:103],receive_asserted>	31	1	_	Covered
bin <auto[96:99],receive_asserted></auto[96:99],receive_asserted>	31	1	_	Covered
bin <auto[92:95],receive_asserted></auto[92:95],receive_asserted>	32	1		Covered
bin <auto[88:91],receive_asserted></auto[88:91],receive_asserted>	31	1		Covered
bin <auto[84:87],receive_asserted></auto[84:87],receive_asserted>	32	1		Covered
· · · · =	31	1		
bin <auto[80:83],receive_asserted></auto[80:83],receive_asserted>	31	т	-	Covered

```
bin <auto[76:79],receive_asserted>
                                                            Covered
    bin <auto[72:75],receive asserted>
                                                            Covered
                                                   1
    bin <auto[68:71],receive_asserted>
                                                            Covered
    bin <auto[64:67],receive_asserted>
                                            31
                                                   1
                                                            Covered
    bin <auto[60:63],receive_asserted>
                                            31
                                                   1
                                                            Covered
    bin <auto[56:59],receive_asserted>
                                            32
                                                   1
                                                             Covered
   bin <auto[52:55],receive_asserted>
                                            30
                                                   1
                                                            Covered
                                                          - Covered
   bin <auto[48:51],receive asserted>
                                            32
                                                   1
    bin <auto[44:47],receive asserted>
                                                            Covered
   bin <auto[40:43],receive_asserted>
                                            30
                                                   1
                                                            Covered
    bin <auto[36:39],receive_asserted>
                                            32
                                                   1
                                                            Covered
    bin <auto[32:35],receive asserted>
                                            32
                                                   1
                                                            Covered
   bin <auto[28:31],receive_asserted>
                                            32
                                                   1
                                                            Covered
                                                         - Covered
   bin <auto[24:27],receive_asserted>
                                            32
                                                   1
   bin <auto[20:23],receive_asserted>
                                                          - Covered
                                                   1
   bin <auto[16:19],receive_asserted>
                                            32
                                                          - Covered
   bin <auto[12:15],receive_asserted>
                                            31
                                                            Covered
                                                   1
    bin <auto[8:11], receive asserted>
                                           32
                                                            Covered
                                                  1
                                          31
                                                           Covered
    bin <auto[4:7],receive_asserted>
   bin <auto[0:3],receive_asserted>
                                         6031
                                                   1
                                                          - Covered
Cross Writing_data
                                  100.00%
                                              100
                                                         Covered
 covered/total bins:
                                   128
                                           128
 missing/total bins:
                                         128
 % Hit:
                            100.00%
                                        100
 Auto, Default and User Defined Bins:
    bin <auto[252:255],receive_disable>
                                                             Covered
   bin <auto[248:251],receive_disable>
                                                             Covered
    bin <auto[244:247],receive_disable>
                                                             Covered
    bin <auto[240:243],receive_disable>
                                                             Covered
    bin <auto[236:239],receive_disable>
                                                             Covered
    bin <auto[232:235],receive_disable>
                                            61
                                                    1
                                                             Covered
    bin <auto[228:231],receive_disable>
                                                    1
                                                             Covered
    bin <auto[224:227],receive_disable>
                                            64
                                                             Covered
   bin <auto[220:223],receive_disable>
                                            64
                                                    1
                                                             Covered
    bin <auto[216:219],receive_disable>
                                                             Covered
                                            63
    bin <auto[212:215],receive_disable>
                                                             Covered
    bin <auto[208:211],receive_disable>
                                            63
                                                   1
                                                             Covered
    bin <auto[204:207],receive_disable>
                                            63
                                                             Covered
                                                    1
    bin <auto[200:203],receive_disable>
                                                             Covered
    bin <auto[196:199],receive_disable>
                                            61
                                                             Covered
    bin <auto[192:195],receive_disable>
                                                             Covered
    bin <auto[188:191],receive_disable>
                                                             Covered
    bin <auto[184:187],receive_disable>
                                                    1
                                                             Covered
    bin <auto[180:183],receive_disable>
                                            62
                                                    1
                                                             Covered
    bin <auto[176:179],receive_disable>
                                            64
                                                    1
                                                             Covered
    bin <auto[172:175],receive_disable>
                                            63
                                                             Covered
   bin <auto[168:171],receive_disable>
                                            63
                                                    1
                                                             Covered
   bin <auto[164:167], receive disable>
                                            61
                                                    1
                                                             Covered
    bin <auto[160:163],receive disable>
                                                             Covered
   bin <auto[156:159],receive_disable>
                                            63
                                                             Covered
    bin <auto[152:155],receive_disable>
                                            63
                                                    1
                                                             Covered
    bin <auto[148:151], receive disable>
                                                             Covered
   bin <auto[144:147],receive_disable>
                                            61
                                                             Covered
   bin <auto[140:143],receive_disable>
                                            62
                                                             Covered
   bin <auto[136:139],receive disable>
                                                             Covered
   bin <auto[132:135],receive_disable>
                                                             Covered
   bin <auto[128:131],receive_disable>
                                            61
                                                    1
                                                             Covered
    bin <auto[124:127],receive disable>
                                            63
                                                             Covered
                                                    1
    bin <auto[120:123],receive_disable>
                                                             Covered
   bin <auto[116:119],receive_disable>
                                            63
                                                    1
                                                             Covered
   bin <auto[112:115],receive_disable>
                                            62
                                                    1
                                                             Covered
    bin <auto[108:111],receive disable>
                                                             Covered
    bin <auto[104:107],receive_disable>
                                            59
                                                             Covered
    bin <auto[100:103],receive_disable>
                                            63
                                                   1
                                                             Covered
    bin <auto[96:99],receive_disable>
                                           63
                                                         - Covered
                                                  1
   bin <auto[92:95],receive_disable>
                                                            Covered
```

```
bin <auto[88:91],receive_disable>
                                              1
                                                        Covered
bin <auto[84:87], receive disable>
                                       60
                                                       Covered
                                              1
bin <auto[80:83],receive_disable>
                                       64
                                                        Covered
bin <auto[76:79],receive_disable>
                                       62
                                              1
                                                       Covered
bin <auto[72:75],receive_disable>
                                       61
                                                        Covered
                                              1
bin <auto[68:71],receive_disable>
                                       62
                                                        Covered
bin <auto[64:67],receive_disable>
                                       63
                                              1
                                                        Covered
                                                     - Covered
bin <auto[60:63],receive_disable>
                                       64
                                              1
bin <auto[56:59],receive disable>
                                                        Covered
bin <auto[52:55],receive_disable>
                                       62
                                              1
                                                     - Covered
bin <auto[48:51],receive_disable>
                                       63
                                              1
                                                        Covered
bin <auto[44:47],receive disable>
                                              1
                                                        Covered
bin <auto[40:43],receive_disable>
                                       63
                                              1
                                                        Covered
bin <auto[36:39],receive_disable>
                                       62
                                              1
                                                        Covered
bin <auto[32:35],receive_disable>
                                                       Covered
                                              1
bin <auto[28:31],receive_disable>
                                                     - Covered
                                       61
                                                     - Covered
bin <auto[24:27],receive_disable>
                                              1
bin <auto[20:23],receive_disable>
                                       63
                                                        Covered
                                              1
bin <auto[16:19],receive_disable>
                                       63
                                                        Covered
bin <auto[12:15],receive_disable>
                                       64
                                              1
                                                        Covered
bin <auto[8:11],receive_disable>
                                      64
                                                    - Covered
                                              1
bin <auto[4:7],receive disable>
                                                    - Covered
bin <auto[0:3],receive_disable>
                                    110075
                                                         Covered
bin <auto[252:255],receive_asserted>
                                                1
                                                         Covered
                                                          Covered
bin <auto[248:251],receive_asserted>
                                         32
                                                1
                                                          Covered
bin <auto[244:247],receive_asserted>
bin <auto[240:243],receive_asserted>
                                         32
                                                1
                                                         Covered
                                                         Covered
bin <auto[236:239],receive_asserted>
                                         31
                                                1
                                                          Covered
bin <auto[232:235],receive_asserted>
bin <auto[228:231],receive_asserted>
                                                1
                                                         Covered
                                         32
                                                         Covered
bin <auto[224:227],receive_asserted>
                                                1
bin <auto[220:223],receive_asserted>
                                         31
                                                1
                                                          Covered
bin <auto[216:219],receive_asserted>
                                         31
                                                 1
                                                          Covered
bin <auto[212:215],receive_asserted>
                                         29
                                                1
                                                          Covered
bin <auto[208:211],receive_asserted>
                                                          Covered
                                                1
bin <auto[204:207],receive_asserted>
                                                         Covered
                                                         Covered
bin <auto[200:203],receive_asserted>
                                         31
                                                1
                                                         Covered
bin <auto[196:199],receive_asserted>
                                         32
                                                1
bin <auto[192:195],receive_asserted>
                                                          Covered
bin <auto[188:191],receive_asserted>
                                         32
                                                1
                                                         Covered
                                                         Covered
bin <auto[184:187],receive_asserted>
                                                1
                                                          Covered
bin <auto[180:183],receive_asserted>
bin <auto[176:179],receive_asserted>
                                                1
                                                         Covered
bin <auto[172:175],receive_asserted>
                                         32
                                                1
                                                       - Covered
bin <auto[168:171],receive_asserted>
                                         32
                                                1
                                                         Covered
bin <auto[164:167],receive_asserted>
                                         31
                                                 1
                                                          Covered
                                                         Covered
bin <auto[160:163],receive_asserted>
                                         31
                                                1
                                                         Covered
bin <auto[156:159],receive_asserted>
                                         32
                                                1
bin <auto[152:155],receive asserted>
                                                          Covered
bin <auto[148:151],receive_asserted>
                                                1
                                                       - Covered
                                         30
                                                         Covered
bin <auto[144:147],receive_asserted>
                                                1
bin <auto[140:143],receive asserted>
                                         29
                                                1
                                                         Covered
bin <auto[136:139],receive_asserted>
                                         31
                                                1
                                                         Covered
                                                       - Covered
bin <auto[132:135],receive_asserted>
                                                1
bin <auto[128:131],receive asserted>
                                                         Covered
bin <auto[124:127],receive_asserted>
                                                         Covered
bin <auto[120:123],receive_asserted>
                                         28
                                                1
                                                       - Covered
bin <auto[116:119],receive asserted>
                                         31
                                                         Covered
                                                1
bin <auto[112:115],receive_asserted>
                                         31
                                                          Covered
bin <auto[108:111],receive_asserted>
                                         32
                                                1
                                                         Covered
                                                         Covered
bin <auto[104:107],receive_asserted>
                                         32
                                                1
bin <auto[100:103],receive asserted>
                                                          Covered
bin <auto[96:99],receive_asserted>
                                        30
                                               1
                                                        Covered
bin <auto[92:95],receive_asserted>
                                        31
                                               1
                                                        Covered
bin <auto[88:91],receive_asserted>
                                        32
                                                        Covered
                                               1
bin <auto[84:87],receive_asserted>
                                                        Covered
```

```
31
    bin <auto[80:83],receive_asserted>
                                                   1
                                                            Covered
    bin <auto[76:79],receive asserted>
                                                            Covered
                                                   1
    bin <auto[72:75],receive_asserted>
                                            31
                                                            Covered
    bin <auto[68:71],receive_asserted>
                                            32
                                                   1
                                                            Covered
    bin <auto[64:67],receive_asserted>
                                            29
                                                   1
                                                            Covered
    bin <auto[60:63],receive_asserted>
                                            31
                                                   1
                                                            Covered
   bin <auto[56:59],receive_asserted>
                                            31
                                                   1
                                                            Covered
   bin <auto[52:55],receive_asserted>
                                            32
                                                   1
                                                            Covered
   bin <auto[48:51],receive asserted>
                                                            Covered
   bin <auto[44:47],receive_asserted>
                                            32
                                                   1
                                                            Covered
    bin <auto[40:43],receive_asserted>
                                            32
                                                   1
                                                            Covered
                                                            Covered
    bin <auto[36:39],receive asserted>
                                            32
                                                   1
   bin <auto[32:35],receive_asserted>
                                            31
                                                   1
                                                            Covered
   bin <auto[28:31],receive_asserted>
                                            30
                                                   1
                                                            Covered
   bin <auto[24:27],receive_asserted>
                                                            Covered
                                                   1
   bin <auto[20:23],receive_asserted>
                                            32
                                                            Covered
   bin <auto[16:19],receive_asserted>
                                            32
                                                   1
                                                            Covered
    bin <auto[12:15],receive_asserted>
                                           31
                                                   1
                                                            Covered
    bin <auto[8:11],receive_asserted>
                                           31
                                                            Covered
   bin <auto[4:7],receive_asserted>
                                          31
                                                  1
                                                           Covered
   bin <auto[0:3],receive_asserted>
                                         6032
                                                            Covered
                                                   1
Cross reading address
                                                           Covered
 covered/total bins:
                                           64
 missing/total bins:
                                    0
                                          64
                                        100
 % Hit:
                            100.00%
 Auto, Default and User Defined Bins:
   bin <auto[252:255],receive_asserted>
                                             31
                                                     1

    Covered

   bin <auto[124:127],receive_asserted>
                                                              Covered
                                             32
                                                    1
                                                              Covered
    bin <auto[188:191],receive_asserted>
    bin <auto[60:63],receive_asserted>
                                            31
                                                          - Covered
                                             30
    bin <auto[220:223],receive_asserted>
                                                             Covered
                                                    1
    bin <auto[92:95],receive_asserted>
                                            32
                                                          - Covered
                                                   1
    bin <auto[156:159],receive_asserted>
                                             31
                                                             Covered
                                                          - Covered
   bin <auto[28:31],receive_asserted>
                                            32
                                                   1
   bin <auto[236:239],receive_asserted>
                                                           - Covered
    bin <auto[108:111],receive_asserted>
                                                             Covered
                                             30
    bin <auto[172:175],receive_asserted>
                                                    1
                                                             Covered
    bin <auto[44:47],receive_asserted>
                                            31
                                                            Covered
                                                   1
    bin <auto[204:207],receive_asserted>
                                                             Covered
                                                          - Covered
   bin <auto[76:79],receive_asserted>
                                            32
    bin <auto[140:143],receive_asserted>

    Covered

                                             31
                                                    1
    bin <auto[12:15],receive_asserted>
                                                          - Covered
    bin <auto[244:247],receive_asserted>
                                             32
                                                    1
                                                           - Covered
    bin <auto[116:119],receive_asserted>
                                             31
                                                           - Covered
                                                    1
    bin <auto[180:183],receive_asserted>
                                             32
                                                             Covered
                                                    1
    bin <auto[52:55],receive_asserted>
                                            29
                                                            Covered
   bin <auto[212:215],receive_asserted>
                                             31
                                                    1
                                                           - Covered
   bin <auto[84:87],receive asserted>
                                            32
                                                   1
                                                          - Covered
    bin <auto[148:151],receive asserted>

    Covered

   bin <auto[20:23],receive_asserted>
                                            32
                                                   1
                                                          - Covered
                                                           - Covered
    bin <auto[228:231],receive_asserted>
                                             31
                                                    1
    bin <auto[100:103],receive asserted>
                                             31
                                                    1
                                                              Covered
   bin <auto[164:167],receive_asserted>
                                             32
                                                    1
                                                             Covered
                                                          - Covered
   bin <auto[36:39],receive_asserted>
                                            31
   bin <auto[196:199],receive asserted>
                                             32
                                                           - Covered
   bin <auto[68:71],receive_asserted>
                                            30
                                                          - Covered
   bin <auto[132:135],receive_asserted>
                                             32
                                                    1
                                                           - Covered
                                          32
    bin <auto[4:7],receive asserted>
                                                          Covered
                                                  1
    bin <auto[248:251],receive_asserted>
                                             32
                                                              Covered
   bin <auto[120:123],receive_asserted>
                                             32
                                                    1
                                                             Covered
   bin <auto[184:187],receive_asserted>
                                             30
                                                             Covered
                                                    1
    bin <auto[56:59],receive asserted>
                                            32
                                                            Covered
    bin <auto[216:219],receive_asserted>
                                             32
                                                    1
                                                          - Covered
    bin <auto[88:91],receive_asserted>
                                            32
                                                   1
                                                            Covered
    bin <auto[152:155],receive_asserted>
                                            31
                                                           - Covered
                                                    1
   bin <auto[24:27],receive_asserted>
                                                            Covered
```

```
bin <auto[232:235],receive_asserted>
                                             31
                                                     1
                                                              Covered
    bin <auto[104:107],receive asserted>
                                             32
                                                              Covered
                                                     1
    bin <auto[168:171],receive_asserted>
                                             30
                                                              Covered
    bin <auto[40:43],receive_asserted>
                                            32
                                                    1
                                                             Covered
    bin <auto[200:203],receive_asserted>
                                             32
                                                              Covered
                                                     1
    bin <auto[72:75],receive_asserted>
                                            30
                                                             Covered
   bin <auto[136:139],receive_asserted>
                                             31
                                                     1
                                                              Covered
   bin <auto[8:11],receive asserted>
                                           32
                                                   1

    Covered

   bin <auto[240:243],receive asserted>
                                                              Covered
   bin <auto[112:115],receive_asserted>
                                             31
                                                     1
                                                              Covered
    bin <auto[176:179],receive_asserted>
                                             32
                                                     1
                                                              Covered
    bin <auto[48:51], receive asserted>
                                            32
                                                             Covered
   bin <auto[208:211],receive_asserted>
                                             28
                                                     1
                                                           - Covered
   bin <auto[80:83],receive_asserted>
                                            31
                                                    1
                                                          - Covered
   bin <auto[144:147],receive asserted>
                                                           - Covered
                                             31
   bin <auto[16:19],receive_asserted>
                                            32
                                                          - Covered
   bin <auto[224:227],receive_asserted>
                                             31
                                                     1
                                                              Covered
    bin <auto[96:99],receive_asserted>
                                                             Covered
                                            32
                                                    1
    bin <auto[160:163],receive_asserted>
                                                              Covered
   bin <auto[32:35],receive_asserted>
                                            32
                                                    1
                                                             Covered
   bin <auto[192:195],receive_asserted>
                                                              Covered
                                             31
                                                    1
   bin <auto[64:67],receive asserted>
                                            32
                                                             Covered
    bin <auto[128:131],receive_asserted>
                                             31
                                                              Covered
    bin <auto[0:3],receive_asserted>
                                          6031
                                                             Covered
 Illegal and Ignore Bins:
    ignore_bin ignore_bin1
                                     114012
                                                          Occurred
Cross reading_data
                                   100.00%
                                               100
                                                          Covered
                                           64
 covered/total bins:
                                    64
 missing/total bins:
                                          64
 % Hit:
                            100.00%
                                         100
 Auto, Default and User Defined Bins:
    bin <auto[252:255],receive_asserted>
                                             92
                                                              Covered
                                                     1
    bin <auto[124:127],receive_asserted>
                                             96
                                                              Covered
                                                     1
   bin <auto[188:191],receive_asserted>
                                             96
                                                     1
                                                              Covered
   bin <auto[60:63], receive asserted>
                                                             Covered
                                            86
                                                    1
    bin <auto[220:223],receive_asserted>
                                                              Covered
    bin <auto[92:95],receive_asserted>
                                            96
                                                    1
                                                             Covered
    bin <auto[156:159],receive_asserted>
                                             96
                                                              Covered
                                                     1
    bin <auto[28:31],receive_asserted>
                                                             Covered
   bin <auto[236:239],receive_asserted>
                                             90
                                                     1

    Covered

                                                              Covered
    bin <auto[108:111],receive_asserted>
                                             94
                                                     1
    bin <auto[172:175],receive_asserted>
                                                              Covered
    bin <auto[44:47],receive_asserted>
                                            96
                                                          - Covered
    bin <auto[204:207],receive_asserted>
                                             90
                                                              Covered
                                                     1
    bin <auto[76:79],receive asserted>
                                            84
                                                             Covered
                                                    1
    bin <auto[140:143],receive_asserted>
                                                              Covered
   bin <auto[12:15],receive_asserted>
                                            96
                                                    1
                                                             Covered
   bin <auto[244:247],receive asserted>
                                             96

    Covered

                                                     1
   bin <auto[116:119],receive asserted>
                                                              Covered
   bin <auto[180:183],receive_asserted>
                                             90
                                                              Covered
    bin <auto[52:55],receive_asserted>
                                            96
                                                             Covered
                                                    1
    bin <auto[212:215],receive asserted>
                                             84
                                                     1
                                                              Covered
   bin <auto[84:87],receive_asserted>
                                            96
                                                             Covered
   bin <auto[148:151],receive_asserted>
                                             96
                                                    1

    Covered

   bin <auto[20:23],receive asserted>
                                            96
                                                          - Covered
   bin <auto[228:231],receive_asserted>
                                             96
                                                              Covered
   bin <auto[100:103],receive_asserted>
                                             96
                                                     1
                                                           - Covered
    bin <auto[164:167],receive asserted>
                                             102
                                                               Covered
    bin <auto[36:39],receive_asserted>
                                            94
                                                             Covered
   bin <auto[196:199],receive_asserted>
                                             96
                                                     1
                                                              Covered
   bin <auto[68:71],receive_asserted>
                                            94
                                                    1
                                                          - Covered
    bin <auto[132:135],receive asserted>
                                                              Covered
    bin <auto[4:7],receive_asserted>
                                           86
                                                            Covered
    bin <auto[248:251],receive_asserted>
                                             94
                                                              Covered
                                                     1
                                             92
                                                              Covered
    bin <auto[120:123],receive_asserted>
                                                     1
   bin <auto[184:187],receive_asserted>
                                                              Covered
```

```
92
                                                      1
                                                               Covered
      bin <auto[56:59],receive_asserted>
      bin <auto[216:219],receive asserted>
                                               88
                                                                Covered
                                                       1
     bin <auto[88:91],receive_asserted>
                                              96
                                                            - Covered
     bin <auto[152:155],receive_asserted>
                                               84
                                                       1
                                                                Covered
      bin <auto[24:27],receive_asserted>
                                              96
                                                               Covered
                                                      1
      bin <auto[232:235],receive_asserted>
                                               96
                                                                Covered
     bin <auto[104:107],receive_asserted>
                                               96
                                                       1
                                                                Covered
     bin <auto[168:171],receive asserted>
                                               96
                                                                Covered
                                                       1
     bin <auto[40:43],receive asserted>
                                              96
                                                               Covered
     bin <auto[200:203],receive_asserted>
                                               102
                                                       1
                                                                 Covered
     bin <auto[72:75],receive_asserted>
                                              98
                                                      1
                                                               Covered
      bin <auto[136:139],receive asserted>
                                              104
                                                       1
                                                                 Covered
     bin <auto[8:11],receive_asserted>
                                              92
                                                              Covered
     bin <auto[240:243],receive_asserted>
                                               96
                                                       1
                                                                Covered
     bin <auto[112:115],receive_asserted>
                                               96
                                                                Covered
                                                       1
     bin <auto[176:179],receive_asserted>
                                               96
                                                                Covered
     bin <auto[48:51],receive_asserted>
                                              96
                                                      1

    Covered

      bin <auto[208:211],receive asserted>
                                               96
                                                       1
                                                                Covered
      bin <auto[80:83],receive_asserted>
                                              96
                                                               Covered
     bin <auto[144:147],receive_asserted>
                                               90
                                                       1
                                                                Covered
     bin <auto[16:19],receive_asserted>
                                              96
                                                            - Covered
                                                      1
     bin <auto[224:227],receive asserted>
                                                                Covered
      bin <auto[96:99],receive_asserted>
                                              80
                                                               Covered
     bin <auto[160:163],receive_asserted>
                                               92
                                                       1
                                                                Covered
                                              92
      bin <auto[32:35],receive_asserted>
                                                      1
                                                               Covered
      bin <auto[192:195],receive_asserted>
                                               100
                                                                 Covered
     bin <auto[64:67],receive_asserted>
                                              80
                                                      1
                                                            - Covered
     bin <auto[128:131],receive_asserted>
                                               92

    Covered

                                                       1
     bin <auto[0:3],receive_asserted>
                                            2118
                                                               Covered
   Illegal and Ignore Bins:
                                       114012
      ignore_bin ignore_bin1
                                                         - Occurred
TYPE /SPI_coverage_pkg/SPI_coverage/SPI_Wrapper
                                                     100.00%
                                                                          - Covered
 covered/total bins:
                                      522
                                             522
 missing/total bins:
                                      0
                                            522
 % Hit:
                              100.00%
                                           100
 Coverpoint reset
                                   100.00%
                                                           Covered
                                               100
   covered/total bins:
                                       2
                                             2
                                      0
   missing/total bins:
                                             2
   % Hit:
                              100.00%
                                           100
 Coverpoint Address_write
                                       100.00%
                                                    100
                                                                Covered
   covered/total bins:
                                      64
                                             64
   missing/total bins:
                                      0
                                            64
   % Hit:
                              100.00%
                                           100
 Coverpoint Data_write
                                      100.00%
                                                   100
                                                             Covered
   covered/total bins:
                                      64
                                             64
   missing/total bins:
                                      0
                                            64
                              100.00%
   % Hit:
                                           100
 Coverpoint Data read
                                      100.00%
                                                  100
                                                             Covered
   covered/total bins:
                                      64
                                             64
   missing/total bins:
                                      0
                                            64
   % Hit:
                              100.00%
                                           100
 Coverpoint Address read
                                       100.00%
                                                    100
                                                               Covered
   covered/total bins:
                                      64
                                             64
   missing/total bins:
                                      0
                                            64
                              100.00%
                                           100
 Coverpoint Send_Address_wr
                                          100.00%
                                                       100
                                                                 Covered
   covered/total bins:
                                       1
                                             1
   missing/total bins:
                                      0
                                             1
   % Hit:
                              100.00%
                                           100
 Coverpoint Send_Address_rd
                                         100.00%
                                                      100
                                                                 Covered
   covered/total bins:
                                       1
                                             1
   missing/total bins:
                              100.00%
   % Hit:
                                           100
 Coverpoint send_Data_wr
                                        100.00%
                                                     100

    Covered

   covered/total bins:
                                       1
                                             1
   missing/total bins:
```

```
% Hit:
                              100.00%
                                          100
                                         100.00%
 Coverpoint Recieving_Data_rd
                                                      100
                                                               - Covered
   covered/total bins:
   missing/total bins:
                                      0
                                            1
   % Hit:
                              100.00%
                                          100
 Coverpoint Sending_order_Read_data
                                              100.00%
                                                          100
                                                                      Covered
   covered/total bins:
                                             1
   missing/total bins:
                                            1
   % Hit:
                              100.00%
                                          100
 Coverpoint Starting_Communication
                                            100.00%
                                                         100
                                                                  - Covered
   covered/total bins:
                                      3
                                             3
   missing/total bins:
                                      0
                                            3
   % Hit:
                              100.00%
                                          100
                                                       100
 Cross Actualiy_sending_addr_wr
                                           100.00%
                                                                - Covered
   covered/total bins:
                                      64
                                             64
   missing/total bins:
                                            64
                              100.00%
   % Hit:
                                          100
 Cross Actualiy_sending_data_wr
                                          100.00%
                                                       100
                                                                  Covered
   covered/total bins:
                                      64
                                             64
   missing/total bins:
                                            64
   % Hit:
                              100.00%
                                          100
 Cross Actualiy_sending_addr_rd
                                          100.00%
                                                      100
                                                               - Covered
   covered/total bins:
   missing/total bins:
                                      0
                                            64
   % Hit:
                              100.00%
                                          100
 Cross Actualiy_recieving_data
                                        100.00%
                                                     100
                                                                Covered
   covered/total bins:
                                      64
                                             64
   missing/total bins:
                                      0
                                            64
                              100.00%
                                          100
Covergroup instance \SPI_coverage_pkg::SPI_coverage::SPI_Wrapper
                           100.00%
                                        100
                                                   Covered
 covered/total bins:
                                      522
                                             522
 missing/total bins:
                                      0
                                           522
                                          100
 % Hit:
                              100.00%
 Coverpoint reset
                                   100.00%
                                               100
                                                          Covered
   covered/total bins:
                                       2
                                             2
   missing/total bins:
                                      0
   % Hit:
                              100.00%
                                          100
   bin reset_asserted
                                      12
                                                       Covered
   bin reset_disable
                                   122000
                                                         Covered
 Coverpoint Address_write
                                       100.00%
                                                    100
                                                             - Covered
   covered/total bins:
   missing/total bins:
                                      0
                                            64
                              100.00%
   % Hit:
                                          100
   bin auto[0:3]
                                 121028
                                                       Covered
   bin auto[4:7]
                                    16
                                                    Covered
   bin auto[8:11]
                                    16
                                            1
                                                     Covered
   bin auto[12:15]
                                     15
                                            1
                                                     Covered
   bin auto[16:19]
                                     16
                                                      Covered
   bin auto[20:23]
                                     16
                                            1
                                                      Covered
   bin auto[24:27]
                                     16
                                            1
                                                      Covered
   bin auto[28:31]
                                     16
                                                      Covered
   bin auto[32:35]
                                     16
                                                      Covered
   bin auto[36:39]
                                     16
                                                      Covered
   bin auto[40:43]
                                     16
                                                      Covered
   bin auto[44:47]
                                     16
                                                      Covered
   bin auto[48:51]
                                     16
                                            1
                                                      Covered
   bin auto[52:55]
                                     14
                                            1
                                                      Covered
   bin auto[56:59]
                                     16
                                                      Covered
   bin auto[60:63]
                                     15
                                            1
                                                      Covered
   bin auto[64:67]
                                     16
                                            1
                                                      Covered
   bin auto[68:71]
                                     16
                                            1
                                                      Covered
   bin auto[72:75]
                                     15
                                            1
                                                      Covered
   bin auto[76:79]
                                     16
                                            1
                                                      Covered
   bin auto[80:83]
                                     15
                                                      Covered
                                            1
   bin auto[84:87]
                                     16
                                                      Covered
```

```
bin auto[88:91]
                                   16
                                           1
                                                    Covered
 bin auto[92:95]
                                   16
                                           1
                                                    Covered
 bin auto[96:99]
                                   16
                                                    Covered
 bin auto[100:103]
                                    15
                                           1
                                                     Covered
 bin auto[104:107]
                                    16
                                                     Covered
                                            1
 bin auto[108:111]
                                    16
                                                     Covered
                                    15
 bin auto[112:115]
                                            1
                                                     Covered
                                    15
 bin auto[116:119]
                                            1
                                                     Covered
 bin auto[120:123]
                                                     Covered
                                    16
 bin auto[124:127]
                                    16
                                            1
                                                     Covered
 bin auto[128:131]
                                    15
                                            1
                                                     Covered
 bin auto[132:135]
                                    16
                                                     Covered
                                            1
 bin auto[136:139]
                                    15
                                            1
                                                     Covered
 bin auto[140:143]
                                    16
                                            1
                                                     Covered
 bin auto[144:147]
                                    16
                                            1
                                                     Covered
 bin auto[148:151]
                                    16
                                                     Covered
 bin auto[152:155]
                                    16
                                            1
                                                     Covered
 bin auto[156:159]
                                    15
                                            1
                                                     Covered
 bin auto[160:163]
                                    16
                                            1
                                                     Covered
 bin auto[164:167]
                                    16
                                            1
                                                     Covered
 bin auto[168:171]
                                    16
                                                     Covered
                                            1
 bin auto[172:175]
                                    14
                                                     Covered
 bin auto[176:179]
                                    16
                                                     Covered
 bin auto[180:183]
                                    16
                                            1
                                                     Covered
 bin auto[184:187]
                                    14
                                                     Covered
                                            1
 bin auto[188:191]
                                    15
                                                     Covered
 bin auto[192:195]
                                    15
                                            1
                                                     Covered
 bin auto[196:199]
                                                     Covered
                                    16
                                            1
 bin auto[200:203]
                                                     Covered
                                    16
                                            1
 bin auto[204:207]
                                    15
                                            1
                                                     Covered
 bin auto[208:211]
                                    14
                                            1
                                                     Covered
 bin auto[212:215]
                                    16
                                            1
                                                     Covered
 bin auto[216:219]
                                    16
                                            1
                                                     Covered
 bin auto[220:223]
                                    15
                                            1
                                                     Covered
 bin auto[224:227]
                                    15
                                                     Covered
                                            1
 bin auto[228:231]
                                    16
                                                     Covered
                                    16
 bin auto[232:235]
                                            1
                                                     Covered
                                    16
 bin auto[236:239]
                                            1
                                                     Covered
 bin auto[240:243]
                                    15
                                                     Covered
 bin auto[244:247]
                                    16
                                            1
                                                     Covered
 bin auto[248:251]
                                    16
                                                     Covered
                                            1
 bin auto[252:255]
                                    16
                                            1
                                                     Covered
Coverpoint Data_write
                                    100.00%
                                                100
                                                         - Covered
 covered/total bins:
                                    64
                                           64
 missing/total bins:
                                    0
                                          64
 % Hit:
                            100.00%
                                        100
 bin auto[0:3]
                               121028
                                            1
                                                     Covered
 bin auto[4:7]
                                  16
                                         1
                                                  Covered
 bin auto[8:11]
                                  15
                                          1
                                                   Covered
 bin auto[12:15]
                                   16
                                          1
                                                    Covered
 bin auto[16:19]
                                   16
                                                    Covered
                                          1
 bin auto[20:23]
                                   16
                                                    Covered
 bin auto[24:27]
                                   16
                                                    Covered
 bin auto[28:31]
                                   15
                                                    Covered
 bin auto[32:35]
                                   15
                                                    Covered
 bin auto[36:39]
                                   16
                                                    Covered
 bin auto[40:43]
                                   16
                                          1
                                                    Covered
 bin auto[44:47]
                                   16
                                          1
                                                    Covered
 bin auto[48:51]
                                   16
                                                    Covered
 bin auto[52:55]
                                   16
                                           1
                                                    Covered
 bin auto[56:59]
                                   16
                                          1
                                                    Covered
 bin auto[60:63]
                                   15
                                                    Covered
                                           1
 bin auto[64:67]
                                   14
                                           1
                                                    Covered
                                   16
 bin auto[68:71]
                                           1
                                                    Covered
 bin auto[72:75]
                                   15
                                                    Covered
                                           1
 bin auto[76:79]
                                                    Covered
```

```
bin auto[80:83]
                                   16
                                           1
                                                    Covered
 bin auto[84:87]
                                   16
                                           1
                                                    Covered
 bin auto[88:91]
                                   16
                                                    Covered
 bin auto[92:95]
                                   16
                                           1
                                                    Covered
 bin auto[96:99]
                                   16
                                           1
                                                    Covered
 bin auto[100:103]
                                    16
                                                     Covered
 bin auto[104:107]
                                    16
                                            1
                                                     Covered
 bin auto[108:111]
                                    16
                                            1
                                                     Covered
 bin auto[112:115]
                                                     Covered
                                    16
 bin auto[116:119]
                                    15
                                            1
                                                     Covered
 bin auto[120:123]
                                    13
                                            1
                                                     Covered
 bin auto[124:127]
                                    16
                                            1
                                                     Covered
 bin auto[128:131]
                                    15
                                            1
                                                     Covered
 bin auto[132:135]
                                    15
                                            1
                                                     Covered
 bin auto[136:139]
                                    16
                                            1
                                                     Covered
 bin auto[140:143]
                                    14
                                                     Covered
 bin auto[144:147]
                                    15
                                            1
                                                     Covered
 bin auto[148:151]
                                    16
                                            1
                                                     Covered
 bin auto[152:155]
                                    15
                                                     Covered
                                            1
 bin auto[156:159]
                                    16
                                            1
                                                     Covered
 bin auto[160:163]
                                    15
                                                     Covered
                                            1
 bin auto[164:167]
                                    16
                                                     Covered
 bin auto[168:171]
                                    16
                                                     Covered
 bin auto[172:175]
                                    16
                                            1
                                                     Covered
 bin auto[176:179]
                                    16
                                                     Covered
                                            1
 bin auto[180:183]
                                    15
                                                     Covered
 bin auto[184:187]
                                    16
                                            1
                                                     Covered
 bin auto[188:191]
                                                     Covered
                                    16
                                            1
 bin auto[192:195]
                                                     Covered
                                    16
                                            1
 bin auto[196:199]
                                    16
                                            1
                                                     Covered
 bin auto[200:203]
                                    16
                                            1
                                                     Covered
 bin auto[204:207]
                                    16
                                            1
                                                     Covered
 bin auto[208:211]
                                    16
                                            1
                                                     Covered
 bin auto[212:215]
                                    13
                                            1
                                                     Covered
 bin auto[216:219]
                                    16
                                                     Covered
                                            1
 bin auto[220:223]
                                    16
                                                     Covered
                                    16
 bin auto[224:227]
                                            1
                                                     Covered
                                    16
 bin auto[228:231]
                                                     Covered
                                            1
 bin auto[232:235]
                                    16
                                                     Covered
 bin auto[236:239]
                                    15
                                            1
                                                     Covered
 bin auto[240:243]
                                                     Covered
                                    16
                                            1
 bin auto[244:247]
                                                     Covered
                                    16
 bin auto[248:251]
                                    16
                                            1
                                                     Covered
 bin auto[252:255]
                                    16
                                            1
                                                     Covered
Coverpoint Data read
                                    100.00%
                                                100
                                                         - Covered
 covered/total bins:
                                    64
                                           64
 missing/total bins:
                                    0
                                          64
                            100.00%
                                         100
 % Hit:
 bin auto[0:3]
                                121028
                                                     Covered
 bin auto[4:7]
                                  16
                                         1
                                                   Covered
 bin auto[8:11]
                                  15
                                          1
                                                   Covered
 bin auto[12:15]
                                   16
                                          1
                                                    Covered
 bin auto[16:19]
                                   16
                                                    Covered
 bin auto[20:23]
                                   16
                                                    Covered
                                          1
 bin auto[24:27]
                                   16
                                                    Covered
 bin auto[28:31]
                                   15
                                                    Covered
 bin auto[32:35]
                                   15
                                          1
                                                    Covered
 bin auto[36:39]
                                   16
                                          1
                                                    Covered
 bin auto[40:43]
                                   16
                                                    Covered
 bin auto[44:47]
                                   16
                                           1
                                                    Covered
 bin auto[48:51]
                                   16
                                          1
                                                    Covered
 bin auto[52:55]
                                                    Covered
                                   16
                                          1
 bin auto[56:59]
                                   16
                                           1
                                                    Covered
 bin auto[60:63]
                                   15
                                           1
                                                    Covered
 bin auto[64:67]
                                   14
                                                    Covered
                                           1
 bin auto[68:71]
                                                    Covered
```

```
bin auto[72:75]
                                   15
                                          1
                                                    Covered
 bin auto[76:79]
                                   15
                                          1
                                                    Covered
 bin auto[80:83]
                                   16
                                                    Covered
 bin auto[84:87]
                                   16
                                          1
                                                    Covered
 bin auto[88:91]
                                   16
                                          1
                                                    Covered
 bin auto[92:95]
                                   16
                                                    Covered
 bin auto[96:99]
                                   16
                                          1
                                                    Covered
 bin auto[100:103]
                                    16
                                           1
                                                     Covered
 bin auto[104:107]
                                                     Covered
                                    16
 bin auto[108:111]
                                    16
                                            1
                                                     Covered
 bin auto[112:115]
                                    16
                                           1
                                                     Covered
 bin auto[116:119]
                                    15
                                                     Covered
                                           1
 bin auto[120:123]
                                    13
                                            1
                                                     Covered
 bin auto[124:127]
                                    16
                                           1
                                                     Covered
 bin auto[128:131]
                                    15
                                           1
                                                     Covered
 bin auto[132:135]
                                    15
                                                     Covered
 bin auto[136:139]
                                    16
                                           1
                                                     Covered
 bin auto[140:143]
                                    14
                                           1
                                                     Covered
 bin auto[144:147]
                                    15
                                                     Covered
                                            1
 bin auto[148:151]
                                    16
                                            1
                                                     Covered
 bin auto[152:155]
                                    15
                                                     Covered
                                            1
 bin auto[156:159]
                                    16
                                                     Covered
 bin auto[160:163]
                                    15
                                                     Covered
 bin auto[164:167]
                                    16
                                           1
                                                     Covered
 bin auto[168:171]
                                    16
                                                     Covered
                                           1
 bin auto[172:175]
                                    16
                                                     Covered
 bin auto[176:179]
                                    16
                                            1
                                                     Covered
 bin auto[180:183]
                                    15
                                                     Covered
                                           1
 bin auto[184:187]
                                                     Covered
                                    16
                                            1
 bin auto[188:191]
                                    16
                                            1
                                                     Covered
 bin auto[192:195]
                                    16
                                           1
                                                     Covered
 bin auto[196:199]
                                    16
                                           1
                                                     Covered
 bin auto[200:203]
                                    16
                                            1
                                                     Covered
 bin auto[204:207]
                                    16
                                            1
                                                     Covered
 bin auto[208:211]
                                    16
                                                     Covered
                                            1
 bin auto[212:215]
                                    13
                                                     Covered
 bin auto[216:219]
                                    16
                                           1
                                                     Covered
                                    16
 bin auto[220:223]
                                           1
                                                     Covered
 bin auto[224:227]
                                    16
                                                     Covered
 bin auto[228:231]
                                    16
                                            1
                                                     Covered
 bin auto[232:235]
                                                     Covered
                                    16
                                           1
                                                     Covered
 bin auto[236:239]
                                    15
                                            1
 bin auto[240:243]
                                    16
                                            1
                                                     Covered
 bin auto[244:247]
                                    16
                                           1
                                                     Covered
 bin auto[248:251]
                                    16
                                           1
                                                     Covered
 bin auto[252:255]
                                    16
                                            1
                                                     Covered
                                                  100
                                                          - Covered
Coverpoint Address_read
                                     100.00%
 covered/total bins:
                                    64
                                           64
 missing/total bins:
                                          64
                            100.00%
 % Hit:
                                        100
 bin auto[0:3]
                               121028
                                                     Covered
                                            1
 bin auto[4:7]
                                  16
                                                  Covered
 bin auto[8:11]
                                  16
                                          1
                                                   Covered
 bin auto[12:15]
                                   15
                                                   Covered
                                          1
 bin auto[16:19]
                                   16
                                                    Covered
                                          1
 bin auto[20:23]
                                   16
                                                    Covered
 bin auto[24:27]
                                   16
                                          1
                                                    Covered
 bin auto[28:31]
                                   16
                                          1
                                                    Covered
 bin auto[32:35]
                                   16
                                                    Covered
 bin auto[36:39]
                                   16
                                          1
                                                    Covered
 bin auto[40:43]
                                   16
                                          1
                                                    Covered
 bin auto[44:47]
                                                    Covered
                                   16
                                          1
 bin auto[48:51]
                                   16
                                          1
                                                    Covered
 bin auto[52:55]
                                   14
                                          1
                                                    Covered
 bin auto[56:59]
                                   16
                                                    Covered
                                          1
 bin auto[60:63]
                                                    Covered
```

```
bin auto[64:67]
                                   16
                                           1
                                                    Covered
 bin auto[68:71]
                                   16
                                                    Covered
 bin auto[72:75]
                                   15
                                                    Covered
 bin auto[76:79]
                                   16
                                          1
                                                    Covered
 bin auto[80:83]
                                   15
                                          1
                                                    Covered
 bin auto[84:87]
                                   16
                                                    Covered
 bin auto[88:91]
                                   16
                                           1
                                                    Covered
 bin auto[92:95]
                                   16
                                           1
                                                    Covered
 bin auto[96:99]
                                   16
                                                    Covered
 bin auto[100:103]
                                    15
                                            1
                                                     Covered
 bin auto[104:107]
                                    16
                                            1
                                                     Covered
 bin auto[108:111]
                                    16
                                                     Covered
                                            1
 bin auto[112:115]
                                    15
                                            1
                                                     Covered
 bin auto[116:119]
                                    15
                                            1
                                                     Covered
 bin auto[120:123]
                                    16
                                                     Covered
                                            1
 bin auto[124:127]
                                    16
                                                     Covered
 bin auto[128:131]
                                    15
                                            1
                                                     Covered
 bin auto[132:135]
                                    16
                                            1
                                                     Covered
 bin auto[136:139]
                                    15
                                                     Covered
                                            1
 bin auto[140:143]
                                    16
                                            1
                                                     Covered
 bin auto[144:147]
                                    16
                                                     Covered
                                            1
 bin auto[148:151]
                                    16
                                                     Covered
 bin auto[152:155]
                                    16
                                                     Covered
 bin auto[156:159]
                                    15
                                            1
                                                     Covered
 bin auto[160:163]
                                    16
                                                     Covered
                                            1
 bin auto[164:167]
                                    16
                                                     Covered
 bin auto[168:171]
                                    16
                                            1
                                                     Covered
 bin auto[172:175]
                                                     Covered
                                    14
                                            1
 bin auto[176:179]
                                                     Covered
                                    16
 bin auto[180:183]
                                    16
                                            1
                                                     Covered
 bin auto[184:187]
                                    14
                                            1
                                                     Covered
 bin auto[188:191]
                                    15
                                            1
                                                     Covered
 bin auto[192:195]
                                    15
                                            1
                                                     Covered
 bin auto[196:199]
                                    16
                                            1
                                                     Covered
 bin auto[200:203]
                                    16
                                                     Covered
                                            1
 bin auto[204:207]
                                    15
                                                     Covered
 bin auto[208:211]
                                    14
                                            1
                                                     Covered
                                    16
 bin auto[212:215]
                                                     Covered
                                            1
 bin auto[216:219]
                                    16
                                                     Covered
 bin auto[220:223]
                                    15
                                            1
                                                     Covered
 bin auto[224:227]
                                                     Covered
                                    15
                                            1
 bin auto[228:231]
                                    16
                                                     Covered
 bin auto[232:235]
                                    16
                                            1
                                                     Covered
 bin auto[236:239]
                                    16
                                            1
                                                     Covered
 bin auto[240:243]
                                    15
                                                     Covered
                                            1
 bin auto[244:247]
                                    16
                                                     Covered
 bin auto[248:251]
                                    16
                                            1
                                                     Covered
 bin auto[252:255]
                                    16
                                            1
                                                     Covered
Coverpoint Send Address wr
                                        100.00%
                                                             - Covered
 covered/total bins:
                                     1
                                           1
 missing/total bins:
                                    O
                                           1
 % Hit:
                            100.00%
                                        100
 bin writing_add
                                  11000
                                                     Covered
Coverpoint Send_Address_rd
                                       100.00%
                                                    100

    Covered

 covered/total bins:
                                     1
                                           1
 missing/total bins:
                                    0
                                        100
 % Hit:
                            100.00%
 bin reading add
                                  11000
                                                      Covered
                                             1
Coverpoint send_Data_wr
                                      100.00%
                                                  100
                                                             Covered
 covered/total bins:
                                           1
 missing/total bins:
                                    O
                                           1
                            100.00%
 % Hit:
                                        100
 bin writing_data
                                  11000
                                             1
                                                     Covered
Coverpoint Recieving_Data_rd
                                       100.00%
                                                    100
                                                            - Covered
  covered/total bins:
                                     1
                                           1
  missing/total bins:
```

```
% Hit:
                            100.00%
                                        100
 bin reading data
                                   8000
                                            1
                                                      Covered
Coverpoint Sending_order_Read_data
                                            100.00%
                                                        100
                                                                    Covered
 covered/total bins:
                                     1
                                           1
 missing/total bins:
                                    0
                                          1
 % Hit:
                            100.00%
                                        100
 bin order_reading_data
                                     11000
                                                1
                                                       - Covered
                                          100.00%
Coverpoint Starting_Communication
                                                       100
                                                               - Covered
 covered/total bins:
 missing/total bins:
                                    0
                                          3
 % Hit:
                            100.00%
                                        100
 bin Start
                             114000
                                          1
                                                   Covered
 bin End
                              8012
                                        1
                                                  Covered
                                    7988
 bin transaction_back
                                              1

    Covered

Cross Actually sending addr wr
                                         100.00%
                                                     100
                                                             - Covered
 covered/total bins:
                                    64
                                           64
                                          64
 missing/total bins:
                                    0
                            100.00%
                                        100
 % Hit:
 Auto, Default and User Defined Bins:
   bin <writing_add,auto[252:255]>
                                           16
                                                  1
                                                            Covered
   bin <writing_add,auto[248:251]>
                                                            Covered
                                           16
                                                  1
   bin <writing add,auto[244:247]>
                                           16
                                                  1
                                                            Covered
    bin <writing_add,auto[240:243]>
                                           15
                                                            Covered
   bin <writing_add,auto[236:239]>
                                           16
                                                  1
                                                            Covered
    bin <writing_add,auto[232:235]>
                                           16
                                                  1
                                                            Covered
    bin <writing_add,auto[228:231]>
                                           16
                                                  1
                                                            Covered
    bin <writing_add,auto[224:227]>
                                           15
                                                  1
                                                            Covered
    bin <writing_add,auto[220:223]>
                                           15
                                                  1
                                                            Covered
    bin <writing_add,auto[216:219]>
                                           16
                                                  1
                                                            Covered
    bin <writing_add,auto[212:215]>
                                           16
                                                  1
                                                            Covered
    bin <writing_add,auto[208:211]>
                                           14
                                                  1
                                                            Covered
    bin <writing_add,auto[204:207]>
                                           15
                                                  1
                                                            Covered
    bin <writing_add,auto[200:203]>
                                           16
                                                  1
                                                            Covered
   bin <writing_add,auto[196:199]>
                                           16
                                                  1
                                                            Covered
   bin <writing_add,auto[192:195]>
                                                            Covered
                                           15
                                                  1
    bin <writing_add,auto[188:191]>
                                                            Covered
    bin <writing_add,auto[184:187]>
                                           14
                                                  1
                                                            Covered
    bin <writing_add,auto[180:183]>
                                           16
                                                  1
                                                            Covered
    bin <writing_add,auto[176:179]>
                                           16
                                                  1
                                                            Covered
    bin <writing_add,auto[172:175]>
                                           14
                                                  1
                                                            Covered
    bin <writing_add,auto[168:171]>
                                           16
                                                  1
                                                            Covered
    bin <writing_add,auto[164:167]>
                                           16
                                                  1
                                                            Covered
    bin <writing_add,auto[160:163]>
                                           16
                                                  1
                                                            Covered
   bin <writing_add,auto[156:159]>
                                           15
                                                  1
                                                            Covered
    bin <writing_add,auto[152:155]>
                                           16
                                                  1
                                                            Covered
    bin <writing_add,auto[148:151]>
                                           16
                                                  1
                                                            Covered
   bin <writing_add,auto[144:147]>
                                           16
                                                  1
                                                            Covered
   bin <writing_add,auto[140:143]>
                                           16
                                                  1
                                                            Covered
   bin <writing add,auto[136:139]>
                                           15
                                                            Covered
   bin <writing_add,auto[132:135]>
                                           16
                                                  1
                                                            Covered
    bin <writing_add,auto[128:131]>
                                           15
                                                  1
                                                            Covered
    bin <writing add,auto[124:127]>
                                           16
                                                  1
                                                            Covered
   bin <writing_add,auto[120:123]>
                                           16
                                                  1
                                                            Covered
   bin <writing_add,auto[116:119]>
                                           15
                                                  1
                                                            Covered
   bin <writing_add,auto[112:115]>
                                           15
                                                            Covered
                                                  1
    bin <writing_add,auto[108:111]>
                                                            Covered
                                           16
   bin <writing_add,auto[104:107]>
                                           16
                                                  1
                                                            Covered
                                           15
    bin <writing add,auto[100:103]>
                                                  1
                                                            Covered
    bin <writing_add,auto[96:99]>
                                          16
                                                 1
                                                           Covered
   bin <writing_add,auto[92:95]>
                                          16
                                                 1
                                                           Covered
   bin <writing_add,auto[88:91]>
                                          16
                                                 1
                                                          Covered
   bin <writing add,auto[84:87]>
                                          16
                                                          Covered
   bin <writing_add,auto[80:83]>
                                          15
                                                 1
                                                           Covered
                                          16
                                                 1
    bin <writing_add,auto[76:79]>
                                                          Covered
                                          15
    bin <writing_add,auto[72:75]>
                                                 1
                                                          Covered
    bin <writing_add,auto[68:71]>
                                          16
                                                           Covered
```

```
bin <writing_add,auto[64:67]>
                                          16
                                                           Covered
    bin <writing add,auto[60:63]>
                                          15
                                                          Covered
    bin <writing_add,auto[56:59]>
                                          16
                                                          Covered
    bin <writing_add,auto[52:55]>
                                          14
                                                 1
                                                          Covered
                                          16
    bin <writing_add,auto[48:51]>
                                                 1
                                                           Covered
    bin <writing_add,auto[44:47]>
                                          16
                                                           Covered
   bin <writing_add,auto[40:43]>
                                          16
                                                 1
                                                           Covered
   bin <writing add,auto[36:39]>
                                          16
                                                 1
                                                          Covered
   bin <writing add,auto[32:35]>
                                          16
                                                          Covered
   bin <writing_add,auto[28:31]>
                                          16
                                                 1
                                                          Covered
    bin <writing_add,auto[24:27]>
                                          16
                                                 1
                                                          Covered
    bin <writing add,auto[20:23]>
                                          16
                                                 1
                                                           Covered
   bin <writing_add,auto[16:19]>
                                          16
                                                           Covered
   bin <writing_add,auto[12:15]>
                                          15
                                                 1
                                                          Covered
   bin <writing_add,auto[8:11]>
                                         16
                                                          Covered
   bin <writing_add,auto[4:7]>
                                         16
                                                       - Covered
   bin <writing_add,auto[0:3]>
                                       10016
                                                  1

    Covered

                                        100.00%
Cross Actualiy_sending_data_wr
                                                     100
                                                              - Covered
 covered/total bins:
                                           64
 missing/total bins:
                                    O
                                          64
 % Hit:
                            100.00%
                                        100
 Auto, Default and User Defined Bins:
    bin <writing_data,auto[252:255]>
                                                            Covered
                                           16
    bin <writing_data,auto[248:251]>
                                           16
                                                  1
                                                            Covered
    bin <writing_data,auto[244:247]>
                                           16
                                                            Covered
                                                   1
    bin <writing_data,auto[240:243]>
                                           16
                                                   1
                                                            Covered
   bin <writing_data,auto[236:239]>
                                           15
                                                   1
                                                            Covered
    bin <writing_data,auto[232:235]>
                                           16
                                                            Covered
                                                   1
    bin <writing_data,auto[228:231]>
                                           16
                                                   1
                                                            Covered
    bin <writing_data,auto[224:227]>
                                           16
                                                   1
                                                            Covered
    bin <writing_data,auto[220:223]>
                                           16
                                                  1
                                                            Covered
    bin <writing_data,auto[216:219]>
                                           16
                                                  1
                                                            Covered
    bin <writing_data,auto[212:215]>
                                           13
                                                   1
                                                            Covered
   bin <writing_data,auto[208:211]>
                                           16
                                                  1
                                                            Covered
    bin <writing_data,auto[204:207]>
                                           16
                                                   1
                                                            Covered
    bin <writing_data,auto[200:203]>
                                                            Covered
    bin <writing_data,auto[196:199]>
                                           16
                                                  1
                                                            Covered
    bin <writing_data,auto[192:195]>
                                           16
                                                  1
                                                            Covered
    bin <writing_data,auto[188:191]>
                                           16
                                                   1
                                                            Covered
    bin <writing_data,auto[184:187]>
                                           16
                                                  1
                                                            Covered
    bin <writing_data,auto[180:183]>
                                                            Covered
                                           15
                                                   1
    bin <writing_data,auto[176:179]>
                                           16
                                                   1
                                                            Covered
    bin <writing_data,auto[172:175]>
                                           16
                                                   1
                                                            Covered
   bin <writing_data,auto[168:171]>
                                           16
                                                  1
                                                            Covered
    bin <writing_data,auto[164:167]>
                                           16
                                                  1
                                                            Covered
    bin <writing_data,auto[160:163]>
                                           15
                                                   1
                                                            Covered
   bin <writing_data,auto[156:159]>
                                           16
                                                  1
                                                            Covered
   bin <writing_data,auto[152:155]>
                                           15
                                                            Covered
                                                  1
   bin <writing data,auto[148:151]>
                                           16
                                                   1
                                                            Covered
   bin <writing_data,auto[144:147]>
                                           15
                                                   1
                                                            Covered
    bin <writing_data,auto[140:143]>
                                           14
                                                  1
                                                            Covered
    bin <writing_data,auto[136:139]>
                                           16
                                                  1
                                                            Covered
   bin <writing_data,auto[132:135]>
                                           15
                                                   1
                                                            Covered
   bin <writing_data,auto[128:131]>
                                           15
                                                  1
                                                            Covered
                                                            Covered
   bin <writing_data,auto[124:127]>
                                           16
                                                  1
                                                            Covered
    bin <writing_data,auto[120:123]>
   bin <writing_data,auto[116:119]>
                                           15
                                                  1
                                                            Covered
    bin <writing data,auto[112:115]>
                                           16
                                                  1
                                                            Covered
    bin <writing_data,auto[108:111]>
                                           16
                                                  1
                                                            Covered
   bin <writing_data,auto[104:107]>
                                           16
                                                  1
                                                            Covered
   bin <writing_data,auto[100:103]>
                                           16
                                                            Covered
                                                  1
   bin <writing data,auto[96:99]>
                                          16
                                                 1
                                                           Covered
    bin <writing_data,auto[92:95]>
                                          16
                                                 1
                                                           Covered
                                          16
                                                 1
    bin <writing_data,auto[88:91]>
                                                           Covered
    bin < writing_data, auto[84:87]>
                                          16
                                                           Covered
                                                 1
    bin <writing_data,auto[80:83]>
                                                           Covered
```

```
15
    bin < writing_data, auto [76:79] >
                                                 1
                                                           Covered
    bin <writing data,auto[72:75]>
                                          15
                                                           Covered
    bin <writing_data,auto[68:71]>
                                          16
                                                           Covered
    bin <writing_data,auto[64:67]>
                                          14
                                                 1
                                                           Covered
    bin <writing_data,auto[60:63]>
                                          15
                                                           Covered
                                                 1
    bin <writing_data,auto[56:59]>
                                          16
                                                           Covered
    bin <writing_data,auto[52:55]>
                                          16
                                                 1
                                                           Covered
    bin <writing data,auto[48:51]>
                                          16
                                                 1
                                                           Covered
    bin <writing data,auto[44:47]>
                                          16
                                                           Covered
    bin <writing_data,auto[40:43]>
                                          16
                                                 1
                                                           Covered
    bin <writing_data,auto[36:39]>
                                          16
                                                 1
                                                           Covered
    bin <writing data,auto[32:35]>
                                          15
                                                 1
                                                           Covered
    bin <writing_data,auto[28:31]>
                                          15
                                                 1
                                                           Covered
    bin <writing_data,auto[24:27]>
                                          16
                                                 1
                                                           Covered
    bin <writing_data,auto[20:23]>
                                          16
                                                           Covered
    bin <writing_data,auto[16:19]>
                                          16
                                                           Covered
    bin <writing_data,auto[12:15]>
                                          16
                                                 1
                                                          Covered
                                         15
    bin < writing_data, auto[8:11]>
                                                 1
                                                          Covered
                                         16
    bin <writing_data,auto[4:7]>
                                                         Covered
    bin <writing_data,auto[0:3]>
                                       10016
                                                  1
                                                           Covered
Cross Actualiy_sending_addr_rd
                                        100.00%
                                                             - Covered
                                                    100
 covered/total bins:
                                           64
  missing/total bins:
                                          64
 % Hit:
                            100.00%
                                        100
  Auto, Default and User Defined Bins:
    bin <reading_add,auto[252:255]>
                                                            Covered
                                            16
    bin <reading_add,auto[248:251]>
                                            16
                                                   1
                                                            Covered
    bin <reading_add,auto[244:247]>
                                            16
                                                            Covered
                                                   1
    bin <reading_add,auto[240:243]>
                                            15
                                                            Covered
    bin <reading_add,auto[236:239]>
                                            16
                                                   1
                                                            Covered
    bin <reading_add,auto[232:235]>
                                            16
                                                            Covered
                                                   1
    bin <reading_add,auto[228:231]>
                                            16
                                                   1
                                                             Covered
    bin <reading_add,auto[224:227]>
                                            15
                                                             Covered
                                                   1
    bin <reading_add,auto[220:223]>
                                            15
                                                   1
                                                            Covered
    bin <reading_add,auto[216:219]>
                                                            Covered
                                            16
                                                   1
    bin <reading_add,auto[212:215]>
                                                             Covered
    bin <reading_add,auto[208:211]>
                                            14
                                                   1
                                                            Covered
    bin <reading_add,auto[204:207]>
                                            15
                                                            Covered
                                                   1
    bin <reading_add,auto[200:203]>
                                            16
                                                             Covered
    bin <reading_add,auto[196:199]>
                                            16
                                                   1
                                                            Covered
    bin <reading_add,auto[192:195]>
                                            15
                                                            Covered
                                                   1
    bin <reading_add,auto[188:191]>
                                            15
                                                   1
                                                            Covered
    bin <reading_add,auto[184:187]>
                                            14
                                                   1
                                                            Covered
    bin <reading_add,auto[180:183]>
                                            16
                                                   1
                                                            Covered
    bin <reading_add,auto[176:179]>
                                            16
                                                   1
                                                            Covered
    bin <reading_add,auto[172:175]>
                                            14
                                                             Covered
                                                   1
    bin <reading_add,auto[168:171]>
                                            16
                                                   1
                                                            Covered
    bin <reading add,auto[164:167]>
                                            16
                                                   1
                                                            Covered
    bin <reading add,auto[160:163]>
                                            16
                                                            Covered
    bin <reading_add,auto[156:159]>
                                            15
                                                   1
                                                            Covered
    bin <reading_add,auto[152:155]>
                                            16
                                                   1
                                                            Covered
    bin <reading add,auto[148:151]>
                                            16
                                                   1
                                                            Covered
    bin <reading_add,auto[144:147]>
                                            16
                                                   1
                                                            Covered
    bin <reading_add,auto[140:143]>
                                            16
                                                   1
                                                            Covered
    bin <reading_add,auto[136:139]>
                                                            Covered
                                            15
                                                   1
    bin <reading_add,auto[132:135]>
                                                            Covered
    bin <reading_add,auto[128:131]>
                                            15
                                                   1
                                                            Covered
    bin <reading add,auto[124:127]>
                                            16
                                                   1
                                                            Covered
    bin <reading_add,auto[120:123]>
                                            16
                                                   1
                                                             Covered
    bin <reading_add,auto[116:119]>
                                            15
                                                   1
                                                            Covered
    bin <reading_add,auto[112:115]>
                                            15
                                                            Covered
                                                   1
    bin <reading add,auto[108:111]>
                                            16
                                                            Covered
    bin <reading_add,auto[104:107]>
                                            16
                                                   1
                                                            Covered
    bin <reading_add,auto[100:103]>
                                           15
                                                   1
                                                            Covered
    bin <reading_add,auto[96:99]>
                                          16
                                                           Covered
                                                  1
    bin <reading_add,auto[92:95]>
                                          16
                                                           Covered
```

```
bin <reading_add,auto[88:91]>
                                          16
                                                 1
                                                          Covered
    bin <reading add,auto[84:87]>
                                          16
                                                          Covered
    bin <reading_add,auto[80:83]>
                                          15
                                                          Covered
   bin <reading_add,auto[76:79]>
                                          16
                                                 1

    Covered

    bin <reading_add,auto[72:75]>
                                          15
                                                 1
                                                          Covered
    bin <reading_add,auto[68:71]>
                                          16
                                                           Covered
   bin <reading_add,auto[64:67]>
                                          16
                                                 1
                                                          Covered
   bin <reading add,auto[60:63]>
                                          15
                                                 1
                                                          Covered
   bin <reading add,auto[56:59]>
                                          16
                                                          Covered
   bin <reading_add,auto[52:55]>
                                          14
                                                 1
                                                          Covered
    bin <reading_add,auto[48:51]>
                                          16
                                                 1
                                                          Covered
    bin <reading add,auto[44:47]>
                                          16
                                                 1
                                                          Covered
   bin <reading_add,auto[40:43]>
                                          16
                                                 1
                                                          Covered
   bin <reading_add,auto[36:39]>
                                          16
                                                 1
                                                          Covered
   bin <reading_add,auto[32:35]>
                                                          Covered
                                          16
   bin <reading_add,auto[28:31]>
                                          16
                                                       - Covered
                                          16
   bin <reading_add,auto[24:27]>
                                                 1

    Covered

    bin <reading_add,auto[20:23]>
                                          16
                                                 1
                                                          Covered
    bin <reading_add,auto[16:19]>
                                          16
                                                          Covered
   bin <reading_add,auto[12:15]>
                                          15
                                                 1
                                                          Covered
   bin <reading_add,auto[8:11]>
                                         16
                                                 1
                                                          Covered
   bin <reading add,auto[4:7]>
                                        16
                                                         Covered
   bin <reading_add,auto[0:3]>
                                       10016
                                                  1
                                                           Covered
Cross Actualiy_recieving_data
                                      100.00%
                                                  100
                                                           - Covered
 covered/total bins:
                                    64
                                          64
                                          64
 missing/total bins:
                                    0
 % Hit:
                            100.00%
                                        100
 Auto, Default and User Defined Bins:
    bin <reading_data,auto[252:255]>
                                           16
                                                            Covered
    bin <reading_data,auto[248:251]>
                                           16
                                                            Covered
    bin <reading_data,auto[244:247]>
                                           16
                                                            Covered
                                                  1
    bin <reading_data,auto[240:243]>
                                           16
                                                  1
                                                            Covered
    bin <reading_data,auto[236:239]>
                                           15
                                                   1
                                                            Covered
   bin <reading_data,auto[232:235]>
                                           16
                                                  1
                                                            Covered
   bin <reading_data,auto[228:231]>
                                                            Covered
                                           16
                                                  1
    bin <reading_data,auto[224:227]>
                                                            Covered
    bin <reading_data,auto[220:223]>
                                           16
                                                  1
                                                            Covered
    bin <reading_data,auto[216:219]>
                                           16
                                                  1
                                                            Covered
    bin <reading_data,auto[212:215]>
                                           13
                                                  1
                                                            Covered
   bin <reading_data,auto[208:211]>
                                           16
                                                  1
                                                            Covered
    bin <reading_data,auto[204:207]>
                                           16
                                                  1
                                                            Covered
    bin <reading_data,auto[200:203]>
                                           16
                                                  1
                                                            Covered
    bin <reading_data,auto[196:199]>
                                           16
                                                  1
                                                            Covered
   bin <reading_data,auto[192:195]>
                                           16
                                                            Covered
                                                  1
    bin <reading_data,auto[188:191]>
                                           16
                                                  1
                                                            Covered
    bin <reading_data,auto[184:187]>
                                           16
                                                            Covered
                                                   1
   bin <reading_data,auto[180:183]>
                                           15
                                                  1
                                                            Covered
   bin <reading data,auto[176:179]>
                                           16
                                                  1
                                                            Covered
   bin <reading data,auto[172:175]>
                                           16
                                                            Covered
   bin <reading_data,auto[168:171]>
                                           16
                                                  1
                                                            Covered
    bin <reading_data,auto[164:167]>
                                           16
                                                  1
                                                            Covered
    bin <reading data,auto[160:163]>
                                           15
                                                  1
                                                            Covered
   bin <reading_data,auto[156:159]>
                                           16
                                                  1
                                                            Covered
   bin <reading_data,auto[152:155]>
                                           15
                                                  1
                                                            Covered
   bin <reading_data,auto[148:151]>
                                                            Covered
                                           16
                                                  1
   bin <reading_data,auto[144:147]>
                                                            Covered
   bin <reading_data,auto[140:143]>
                                           14
                                                  1
                                                            Covered
                                           16
   bin <reading data,auto[136:139]>
                                                  1
                                                            Covered
    bin <reading_data,auto[132:135]>
                                           15
                                                   1
                                                            Covered
   bin <reading_data,auto[128:131]>
                                           15
                                                  1
                                                            Covered
   bin <reading_data,auto[124:127]>
                                           16
                                                  1
                                                            Covered
   bin <reading data,auto[120:123]>
                                           13
                                                            Covered
   bin <reading_data,auto[116:119]>
                                           15
                                                  1
                                                            Covered
    bin <reading_data,auto[112:115]>
                                           16
                                                  1
                                                            Covered
    bin <reading_data,auto[108:111]>
                                           16
                                                  1
                                                            Covered
   bin <reading_data,auto[104:107]>
                                                            Covered
```

bin <reading_data,auto[100:103]></reading_data,auto[100:103]>	16	1	- Covered
bin <reading_data,auto[96:99]></reading_data,auto[96:99]>	16	1	 Covered
bin <reading_data,auto[92:95]></reading_data,auto[92:95]>	16	1	 Covered
bin <reading_data,auto[88:91]></reading_data,auto[88:91]>	16	1	 Covered
bin <reading_data,auto[84:87]></reading_data,auto[84:87]>	16	1	 Covered
bin <reading_data,auto[80:83]></reading_data,auto[80:83]>	16	1	 Covered
bin <reading_data,auto[76:79]></reading_data,auto[76:79]>	15	1	 Covered
bin <reading_data,auto[72:75]></reading_data,auto[72:75]>	15	1	 Covered
bin <reading_data,auto[68:71]></reading_data,auto[68:71]>	16	1	 Covered
bin <reading_data,auto[64:67]></reading_data,auto[64:67]>	14	1	 Covered
bin <reading_data,auto[60:63]></reading_data,auto[60:63]>	15	1	 Covered
bin <reading_data,auto[56:59]></reading_data,auto[56:59]>	16	1	 Covered
bin <reading_data,auto[52:55]></reading_data,auto[52:55]>	16	1	 Covered
bin <reading_data,auto[48:51]></reading_data,auto[48:51]>	16	1	 Covered
bin <reading_data,auto[44:47]></reading_data,auto[44:47]>	16	1	 Covered
bin <reading_data,auto[40:43]></reading_data,auto[40:43]>	16	1	 Covered
bin <reading_data,auto[36:39]></reading_data,auto[36:39]>	16	1	 Covered
bin <reading_data,auto[32:35]></reading_data,auto[32:35]>	15	1	 Covered
bin <reading_data,auto[28:31]></reading_data,auto[28:31]>	15	1	 Covered
bin <reading_data,auto[24:27]></reading_data,auto[24:27]>	16	1	 Covered
bin <reading_data,auto[20:23]></reading_data,auto[20:23]>	16	1	 Covered
bin <reading_data,auto[16:19]></reading_data,auto[16:19]>	16	1	 Covered
bin <reading_data,auto[12:15]></reading_data,auto[12:15]>	16	1	 Covered
bin <reading_data,auto[8:11]></reading_data,auto[8:11]>	15	1	 Covered
bin <reading_data,auto[4:7]></reading_data,auto[4:7]>	16	1	- Covered
bin <reading_data,auto[0:3]></reading_data,auto[0:3]>	7016	1	 Covered

TOTAL COVERGROUP COVERAGE: 100.00% COVERGROUP TYPES: 2

Total Coverage By Instance (filtered view): 100.00%