

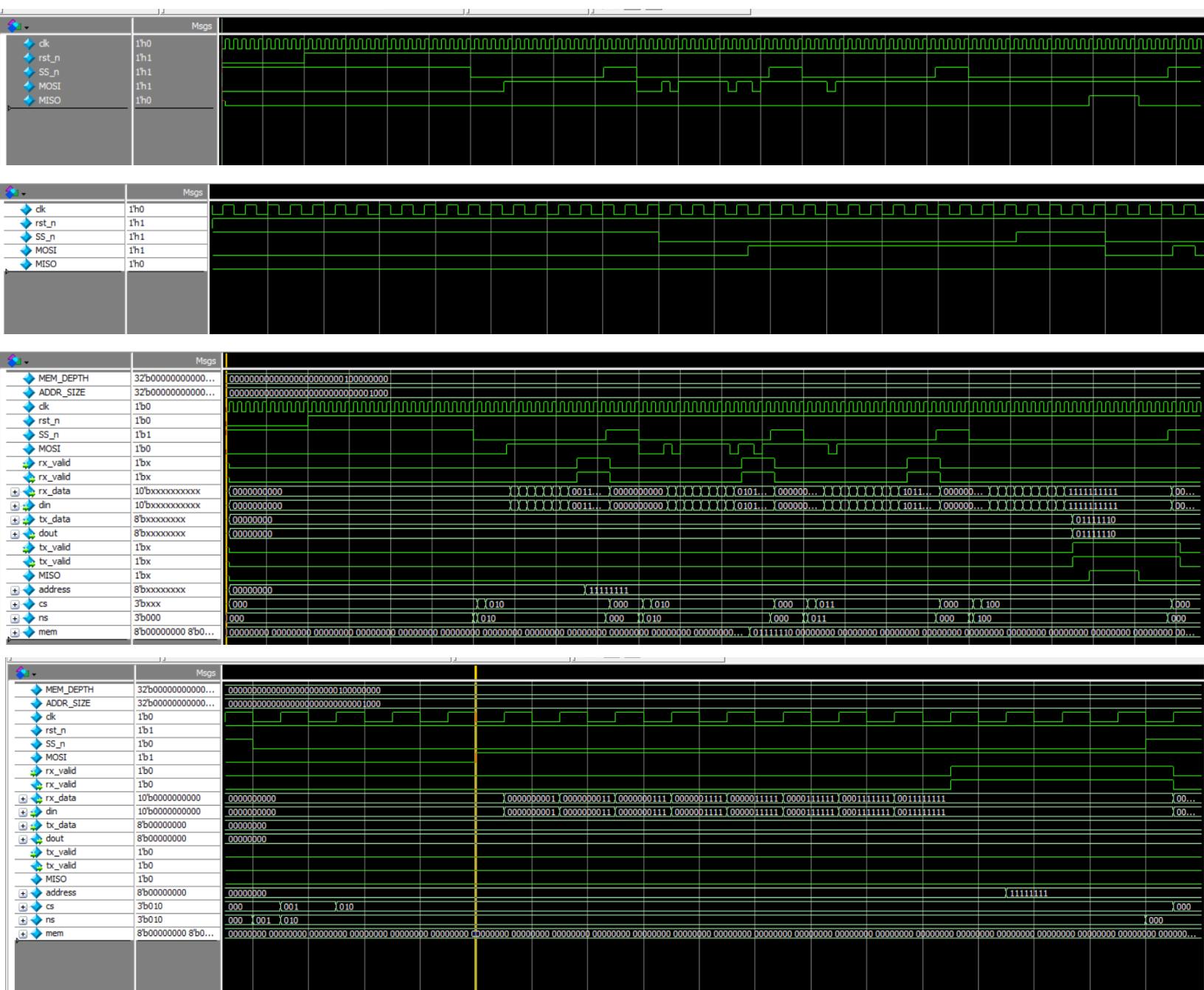
# Project2 SPI

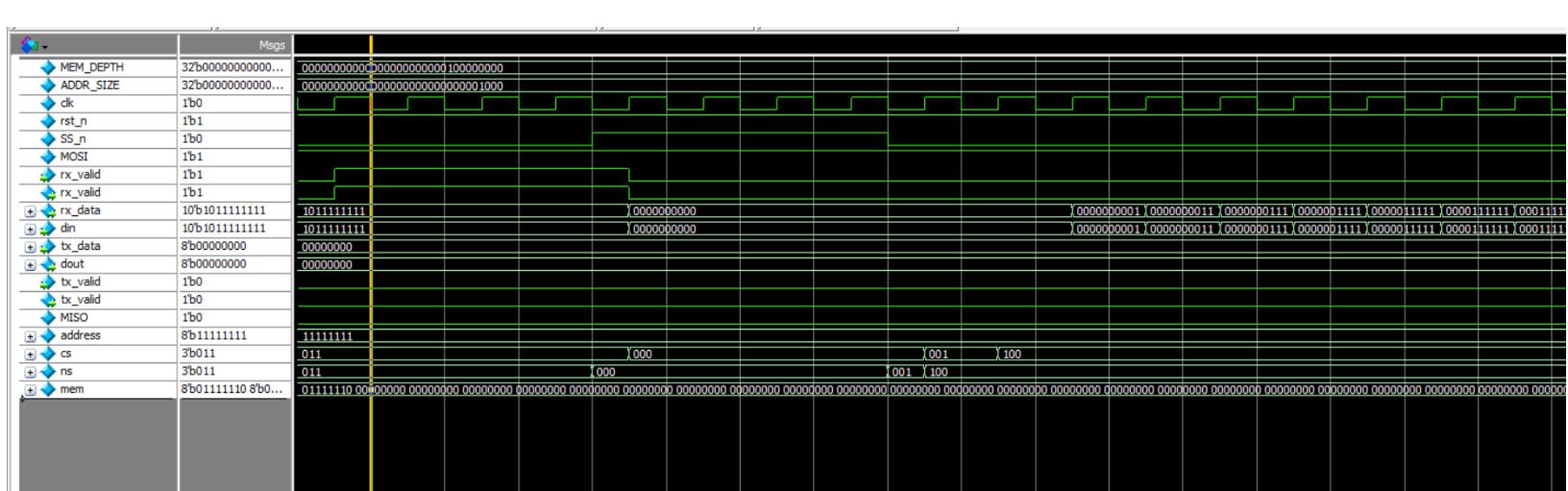
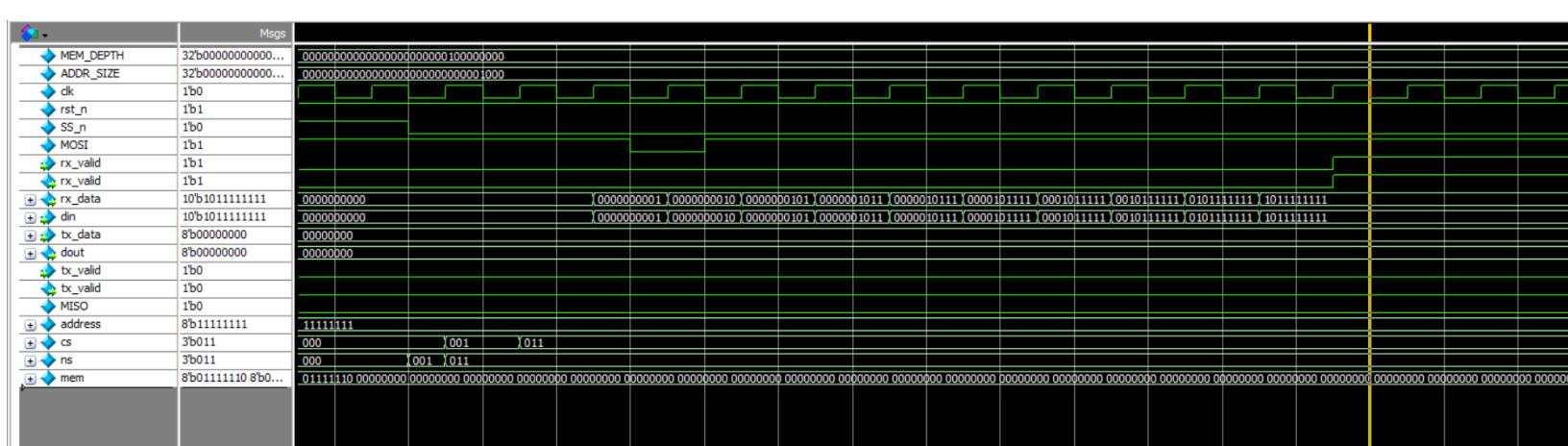
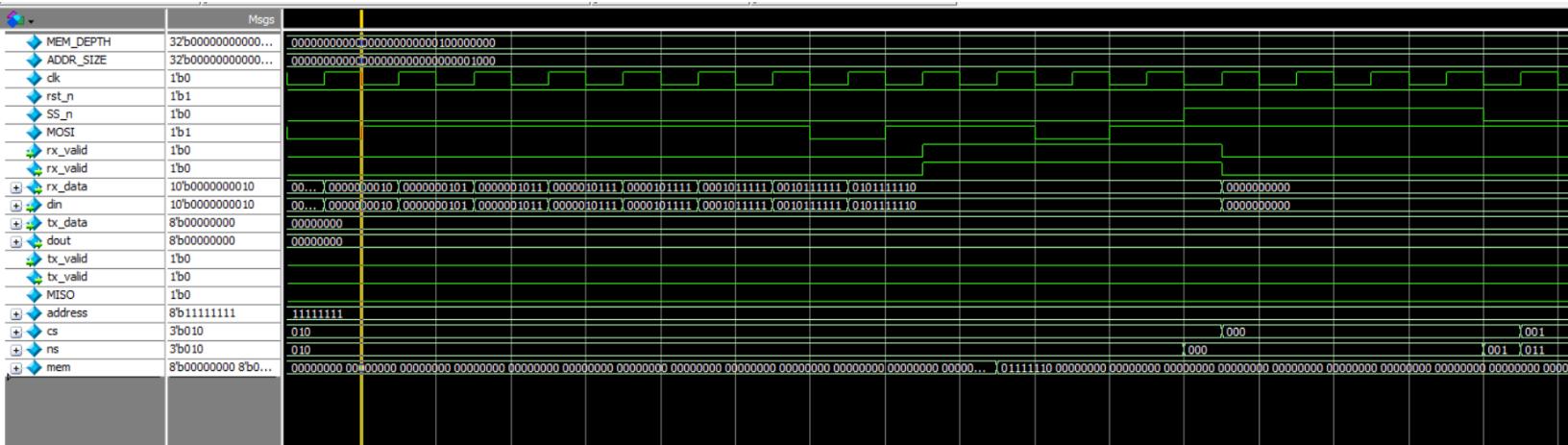
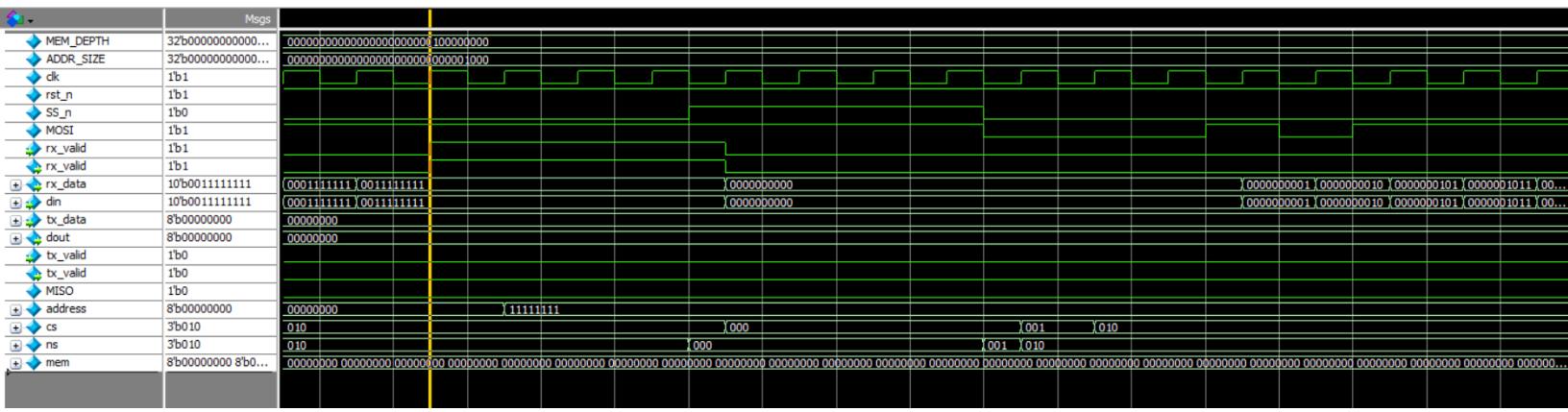
## ANUBIS Team

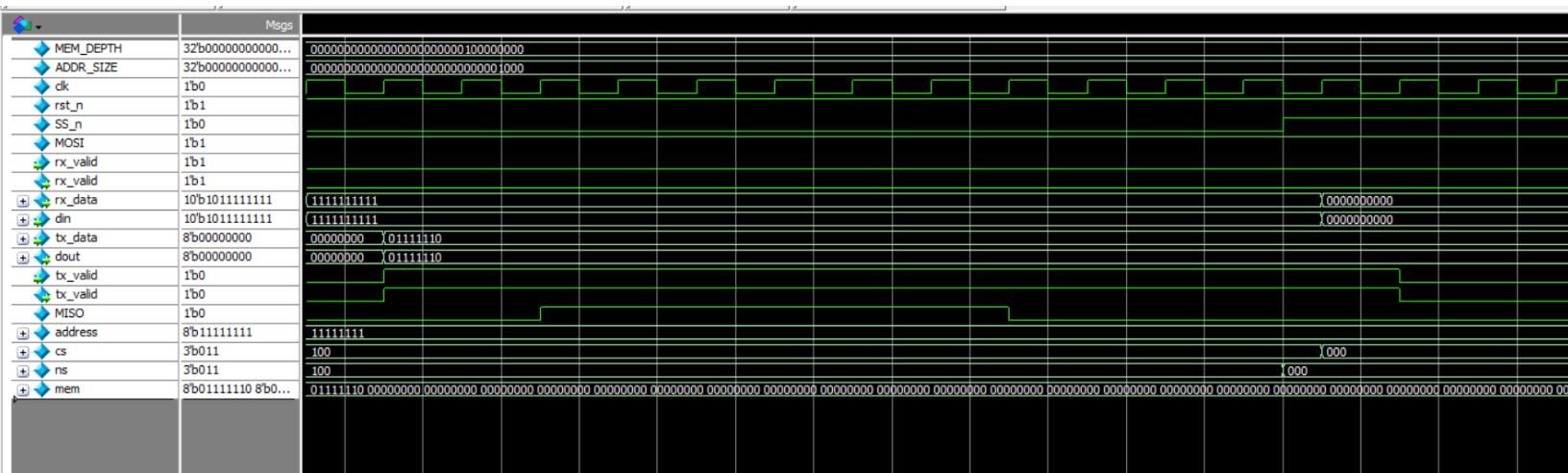
### ➤ Names:

- Youssef Ehab Mamdouh Gorgy
- Mustafa Ibrahim Mohamed Ibrahim
- Nada Mamdouh Ismail

### ➤ QuestaSim waveforms:

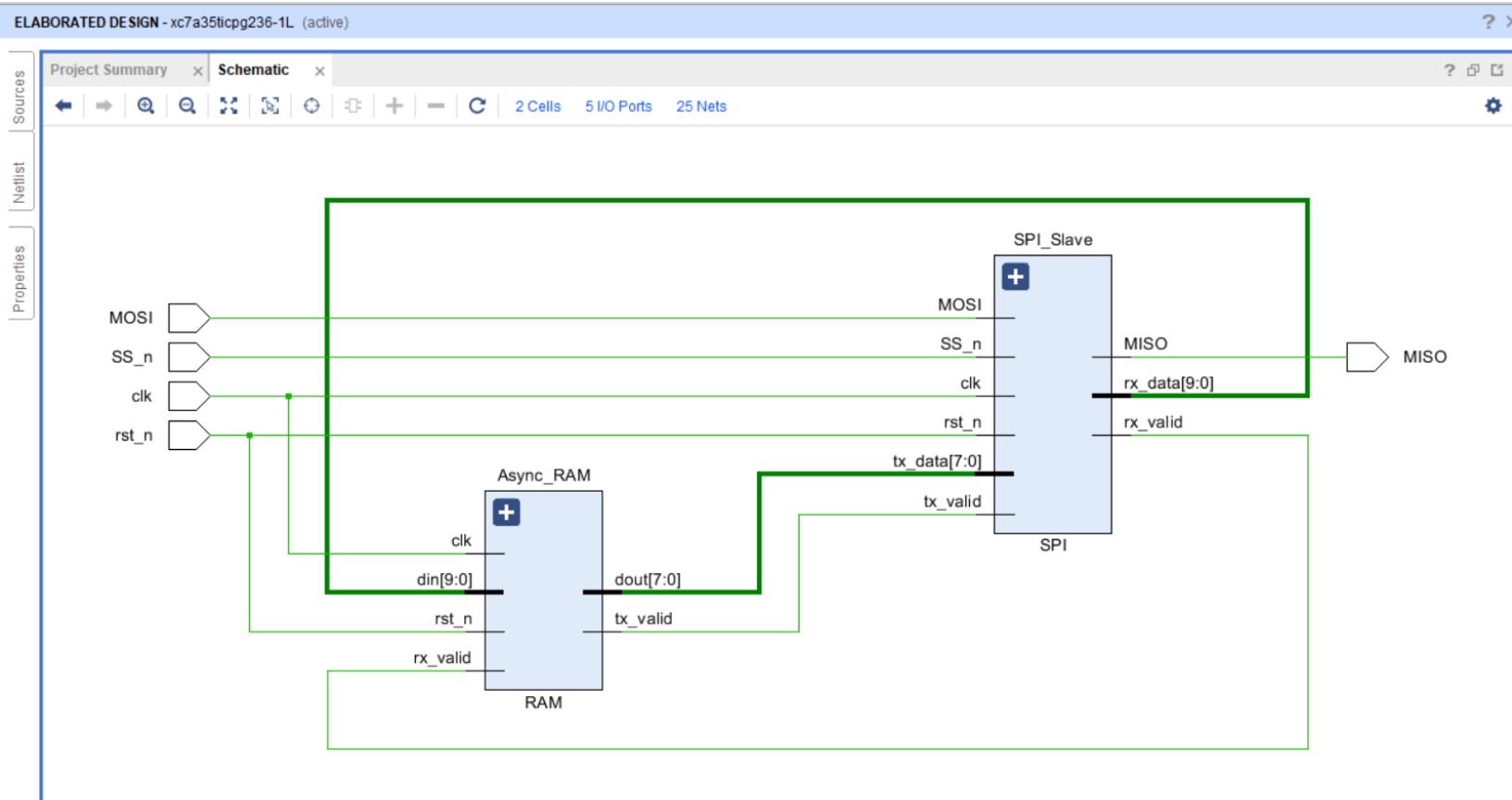




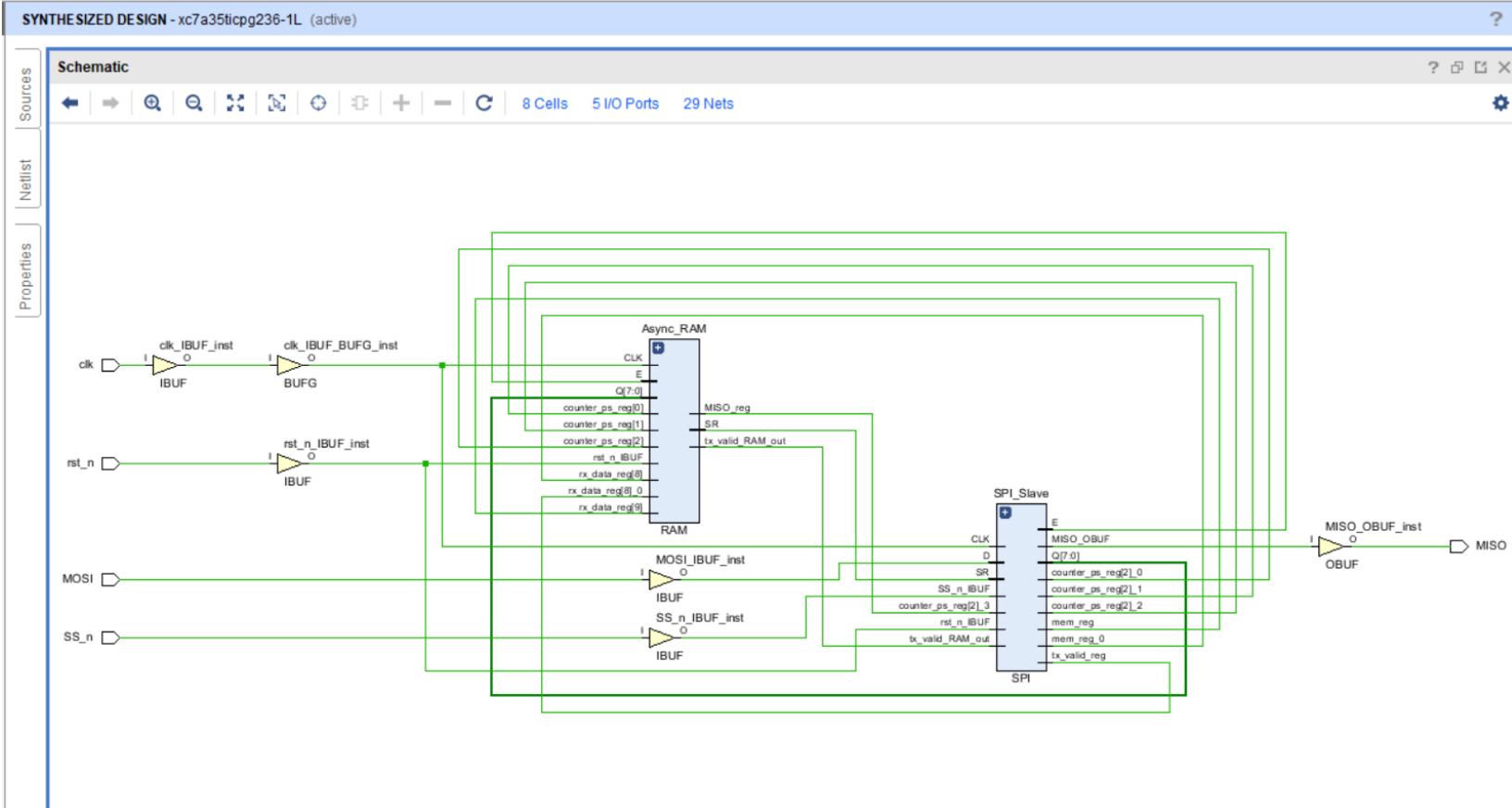


## ➤ Synthesis snippets for gray encoding:

a) Schematic after the elaboration:



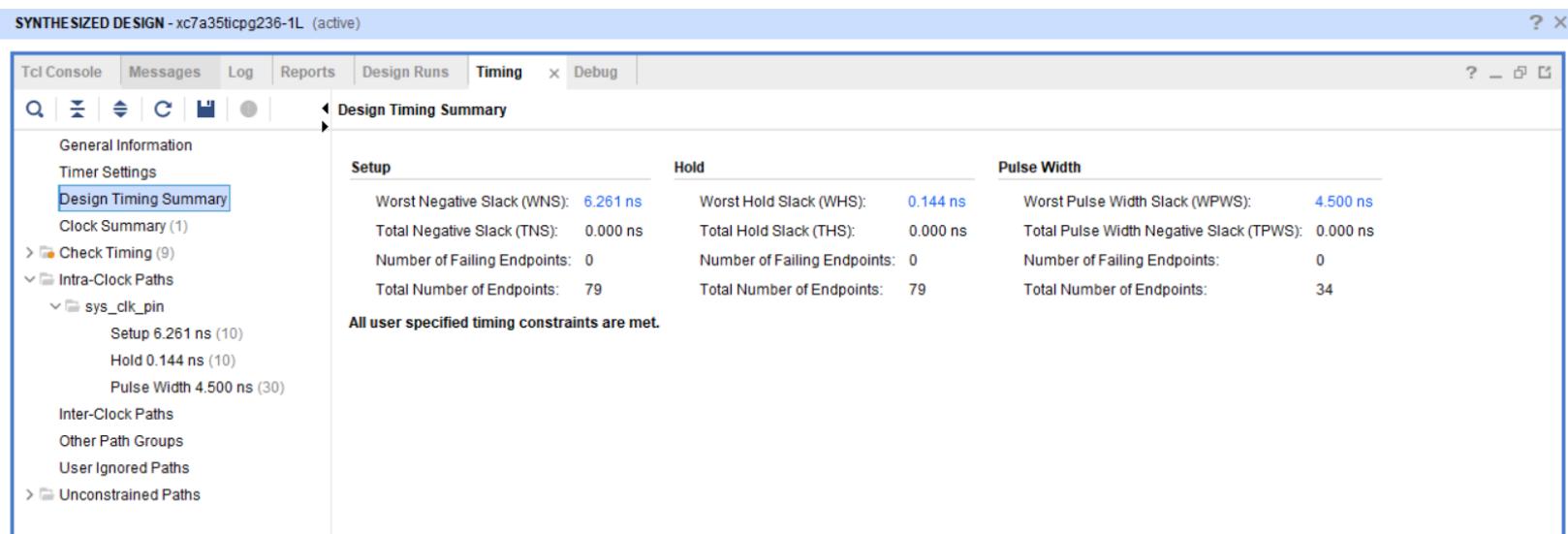
## b) Schematic after the synthesis:



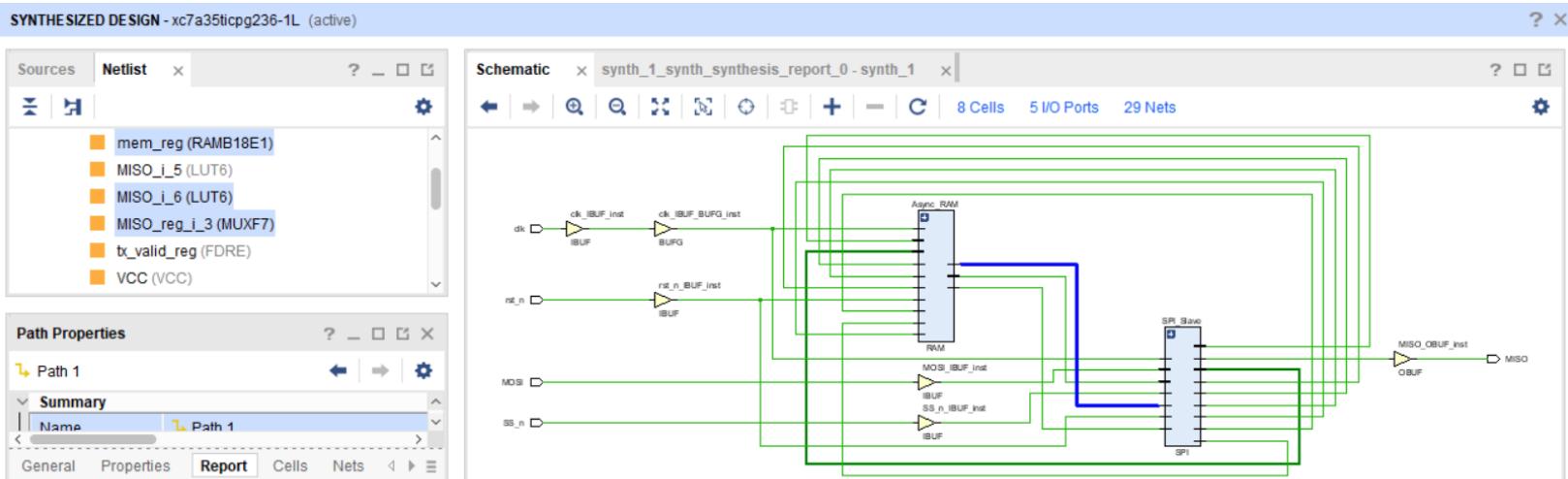
## c) Synthesis report showing the encoding used:

	State	New Encoding	Previous Encoding
96			
97			
98			
99	IDLE	000	000
100	CHK_CMD	001	001
101	READ_DATA	011	100
102	READ_ADD	010	011
103	WRITE	111	010
104			
105	INFO: [Synth 8-3354] encoded FSM with state register 'cs_reg' using encoding 'gray' in module 'SPI'		

#### d) Timing report snippet:



#### e) Snippet of the critical path highlighted in the schematic:



Tcl Console    Messages    Log    Reports    Design Runs    Timing    Debug

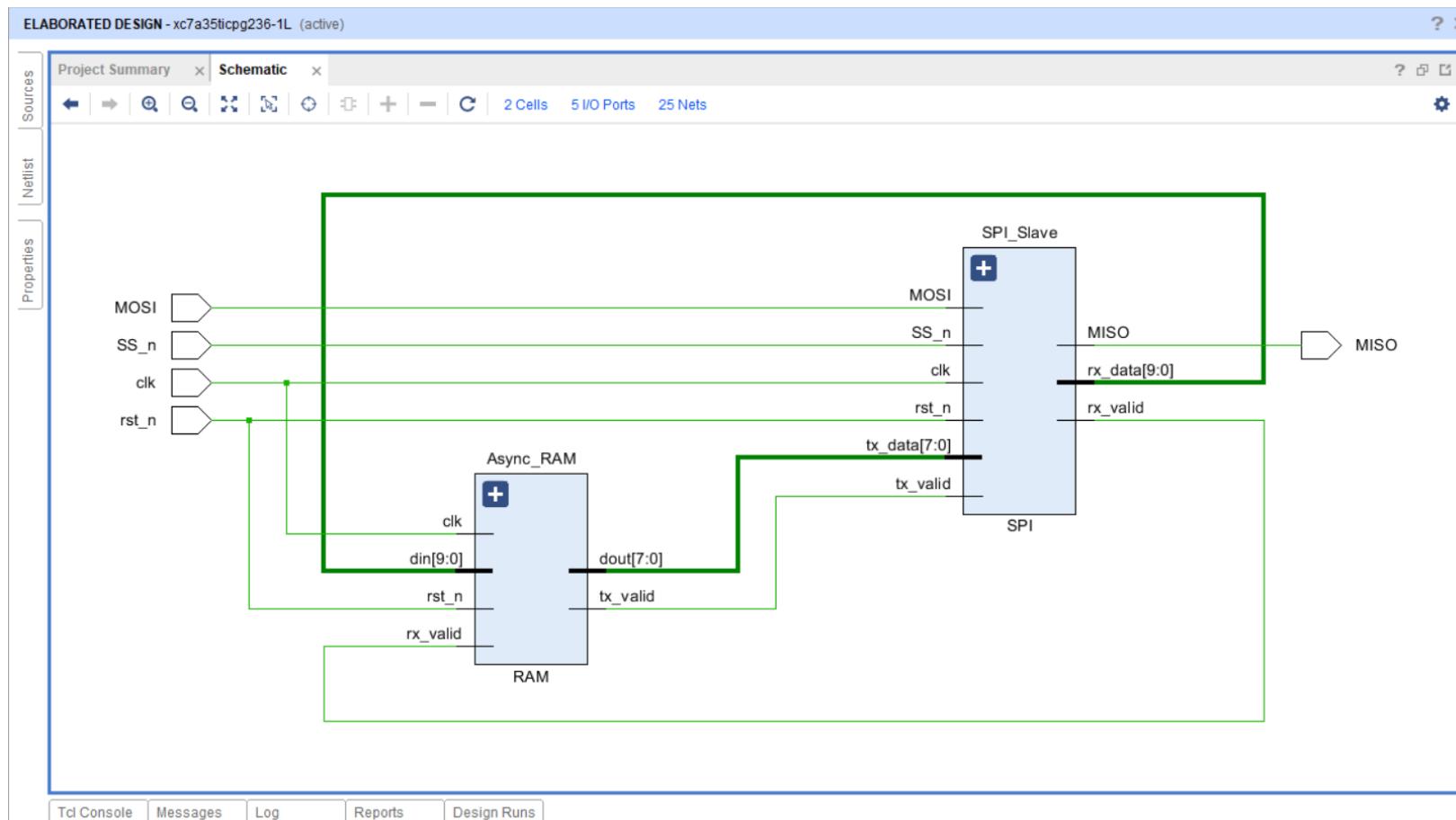
General Information    Name    Slack    Levels    High Fanout    From    To    Total Delay    Logic Delay    Net Delay    Requirement

Path 1	6.261	2	1	Asyn.../CLKBWRCLK	SPI_Slave/MISO_Reg/D	3.623	2.823	0.800	10.0
Path 2	7.019	2	4	SPI_Slave/counter_sp_Reg[3]/C	SPI_Slave/MISO_Reg/CE	2.599	0.901	1.698	10.0
Path 3	7.057	1	5	SPI_Slave/rx_data_Reg[8]/C	Asyn.../mem_Reg/ENBWREN	2.320	0.751	1.569	10.0
Path 4	7.067	1	3	SPI_Slave/rx_data_Reg[9]/C	Asyn.../mem_Reg/ENARDEN	2.310	0.751	1.559	10.0
Path 5	7.132	3	4	SPI_Slave/counter_sp_Reg[3]/C	SPI_Slave/counter_ps_Reg[1]/D	2.717	1.025	1.692	10.0
Path 6	7.132	3	4	SPI_Slave/counter_sp_Reg[3]/C	SPI_Slave/counter_ps_Reg[2]/D	2.717	1.025	1.692	10.0
Path 7	7.138	3	4	SPI_Slave/counter_sp_Reg[3]/C	SPI_Slave/counter_ps_Reg[0]/D	2.711	1.019	1.692	10.0
Path 8	7.350	1	14	SPI_Slave/counter_sp_Reg[2]/C	SPI_Slave/counter_ps_Reg[0]/CE	2.268	0.751	1.517	10.0

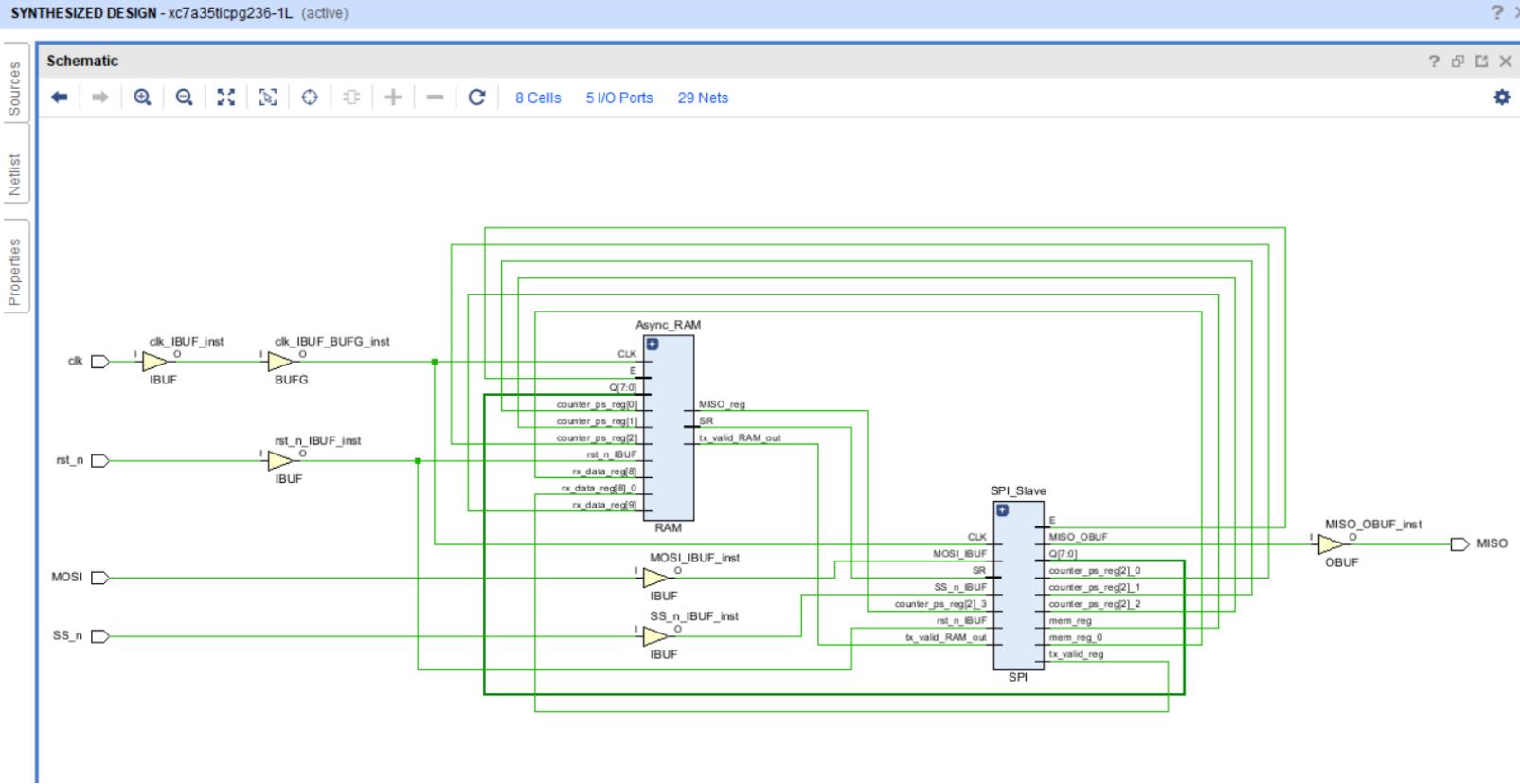
Timing Summary - timing\_1

## ➤ Synthesis snippets for one\_hot encoding:

a) Schematic after the elaboration:



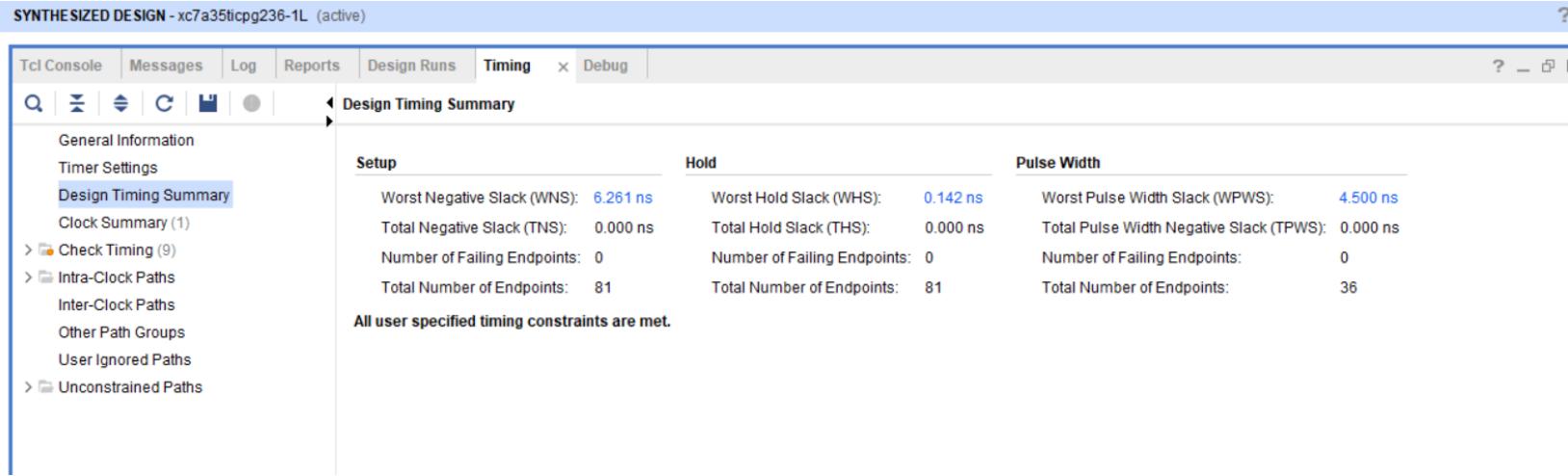
## b) Schematic after the synthesis:



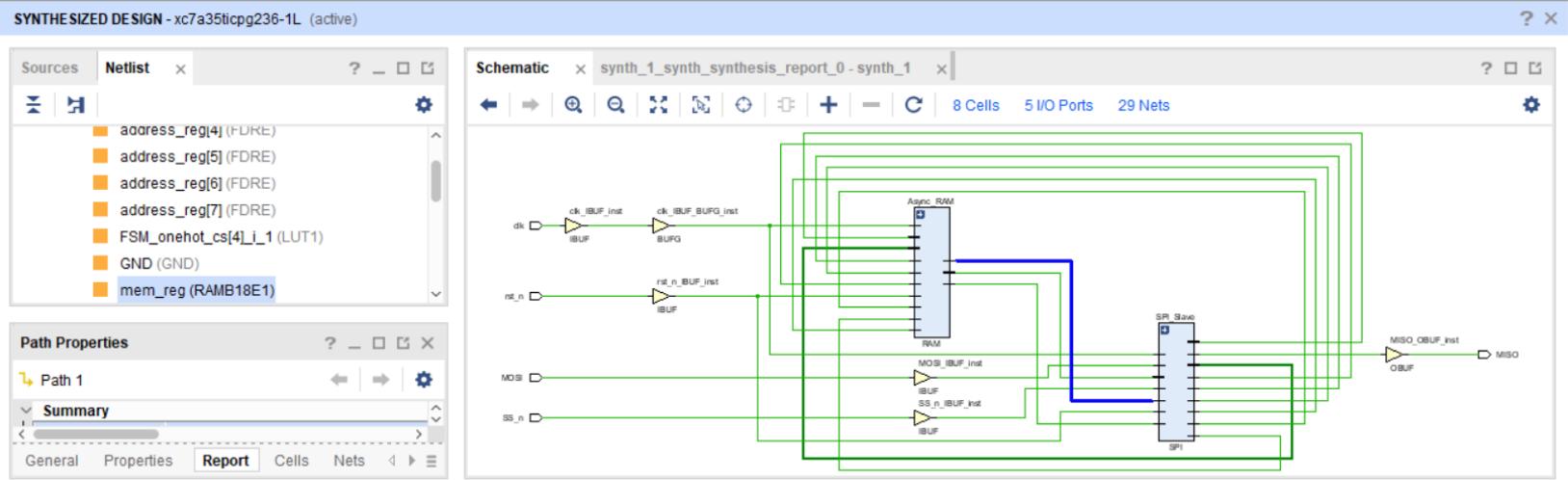
## c) Synthesis report showing the encoding used:

	State	New Encoding	Previous Encoding
96			
97			
98			
99	IDLE	00001	000
100	CHK_CMD	00010	001
101	READ_DATA	00100	100
102	READ_ADD	01000	011
103	WRITE	10000	010
104			
105	INFO: [Synth 8-3354] encoded FSM with state register 'cs_reg' using encoding 'one-hot' in module 'SPI'		

#### d) Timing report snippet:



#### e) Snippet of the critical path highlighted in the schematic:



Tcl Console    Messages    Log    Reports    Design Runs    Timing    Debug

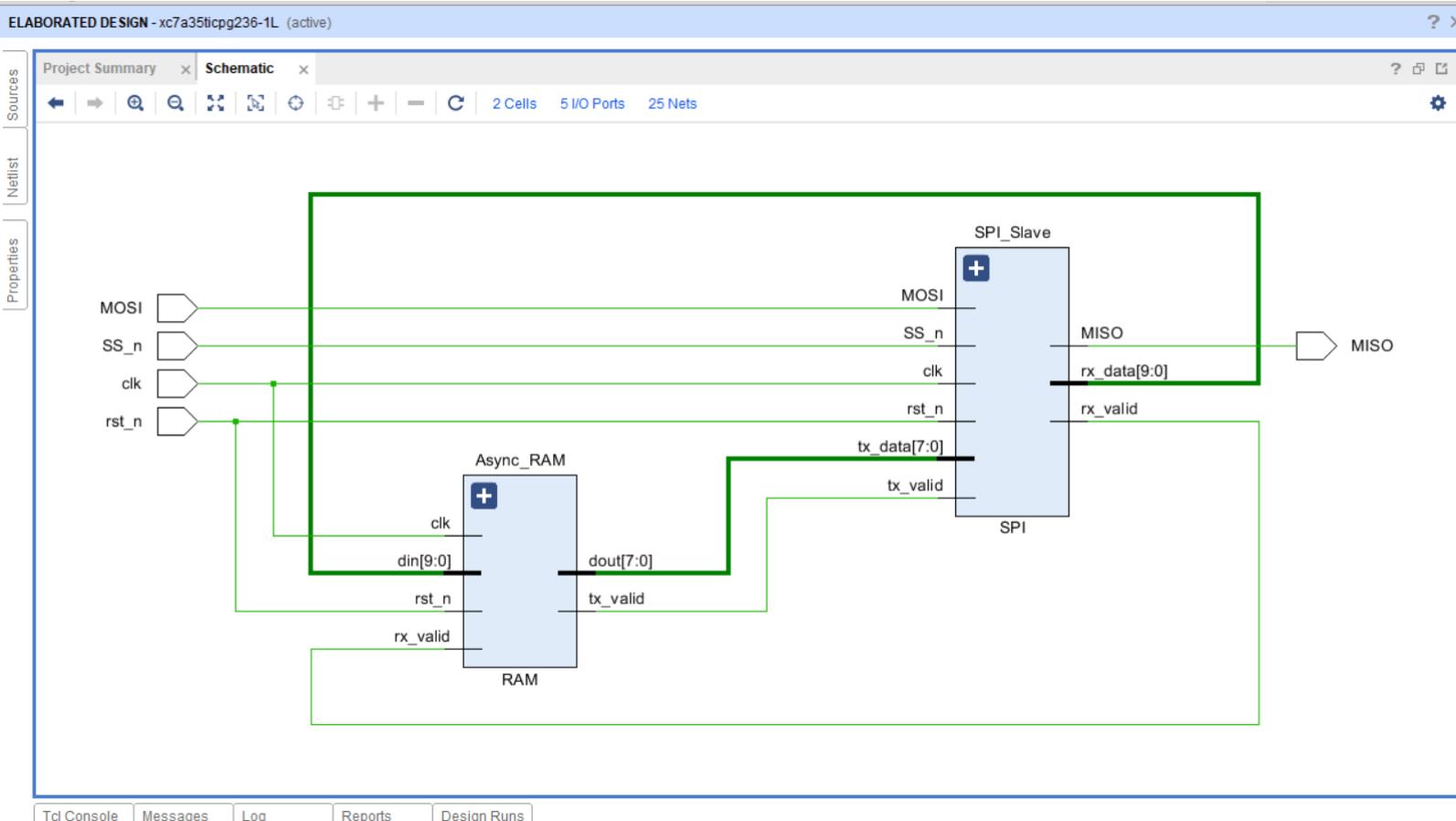
Intra-Clock Paths - sys\_clk\_pin - Setup

Name	Slack	Levels	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement
Path 1	6.261	2	1	Async_RAM/me...g/CLKBWRCLK	SPI_Slave/MISO_reg/D	3.623	2.823	0.800	10.0
Path 2	7.057	1	5	SPI_Slave/rx_data_reg[8]/C	Async_RAM/mem_reg/ENBWREN	2.320	0.751	1.569	10.0
Path 3	7.067	1	3	SPI_Slave/rx_data_reg[9]/C	Async_RAM/mem_reg/ENARDEN	2.310	0.751	1.559	10.0
Path 4	7.139	3	5	SPI_Slave/counter_sp_reg[3]/C	SPI_Slave/counter_ps_reg[1]/D	2.710	1.025	1.685	10.0
Path 5	7.139	3	5	SPI_Slave/counter_sp_reg[3]/C	SPI_Slave/counter_ps_reg[2]/D	2.710	1.025	1.685	10.0
Path 6	7.145	3	5	SPI_Slave/counter_sp_reg[3]/C	SPI_Slave/counter_ps_reg[0]/D	2.704	1.019	1.685	10.0
Path 7	7.346	1	14	SPI_Slave/counter_sp_reg[2]/C	SPI_Slave/counter_ps_reg[0]/CE	2.272	0.751	1.521	10.0

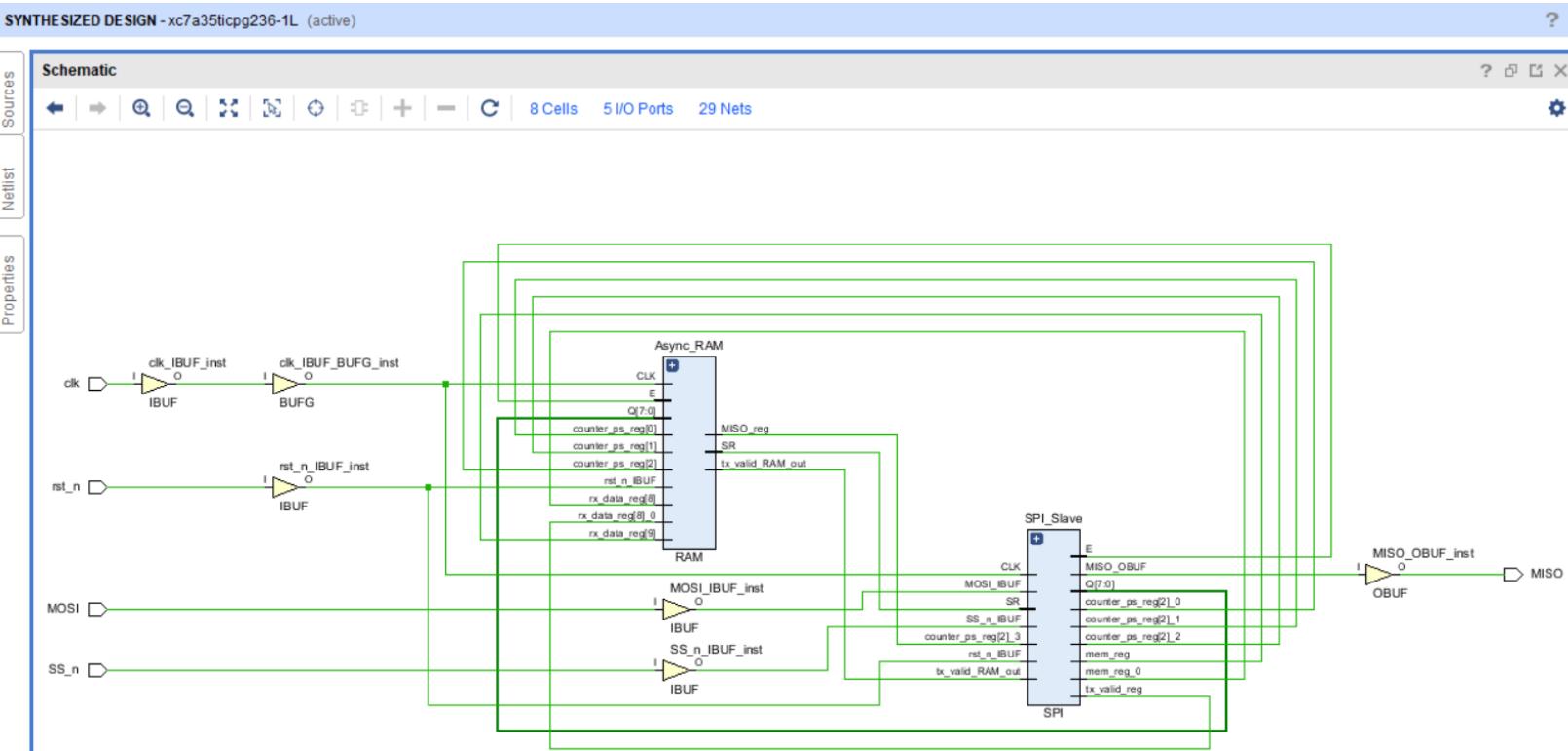
General Information  
Timer Settings  
Design Timing Summary  
Clock Summary (1)  
> Check Timing (9)  
> Intra-Clock Paths  
> sys\_clk\_pin  
Setup 6.261 ns (10)

## ► Synthesis snippets for seq encoding:

### a) Schematic after the elaboration:



### b) Schematic after the synthesis:



c) Synthesis report showing the encoding used:

	State	New Encoding	Previous Encoding
96	IDLE	000	000
97	CHK_CMD	001	001
98	READ_DATA	010	100
99	READ_ADD	011	011
100	WRITE	100	010
101			
102			
103			
104			
105	NFO: [Synth 8-3354] encoded FSM with state register 'cs_reg' using encoding 'sequential' in module 'SPI'		

d) Timing report snippet:

SYNTHESIZED DESIGN - xc7a35ticpg236-1L (active)

Tcl Console Messages Log Reports Design Runs **Timing** x Debug

Design Timing Summary

General Information

Timer Settings

Design Timing Summary

Clock Summary (1)

> Check Timing (9)

> Intra-Clock Paths

Inter-Clock Paths

Other Path Groups

User Ignored Paths

> Unconstrained Paths

Setup	Hold	Pulse Width
Worst Negative Slack (WNS): 6.261 ns	Worst Hold Slack (WHS): 0.144 ns	Worst Pulse Width Slack (WPWS): 4.500 ns
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
Total Number of Endpoints: 79	Total Number of Endpoints: 79	Total Number of Endpoints: 34

All user specified timing constraints are met.

e) Snippet of the critical path highlighted in the schematic:

SYNTHESIZED DESIGN - xc7a35ticpg236-1L (active)

Sources Netlist x ? □ □

address\_reg[4] (FDRE)  
address\_reg[5] (FDRE)  
address\_reg[6] (FDRE)  
address\_reg[7] (FDRE)  
FSM\_sequential\_cs[2]\_i\_1 (LUT1)  
GND (GND)  
mem\_reg (RAMB18E1)

Path Properties ? \_ □ □ x

Path 1

Summary

General Properties Report Cells Nets

Schematic x synth\_1\_synth\_synthesis\_report\_0 - synth\_1 x

8 Cells 5 I/O Ports 29 Nets

Tcl Console Messages Log Reports Design Runs **Timing** x Debug

Design Timing Summary

Intra-Clock Paths - sys\_clk\_pin - Setup

Name	Slack	Levels	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement
Path 1	6.261	2	1	Async_RAM/me...g/CLKBWRCLK	SPI_Slave/MISO_reg/D	3.623	2.823	0.800	10.0
Path 2	7.019	2	4	SPI_Slave/counter_sp_reg[3]/C	SPI_Slave/MISO_reg/CE	2.599	0.901	1.698	10.0
Path 3	7.057	1	5	SPI_Slave/rx_data_reg[8]/C	Async_RAM/mem_reg/ENBWREN	2.320	0.751	1.569	10.0
Path 4	7.067	1	3	SPI_Slave/rx_data_reg[9]/C	Async_RAM/mem_reg/ENARDEN	2.310	0.751	1.559	10.0
Path 5	7.132	3	4	SPI_Slave/counter_sp_reg[3]/C	SPI_Slave/counter_ps_reg[1]/D	2.717	1.025	1.692	10.0
Path 6	7.132	3	4	SPI_Slave/counter_sp_reg[3]/C	SPI_Slave/counter_ps_reg[2]/D	2.717	1.025	1.692	10.0
Path 7	7.138	3	4	SPI_Slave/counter_sp_reg[3]/C	SPI_Slave/counter_ps_reg[0]/D	2.711	1.019	1.692	10.0
Path 8	7.350	1	14	SPI_Slave/counter_sp_reg[2]/C	SPI_Slave/counter_sp_reg[0]/CE	2.268	0.751	1.517	10.0

## ➤ Implementation snippets for gray encoding:

### a) Utilization report:

**IMPLEMENTED DESIGN - xc7a35ticpg236-1L (active)**

Tcl Console | Messages | Log | Reports | Design Runs | Timing | Utilization | ? - □

Hierarchy

Name	Slice LUTs (20800)	Slice Registers (41600)	F7 Muxes (16300)	Slice (8150)	LUT as Logic (20800)	LUT Flip Flop Pairs (20800)	Block RAM Tile (50)	Bonded IOB (106)	BUFGCTRL (32)
N SPI_Wrapper	24	32	1	13	24	10	0.5	5	1
Async_RAM (RAM)	4	9	1	4	4	0	0.5	0	0
SPI_Slave (SPI)	20	23	0	12	20	9	0	0	0

**IMPLEMENTED DESIGN - xc7a35ticpg236-1L (active)**

Tcl Console | Messages | Log | Reports | Design Runs | Timing | Utilization | ? - □

Summary

Resource	Utilization	Available	Utilization %
LUT	24	20800	0.12
FF	32	41600	0.08
BRAM	0.50	50	1.00
IO	5	106	4.72

Utilization (%)

### b) Timing report snippet:

**IMPLEMENTED DESIGN - xc7a35ticpg236-1L (active)**

Tcl Console | Messages | Log | Reports | Design Runs | Timing | Utilization | ? - □

Design Timing Summary

General Information

Timer Settings

Design Timing Summary

Clock Summary (1)

> Check Timing (9)

> Intra-Clock Paths

Inter-Clock Paths

Other Path Groups

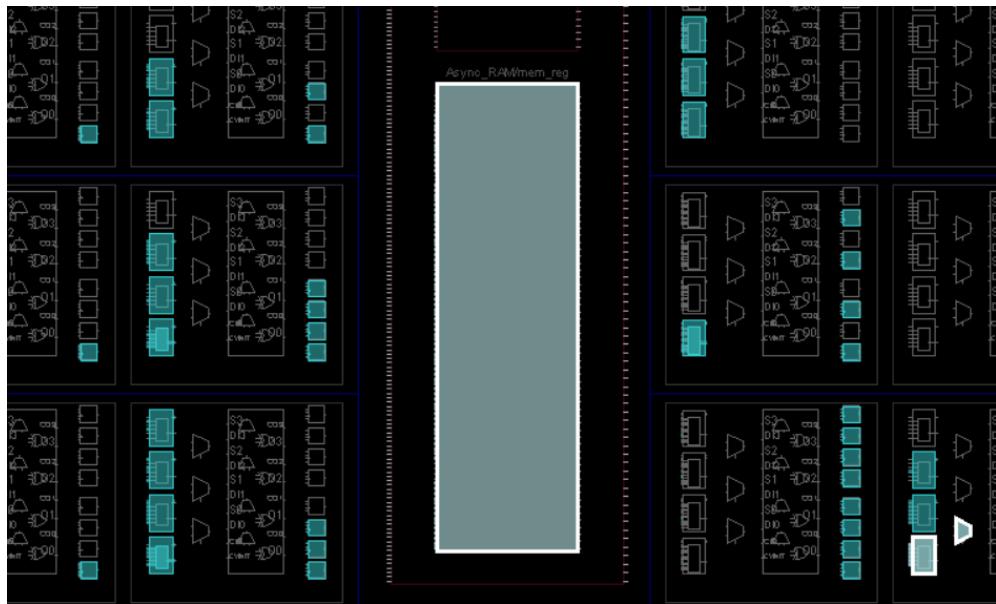
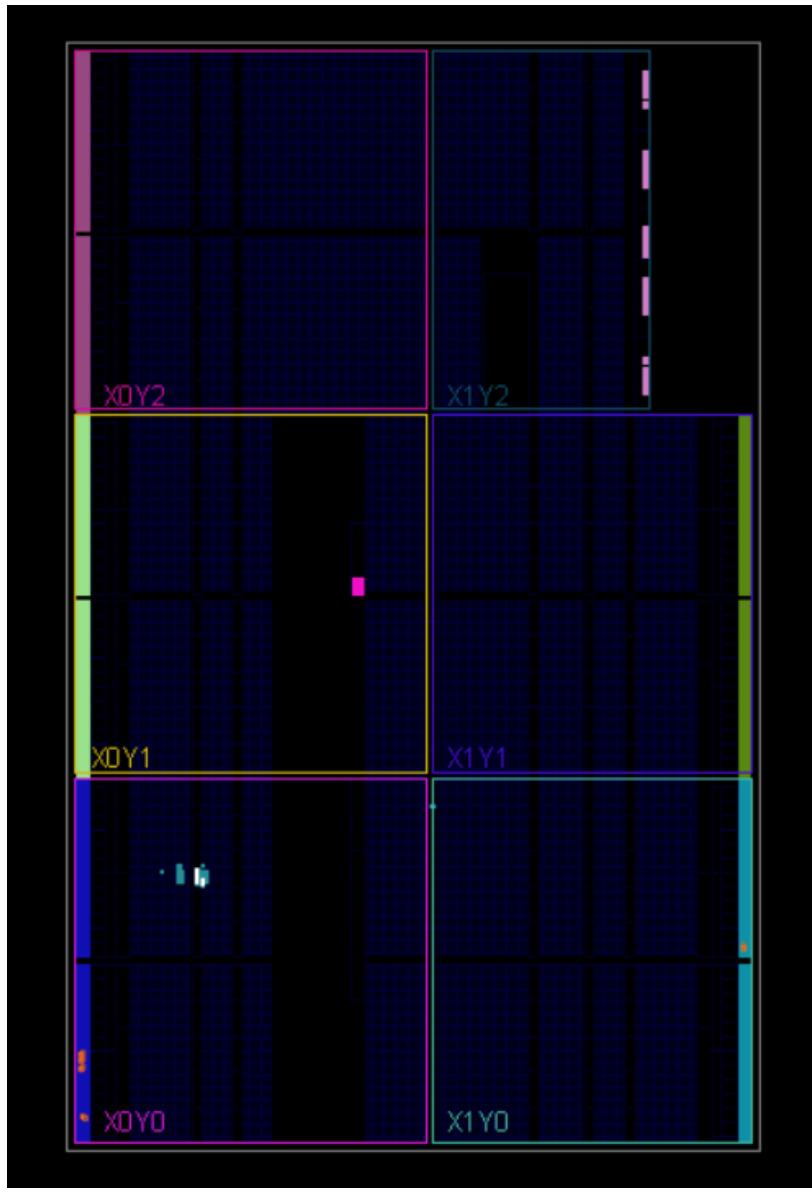
User Ignored Paths

> Unconstrained Paths

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	5.961 ns	Worst Hold Slack (WHS):	0.042 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWNS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	79	Total Number of Endpoints:	79	Total Number of Endpoints:	34

All user specified timing constraints are met.

c) FPGA device snippet:



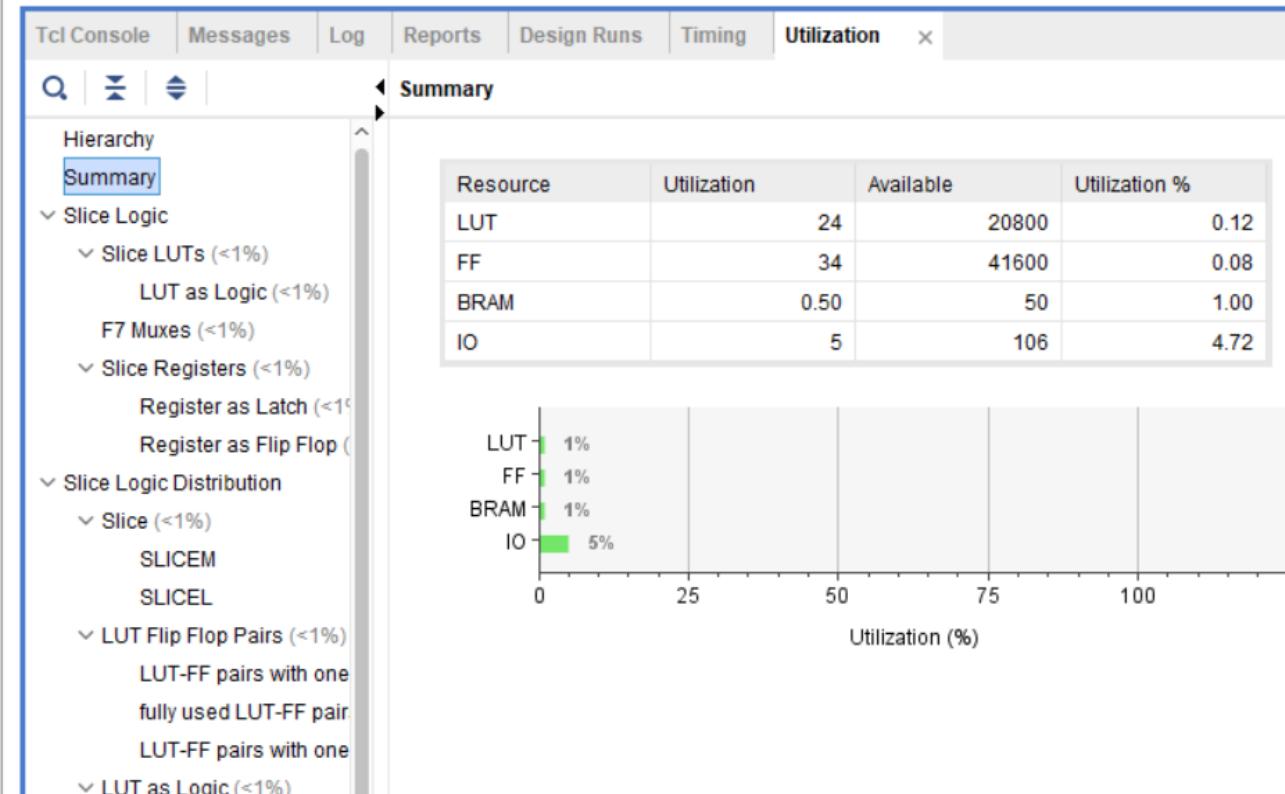
## ➤ Implementation snippets for one\_hot encoding:

### a) Utilization report:

IMPLEMENTED DESIGN - xc7a35ticpg236-1L (active)

Utilization											
	Name	1	Slice LUTs (20800)	Slice Registers (41600)	F7 Muxes (16300)	Slice (8150)	LUT as Logic (20800)	LUT Flip Flop Pairs (20800)	Block RAM Tile (50)	Bonded IOB (106)	BUFGCTRL (32)
<b>Hierarchy</b>											
Summary											
Slice Logic											
Slice LUTs (<1%)											
LUT as Logic (<1%)											
F7 Muxes (<1%)											
Slice Registers (<1%)											
Register as Latch (<1%)											
Register as Flip Flop (											
Slice Logic Distribution											
Slice (<1%)											
SLICEM											

IMPLEMENTED DESIGN - xc7a35ticpg236-1L (active)



## b) Timing report snippet:

IMPLEMENTED DESIGN - xc7a35ticpg236-1L (active)

Tcl Console | Messages | Log | Reports | Design Runs | **Timing** | Utilization | ? - □

Design Timing Summary

General Information

Timer Settings

**Design Timing Summary**

Clock Summary (1)

> Check Timing (9)

✓ Intra-Clock Paths

  sys\_clk\_pin

    Setup 5.890 ns (10)  
    Hold 0.048 ns (10)  
    Pulse Width 4.500 ns (30)

Inter-Clock Paths

Other Path Groups

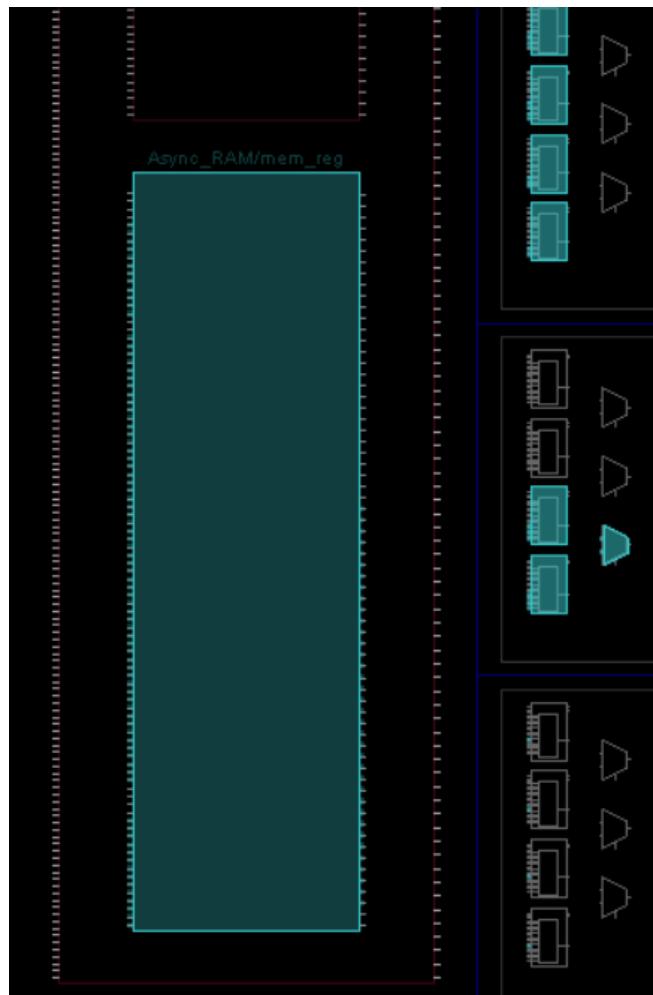
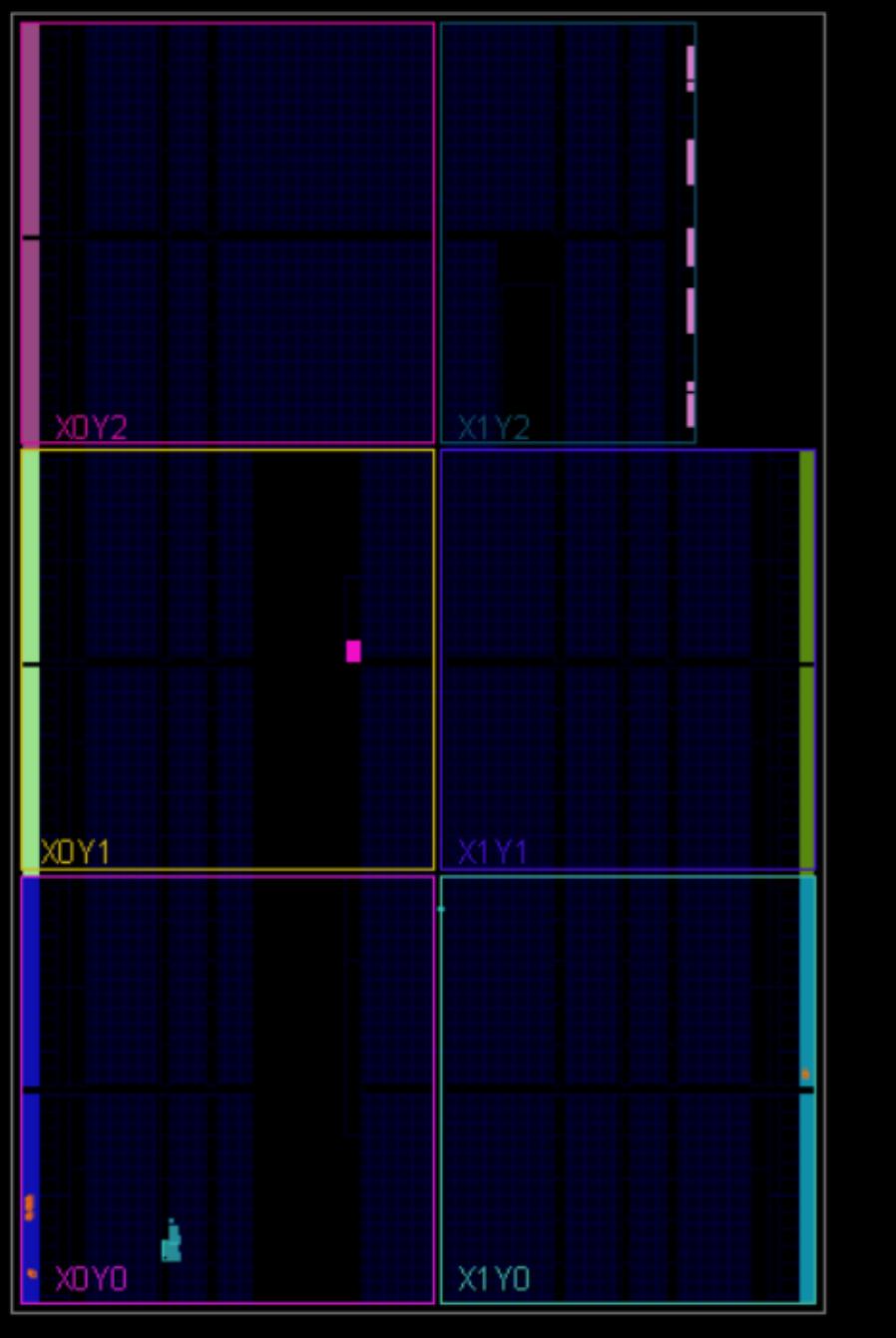
User Ignored Paths

> Unconstrained Paths

Setup	Hold	Pulse Width
Worst Negative Slack (WNS): <b>5.890 ns</b>	Worst Hold Slack (WHS): <b>0.048 ns</b>	Worst Pulse Width Slack (WPWS): <b>4.500 ns</b>
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
Total Number of Endpoints: 81	Total Number of Endpoints: 81	Total Number of Endpoints: 36

All user specified timing constraints are met.

c) FPGA device snippet:



## ➤ Implementation snippets for seq encoding:

### a) Utilization report:

IMPLEMENTED DESIGN - xc7a35ticpg236-1L (active)

Name	Slice LUTs (20800)	Slice Registers (41600)	F7 Muxes (16300)	Slice (815 0)	LUT as Logic (20800)	LUT Flip Flop Pairs (20800)	Block RAM Tile (50)	Bonded IOB (106)	BUFGCTRL (32)	
N SPI_Wrapper	23	32	1	12	23		11	0.5	5	1
Async_RAM (RAM)	4	9	1	4	4		0	0.5	0	0
SPI_Slave (SPI)	19	23	0	11	19		10	0	0	0

IMPLEMENTED DESIGN - xc7a35ticpg236-1L (active)

Resource	Utilization	Available	Utilization %
LUT	23	20800	0.11
FF	32	41600	0.08
BRAM	0.50	50	1.00
IO	5	106	4.72

The chart displays the utilization percentage for four resource types: LUT, FF, BRAM, and IO. The x-axis represents the utilization percentage from 0 to 100. The bars show that LUT, FF, and BRAM each account for 1% utilization, while IO accounts for 5% utilization.

## b) Timing report snippet:

IMPLEMENTED DESIGN - xc7a35ticpg236-1L (active)

Tcl Console | Messages | Log | Reports | Design Runs | **Timing** | Utilization | ?

Design Timing Summary

General Information

Timer Settings

**Design Timing Summary**

Clock Summary (1)

> Check Timing (9)

Intra-Clock Paths

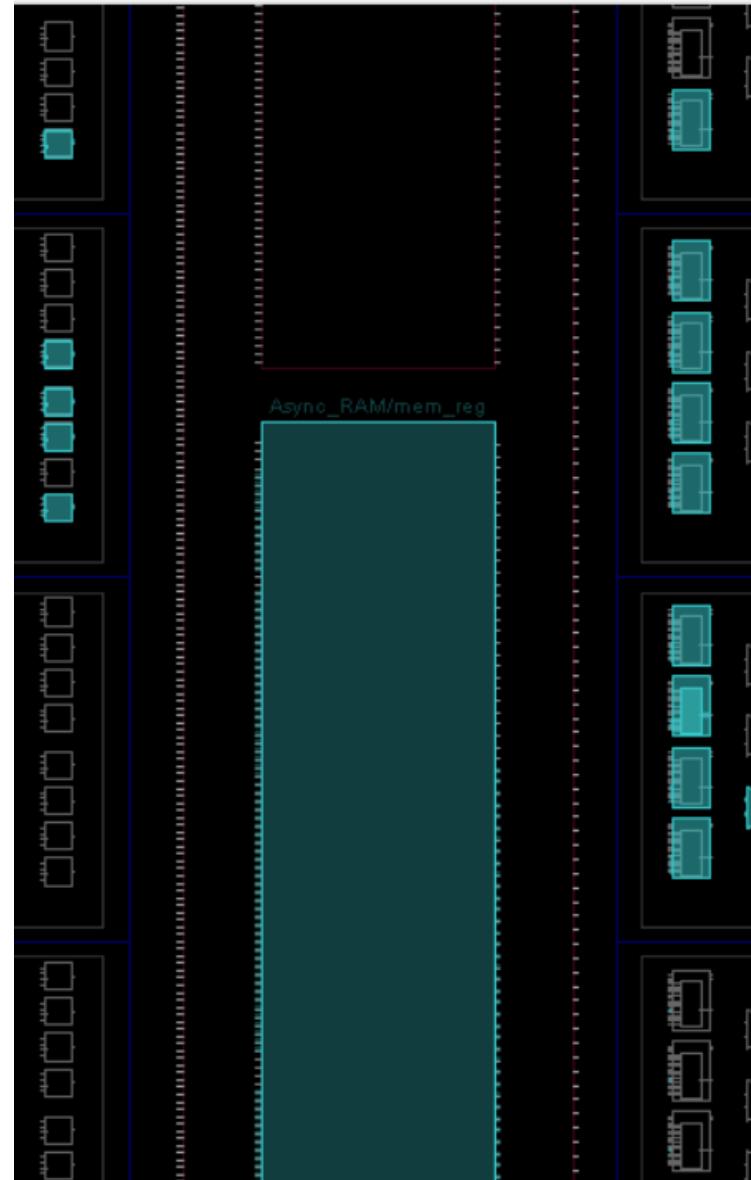
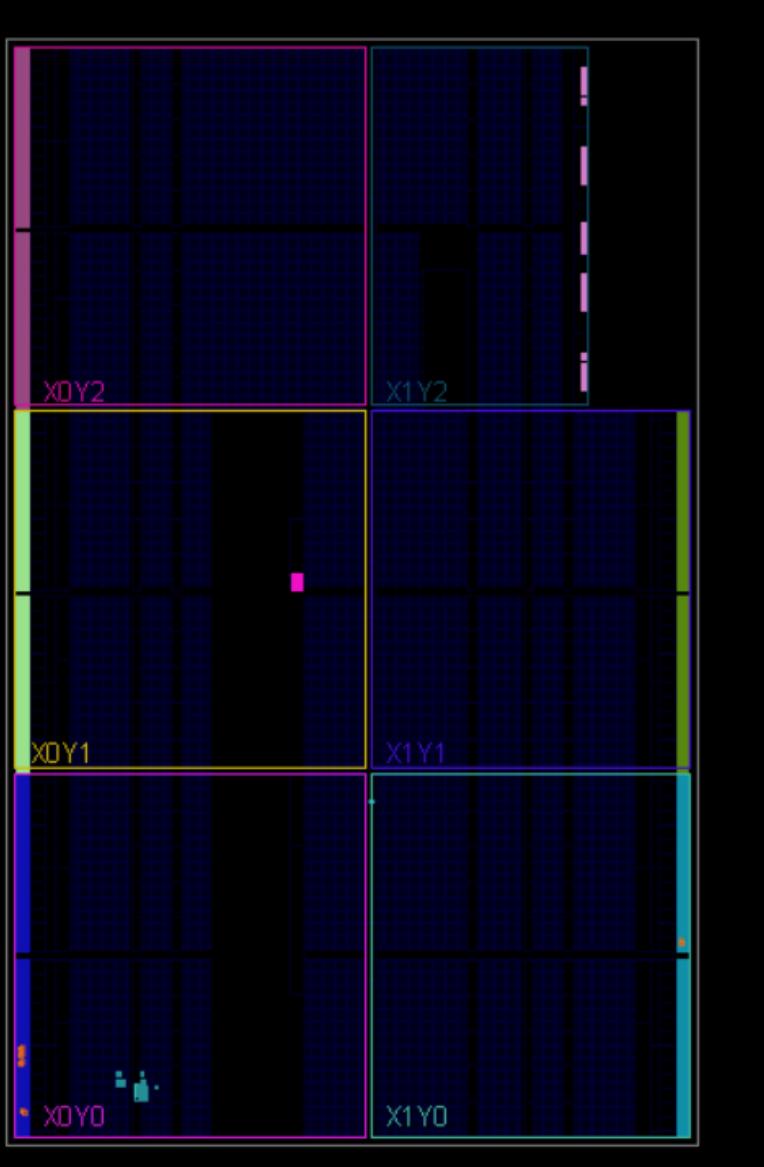
sys\_clk\_pin

- Setup 6.023 ns (10)
- Hold 0.048 ns (10)

All user specified timing constraints are met.

Setup	Hold	Pulse Width
Worst Negative Slack (WNS): 6.023 ns	Worst Hold Slack (WHS): 0.048 ns	Worst Pulse Width Slack (WPWS): 4.500 ns
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
Total Number of Endpoints: 79	Total Number of Endpoints: 79	Total Number of Endpoints: 34

## c) FPGA device snippet:



## ➤ Snippet of the “Messages” tab:

### a) gray encoding:

Window Layout View Help Quick Access

HARDWARE MANAGER - unconnected

No hardware target is open. Open target

Tcl Console Messages x Serial I/O Links Serial I/O Scans

?

Warning (4) Info (280) Status (540) Show All

Synthesis (2 warnings)

- [Synth 8-327] inferring latch for variable 'address\_recieved\_reg' [SPIv.45]
- [Constraints 18-5210] No constraint will be written out.

Implementation (1 warning)

- Write Bitstream (1 warning)
  - DRC (1 warning)
    - Physical Configuration (1 warning)
      - Chip Level (1 warning)
        - [DRC PDRC-153] Gated clock check: Net SPI\_Slave/address\_recieved\_reg\_i\_2\_n\_0 is a gated clock net sourced by a combinational pin SPI\_Slave/address\_recieved\_reg\_i\_2/I/O, cell SPI\_Slave/address\_recieved\_reg\_i\_2. This is not good design practice and will likely impact performance. For SLICE registers, for example, use the CE pin to control the loading of data.

### b) one\_hot encoding:

Window Layout View Help Quick Access

HARDWARE MANAGER - unconnected

No hardware target is open. Open target

Tcl Console Messages x Serial I/O Links Serial I/O Scans

?

Warning (4) Info (282) Status (546) Show All

Synthesis (2 warnings)

- [Synth 8-327] inferring latch for variable 'address\_recieved\_reg' [SPIv.45]
- [Constraints 18-5210] No constraint will be written out.

Implementation (1 warning)

- Write Bitstream (1 warning)
  - DRC (1 warning)
    - Physical Configuration (1 warning)
      - Chip Level (1 warning)
        - [DRC PDRC-153] Gated clock check: Net SPI\_Slave/address\_recieved\_reg\_i\_2\_n\_0 is a gated clock net sourced by a combinational pin SPI\_Slave/address\_recieved\_reg\_i\_2/I/O, cell SPI\_Slave/address\_recieved\_reg\_i\_2. This is not good design practice and will likely impact performance. For SLICE registers, for example, use the CE pin to control the loading of data.

### c) seq encoding:

Window Layout View Help Quick Access

HARDWARE MANAGER - unconnected

No hardware target is open. Open target

Tcl Console Messages x Serial I/O Links Serial I/O Scans

?

Warning (4) Info (282) Status (546) Show All

Synthesis (2 warnings)

- [Synth 8-327] inferring latch for variable 'address\_recieved\_reg' [SPIv.45]
- [Constraints 18-5210] No constraint will be written out.

Implementation (1 warning)

- Write Bitstream (1 warning)
  - DRC (1 warning)
    - Physical Configuration (1 warning)
      - Chip Level (1 warning)
        - [DRC PDRC-153] Gated clock check: Net SPI\_Slave/address\_recieved\_reg\_i\_2\_n\_0 is a gated clock net sourced by a combinational pin SPI\_Slave/address\_recieved\_reg\_i\_2/I/O, cell SPI\_Slave/address\_recieved\_reg\_i\_2. This is not good design practice and will likely impact performance. For SLICE registers, for example, use the CE pin to control the loading of data.

- Since sequential encoding has high setup slack after implementation (which is = 6.023ns). Therefore sequential encoding is the best.
- After adding debug core:

Set Up Debug

**Nets to Debug**

The nets below will be debugged with ILA cores. To add nets click "Find Nets to Add". You can also select nets in the Netlist or other windows, then drag them to the list or click "Add Selected Nets".

Name	Clock Domain	Driver Cell	Probe Type
clk_IBUF	clk_IBUF_BUFG	IBUF	Trigger
MISO_OBUF	clk_IBUF_BUFG	FDRE	Data
MOSI_IBUF	clk_IBUF_BUFG	IBUF	Data
rst_n_IBUF	clk_IBUF_BUFG	IBUF	Data
SS_n_IBUF	clk_IBUF_BUFG	IBUF	Data

Find Nets to Add...

Nets to debug: 5

?

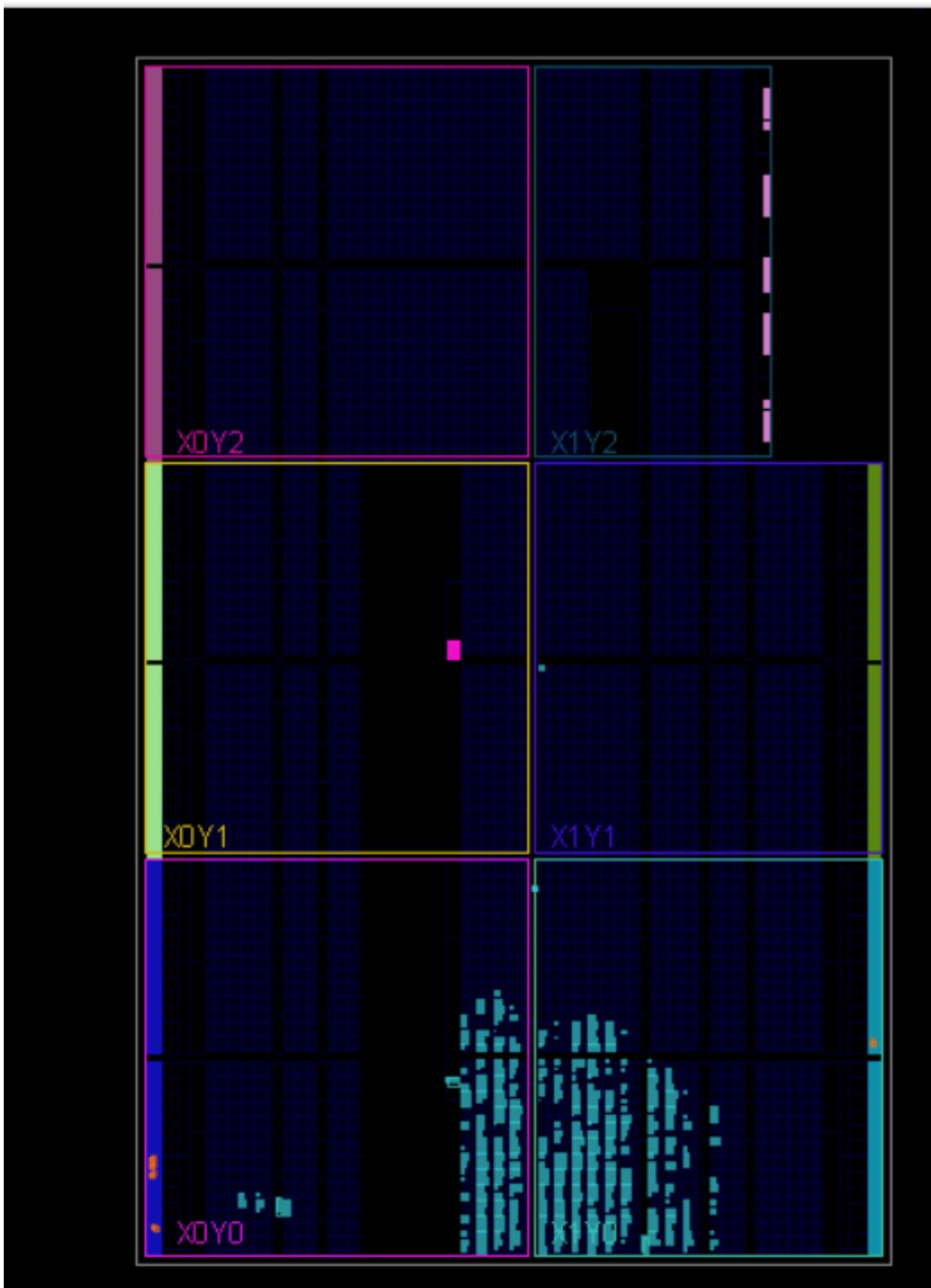
< Back

Next >

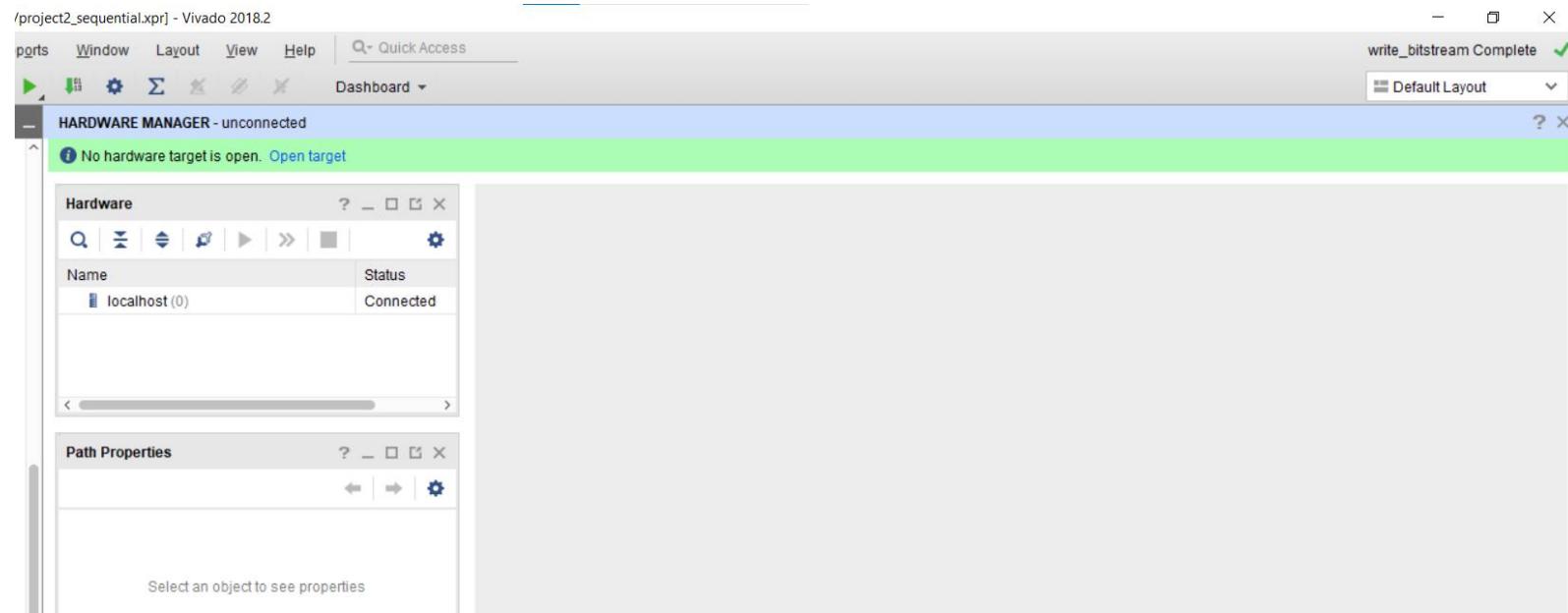
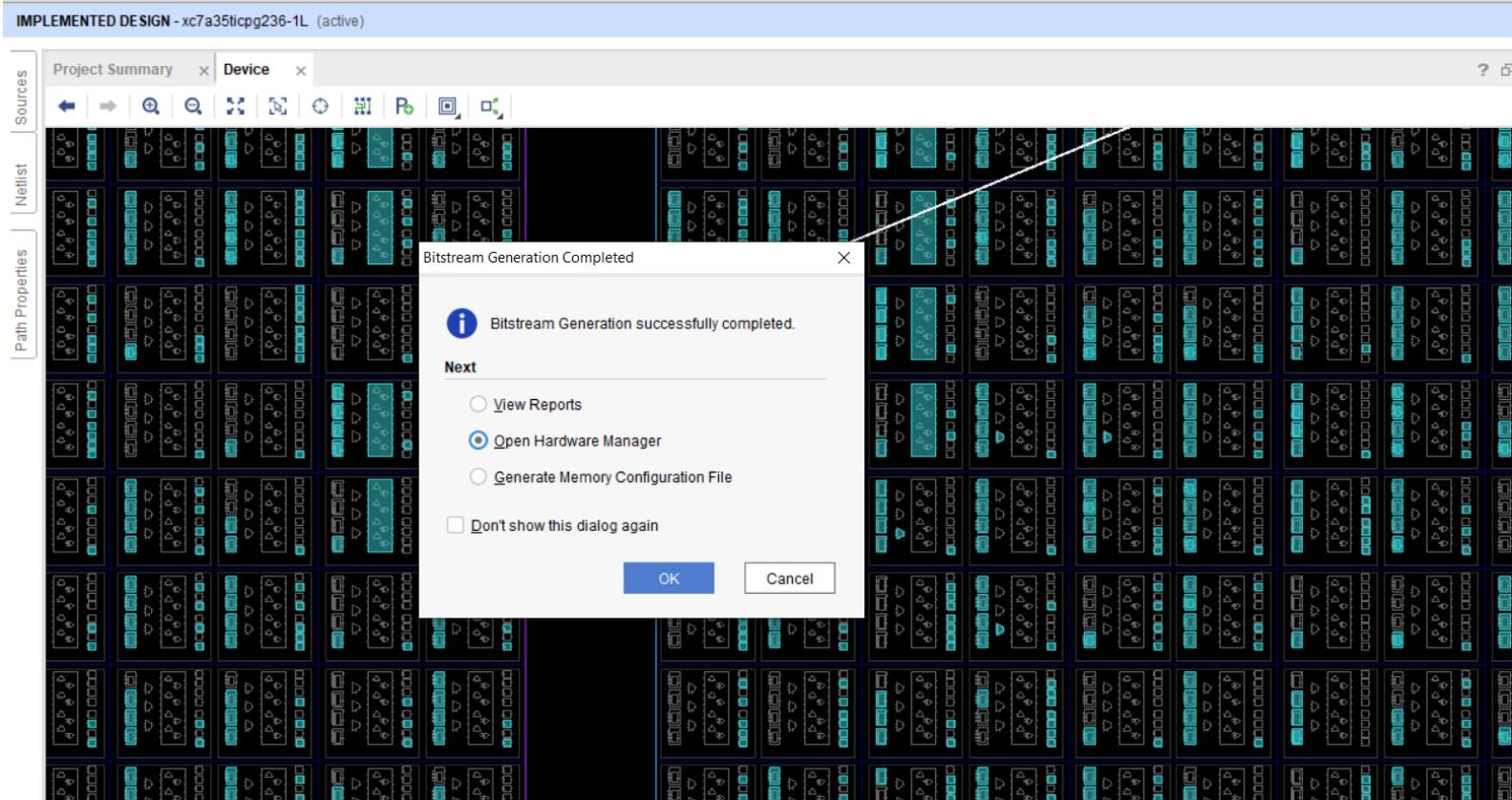
Finish

Cancel

a) Implementation:



## b) Successful bitstream:



➤ Note: sync rst is used because async rst is not supported with RAM

```
parameter ADDR_SIZE bound to: 0 - type: integer
WARNING: [Synth 8-5788] Register address_reg in module RAM is has both Set and reset with same priority. This may cause simulation mismatches. Consider rewriting code [C:/Pro
WARNING: [Synth 8-5788] Register mem_reg in module RAM is has both Set and reset with same priority. This may cause simulation mismatches. Consider rewriting code
WARNING: [Synth 8-4767] Trying to implement RAM 'mem_reg' in registers. Block RAM or DRAM implementation is not possible; see log for reasons.
Reason is one or more of the following :
 1: RAM is sensitive to asynchronous reset signal. this RTL style is not supported.
```