

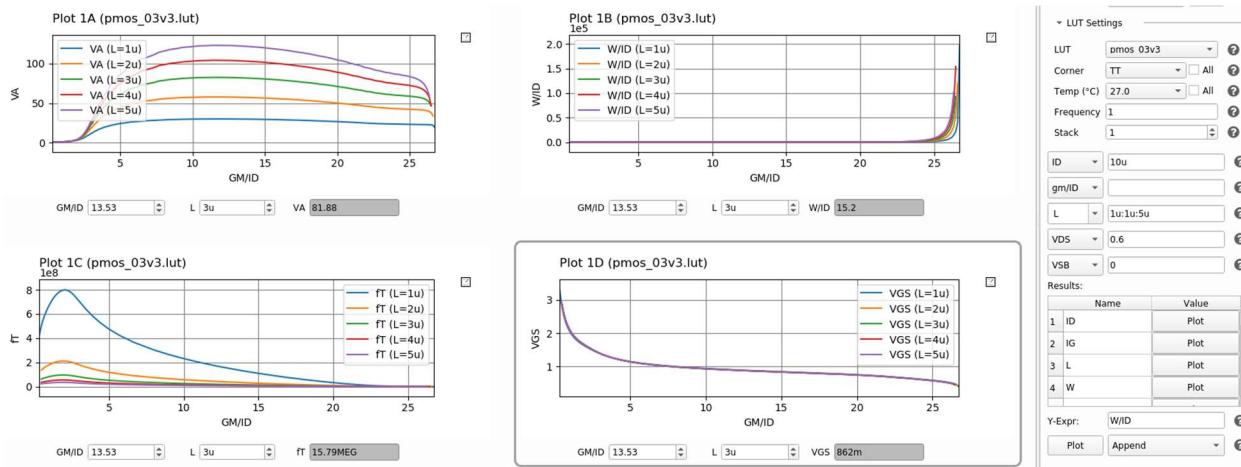
Analog IC Design

Lab 11 (Mini Project 02)

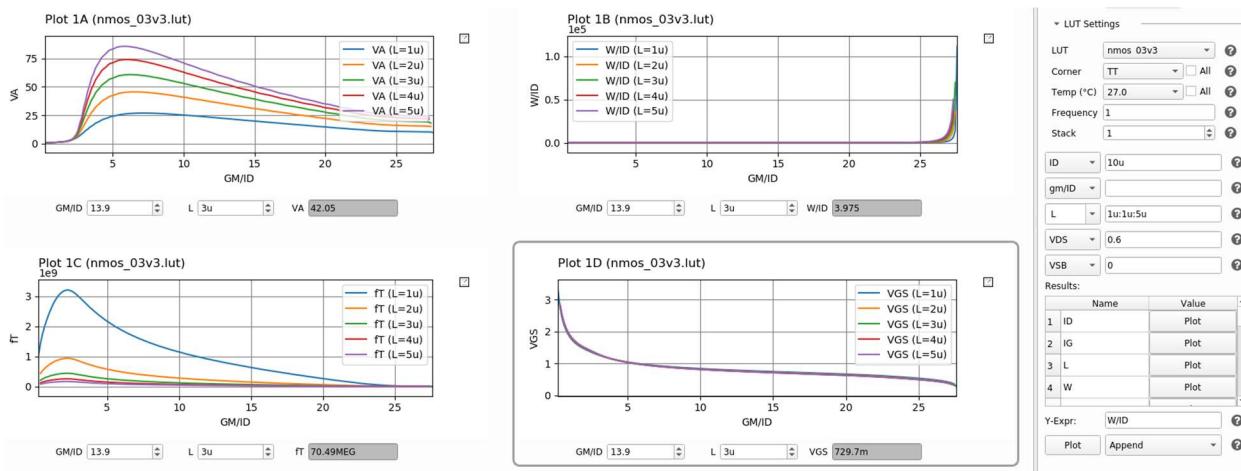
Fully Differential Folded Cascode OTA

PART 1: gm/ID Design Charts

PMOS



NMOS

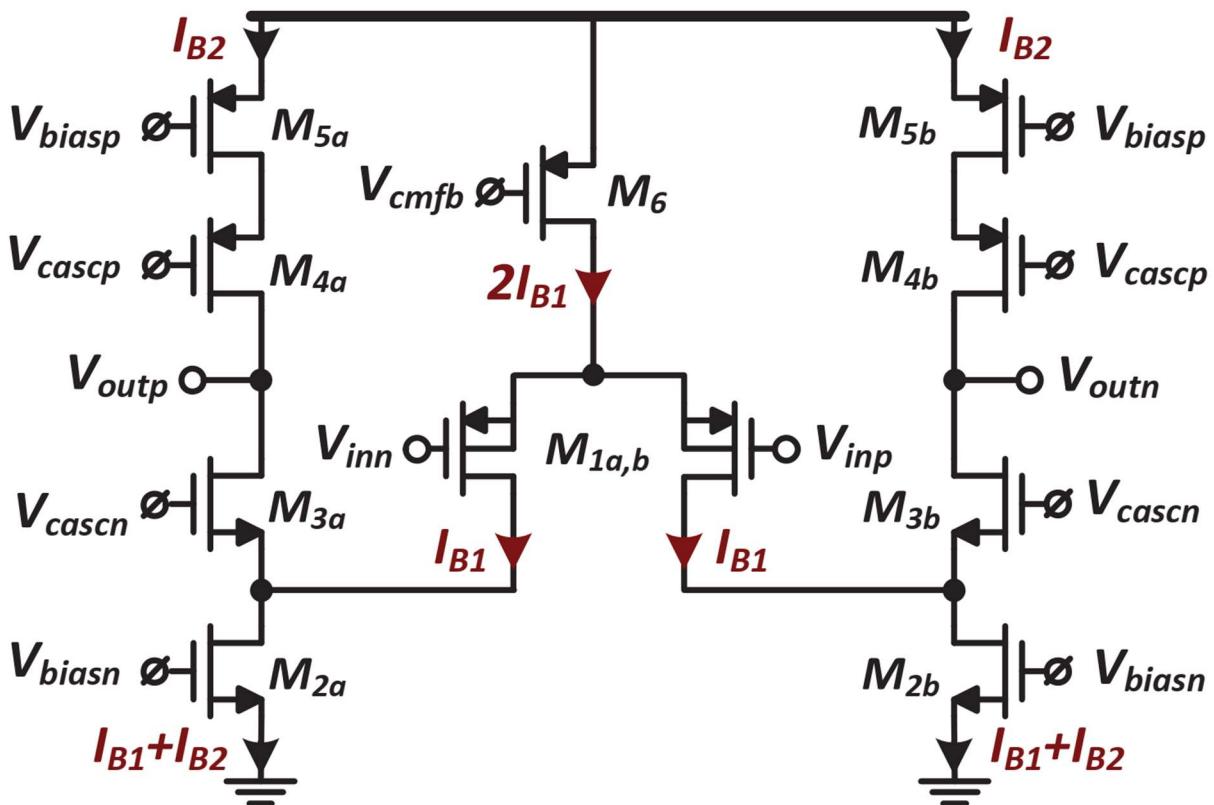


PART 2: OTA Design

Technology

GF180MCU

<i>Supply voltage</i>	2.5V
<i>Closed loop gain</i>	2
<i>Phase margin at the required ACL</i>	$\geq 70^\circ$
<i>CM input range – low</i>	≤ 0
<i>CM input range – high</i>	$\geq 1V$
<i>Differential output swing</i>	1.2Vpk-to-pk
<i>Load</i>	500fF
<i>DC Loop gain</i>	60dB
<i>CL settling time for 1% error</i>	100ns



The Design

$$VOUT = VIN (1 - e^{t/\tau}) \rightarrow \ln(0.01) = -t/\tau \rightarrow t = 100n$$

$$\tau = 21.71n \rightarrow \tau = \frac{1}{\omega} \rightarrow \omega = 46M$$

$$LG = \beta Aol$$

$$ACL \neq 1/\beta \rightarrow \beta = \frac{Cl}{Cf + Cs + C_{OTA}}$$

$$Assume C_{OTA} = 100f \rightarrow \beta \approx 0.3$$

$$DC.LG = \beta Aol \geq 1000$$

$$BW = \frac{\omega}{2\pi} = 7.32M$$

$$GBW = BW.ACL = 14.65M$$

$$GBW = \frac{gm}{2\pi * [CL + COTA + (Cf || (Cs + COTA))]}$$

$$gm \approx 175u$$

INPUT PAIR (PMOS).

We will use the short L and bias it in MI or WI this maximizes the GBW (good efficiency) and minimizes the input capacitive loading (avoid reducing the DC LG).

$$\text{Gain} = \frac{(gm \cdot ro)^2}{4} = 3 \text{ K} \rightarrow ro \approx 626\text{K} \rightarrow \frac{gm}{gds} = 110$$

We will use $ID = 10\text{u}$ $\rightarrow \frac{gm}{ID} = 17.5$

ID	10u	?
gm/ID	17.5	?
gm/gds	110	?
VDS	0.6	?
VSB	0	?
Results:		
Name	TT-27.0	
1 ID	10u	
2 IG	N/A	
3 L	370n	
4 W	35.21u	
5 VGS	792.6m	
6 VDS	600m	
7 VSB	0	
8 gm/ID	17.19	
9 Vstar	116.3m	

Cascode

We will use moderate L and bias it MI or WI, e.g., $L = 0.5\text{um}$ and $gm/ID = 15$, These transistors do not contribute significant offset and noise, so they don't need to be large. A large gm helps the gain and doesn't increase the noise.

We will use $ID = 10\text{u}$

(PMOS).

ID	10u	?
gm/ID	15	?
L	0.5u	?
VDS	0.6	?
VSB	0	?
Results:		
Name	TT-27.0	
1 ID	10u	
2 IG	N/A	
3 L	500n	
4 W	26.63u	
5 VGS	848.8m	
6 VDS	600m	
7 VSB	0	
8 gm/ID	14.94	
9 Vstar	133.8m	

NMOS

ID	10u	?
gm/ID	15	?
L	0.5u	?
VDS	0.6	?
VSB	0	?
Results:		
Name	TT-27.0	
1 ID	10u	
2 IG	N/A	
3 L	500n	
4 W	7.49u	
5 VGS	752.2m	
6 VDS	600m	
7 VSB	0	
8 gm/ID	14.91	
9 Vstar	134.1m	

Tail Current Source.

relatively long L and bias them in SI, e.g., L = 1um and gm/ID =10, These transistors contribute significant offset and noise. A large gm will not help the gain but will increase the offset and noise.

(PMOS).

(PMOS) Current Mirrors

NMOS Current Mirror

ID	20u
gm/ID	10
L	1u
VDS	0.6
VSB	0.3

Results:

Name	TT-27.0
1 ID	20u
2 IG	N/A
3 L	1u
4 W	37.8u
5 VGS	1.082
6 VDS	600m
7 VSB	300m
8 gm/ID	9.531
9 Vstar	209.9m

ID	10u
gm/ID	10
L	1u
VDS	0.6
VSB	0.3

Results:

Name	TT-27.0
1 ID	10u
2 IG	N/A
3 L	1u
4 W	18.9u
5 VGS	1.082
6 VDS	600m
7 VSB	300m
8 gm/ID	9.531
9 Vstar	209.9m

ID	20u
gm/ID	10
L	1u
VDS	0.6
VSB	0

Results:

Name	TT-27.0
1 ID	20u
2 IG	N/A
3 L	1u
4 W	9.13u
5 VGS	836.3m
6 VDS	600m
7 VSB	0
8 gm/ID	9.875
9 Vstar	202.5m

ID	10u
gm/ID	10
L	1u
VDS	0.6
VSB	0

Results:

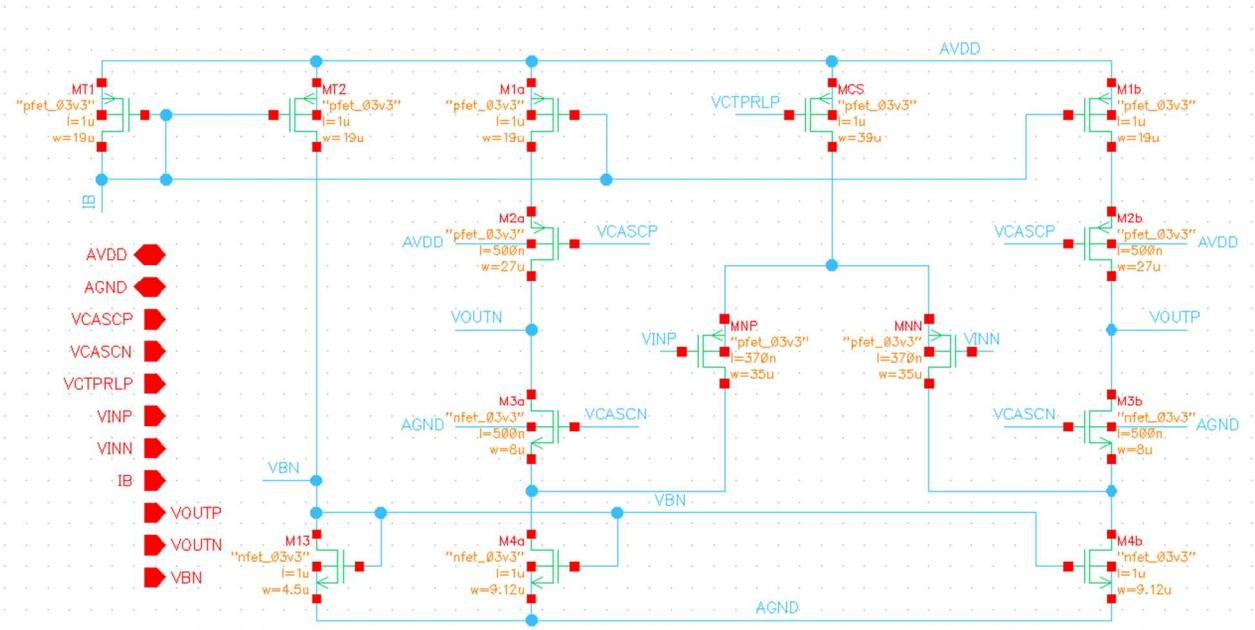
Name	TT-27.0
1 ID	10u
2 IG	N/A
3 L	1u
4 W	4.57u
5 VGS	836.1m
6 VDS	600m
7 VSB	0
8 gm/ID	9.88
9 Vstar	202.4m

OUT_DESINE_COCKPIT

Vstb_dm LG DC Gain	1.163k
Vstb_dm LG UGF	1.111MEG
Vstb_dm PM	74.68
Vstb_cm LG DC Gain	10.63k
Vstb_cm LG UGF	3.92MEG
Vstb_cm PM	23.29
DC Gain	999.1m
BW	1.726MEG
GBW	1.724MEG
UGF	N/A
Total Input ...	829.3u
Thermal Input Nois...	76.86f

Cgg	7.102p
Itotal	40u
VDD	2.5
VIN_CM	724.7m
VOUT_CM	954.5m
VBN	786.4m
VCASCN	1.037
VCASCP	1.38
VBP	1.708
VCMFB	1.63
VINP	724.7m
VINN	724.7m

M1a(W)	378.1u
M2a(W)	21.76u
M3a(W)	328.4u
M4a(W)	6.14u
M5a(W)	804.2u
M6(W)	316.2u
MVBN(W)	21.76u
MVBP(W)	804.2u
MVCMFB(W)	316.2u
MVBN(L)	1.484u
MVBP(L)	5.311u
MVCMFB(L)	3.459u

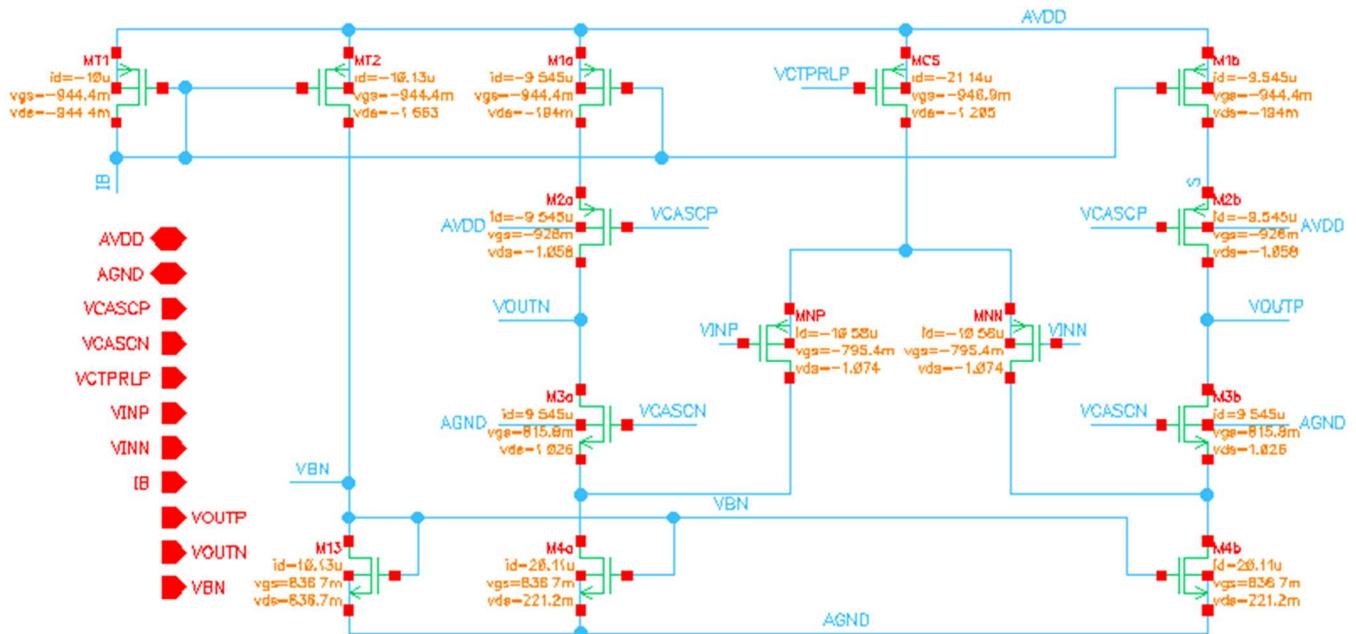


Select VREF to maximize the symmetrical output swing.

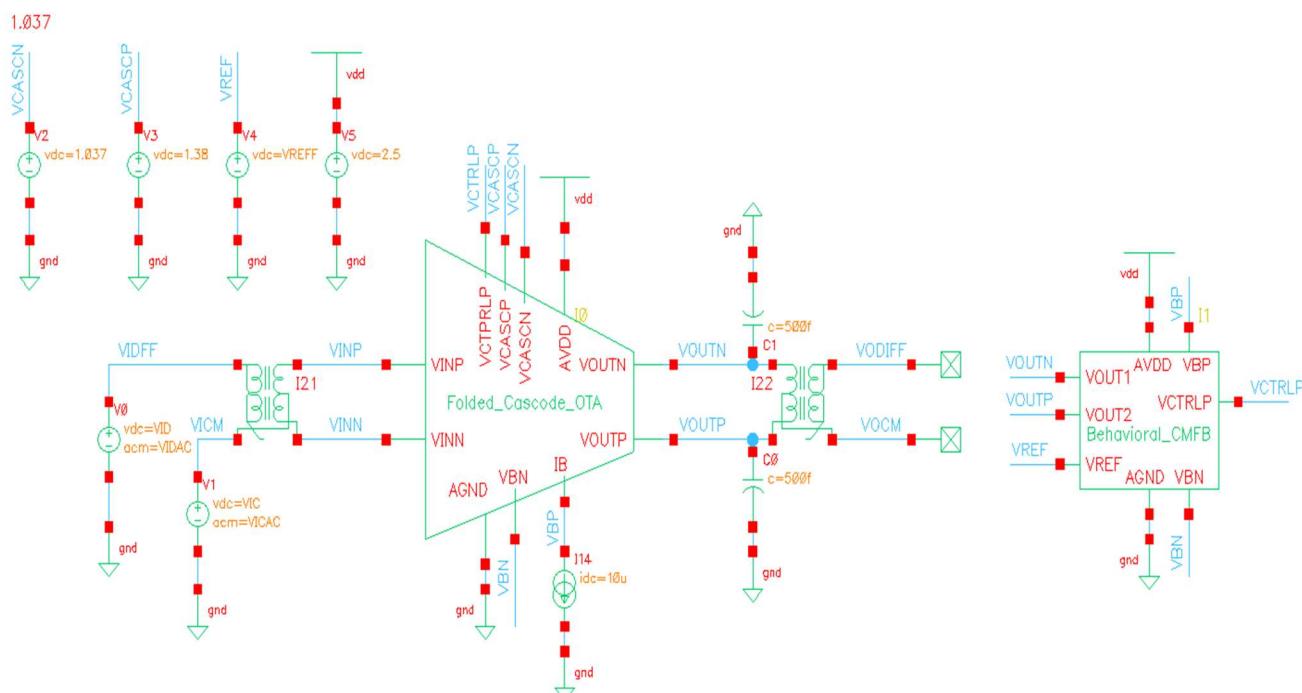
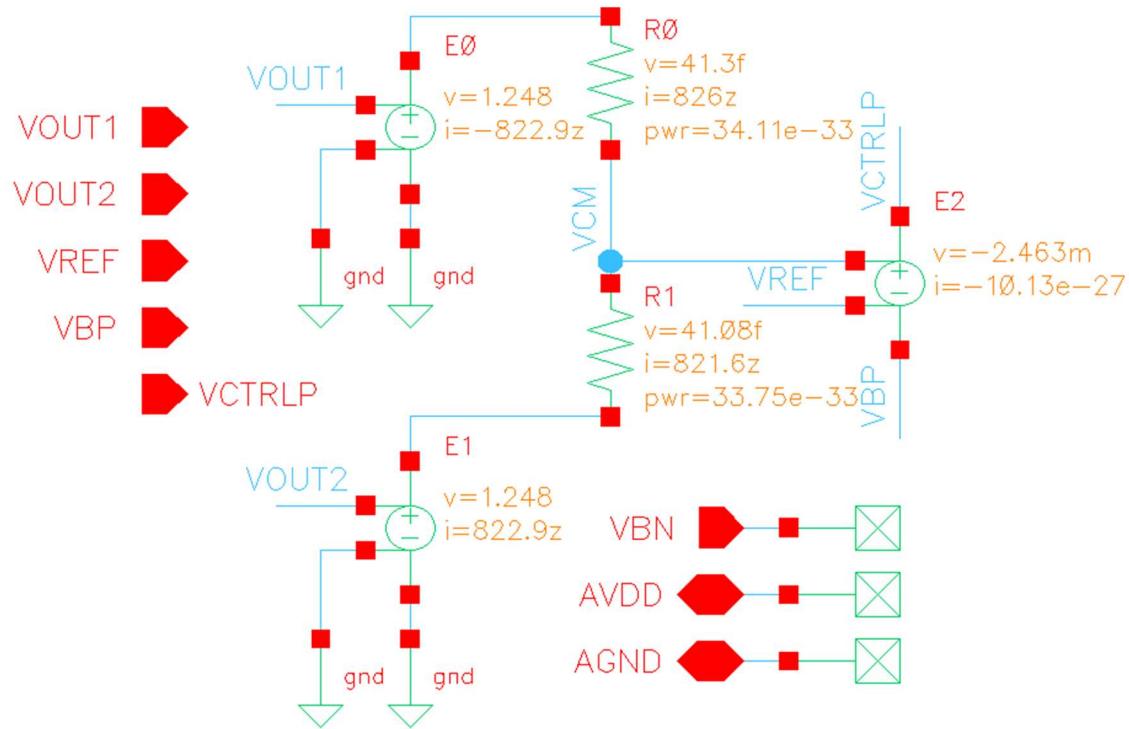
$$V_{out, max} = VDD - V_{cascp} - V_{PCM} \approx VDD - 2V^* \rightarrow V_{cascp} = 1.3$$

$$V_{out, min} = V_{cascn} - V_{NCM} \approx 2V^* \rightarrow V_{cascp} = 1.04$$

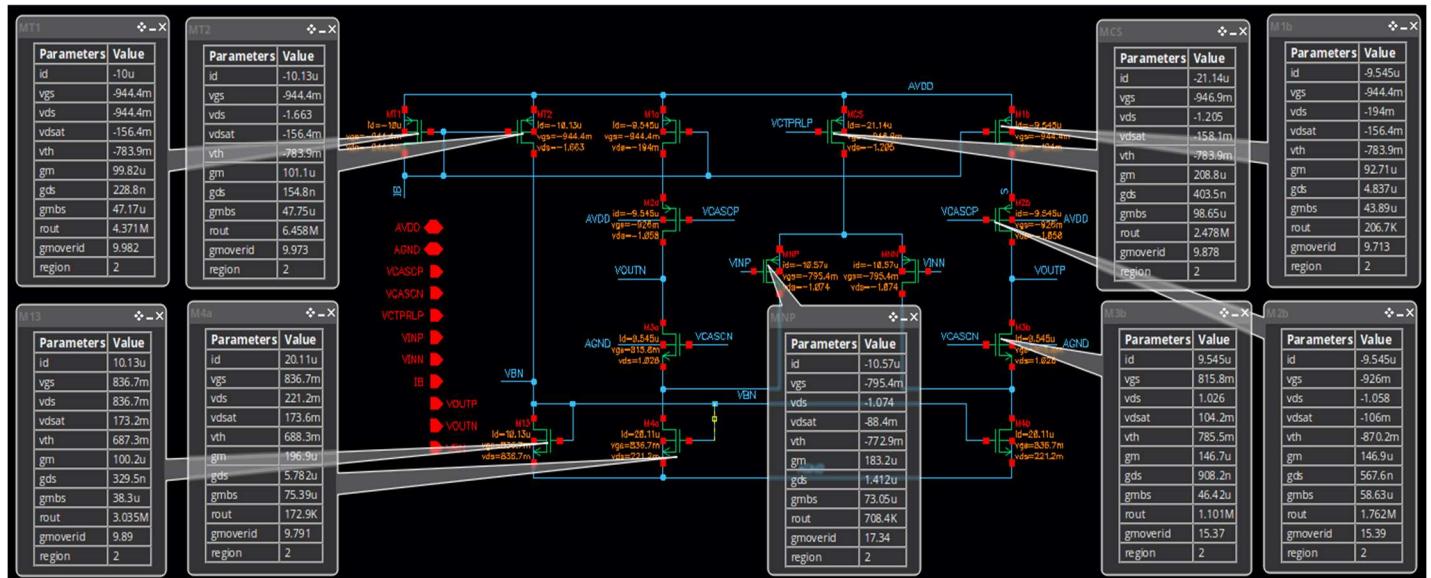
$$V_{out, CM} = (V_{out, max} + V_{out, min})/2 = VDD/2 = \text{VREF} = 2.5/2 = 1.25$$



PART 3: Open-Loop OTA Simulation (Behavioral CMFB)



1) Schematic of the OTA and bias circuit with DC node voltages and transistors OP parameters (id , vgs , vds , $vdsat$, vth , gm , gds , $region$) clearly annotated



Select VREF to maximize the symmetrical output swing.

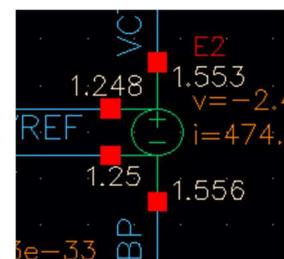
$$V_{out, CM} = \frac{V_{out, max} + V_{out, min}}{2} = \frac{V_{DD}}{2} = 1.25 = V_{REF}$$

What is the CM level at the OTA output?

The CM level at OTA output = $1.248 \text{ V} \approx \frac{VDD}{2} = VREF$

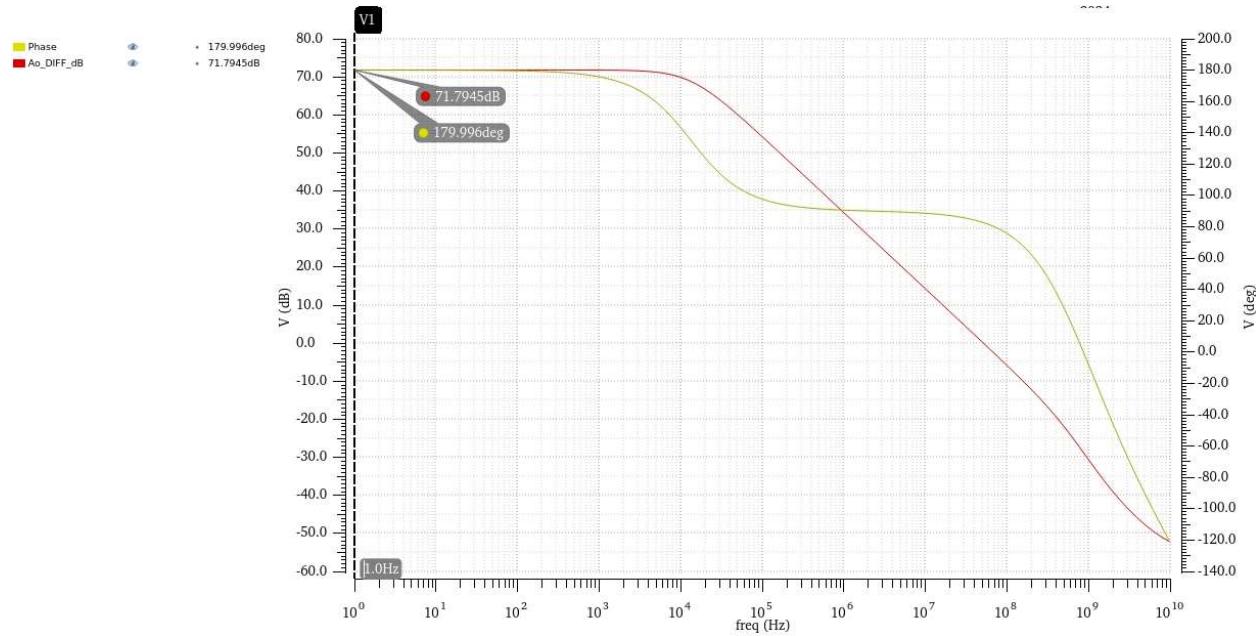
What are the differential input and output voltages of the error amplifier? What is the relation between them?

The differential input of the error amplifier is 2 mV, and the differential output is 3 mV the relation between them is $V_{indiff} \approx V_{outdiff}$ as the gain of the error amplifier is equal to 1.



Diff Small Signal.

Plot diff gain (magnitude in dB and phase) vs frequency.



Calculate circuit parameters (DC gain, BW, GBW, UGF, and PM).

Lab_11:TEST_Folded_Cascode_OTA_1:1	Ao_DIFF	
Lab_11:TEST_Folded_Cascode_OTA_1:1	Ao_DIFF_dB	
Lab_11:TEST_Folded_Cascode_OTA_1:1	Phase	
Lab_11:TEST_Folded_Cascode_OTA_1:1	AO	3.888k
Lab_11:TEST_Folded_Cascode_OTA_1:1	AO_dB	71.79
Lab_11:TEST_Folded_Cascode_OTA_1:1	BW	13.62k
Lab_11:TEST_Folded_Cascode_OTA_1:1	UGF	53.21M
Lab_11:TEST_Folded_Cascode_OTA_1:1	GBW	53.07M
Lab_11:TEST_Folded_Cascode_OTA_1:1	phase_Margin	82.66

Compare simulation results with hand calculations in a table (use SS parameters from OP simulation in your hand analysis).

$$\text{Diff Gain} = gm_{\text{input}} * \left(((gm + gmb) ro)_{\text{cascp}} * ro_{\text{PCM}} \right) \parallel \left(((gm + gmb) ro)_{\text{cascn}} * (ro_{\text{NCM}} || ro_{\text{input}}) \right) = 3.872K$$

$$BW = 1/(2\pi R_{out} * CL) = 13.83k$$

$$GBW = UGF = A_{vd} * BW = 53.95M$$

	Analytically	simulation
<i>DC Gain</i>	3.87k	3.88k
<i>BW</i>	13.83k	13.6k
<i>GBW</i>	53.95M	53.07M

PART 4: Open-Loop OTA Simulation (Actual CMFB)

$$\begin{aligned}
 \text{CMFB Current} &= 50\% \text{ of the amplifier current} \\
 &= 0.5 * (40 + 40 + 10)u = 25u \\
 \text{CMFB Current} &= 7.5 + 7.5 + 10 = 25u
 \end{aligned}$$

Buffer (assume ID = 7.5)

Current Mirror (PMOS):

The buffer current mirror should have the same L and gm/ID of the PMOS current mirror in the folded cascode OTA so we will use $L = 1\mu m$ and $gm/ID= 10$

ID	7.5u	
gm/ID	10	
L	1u	
VDS	0.9	
VSB	0	
Results:		
	TT-27.0	
1	ID	7.5u
2	IG	N/A
3	L	1u
4	W	14.56u
5	VGS	943.4m

CD (PMOS):

assume $L = 1 \mu m$ & $gm/ID= 15$

ID	7.5u	
gm/ID	15	
L	1u	
VDS	1.6	
VSB	0	
Results:		
	TT-27.0	
1	ID	7.5u
2	IG	N/A
3	L	1u
4	W	47.63u
5	VGS	846m

Amplifier

Tail CS (NMOS) (ID = 10u):

This device should have the same L and gm/ID of the NMOS current mirror in the folded cascode OTA so we will use $L = 1\mu m$ & $gm/ID = 10$

ID	10u
gm/ID	10
L	1u
VDS	0.9
VSB	0.3
Results:	
Name	TT-27.0
1 ID	10u
2 IG	N/A
3 L	1u
4 W	4.51u
5 VGS	942.9m

Load (PMOS), (ID = 10/2 = 5u):

this device should have the same L & gm/ID of the Tail CS of the folded cascode OTA, so we will use $L = 1\mu m$ & $gm/ID = 10$

ID	5u
gm/ID	10
L	1u
VDS	0.9
VSB	0
Results:	
Name	TT-27.0
1 ID	5u
2 IG	N/A
3 L	1u
4 W	9.71u
5 VGS	943.4m

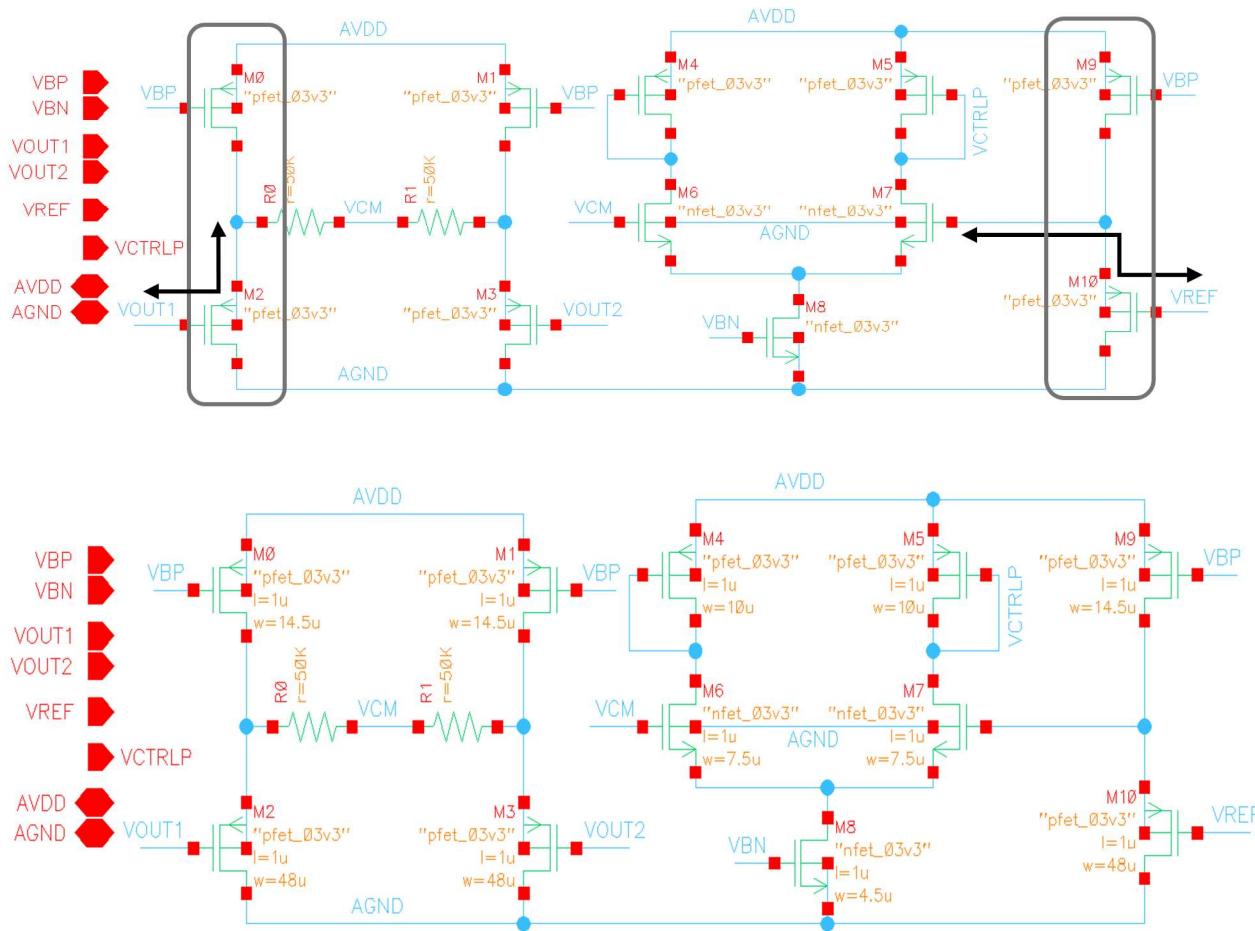
Input Pair (NMOS), (ID=5u):

assume $L = 1 \mu m$ & $gm/ID = 15$

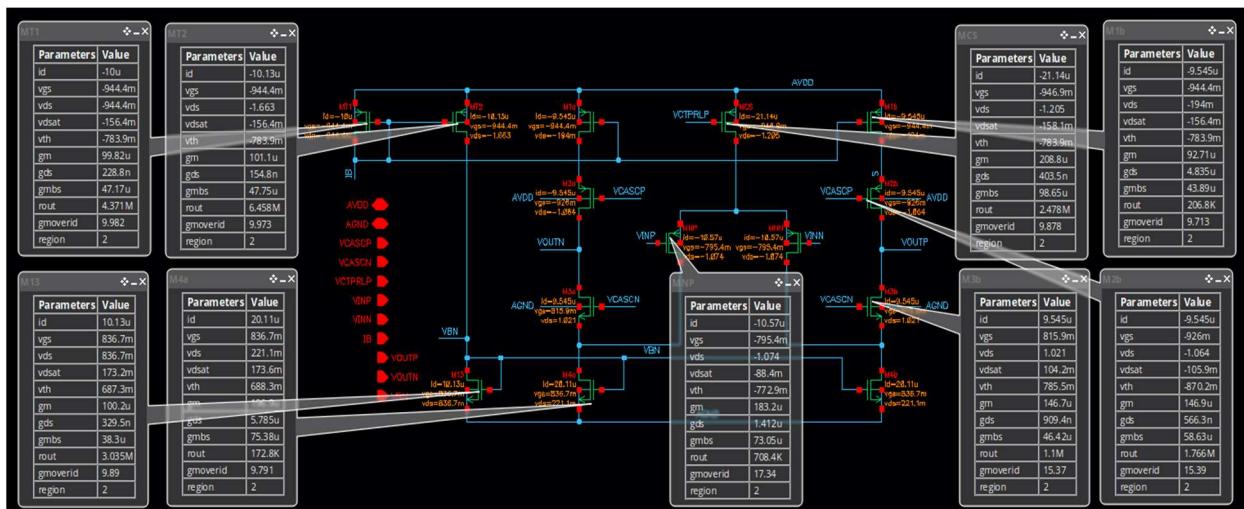
ID	5u
gm/ID	15
L	1u
VDS	0.9
VSB	0
Results:	
Name	TT-27.0
1 ID	5u
2 IG	N/A
3 L	1u
4 W	7.23u
5 VGS	741.6m

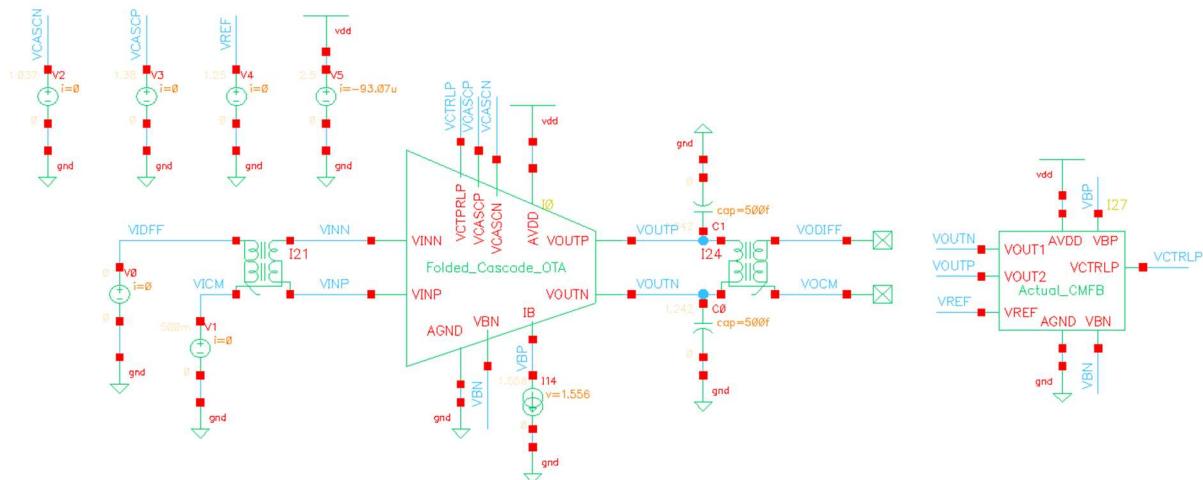
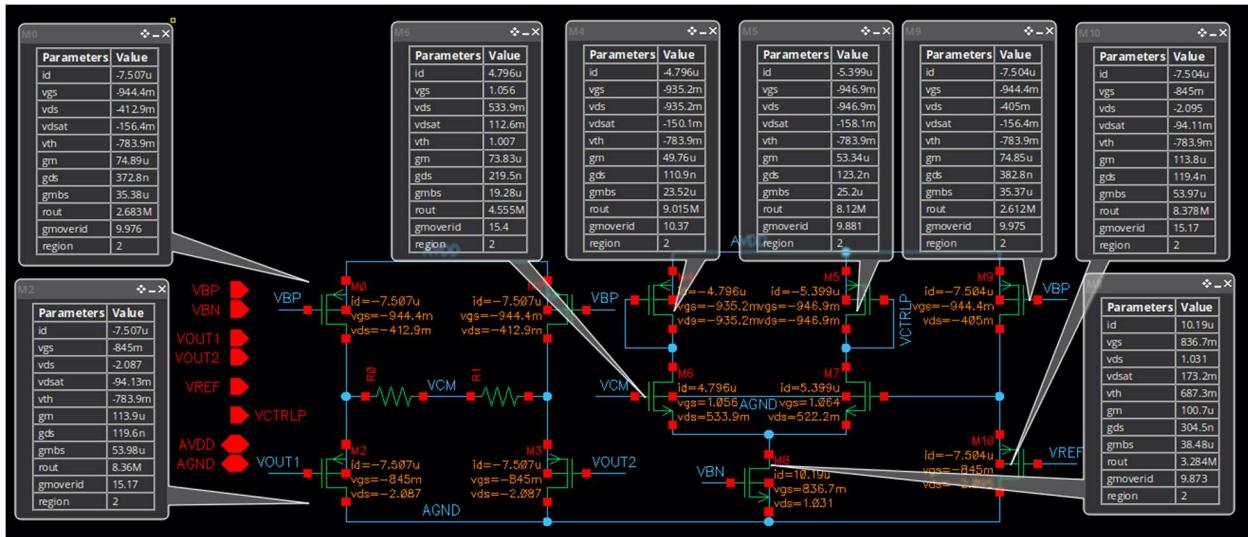
To the VREF matched with the CD buffer in the DC shift → enter the some buffer
 → you copy the buffer from CD → in the VREF.

$$VREF = \frac{VDD - vgs - v^*}{2} = 0.893V$$



1. Schematic of the OTA and CMFB circuit with DC node voltages and transistors OP parameters (id, vgs, vds, vdsat, vth, gm, gds, region) clearly annotated.





What is the CM level at the OTA output? Why?

CM level at the OTA level is 884.1 mV as expected because we used.

$V_{REF} = 893\text{mV}$, we note that we used $V_{REF} = 1.25\text{ V}$ with the behavioral CMFB and 893 mV with the actual CMFB and this is because actual buffer in the CMFB is implemented with a PMOS Common-Drain amplifier, so its VGS reduces the maximum output swing which reduces V_{REF} as well because $V_{REF} = \frac{V_{out,max} + V_{out,min}}{2}$

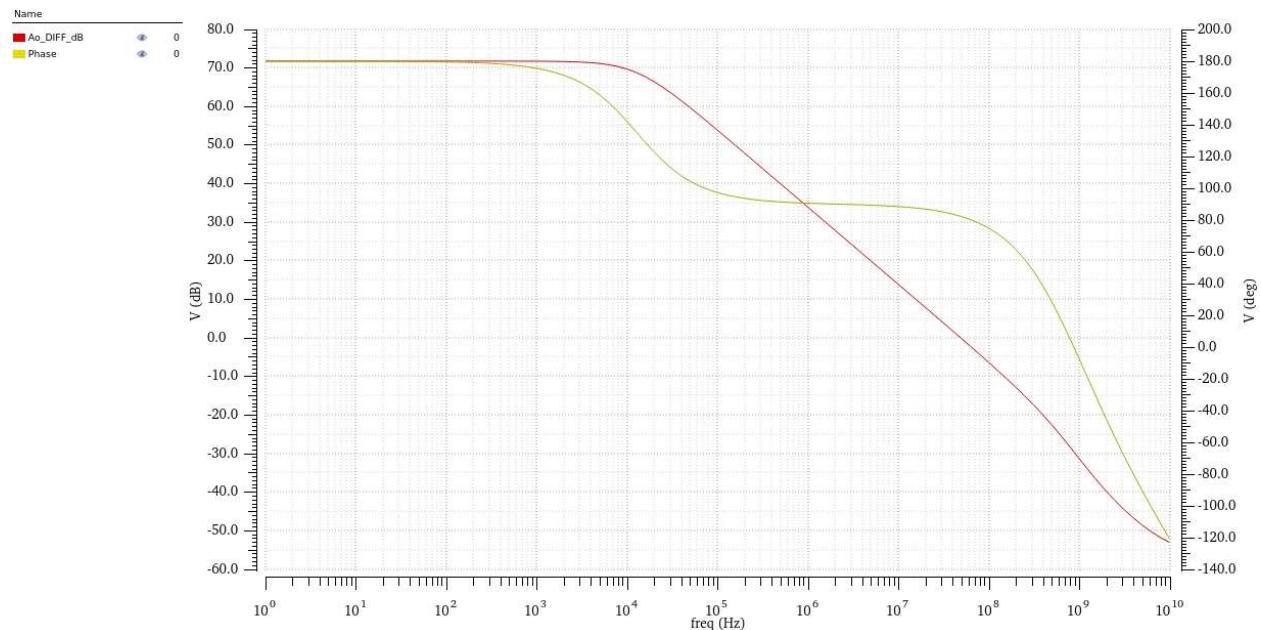
What are the differential input and output voltages of the error amplifier?
What is the relation between them?

The differential input of the error amplifier = $(V_{GS,CD} + V_{OCM}) - (V_{GS,CD} + V_{REF}) = 1.729\text{ V} - 1.738\text{ V} = -9\text{ mV}$.

The differential Output of the error amplifier = -9 mV , the relation between them is that $V_{indiff} = V_{outdiff}$ as the gain of the error amplifier is 1

2) Diff small signal ccs:

Plot diff gain (magnitude in dB and phase) vs frequency.

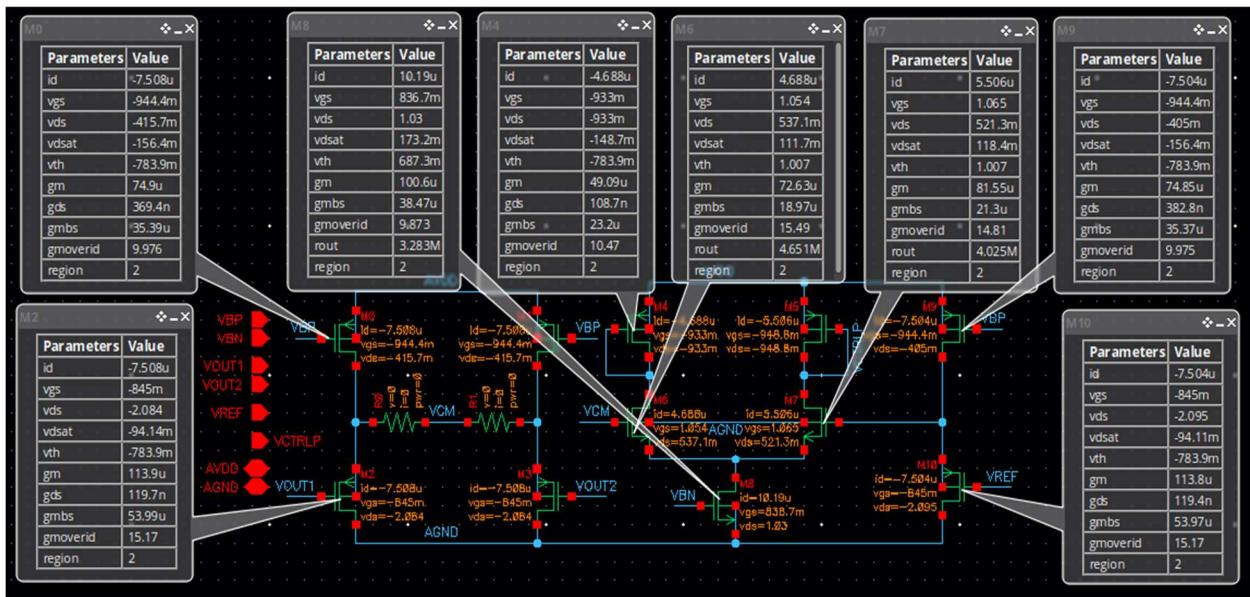
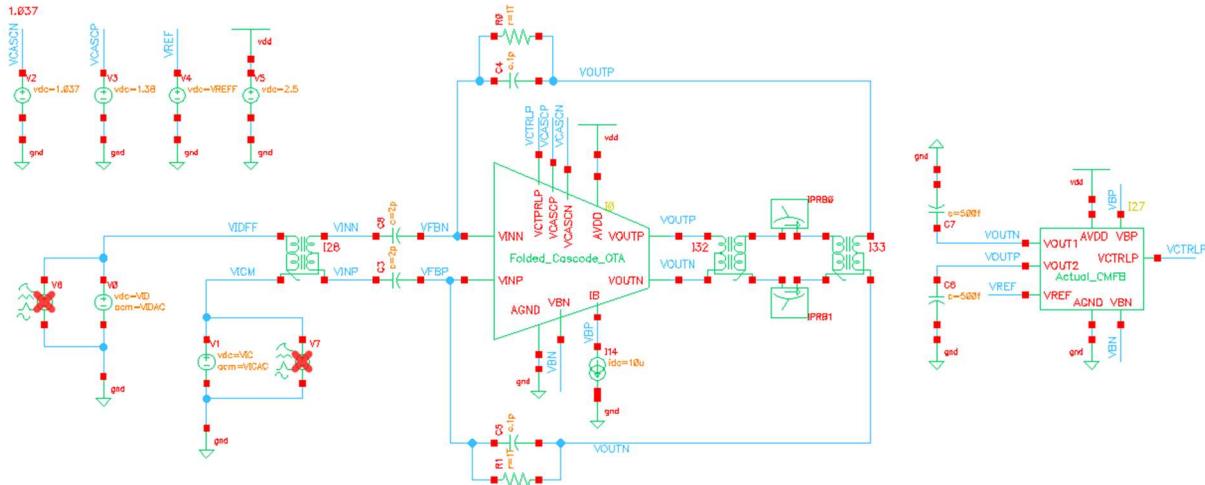


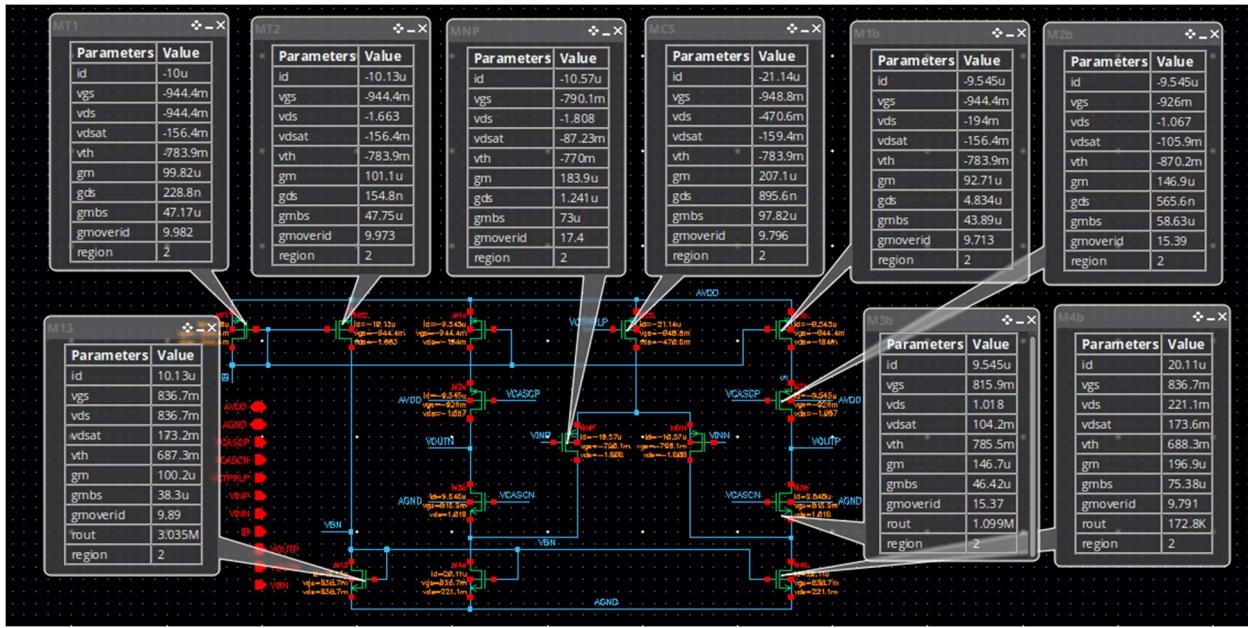
Calculate circuit parameters (DC gain, BW, GBW, UGF, and PM).

Lab_11:TEST_Folded_Cascode_OTA_1:1	Ao_DIFF	
Lab_11:TEST_Folded_Cascode_OTA_1:1	Ao_DIFF_dB	
Lab_11:TEST_Folded_Cascode_OTA_1:1	Phase	
Lab_11:TEST_Folded_Cascode_OTA_1:1	AO	3.885k
Lab_11:TEST_Folded_Cascode_OTA_1:1	AO_dB	71.79
Lab_11:TEST_Folded_Cascode_OTA_1:1	BW	12.87k
Lab_11:TEST_Folded_Cascode_OTA_1:1	UGF	49.74M
Lab_11:TEST_Folded_Cascode_OTA_1:1	GBW	50.13M
Lab_11:TEST_Folded_Cascode_OTA_1:1	phase_Margin	82.33

PART 5: Closed Loop Simulation (AC and STB Analysis)

1) Schematic of the OTA and the CMFB circuit with DC OP point clearly annotated in closed-loop configuration.





What is the CM level at the OTA output? Why?

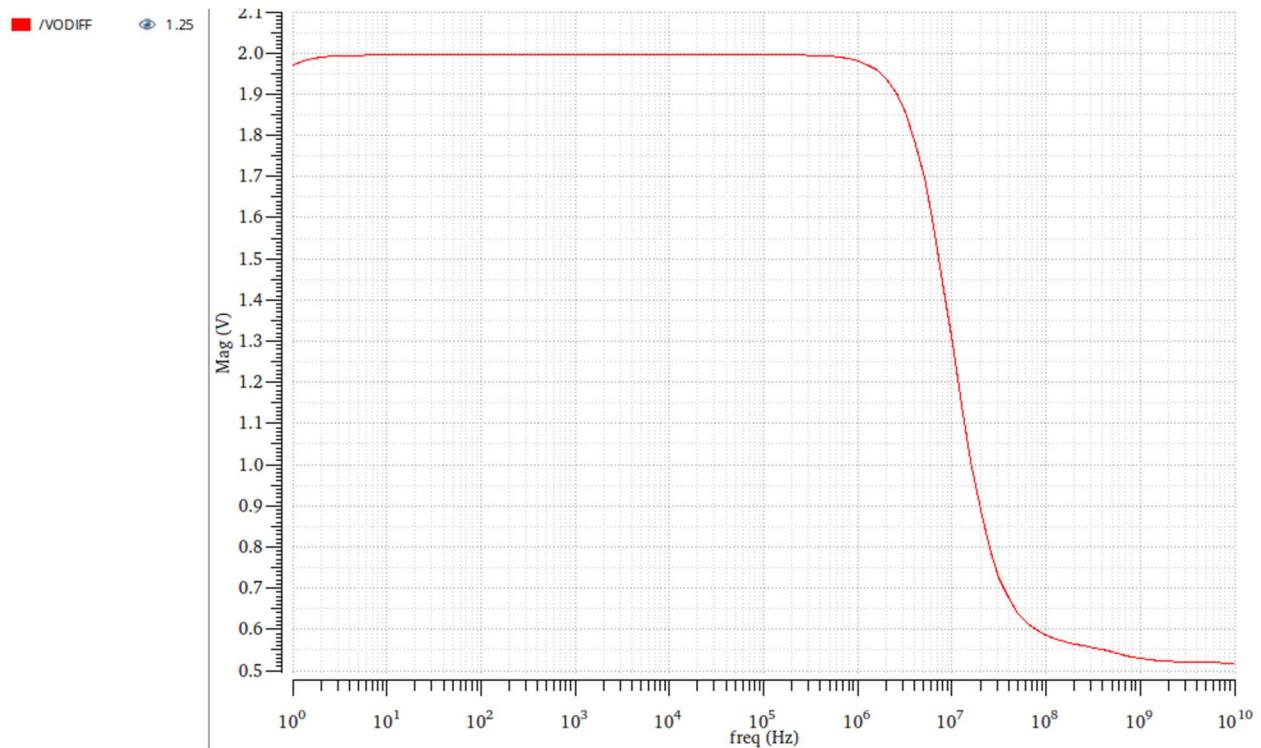
It's 889mV as expected as we used $V_{REF} = 893$ mV which is the voltage at which the CMFB circuit defines the output voltage to obtain maximum output swing.

What is the CM level at the OTA input? Why?

It's 889 mV identical to CM level at the output and this is because we used capacitors to block DC input and defined the CM level of the input using a very large feedback resistance (1T ohm) which takes 0 voltage drop which is the reason why the CM level of the input is exactly the CM level of the output.

Differential closed-loop response:

Plot VODIFF vs frequency.

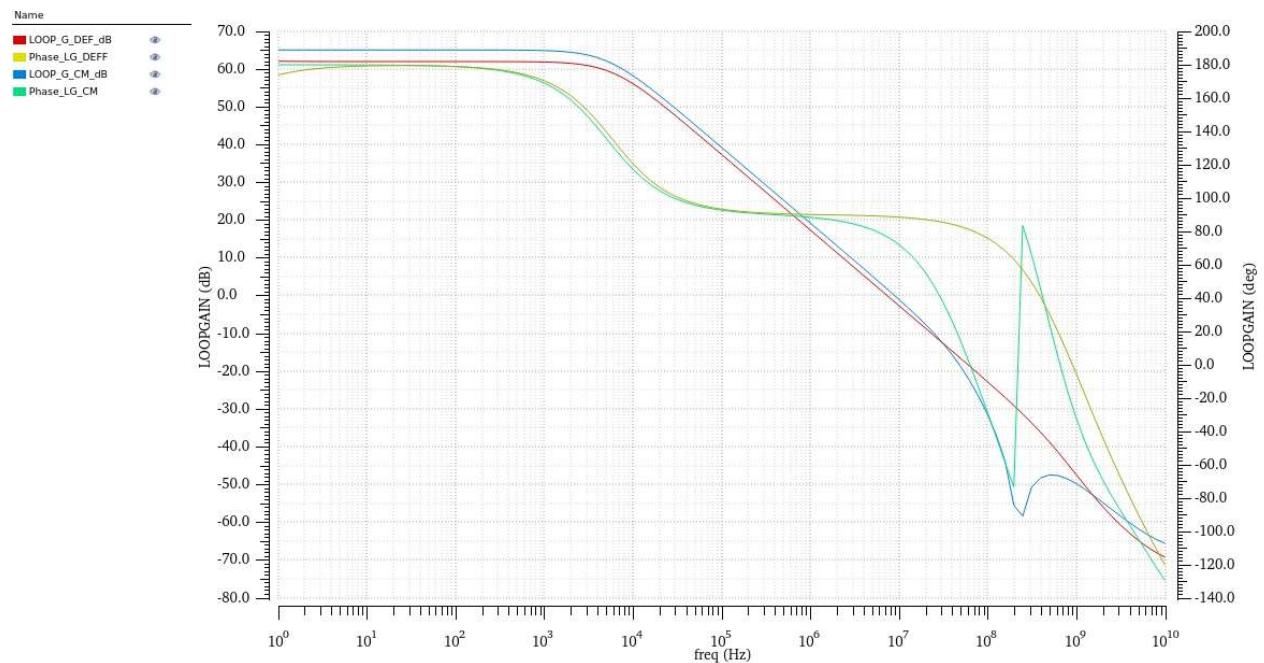


Use Measures or cursors to calculate circuit parameters (DC gain, CL BW, CL GBW).

Lab_11:Closed_Loop_ota_test2:1	AV_DEFF_CL	
Lab_11:Closed_Loop_ota_test2:1	AV_DEFF_CL_dB	
Lab_11:Closed_Loop_ota_test2:1	DC_Gain	1.998
Lab_11:Closed_Loop_ota_test2:1	DC_Gain_dB	6.014
Lab_11:Closed_Loop_ota_test2:1	BW_CL	8.616M
Lab_11:Closed_Loop_ota_test2:1	UGF_CL	16.22M
Lab_11:Closed_Loop_ota_test2:1	GBW_CL	17.05M

Differential and CMFB loops stability (STB analysis)

Plot loop gain in dB and phase vs frequency for the two simulations overlaid.



Compare GBW and PM of diff and CM loops. Comment

Diff Loop:

Lab_11:Closed_Loop_ota_test2:1	AO	1.277k
Lab_11:Closed_Loop_ota_test2:1	AO_dB	62.12
Lab_11:Closed_Loop_ota_test2:1	BW_CM	5.802k
Lab_11:Closed_Loop_ota_test2:1	UGF_CM	7.562M
Lab_11:Closed_Loop_ota_test2:1	GBW_CM	7.426M
Lab_11:Closed_Loop_ota_test2:1	LG_PM_CM	88.98

CM Loop:

Lab_11:Closed_Loop_ota_test2:1	AO	1.796k
Lab_11:Closed_Loop_ota_test2:1	AO_dB	65.09
Lab_11:Closed_Loop_ota_test2:1	BW_CM	5.157k
Lab_11:Closed_Loop_ota_test2:1	UGF_CM	9.197M
Lab_11:Closed_Loop_ota_test2:1	GBW_CM	9.287M
Lab_11:Closed_Loop_ota_test2:1	LG_PM_CM	73.9

CM loop has PM = 73 while Diff loop has PM = 88, 9 designed the CM loop to have more than 70 PM so that it has a critical damped response

BW → DEFF ≈ CM that would make the CM level of the output change the CM loop responses quickly and maintain the CM level constant.

Compare DC LG and GBW of the diff loop with those obtained from open-loop simulation. Comment.

	Open Loop	Closed Loop
<i>DC Gain</i>	$3.88k * 0.3 = 1.164K$	1.27k
<i>GBW</i>	$50.13M * 7/15 * 1/3 = 7.31M$	7.42M

In closed loop simulation we got DC LG = 1.27K while we got from open loop simulation $AvOL = 3.88K$, this is because the feedback factor $\beta < 1$ and to be precise $\beta = \frac{Cl}{C_f + C_s + C_{OTA}} \approx 0.3$ which justifies the previous statement. For GBW it was $gm, input CL$ in case of open loop, while it became $gm.input CEquivalent$ in case of closed loop, where $CEquivalent = CL + (CF \parallel CIN) \approx 15/7 pF$, and higher capacitance means lower GBW so GBW is reduced by a factor 7/15 because of capacitance increase and is reduced by a factor of $\beta \approx 0.3$ so GBW is reduced by a total of $7/15 * 1/3 = 0.17$, and we see that $7.31 / 50.13 = 0.17$ which justifies the previous statement. We also notice that BW is decreased because of equivalent capacitance increase.

PART 6: Closed Loop Simulation (Transient Analysis)

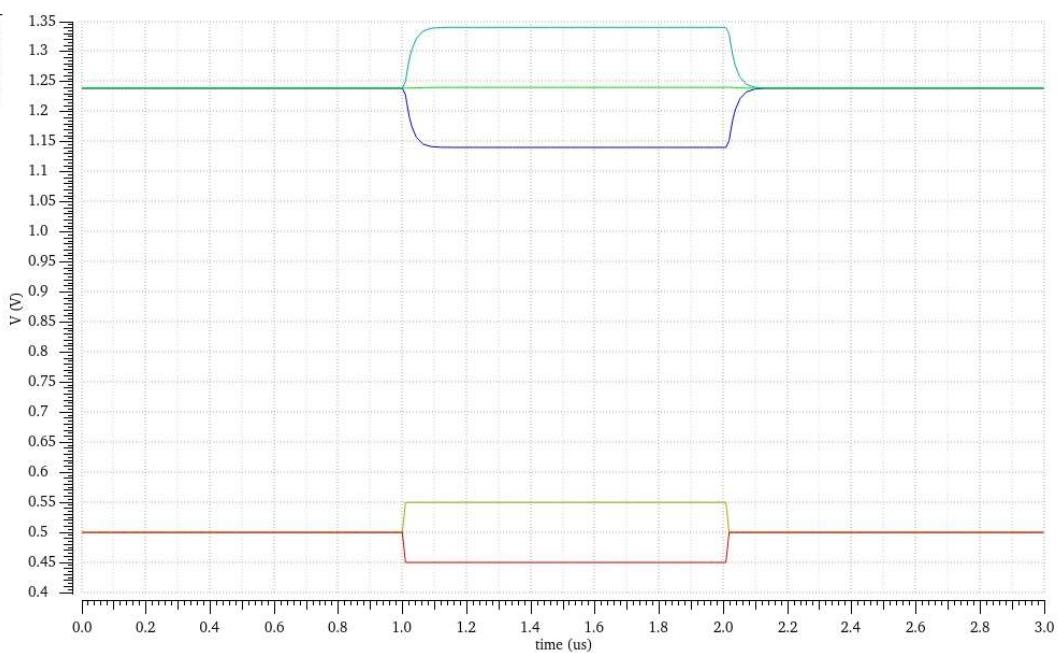
Differential and CMFB loops stability (transient analysis)

Plot the transient signals at VINP, VINN, VOUTP, VOUTN, and VOCM overlaid in the same figure.

Transient Analysis 'tran': time = (0 s -> 3

Name

/VINP
/VINN
/VOCM
/VOUTN
/VOUTP



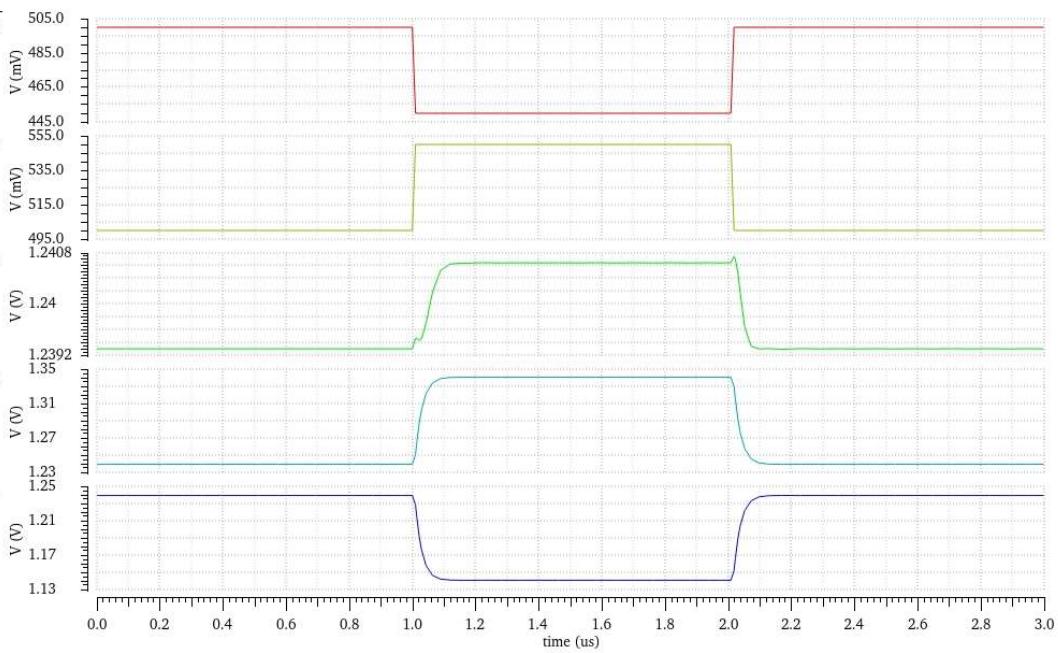
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Transient Analysis 'tran': time = (0 s -> 3

Name

/VINP
/VINN

/VOCM
/VOUTN
/VOUTP



1

Do you notice any differential/CM ringing? Are both loops stable with adequate PM?

No ringing at all and this is because both loops have $PM > 70$ which also means both loops are stable.

Calculate the 1% settling time and compare it to the required specification. If the specification is not satisfied, what design changes could be a possible solution?

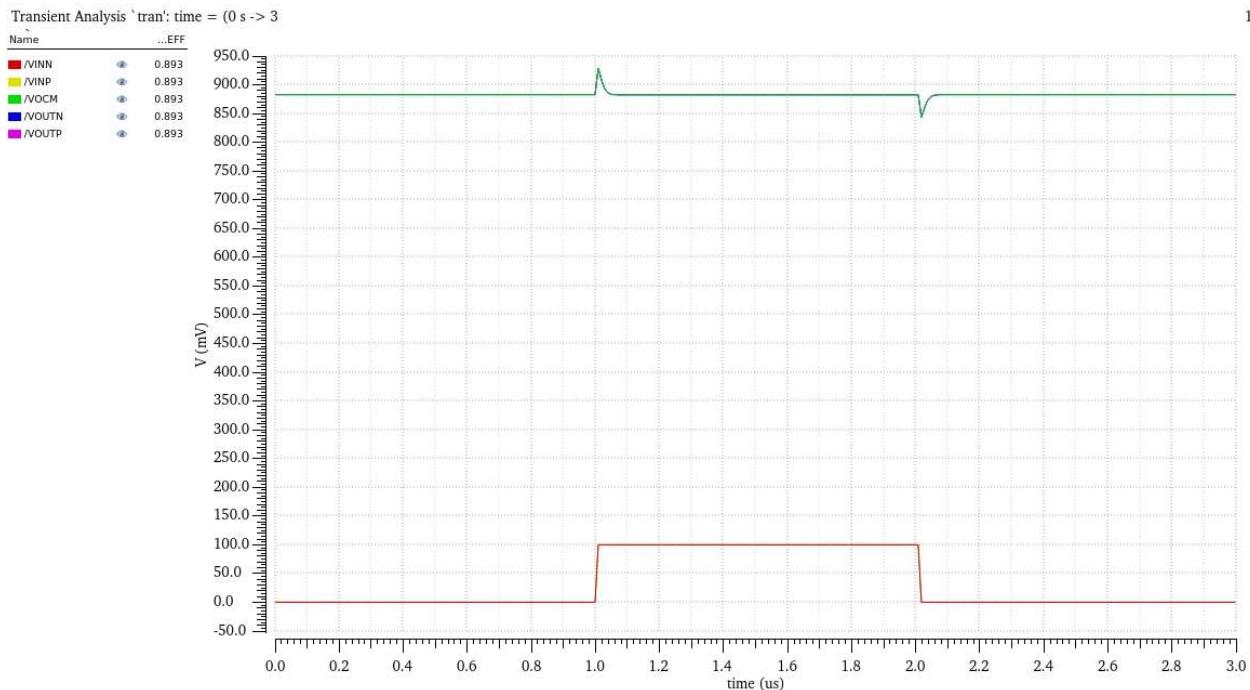
ota_test2:1	Settling_Time	91.9n
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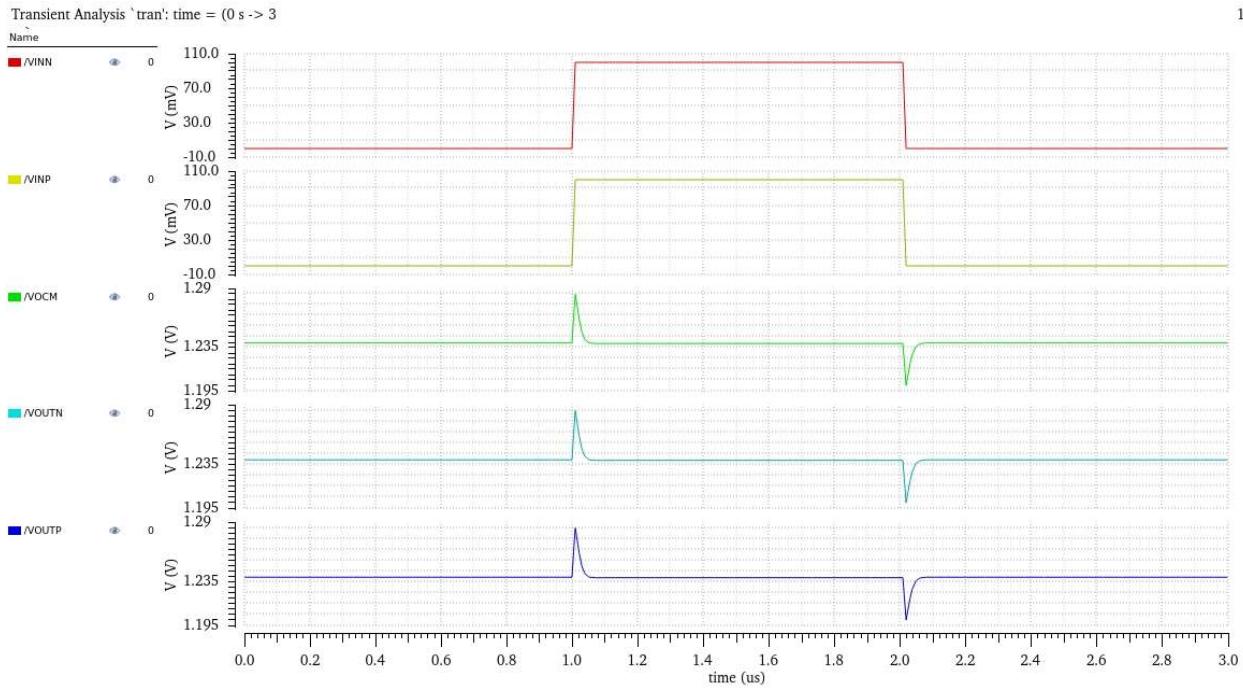
The simulation $\rightarrow 91.9n$ is perfect as the maximum is 100n

- The larger the bandwidth, the faster the types, which are determined by the shorter time. Bandwidth can be improved by reducing internal capacitors or improving gain stages.
- If the phase margin is low, this can lead to increased oscillation and overshoot, which prolongs the settling time \rightarrow can be changing the gm/id to in the input pair.

Differential and CMFB loops stability (transient analysis).

Plot the transient signals at VINN, VINP, VOUTN, and VOCM overlaid in the same figure.



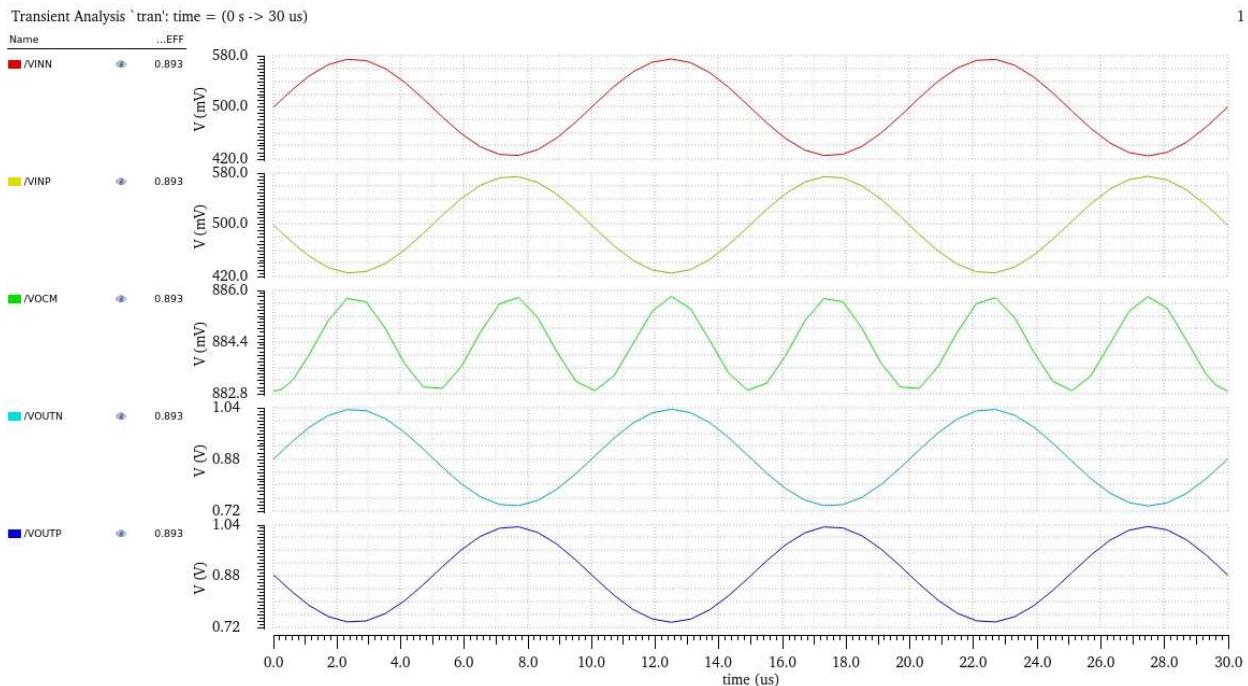
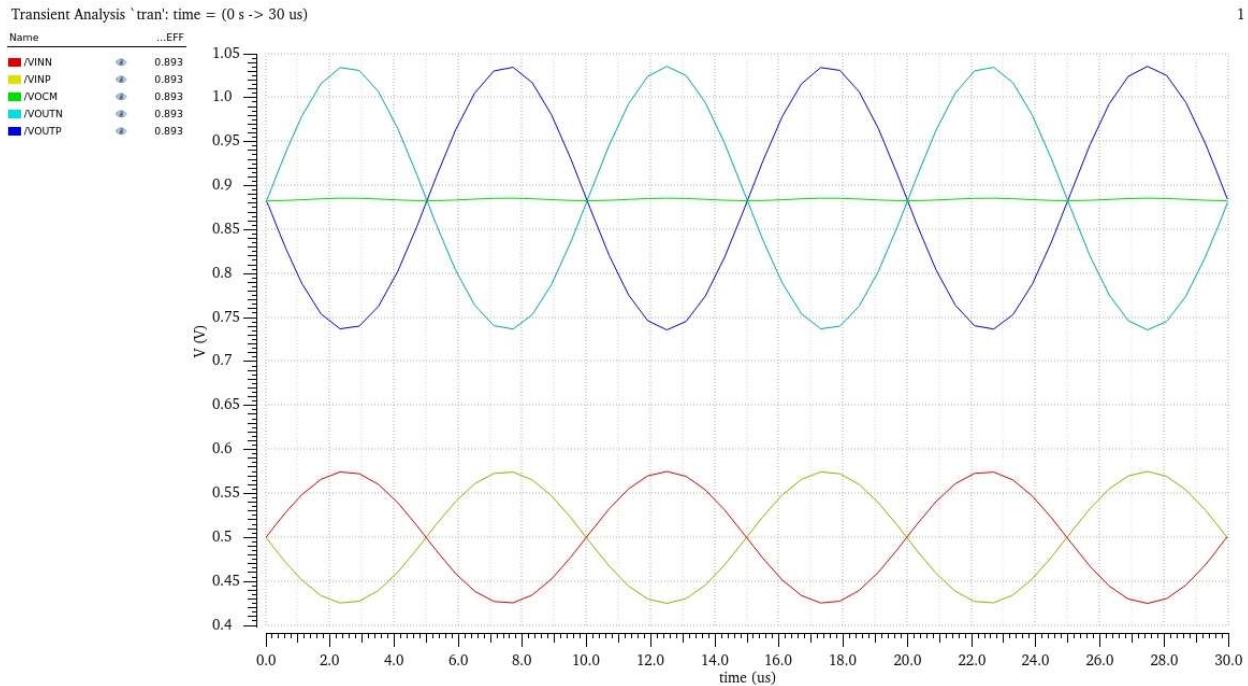


Do you notice any differential/CM ringing? Are both loops stable with adequate PM?

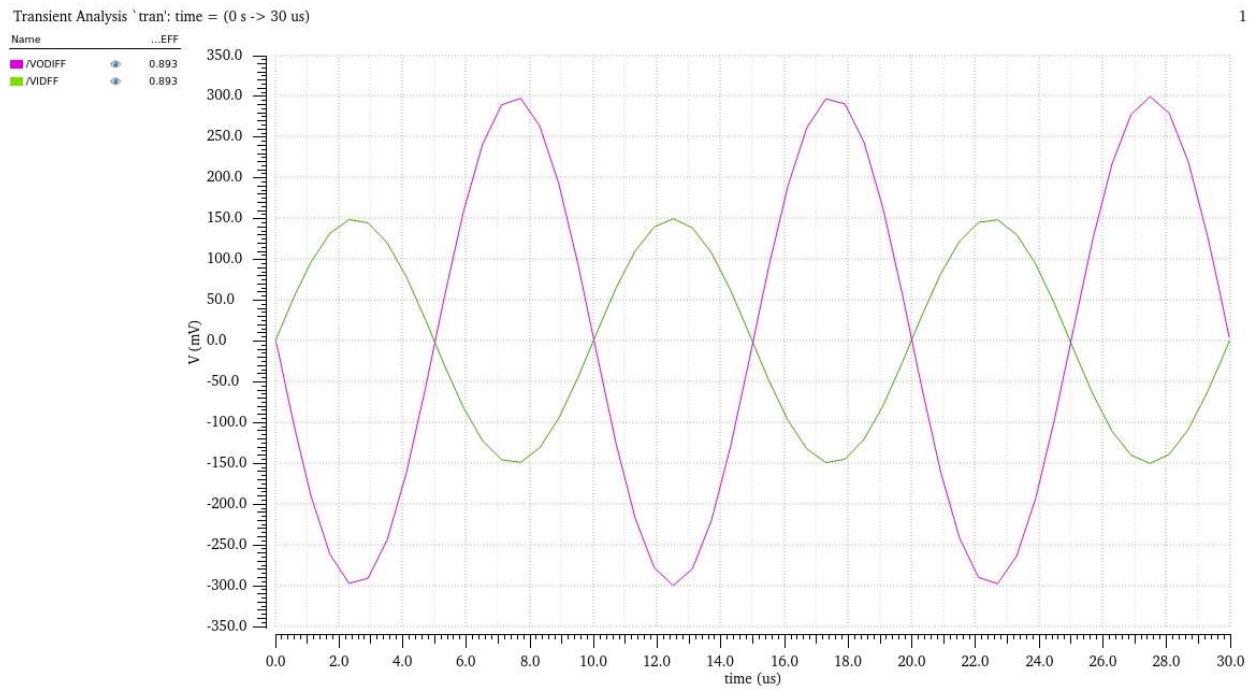
There's a slight spike in the outputs, but this is not due to ringing, this is because when the CM level of input changes (when applying the pulse) the output CM level tends to change as well but as soon as it starts changing the CMFB responds and forces it to change back to its original level which makes this spike at the edges of the pulse.

Output swing:

Plot the transient signals at VINP, VINN, VOUTP, VOUTN, and VOCM overlaid in the same figure.



Plot the transient signals at VIDIFF and VODIFF overlaid in the same figure.



Calculate the diff input and output peak-to-peak swings and the closed loop gain.

VIN_DEFF_PTP	300m
VOUT_DEFF_PTP	599.4m
Closed_Loop_Gain	1.998

Design simulation

<i>Closed loop gain</i>	2	1.99	✓
<i>Phase margin</i>	$\geq 70^\circ$	88.9	✓
<i>DC Loop gain</i>	60dB	62.12dB	✓
<i>CL settling time for 1% error.</i>	100ns	91.9n	✓