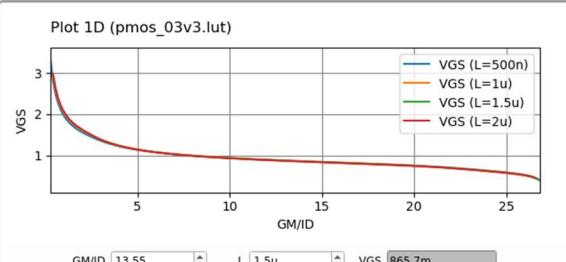
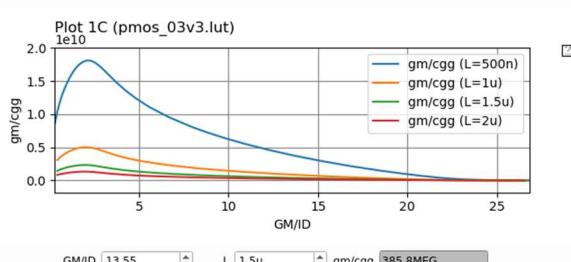
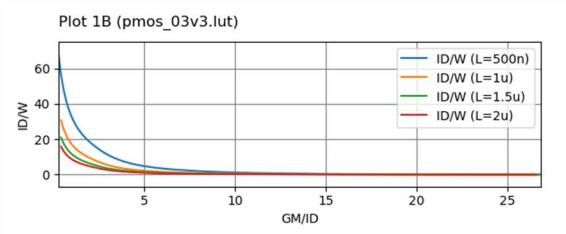
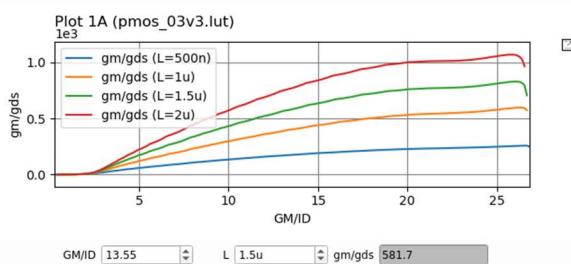
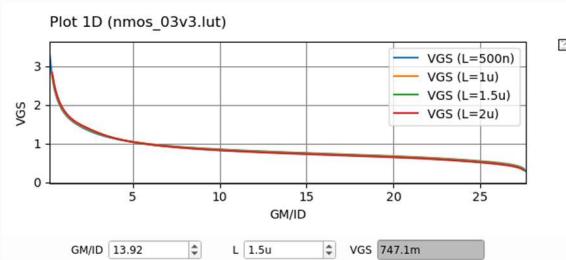
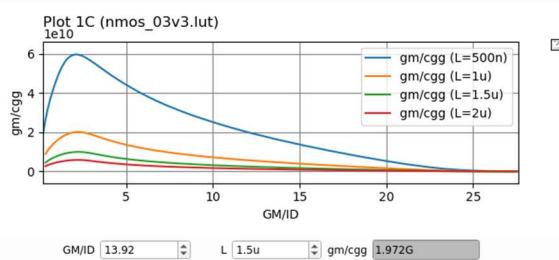
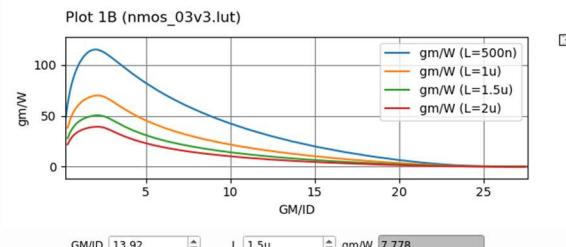
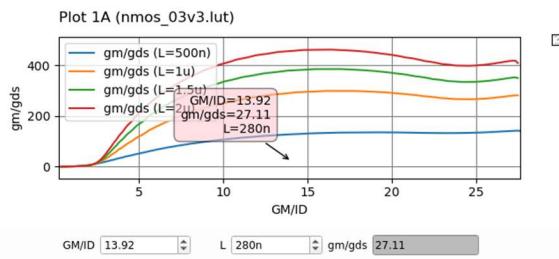


4Analog IC Design

Lab 09 (Mini Project 01)

Two-Stage Miller OTA

PART 1: gm/ID Design Charts

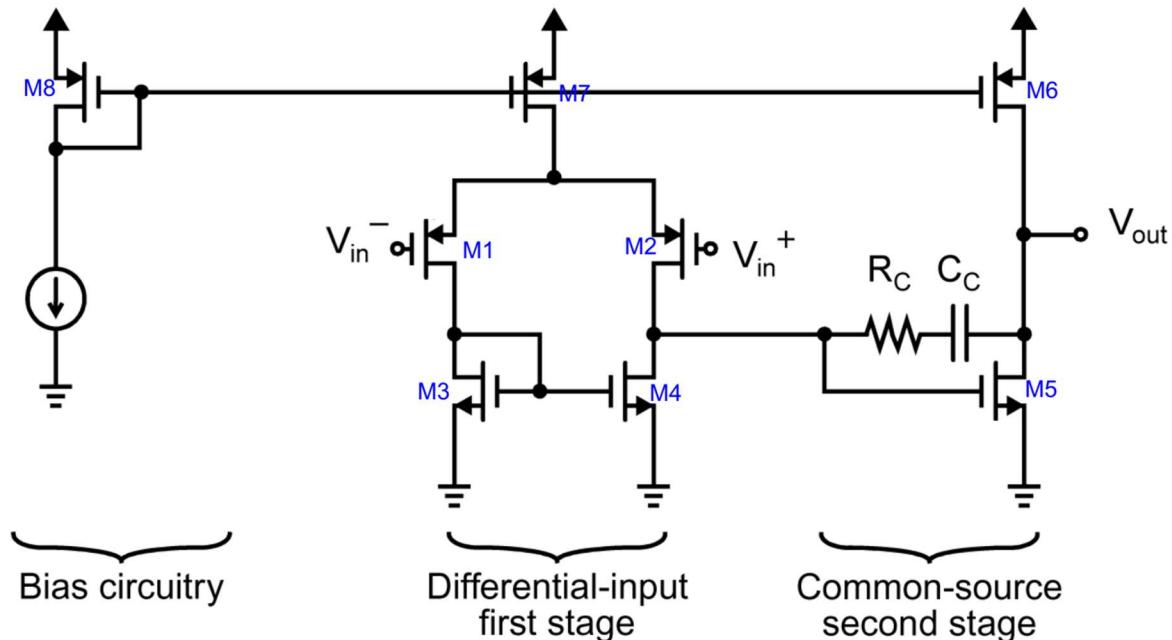


PART 2: OTA Design

The Greek alphabet

Technology	0.13um	0.18um
Supply voltage	1.2V	1.8V
Static gain error	<= 0.05%	<= 0.05%
CMRR @ DC	>= 74dB	>= 74dB
Phase margin (avoid pole-zero doublets)	>= 70°	>= 70°
OTA current consumption	<= 60uA	<= 60uA
CMIR – high	>= 0.6V	>= 1V
CMIR – low	<= 0.2V	<= 0.2V
Output swing	0.2 – 1V	0.2 – 1.6V
Load	5pF	5pF
Buffer closed loop rise time (10% to 90%)	<= 70ns	<= 70ns
Slew rate (SR)	5V/ μ s	5V/ μ s

CMIR closer to the ground rail than VDD rail so we choose the circuit to be PMOS topology.



Input pair (PMOS)

$$C_c = 0.5 \text{ } CL = 2.5 \text{ } pF.$$

$$t_{rise} = 2.2\tau \rightarrow \tau \leq (t_{rise, max}) / 2.2 = 70n/2.2 \rightarrow \tau \leq 31.81 \text{ ns.}$$

$$\tau = 1/BWCL = 1/UGFLG \rightarrow UGFLG \geq 31.436 \text{ M rad/s.}$$

$$UGFLG = gm_{1,2} / CC \rightarrow gm_{1,2} = gm_1 \geq 78.59 \mu S$$

$$SR = IB / CC \rightarrow IB = SR * CC = 12.5 \mu A \rightarrow IB_1 = IB/2 = 6.25 \mu A$$

$$gm/IB_1 = 78.59/6.25 = 12.5744 \text{ S/A}$$

$$AvOL = 1/S_{\text{error}} * 100 = 2000 \approx 66 \text{ dB}$$

Assign larger gain for the first stage (6dB difference).

$$AvOL1 = 36 \text{ dB} \text{ & } AvOL2 = 30 \text{ dB}$$

$$AvOL1 = gm_1 / 2 * gds = 63.09 \rightarrow gm / gds = 126.19$$

LUT	pmos_03v3	
Corner	tt	
Temp (°C)	27.0	
State1	<input type="button" value="Save State"/>	
ID	6.25u	
gm/ID	12.6	
gm/gds	126.19	
VDS	0.9	
VSB	0	

1	ID	6.25u			
2	IG	NaN		16	gm
3	L	390n		17	gmb
4	W	6.98u		18	gds
5	VGS	874.6m		19	ro
6	VDS	900m		20	VTH
7	VSB	0		21	VDSAT
8	gm/ID	12.61		22	cgg
9	Vstar	158.6m		23	cgs
10	IT	1.163G		24	cgd
11	gm/gds	118.6		25	cgb
12	VA	9.399		26	cdb
13	ID/W	895.4m		27	csb
14	gm/W	11.29		28	idnth2
15	AREA	2.722p		29	vgnth2
16	gm	78.83u		30	idnfl2
17	gmb	32.04u		31	vgnfl2
18	gds	665n		32	cdd
19	ro	1.504M		33	idmis
20	VTH	773.7m		34	vgmis

Load (NMOS)

Assume a relatively large gm/ID for CM load of 1st stage.

$$gm/ID = 15 \rightarrow ID = 6.25\mu A \rightarrow gm = 93.75 \mu S$$

$$gds \leq 623.2n$$

$$gm_2/gds = 150.4$$

LUT	nmos_03v3
Corner	tt
Temp (°C)	27.0
State1	Save State
ID	6.25u
gm/ID	15
gm/gds	150.4
VDS	0.6
VSB	0

1	ID	6.25u	16	gm	93.6u
2	IG	NaN	17	gmb	33.75u
3	L	540n	18	gds	641.4n
4	W	5.01u	19	ro	1.559M
5	VGS	750.5m	20	VTH	707.3m
6	VDS	600m	21	VDSAT	109m
7	VSB	0	22	cgg	7.735f
8	gm/ID	14.98	23	cgs	4.731f
9	Vstar	133.5m	24	cgd	975.1e-18
10	FT	1.926G	25	cgb	2.029f
11	gm/gds	145.9	26	cdb	-907.5e-18
12	VA	9.744	27	csb	4.616f
13	ID/W	1.248	28	idnth2	1.099e-24
14	gm/W	18.68	29	vgnth2	125.5e-18
15	AREA	2.705p	30	idnfl2	7.64e-18
16	gm	93.6u	31	vgnfl2	872p
17	gmb	33.75u	32	cdd	3.848f
18	gds	641.4n	33	idmis	135n
19	ro	1.559M	34	vgmis	1.442m

The mirror, tail (PMOS)

OTA current consumption $\leq 60\mu A$

$$IB1 = 12.5\mu A \rightarrow IB2 = 60 - 12.5 = 47.5\mu A$$

$$CMIRHIGH \geq 1V \rightarrow VDD - |VGS1| - VDsat3 \geq 1 \rightarrow VDsat3 \leq VDD - |VGS1| - 1 VGS = VDD/3 \rightarrow VDsat3 \leq 200 mV$$

$$Output SwingHIGH \geq 1.6 \rightarrow VDD - VDsat6 \geq 1.6 \rightarrow VDsat6 \leq 200 mV$$

This assumption already adds some margin to make sure they are driven a little more into saturation.

Choose $VDsat7 = VDsat6 = 180 mV$

$$Assume V* = VDsat \rightarrow (gm/ID)7 = (gm/ID)6 = 2/V* = 12 S/A.$$

$$CMRR \text{ in dB} = Avd - AvCM \rightarrow AvCM \leq Avd - CMRR = 36 - 74 = -38 \text{ dB} = 0.0125$$

$$AvCM = 1/2gm3.4RSS = gds7/2gm3 \rightarrow gds7 \leq 2AvCM * gm3 = 2.34 \mu S.$$

$$gm/ID = 12 \rightarrow gm = gm7 = 150 \mu S \rightarrow gm/gds \geq 64.102$$

LUT	pmos_03v3
Corner	tt
Temp (°C)	27.0
State1	
ID	12.5u
gm/ID	12
gm/gds	64.1
VDS	0.3
VSB	0.3

1	ID	12.5u	16	gm	142.1u
2	IG	NaN	17	gmb	51.04u
3	L	430n	18	gds	2.391u
4	W	14.03u	19	ro	418.2k
5	VGS	1.017	20	VTH	898.2m
6	VDS	300m	21	VDSAT	154m
7	VSB	300m	22	cgg	22.06f
8	gm/ID	11.37	23	cgs	16.13f
9	Vstar	176m	24	cgd	2.409f
10	fT	1.025G	25	cgb	3.522f
11	gm/gds	59.41	26	cdb	-7.273f
12	VA	5.227	27	csb	10.48f
13	ID/W	890.9m	28	idnth2	1.73e-24
14	gm/W	10.13	29	vgnth2	85.69e-18
15	AREA	6.033p	30	idnfl2	8.278e-18
16	gm	142.1u	31	vgnfl2	410.1p
17	gmb	51.04u	32	cdd	8.928f
18	gds	2.391u	33	idmis	413.2n
19	ro	418.2k	34	vgmis	2.908m

LUT	pmos_03v3
Corner	tt
Temp (°C)	27.0
State1	
ID	18u
gm/ID	12
gm/gds	64.1
VDS	0.9
VSB	0.3

1	ID	10u	16	gm	115.7u
2	IG	NaN	17	gmb	34.9u
3	L	320n	18	gds	1.941u
4	W	7.3u	19	ro	515.2k
5	VGS	963.9m	20	VTH	850.6m
6	VDS	900m	21	VDSAT	154.9m
7	VSB	300m	22	cgg	9.532f
8	gm/ID	11.57	23	cgs	6.744f
9	Vstar	172.8m	24	cgd	1.113f
10	fT	1.932G	25	cgb	1.675f
11	gm/gds	59.61	26	cdb	-2.304f
12	VA	5.152	27	csb	5.165f
13	ID/W	1.37	28	idnth2	1.264e-24
14	gm/W	15.85	29	vgnth2	94.43e-18
15	AREA	2.336p	30	idnfl2	17.81e-18
16	gm	115.7u	31	vgnfl2	1.33n
17	gmb	34.9u	32	cdd	4.344f
18	gds	1.941u	33	idmis	437.1n
19	ro	515.2k	34	vgmis	3.778m

LUT	pmos_03v3
Corner	tt
Temp (°C)	27.0
State1	
ID	47.5u
gm/ID	12
gm/gds	64.1
VDS	0.9
VSB	0.3

1	ID	47.5u	16	gm	549.6u
2	IG	NaN	17	gmb	165.7u
3	L	320n	18	gds	9.22u
4	W	34.66u	19	ro	108.5k
5	VGS	963.9m	20	VTH	850.6m
6	VDS	900m	21	VDSAT	155m
7	VSB	300m	22	cgg	45.26f
8	gm/ID	11.57	23	cgs	32.02f
9	Vstar	172.9m	24	cgd	5.283f
10	fT	1.933G	25	cgb	7.954f
11	gm/gds	59.61	26	cdb	-10.94f
12	VA	5.152	27	csb	24.52f
13	ID/W	1.37	28	idnth2	6.005e-24
14	gm/W	15.86	29	vgnth2	19.88e-18
15	AREA	11.09p	30	idnfl2	84.63e-18
16	gm	549.6u	31	vgnfl2	280.2p
17	gmb	165.7u	32	cdd	20.63f
18	gds	9.22u	33	idmis	2.076u
19	ro	108.5k	34	vgmis	3.777m

Common-source 2 (NMOS)

$$\omega p2 = 4\omega u \rightarrow gm5 = 4*gm1,2 * (CL/Cc) = 8* gm1 = 751.52 \mu S, 712.5$$

$$Gm/ID = 751.52 / 47.5 = 15.82 S/A \rightarrow 15$$

15 → to be like load.

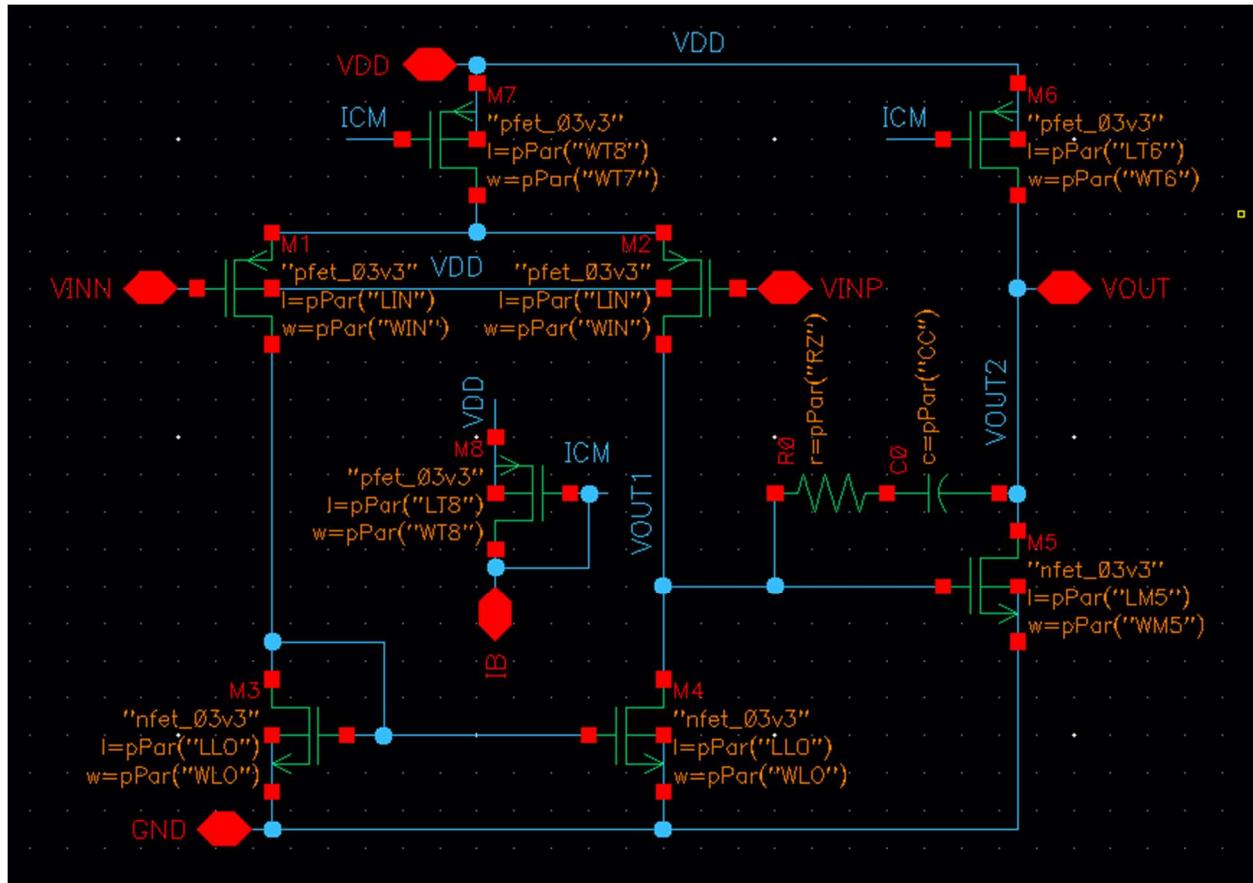
$$AvOL2 \geq 30 dB = 31.6 = gm5 / (gds5+gds6) \rightarrow gds5 = 13.45 \mu S.$$

$$(gm/gds)5 = 52.97$$

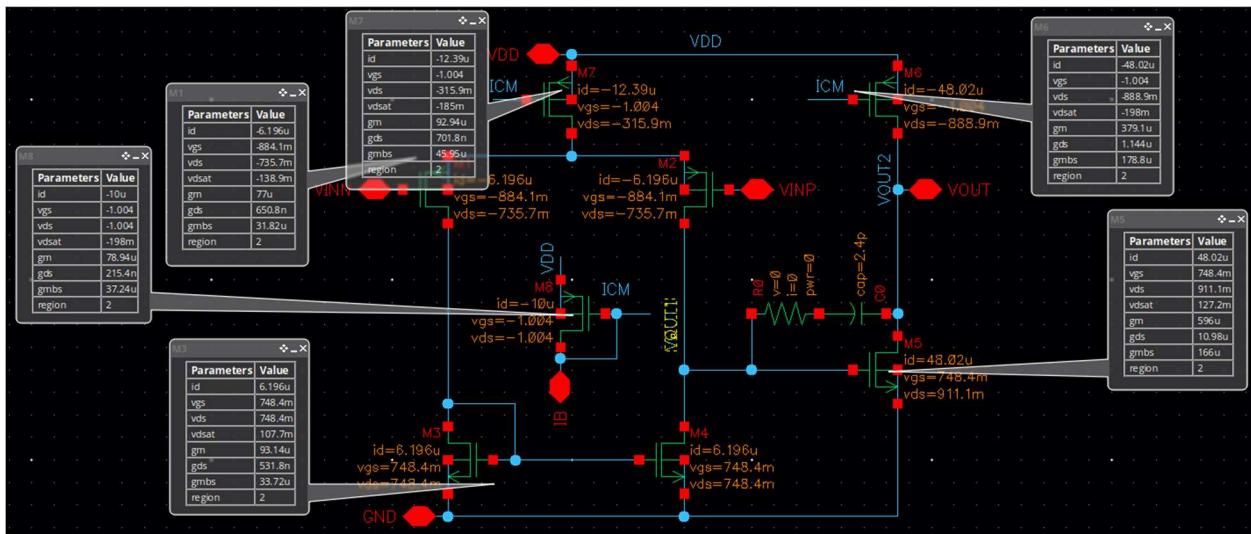
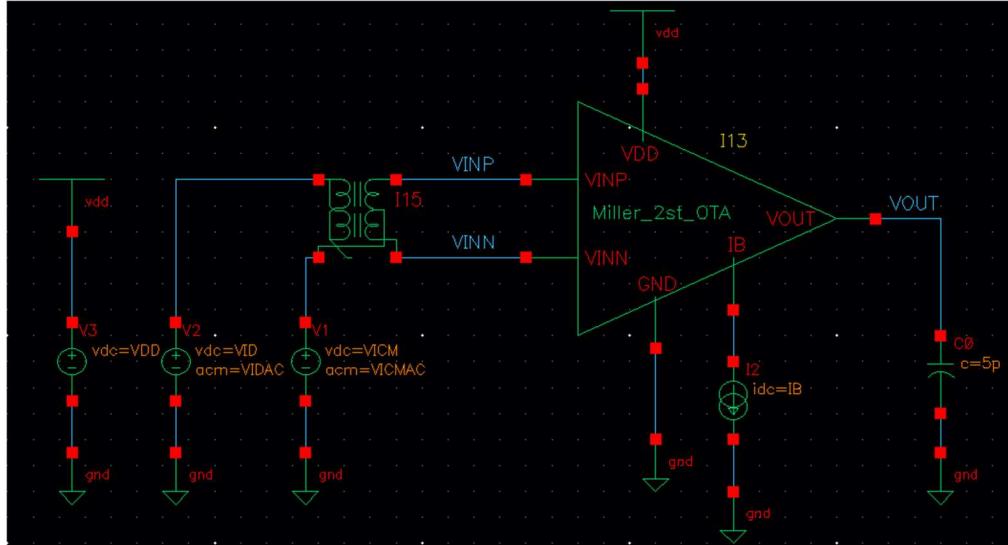
LUT	nmos_03v3
Corner	tt
Temp (°C)	27.0
State1	
Save State	
ID	47.5u
gm/ID	15
gm/gds	52.97
VDS	0.9
VSB	0

1	ID	47.5u	16	gm	691.3u
2	IG	NaN	17	gmb	189.2u
3	L	340n	18	gds	13.65u
4	W	24.82u	19	ro	73.24k
5	VGS	707.6m	20	VTH	673.3m
6	VDS	900m	21	VDSAT	104.2m
7	VSB	0	22	cgg	28.35f
8	gm/ID	14.55	23	cgs	18.73f
9	Vstar	137.4m	24	cgd	4.01f
10	fT	3.881G	25	cgb	5.607f
11	gm/gds	50.63	26	cdb	-321e-18
12	VA	3.479	27	csb	20.49f
13	ID/W	1.914	28	idnth2	7.584e-24
14	gm/W	27.85	29	vgnth2	15.87e-18
15	AREA	8.439p	30	idnfl2	173.4e-18
16	gm	691.3u	31	vgnfl2	362.8p
17	gmb	189.2u	32	cdd	17.08f
18	gds	13.65u	33	idmis	1.488u
19	ro	73.24k	34	vgmis	2.152m

Transistor	gm/ID	Length	Width	Function
M1 and M2	15	390nm	6.9um	Input pair
M3 and M4	15	540nm	5.01um	Current mirror load
M6	12	320nm	24.66um	current mirror-tail Common-source,1
M7	12	430nm	14.03um	Current mirror, St1
M8	12	320nm	7.3um	Current mirror-tail
M5	12	340nm	24.82um	Common-source 2



PART 3: Open-Loop OTA Simulation



1) Schematic of the OTA and bias circuit with DC node voltages clearly annotated.

Is the current (and gm) in the input pair exactly equal? >>> yes

What is DC voltage at the output of the first stage? Why?

Is $747.7\text{mV} = \text{vds to load} = \text{vgs to Common-source 2}$

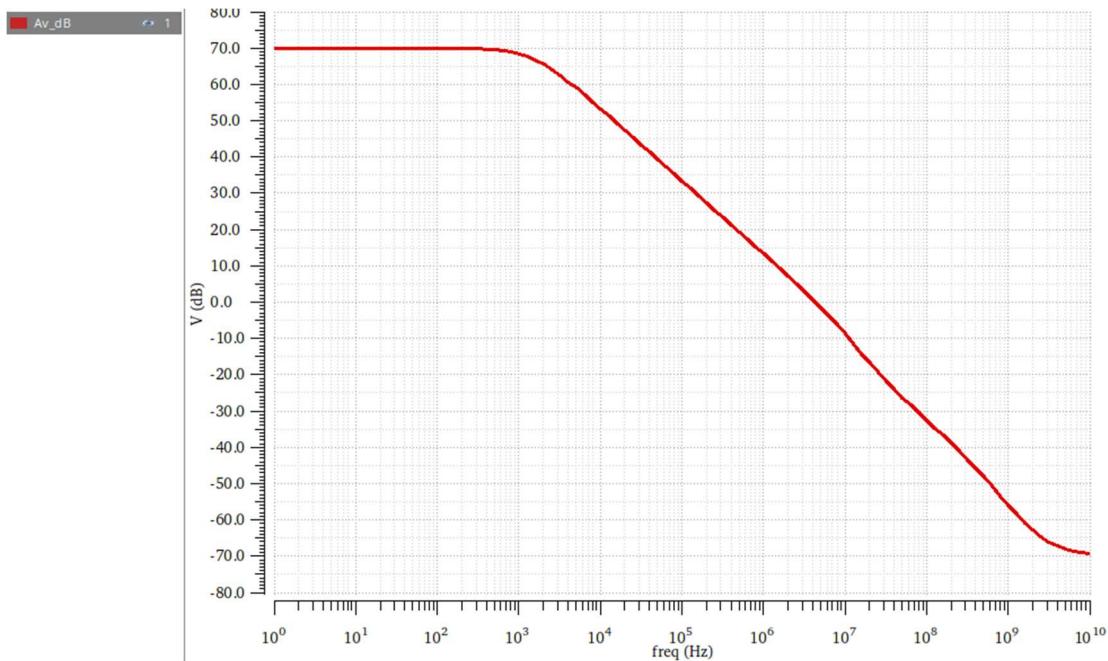
What is DC voltage at the output of the second stage? Why?

Is $911\text{mV} = \text{vgs to Common-source 2}$

Almost $\text{VDD}/2$ as expected from design.

1) Diff small signal ccs:

Plot diff gain (in dB) vs frequency.



Compare simulation results with hand calculations in a table.

Av_dB	
Ao	3.277k
Ao_dB	70.31
BW	1.456k
fn	4.504M
GBW	4.773M

$$AvOL = Av1 * Av2 = gm1 * (ro1|ro3) * gm6 * (ro6|ro5) = 3.32k$$

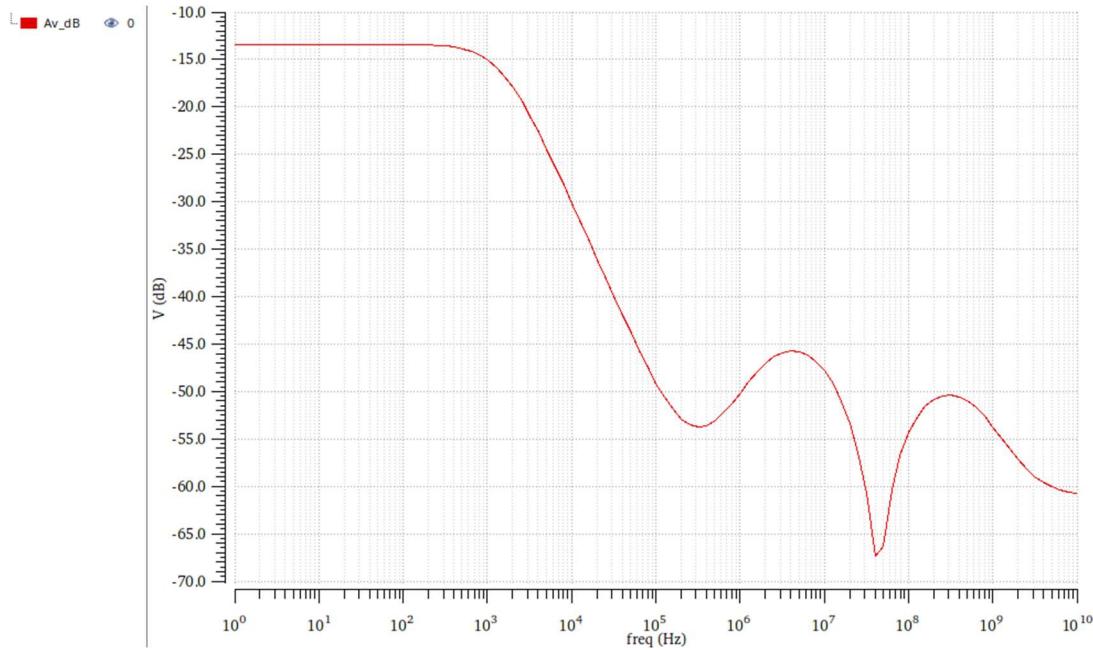
$$BW = 1/(2\pi R_{out1} * (1+Av2) CC) = 1.51k$$

$$GBW = UGF = AvOL * BW = 4.87M$$

	Analytically	simulation
DC Gain	3.32k	3.27k
BW	1.51k	1.45k
GBW	4.87M	4.77M

2) CM small signal ccs:

Plot CM gain in dB vs frequency.



Compare simulation results with hand calculations in a table.

Av_dB	
Ao	216.6m
Ao_dB	-13.29
BW	1.456k
fn	eval err
GBW	315.5

$$Fn \rightarrow \text{UGF IS Undefined when the DC gain is already } < 1$$

$$AvCM \approx 1/(2*gm3ro7) * Av2 = 216.5m$$

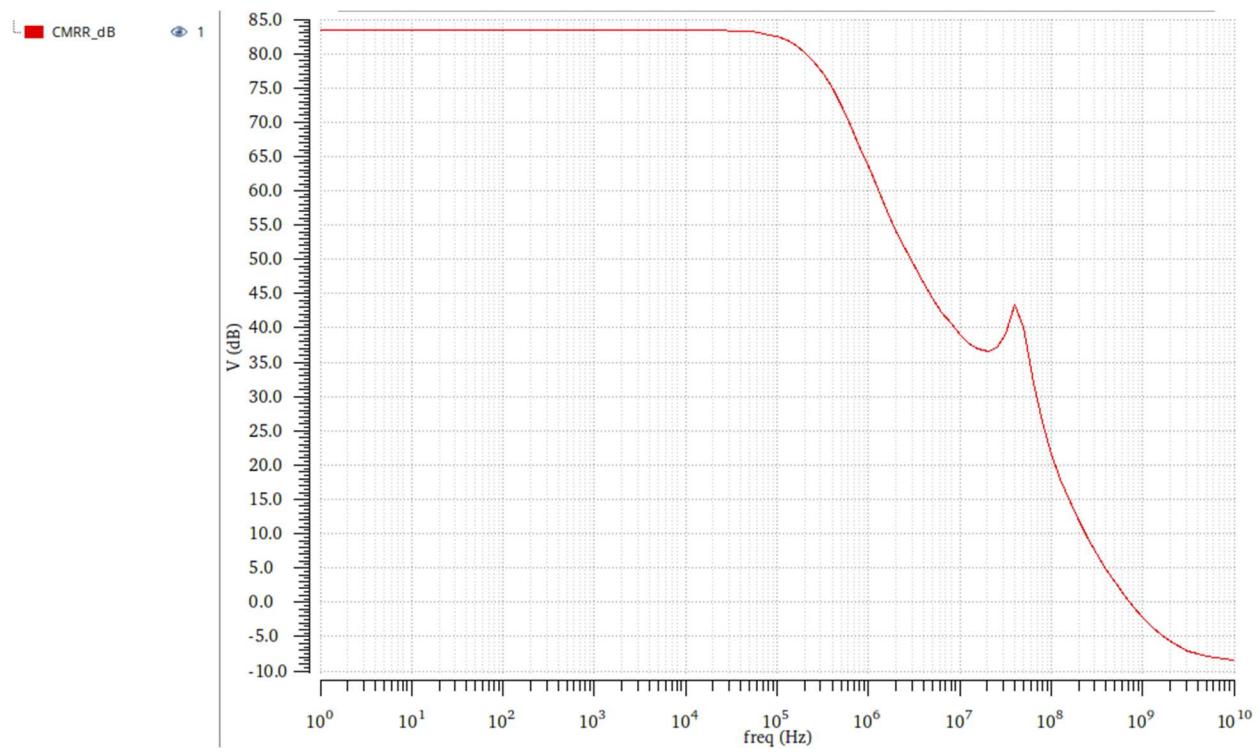
$$BW = 1/(2\pi R_{out1} * (1+Av2) CC) = 1.51k$$

$$GBW = AvCM * BW = 315.68$$

	Analytically	simulation
DC Gain	6.82	216.6m
BW	318.1	1.456k
GBW	315.68	315.5

(Optional) CMRR.

Plot CMRR in dB vs frequency.



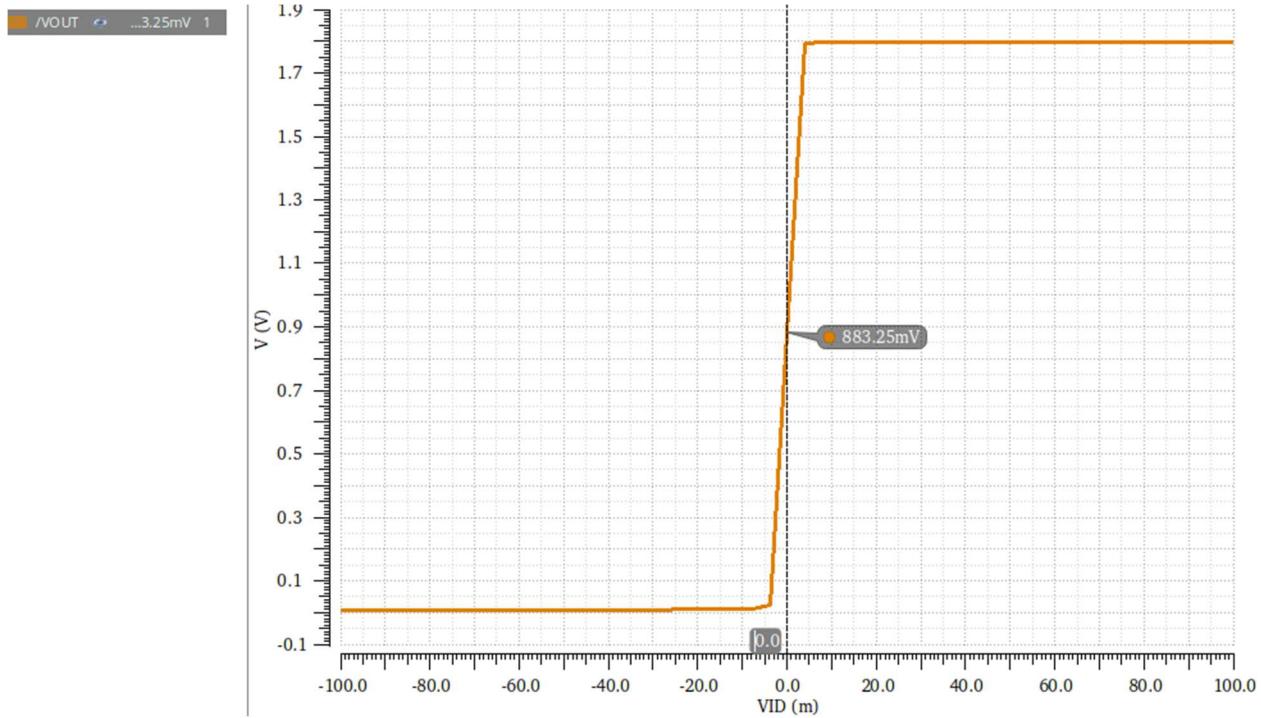
Compare simulation results with hand calculations in a table.

Avd_dB	
Avd	70.31
AvCM_dB	
AvCM	-13.29
CMRR_dB	
CMRR	83.6

$$CMRR \text{ in } dB = Avd \text{ in } dB - AvCM \text{ in } dB = 83.6 \text{ dB}$$

	Analytically	simulation
CMRR	83.6 dB	83.6 dB

(Optional) Diff large signal ccs:

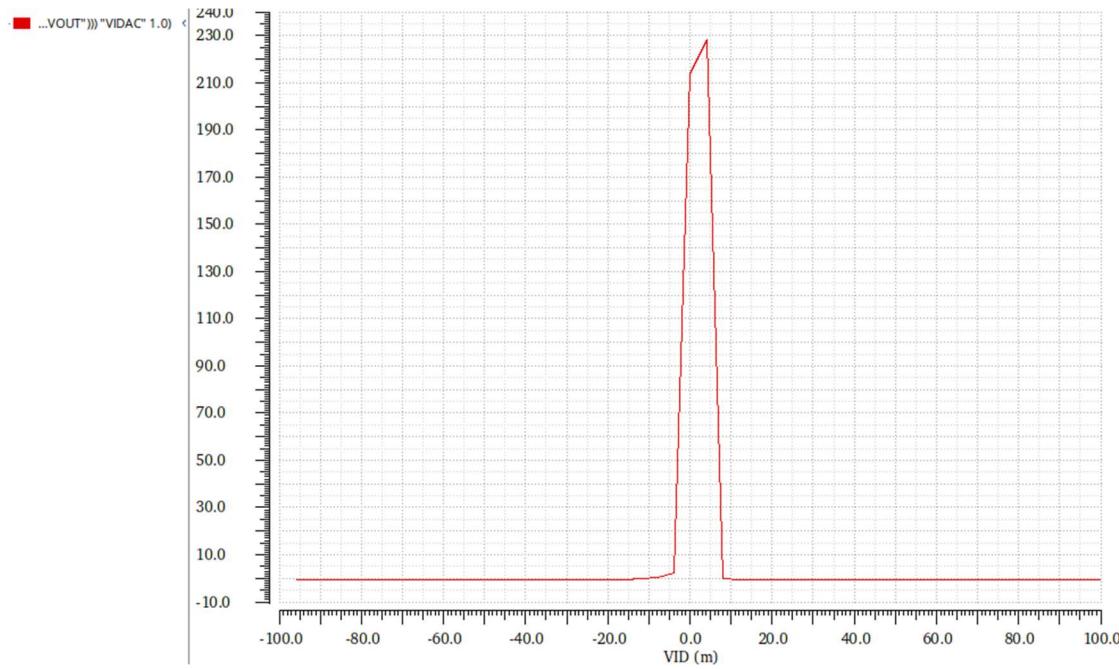


From the plot, what is the value of V_{out} at $VID = 0$. Compare it with the value you obtained in DC OP.

From the plot at $VID = 0$ we got $V_{out} = 883.25\text{ mV}$

while the value obtained in DC OP was 911.1 mV

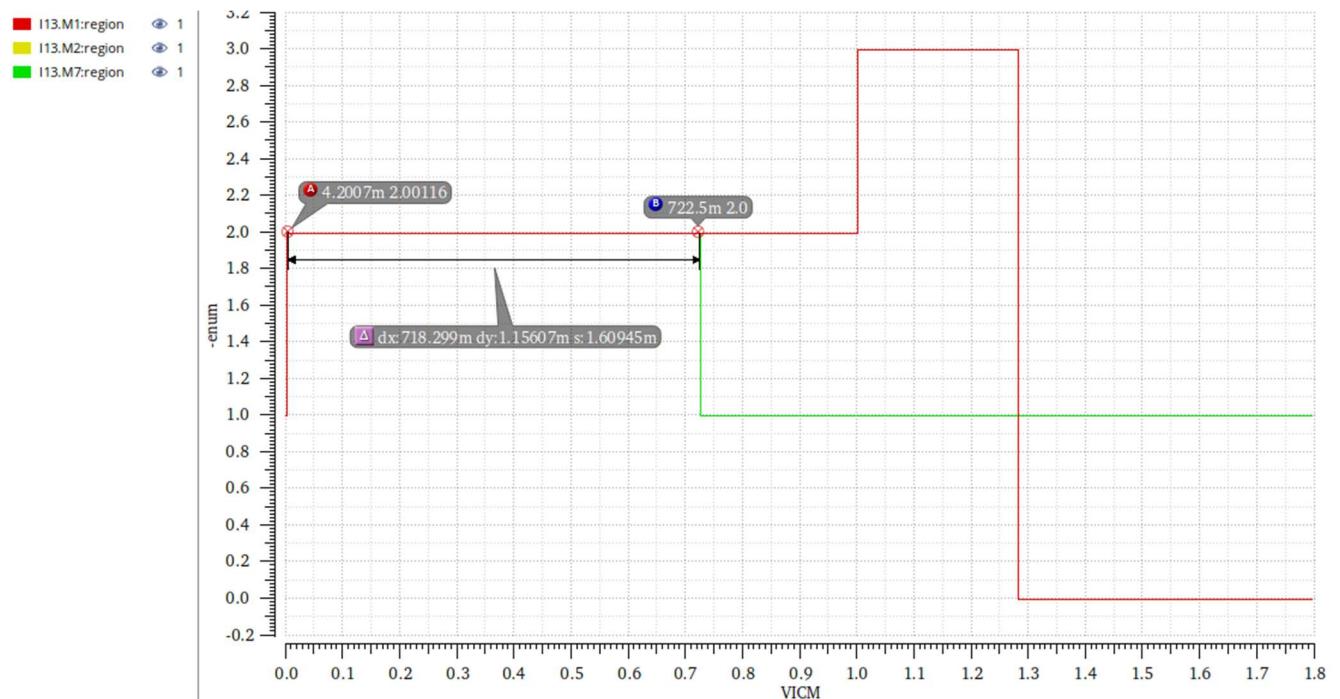
Plot the derivative of VOUT vs VID. Is the peak less than the value of Avd obtained from ac analysis? Why?



/VOUT	
deriv(magVS("VOUT"))	
peak	228.9

3) CM large signal ccs (region vs VICM):

Plot “region” OP parameter vs VICM for the input pair and the tail current source.



Find the CM input range (CMIR). Compare with hand analysis in a table.

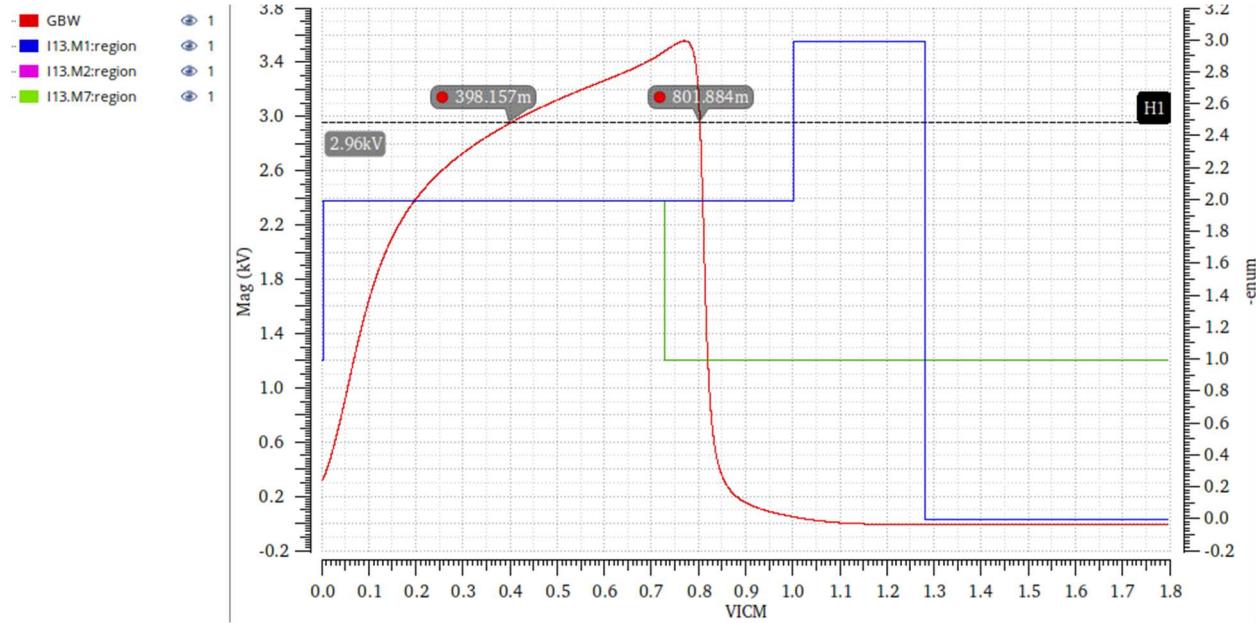
$$CMIR\ High: VICM \leq VDD - |VGS1| - |Vdsat7| = VICM \leq 0.718\ V$$

$$CMIR\ Low: VICM \geq |VGS7| + |Vdsat1| - |VGS1| = VICM \geq 0.0037\ V$$

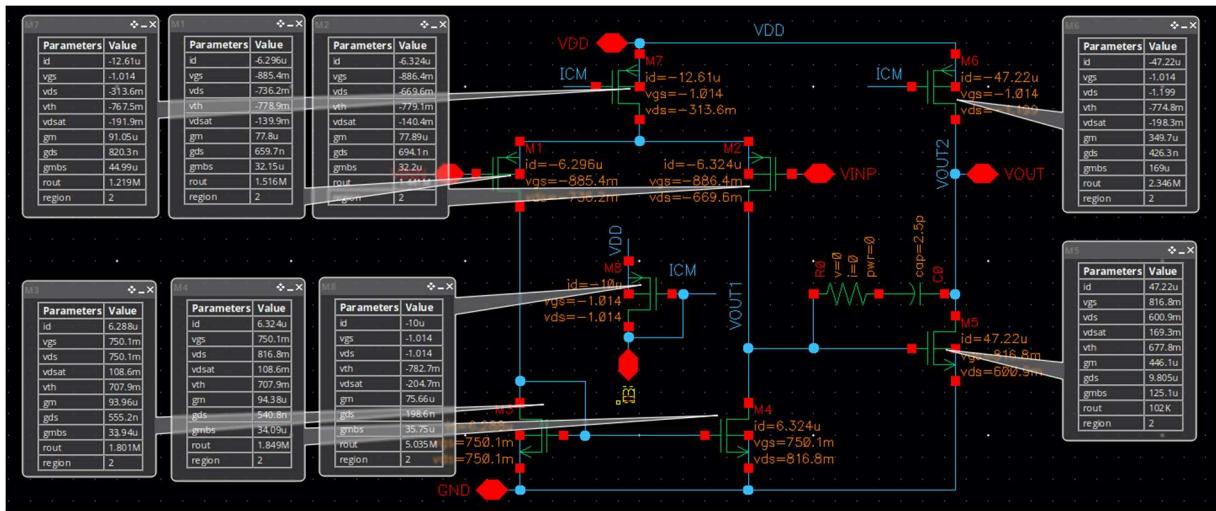
	Analytically	simulation
CMIR	3.7m to 718m	4.2m to 722m

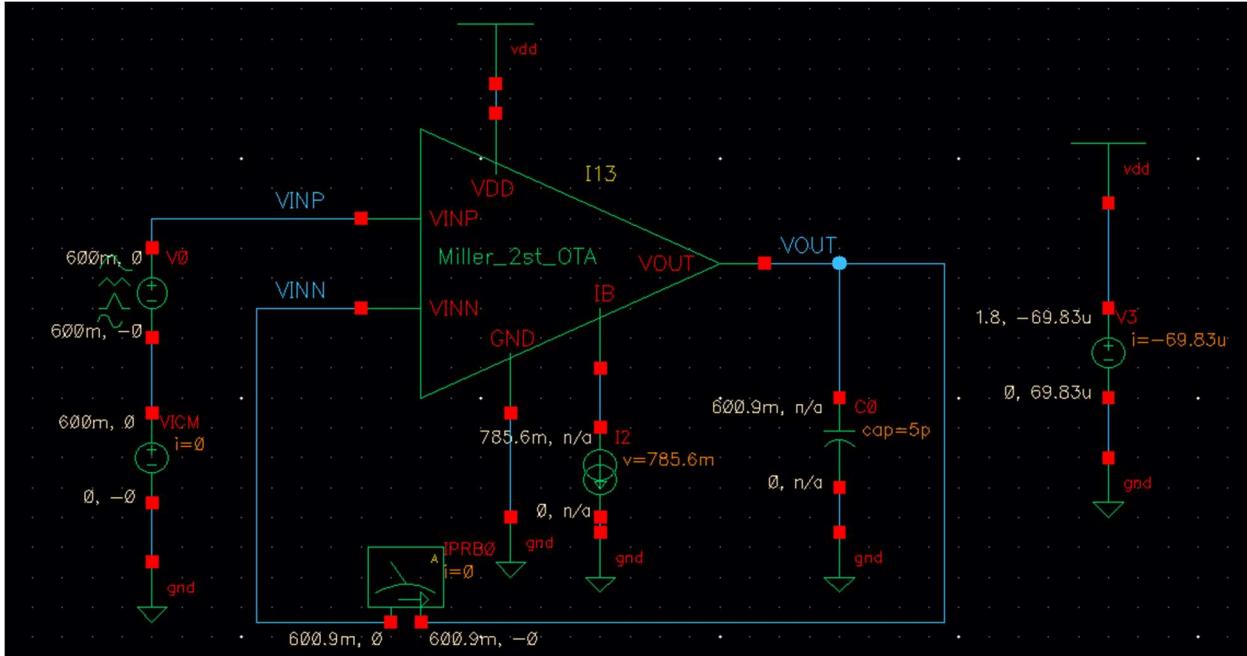
(Optional) CM large signal ccs (GBW vs VICM):

Plot GBW vs VICM. Plot the results overlaid on the results of the previous method (region parameter).



PART 4: Closed-Loop OTA Simulation





Are the DC voltages at the input terminals of the op-amp exactly equal? Why?

No, as the OTA there is a feedback loop.

which creates a differential signal → error signal between the input of the OTA which introduces mismatch between the input voltages.

M1		M2	
Parameters	Value	Parameters	Value
id	-6.296u	id	-6.324u
vgs	-885.4m	vgs	-886.4m
vds	-736.2m	vds	-669.6m
vth	-778.9m	vth	-779.1m
vdsat	-139.9m	vdsat	-140.4m
gm	77.8u	gm	77.89u
gds	659.7n	gds	694.1n
gmbs	32.15u	gmbs	32.2u
rout	1.516M	rout	1.441M
region	2	region	2

Is the DC voltage at the output of the first stage exactly equal to the value in the open-loop simulation? Why?

No, V_{out2} is connected to the inverting input of the OTA.

And the V_{out1} following V_{out2} → as the $V_{out2} = V_{out1} * A_v$

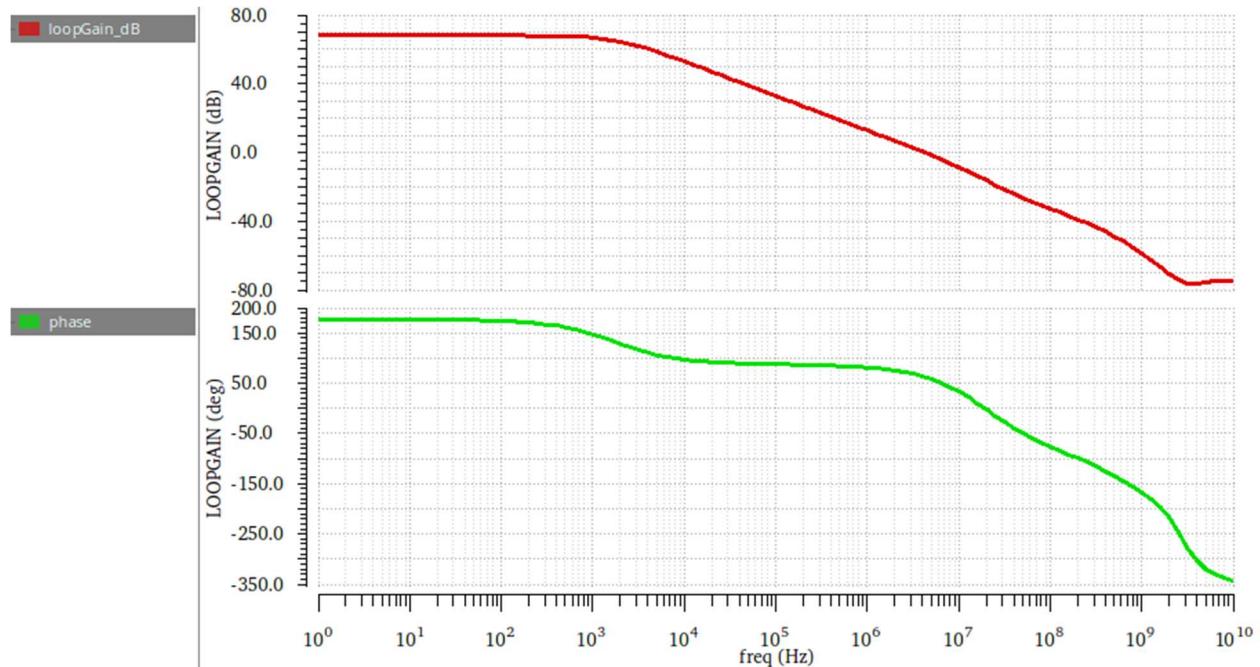
So, the mirror node anymore and will deviate from its common mode level and that's why its value is changed from the value of the open-loop simulation.

Is the current (and gm) in the input pair exactly equal? Why?

No, → there's an error signal at the input of the OTA → which makes the circuit asymmetric and introduces mismatch.

Loop gain:

Plot loop gain in dB and phase vs frequency.



Compare DC gain, fu, and GBW with those obtained from open-loop simulation. Comment

phase	
L_G_Av	2.745k
L_G_BW	1.743k
L_G_UGF	4.647M
L_G_GBW	4.797M

	Loop gain	Open loop
DC Gain	2.74k	3.27k
BW	1.74k	1.45k
UGF	4.647M	4.50M
GBW	4.79M	4.77M

$$\text{Static Gain Error} = 1 / LG = 4.6429 \times 10^4$$

Report PM. Compare with hand calculations. Comment

$$PM = 90^\circ - \tan^{-1}(\omega u / \omega pnd)$$

$$\omega u = CM1/cc \quad \omega pnd = CM2/cl$$

$$\omega u / \omega pnd = gm1 / gm5 * CL/CC = 74.4$$

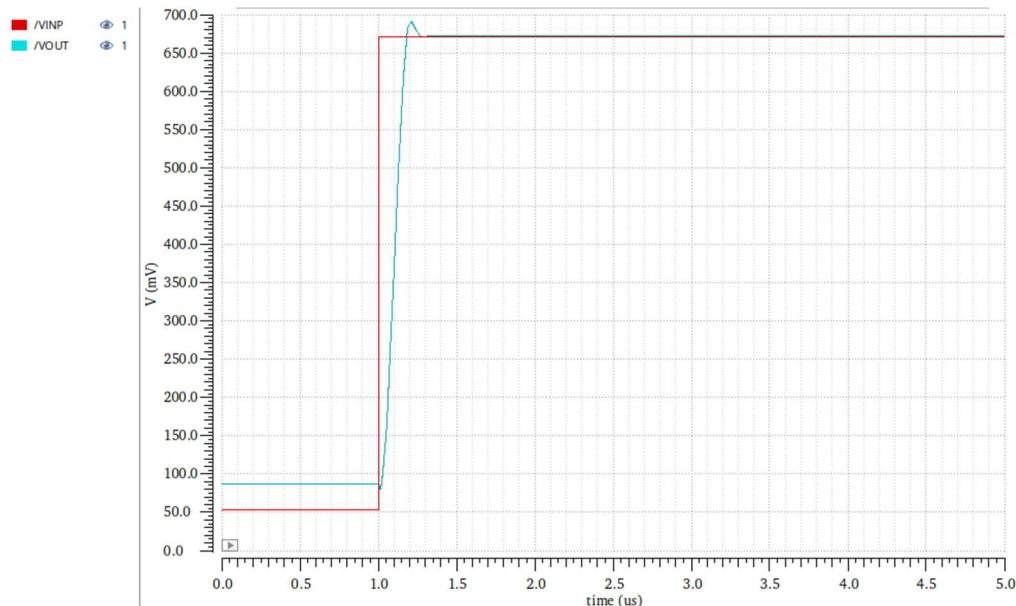
1	L_G_Phase_M	75.1
---	-------------	------

	Analytically	simulation
PM	74.4	75.1

The system has fastest possible response

3) Slew rate:

Report Vin and Vout overlaid.



$$\text{Slew Rate} = IB1/CC = 12.6\mu/2.5p = 5.04 \text{ M}$$

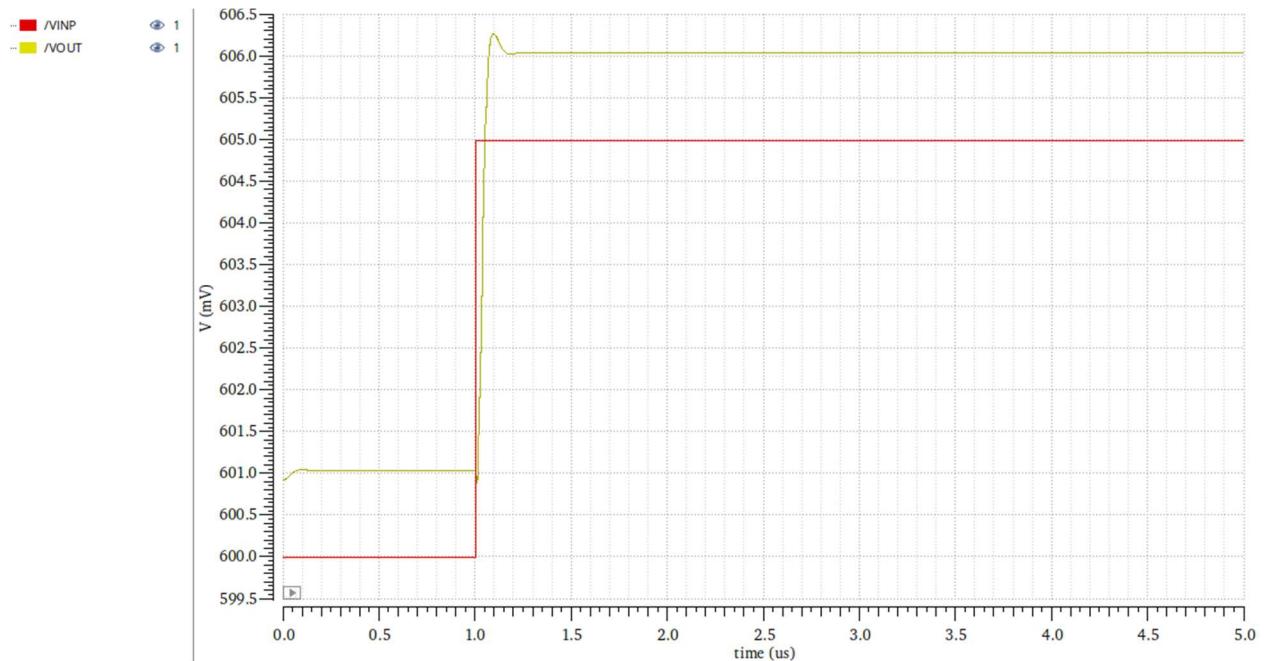
:1	/VOUT	
:1	slew_rate	4.482M

Analytically > simulation → as hand analysis equation is approximated.

can do fine tuning for Cc capacitor to make the SR meet the design.

	Analytically	simulation
Slew Rate	5.04M	4.482M

Settling time



$$\tau = 1/2\pi \cdot UGF = 24.3\text{n} \quad t_{rise} = 2.2\tau = 65.46\text{n}$$

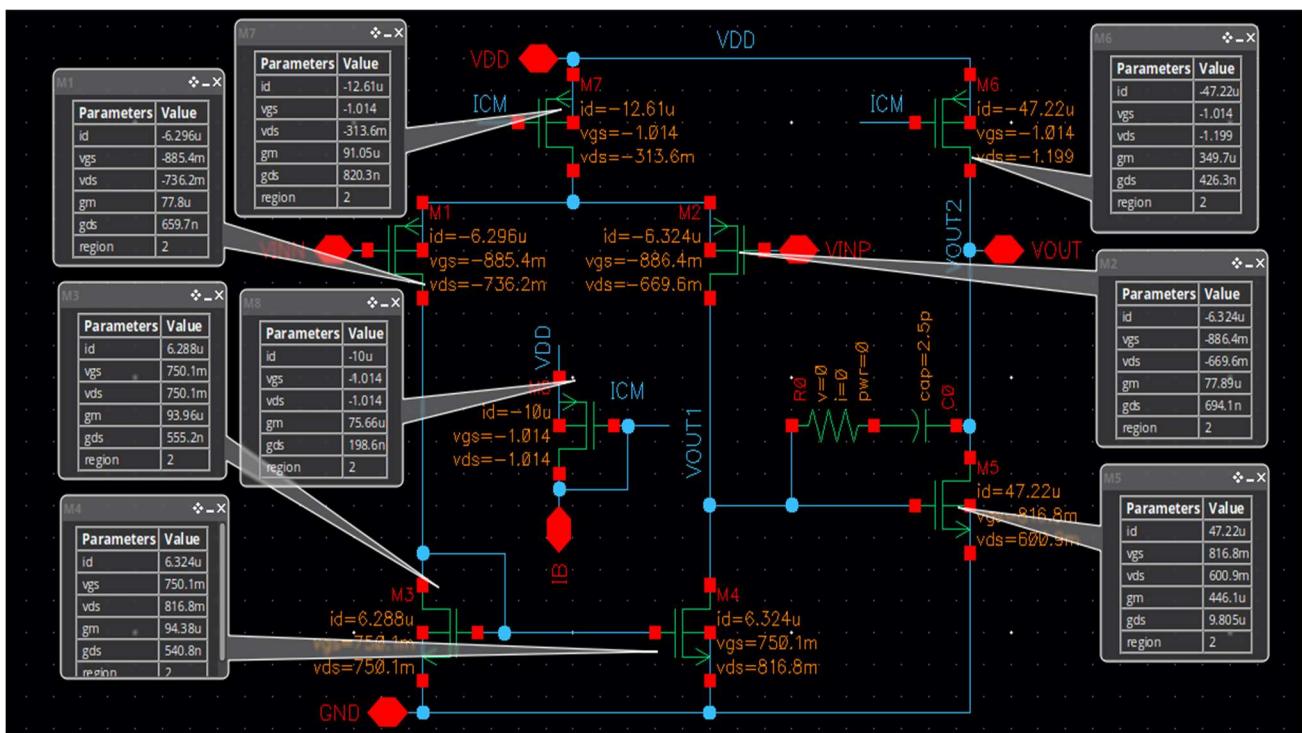
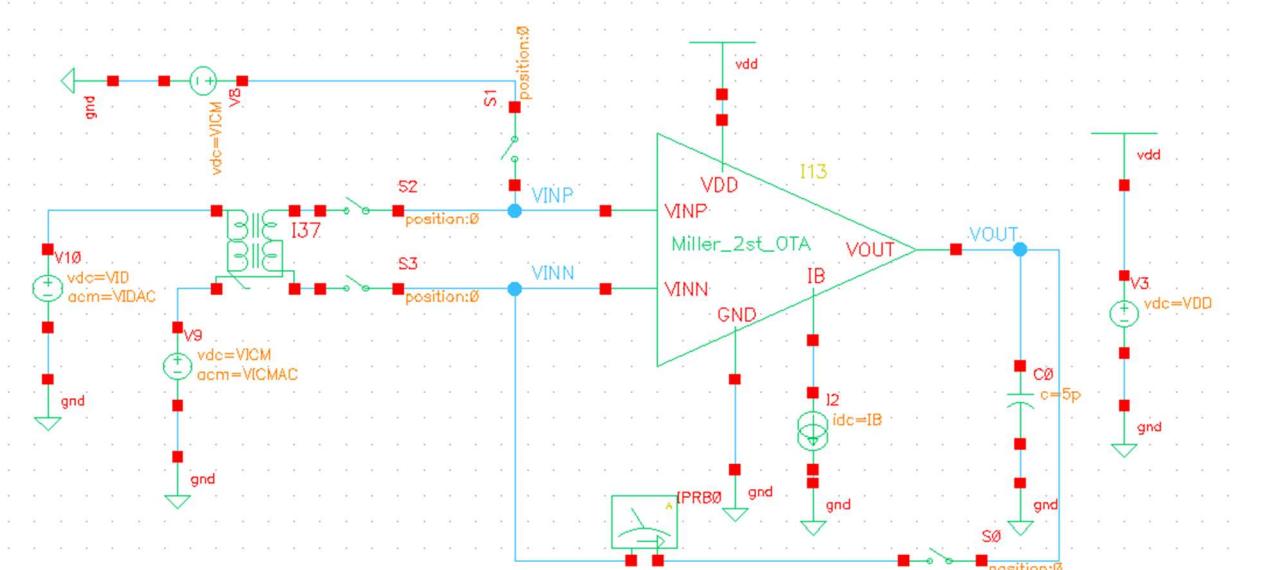
Rise Time 49.76n

	Analytically	simulation
Rise Time	65.46n	49.67n

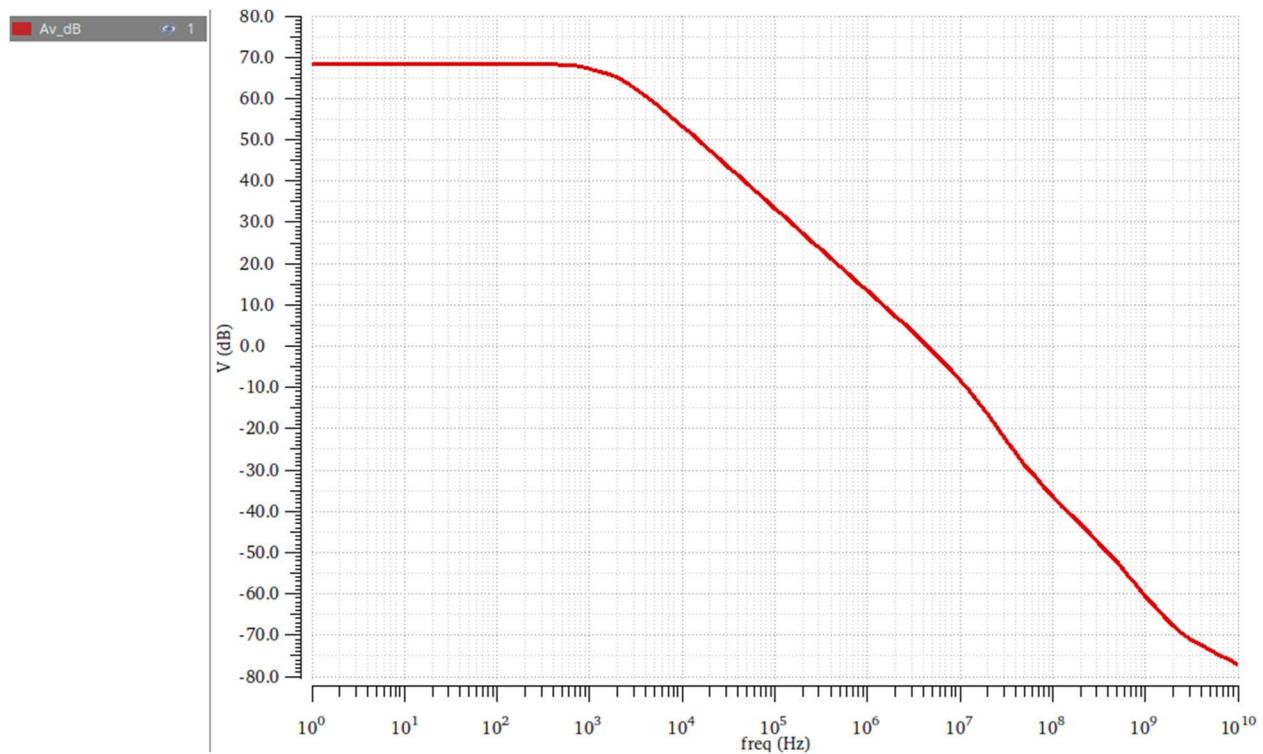
Do you see any ringing? Why?

Yes, there is ringing Very slight, as the Sharpening transition in square signal It is not transmitted ideally in the circuit

Part 5 (optional): DC Closed Loop AC Open-Loop OTA Simulation

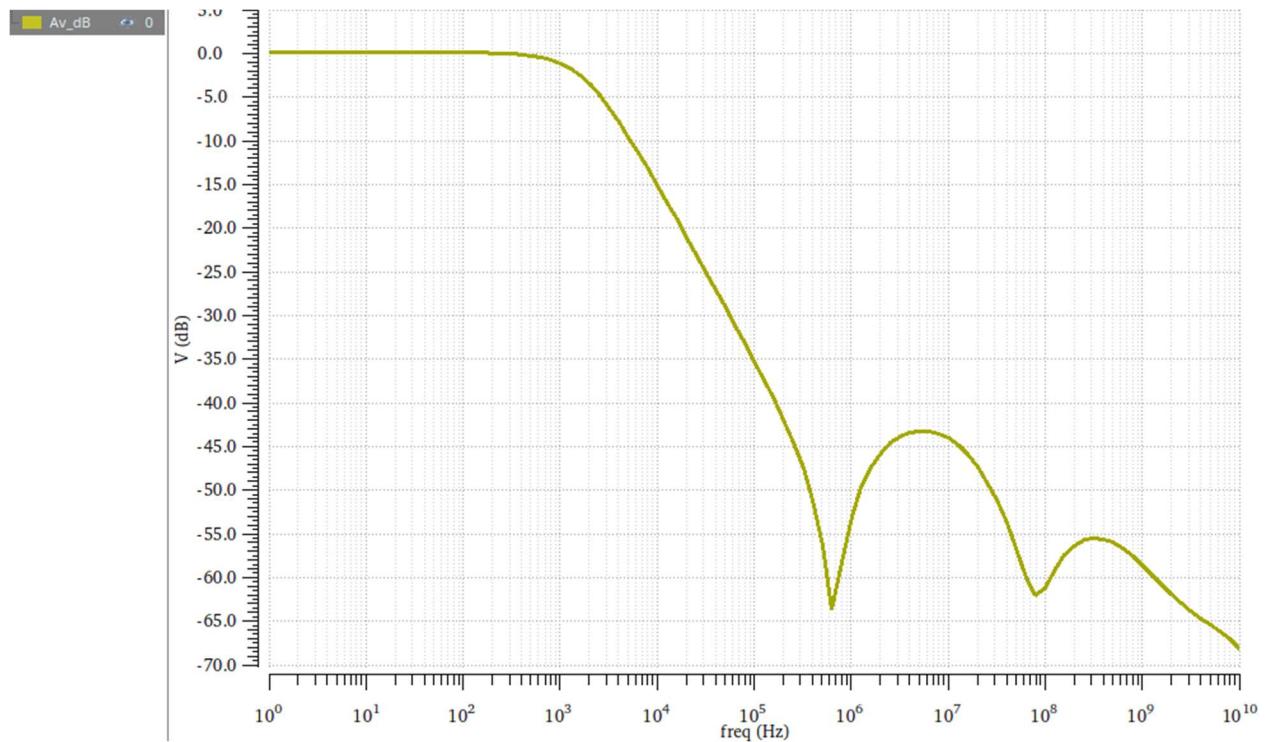


1) Diff small signal ccs:



Av_dB	
Ao	2.745k
Ao_dB	68.77
BW	1.743k
UGF	4.62M

CM small signal ccs:



r:1	Av_dB	
r:1	Ao	1.029
r:1	Ao_dB	244.7m
r:1	BW	1.743k
r:1	UGF	417.7

(Optional) CM large signal ccs (GBW vs VICM)

