Analog IC Design – Cadence Tools
Lab 02
Common Source Amplifier

PART 1: Sizing Chart

1) We would like to design a resistive loaded CS amplifier that meets the specifications below. The design process involves selecting the sizing of the transistor (W and L), the bias point (VGS), and the resistive load (RD).

Design Specs:

DC gain = -10 and ID = 100UA

Supply =VDD= 3 V

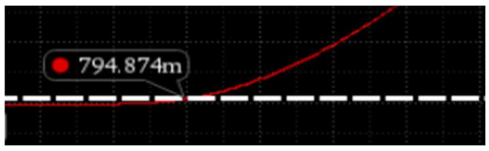
i. L = 2 μm (Because there is no speed limit in the design specification, to avoid short channel effect

ii. AV=gm*RD =2V*RD / Vov gm= 2ID/Vov This shows that the reinforcement does not depend on RD itself, but on the voltage drop across it.

iii. Formula gm= 2ID/Vov Applies only to devices that obey the square law This is not true for real MOSFETs

iv. Av= 2VRD /V' and Av and VRD are known, we can determine the required V' value as follows: According to the design specification, Av = -10 and VRD is selected as To be VDD/2 = 3/2= 1.5 , V' = 2*1.5/10 =0.3V

v. We use W =3u L = 300n VDS = 1.5 V and make a sweep for VGS from 0 to 1.5V with 10 mV steps and plot the ID, VGS.

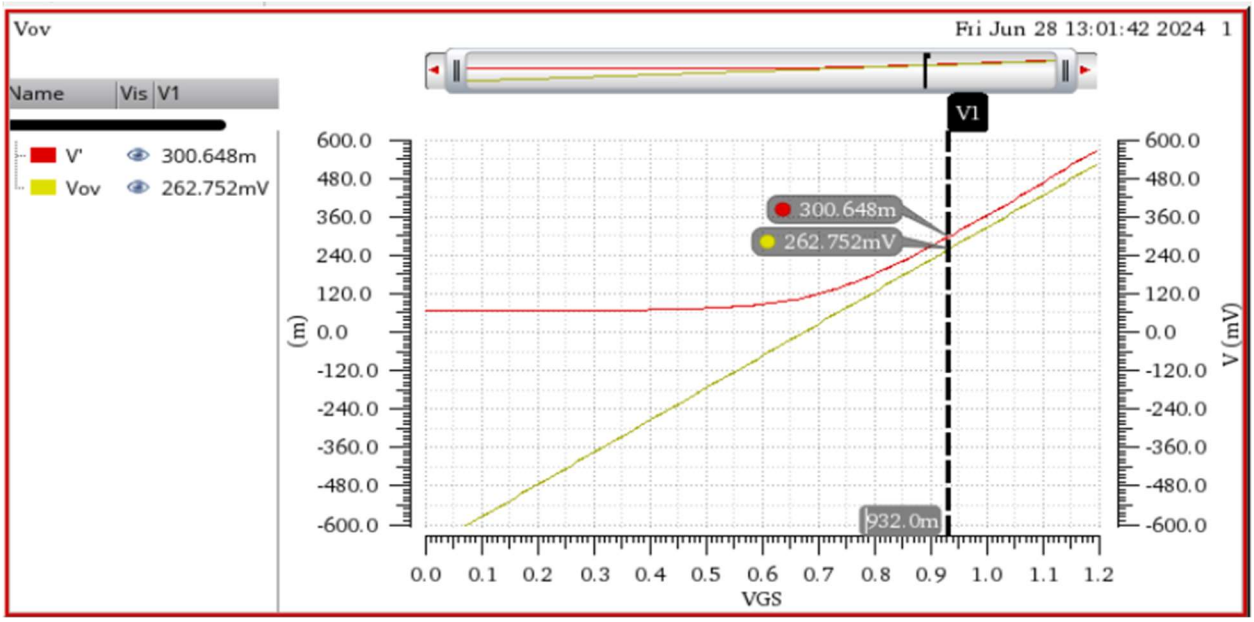
vi. Vth = 

0.794v >>> sweep VGS 0:(0.4+0.794) >>0:1.194.

calculated from actual simulation data using the formula.

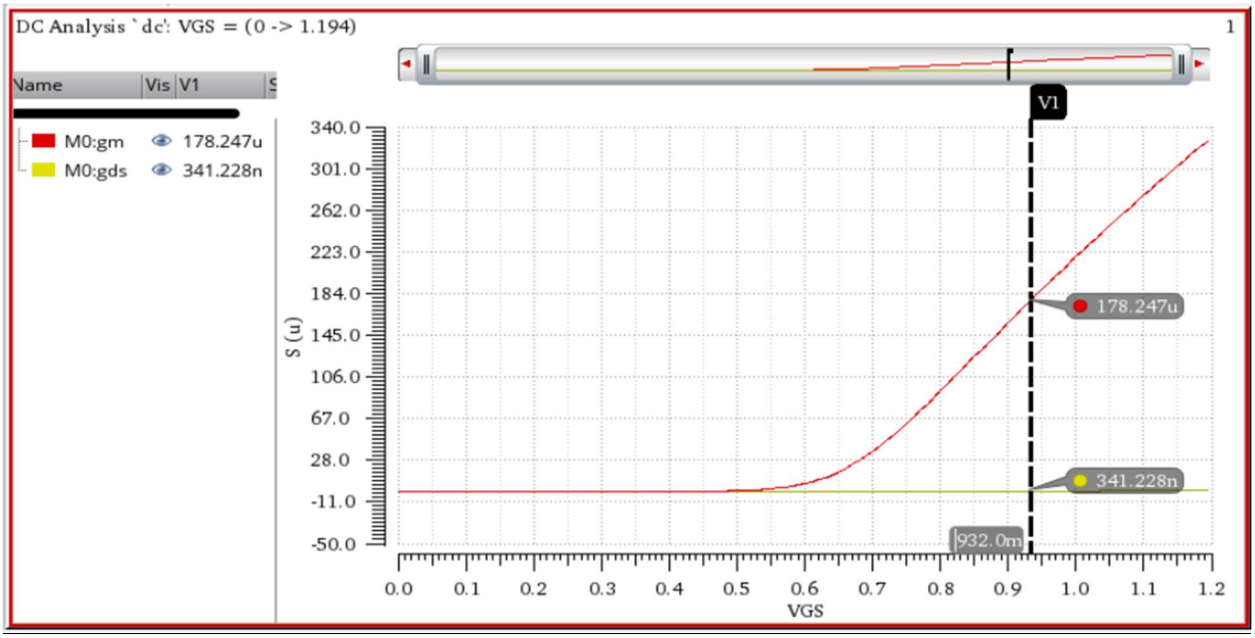
V' =2*ID /gm Vov = VGS-Vth get by the calculator and plot the waveforms

Name	Type	Details
V'	expr	((getData("M0:id" ?result "dc") * 2) / getData("M0:gm" ?result "dc"))
Vov	expr	(v("M0:vgs" ?result "dc") - v("M0:vth" ?result "dc"))

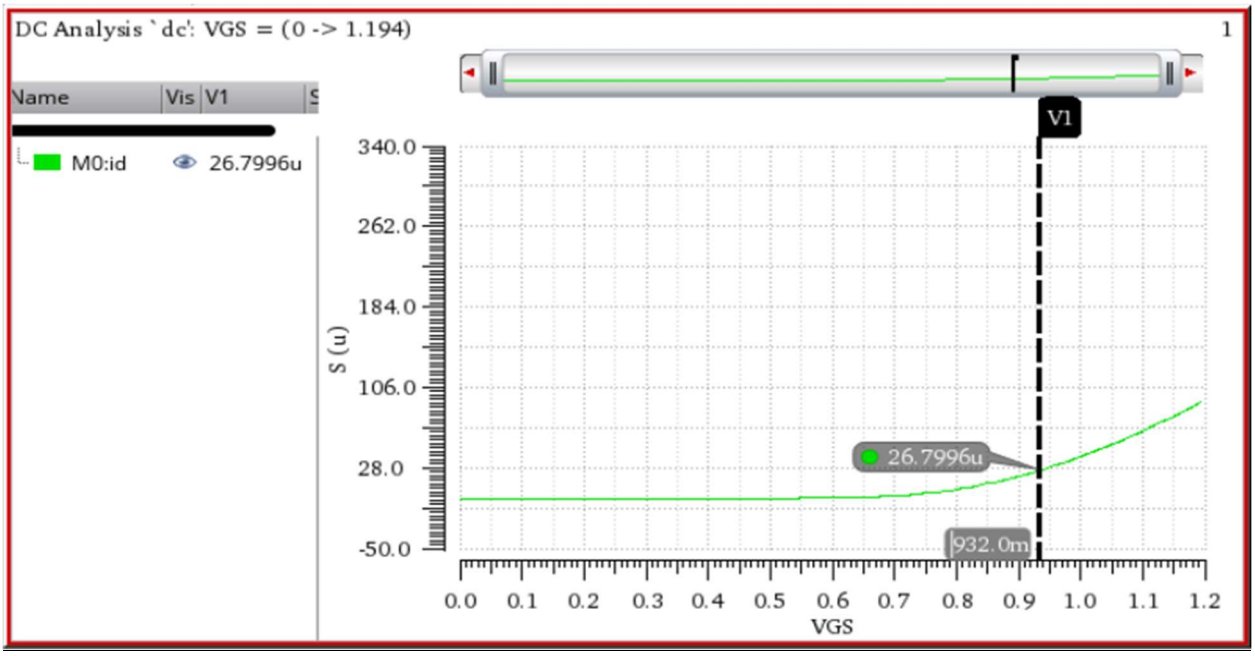


When VGS =932m Vov=262.752mV

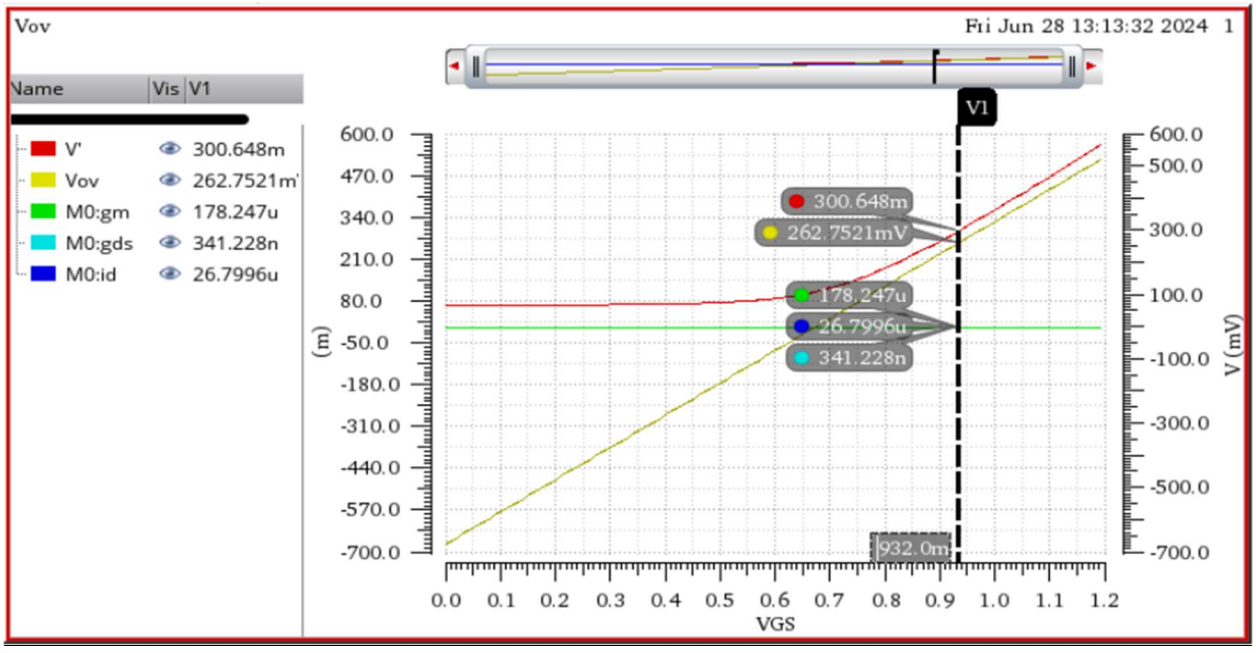
Plot the gm & gds and carse in the VGS =932m



And ID with VGS



Valio all



ID∝ (L&W) can used get the w

ID =IDQ/IDX = (W/L) Q/(W/L) X >>> LQ=LX ID=IDQ/IDX =WQ/WX

>>> WQ= (100u/26.799u) *3u = 11.19um

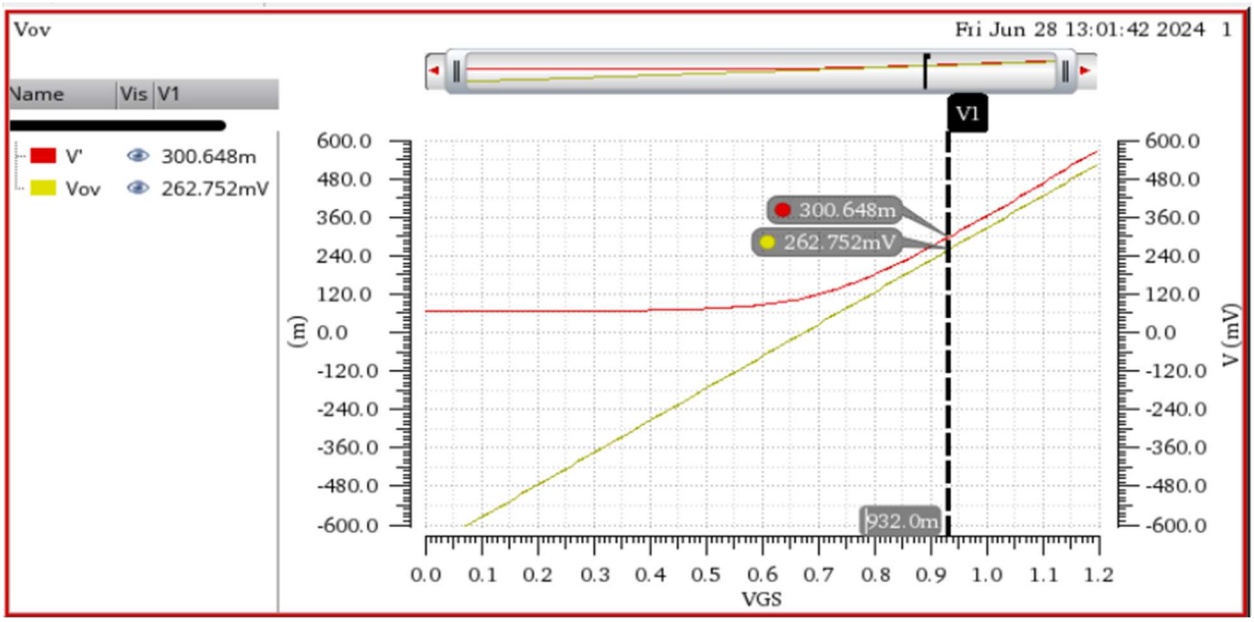
Use W = 10μm (we will understand why shortly)

>>> WQ= (100u/26.799u) *10u = 37.3148um

And gm

gm =(100u/26.799u) *178.247u =665.125u

Plot $V*$ and Vov overlaid vs VGS. Make sure the y-axis of both curves has the same range.



VRD =VDD/2 =3/2=1.5 IDQ =100uA

RD = VRD/IDQ = 1.5/100*10^-6 = 15KΩ

ro= 1/gds = 1/ (314.228*10^-9) =1.9305MΩ

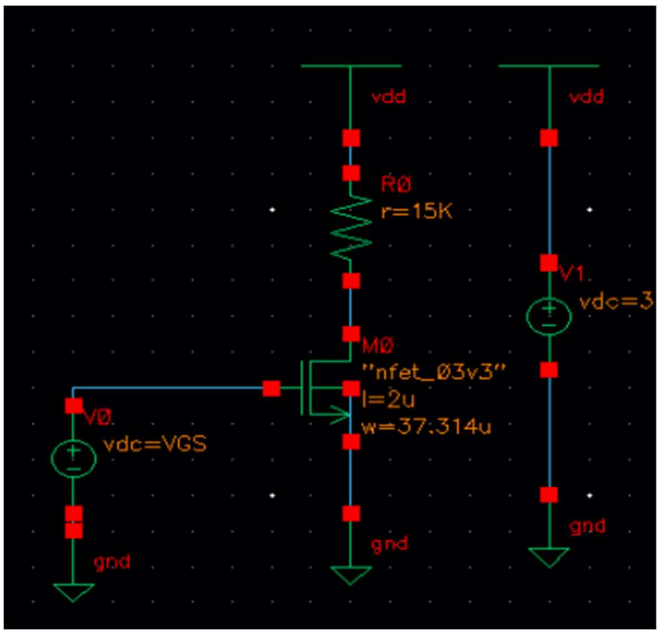
Av= -gm*(RD|| ro) = -665.125u *($\frac{RD*ro}{RD+ro}$) = -9.97 >> The error = $\frac{10-9.97}{10}$ = 0.3 %

W	37.3148um	ro	1.9305MΩ
L	2u m	RD	15KΩ
VGS	932mv	gm	665.125u
IDQ	100uA	Vov	262.752mV
ID	26.799u	Vth	794.874m
AV	-9.97	V’	300mv

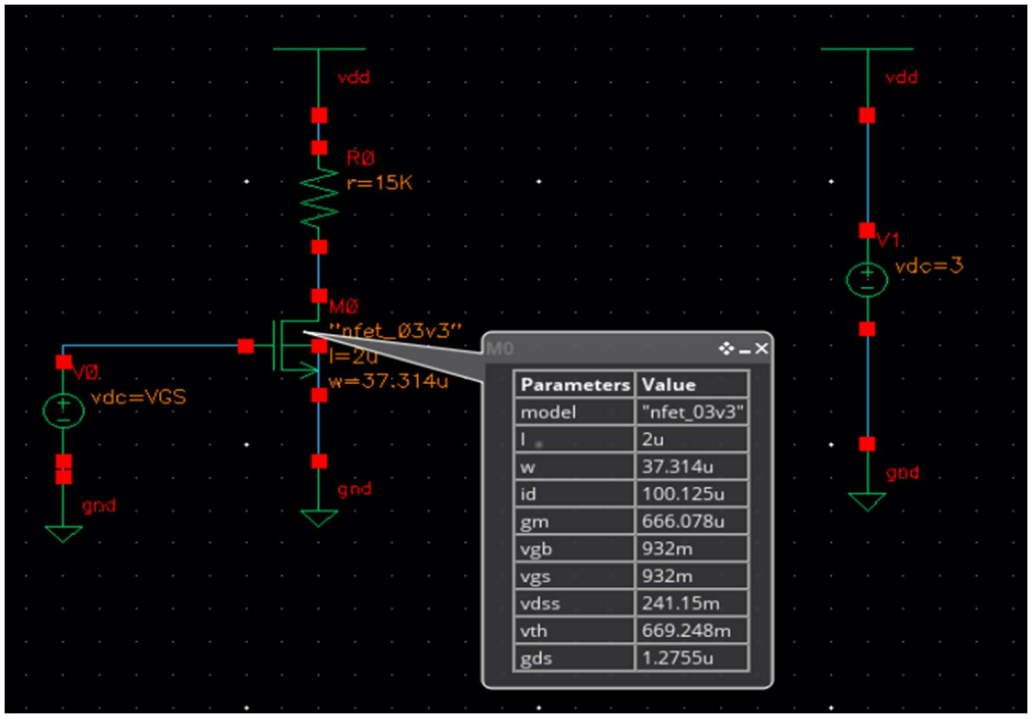
PART 2: CS Amplifier

1. OP and AC Analysis

1) Create a testbench for the resistive loaded CS amplifier using the V_{GSQ}, R_D, L, and W that you got from the previous part.



2) Simulate the DC OP. Report a snapshot for the key operating point (OP) parameters. Compare the results with the results you obtained in Part 1.



3) Compare r_o and R_D. Is the assumption of ignoring r_o justified in this case? Do you expect the error to remain the same if we use min L?

RD is small compared to ro Parallel combinations dominate (ro||RD)
We should neglect the ro.
If we use the minimum L, we might encounter short channel effects that become more pronounced.
ID /VDS =1/ro which means ro decreases, causing the error from neglecting ro to become larger.

4) Calculate the intrinsic gain of the transistor

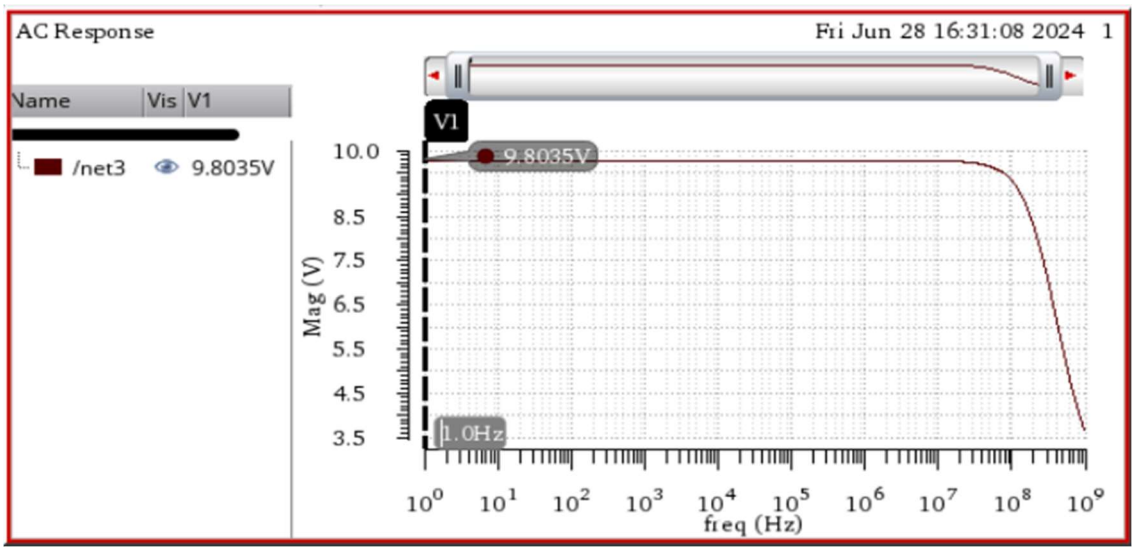
intrinsic gain = ro*gm = (1.93*10^6) *(666*10*-6) =1285.38

5) Calculate the amplifier gain analytically. What is the relation (≪, <, ≈, >, ≫) between the amplifier gain and the intrinsic gain?

Gain of the amplifier $|Av| = gm(RD||ro) =$ 665.125u *$(\frac{RD*ro}{RD+r})$ = 9.97

Gain of the amplifier << intrinsic gain.

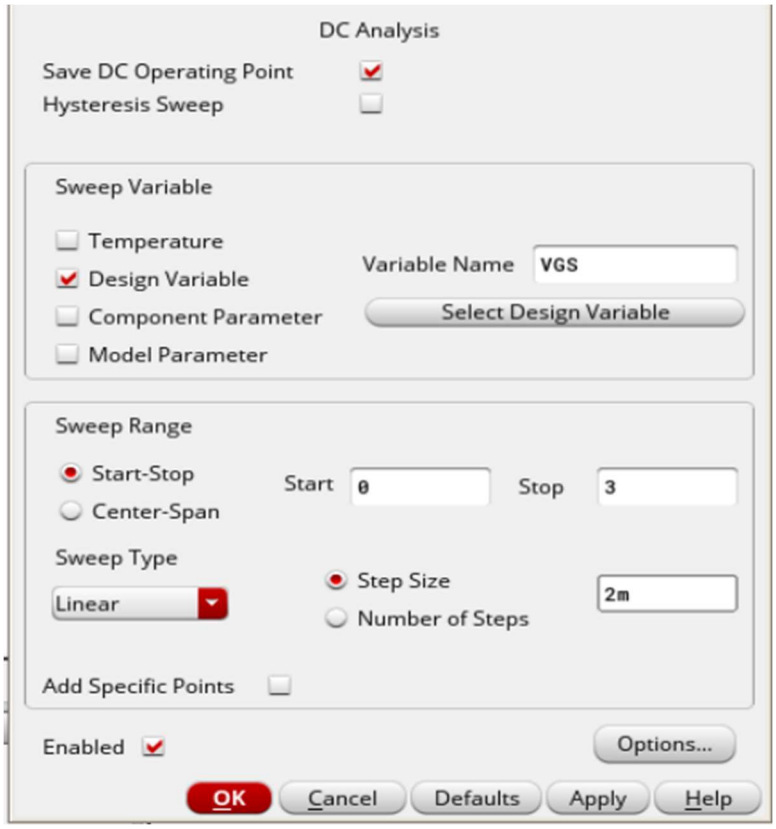
6) Create a new simulation configuration and run AC analysis (from 1Hz to 1GHz). Report the gain vs. frequency. Annotate the DC gain and make sure it meets the spec.



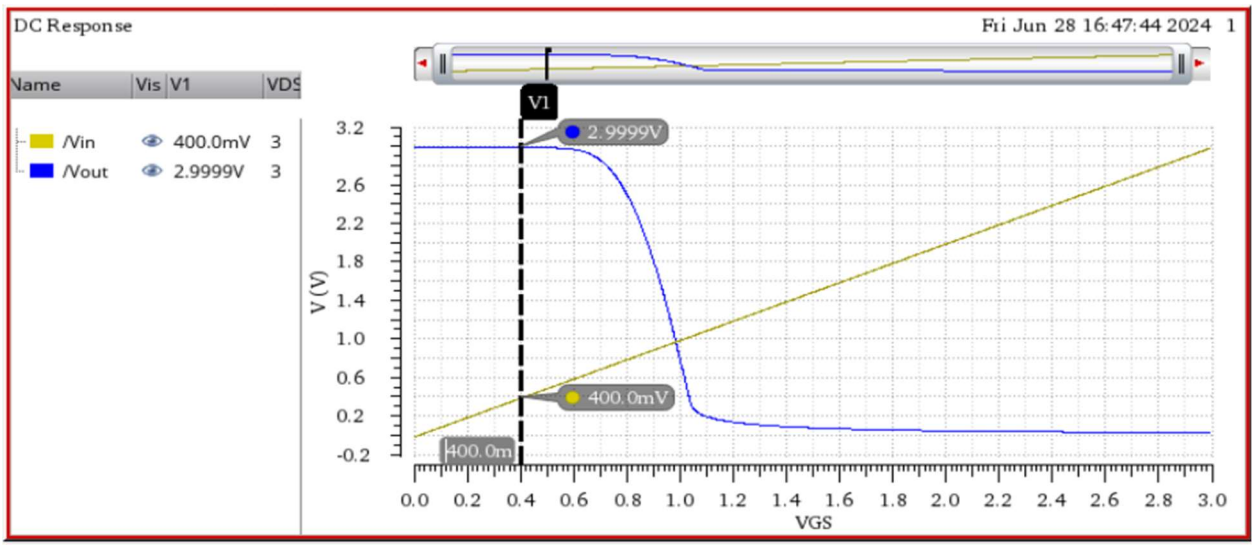
Gain is 9.8 the plot of the gain = gain DC gain The DC Gain is indicated to be 9.97 which matches the expected value

2. Gain Non-Linearity

1) Create a new simulation configuration. Perform a DC sweep for the input voltage from 0 to VDD with 2mV step

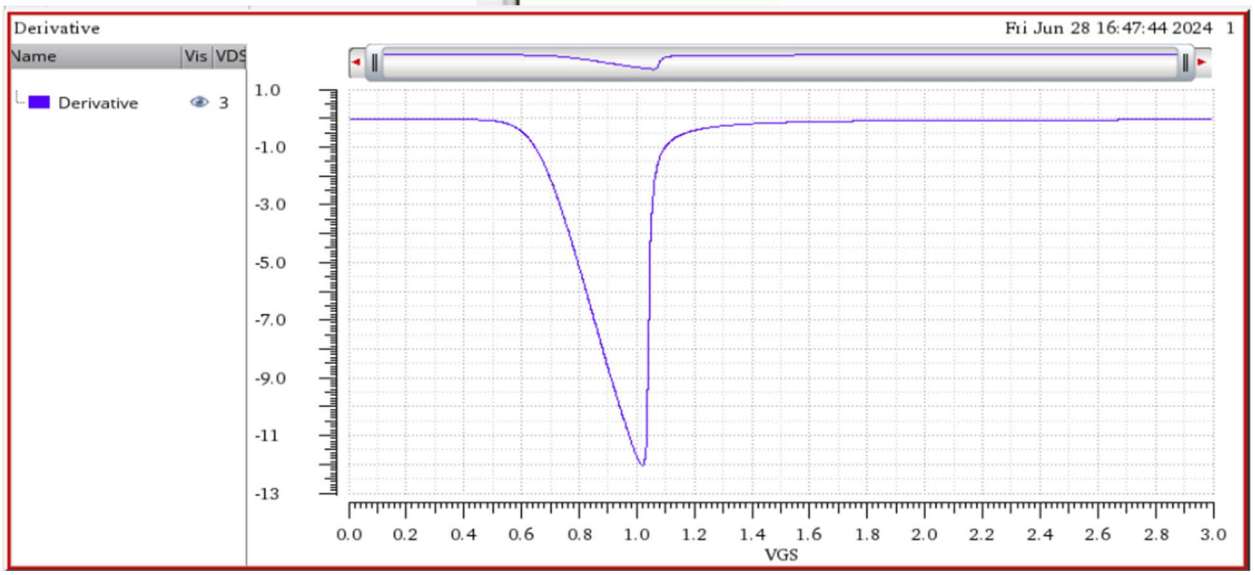


2- Report VOUT vs VIN. Is the relation linear? Why?

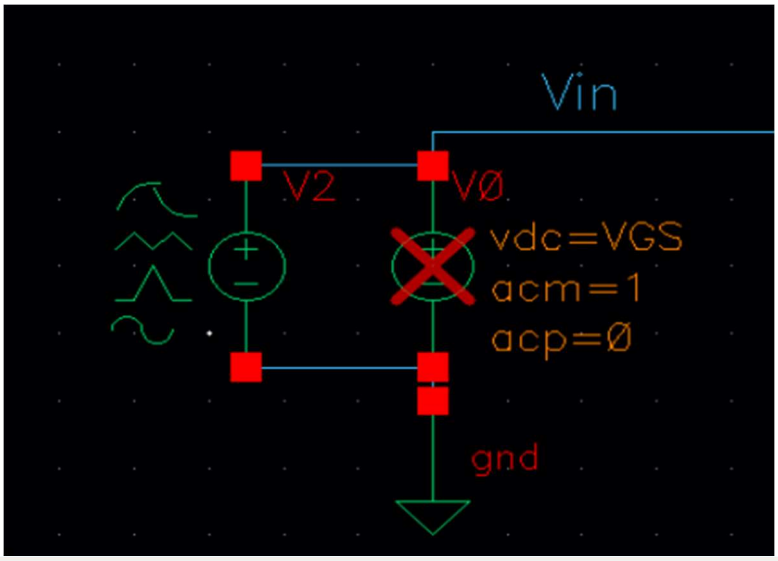


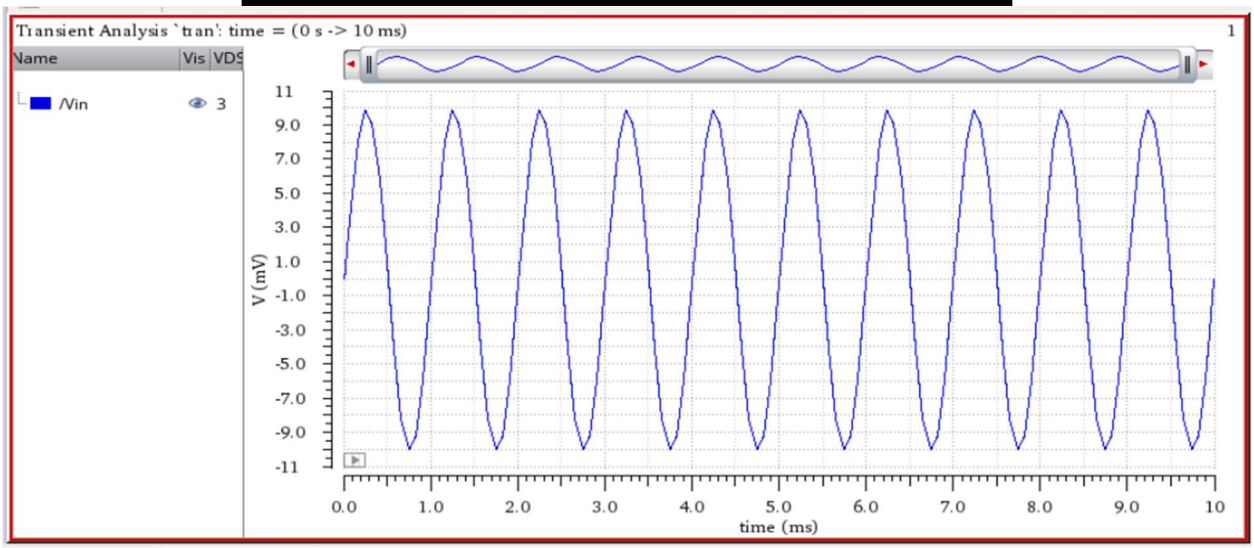
No, the relationship is not linear because the device is a long channel device. This makes the square law relatively applicable, resulting in the transfer characteristic being approximately square in the saturation region.

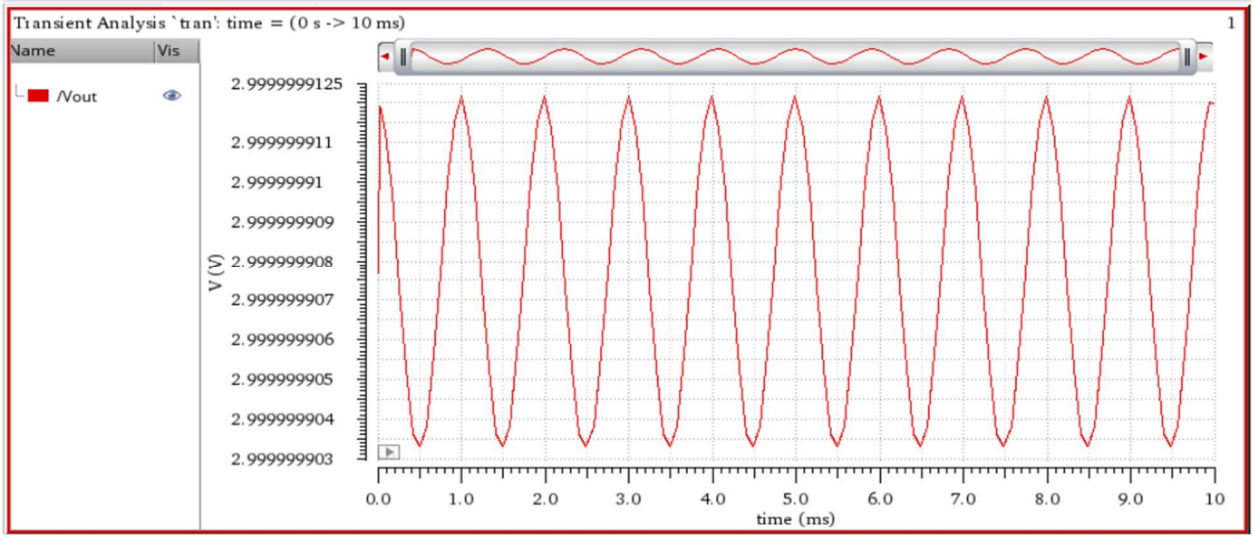
3) Calculate the derivative of VOUT using calculator. Plot the derivative vs VIN. The derivative is itself. the small signal gains. Is the gain linear (independent of the input)? Why?



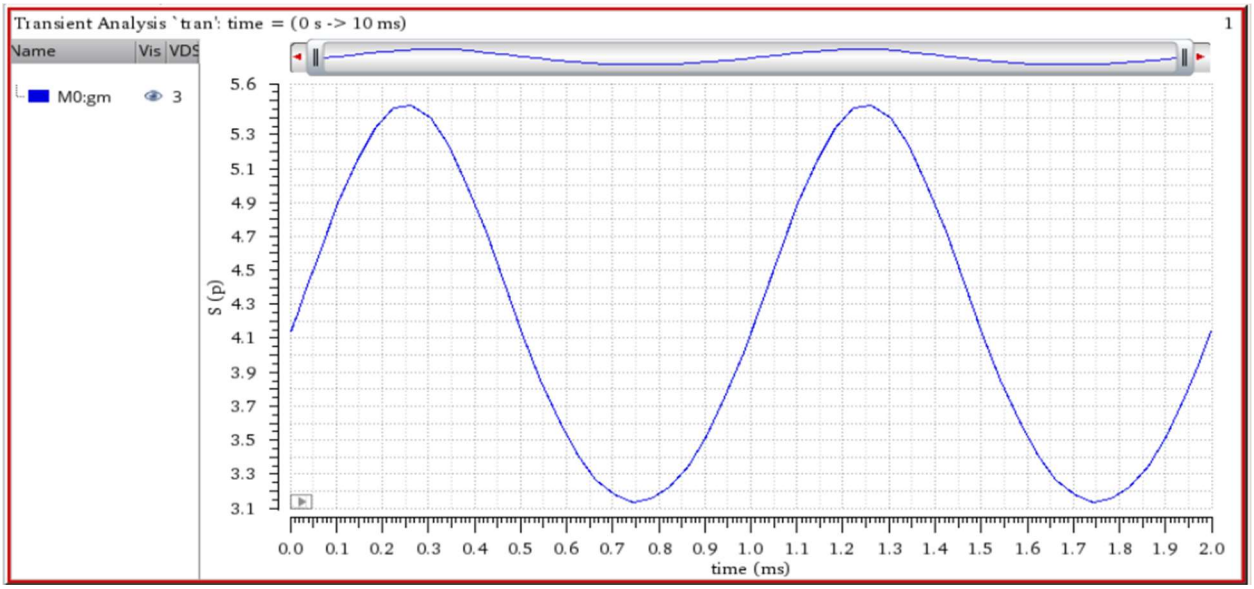
4) Set the properties of the voltage source to apply a transient stimulus (sine wave of 1kHz frequency and 10mV amplitude superimposed on the DC input voltage).


Vin
V2
VØ
vdc=VGS
acm=1
acp=Ø
gnd


Transient Analysis `tran': time = (0 s -> 10 ms)
Name
Vis
VDS
/Vin
3
V (mV)
time (ms)


Transient Analysis `tran': time = (0 s -> 10 ms)
Name
Vis
/Vout
V (V)
time (ms)

5) Create a new simulation configuration. Run transient simulation for 2ms. Plot gm vs time. Does gm vary with the input signal? What does that mean?



gm varies with the input signal level because it depends on the operating point of the transistor, which can vary with different input signals. This variation affects the overall gain of the circuit, making it dependent on the signal level rather than constant.

6) Is this amplifier linear? Comment.

No
As the gain , gm , Vout
Chang by the input signal which means the gain is a function of the input signal.
the amplifier should be the output signal =input signal + Zoom level.