Analog IC Design – Cadence Tools

Lab 03

Cascode Amplifier

Part 1: Sizing Chart

Use V* = 150 mV and ID = 10 uA. Use VDD = 3V

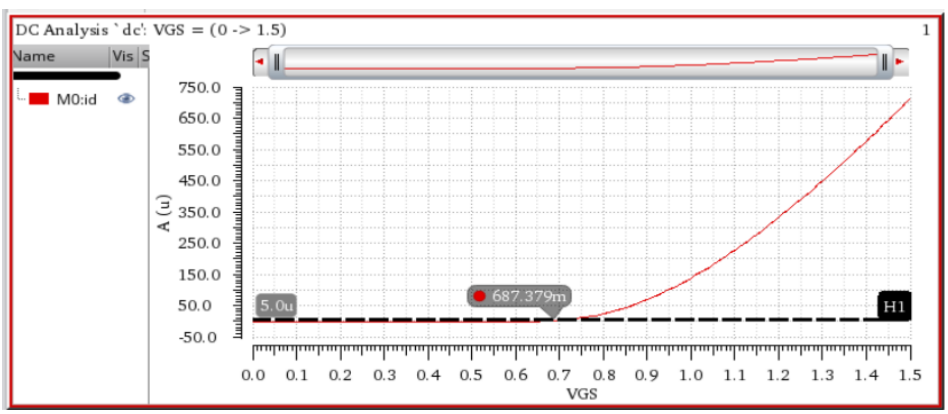
For a square-law device, $V* = Vov$, however, for a real MOSFET they are not equal.

The lower the $V*$ the higher the gain, but the larger the area and the lower the speed.

gm =2*ID /V* = (2*10*10^-6) /150*10^-3 = 133.33u

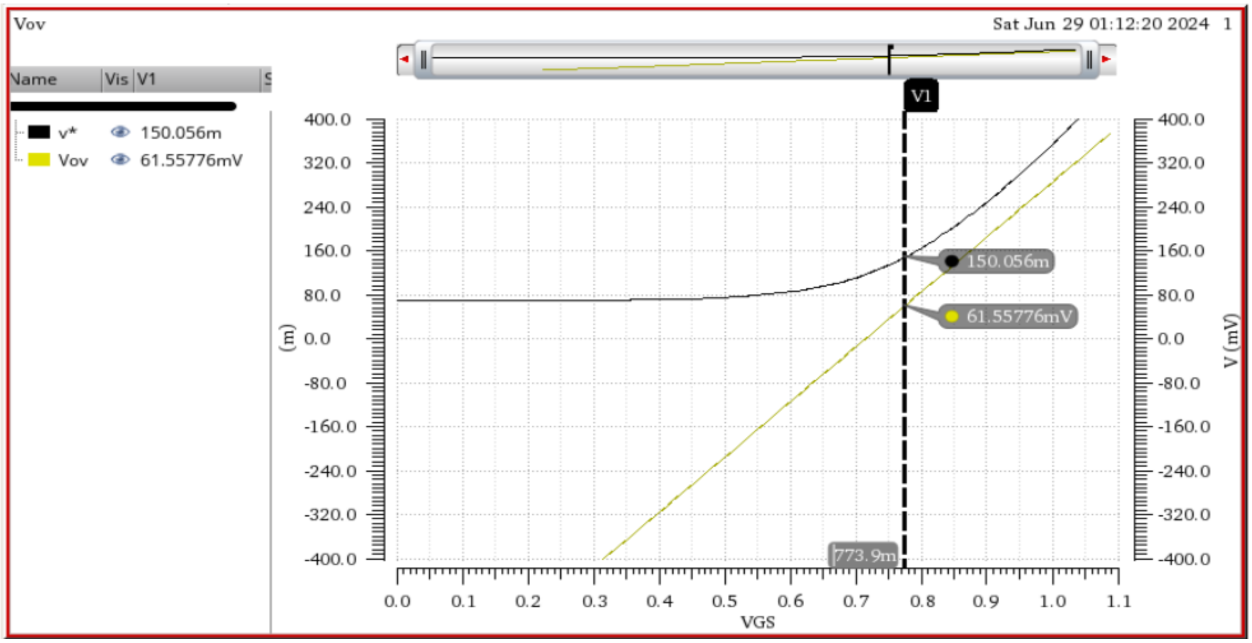
$V\ ov = VGS - VTH$

1. We use $W = 10\mu m$ & $L = 0.5\ \mu m$ & VDS =VDD/2 =3/2= 1.5 V
2. make a sweep for VGS from 0 to VDS with 10 mV steps 0:10m:1.5v
3. plot the $ID\ Vs\ VGS$ >>> determine the VTH value.



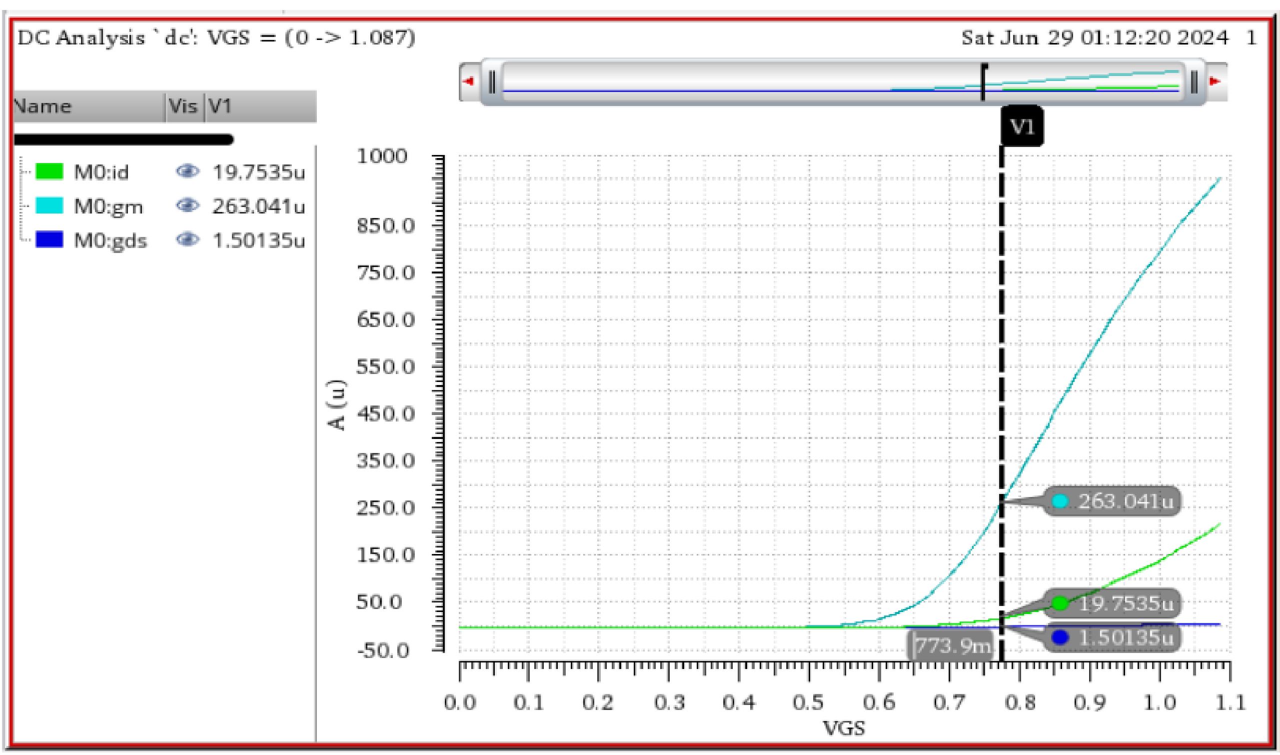
(the Vth is 687.379 mV=0.687)

4. make another sweep for VGS from 0 to 0.4 + VTH with 10 mV steps >> 0:10m:(0.4+0.787) >> 0:10m:1.08.
5. make expressions for $V*$ & Vov by calculator $V* = 2\text{ID}/\text{gm}$ and Vov= $VGS - VTH$.
6. plot them overlaid and we locate the point at which $V* = 150mV$ They should be the same scales.



VGS =773.9m when the v*=150mV

7. Plot ID, gm, and gds vs VGS. Find their values at $VGSQ$.



8. Get the WQ IDQ=10u IDX=19.75 Wx=10u

ID=$\frac{IDQ}{IDX} = \frac{(\frac{W}{L})_Q}{(\frac{W}{Q})_X}$ >> LQ=LX WQ= $(\frac{10u}{19.75u})$*10u =5.06u

9. calculate gmQ and $gdsQ$ using ratio and proportion (cross multiplication).

ID=$\frac{IDQ}{IDX} = \frac{(gm)_Q}{(gm)_X}$ >> $gm_x = = \frac{263.041u \; * \; 10u}{19.75u}$ = 133.188 u

ID=$\frac{IDQ}{IDX} = \frac{(gds)_Q}{(gds)_X}$ >> $gds_x = = \frac{1.5013u \; * \; 10u}{19.75u}$ = 0.7601 u

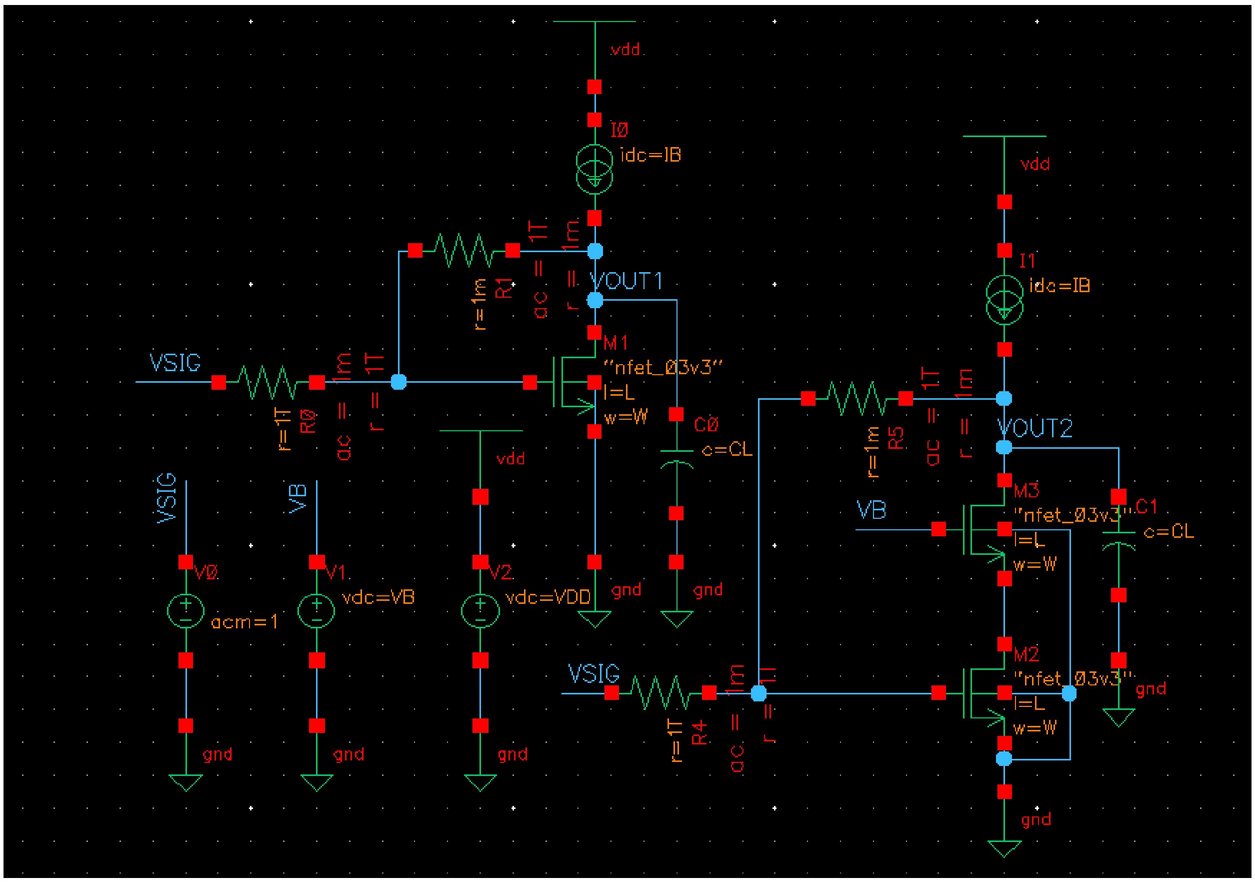
ro = 1/$gds = 666.067$ kΩ

PART 2: Cascode for Gain

1. OP Analysis

1) Create a new cell and schematic. Use $IB = 20\mu A$, $L = 0.5\mu m$, W as selected in Part 1, and $CL = 1pF$.

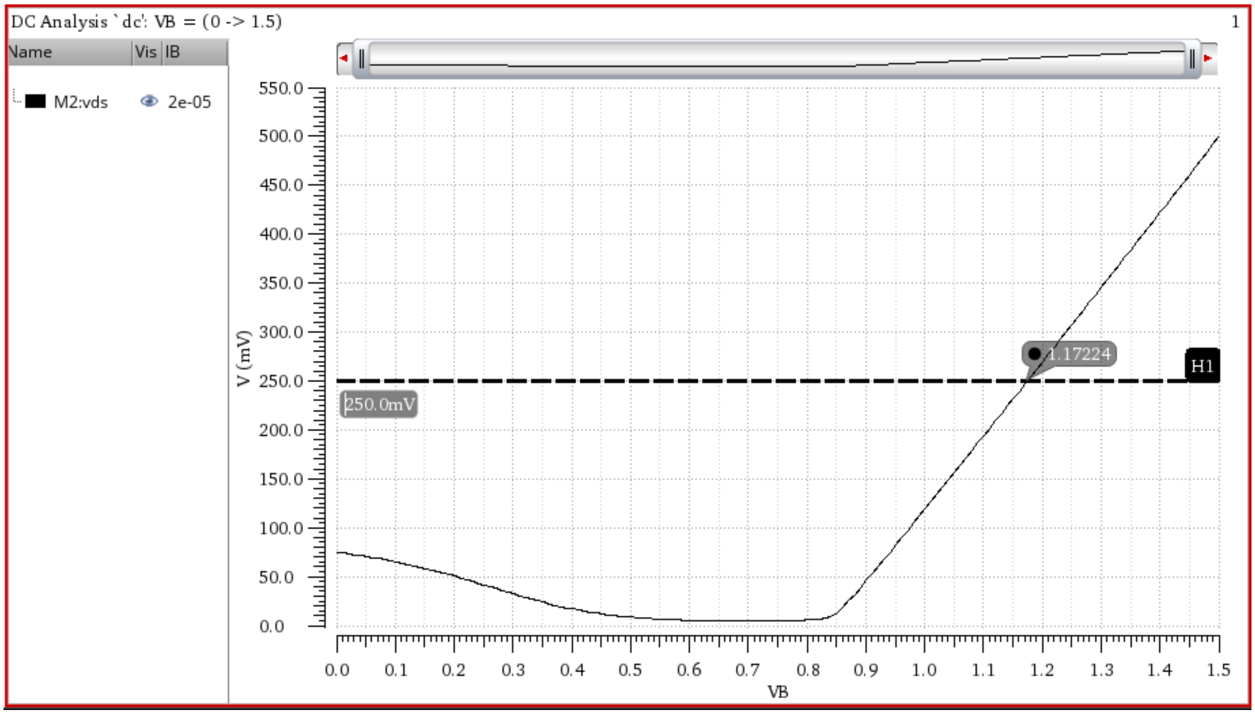
.1



2) $(VDS)M2\ Vs\ VB$:

VDS =V* +100mv = 150m +100m = 250 mv

The value found for VB is $1.172\ V$.



3) Parameters of M1, M2 & M3

Parameters M1	Parameters M2	Parameters M3

M1

Parameters	Value
model	"nfet_03v3"
l	L
w	W
id	10u
vgs	778.3m
vds	778.3m
vth	711.1m
vdsat	124.8m
gm	133.2u
gds	929.5n
gmb	47.63u
cdb	-620a
cgd	-945.6a
cgs	-4.969f
csb	-928.8a
region	2

Inst M2

Parameters	Value
model	"nfet_03v3"
l	L
w	W
id	10u
vgs	782.7m
vds	294.3m
vth	711.7m
vdsat	127.2m
gm	131.6u
gds	1.967u
cdb	-638.4a
cgd	-1.019f
cgs	-5.055f
csb	-947.1a
csb	-947.1a
region	2

M3

Parameters	Value
model	"nfet_03v3"
l	L
w	W
id	10u
vgs	877.7m
vds	488.4m
vth	807.2m
vdsat	128.5m
gm	132.4u
gds	1.181u
cdb	-535.4a
cgd	-1.005f
cgs	-5.06f
csb	-800.2a
csb	-800.2a
region	2

4) <u>Check that all transistors operate in saturation.</u>

in simulation outputs,
VDS > VGS -Vth >>>> all transistors operate in saturation.
all transistors operate in region 2 which is the saturation region.

5) <u>Do all transistors have the same vth? Why?</u>

No, in M1 is approximately equal to M2 But the M3 is very different
VDS is directly proportional to Vth M1 > M2 > M3
It is reduced due to DIBL effect.
Higher VTH because it influences the body because Source voltage.

6 What is the relation (≪, <, =, >, ≫) between gm and gds?

$gm \gg gds.$

7 What is the relation (≪, <, =, >, ≫) between gm and gmb?

$gm >> gmb.$

8 What is the relation (≪, <, =, >, ≫) between cgs and cgd?

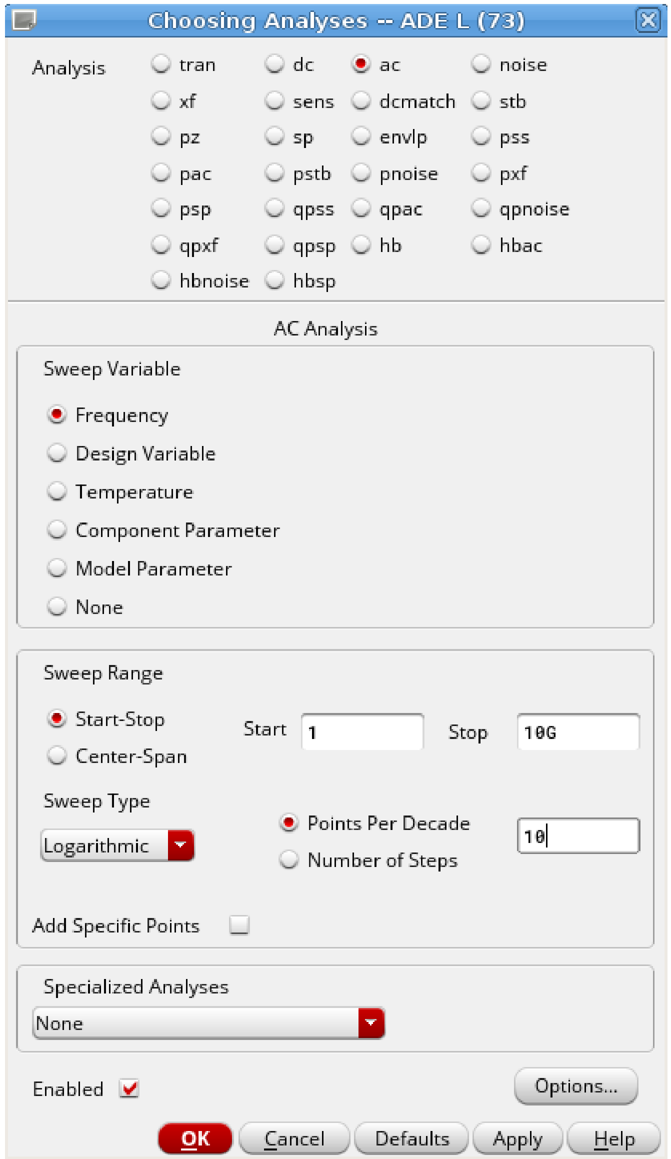
$Cgs >> Cgd$

9 What is the relation (≪, <, =, >, ≫) between csb and cdb?

$Csb >> Cdb$

2. AC Analysis

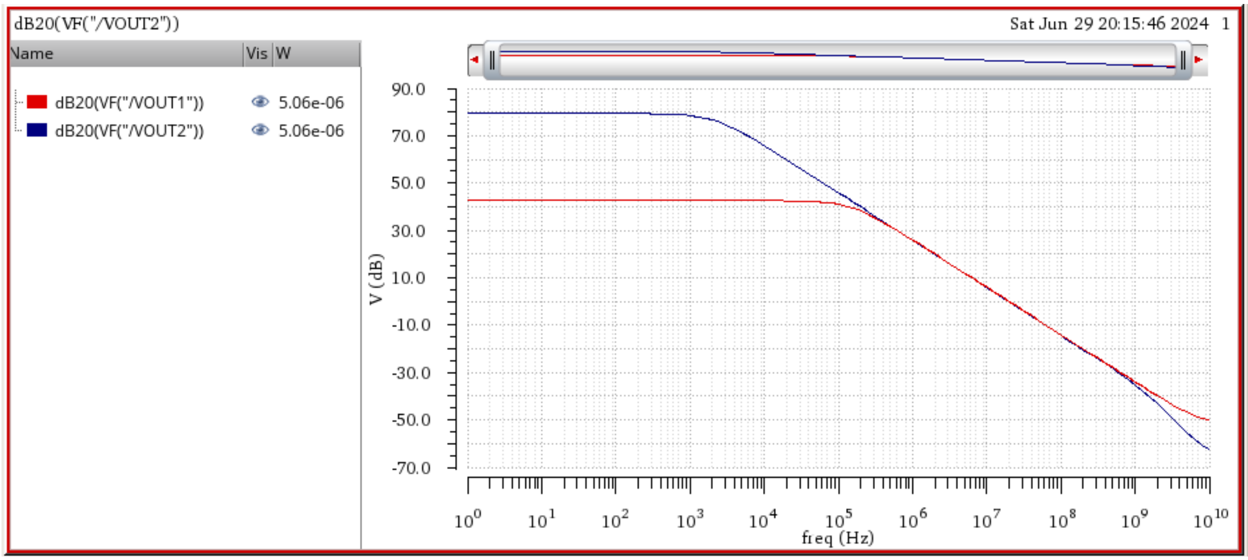
1) Create a new simulation configuration. Perform AC analysis (1Hz:10GHz, logarithmic, 10points/decade) to simulate gain and bandwidth.



2- Use calculator to create expressions for circuit parameters (DC gain, BW, GBW, and UGF) and export them to adexl.

dB20(VF("/VOUT1"))	
ymax(dB20(VF("/VOUT1")))	43.12
ymax(mag(VF("/VOUT1")))	143.3
bandwidth(VF("/VOUT1") 3 "l...	147.2k
gainBwProd(VF("/VOUT1"))	21.14M
unityGainFreq(VF("/VOUT1"))	21.3M
dB20(VF("/VOUT2"))	
ymax(dB20(VF("/VOUT2")))	79.88
ymax(mag(VF("/VOUT2")))	9.86k
bandwidth(VF("/VOUT2") 3 "l...	2.089k
gainBwProd(VF("/VOUT2"))	20.65M
unityGainFreq(VF("/VOUT2"))	20.74M

3) Report the Bode plot (magnitude) of CS and cascode **appended on the same plot**.



4) Using small signal parameters from OP simulation, perform hand analysis to calculate DC gain, BW, and GBW of both circuits.

M2

Parameters	Value
model	"nfet_03v3"
l	L
w	W
id	10u
vgs	782.687m
vds	294.314m
vth	711.652m
vdsat	127.17m
gm	131.611u
gds	1.96746u
gmb	47.0675u
cdb	-638.448a
cgd	-1.01882f
cgs	-5.05539f
csb	-947.093a

M3

Parameters	Value
model	"nfet_03v3"
l	L
w	W
id	10u
vgs	877.686m
vds	488.373m
vth	807.233m
vdsat	128.54m
gm	132.409u
gds	1.18092u
gmb	40.4952u
cdb	-535.371a
cgd	-1.00515f
cgs	-5.05995f
csb	-800.215a

Gain

CS Av =gm1*ro1 = 143.3 = 20log (143.3) =43.12dB

calculate DC $Av = (gm2 + gmb2)\, ro2\, gm3\, ro3$

= (131.611u +47.067u) *(1/1.967u) * 132.41u *(1/1.1809u) = 10.185k =80.159 dB

Bw

For CS: $BW = \frac{1}{(2\pi\, r_o C_L)} = 149.3$ kHZ

For Cascode: $BW = \frac{1}{2\pi(r_{o2}+(1+(g_{m2}+g_{mb2})r_{o2})r_{o3})\, C_L} = 2.31$KHZ

GBW & UGF:

For CS: $GBW = UGF = Av * BW = 24.23\ MHz$

For Cascode: $GBW = UGF = Av * BW = 23.515\ MHz$

5) Report a table comparing the DC gain, BW, UGF, and GBW of both circuits from simulation and hand analysis.

Analysis	Analytical			Simulation		
Quantity	Gain	BW	GBW & UGF	Gain	BW	GBW & UGF
CS	43.12dB	149.3 kHZ	24.23 MHz	43.12dB	147.2k	21.3M
Cascode	10.185k	2.31KHZ	23.515MHz	9.86k	2.089k	20.47M

6) Comment on the results

The bandwidth of the cascode amplifier is much less than the conventional amplifier, but the gain of the cascode amplifier is much greater than the conventional amplifier. This means that almost the same bandwidth is achieved. It is a mixture of gain and bandwidth because more weight increases the bandwidth and vice versa.