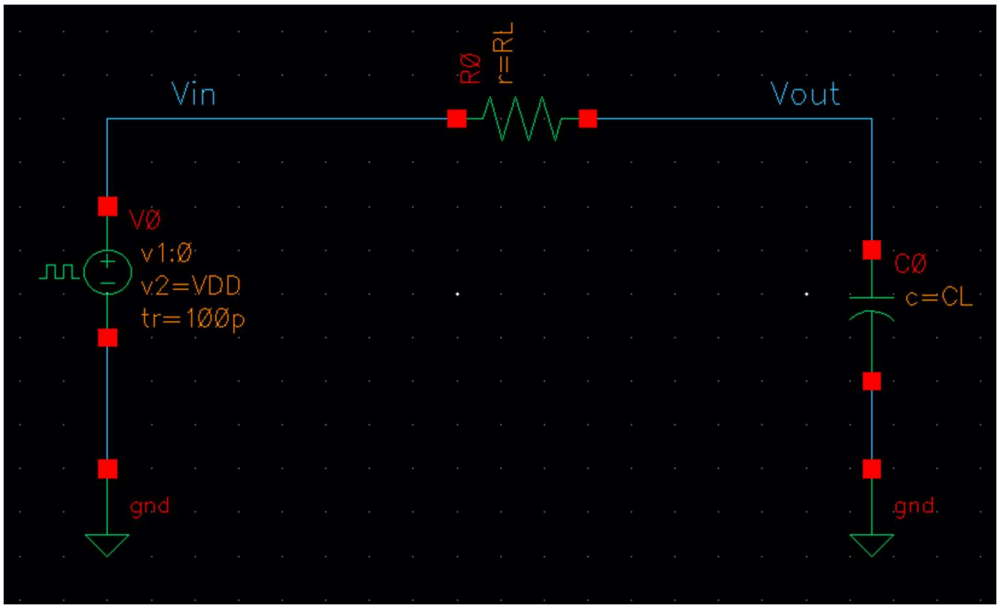
Analog IC Design – Cadence Tools
Lab 01
LPF Simulation and MOSFET Characteristics

PART 1: Low Pass Filter Simulation (LPF)

1. Transient Analysis

Design a first order low pass filter.

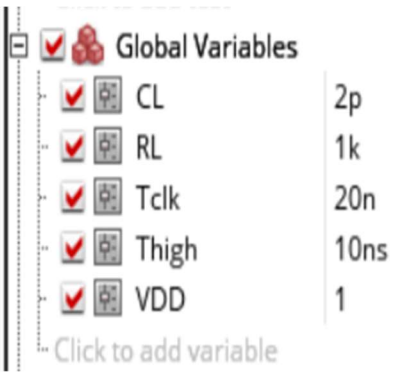


$R = 1k\Omega$ 2 ns time constant

2n/1k = 2p >> CL

Apply a square wave input with $T_{high} = Pulse\ Width = 10ns$, $T_{clk} = Period = 20ns$, and $T_{rise} = T_{fall} = 100ps$

PAC phase	
Voltage 1	0 V
Voltage 2	VDD V
Period	Tclk s
Delay time	Tclk/4 s
Rise time	100p s
Fall time	100p s
Pulse width	Thigh s
Temperature coefficient 1	



Report transient analysis results for two periods.

Output Raining

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ion started at: 9:02:14 PM, Mon Jun 24, 2024, ended at: 9:02:
 completes with 0 errors, 4 warnings, and 0 notices.
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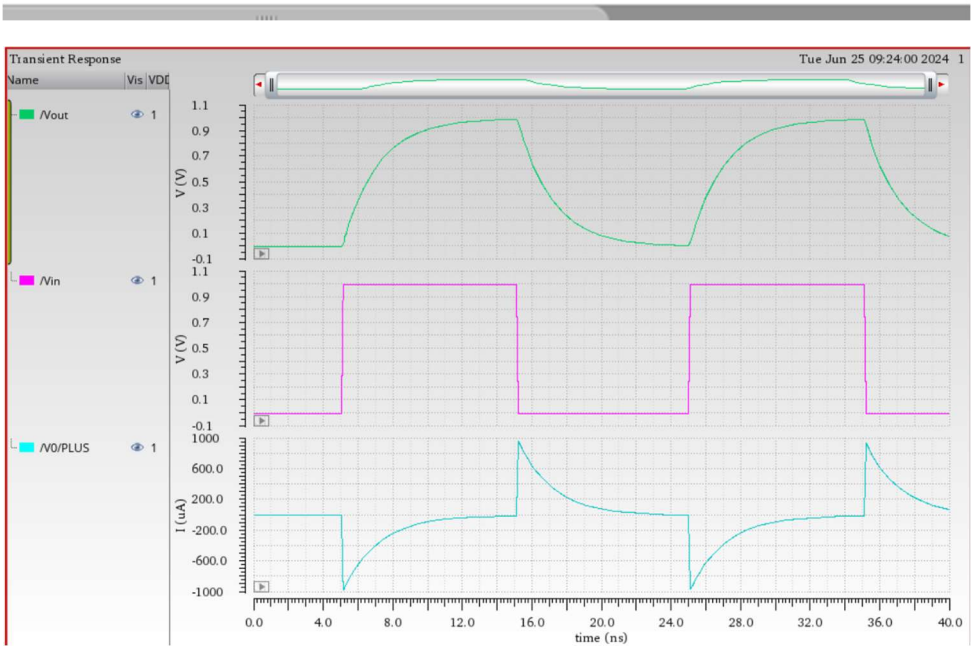


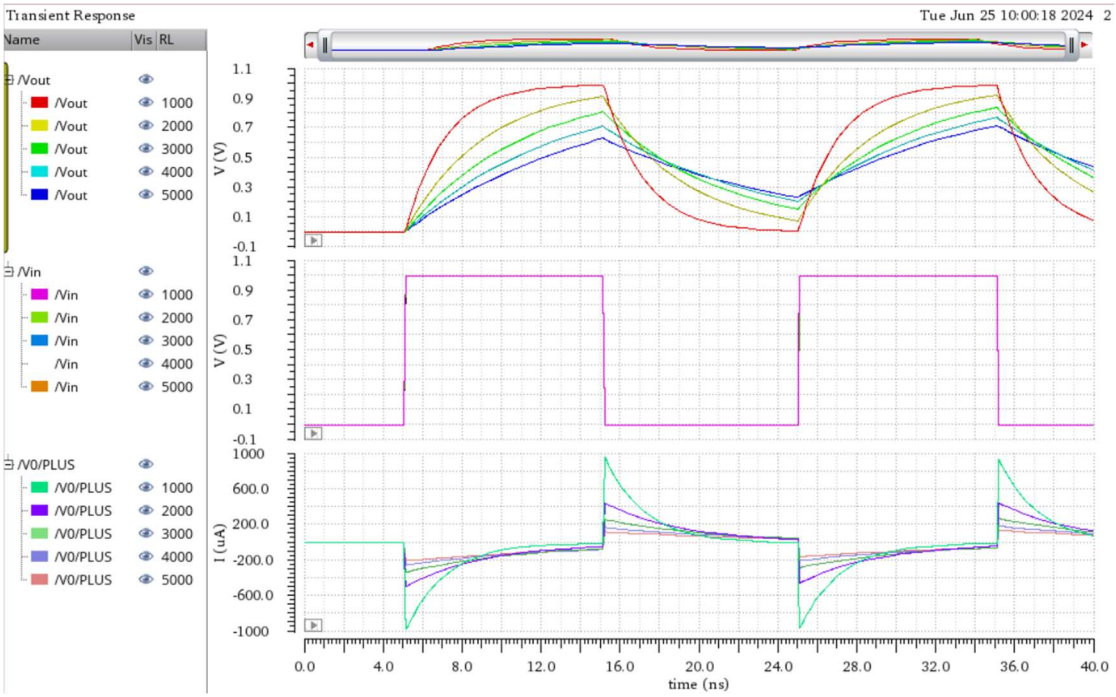
Calculate rise and fall time (10% to 90%) using Cadence calculator expressions. Export the expressions to adexl.

Test	Output	Nominal	Spec	Weight	Pass/Fail
part_1:lpf_tp:1	/Vout				
part_1:lpf_tp:1	/Vin				
part_1:lpf_tp:1	/V0/PLUS				
part_1:lpf_tp:1	Trise	4.392n			
part_1:lpf_tp:1	Tfall	4.392n			

Compare simulation with analytical results in a table.

	Rise Time	**Fall Time**
Analytical (2.2*τ)	4.4n	4.4n
Simulation	4.392n	4.392n

Do parametric sweep for R = 1: 1: 5$k\Omega$ Report overlaid results. Comment on the results.



Point	Test	Output	Nominal	Spec	Weight	Pass/Fail
Parameters: RL=1k						
1	part_1:lpf_tp:1	/Vout				
1	part_1:lpf_tp:1	/Vin				
1	part_1:lpf_tp:1	/V0/PLUS				
1	part_1:lpf_tp:1	Trise	4.392n			
1	part_1:lpf_tp:1	Tfall	4.392n			
Parameters: RL=2k						
2	part_1:lpf_tp:1	/Vout				
2	part_1:lpf_tp:1	/Vin				
2	part_1:lpf_tp:1	/V0/PLUS				
2	part_1:lpf_tp:1	Trise	8.771n			
2	part_1:lpf_tp:1	Tfall	8.771n			
Parameters: RL=3k						
3	part_1:lpf_tp:1	/Vout				
3	part_1:lpf_tp:1	/Vin				
3	part_1:lpf_tp:1	/V0/PLUS				
3	part_1:lpf_tp:1	Trise	eval err			
3	part_1:lpf_tp:1	Tfall	eval err			
Parameters: RL=4k						
4	part_1:lpf_tp:1	/Vout				
4	part_1:lpf_tp:1	/Vin				
4	part_1:lpf_tp:1	/V0/PLUS				
4	part_1:lpf_tp:1	Trise	eval err			
4	part_1:lpf_tp:1	Tfall	eval err			
Parameters: RL=5k						
5	part_1:lpf_tp:1	/Vout				
5	part_1:lpf_tp:1	/Vin				
5	part_1:lpf_tp:1	/V0/PLUS				
5	part_1:lpf_tp:1	Trise	eval err			
5	part_1:lpf_tp:1	Tfall	eval err			

Comment on the results.

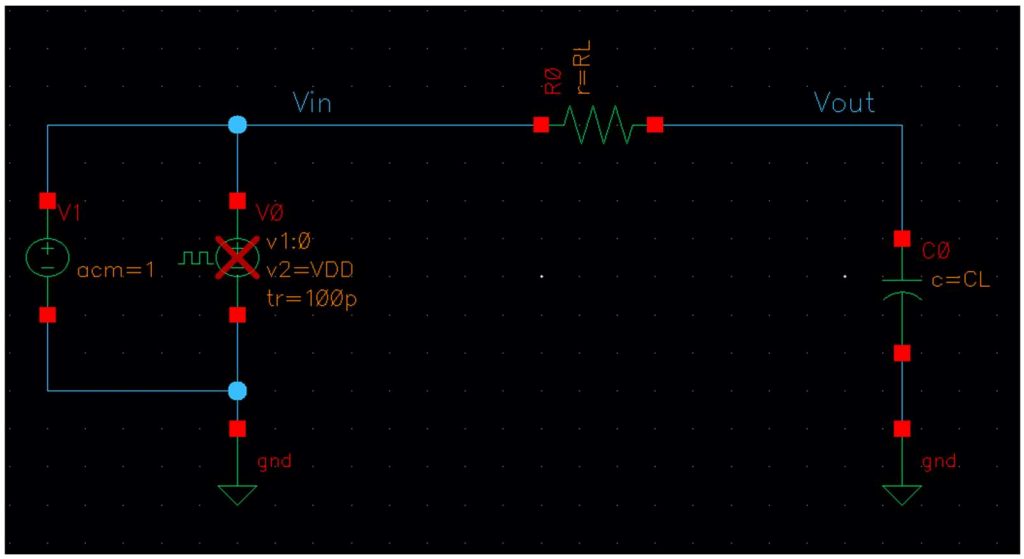
Increasing R results in Increasing τ >> linearly proportional

with τ increasing the cutoff frequency decrease

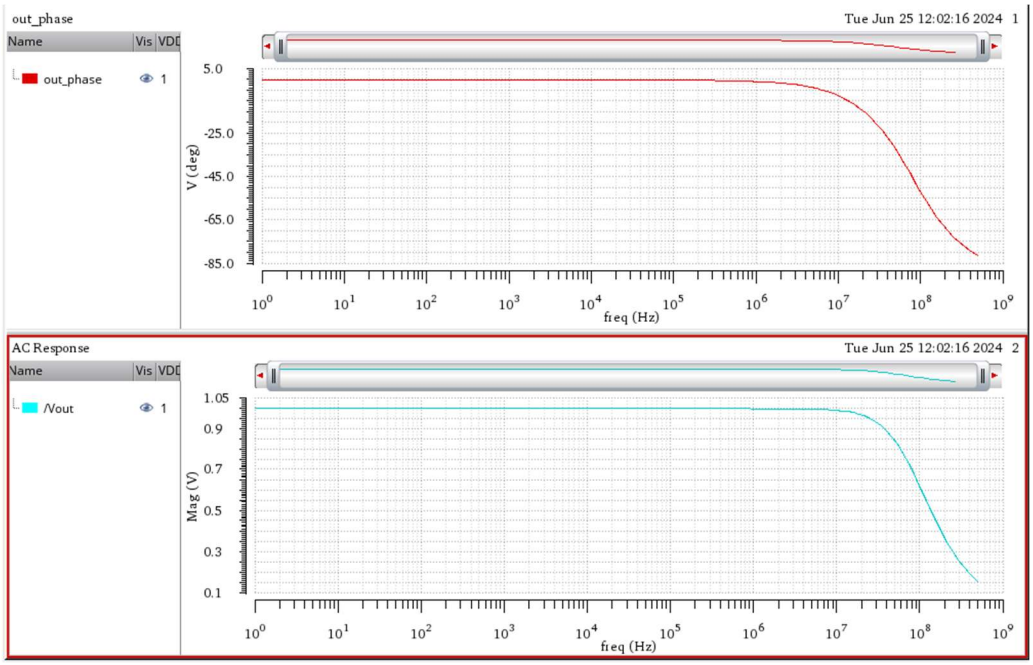
but both the rise time and fall times increase. In case of {R = 3$K\Omega$ - R = 4$K\Omega$ - R = 5$K\Omega$} rise and fall times are bigger than pulse width so it cannot be calculated

2. AC Analysis

Av = Vout /vin vin = 1v Vout = 1v



Analysis F = 1/ Time constant = 1/2n = 500M H

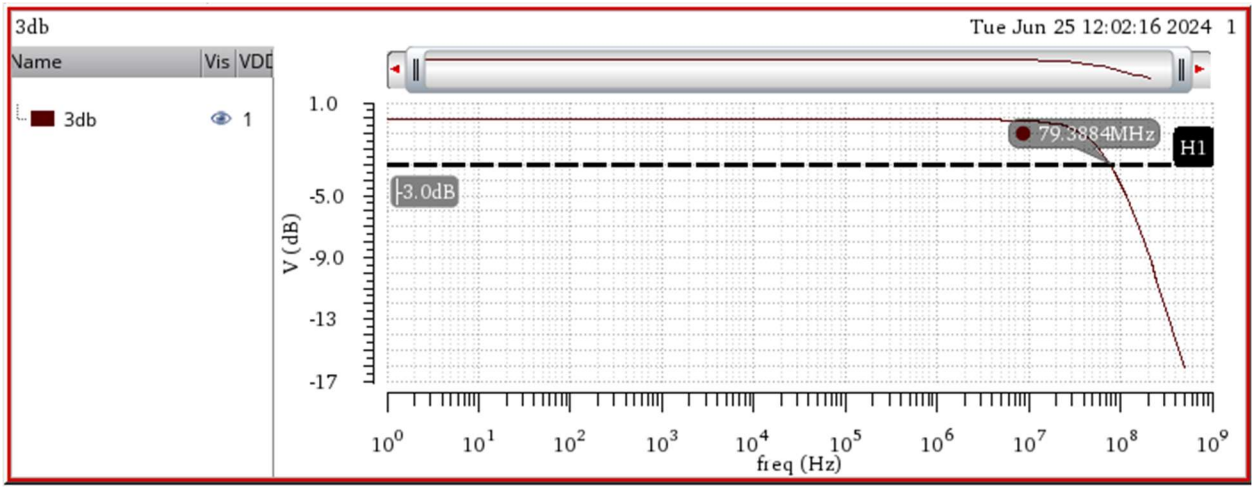


Calculate DC gain and 3dB bandwidth using Cadence calculator expressions. Export the expressions to adexl.

H(S)=Vout/Vin =1/(1+SRC), DC gain $S = 0$ then DC gain $= 1$

$3dB$ BW =1/2π RC 500M/2π =79.57M

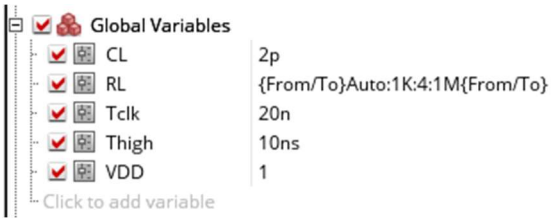
Test	Output	Nominal	Spec	Weight	Pass/Fail
part_1:lpf_tp:1	LPF_out_magntude				
part_1:lpf_tp:1	out_phase				
part_1:lpf_tp:1	3db				
part_1:lpf_tp:1	B.W	79.51M			
part_1:lpf_tp:1	Gain	1			



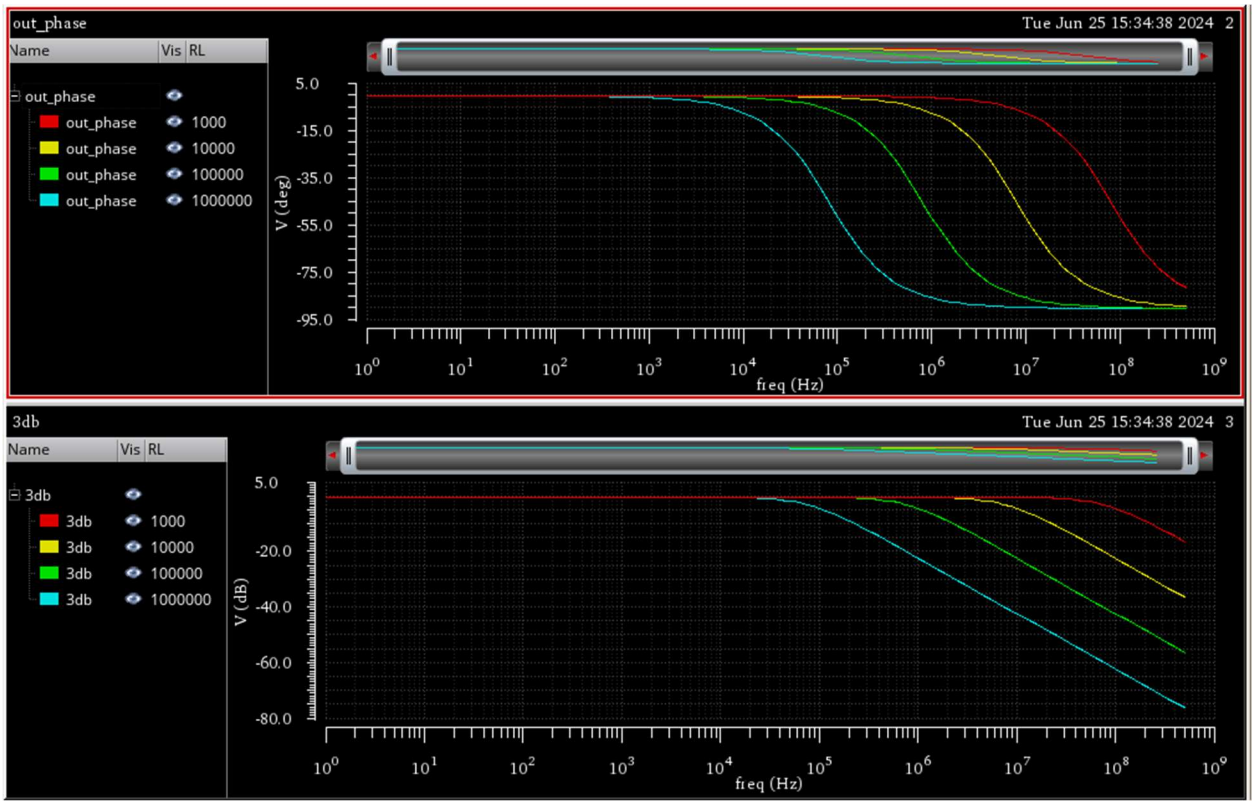
Compare simulation with analytical results in a table.

	3db	Gain
Analytical	79.57M	1
Simulation	79.3884M	1

Do parametric sweep for R = $1,10,100,1000k\Omega$. Report overlaid results. Comment on the results.



Point	Test	Output	Nominal	Spec	Weight	Pass/Fail
Parameters: RL=1k						
1	part_1:lpf_tp:1	LPF_out_magntude				
1	part_1:lpf_tp:1	out_phase				
1	part_1:lpf_tp:1	3db				
1	part_1:lpf_tp:1	B.W	79.51M			
1	part_1:lpf_tp:1	Gain	1			
Parameters: RL=10k						
2	part_1:lpf_tp:1	LPF_out_magntude				
2	part_1:lpf_tp:1	out_phase				
2	part_1:lpf_tp:1	3db				
2	part_1:lpf_tp:1	B.W	7.951M			
2	part_1:lpf_tp:1	Gain	1			
Parameters: RL=100k						
3	part_1:lpf_tp:1	LPF_out_magntude				
3	part_1:lpf_tp:1	out_phase				
3	part_1:lpf_tp:1	3db				
3	part_1:lpf_tp:1	B.W	795.1k			
3	part_1:lpf_tp:1	Gain	1			
Parameters: RL=1M						
4	part_1:lpf_tp:1	LPF_out_magntude				
4	part_1:lpf_tp:1	out_phase				
4	part_1:lpf_tp:1	3db				
4	part_1:lpf_tp:1	B.W	79.51k			
4	part_1:lpf_tp:1	Gain	1			



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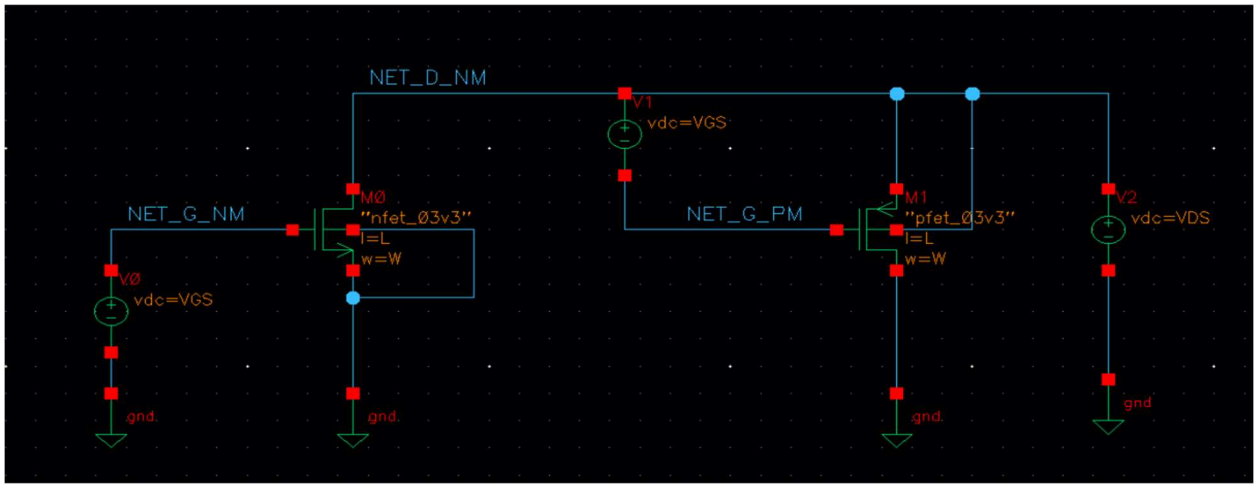
DC gain does not depend on R or C, so it did not change.

while the bandwidth is inversely proportional to RC

When (RC(increases, (phase, B.W) decreases

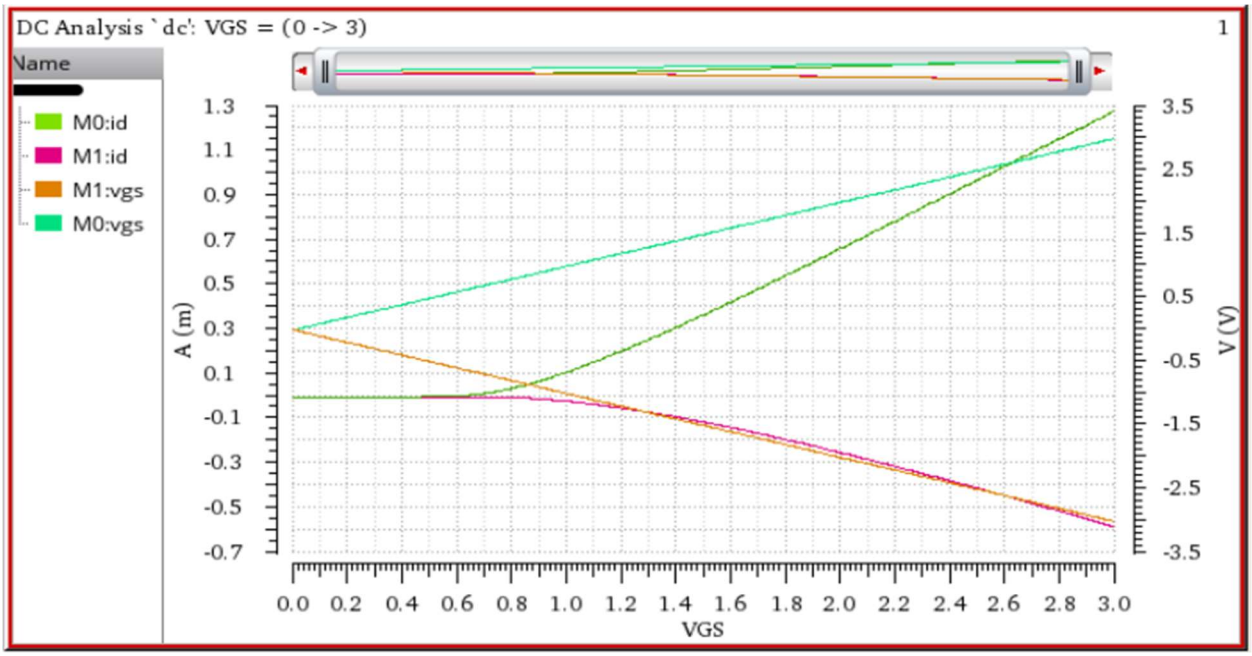
Part 2: MOSFET Characteristics



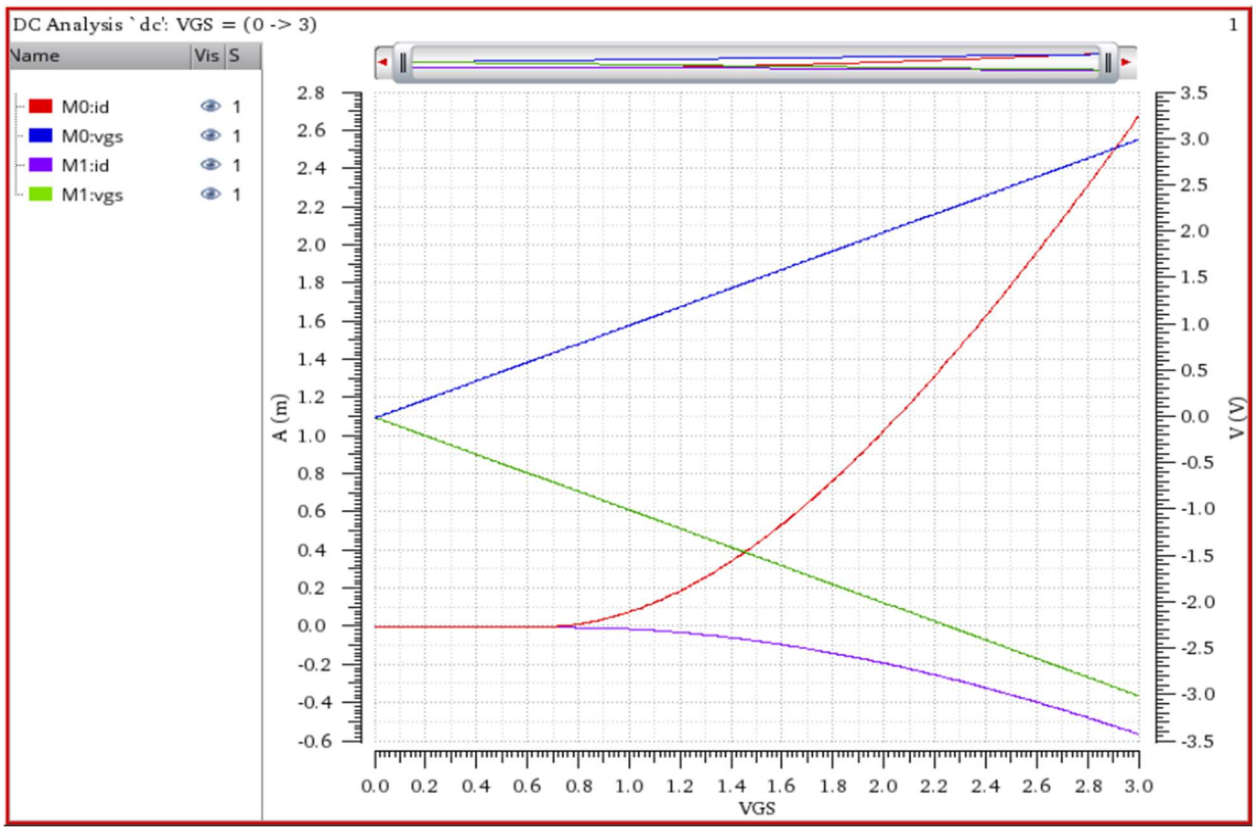
Plot $ID - VGS$ characteristics for NMOS and PMOS devices. Set $VDS = VDD$, and VGS = 0: $10m$: VDD. Use VDD = $1.2V$ for 130nm technology and VDD = $1.8V$ for 180nm technology. Plot the results overlaid for the following.

(Use VDD = 3V) IN CANVAS use W/L = **3u/300n** for the short channel device, and **30u/3u** for the long channel

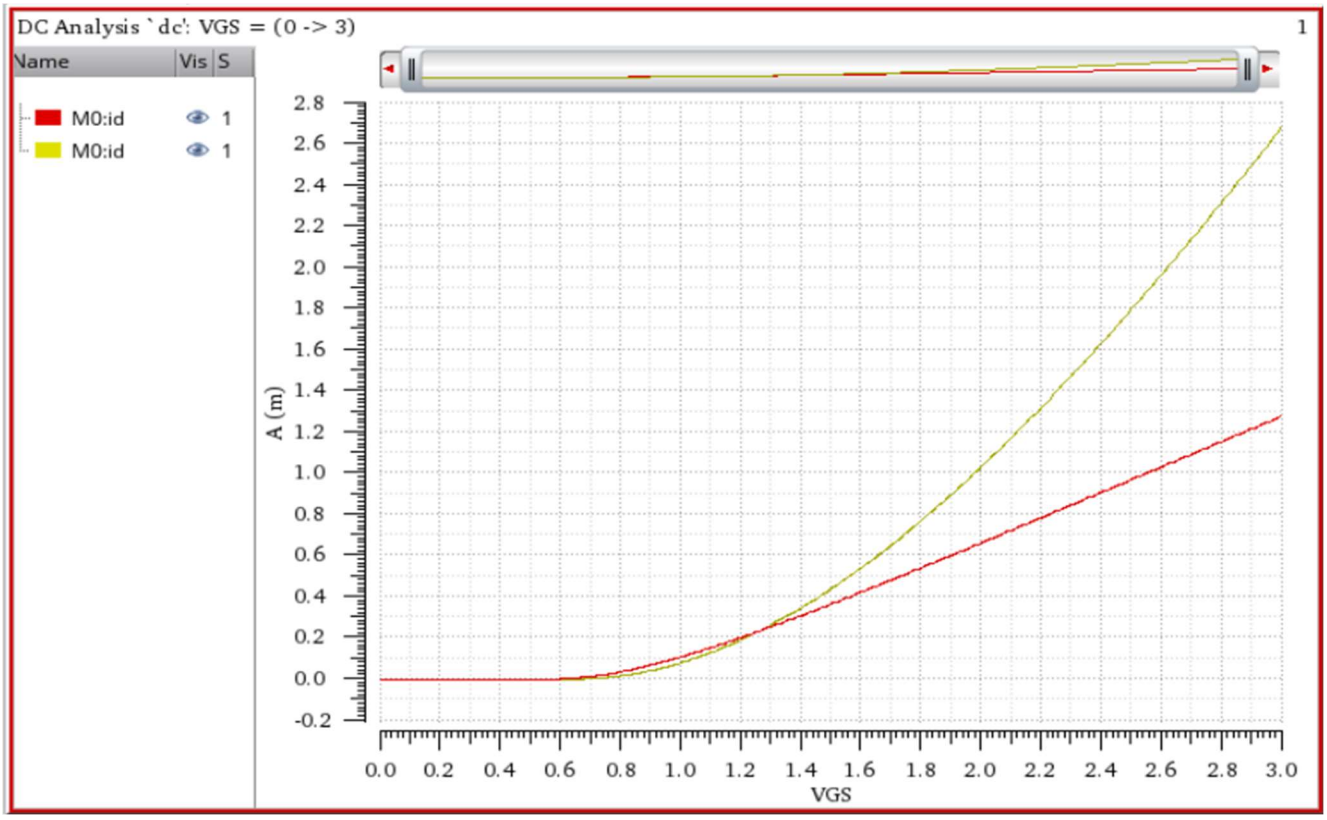
Short channel device vdd=3v. (COMPARD { $ID - VGS$ } TO NMOS & PMOS).



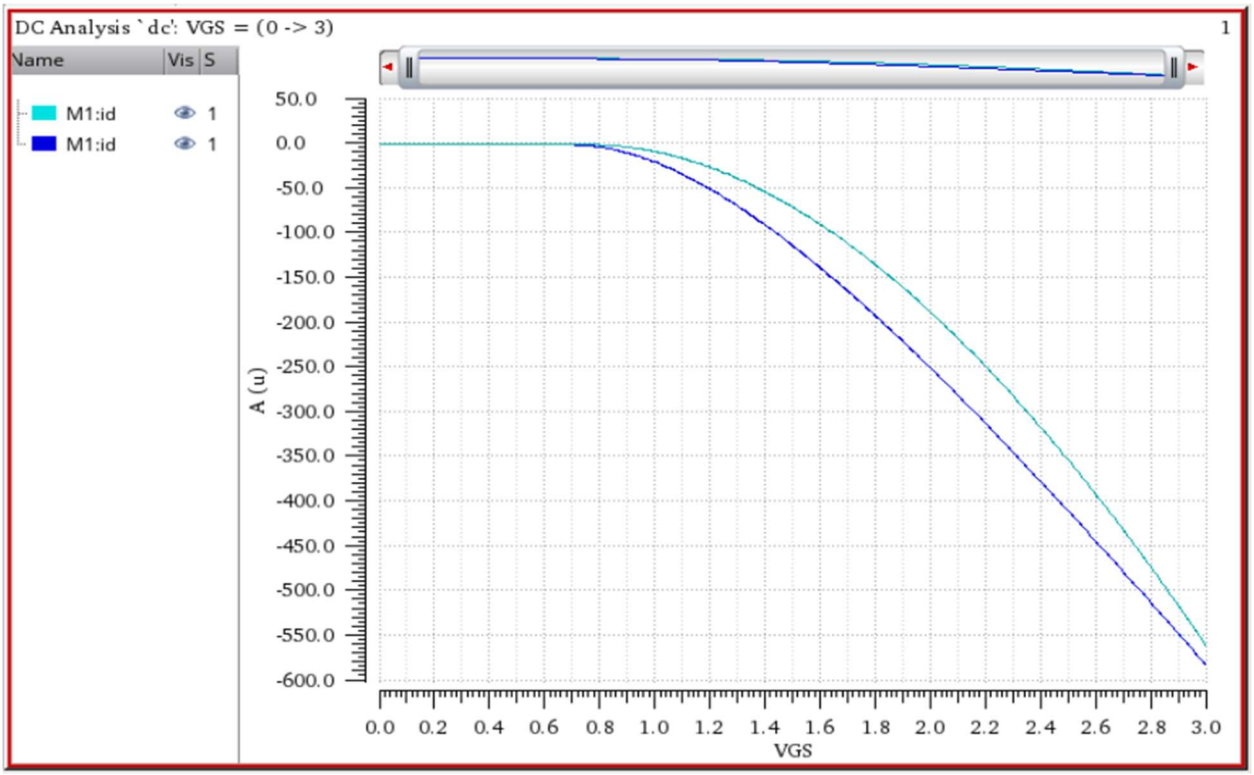
Long channel device vdd= 3v (COMPARD { $ID - VGS$ } TO NMOS & PMOS)



ID IN NMOS OF (SHORT & LONG)



ID IN PMOS OF (SHORT & LONG)



Comment on the differences between short channel and long channel results.

• Which one has higher current? Why?

For NMOS, a high-channel device provides a better display compared to a low-channel device. The reason for this is that the device suffers from a lack of weight due to its effect on speed saturation, which leads to a smaller output than usual, because it does not saturate before it reaches the starting point.

In case of PMOS devices, the current in the short-channel device is higher than the current in the long-channel device. This is due to the effect of voltage-induced barrier lowering (DIBL).

• Is the relation linear or quadratic? Why?

For short-channel devices, the relationship is linear, because the amplification factor (gm) reaches a saturated value and does not increase with increasing V_gs.

As for long-channel devices, the relationship is quadratic, as the amplification factor (g_m) increases with increasing V_gs.

Comment on the differences between NMOS and PMOS.

• Which one has higher current? Why?

NMOS device has the highest comparison with PMOS device. The reason for this is that the alternating current in an NMOS device consists of electrons, while the alternating current in a PMOS device consists of radio. Therefore, the electrons move faster than the radio.

• What is the ratio between NMOS and PMOS currents at VGS = VDD?

The ratio of the currents between the NMOS and PMOS devices at

VGS = VDD un/up
. This is because both devices have the same bias and size, and differ only in the movement of the carriers

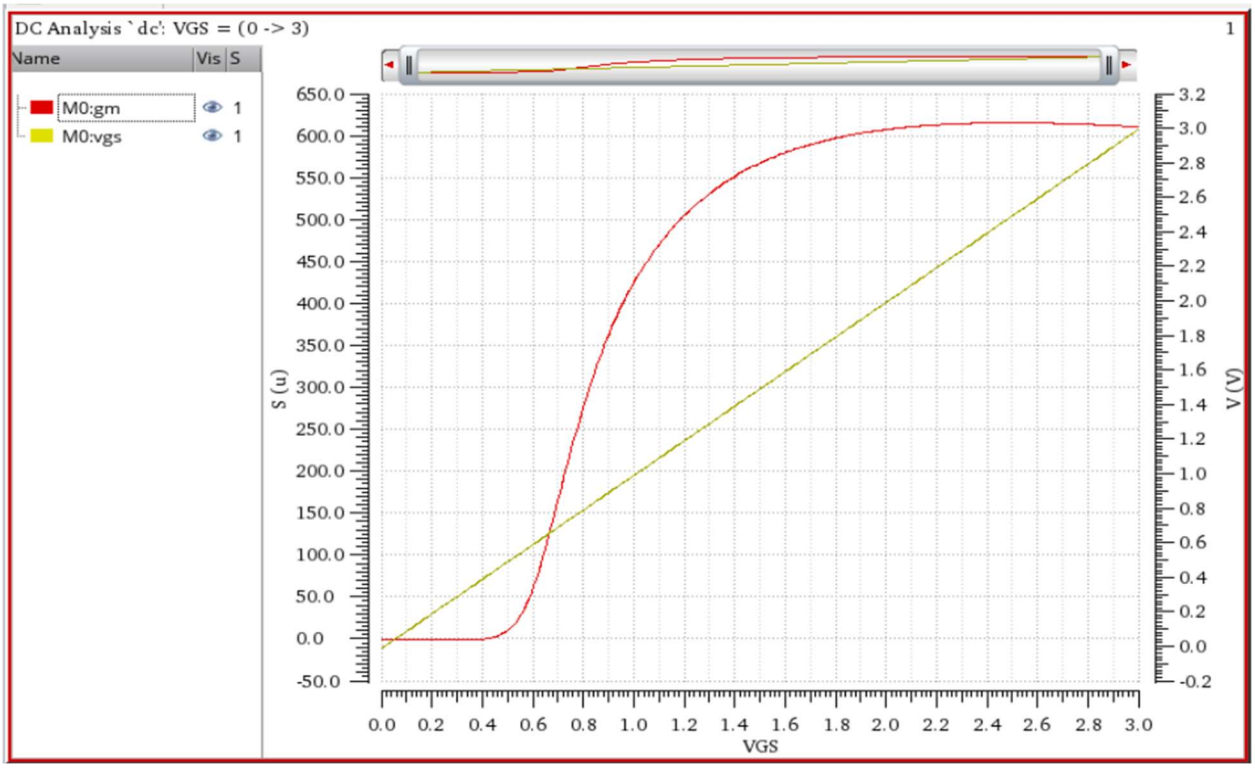
• Which one is more affected by short channel effects?

The NMOS device is more affected by short channel effects. This can be clearly seen from the graph of id vs vgs

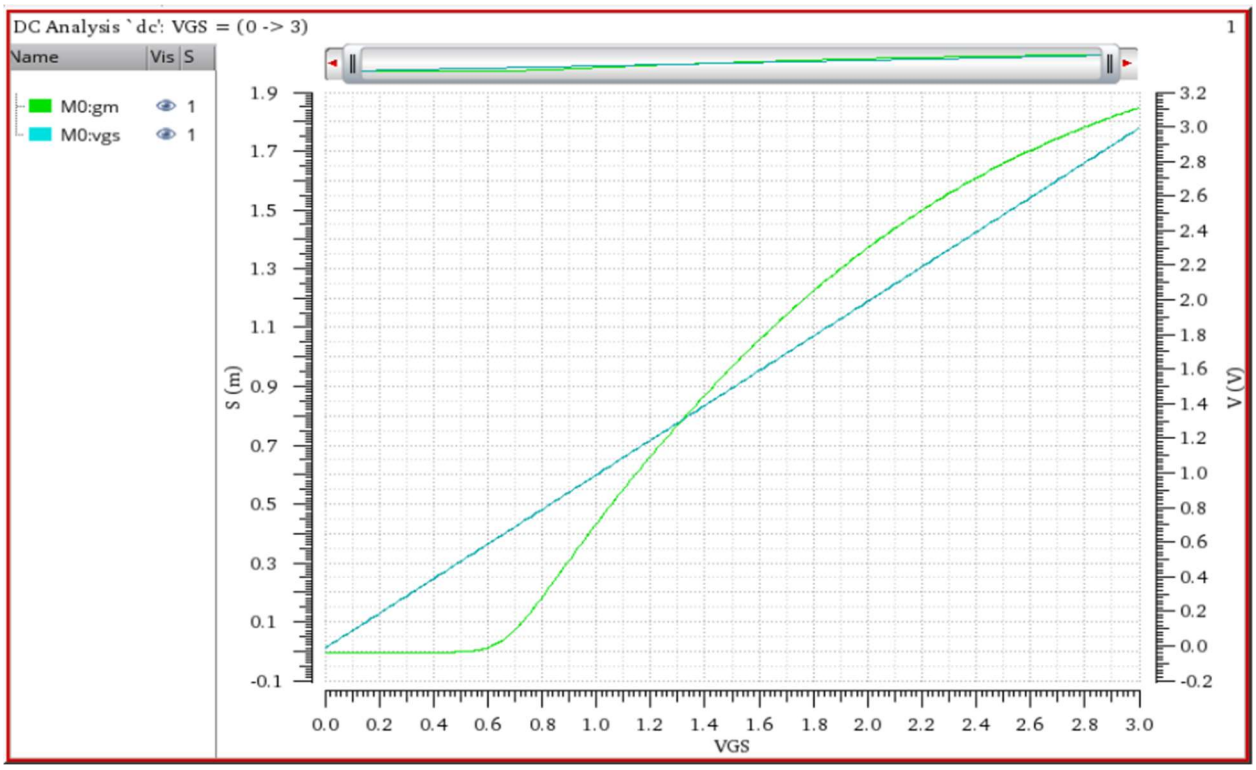
2. g_m vs VGS

1) Plot g_m vs V_{GS} for NMOS device. Set $V_{DS} = V_{DD}$, and $V_{GS} = 0{:}\ 10m{:}\ V_{DD}$. Plot the results overlaid for the following:

Short channel device vdd=3v



Long channel device vdd=3v



2) Comment on the differences between short channel and long channel results.

• Does □□ increase linearly? Why?

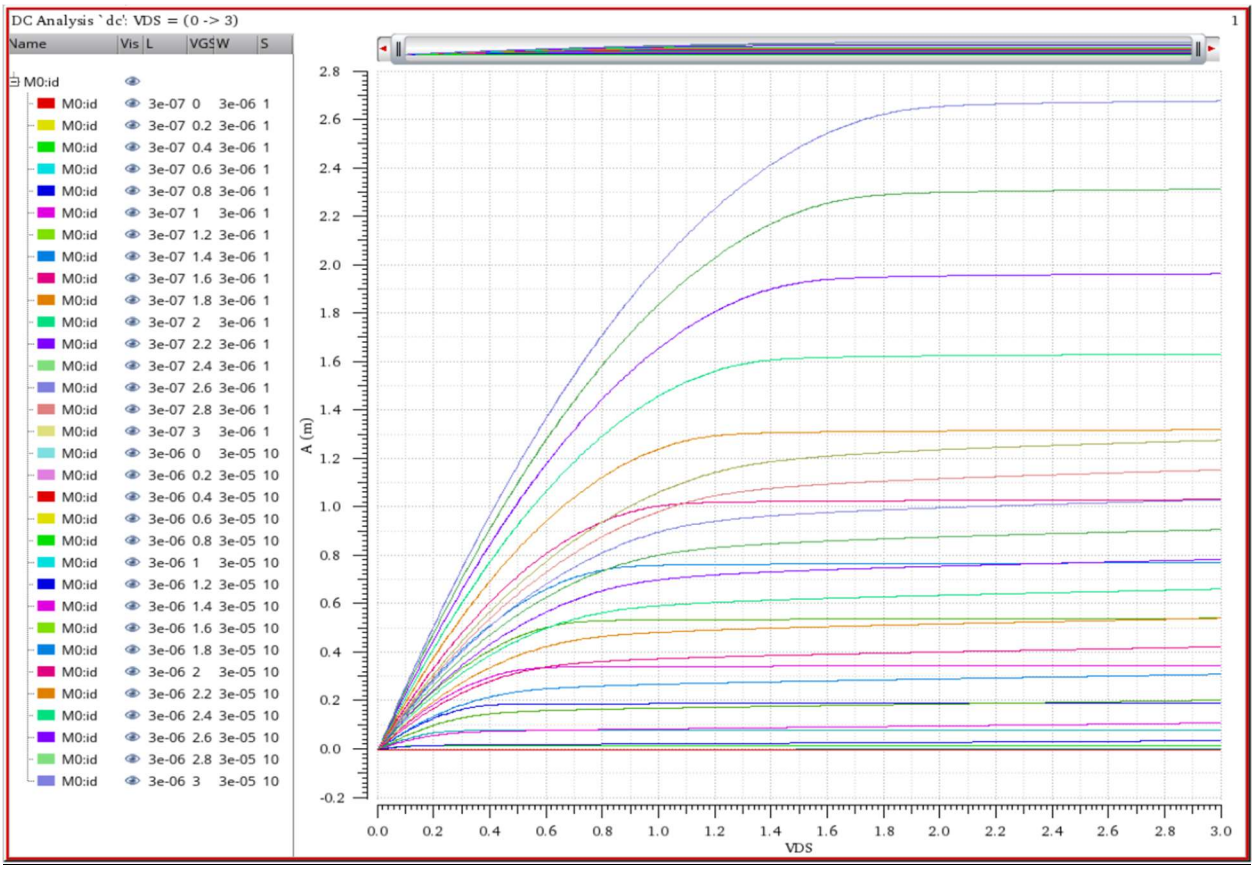
In case of a long channel device, increases.
gm is approximately linear because the device reaches the interruption saturation point before it reaches the speed saturation point and thus a relationship is formed.
ID-VGS quadratic, resulting in a linear relationship between
gm-VGS but in case of short channel device,
g does not increase linearly.

• Does □□ saturate? Why?

In the case of a short channel device, it is saturated gm at a certain value because the device reaches the speed saturation point before it reaches the interruption saturation point, thus a linear ID-VGS relationship is formed and gm is saturated. But in the case of long channel device, The gm does not saturate, but increases linearly

3. ID vs VDS

• Q: Plot *ID-VDS* characteristics for NMOS device



2) Comment on the differences between short channel and long channel results.

• Which one has higher current? Why?

Long channel devices produce higher currents compared to short channel devices due to short channel effects, particularly velocity saturation.

• Which one has higher slope in the saturation region? Why?

Short Channel devices have higher slope in saturation region as the slope of ID ,VDS is 1/ro and ro Proportionate with L , so short channel devices have lower ro which results in bigger slope