Analog IC Design – Cadence Tools
Lab 02
Common Source Amplifier

PART 1: Sizing Chart

1) We would like to design a resistive loaded CS amplifier that meets the specifications below. The design process involves selecting the sizing of the transistor (W and L), the bias point (VGS), and the resistive load (RD).

Design Specs:

DC gain = -8 and ID = 100UA

Supply =VDD= 1.8 V

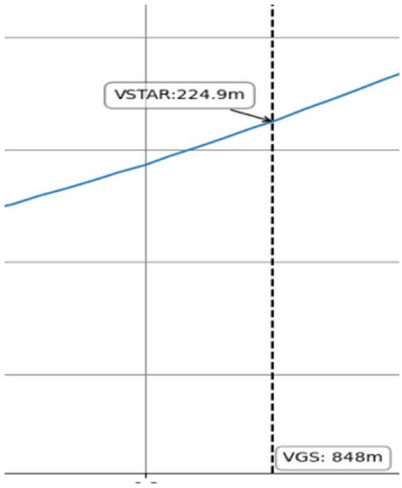
i. L = 2 μm (Because there is no speed limit in the design specification, to avoid short channel effect

ii. AV=gm*RD =2V*RD / Vov gm= 2ID/Vov This shows that the reinforcement does not depend on RD itself, but on the voltage drop across it.

iii. Formula gm= 2ID/Vov Applies only to devices that obey the square law This is not true for real MOSFETs

iv. Av= 2VRD /V' and Av and VRD are known, we can determine the required V' value as follows: According to the design specification, Av = -8 and VRD is selected as To be VDD/2 = 1.8/2= 0.9 , V* = 2*0.9/8=0.225V

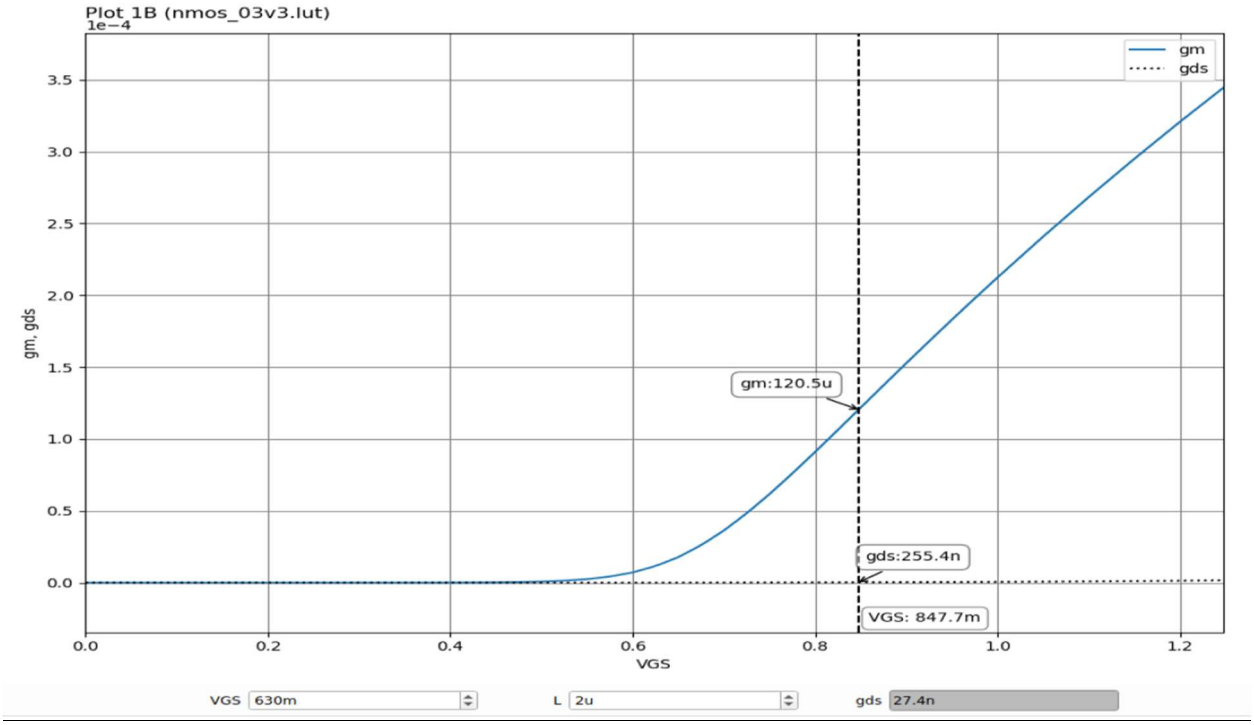
v. We use W =10u L = 2u VDS = 0.9 V and make a sweep for VGS from 0 to 0.9V with 10 mV steps and plot the ID, VGS.



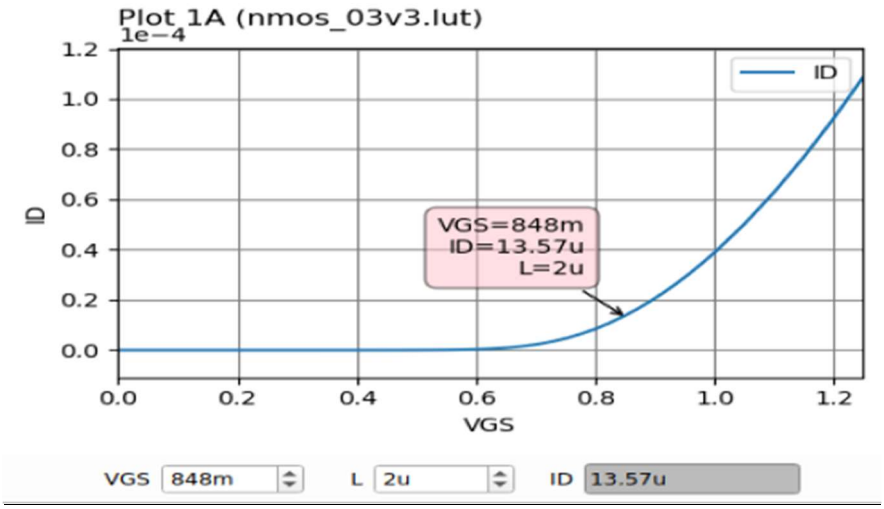
vi. Vth = 848mv >>> sweep VGS 0:(0.4+0.848) >>0:01.248.

calculated from actual simulation data using the formula.

Plot the gm & gds and carse in the VGS =848m



And ID with VGS



ID∝ (L&W) can used get the w

ID =IDQ/IDX = (W/L) Q/(W/L) X >>> LQ=LX ID=IDQ/IDX =WQ/WX

>>> WQ= (100u/13.57u) *10u = 73.69 um

And gm

gm =(100u/13.57u) *120.7u =889.46u

Plot $V*$ and Vov overlaid vs VGS. Make sure the y-axis of both curves has the same range.

VRD =VDD/2 =1.8/2=0.9 IDQ =100uA

RD = VRD/IDQ = 0.9/100*10^-6 = 9KΩ

ro= 1/gds = 1/ (255.9*10^-9) =3.9077MΩ

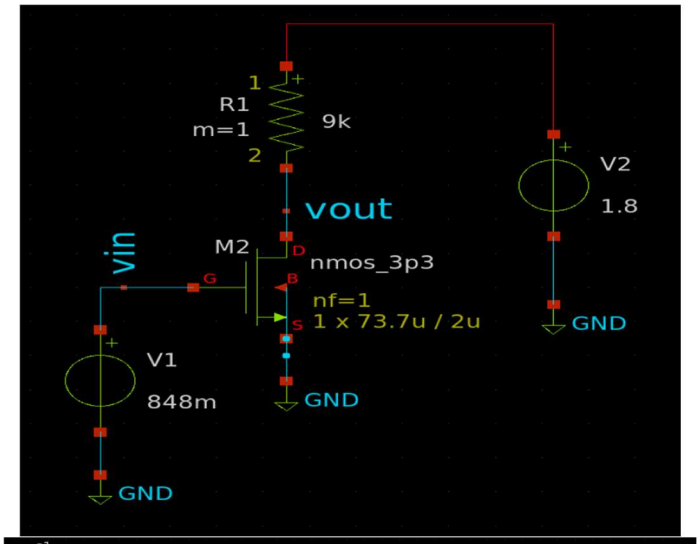
Av= -gm*(RD|| ro) = -889.46u *($\frac{RD*ro}{RD+ro}$) = -8.005 >> The error = $\frac{10-9.97}{10}$ = 19.9 %

W	73.69 um	ro	3.9077MΩ
L	2u m	RD	9KΩ
VGS	848mv	gm	889.4u
IDQ	100uA	Vov	
ID	13.57u	Vth	848m
AV	-8.005	V’	225mv

PART 2: CS Amplifier

1. OP and AC Analysis

1)Create a testbench for the resistive loaded CS amplifier using the V_{GSQ}, R_D, L, and W that you got from the previous part.

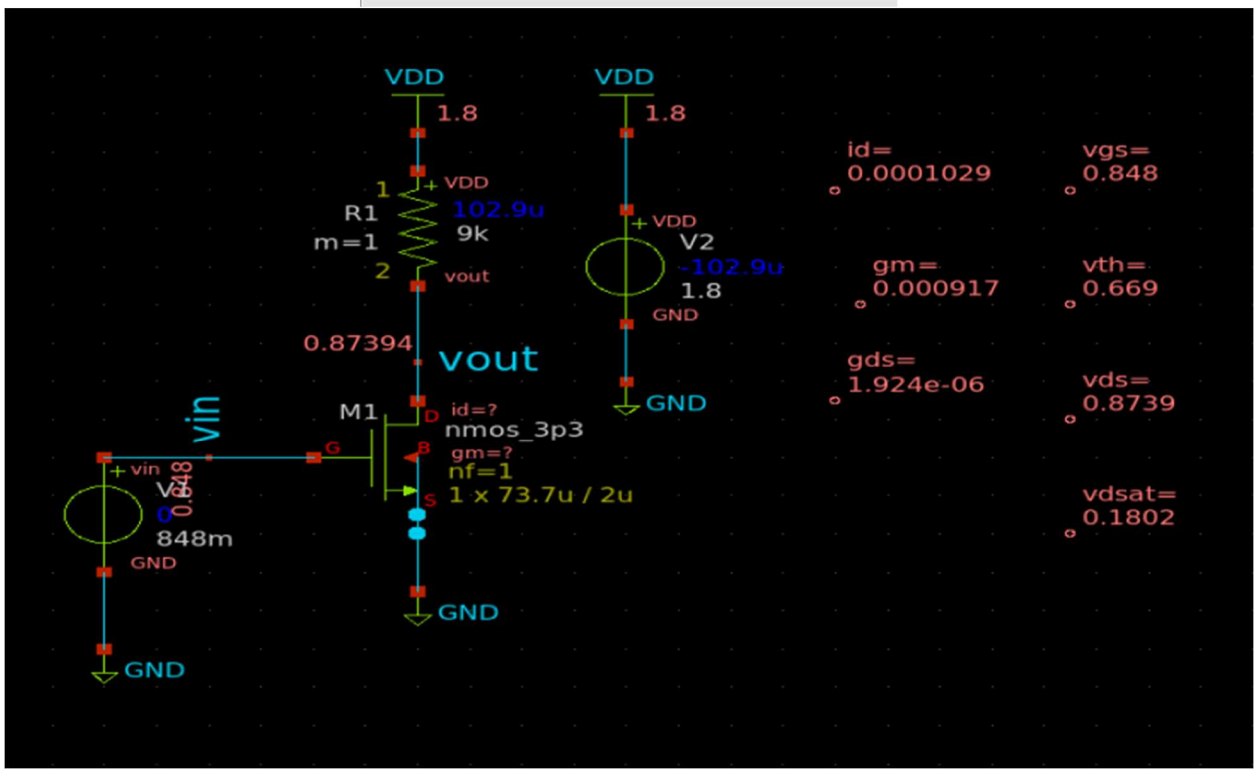



```
s1
.include /home/tare/pdk/gf180mcuC/libs.tech/ngspice/design.ngspice
.lib /home/tare/pdk/gf180mcuC/libs.tech/ngspice/sm141064.ngspice typical

s2
.control
save all
save i(@m.xm2.m0[id])
save @m.xm2.m0[gm]
save @m.xm2.m0[gds]
save v(@m.xm2.m0[vgs])
save v(@m.xm2.m0[vth])
save v(@m.xm2.m0[vds])
save v(@m.xm2.m0[vdsat])
op
let gm= @m.xm2.m0[gm]
let ro = 1/@m.xm2.m0[gds]
let Ao = gm * ro
let Av = - gm * 9000
remzerovec
write lab2.raw
show m : id : vgs : vth : vds : vdsat :gm : gds
descr=Id=
.endc
```

12) Simulate the DC OP. Report a snapshot for the key operating point (OP) parameters. Compare the results with the results you obtained in Part1.

```
Error: RHS "- gm * 9000" invalid
binary raw file "lab2.raw"
 BSIM4v5: Berkeley Short Channel IGFET Model-4
     device                m.xm1.m0
      model             nmos_3p3.14
         id             0.000102346
        vgs                0.847998
        vth                0.669554
        vds                0.878884
      vdsat                0.179757
         gm             0.000914174
        gds             1.91184e-06
```



Vgs1=vgs2 idq1=100u <idq2=102.66u gm2>gm1 gds2>gds1

Compare r_o and R_D. Is the assumption of ignoring r_o justified in this case? Do you expect the error to remain the same if we use min L?

RD is small compared to ro Parallel combinations dominate (ro||RD)
We should neglect the ro.
If we use the minimum L, we might encounter short channel effects that become more pronounced.
ID /VDS =1/ro which means ro decreases, causing the error from neglecting ro to become larger.

Calculate the intrinsic gain of the transistor

ro=1/gds	521.3764 kΩ

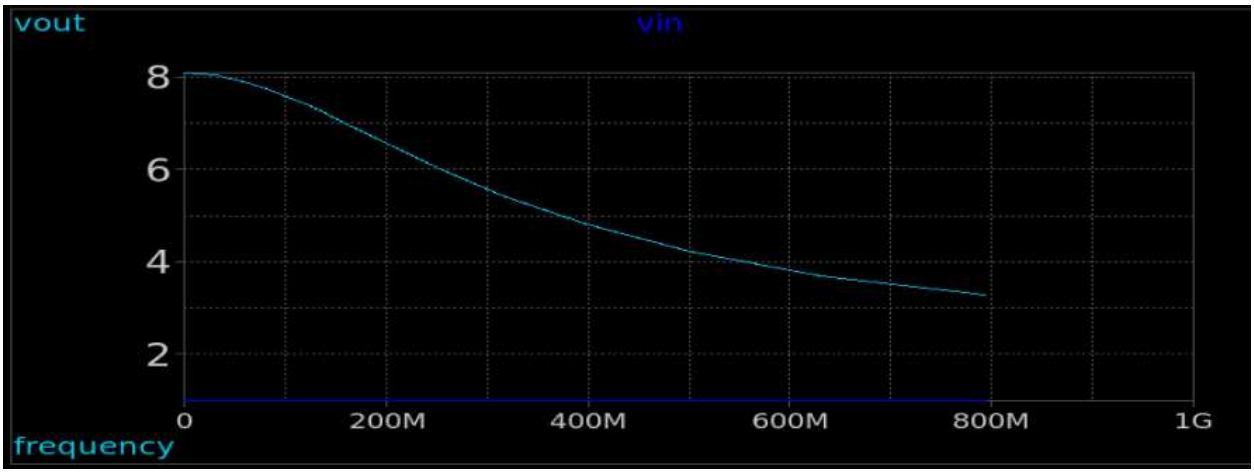
intrinsic gain = ro*gm = (914.1*10^-6) *(521.3764*10^3) =476.53

5) Calculate the amplifier gain analytically. What is the relation (≪, <, ≈, >, ≫) between the amplifier gain and the intrinsic gain?

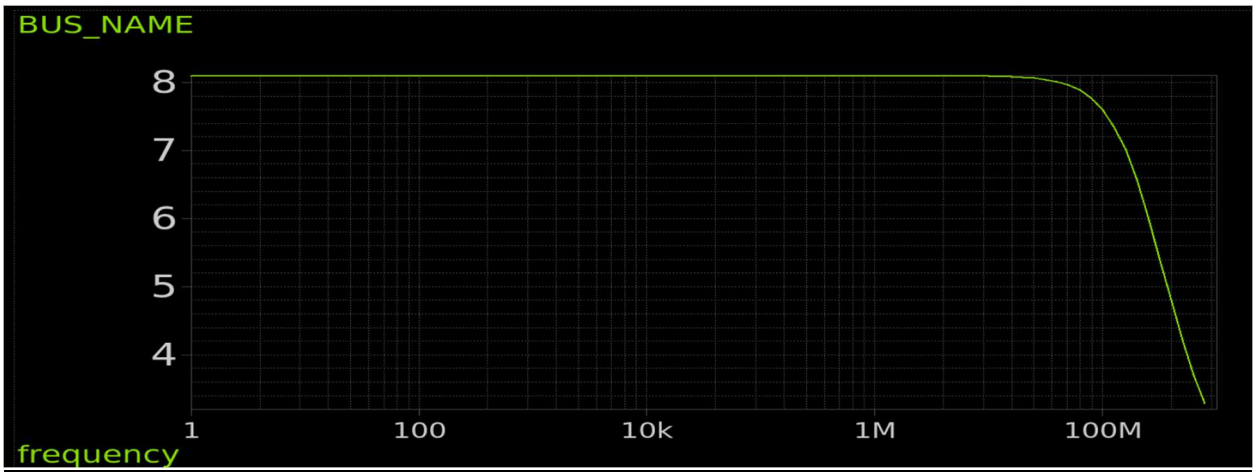
Gain of the amplifier $|Av| = gm(RD||ro) =$ 914u *($\frac{RD*ro}{RD+r}$) = 8.2

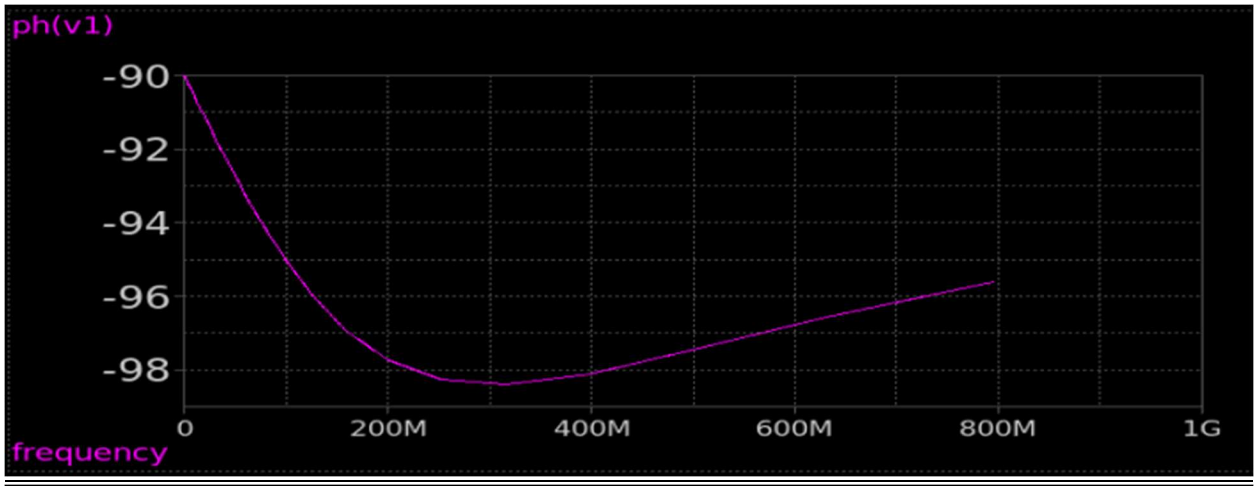
Gain of the amplifier << intrinsic gain.

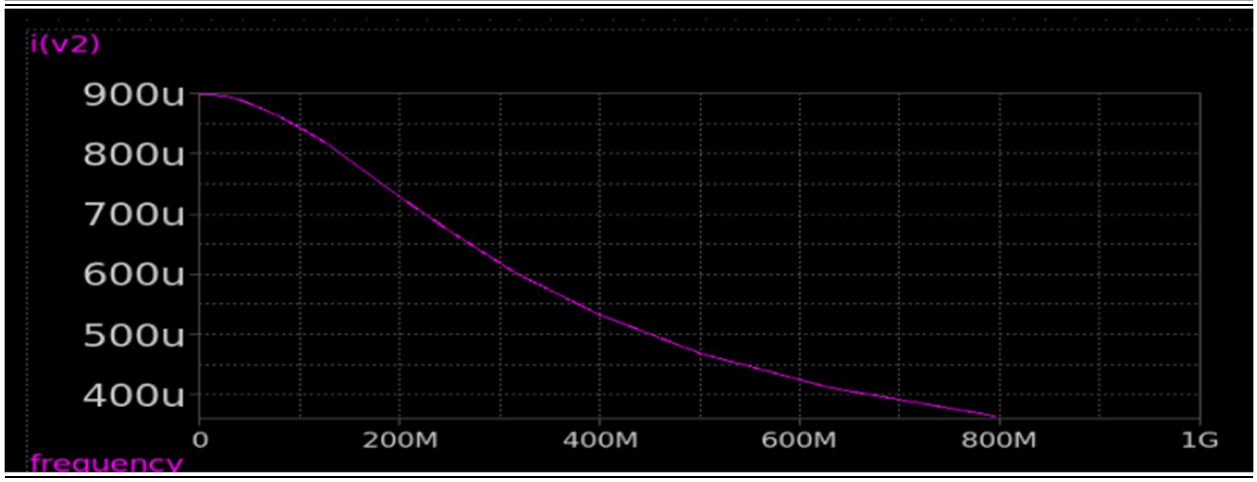
Create a new simulation configuration and run AC analysis (from 1Hz to 1GHz). Report the gain vs. frequency. Annotate the DC gain and make sure it meets the spec.



logX to vout

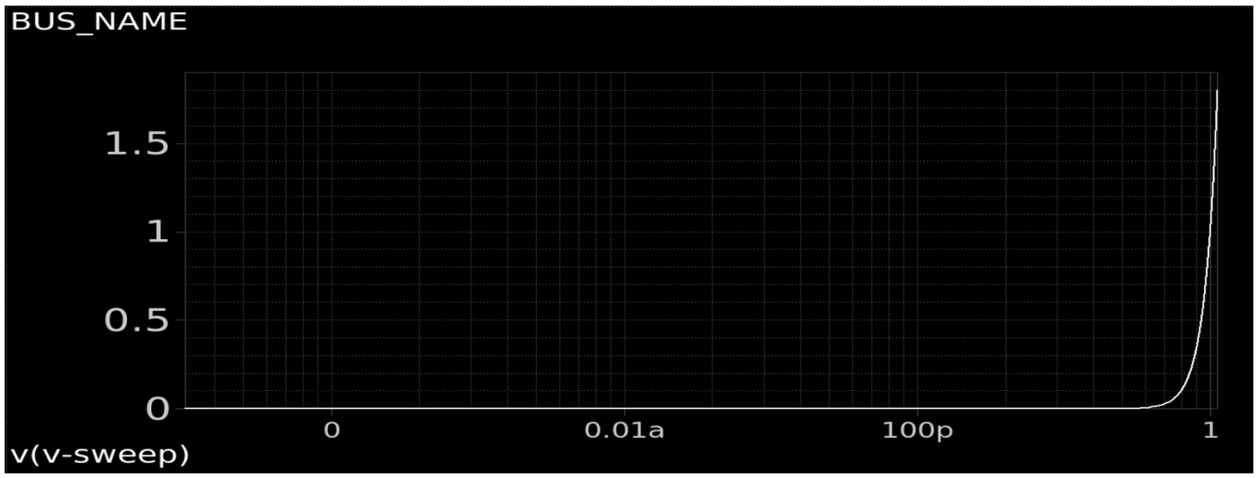






2. Gain Non-Linearity

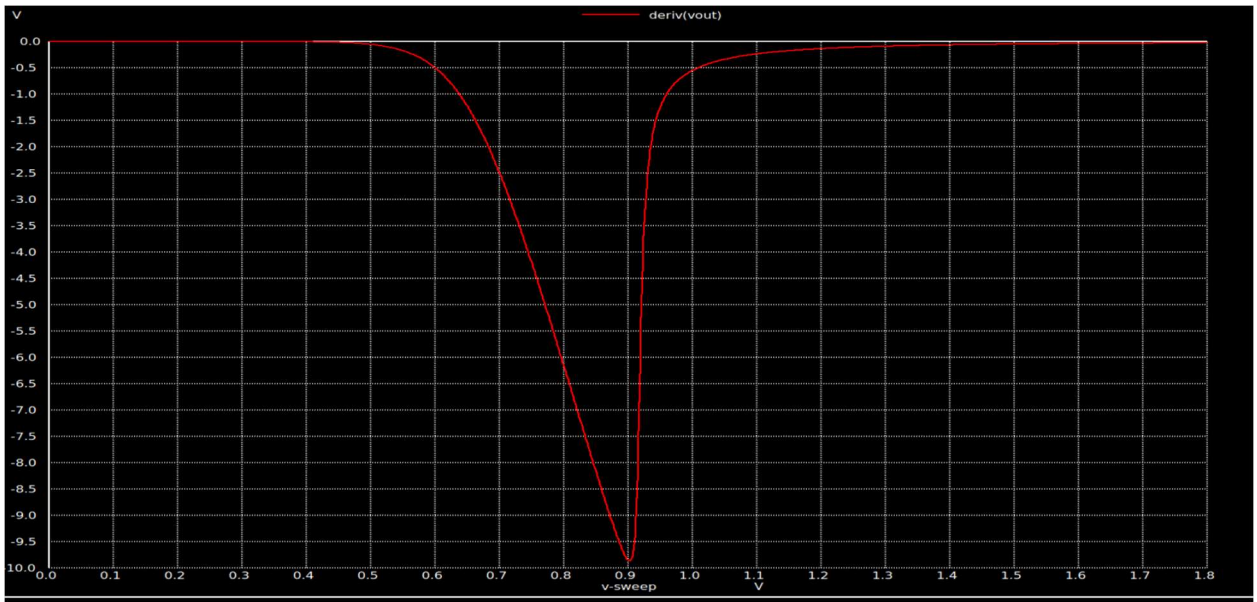
1) Create a new simulation configuration. Perform a DC sweep for the input voltage from 0 to VDD with 2mV step

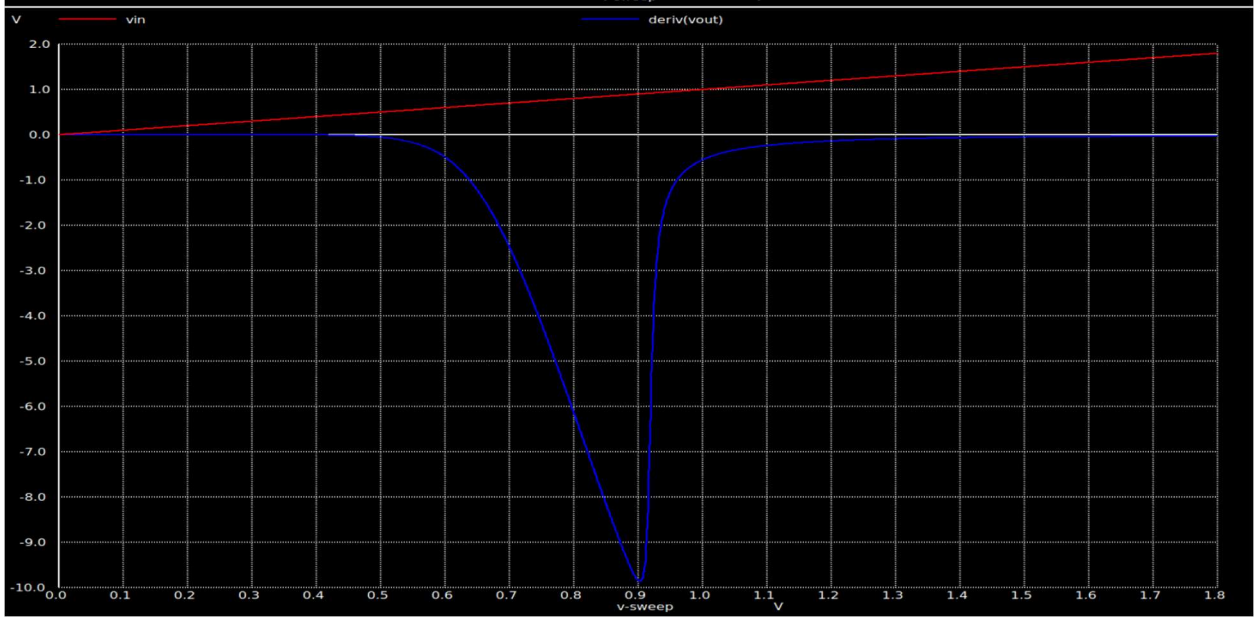


2- Report VOUT vs VIN. Is the relation linear? Why?

No, the relationship is not linear because the device is a long channel device. This makes the square law relatively applicable, resulting in the transfer characteristic being approximately square in the saturation region.

3) Calculate the derivative of VOUT using calculator. Plot the derivative vs VIN. The derivative is itself. the small signal gains. Is the gain linear (independent of the input)? Why?

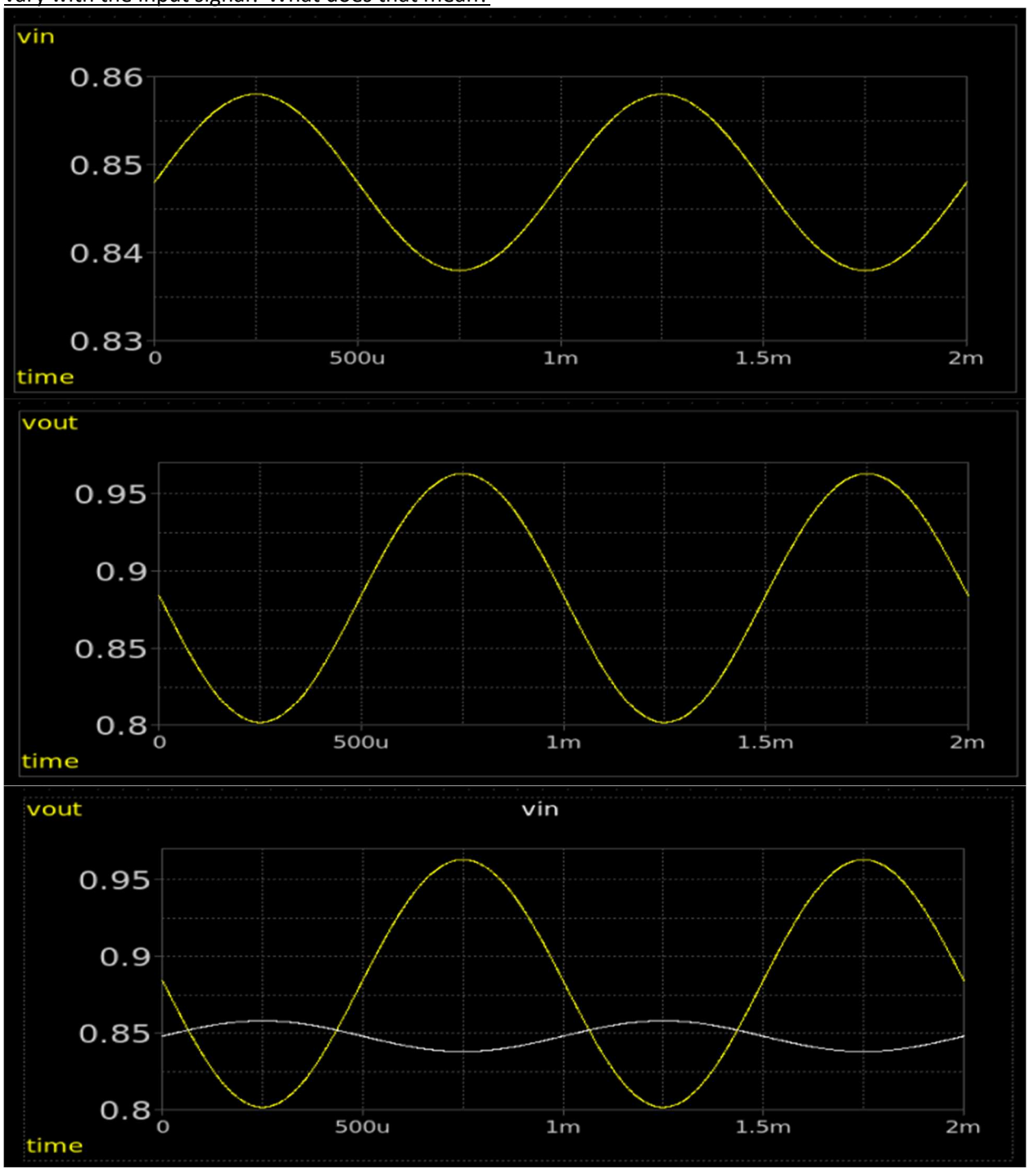


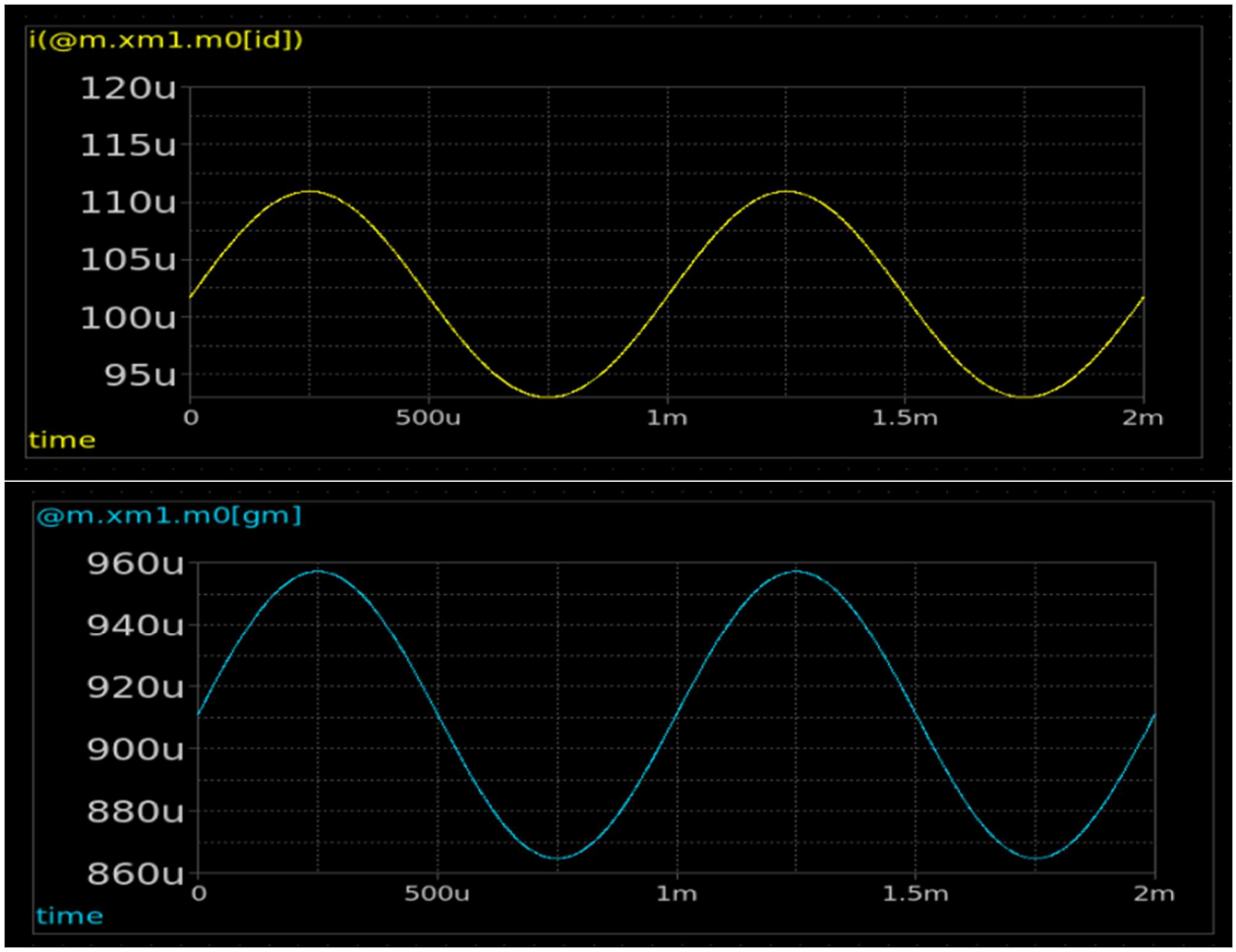


Not linear , the gain is dependent on gm & ro

4) Set the properties of the voltage source to apply a transient stimulus (sine wave of 1kHz frequency and 10mV amplitude superimposed on the DC input voltage).

5) Create a new simulation configuration. Run transient simulation for 2ms. Plot gm vs time. Does gm vary with the input signal? What does that mean?





gm varies with the input signal level because it depends on the operating point of the transistor, which can vary with different input signals. This variation affects the overall gain of the circuit, making it dependent on the signal level rather than constant.

6) Is this amplifier linear? Comment.

No
As the gain , gm , Vout
Chang by the input signal which means the gain is a function of the input signal.
the amplifier should be the output signal =input signal + Zoom level.