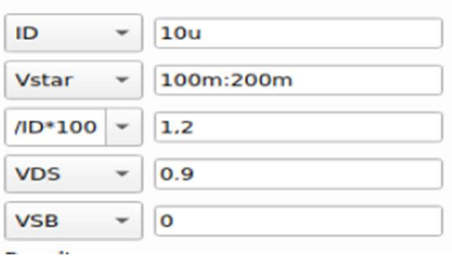
Analog IC Design – Xschem/Ngspice and ADT

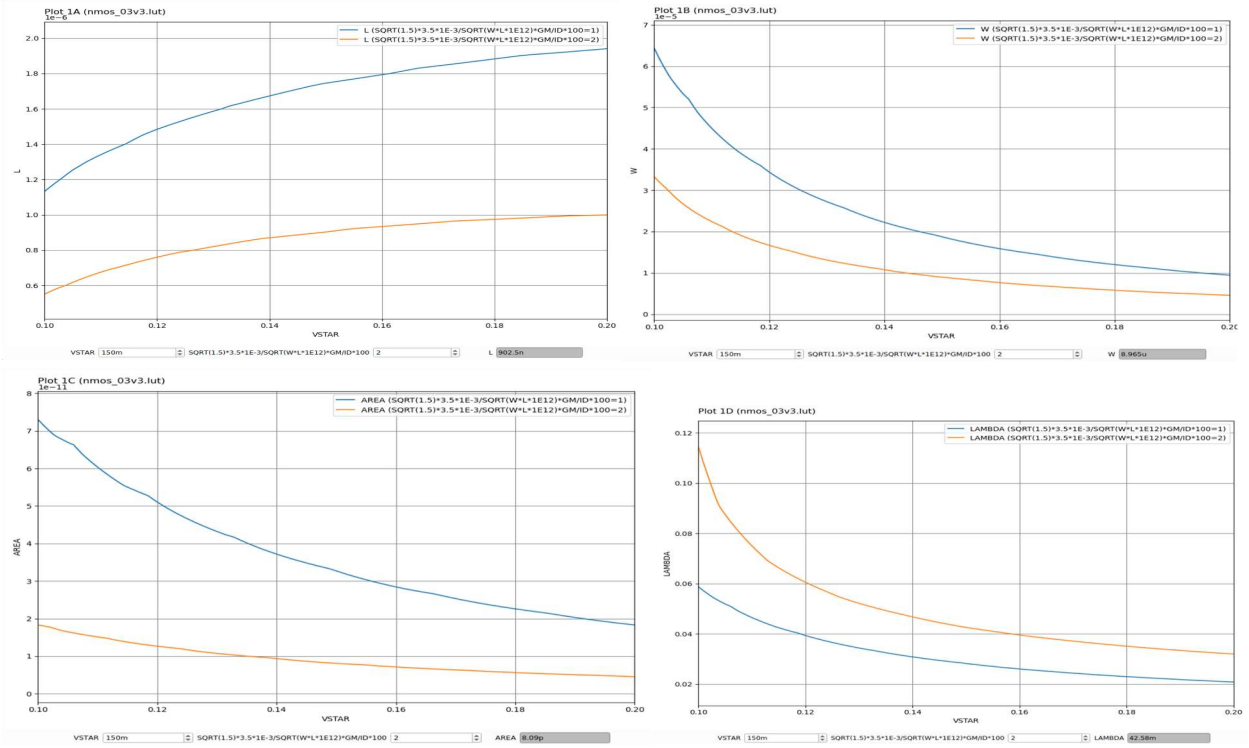
Lab 05

Simple vs Wide Swing (Low Compliance) Cascode Current Mirror

Part 1: Exploring Sizing Tradeoffs Using SA

Parameter	
Current direction (source/sink)	Sink
Input Current	$10\mu A$
Output Current	$20\mu A$
% Change in Current for $\Delta V_{out} = 1V$	$< 10\%$
Percent mismatch: $\sigma(I_{out})/I_{out}$	$\leq 2\%$
Compliance voltage	$\leq 150mV$
Area	Minimize





LAMBDA = 42.5m Iam Using 40m

ID	10u
Vstar	150m
AMBDA	40m
VDS	0.9
VSB	0

Results:

	Name	TT-27.0
1	ID	10u
2	IG	N/A
3	L	990n
4	W	9.8u
5	VGS	768.3m

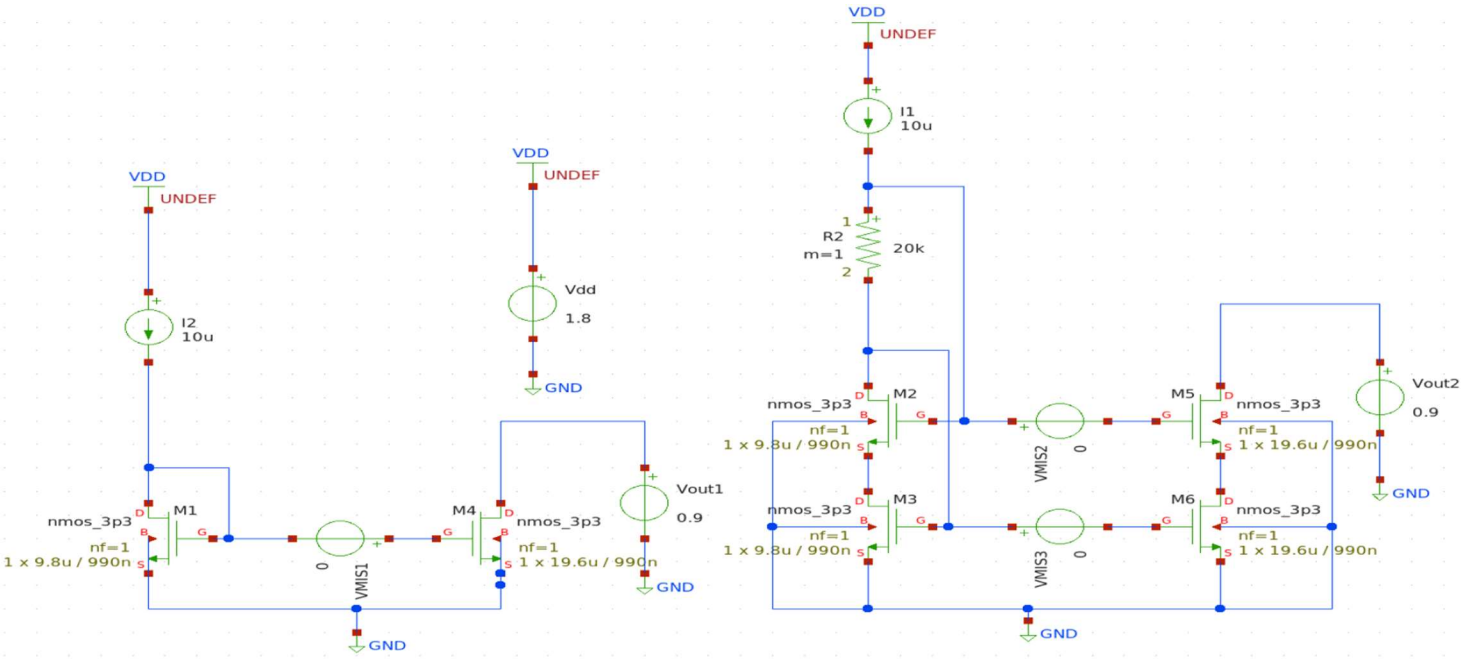
15	AREA	9.702p
16	gm	131.6u
17	gmb	50.32u
18	gds	397n
19	ro	2.519MEG
20	VTH	687.3m

Part 2: Current Mirror Simulation

$$VDS6 \approx VDS3 \approx V* + 50mV$$

$$RB = VGS5+VDS6-VGS6\ /IB \approx VDS6\ /\ IB = (150+50)\ \text{m}/10\text{u} = 20\ \text{k}$$

L= 990n W=9.8u, 2*9.8=19.6u

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No. of Data Rows : 31
Binary raw file "CM_TB_final.raw"
BSIM4v5: Berkeley Short Channel IGFET Model-4
    device              m.xm1.m0              m.xm2.m0              m.xm3.m0
     model           nmos_3p3.9            nmos_3p3.9            nmos_3p3.9
        id                 1e-05                 1e-05                 1e-05
       vgs              0.765733              0.846678              0.76935
       vds              0.765732              0.546677             0.222669
     vdsat              0.124265              0.126922             0.125793
       vth              0.688097              0.768275             0.689375
        gm         0.000134164           0.000134107          0.000133041
       gds         4.08393e-07           4.5574e-07           1.37809e-06
      gmbs         5.13466e-05           4.60414e-05          5.08999e-05

BSIM4v5: Berkeley Short Channel IGFET Model-4
    device              m.xm4.m0              m.xm5.m0              m.xm6.m0
     model          nmos_3p3.13           nmos_3p3.13           nmos_3p3.13
        id          2.00318e-05           1.99506e-05           1.99506e-05
       vgs              0.765733              0.847988              0.76935
       vds              0.899997              0.678635              0.22136
     vdsat              0.124031              0.126473             0.125626
       vth              0.688482              0.770272             0.689656
        gm         0.000268778           0.000267974          0.000265721
       gds         7.79918e-07           8.27203e-07          2.78732e-06
      gmbs         0.000102881            9.2073e-05          0.000101664
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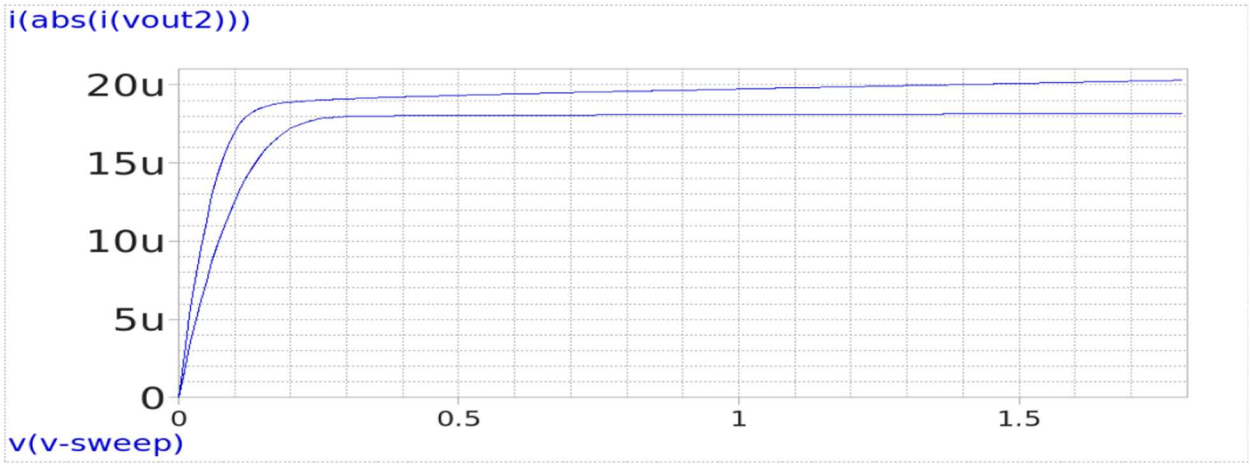


3) Simulate the OP point. Report a snapshot clearly showing the following parameters.

No. of Data Rows : 1

BSIM4v5: Berkeley Short Channel IGFET Model-4

device	m.xm1.m0	m.xm2.m0	m.xm3.m0
model	nmos_3p3.9	nmos_3p3.9	nmos_3p3.9
id	1e-05	1e-05	1e-05
vgs	0.766195	0.822332	0.771462
vds	0.766194	0.622331	0.149127
vdsat	0.124268	0.126074	0.126913
vth	0.688555	0.744225	0.689781
gm	0.000134161	0.000134118	0.000128863
gds	4.08306e-07	4.32873e-07	7.06529e-06
gmbs	5.13458e-05	4.76193e-05	4.935e-05

BSIM4v5: Berkeley Short Channel IGFET Model-4

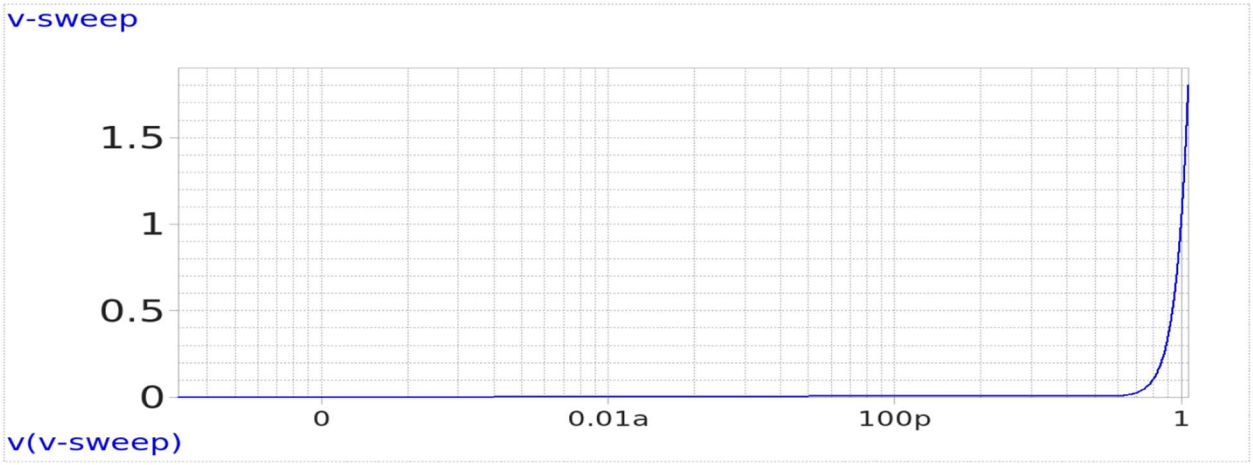
device	m.xm4.m0	m.xm5.m0	m.xm6.m0
model	nmos_3p3.13	nmos_3p3.13	nmos_3p3.13
id	2.03301e-05	2.10252e-05	2.10252e-05
vgs	0.766195	0.824504	0.771462
vds	0.899997	0.753039	0.146955
vdsat	0.124746	0.12821	0.1295
vth	0.687847	0.743162	0.685893
gm	0.000271485	0.000277645	0.000264879
gds	7.88081e-07	8.36061e-07	1.71715e-05
gmbs	0.000103916	9.86928e-05	0.000101457

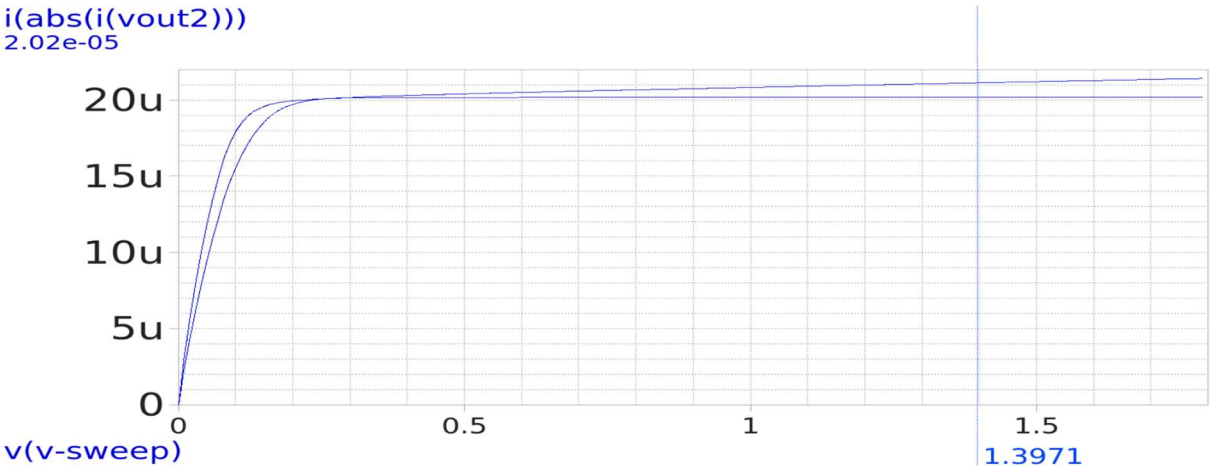
4) Do all transistors operate in saturation?

No, M3, M6 not saturation VDS > Vdsat*1.2.

2. DC Sweep (I_{out} vs VOUT)

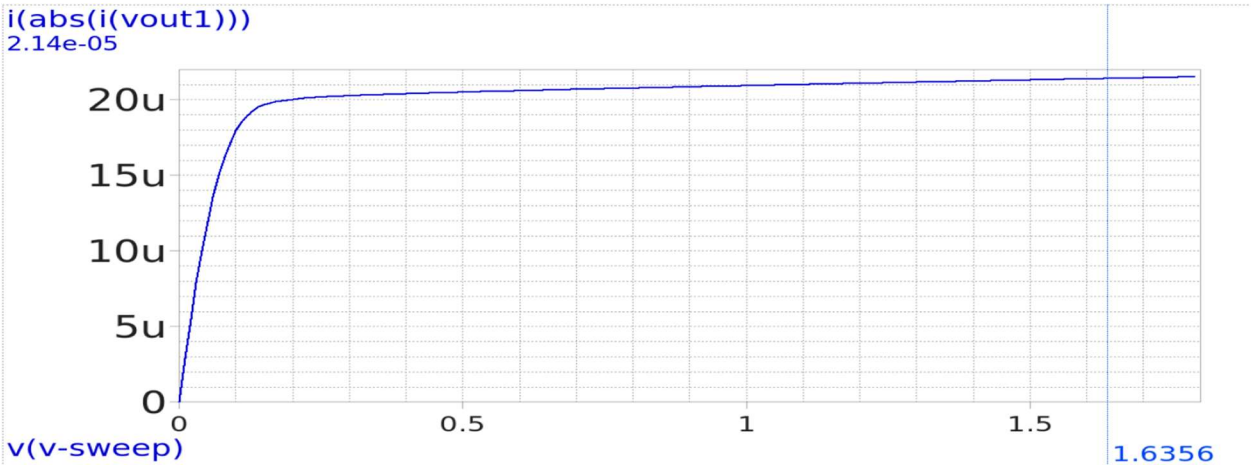
1) Perform DC sweep (not parametric sweep) using VOUT = 0:10m: VDD. Report I out vs VOUT for the two CMs overlaid in the same plot.

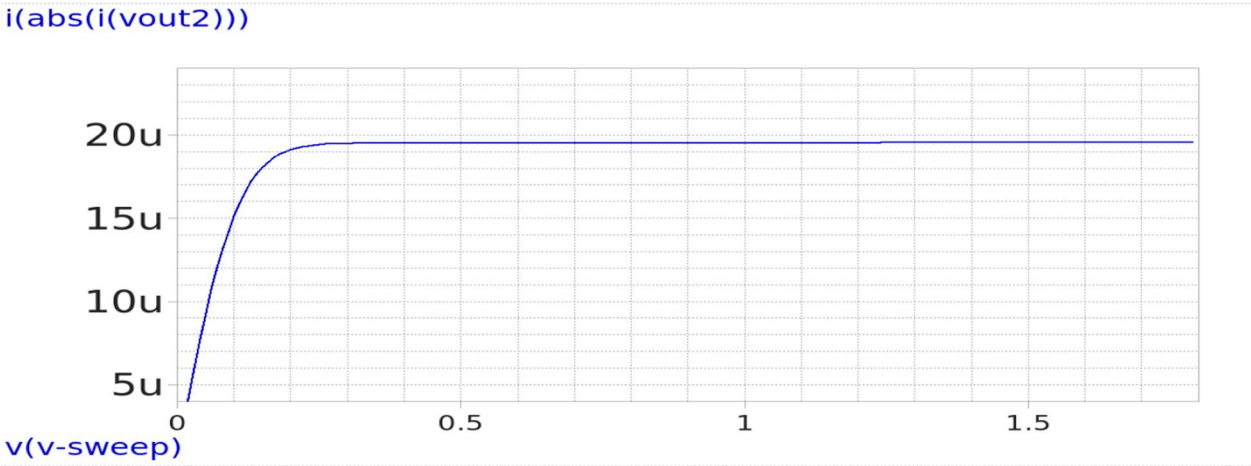




o Comment on the difference between the two circuits.

- M1 and M4 have the same VGS and both work in saturation. ▪ They will have the same current (if they are MATCHED).
- in Cascode Current Mirror Note that the mirroring action is performed by M3 and M6 only, the role of M2 and M5 is to guarantee $VDS3 = VDS6$.

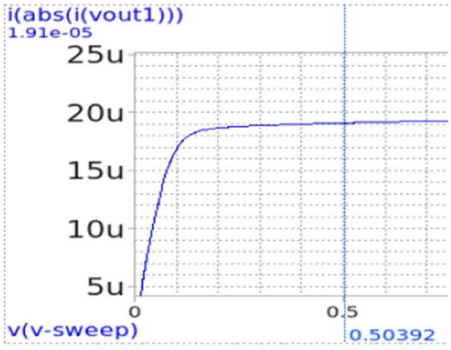




o $Iout$ of the simple CM is exactly equal to IB*2 at a specific value of VOUT. Why?

VDS of output transistor is almost equal to VDS of the mirroring transistor so the two transistors are totally matched, and the mirroring is perfect.

2) For the simple current mirror, calculate the percent change in $Iout$ when VOUT changes from 0.5V to 1.5V (i.e., 1V change). Compare the result to the value expected from Part 1



$\frac{i_{0.5}}{i_1} = \frac{1.91u}{1.95u} = 0.979 \ = 97.94\%$ the i(vout2) current is constant in the range between (0.3 to end)

Error = (100-97.94)/100 = 0.0205 =2.05%

o Comment on the difference between the two circuits.

The WS CM maintains almost 0% error in the operation region even though VOUT is changing while the Simple CM error is changing with the sweep of VOUT. (For the same reasons explained in previous comment).

No. of Data Rows : 1

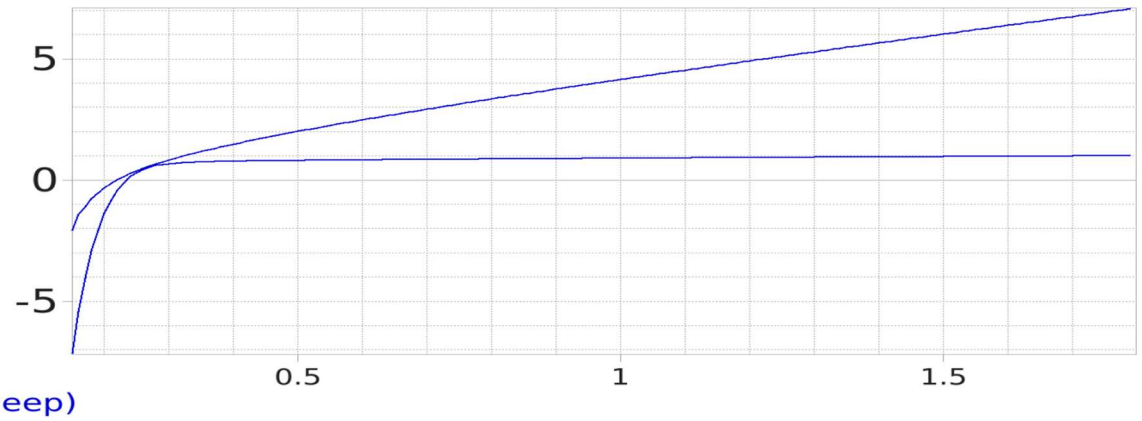
BSIM4v5: Berkeley Short Channel IGFET Model-4

device	m.xm1.m0	m.xm2.m0	m.xm3.m0
model	nmos_3p3.9	nmos_3p3.9	nmos_3p3.9
id	1e-05	1e-05	1e-05
gm	0.000134151	0.000134134	0.000128923
gds	4.08073e-07	4.33476e-07	6.995e-06
vgs	0.767443	0.820355	0.769763
vth	0.689793	0.742267	0.688118
vds	0.767442	0.620354	0.149406
gmbs	5.13436e-05	4.76168e-05	4.93708e-05

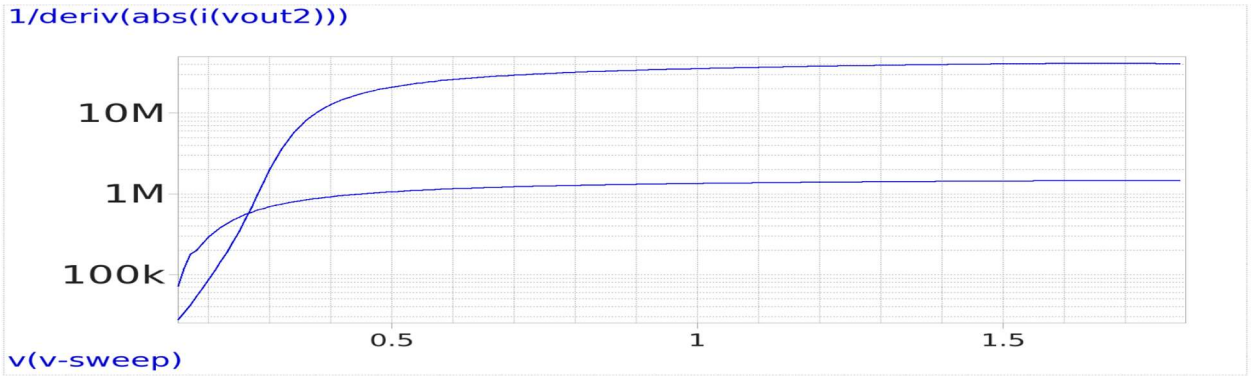
BSIM4v5: Berkeley Short Channel IGFET Model-4

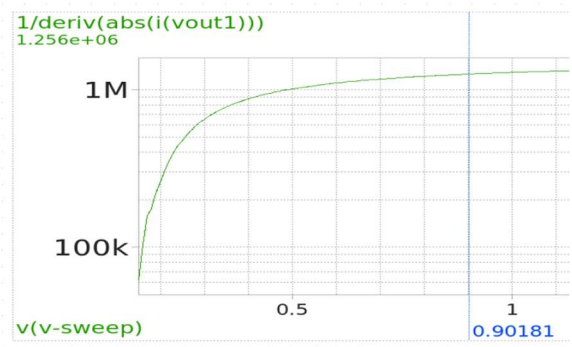
device	m.xm4.m0	m.xm5.m0	m.xm6.m0
model	nmos_3p3.13	nmos_3p3.13	nmos_3p3.13
id	2.07509e-05	2.01767e-05	2.01767e-05
gm	0.00027526	0.000270066	0.000259103
gds	7.99513e-07	8.11848e-07	1.46506e-05
vgs	0.767443	0.821129	0.769763
vth	0.687559	0.74289	0.687514
vds	0.899997	0.751363	0.148631
gmbs	0.00010536	9.5923e-05	9.92284e-05

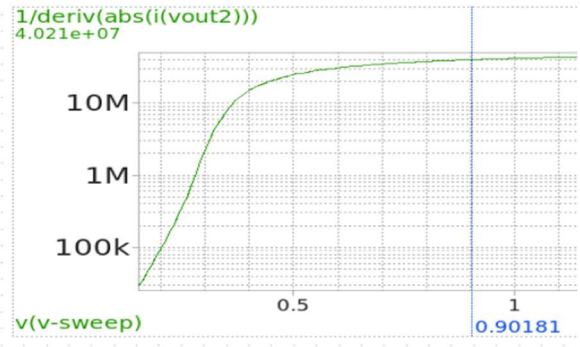
(abs(i(vout2))-20u)*100/20u



4) Report Rout vs VOUT (take the inverse of the derivative of I_{out} plot) for the two CMs in the current mirror operating region (VOUT ≈ $V_*$to VDD) overlaid in the same plot. Use log scale on the y-axis. Add a cursor at VOUT = VDD/2.







- **Comment on the difference between the two circuits.**

WS CM has very high output impedance compared to the SIMPLE CM.

- **Does Rout change with VOUT? Why?**

Yes, Increasing Vout decreases VDS of the output transistor which decreases Rout, hence decreasing the output impedance.

5) Analytically calculate Rout of both circuits at VOUT = VDD/2. Compare with simulation results in a table.

at $Vout = V_{DD}/2$, $RoutWS = (g_{m5}+g_{mb5})/(g_{ds5}*g_{ds6}) = 78.22\text{M}\,\Omega$
at $Vout = V_{DD}/2$, $RoutSimple = 1/g_{ds4} = 2.56\text{M}\Omega$

	Analytically	simulation
RoutSimple	2.56M Ω	1.25M Ω
RoutWS	78.22M Ω	40.2M Ω

The numbers coming out of the simulation contain errors and do not match the numbers coming out of the calculations.

3. Mismatch

1) Perform DC sweep for VMIS1 and VMIS2 from 0 to sqrt (1.5)*3.5m/sqrt(W*L*1e12) using the code below and set VMIS3 = 0. This models the standard deviation of the mismatch in V_{TH} for the current mirror devices. Find the percent change in I_{out}.

simple current mirror

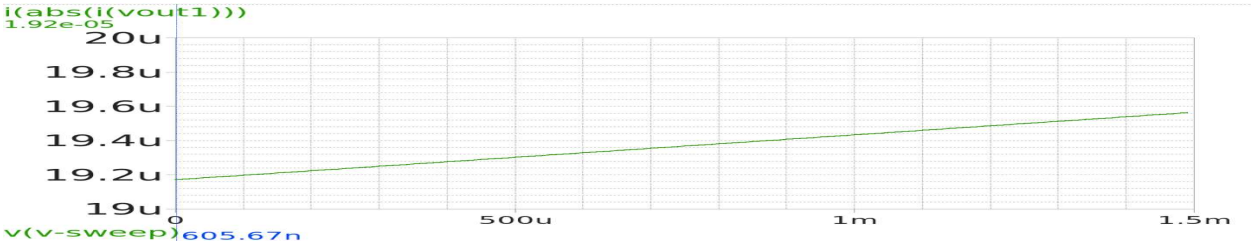
No. of Data Rows : 1

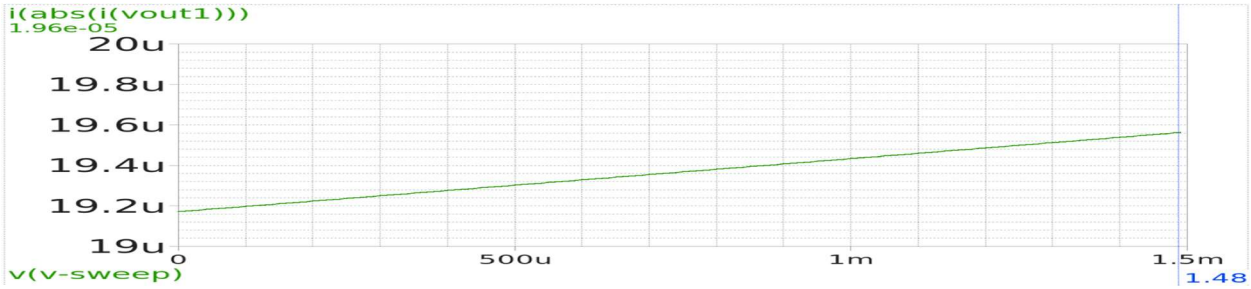
BSIM4v5: Berkeley Short Channel IGFET Model-4

device	m.xm1.m0	m.xm2.m0	m.xm3.m0
model	nmos_3p3.9	nmos_3p3.9	nmos_3p3.9
id	1e-05	1e-05	1e-05
vgs	0.767822	0.822108	0.768943
vdsat	0.124277	0.126058	0.126977
vth	0.690168	0.743995	0.687163
vds	0.767821	0.622107	0.146833
gm	0.000134149	0.00013413	0.000128494
gds	4.08002e-07	4.33044e-07	7.65136e-06
gmbs	5.13429e-05	4.76693e-05	4.9211e-05

BSIM4v5: Berkeley Short Channel IGFET Model-4

device	m.xm4.m0	m.xm5.m0	m.xm6.m0
model	nmos_3p3.13	nmos_3p3.13	nmos_3p3.13
id	1.95561e-05	1.99315e-05	1.99315e-05
vgs	0.767822	0.820115	0.768943
vdsat	0.122904	0.125572	0.126672
vth	0.692312	0.74279	0.687653
vds	0.899997	0.751169	0.148825
gm	0.000264379	0.000267846	0.000257271
gds	7.66728e-07	8.04716e-07	1.4131e-05
gmbs	0.000101205	9.51257e-05	9.85229e-05





Wide swing CM

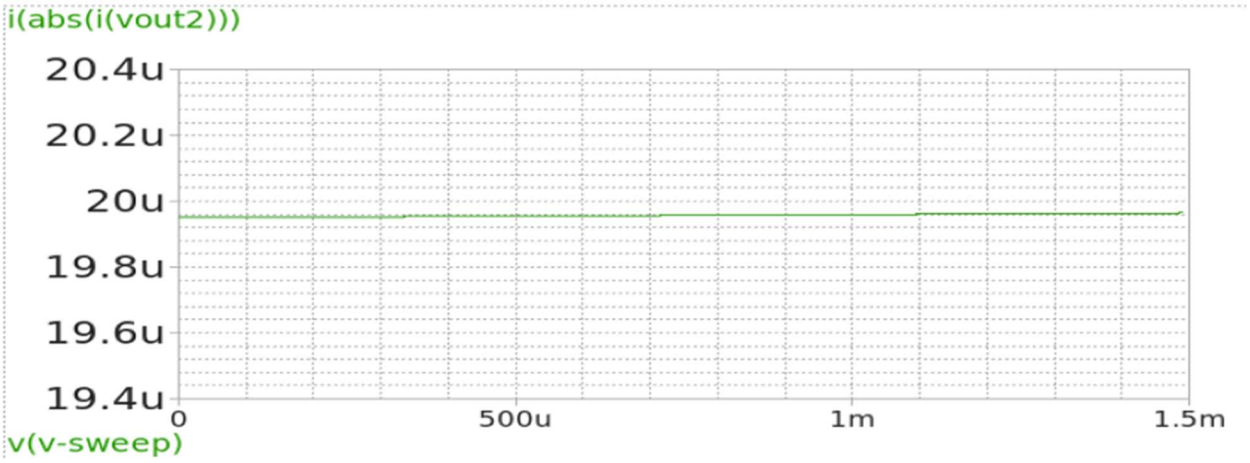
No. of Data Rows : 1

BSIM4v5: Berkeley Short Channel IGFET Model-4

device	m.xm1.m0	m.xm2.m0	m.xm3.m0
model	nmos_3p3.9	nmos_3p3.9	nmos_3p3.9
id	1e-05	1e-05	1e-05
vgs	0.767647	0.821386	0.769033
vdsat	0.124276	0.126058	0.126947
vth	0.689995	0.743282	0.687299
vds	0.767646	0.621385	0.147645
gm	0.00013415	0.00013412 1	0.000128635
gds	4.08035e-07	4.33233e-07	7.43595e-06
gmbs	5.13433e-05	4.7653e-05	4.92635e-05

BSIM4v5: Berkeley Short Channel IGFET Model-4

device	m.xm4.m0	m.xm5.m0	m.xm6.m0
model	nmos_3p3.13	nmos_3p3.13	nmos_3p3.13
id	2.07283e-05	1.97239e-05	1.97239e-05
vgs	0.767647	0.822271	0.769033
vdsat	0.125698	0.12507	0.126223
vth	0.687842	0.745685	0.688428
vds	0.899997	0.753235	0.14676
gm	0.000275054	0.000265893	0.000254951
gds	7.9889e-07	7.97966e-07	1.48151e-05
gmbs	0.000105282	9.45314e-05	9.76423e-05



2) Analytically calculate the percent change in I_{out} and compare it to the simulation result.

Percent Change = $\frac{i2-i1}{i1}$ = $\frac{19.6u-19.2u}{19.2u}$ = 2.08%

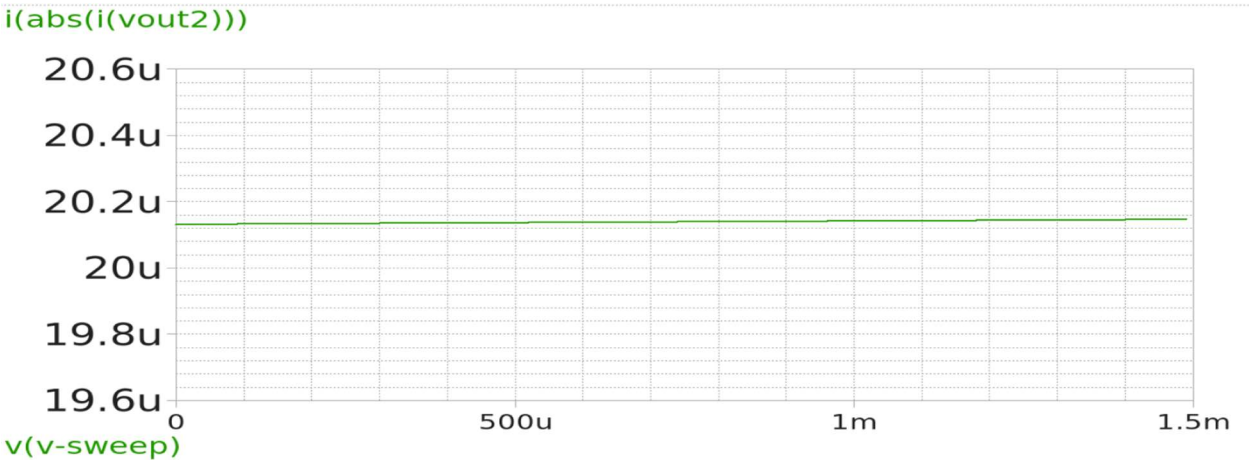
No. of Data Rows : 1

BSIM4v5: Berkeley Short Channel IGFET Model-4

device	m.xm1.m0	m.xm2.m0	m.xm3.m0
model	nmos_3p3.9	nmos_3p3.9	nmos_3p3.9
id	1e-05	1e-05	1e-05
vgs	0.764885	0.822633	0.771921
vdsat	0.12426	0.126077	0.126911
vth	0.687256	0.744524	0.690243
vds	0.764883	0.622632	0.149285
gm	0.00013417	0.000134116	0.000128884
gds	4.08552e-07	4.32773e-07	7.02755e-06
gmbs	5.13481e-05	4.76154e-05	4.93585e-05

BSIM4v5: Berkeley Short Channel IGFET Model-4

device	m.xm4.m0	m.xm5.m0	m.xm6.m0
model	nmos_3p3.13	nmos_3p3.13	nmos_3p3.13
id	1.98638e-05	2.01469e-05	2.01469e-05
vgs	0.764885	0.823293	0.771921
vdsat	0.123622	0.126119	0.127247
vth	0.688263	0.745136	0.68976
vds	0.899997	0.75137	0.148625
gm	0.000267254	0.000269759	0.000258831
gds	7.75325e-07	8.1089e-07	1.46087e-05
gmbs	0.000102297	9.58183e-05	9.91286e-05



5) Which mismatch contribution is more pronounced? Why?

The mismatch is more noticeable in small devices due to its new effect on operations. Therefore, larger devices are used in analog circuits to improve the matching and mismatches.

6) Which design decision is better: setting the same W and L for the mirror and cascode devices? Or using larger W and L for the current mirror devices? Why?

- Using the same W and L for reflectors and cascodes simplifies the design and improves matching,
- While larger W and L for reflectors improves matching performance and copy accuracy but consumes more space.
- The choice depends on the application requirements, balance and space.