Part 1: Sizing Chart Using ADT SA

Design Specs:

1. PMOS Device
2. $L = 1\ \mu m$
3. Supply = $1.8\ V$
4. Current = $10\ \mu A$

Parameters needed:

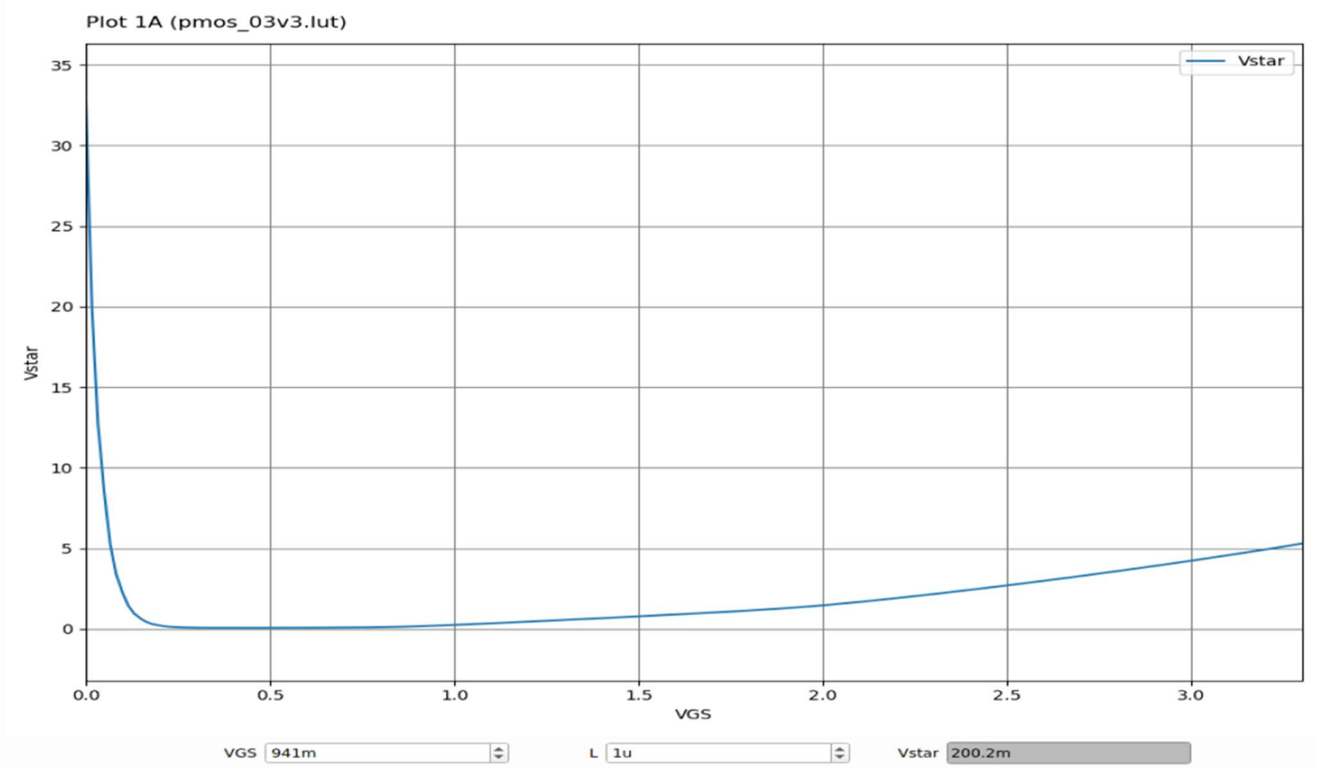
1. Sizing (W & L)
2. Bias Point (VGS)
3. Small signal parameters (gm, gds)

Given information:

1. $L = 1\ \mu m$
2. $|Av| \approx gmro = 2/\lambda Vov$ (knowing that $gm = 2Vov\ ID$, it's shown that the gain doesn't depend on ro itself but the early voltage.)
3. The formula $gm = 2ID/Vov$ is valid only for devices obeying square law which isn't the case for real MOSFETs.
4. We introduce a new parameter called V-star ($V*$) such that $V* = 2ID/gm$.
5. For a real MOSFET the gain is given by $|Av| \approx 2/\lambda V*$.
6. $V*$ is chosen to be $200\ mV$.

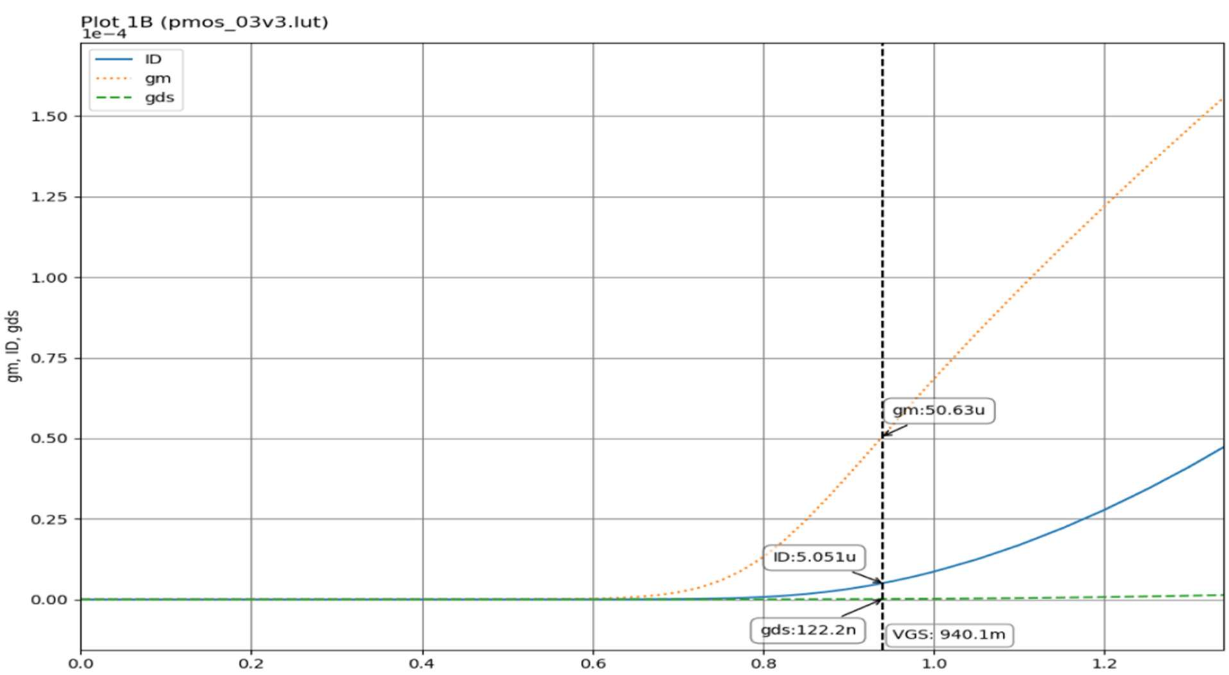
Design steps:

1. We use $W = 10\ \mu m$ & $L = 1\ \mu m$ & $VDS = 0.9\ V$ and get the VGS in the $V* = 200mV$
2. Using the values we make another sweep for VGS from 0 to $0.4 + VTH$ with $10\ mV$ steps.
3. Plot ID, gm, and gds vs VGS.
4. Find their values at $VGSQ$. Let's name these values IDX, gmX, and $gdsX$.



Vgs=941mv	The sweep 0:10m:(vth+0.4)	0:10m:1.32

Plot ID, gm, and gds vs VGS.



Find their values at $VGSQ$. Let's name these values IDX, gmX, and $gdsX$.

IDQ = 10uA   IDX = 5.051uA

1. calculate gmQ and $gdsQ$ using ratio and proportion (cross multiplication).

$$\text{ID}=\frac{IDQ}{IDX}=\frac{(gm)_Q}{(gm)_X} \quad >> \quad gm_Q=\frac{50.63u\ *\ 10u}{5.051u}=100.25\text{u}$$

$$\text{ID}=\frac{IDQ}{IDX}=\frac{(gds)_Q}{(gds)_X} \quad >> \quad gds_Q=\frac{122.2n\ *\ 10u}{5.051n}=241.98\text{ n}$$

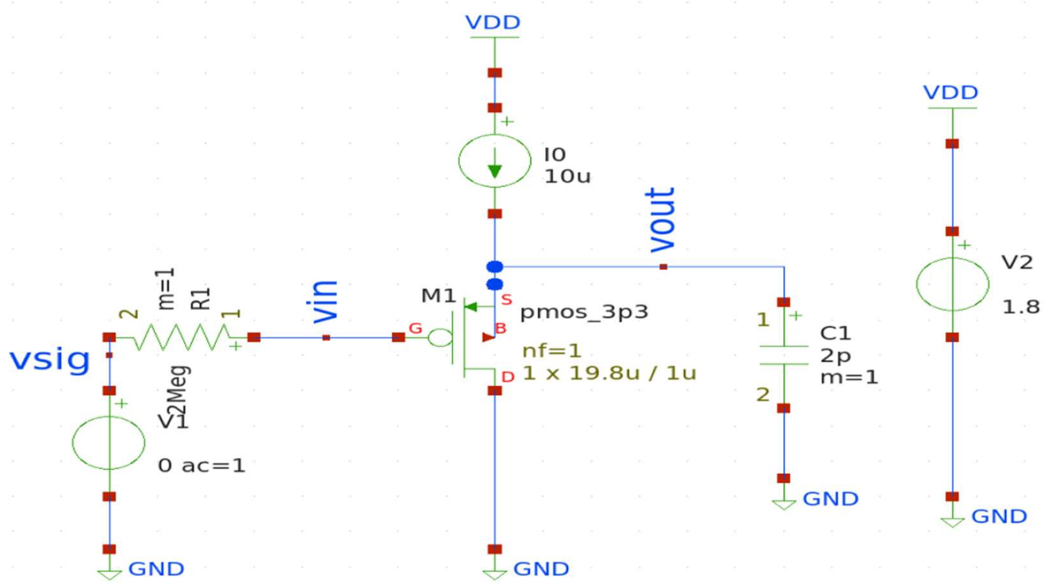
$$\text{ID}=\frac{IDQ}{IDX}=\frac{(\frac{W}{L})_Q}{(\frac{W}{Q})_X} \quad >> \text{LQ=LX} \qquad \text{WQ}=\frac{10u\ *\ 10u}{5.051n}=19.801\text{u}$$

$$ro = 1/gds = 4.132\ \text{M}\Omega$$

Parameter	value
W	19.801u
L	1u
Vgs	940.1mv
gm	100.25u
ro	4.132 MΩ

Part 2: CD Amplifier

1. OP (Operating Point) Analysis



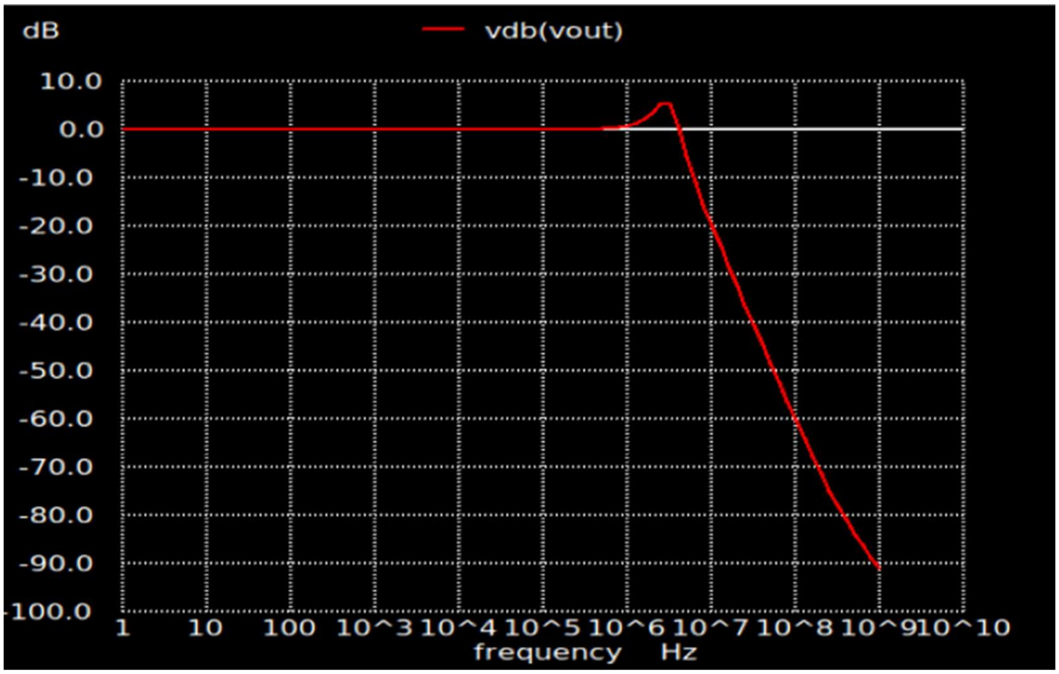

```
No. of Data Rows : 1
binary raw file "lab4.raw"
 BSIM4v5: Berkeley Short Channel IGFET Model-4
        device                  m.xm1.m0
         model                pmos_3p3.13
            gm               0.000101537
           gds                2.2985e-07
            id                     1e-05
           vgs                  0.940426
           vth                  0.784047
           vds                  0.940426
         vdsat                  0.153611
          gmbs               4.79819e-05
           cdb              -9.87145e-15
           cgd              -1.41519e-17
           cgs              -5.06278e-14
           csb              -1.47829e-14
```

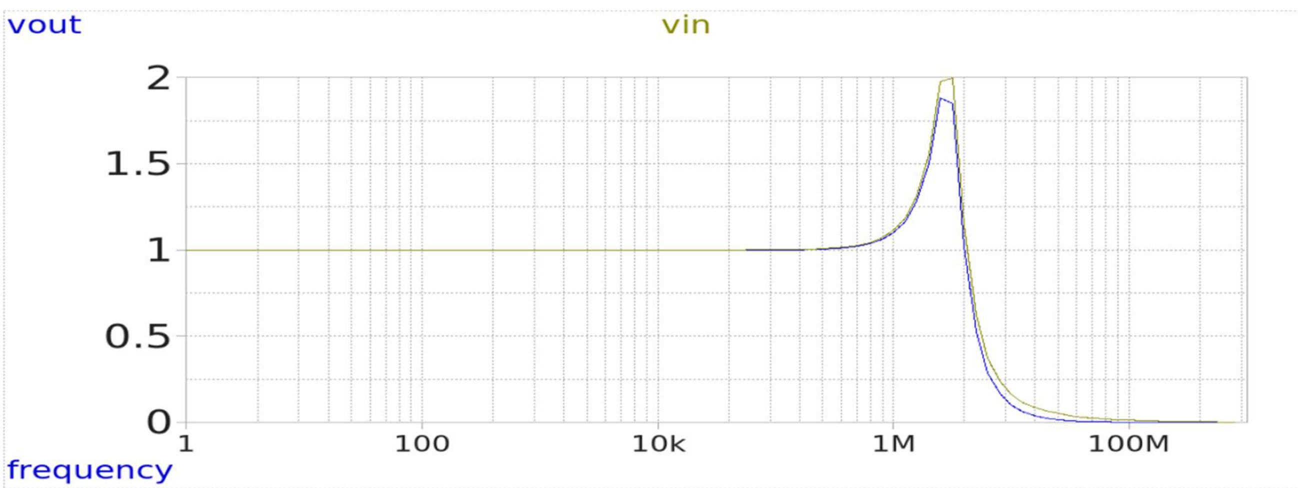
Id=. 1e-05	vgs=. 0.9419	vds=. 0.9419	vdsat=. 0.1536	vth=. 0.7855
gm=. 0.0001015	gds=. 2.295e-07	gmbs=. 4.797e-05		

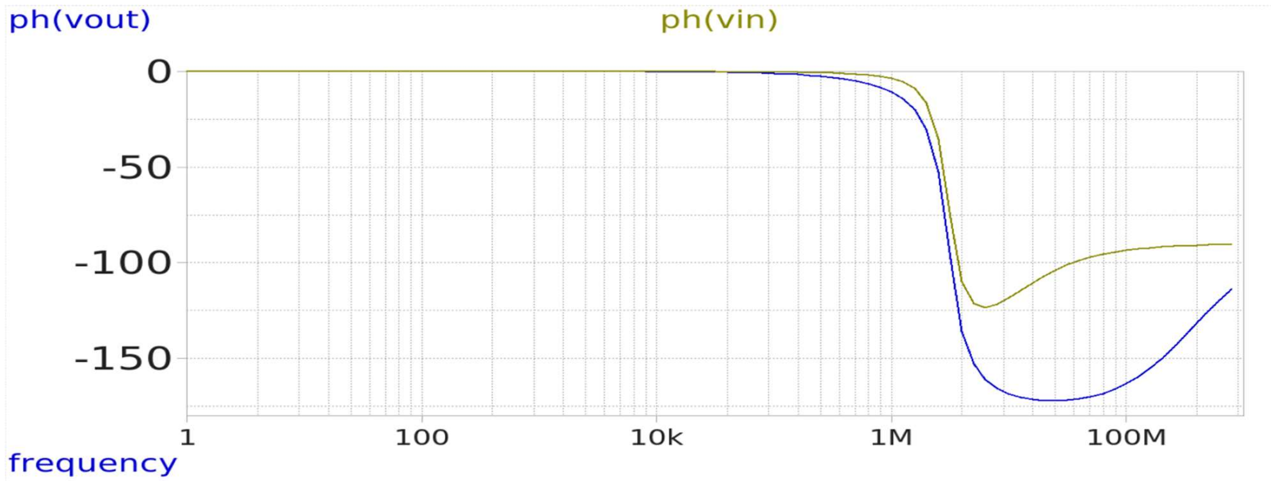
3) Check that the transistor operates in saturation.

Yes : the transistor in saturation vds >> vdsat

2. AC Analysis







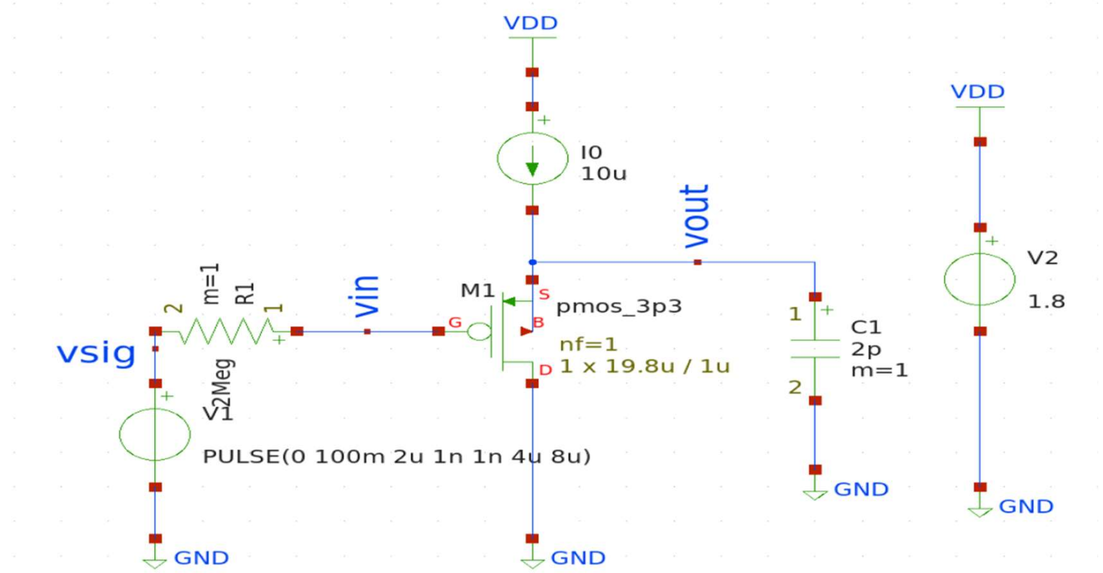
2) Do you notice frequency domain peaking?

Yes, there's a peaking in the frequency domain as shown in the previous plot, its value is 5.487 dB as evaluated in simulation.

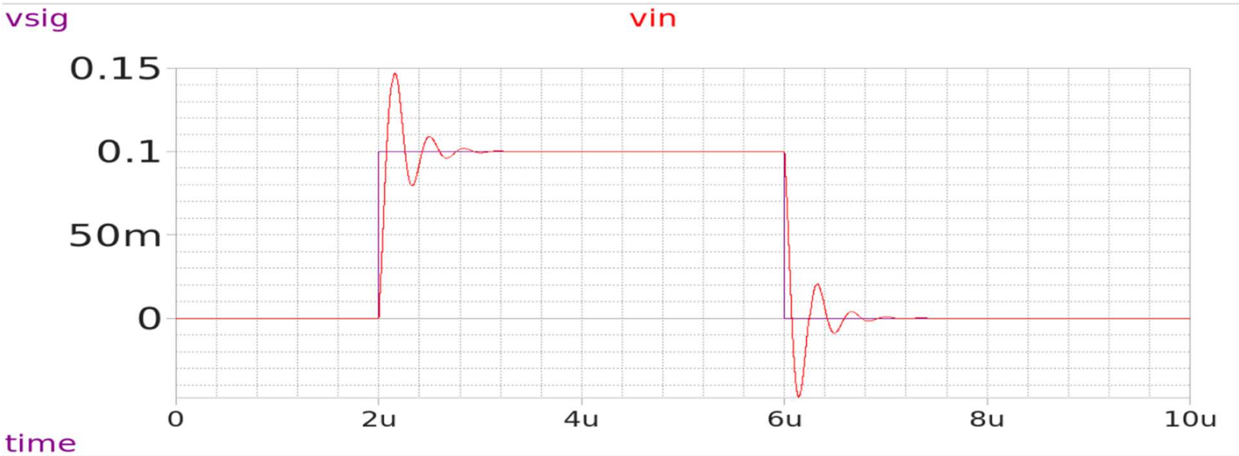
3) Analytically calculate quality factor (use approximate expressions). Is the system underdamped or overdamped?

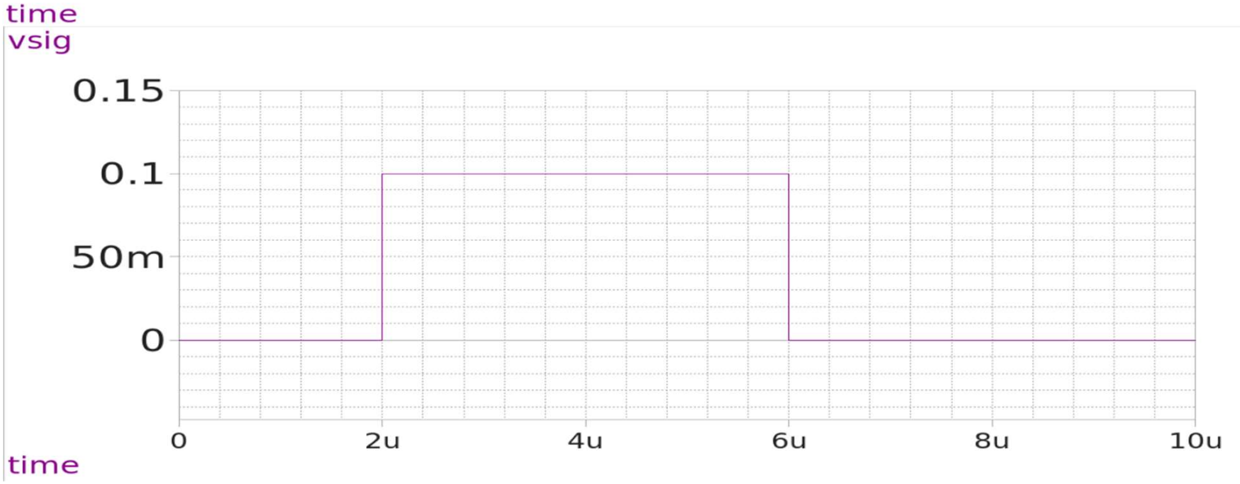
$$Q \approx \sqrt{\frac{g_m(C_{gs}+C_{gd})R_{sig}}{Cl}} = 2.266 > 0.5, \text{ system is underdamped.}$$

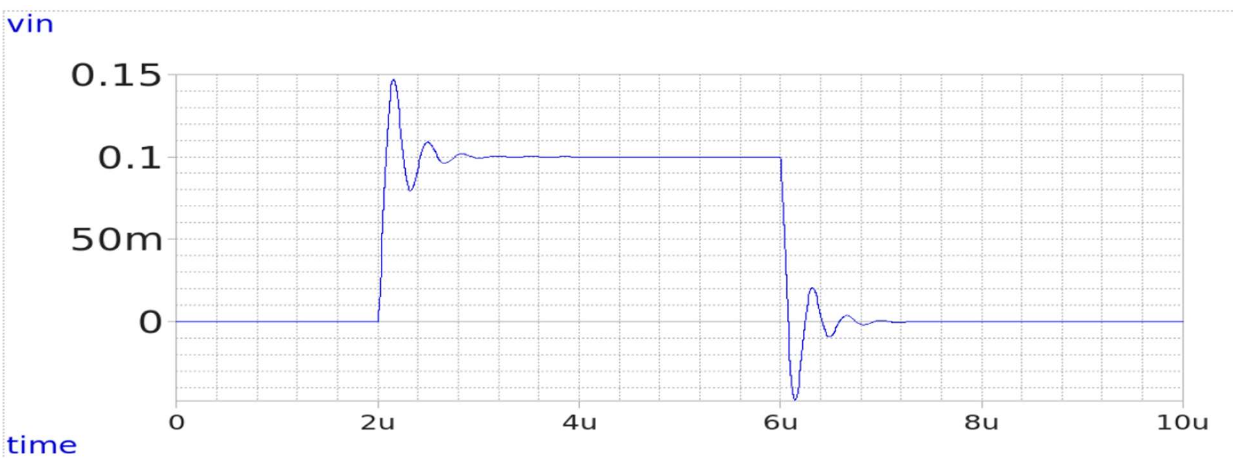
3. Transient Analysis

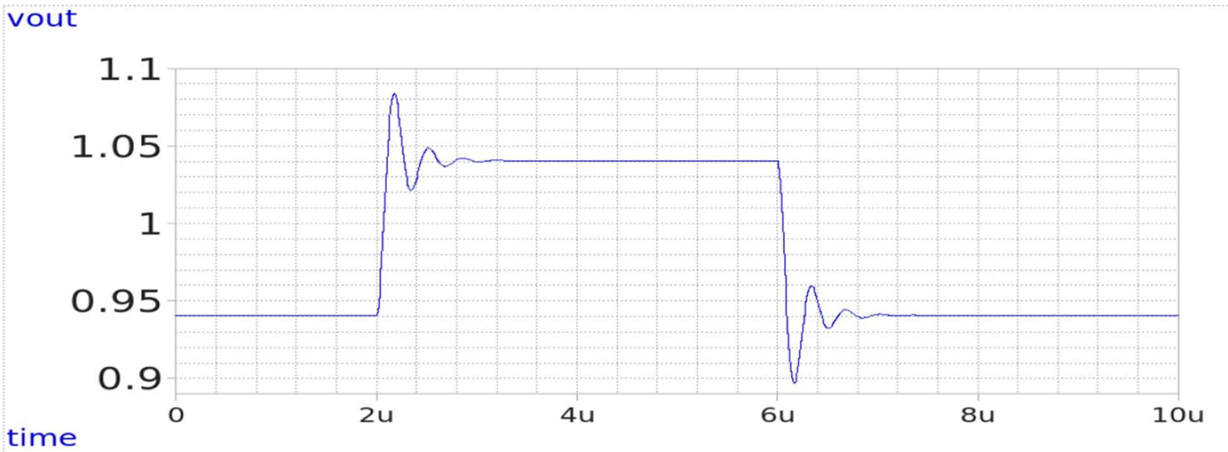



```
Initial Transient Solution
--------------------------

Node                                   Voltage
----                                   -------
vin                                          0
vout                                  0.938728
net1                                         0
vdd                                        1.8
v2#branch                               -1e-05
v1#branch                                    0


No. of Data Rows : 1028
peak1               =  1.081701e+00 at=  2.181160e-06
overshoot           =  4.602157e+00 at=  5.141160e-06
binary raw file "lab4_tran.raw"
ngspice 1 ->
```


vsig
vin
0.15
0.1
50m
0
0
2u
4u
6u
8u
10u
time


vsig
0.15
0.1
50m
0
0
2u
4u
6u
8u
10u
time


vin
0.15
0.1
50m
0
0
2u
4u
6u
8u
10u
time



<u>2) Calculate the DC voltage difference (DC shift) between Vin and Vout.</u>

DC shift $= 0.938V$

```
vin                                   0
vout                           0.938728
```

<u>• What is the relation between the DC shift and VGS of the transistor?</u>

DC shift $\approx VGS$.

```
vgs                  0.940426
```

<u>• How to shift the signal down instead of shifting it up?</u>

To make the shift down instead of up we should use NMOS device instead of PMOS device.

<u>3) Do you notice time domain ringing? How much is the overshot?</u>

Yes, there's domain ringing and its value is.

$$\frac{max-top}{top-mean} * 100 \quad = \frac{1.084- \ .041}{1.041-0.941} * 100 = 43\%$$

as evaluated from simulation.

```
overshoot              =  4.602157e+00 at=  5.141160e-06
```