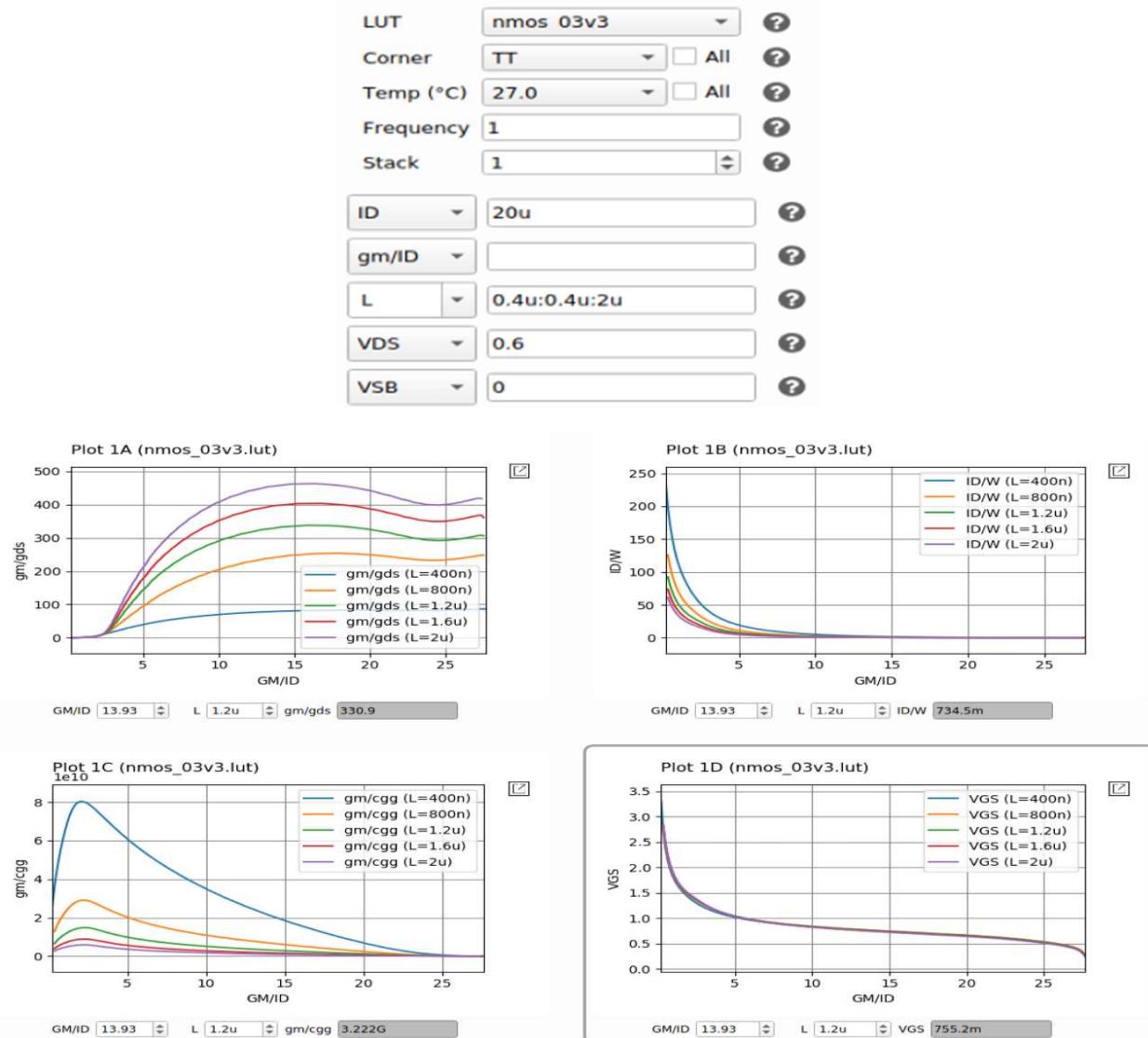


Analog IC Design – Xschem/Ngspice

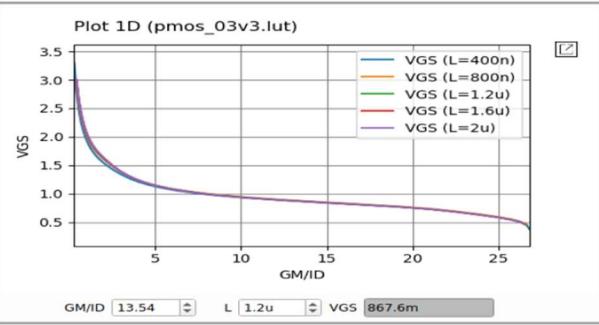
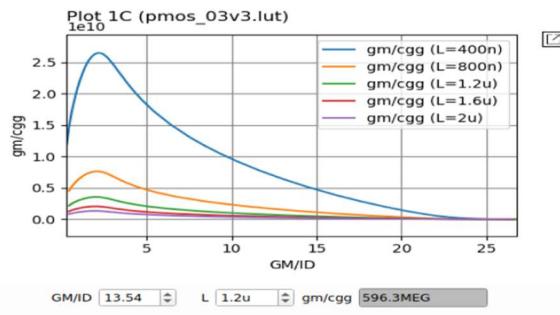
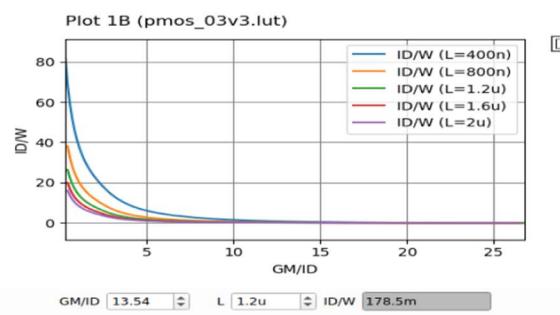
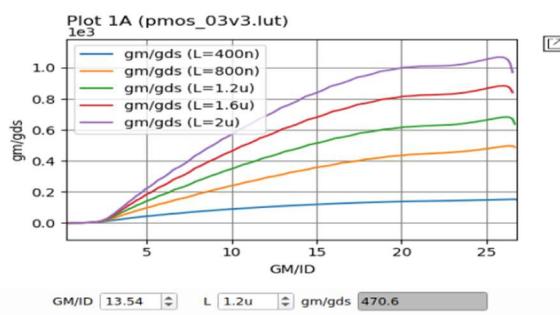
Lab 07

Gm/ID Design Methodology

PART 1: gm/ID design charts



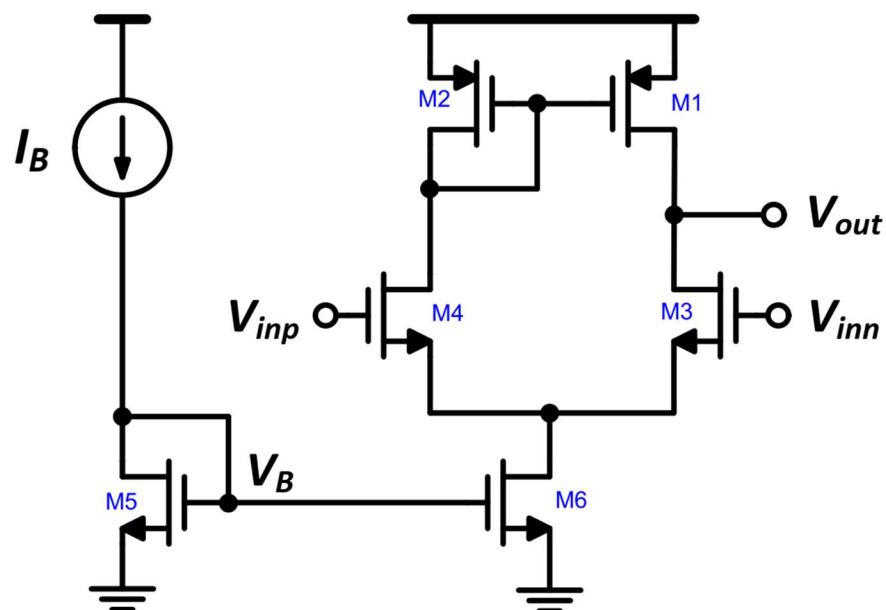
LUT	pmos_03v3	<input type="button" value="?"/>
Corner	TT	<input type="checkbox"/> All <input type="button" value="?"/>
Temp (°C)	27.0	<input type="checkbox"/> All <input type="button" value="?"/>
Frequency	1	<input type="button" value="?"/>
Stack	1	<input type="button" value="?"/>
ID	20u	<input type="button" value="?"/>
gm/ID		<input type="button" value="?"/>
L	0.4u:0.4u:2u	<input type="button" value="?"/>
VDS	0.6	<input type="button" value="?"/>
VSB	0	<input type="button" value="?"/>



Part 2: OTA Design

Use gm/ID methodology to design a diff input SE output operational transconductance amplifier (OTA) that achieves the following specs. Use an ideal external 10uA DC current source in your test bench (not included in the OTA current consumption spec).

Technology	0.13 um CMOS	0.18 um CMOS
Supply Voltage	1.2V	1.8V
Load	5pF	5pF
Open Loop DC Voltage Gain	$\geq 34\text{dB}$	$\geq 34\text{dB}$
CMRR @ DC	$\geq 74\text{dB}$	$\geq 74\text{dB}$
Phase Margin	$\geq 70^\circ$	$\geq 70^\circ$
CM input range - low	$\leq 0.6\text{V}$	$\leq 1\text{V}$
CM input range - high	$\geq 1\text{V}$	$\geq 1.5\text{V}$
GBW	$\geq 10\text{MHz}$	$\geq 10\text{MHz}$



Input pair

$$GBW = gm/2\pi CL \rightarrow gm=10M*2\pi*5pF = 314.15u$$

Assume $\rightarrow gm/ID = 15 \rightarrow ID = 314.15/15 = 20.93uA$

Voltage Gain $\geq 34dB = gm*ro / 2$ $gm/gds > 2*50 > 100$

LUT	nmos 03v3		1	ID	21	11	gm/gds	97.42
Corner	TT	All	2	IG	N/A	12	VA	6.651
Temp (°C)	27.0	All	3	L	440n	13	ID/W	1.506
Frequency	1		4	W	13.94	14	gm/W	22.06
Stack	1		5	VGS	835.6m	15	AREA	6.134u
ID	21		6	VDS	600m	16	gm	307.6
gm/ID	15		7	VSB	300m	17	gmb	87.04
gm/gds	100		8	gm/ID	14.65	18	gds	3.157
VDS	0.6		9	Vstar	136.5m	19	ro	316.7m
VSB	0.3		10	fT	2.686G	20	VTH	792.8m

I needed to increase w to get $\rightarrow gbw \approx 10M$

Load

$$Gm*ro = 100 \rightarrow ro = 318.31k \rightarrow gds = 3.14u \rightarrow ID = 21u$$

Assume $\rightarrow gm/ID = 10 \rightarrow gm = 210u \rightarrow gm/gds = 66.87$

LUT	pmos 03v3		1	ID	21u	11	gm/gds	61.35
Corner	TT	All	2	IG	N/A	12	VA	6.22
Temp (°C)	27.0	All	3	L	320n	13	ID/W	2.117
Frequency	1		4	W	9.92u	14	gm/W	20.88
Stack	1		5	VGS	904.5m	15	AREA	3.174p
ID	21u		6	VDS	900m	16	gm	207.1u
gm/ID	10		7	VSB	0	17	gmb	75.26u
gm/gds	66.87		8	gm/ID	9.863	18	gds	3.376u
VDS	0.9		9	Vstar	202.8m	19	ro	296.2k
VSB	0		10	fT	2.47G	20	VTH	751.4m

taill

$$ID^*2 = ID \rightarrow \text{tail} = 42\mu\text{A}$$

Assume L = 1u, gm/ID = 10

LUT	nmos 03v3					
Corner	TT	All				
Temp (°C)	27.0	All				
Frequency	1					
Stack	1					
ID	42u					
gm/ID	10					
L	1u					
VDS	0.3					
VSB	0					
1	ID	42u		11	gm/gds	99.59
2	IG	N/A		12	VA	10.08
3	L	1u		13	ID/W	2.146
4	W	19.57u		14	gm/W	21.19
5	VGS	835.9m		15	AREA	19.57p
6	VDS	300m		16	gm	414.8u
7	VSB	0		17	gmb	158.4u
8	gm/ID	9.875		18	gds	4.165u
9	Vstar	202.5m		19	ro	240.1k
10	fT	1.124G		20	VTH	687m

ID in M5=10u and needed 42u in M6

W in M6 = 19.57u $\rightarrow \approx 40$ u

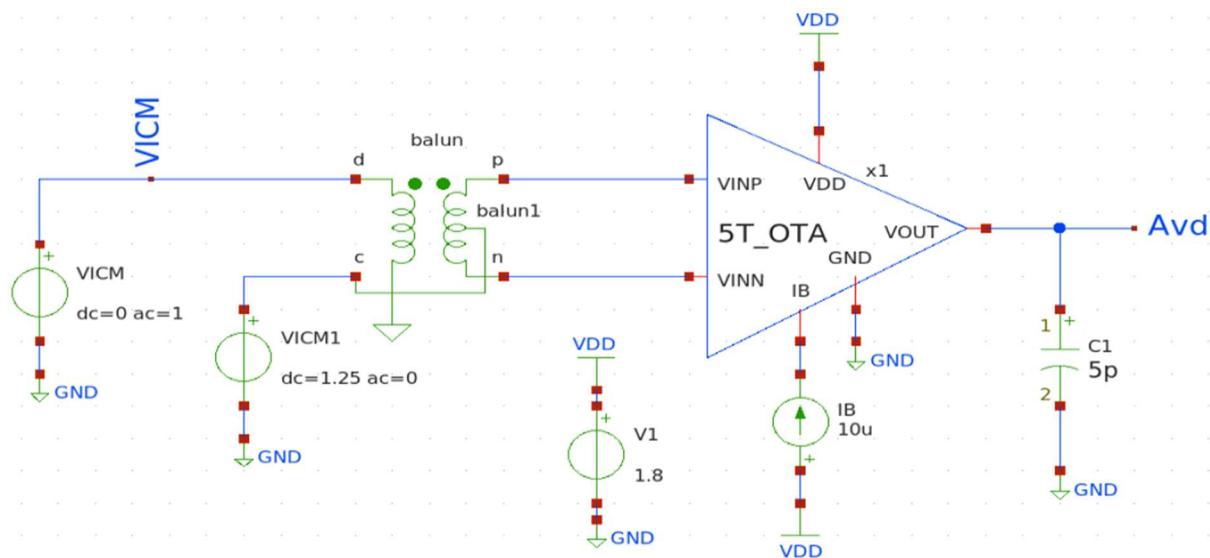
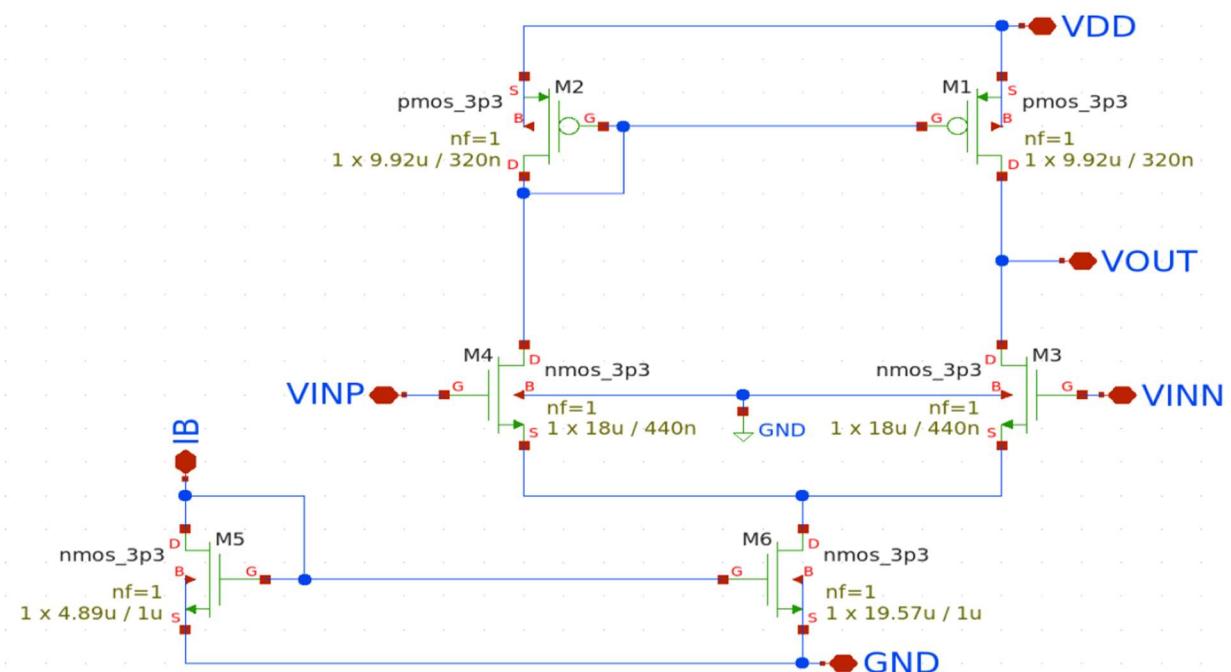
W \rightarrow = 10 u

W = 4.89um

Transistor	gm/ID	Length	Width	Function
M3 and M4	15	440nm	18um	Input pair
M1 and M2	10	320nm	9.92um	current mirror load
M5 and M6	10	1um	4.89um and 19.57um	tail current source

Part 3: Open - loop OTA simulation1

(1) Schematic of the OTA showing sizing of the transistors:



```

f2 = 2.174061e+05
peak = 4.624732e+01
f2 = 2.174061e+05
gbw = 1.005445e+07
BSIM4v5: Berkeley Short Channel IGFET Model-4
device m.x1.xm5.m0 m.x1.xm6.m0 m.x1.xm3.m0
model nmos_3p3.9 nmos_3p3.13 nmos_3p3.12
id 1e-05 4.01853e-05 2.00927e-05
vgs 0.82696 0.82696 0.725504
vds 0.826957 0.524489 0.369475
vdsat 0.166104 0.16646 0.0976014
vth 0.687465 0.688438 0.705265
gm 0.000103022 0.000415893 0.000322047
gds 3.33503e-07 1.67549e-06 3.83695e-06
gmbs 3.93924e-05 0.000159166 0.000107684

BSIM4v5: Berkeley Short Channel IGFET Model-4
device m.x1.xm4.m0 m.x1.xm2.m0 m.x1.xm1.m0
model nmos_3p3.12 pmos_3p3.8 pmos_3p3.8
id 2.00927e-05 2.00927e-05 2.00927e-05
vgs 0.725504 0.906025 0.906025
vds 0.369475 0.906023 0.906023
vdsat 0.0976014 0.176382 0.176382
vth 0.705265 0.757188 0.757188
gm 0.000322047 0.000204135 0.000204135
gds 3.83695e-06 3.07483e-06 3.07483e-06
gmbs 0.000107684 7.51581e-05 7.51581e-05

binary raw file "OTA_TB.raw"
ngspice 1 -> ■

```

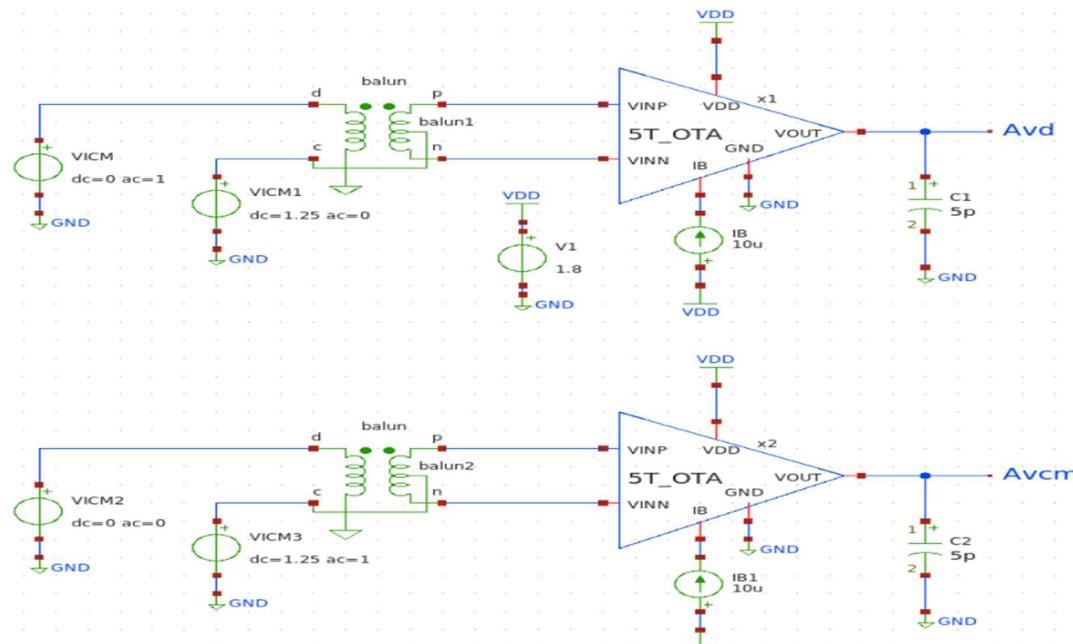
Is the current (and gm) in the input pair exactly equal?

Yes, the current and gm are exactly equal.

What is DC voltage at VOUT? Why?

Is 0.84v, $V_{DD} - V_{DS1} = 1.8 - 0.96 = 0.84v$

(2) Diff small signal ccs:



No. of Data Rows : 101

BSIM4v5: Berkeley Short Channel IGFET Model-4

device	m.x2.xm5.m0	m.x1.xm5.m0	m.x2.xm6.m0
model	nmos_3p3.9	nmos_3p3.9	nmos_3p3.13
id	1e-05	1e-05	4.01853e-05
vgs	0.82696	0.82696	0.82696
vds	0.826957	0.826957	0.524489
vdsat	0.166104	0.166104	0.16646
vth	0.687465	0.687465	0.688438
gm	0.000103022	0.000103022	0.000415893
gds	3.33503e-07	3.33503e-07	1.67549e-06
gmbs	3.93924e-05	3.93924e-05	0.000159166

BSIM4v5: Berkeley Short Channel IGFET Model-4

device	m.x1.xm6.m0	m.x2.xm3.m0	m.x2.xm4.m0
model	nmos_3p3.13	nmos_3p3.12	nmos_3p3.12
id	4.01853e-05	2.00927e-05	2.00927e-05
vgs	0.82696	0.725504	0.725504
vds	0.524489	0.369475	0.369475
vdsat	0.16646	0.0976014	0.0976014
vth	0.688438	0.705265	0.705265
gm	0.000415893	0.000322047	0.000322047
gds	1.67549e-06	3.83695e-06	3.83695e-06
gmbs	0.000159166	0.000107684	0.000107684

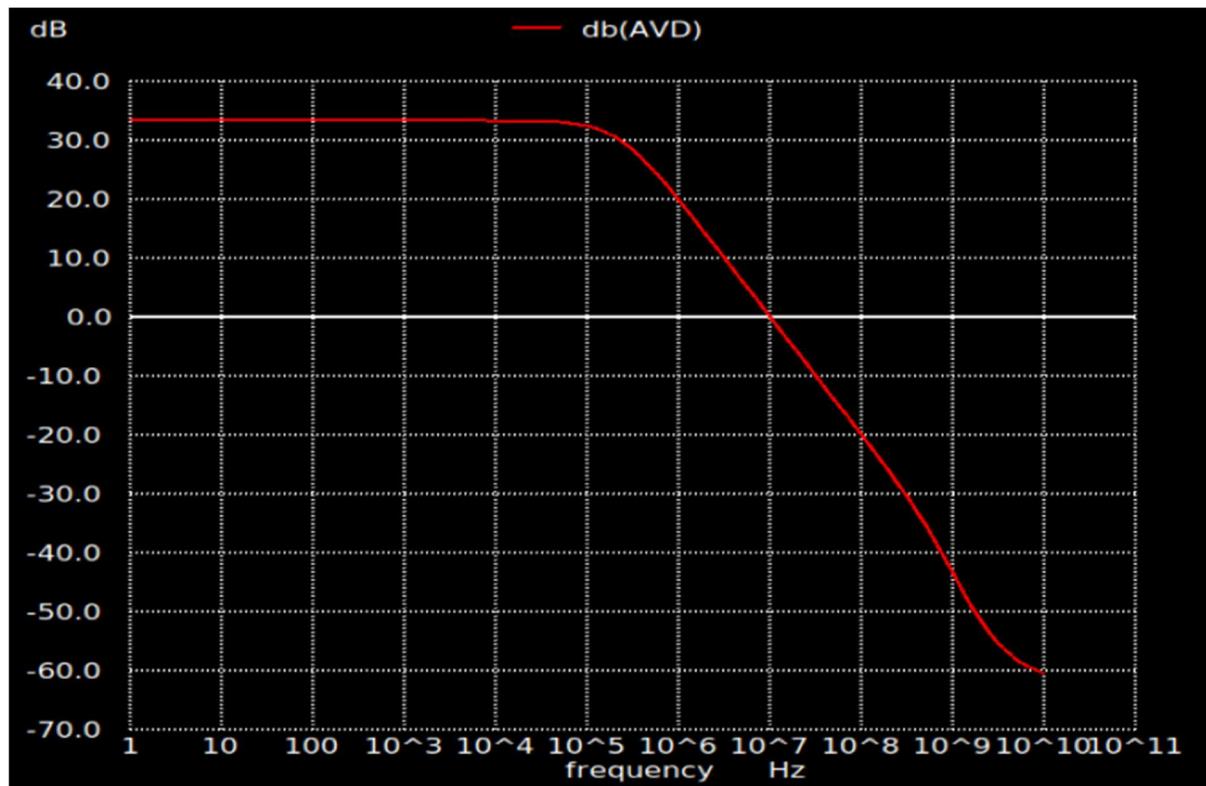
BSIM4v5: Berkeley Short Channel IGFET Model-4

device	m.x1.xm3.m0	m.x1.xm4.m0	m.x2.xm2.m0
model	nmos_3p3.12	nmos_3p3.12	pmos_3p3.8
id	2.00927e-05	2.00927e-05	2.00927e-05
vgs	0.725504	0.725504	0.906025
vds	0.369475	0.369475	0.906023
vdsat	0.0976014	0.0976014	0.176382
vth	0.705265	0.705265	0.757188
gm	0.000322047	0.000322047	0.000204135
gds	3.83695e-06	3.83695e-06	3.07483e-06
gmbs	0.000107684	0.000107684	7.51581e-05

BSIM4v5: Berkeley Short Channel IGFET Model-4

device	m.x2.xm1.m0	m.x1.xm2.m0	m.x1.xm1.m0
model	pmos_3p3.8	pmos_3p3.8	pmos_3p3.8
id	2.00927e-05	2.00927e-05	2.00927e-05
vgs	0.906025	0.906025	0.906025
vds	0.906023	0.906023	0.906023
vdsat	0.176382	0.176382	0.176382
vth	0.757188	0.757188	0.757188
gm	0.000204135	0.000204135	0.000204135
gds	3.07483e-06	3.07483e-06	3.07483e-06
gmbs	7.51581e-05	7.51581e-05	7.51581e-05

Plot diff gain (in dB) vs frequency.



Compare simulation results with hand calculations in a table.

$$\text{DC Gain} = gm_{3,4} * (ro_{1,2}|ro_{3,4}) = 46.6 = 33.36 \text{ dB}$$

$$\text{BW} = 1 / 2\pi CL(ro_{1,2}|ro_{3,4}) = 219.95 \text{ k Hz}$$

$$\text{GBW} = gm_{3,4}/2\pi CL = 10.24 \text{ M}$$

	Analytically	simulation
DC Gain	46.6	46.24
BW	219.9K	217.4K
GBW	10.24M	10.05M

(3) CM small signal ccs:

```

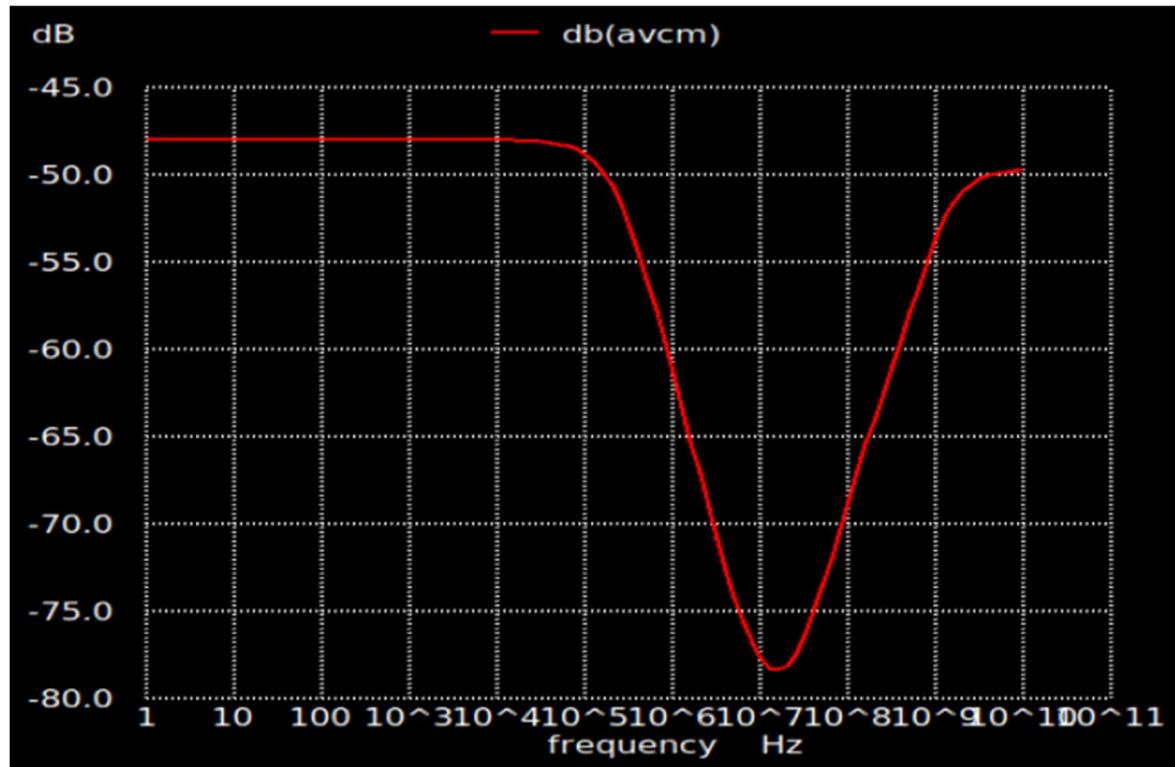
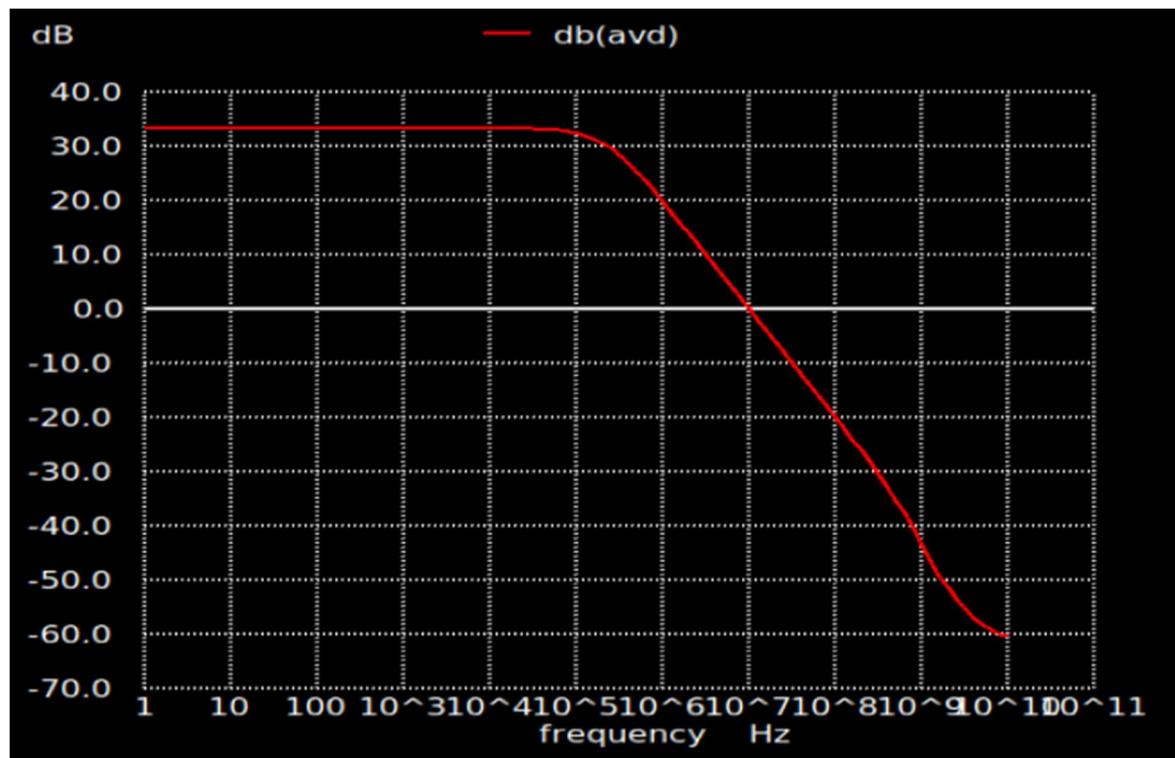
peak = 3.984955e-03 at= 3.162278e+00
f1 = 1.938967e+09
f2 = 2.175168e+05
peak = 3.984955e-03
f2 = 2.175168e+05
gbw = 8.667947e+02
BSIM4v5: Berkeley Short Channel IGFET Model-4
device m.x2.xm5.m0 m.x1.xm5.m0 m.x2.xm6.m0
model nmos_3p3.9 nmos_3p3.9 nmos_3p3.13
id 1e-05 1e-05 4.01853e-05
vgs 0.82696 0.82696 0.82696
vds 0.826957 0.826957 0.524489
vdsat 0.166104 0.166104 0.16646
vth 0.687465 0.687465 0.688438
gm 0.000103022 0.000103022 0.000415893
gds 3.33503e-07 3.33503e-07 1.67549e-06
gmbs 3.93924e-05 3.93924e-05 0.000159166

BSIM4v5: Berkeley Short Channel IGFET Model-4
device m.x1.xm6.m0 m.x2.xm3.m0 m.x2.xm4.m0
model nmos_3p3.13 nmos_3p3.12 nmos_3p3.12
id 4.01853e-05 2.00927e-05 2.00927e-05
vgs 0.82696 0.725504 0.725504
vds 0.524489 0.369475 0.369475
vdsat 0.16646 0.0976014 0.0976014
vth 0.688438 0.705265 0.705265
gm 0.000415893 0.000322047 0.000322047
gds 1.67549e-06 3.83695e-06 3.83695e-06
gmbs 0.000159166 0.000107684 0.000107684

BSIM4v5: Berkeley Short Channel IGFET Model-4
device m.x1.xm3.m0 m.x1.xm4.m0 m.x2.xm2.m0
model nmos_3p3.12 nmos_3p3.12 pmos_3p3.8
id 2.00927e-05 2.00927e-05 2.00927e-05
vgs 0.725504 0.725504 0.906025
vds 0.369475 0.369475 0.906023
vdsat 0.0976014 0.0976014 0.176382
vth 0.705265 0.705265 0.757188
gm 0.000322047 0.000322047 0.000204135
gds 3.83695e-06 3.83695e-06 3.07483e-06
gmbs 0.000107684 0.000107684 7.51581e-05

BSIM4v5: Berkeley Short Channel IGFET Model-4
device m.x2.xm1.m0 m.x1.xm2.m0 m.x1.xm1.m0
model pmos_3p3.8 pmos_3p3.8 pmos_3p3.8
id 2.00927e-05 2.00927e-05 2.00927e-05
vgs 0.906025 0.906025 0.906025
vds 0.906023 0.906023 0.906023
vdsat 0.176382 0.176382 0.176382
vth 0.757188 0.757188 0.757188
gm 0.000204135 0.000204135 0.000204135
gds 3.07483e-06 3.07483e-06 3.07483e-06
gmbs 7.51581e-05 7.51581e-05 7.51581e-05

```



Compare simulation results with hand calculations in a table.

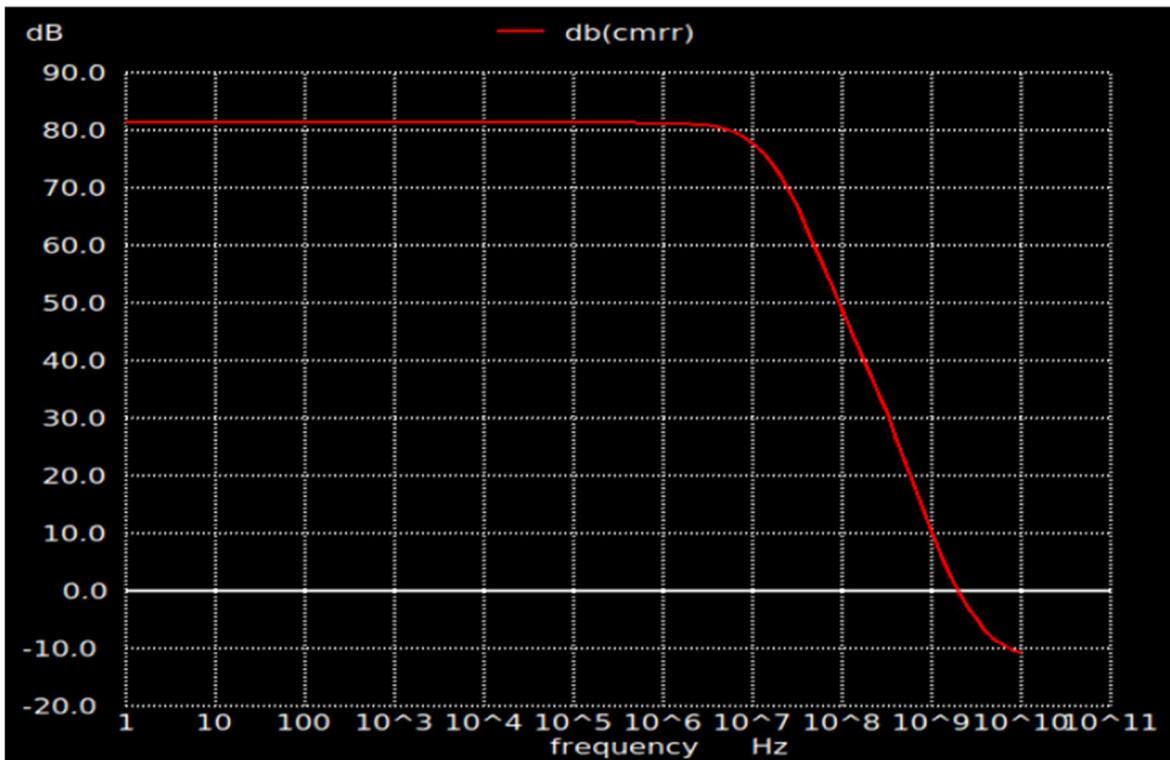
$$\text{DC Gain} = 1/(1+2gm_1,2 \cdot ro_6) = 4.087\text{m} = -47.7\text{dB}$$

$$\text{BW} = 1/(2\pi CL(ro_1,2|ro_3,4)) = 219.95\text{k Hz}$$

$$\text{GBW} = \text{Av} * \text{BW} = 10.24\text{M}$$

	Analytically	simulation
DC Gain	-47.77dB	-48dB
BW	219.9K	217.4K
GBW	875.4	866.7

(4) CMRR:

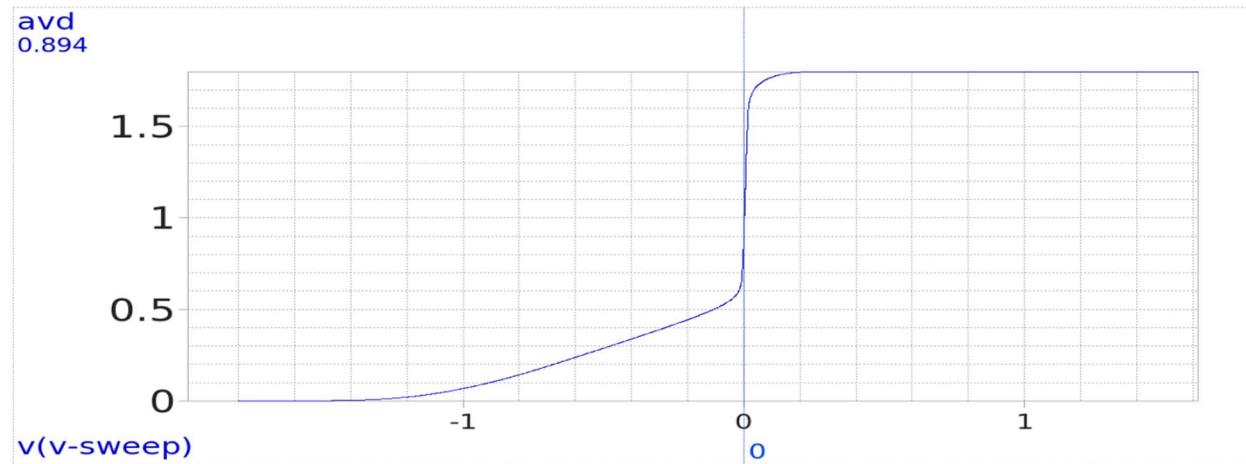


$$\text{CMRR in dB} = \text{Avd in dB} - \text{Avcm in dB} = 81.07 \text{ dB}$$

	Analytically	simulation
CMRR	81.07dB	81.3 dB

(5) Diff large signal ccs:

Plot VOUT vs VID.

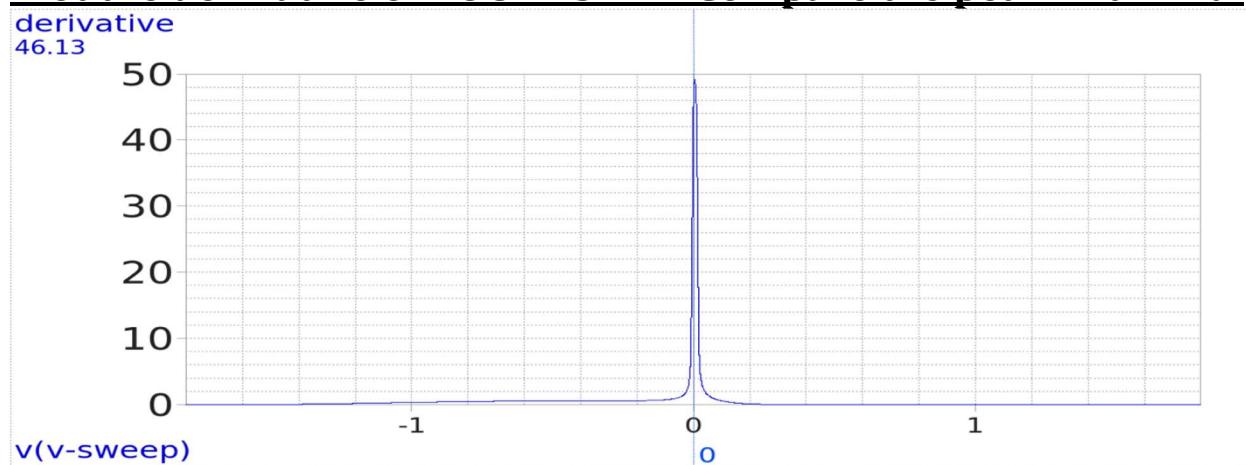


From the plot, what is the value of Vout at VID = 0? Why?

At VID = 0 VOUT = 0.894v

$$V_{out} = V_{dd} - V_{ds} = 1.8 - 0.906 = 0.894v$$

Plot the derivative of VOUT vs VID. Compare the peak with Avd.



The peak = 46.13 & Avd = 46.2, they're almost equal

(6) (Optional) CM large signal ccs (GBW vs VICM):

```
vicmmax = 1.790000e+00
vicmmin = 3.800000e-01
ngspice 1 -> [REDACTED]
```

PART 4: Closed-Loop OTA Simulation

```
No. of Data Rows : 1
gm_mismatch = 1.330528e-05
id_mismatch = 1.183353e-06
BSIM4v5: Berkeley Short Channel IGFET Model-4
device          m.x1.xm5.m0          m.x1.xm6.m0          m.x1.xm3.m0
model           nmos_3p3.9          nmos_3p3.13          nmos_3p3.12
id              1e-05             4.01823e-05         1.94995e-05
vgs              0.82696           0.82696           0.720154
vds              0.826957          0.522664          0.720152
vdsat             0.166104          0.16646           0.0953147
vth              0.687465           0.688438          0.70436
gm               0.000103022        0.000415866        0.000315818
gds              3.33503e-07          1.67984e-06         2.80961e-06
gmbs             3.93924e-05          0.000159155        0.000105545

BSIM4v5: Berkeley Short Channel IGFET Model-4
device          m.x1.xm4.m0          m.x1.xm2.m0          m.x1.xm1.m0
model           nmos_3p3.12          pmos_3p3.8          pmos_3p3.8
id              2.06828e-05          2.06828e-05         1.94995e-05
vgs              0.727329           0.90885           0.90885
vds              0.368475           0.908847          0.55717
vdsat             0.0985556          0.178599          0.176613
vth              0.705268           0.757167          0.75972
gm               0.000329123        0.000207542        0.000197814
gds              3.9428e-06           3.14149e-06         3.67846e-06
gmbs             0.000110056          7.6427e-05          7.31319e-05
```

Is the current (and gm) in the input pair exactly equal? Why?

No, there's mismatch between them.

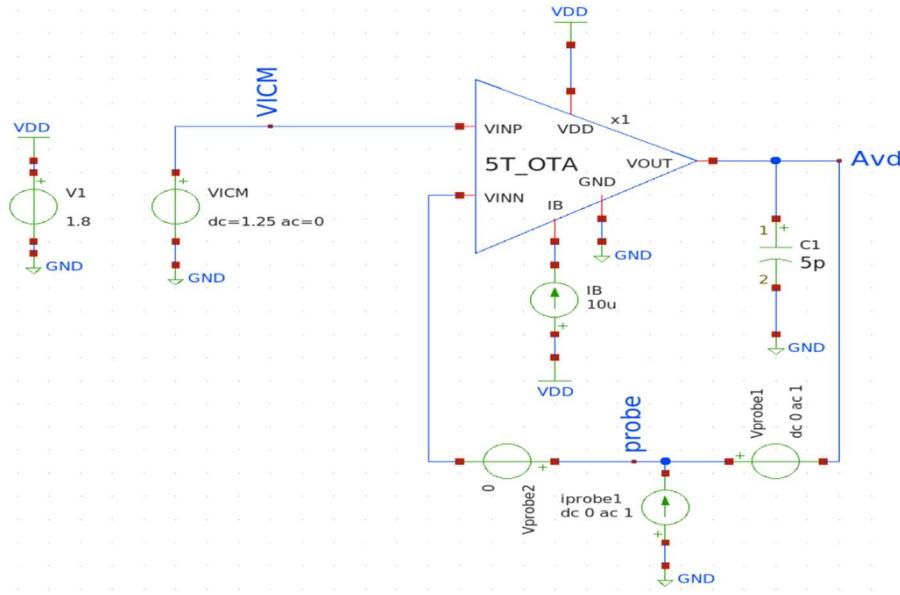
As the out is follow the Vin negative, and the tail current doesn't split between equally the two sides and gm.

Calculate the mismatch in Id and gm.

The mismatch in $I_D = (4.057 \times 10^{-5}) - (2.48 \times 10^{-10}) = 40.569 \mu A$

The mismatch in $g_m = 127.22 \mu S - 6.875 nS = 1S$

(2) Loop Gain:



```
No. of Data Rows : 241
Warning from checkvalid: vector @c1[i] is not available or has zero length.
all: no such command available in ngspace
```

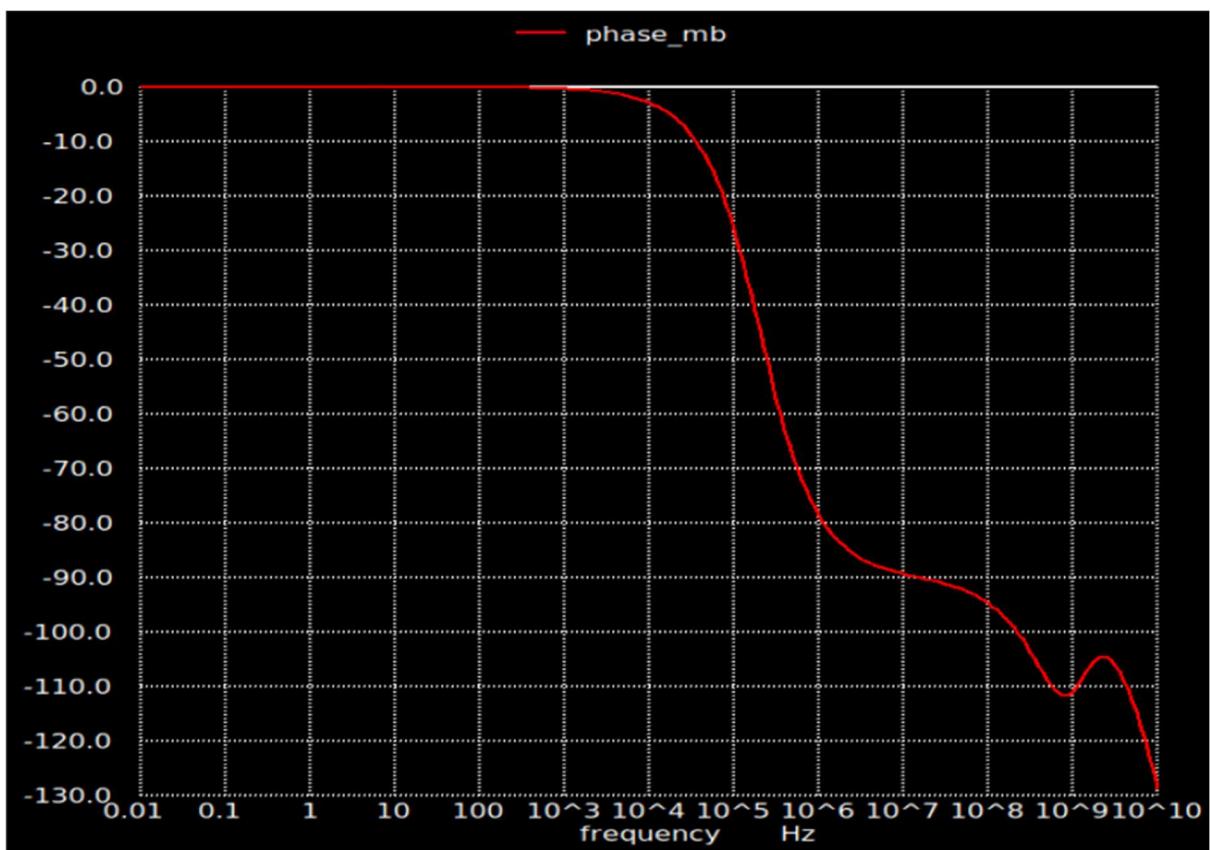
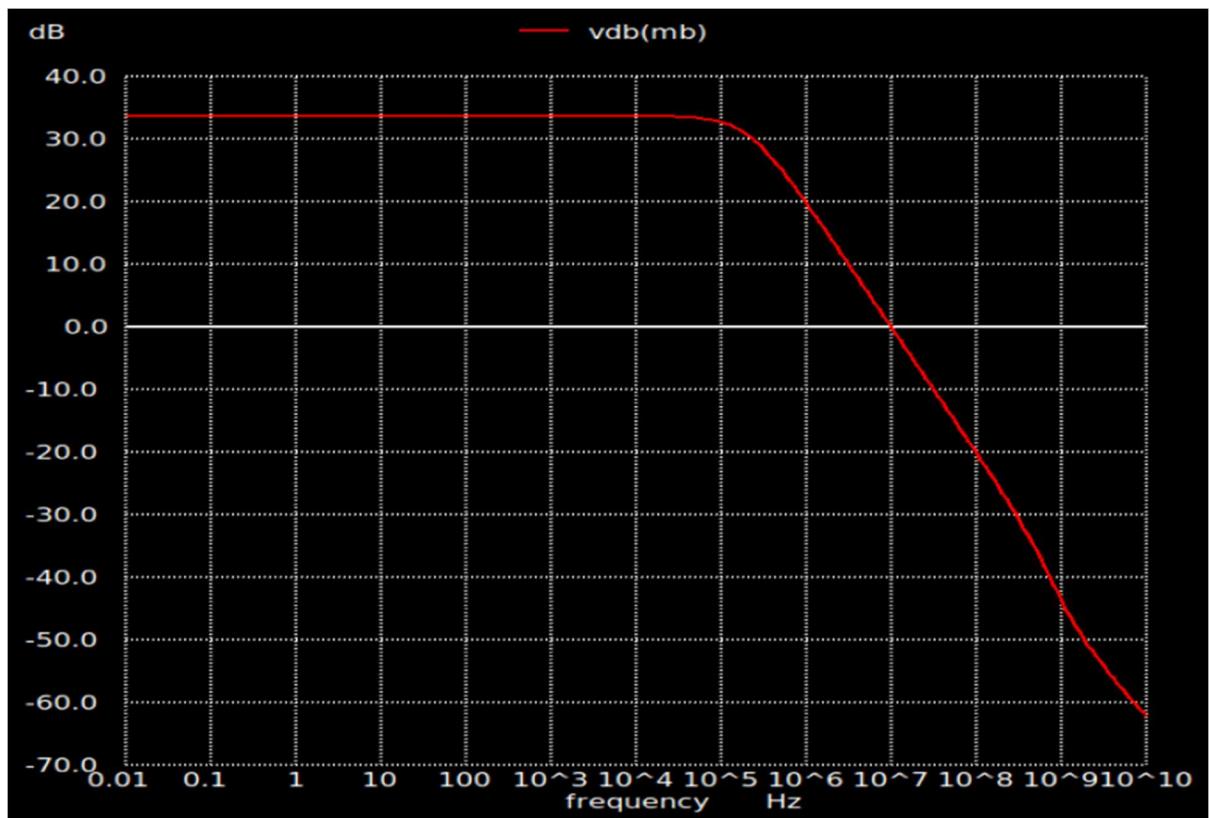
```
peak = 4.817608e+01 at= 2.238721e+00
```

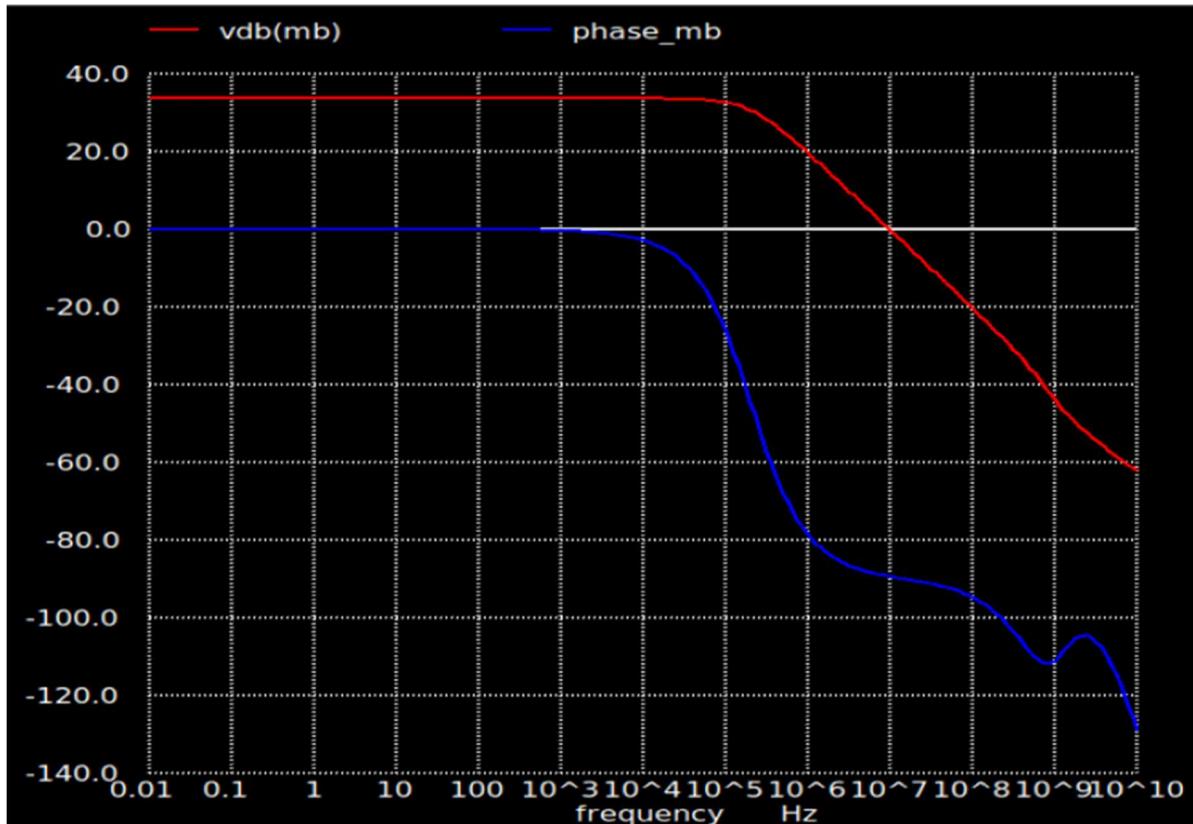
```
Error: measure f1 when(WHEN) : out of interval
meas ac f1 when vmag(mb)=3.406563e+01 rise=1 failed!
```

```
bw = 2.036348e+05
pm_deg = -8.928507e+01
dominant_pole_f = 9.811295e+06
loop_gain = 3.365663e+01
gbw = 9.810326e+06
Doing analysis at TEMP = 27.000000 and TNOM = 27.000000
```

```
No. of Data Rows : 1
BSIM4v5: Berkeley Short Channel IGFET Model-4
device m.x1.xm5.m0 m.x1.xm6.m0 m.x1.xm3.m0
model nmos_3p3.9 nmos_3p3.13 nmos_3p3.12
id 1e-05 4.01823e-05 1.34995e-05
vgs 0.82696 0.82696 0.720154
vds 0.826957 0.522664 0.720152
vdsat 0.166104 0.16646 0.0953147
vth 0.687465 0.688438 0.70436
gm 0.000103022 0.000415866 0.000315818
gds 3.33503e-07 1.67984e-06 2.80961e-06
gmbs 3.93924e-05 0.000159155 0.000105545
```

```
BSIM4v5: Berkeley Short Channel IGFET Model-4
device m.x1.xm4.m0 m.x1.xm2.m0 m.x1.xm1.m0
model nmos_3p3.12 pmos_3p3.8 pmos_3p3.8
id 2.06828e-05 2.06828e-05 1.34995e-05
vgs 0.727329 0.90885 0.90885
vds 0.368475 0.908847 0.55717
vdsat 0.0985556 0.178599 0.176613
vth 0.705268 0.757167 0.75972
gm 0.000329123 0.000207542 0.000197814
gds 3.9428e-06 3.14149e-06 3.67846e-06
gmbs 0.000110056 7.6427e-05 7.31319e-05
```





Compare DC gain and GBW with those obtained from open-loop simulation.

Comment.

```

peak           = 4.817608e+01 at= 2.238721e+00
Error: measure f1 when(WHEN) : out of interval
      meas ac f1 when vmag(mb)=3.406563e+01 rise=1 failed!

bw            = 2.036348e+05
pm_deg        = -8.928507e+01
dominant_pole_f = 9.811295e+06
loop_gain     = 3.365663e+01
gbw = 9.810326e+06
Doing analysis at TEMP = 27.000000 and TNOM = 27.000000

```

	Loop gain	open Loop
DC Gain	48.17	46.24
BW	203.63K	217.4K
GBW	9.81M	10.05M

Compare simulation results (DC gain and GBW) with hand calculations in a table.

$$\text{DC Gain} = gm_{3,4} * (ro_{1,2}|ro_{3,4}) = 48.68$$

$$\text{BW} = 1/ 2\pi CL(ro_{1,2}|ro_{3,4}) = 206.48 \text{K HZ}$$

$$\text{GBW} = gm_{3,4}/2\pi CL = 10.05 \text{M}$$

Loop gain		
	Analytically	simulation
DC Gain	48.68	48.17
BW	206.48K	203.63K
GBW	10.05M	9.81M

open Loop		
	Analytically	simulation
DC Gain	46.6	46.24
BW	219.9K	217.4K
GBW	10.24M	10.05M