Code:

```vhdl
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

ENTITY hw1_alu IS
   Port (
   A : IN  STD_LOGIC_VECTOR(3 downto 0);
   B : IN  STD_LOGIC_VECTOR(3 downto 0);
   sel: IN  STD_LOGIC_VECTOR(2 downto 0);
   Q : OUT STD_LOGIC_VECTOR(3 downto 0);
   cout : OUT STD_LOGIC ;
        overflow : OUT STD_LOGIC
);
END hw1_alu;
ARCHITECTURE hw1_alu_a of hw1_alu IS
SIGNAL s1 : STD_LOGIC_VECTOR(4 downto 0);
SIGNAL s2 : STD_LOGIC_VECTOR(3 downto 0);
BEGIN
 PROCESS(A,B,sel)
BEGIN
CASE sel IS
--AND
WHEN "000" =>
Q <= A AND B;
--OR
WHEN "001" =>
Q <= A OR B;
--ADD
```

```vhdl
WHEN "010" =>

s1(0) <= '0';

Q(0) <= A(0) XOR B(0) XOR s1(0);

s1(1) <= (A(0) AND B(0)) OR (A(0) AND s1(0)) OR (s1(0) AND B(0));

Q(1) <= A(1) XOR B(1) XOR s1(1);

s1(2) <= (A(1) AND B(1)) OR (A(1) AND s1(1)) OR (s1(1) AND B(1));

Q(2)<= A(2) XOR B(2) XOR s1(2);

s1(3)<= (A(2) AND B(2)) OR (A(2) AND s1(2)) OR (s1(2) AND B(2));

Q(3)<=A(3) XOR B(3) XOR s1(3);

s1(4)<= (A(3) AND B(3)) OR (A(3) AND s1(3)) OR (s1(3) AND B(3));

cout <= s1(4);

--SUB

WHEN "011" =>

s2 <= NOT B;

s1(0) <= '1';

Q(0) <= A(0) XOR s2(0) XOR s1(0);

s1(1) <= (A(0) AND s2(0)) OR (A(0) AND s1(0)) OR (s1(0) AND s2(0));

Q(1) <= A(1) XOR s2(1) XOR s1(1);

s1(2) <= (A(1) AND B(1)) OR (A(1) AND s1(1)) OR (s1(1) AND s2(1));

Q(2) <= A(2) XOR s2(2) XOR s1(2);

s1(3) <= (A(2) AND s2(2)) OR (A(2) AND s1(2)) OR (s1(2) AND s2(2));

Q(3) <= A(3) XOR s2(3) XOR s1(3);

s1(4) <= (A(3) AND s2(3)) OR (A(3) AND s1(3)) OR (s1(3) AND s2(3));

cout <= s1(4);

--ASR

WHEN "100" =>

Q(0) <= A(1);

Q(1) <= A(2);

Q(2) <= A(3);

Q(3) <= A(3);
```

```vhdl
--ASL
WHEN "101" =>
Q(0) <= '0';
Q(1) <= A(0);
Q(2) <= A(1);
Q(3) <= A(2);
if A(2) /= A(3) then
overflow <= A(2) XOR A(3);
end if;
--CSR
WHEN "110" =>
Q(0) <= A(1);
Q(1) <= A(2);
Q(2) <= A(3);
Q(3) <= A(0);
--CSL
WHEN "111" =>
Q(0) <= A(3);
Q(1) <= A(0);
Q(2) <= A(1);
Q(3) <= A(2);
WHEN OTHERS =>
Q <= "0000";
END CASE;
END PROCESS;
END hw1_alu_a;
```

Waveform:

Name:	Value:	50.0ns	100.0ns	150.0ns	200.0ns	250.0ns	300.0ns	350.0ns	400.0ns	450.0ns	500.0ns	550.0ns	600.0ns	650.0ns	700.0ns	750.0ns	800.
overflow	X																
cout	X																
A	B 0000	0000		0001		0010		0011		0100		0101		0110		0111	
B	B 0000	0000		0001		0010		0011		0100		0101		0110		0111	
sel	B 000	000		001		010		011		100		101		110		111	
Q	B 0000	0000		0001		0100		0000		0010		1010		0011		1110	