Write VHDL code to Design an arithmetic-logic circuit with 3-bit opcode variables $P_2P_1P_0$ and two 4-bits data inputs A and B by using full-adder blocks (FA). The circuit generates the following arithmetic, and logic operations. Draw the logic diagram with carry (C_{OUT}) and overflow (OF) outputs. Test your design with using Altera MuxPlus II or Quartus programme)

P_2	P_1	P_0	**OPCODE**	OPERATION
0	0	0	AND	A $\wedge$ B
0	0	1	OR	A $\vee$ B
0	1	0	ADD	A + B
0	1	1	SUB	A - B
1	0	0	ASR	Arithmetic Shift Right A
1	0	1	ASL	Arithmetic Shift Left A
1	1	0	CSR	Circular Shift Right A
1	1	1	CSL	Circular Shift Left A