Project: Part 3

Generating Chip

Overview:

After synthesizing both floating point adders and multipliers, we can reach the point where a chip is generated, please note that this process can be reiterated multiple times until all design rules are satisfied.

Requirement:

1. Using Phase One adder and Phase two multiplier.
2. Synthesis the multipliers and add the following constraints
    i. Set clock to 2ns.
    ii. Set Input delay to 0.2ns.
    iii. Set load to 10
    iv. Set output load to 0.5ns.
    v. Set Utilization to 60%
    vi. Enable usage of all library cells.
    - Report: Total Area, Max Delay, Max Slack, Min Slack, Total Power, clk.
    - If a design suffers from -ve slack, adjust the timing constraints.
    - Make sure that all designs work on the same constraints after modification.
3. Place and route the multipliers with similar constraints to synthesis.
    - Constraint clock skew to 0.2ns
    - Only use vertical strips
    - Report: Total Area, Utilization, Max Delay, Min Delay, worst slack, Total Power, clk.
    - If a design suffers from -ve slack, adjust the timing constraints.
    - Make sure that all designs work on the same constraints after modification.
4. Apply post-routing simulation using your previously made testbench. **(include your sdf file)**
5. Generate the final GDS file for each design.

Deliverables:

- For adder and multiplier, a folder content the following
    - Code files for Design
    - Code file for testbench.

- Do file to run and configure wave.
- Constraints files
- Scripts used for synthesis
- Scripts used for Floorplanning, Placement & Routing
- Synthesis generated reports
- Routing generated reports
- Post-synthesize code
- Post-routing code
- Sdf file
- GDS
- Final saved database from Routing
- Screenshot from oasys netlists (showing details not just high level)
- Screenshot from Nitro final layout.
- Screenshots of 3 simulations, pre-synthesis, post-synthesis, post-routing

- Excel Sheet containing the reported results in a tabular form. For example

	Verilog (*)	Multiplier Tree	Sequential Multiplier	Original Booth	Radix-4 Booth	Float multiplier
Min Delay						
Max Delay						
Clock						
Total Power						
Area						
Utilization after routing (not after export)						
Number Latches/Flip Flops.						

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Due Dates:

- All files should be zipped together and uploaded on GoogleClassroom by only one team member
- Due Date is the **28th of December at midnight**. (1 mark bonus for early delivery 26th of december).