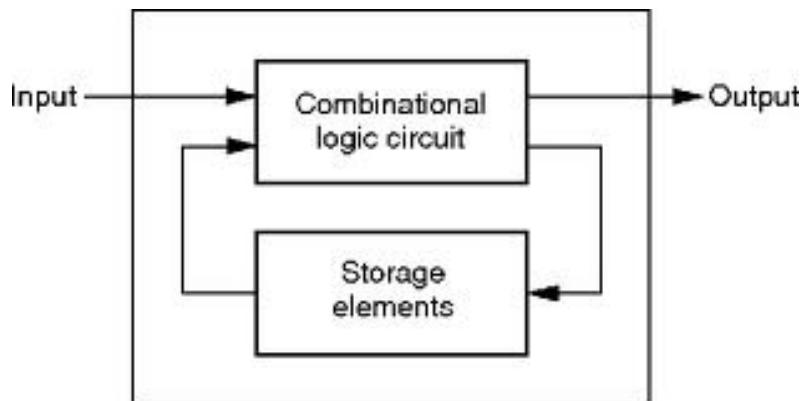


Latches and Flip-Flops

Chapter 7

Nouman M Durrani



LATCHES

The **latch** is a type of temporary storage device that has two stable states (bistable). Latches are similar to flip-flops because they are bistable devices that can reside in either of two states using a feedback arrangement, in which the outputs are connected back to the opposite inputs. The main difference between latches and flip-flops is in the method used for changing their state.

The S-R (SET-RESET) Latch

A latch is a type of **bistable** logic device or **multivibrator**. An active-HIGH input S-R (SET-RESET) latch is formed with two cross-coupled NOR gates, as shown in Figure 7-1(a); an active-LOW input \bar{S} - \bar{R} latch is formed with two cross-coupled NAND gates, as shown in Figure 7-1(b). Notice that the output of each gate is connected to an input of the opposite gate. This produces the regenerative feedback that is characteristic of all latches and flip-flops.

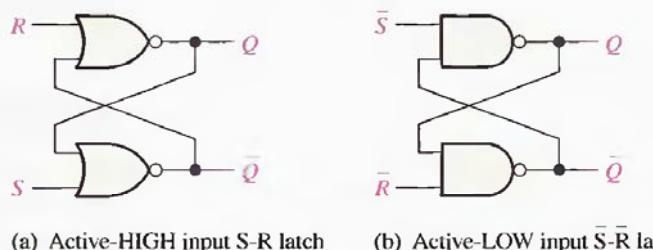
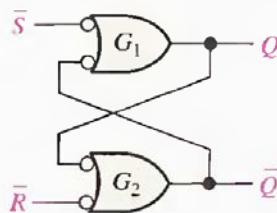


FIGURE 7-1

The latch in Figure 7–2 has two inputs, \bar{S} and \bar{R} , and two outputs, Q and \bar{Q} . Let's start by assuming that both inputs and the Q output are HIGH. Since the Q output is connected back to an input of gate G_2 , and the \bar{R} input is HIGH, the output of G_2 must be LOW. This LOW output is coupled back to an input of gate G_1 , ensuring that its output is HIGH.

► FIGURE 7–2

Negative-OR equivalent of the NAND gate \bar{S} - \bar{R} latch in Figure 9–1(b).



When the Q output is HIGH, the latch is in the **SET** state. It will remain in this state indefinitely until a LOW is temporarily applied to the \bar{R} input. With a LOW on the \bar{R} input and a HIGH on \bar{S} , the output of gate G_2 is forced HIGH. This HIGH on the \bar{Q} output is coupled back to an input of G_1 , and since the \bar{S} input is HIGH, the output of G_1 goes LOW. This LOW on the Q output is then coupled back to an input of G_2 , ensuring that the \bar{Q} output remains HIGH even when the LOW on the \bar{R} input is removed. When the Q output is LOW, the latch is in the **RESET** state. Now the latch remains indefinitely in the RESET state until a LOW is applied to the \bar{S} input.

► TABLE 7–1

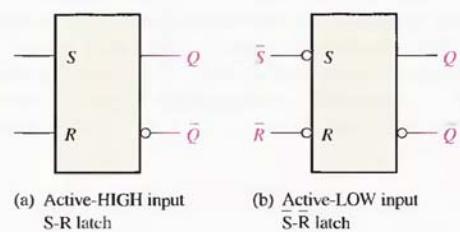
Truth table for an active-LOW input \bar{S} - \bar{R} latch.

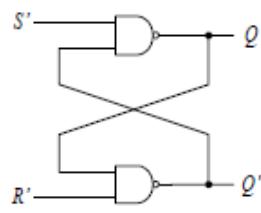
INPUTS		OUTPUTS		COMMENTS
\bar{S}	\bar{R}	Q	\bar{Q}	
1	1	NC	NC	No change. Latch remains in present state.
0	1	1	0	Latch SET.
1	0	0	1	Latch RESET.
0	0	1	1	Invalid condition

Logic symbols for both the active-HIGH input and the active-LOW input latches are shown in Figure 7–4.

► FIGURE 7–4

Logic symbols for the S-R and \bar{S} - \bar{R} latch.

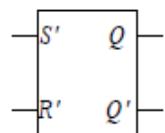




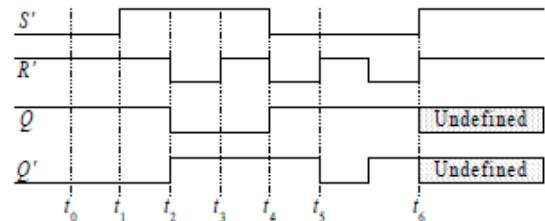
(a)

S	R	Q	Q_{next}	Q_{next}'
0	0	\times	1	1
0	1	\times	1	0
1	0	\times	0	1
1	1	0	0	1
1	1	1	1	0

(b)

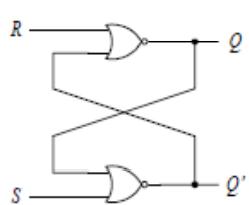


(c)



(d)

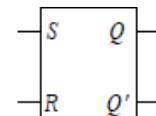
Figure 4. SR latch: (a) circuit using NAND gates; (b) truth table; (c) logic symbol; (d) timing diagram.



(a)

S	R	Q	Q_{next}	Q_{next}'
0	0	0	0	1
0	0	1	1	0
0	1	\times	0	1
1	0	\times	1	0
1	1	\times	0	0

(b)



(c)

Figure 5. SR latch: (a) circuit using NOR gates; (b) truth table; (c) logic symbol.

NOR Gate latch

S	R	Q
0	0	NC
1	0	1
0	1	0
1	1	*Invalid

*Produces $Q=Q'=0$

NAND LATCH

S	R	Q
0	0	NC
1	0	1
0	1	0
1	1	*Invalid

*Produces $Q=Q'=1$

EXAMPLE 7-1

If the \bar{S} and \bar{R} waveforms in Figure 7-5(a) are applied to the inputs of the latch in Figure 7-4(b), determine the waveform that will be observed on the Q output. Assume that Q is initially LOW.

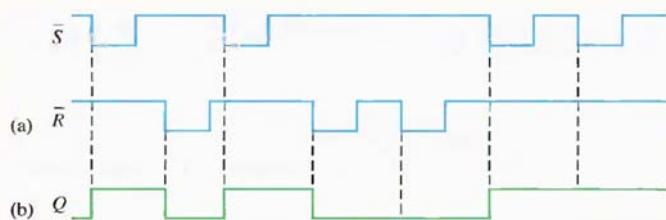


FIGURE 7-5

Solution See Figure 7-5(b).

Related Problem* Determine the Q output of an active-HIGH input S-R latch if the waveforms in Figure 7-5(a) are inverted and applied to the inputs.

Uses of Latches:

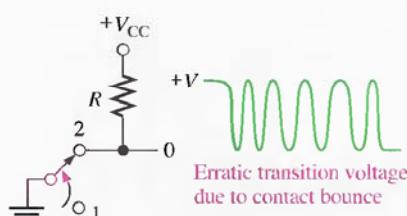
Latches are sometimes used in computer systems for multiplexing data onto a bus.

For example, data being input to a computer from an external source have to share the data bus with data from other sources. When the data bus becomes unavailable to the external source, the existing data must be temporarily stored, and latches placed between the external source and the data bus may be used to do this. When the data bus is unavailable to the external source, the latches must be disconnected from the bus using a method known as tri-stating. When the data bus becomes available, the external data pass through the latches, thus the term transparent latch.

The gated D latch performs this function because when it is enabled, the data on its input appear on the output just as though there were a direct connection. Data on the input are stored as soon as the latch is disabled.

An Application

The Latch as a Contact-Bounce Eliminator A good example of an application of an $\overline{S}-\overline{R}$ latch is in the elimination of mechanical switch contact “bounce.” When the pole of a switch strikes the contact upon switch closure, it physically vibrates or bounces several times before finally making a solid contact. Although these bounces are very short in duration, they produce voltage spikes that are often not acceptable in a digital system. This situation is illustrated in Figure 7–6(a).

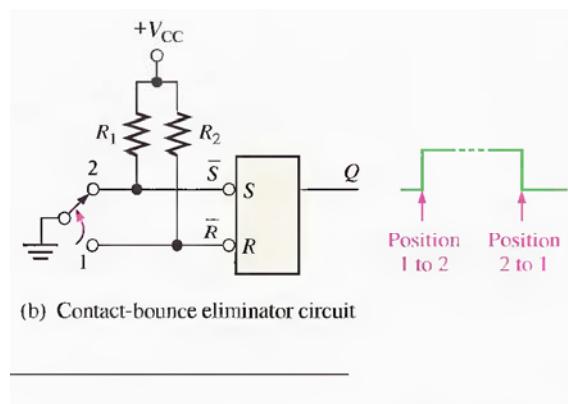


(a) Switch contact bounce

▲ FIGURE 7–6

The $\overline{S}-\overline{R}$ latch used to eliminate switch contact bounce.

An $\overline{S}-\overline{R}$ latch can be used to eliminate the effects of switch bounce as shown in Figure 7–6(b). The switch is normally in position 1, keeping the \overline{R} input LOW and the latch RESET. When the switch is thrown to position 2, \overline{R} goes HIGH because of the pull-up resistor to V_{CC} , and \overline{S} goes LOW on the first contact. Although \overline{S} remains LOW for only a very short time before the switch bounces, this is sufficient to set the latch. Any further voltage spikes on the \overline{S} input due to switch bounce do not affect the latch, and it remains SET. Notice that the Q output of the latch provides a clean transition from LOW to HIGH, thus eliminating the voltage spikes caused by contact bounce. Similarly, a clean transition from HIGH to LOW is made when the switch is thrown back to position 1.



The 74LS279 is a quad $\overline{S}-\overline{R}$ latch represented by the logic diagram of Figure 7–7(a) and the pin diagram in part (b). Notice that two of the latches each have two \overline{S} inputs.

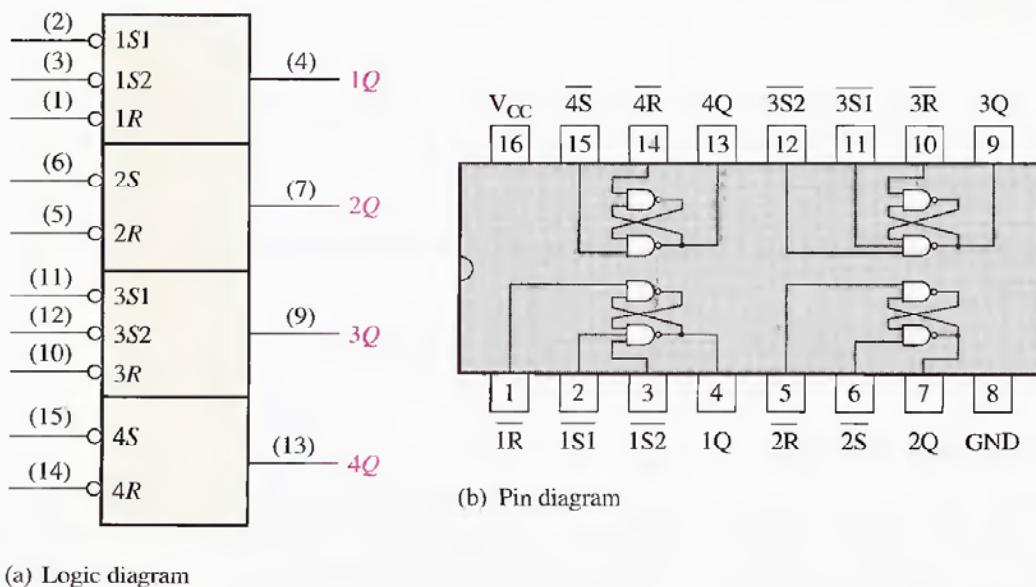


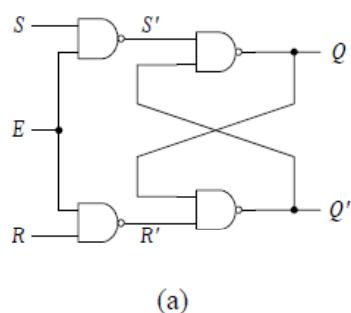
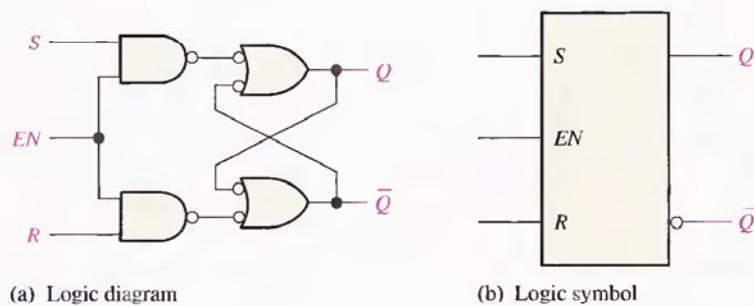
FIGURE 7–7
The 74LS279 quad $\overline{S}-\overline{R}$ latch.

The Gated S-R Latch

A gated latch requires an enable input, EN (G is also used to designate an enable input). The logic diagram and logic symbol for a gated S-R latch are shown in Figure 7–8. The S and R inputs control the state to which the latch will go when a HIGH level is applied to the EN input. The latch will not change until EN is HIGH; but as long as it remains HIGH, the output is controlled by the state of the S and R inputs. In this circuit, the invalid state occurs when both S and R are simultaneously HIGH.

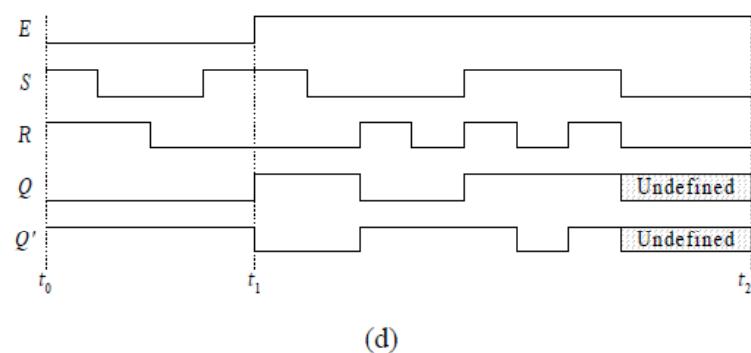
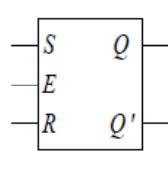
► FIGURE 7–8

A gated S-R latch.



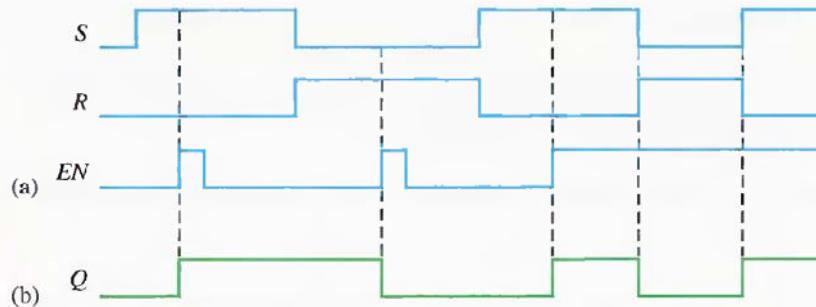
E	S	R	Q	Q_{next}	Q_{next}'
0	x	x	0	0	1
0	x	x	1	1	0
1	0	0	0	0	1
1	0	0	1	1	0
1	0	1	x	0	1
1	1	0	x	1	0
1	1	1	x	1	1

(b)



EXAMPLE 7-2

Determine the Q output waveform if the inputs shown in Figure 7-9(a) are applied to a gated S-R latch that is initially RESET.

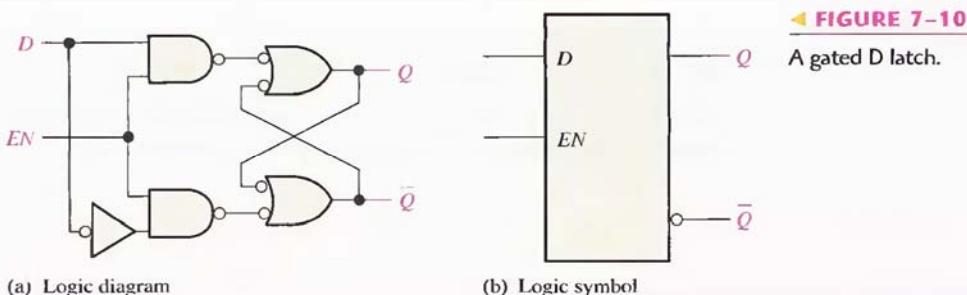


◀ FIGURE 7-9

The Q waveform is shown in Figure 7-9(b). When S is HIGH and R is LOW, a HIGH on the EN input sets the latch. When S is LOW and R is HIGH, a HIGH on the EN input resets the latch.

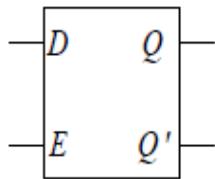
The Gated D Latch

Another type of gated latch is called the D latch. It differs from the S-R latch because it has only one input in addition to EN . This input is called the D (data) input. Figure 7-10 contains a logic diagram and logic symbol of a D latch. When the D input is HIGH and the EN input is HIGH, the latch will set. When the D input is LOW and EN is HIGH, the latch will reset. Stated another way, the output Q follows the input D when EN is HIGH.

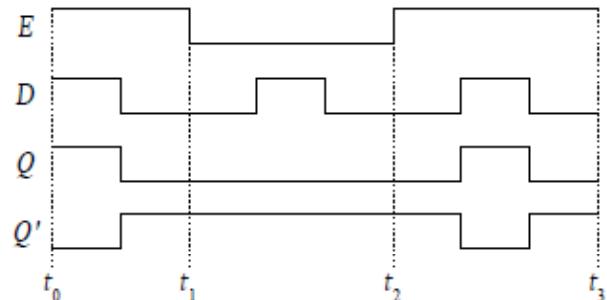


◀ FIGURE 7-10
A gated D latch.

EN	D	Q
1	1	1
1	0	0



(c)



(d)

EXAMPLE 7-3

Determine the Q output waveform if the inputs shown in Figure 7-11(a) are applied to a gated D latch, which is initially RESET.

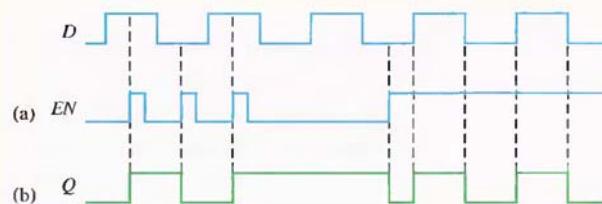


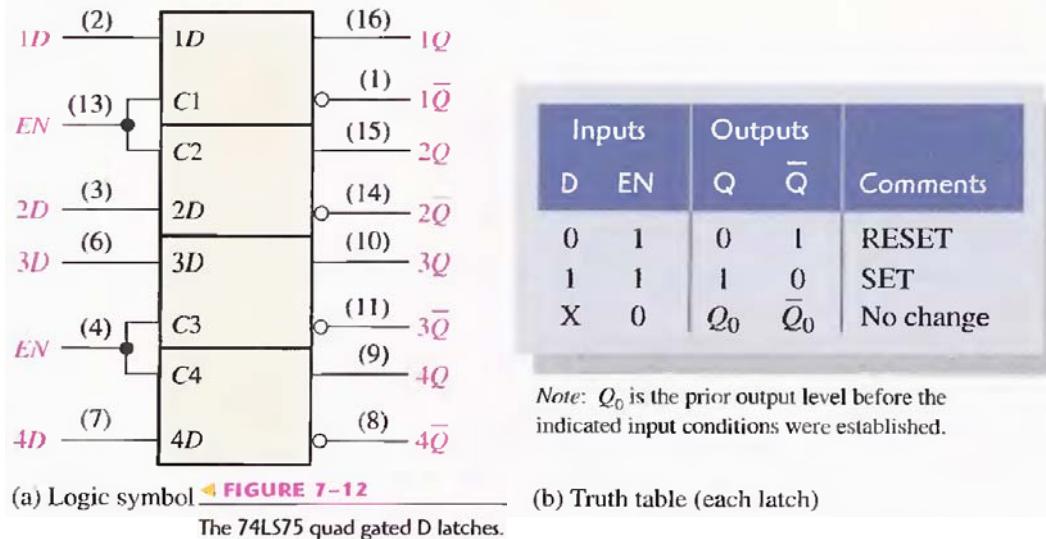
FIGURE 7-11

Solution The Q waveform is shown in Figure 7-11(b). When D is HIGH and EN is HIGH, Q goes HIGH. When D is LOW and EN is HIGH, Q goes LOW. When EN is LOW, the state of the latch is not affected by the D input.

Related Problem Determine the Q output of the gated D latch if the D input in Figure 7-11(a) is inverted.

THE 74LS75 D LATCH

An example of a gated D latch is the 74LS75 represented by the logic symbol in Figure 7–12(a). This device has four latches. Notice that each active-HIGH *EN* input is shared by two latches and is designated as a control input (*C*). The truth table for each latch is shown in Figure 7–12(b). The X in the truth table represents a “don’t care” condition. In this case, when the *EN* input is LOW, it does not matter what the *D* input is because the outputs are unaffected and remain in their prior states.

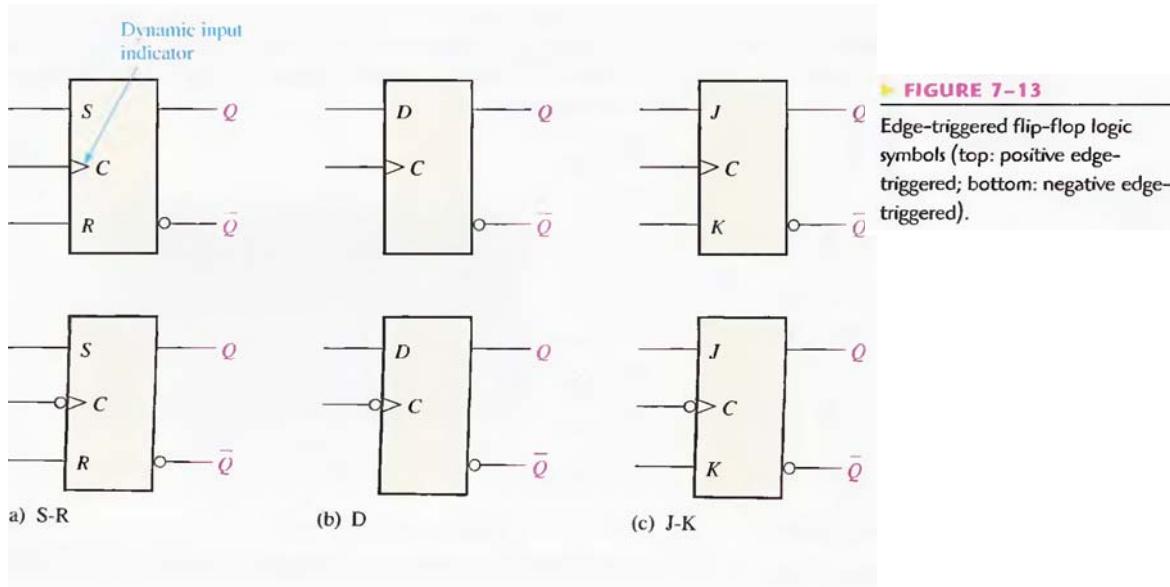


EDGE-TRIGGERED FLIP-FLOPS

Flip-flops are synchronous bistable devices, also known as *bistable multivibrators*. In this case, the term *synchronous* means that the output changes state only at a specified point on the triggering input called the **clock** (CLK), which is designated as a control input, *C*; that is, changes in the output occur in synchronization with the clock.

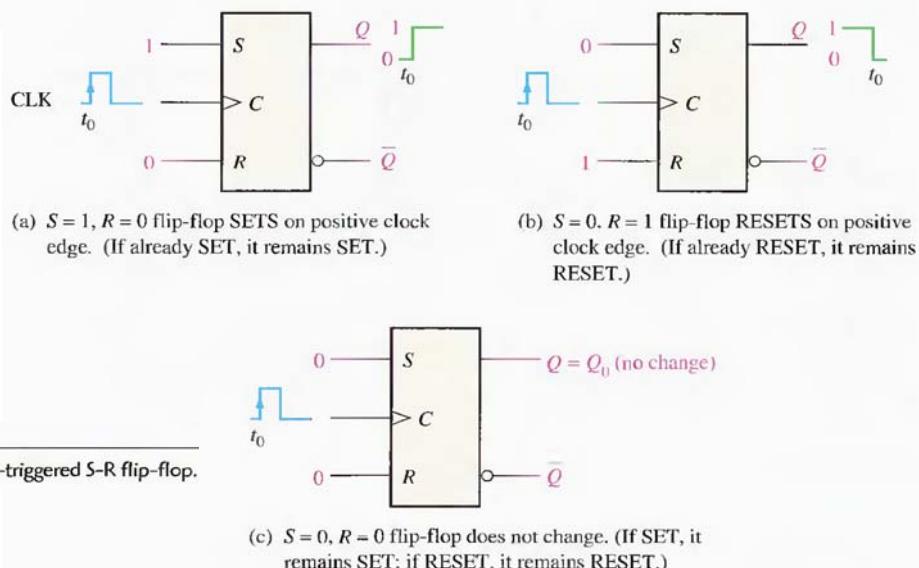
- An edge-triggered flip-flop changes state either at the positive edge (rising edge) or at the negative edge (falling edge) of the clock pulse and is sensitive to its inputs only at this transition of the clock.
- Three types of edge-triggered flip-flops are :
 - S-R,
 - D, and
 - J-K

- The key to identifying an edge-triggered flip-flop by its logic symbol is the small triangle inside the block at the clock (C) input.
- This triangle is called the dynamic input indicator.



The Edge-Triggered S-R Flip-Flop

The S and R inputs of the S-R flip-flop are called **synchronous** inputs because data on these inputs are transferred to the flip-flop's output only on the triggering edge of the clock pulse. When S is HIGH and R is LOW, the Q output goes HIGH on the triggering edge of the clock pulse, and the flip-flop is SET. When S is LOW and R is HIGH, the Q output goes LOW on the triggering edge of the clock pulse, and the flip-flop is RESET. When both S and R are LOW, the output does not change from its prior state. An invalid condition exists when both S and R are HIGH.



◀ TABLE 7-2

Truth table for a positive edge-triggered S-R flip-flop.

INPUTS			OUTPUTS		COMMENTS
S	R	CLK	Q	\bar{Q}	
0	0	X	Q_0	\bar{Q}_0	No change
0	1	↑	0	1	RESET
1	0	↑	1	0	SET
1	1	↑	?	?	Invalid

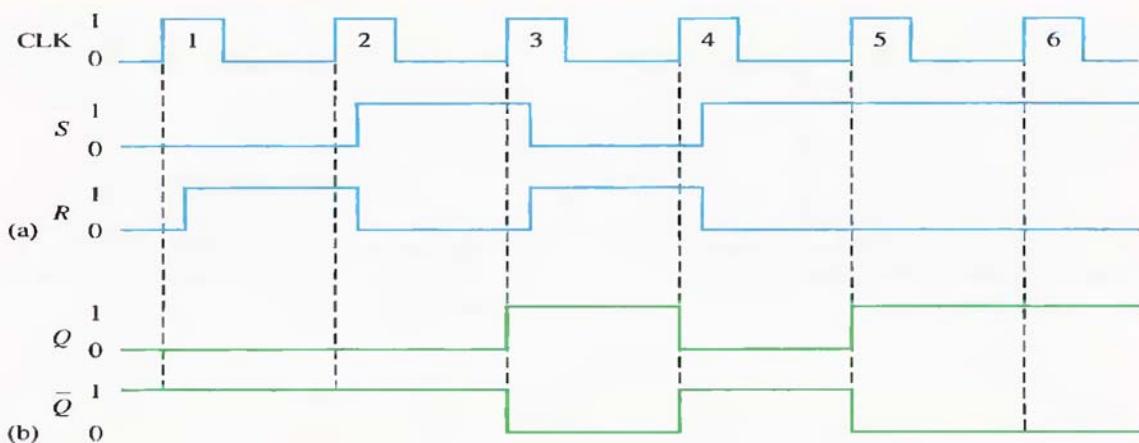
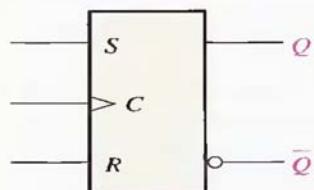
↑ = clock transition LOW to HIGH

X = irrelevant ("don't care")

Q_0 = output level prior to clock transition

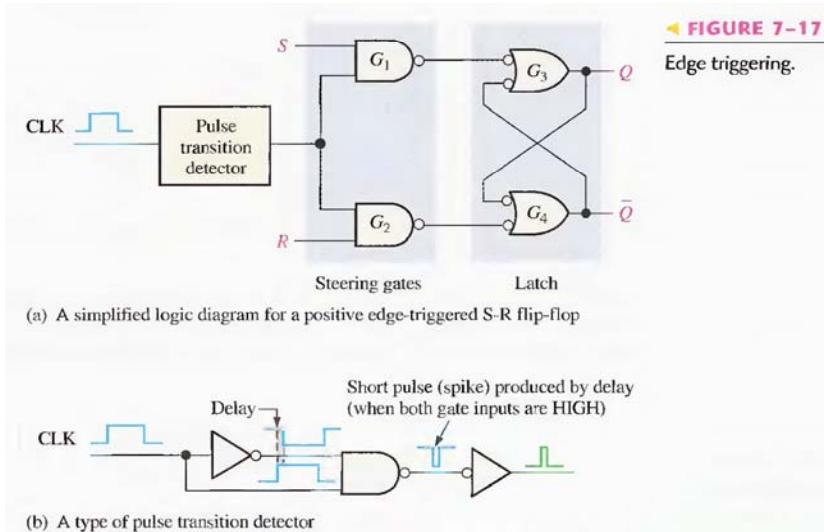
Determine the Q and \bar{Q} output waveforms of the flip-flop in Figure 7-15 for the S , R , and CLK inputs in Figure 7-16(a). Assume that the positive edge-triggered flip-flop is initially RESET.

▶ FIGURE 7-15

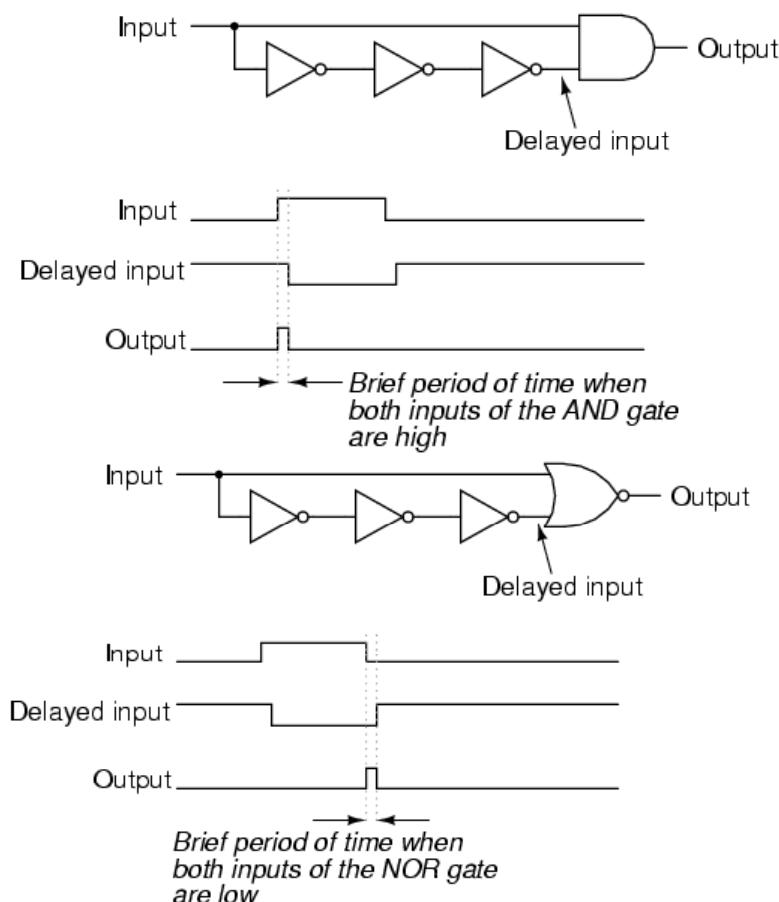


▶ FIGURE 7-16

A Method of Edge-Triggering

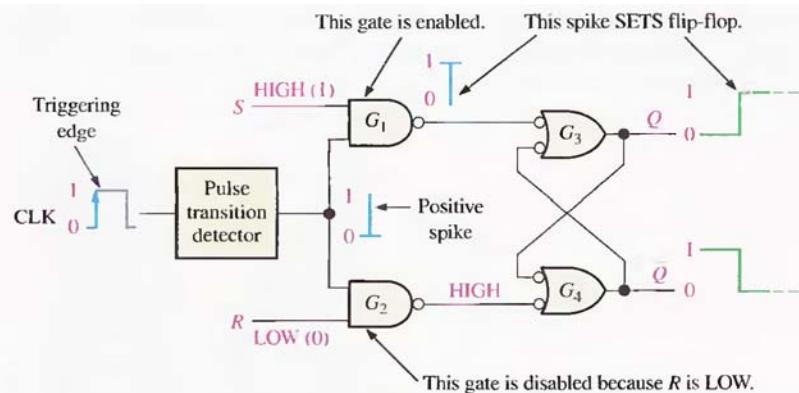


One basic type of pulse transition detector is shown in Figure 7–17(b). As you can see, there is a small delay on one input to the NAND gate so that the inverted clock pulse arrives at the gate input a few nanoseconds after the true clock pulse. This circuit produces a very short-duration spike on the positive-going transition of the clock pulse. In a negative edge-triggered flip-flop the clock pulse is inverted first, thus producing a narrow spike on the negative-going edge.



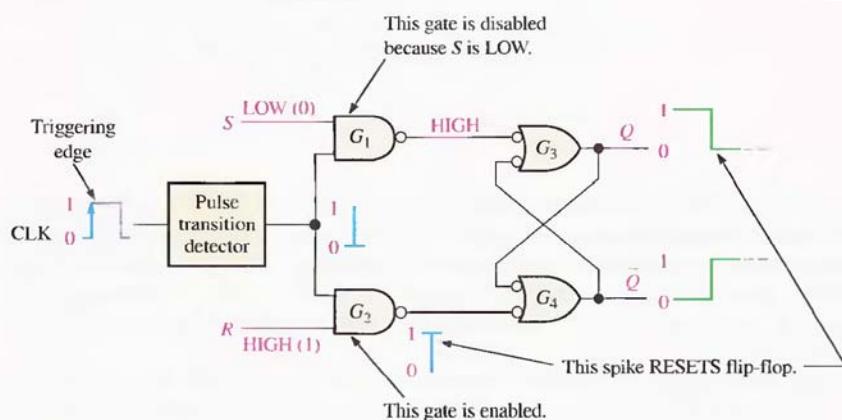
► FIGURE 7-18

Flip-flop making a transition from the RESET state to the SET state on the positive-going edge of the clock pulse.



► FIGURE 7-19

Flip-flop making a transition from the SET state to the RESET state on the positive-going edge of the clock pulse.

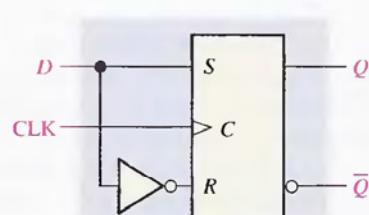


The Edge-Triggered D Flip-Flop

The **D flip-flop** is useful when a single data bit (1 or 0) is to be stored.

► FIGURE 7-20

A positive edge-triggered D flip-flop formed with an S-R flip-flop and an inverter.



► TABLE 7-3

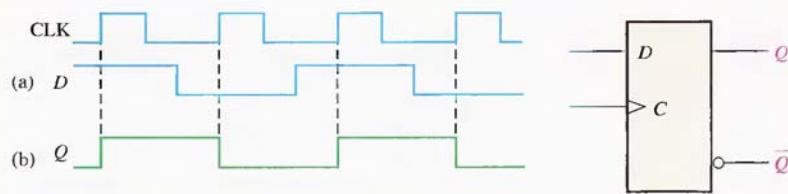
Truth table for a positive edge-triggered D flip-flop.

D	INPUTS CLK	OUTPUTS Q	OUTPUTS \bar{Q}	COMMENTS
1	↑	1	0	SET (stores a 1)
0	↑	0	1	RESET (stores a 0)

↑ = clock transition LOW to HIGH

EXAMPLE 7–5

Given the waveforms in Figure 7–21(a) for the D input and the clock, determine the Q output waveform if the flip-flop starts out RESET.



▲ FIGURE 7–21

Solution The Q output goes to the state of the D input at the time of the positive-going clock edge. The resulting output is shown in Figure 7–21(b).

Related Problem Determine the Q output for the D flip-flop if the D input in Figure 7–21(a) is inverted.

Example:

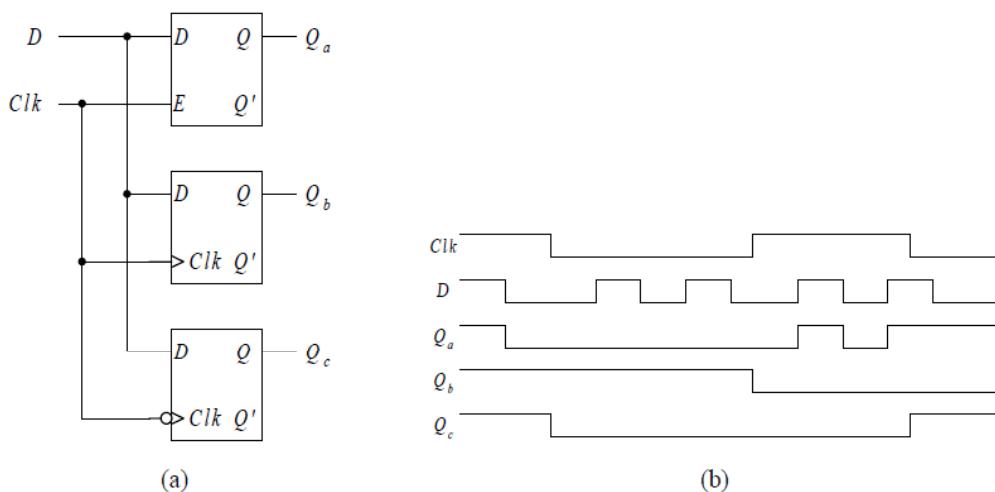
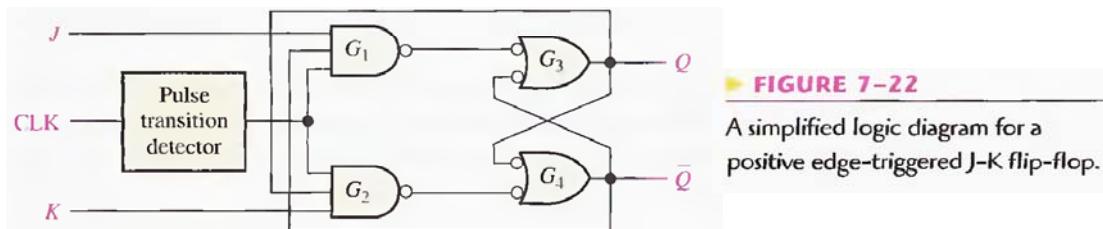


Figure 12. Comparison of a gated latch, a positive-edge-triggered flip-flop, and a negative-edge-triggered flip-flop: (a) circuit; (b) timing diagram.

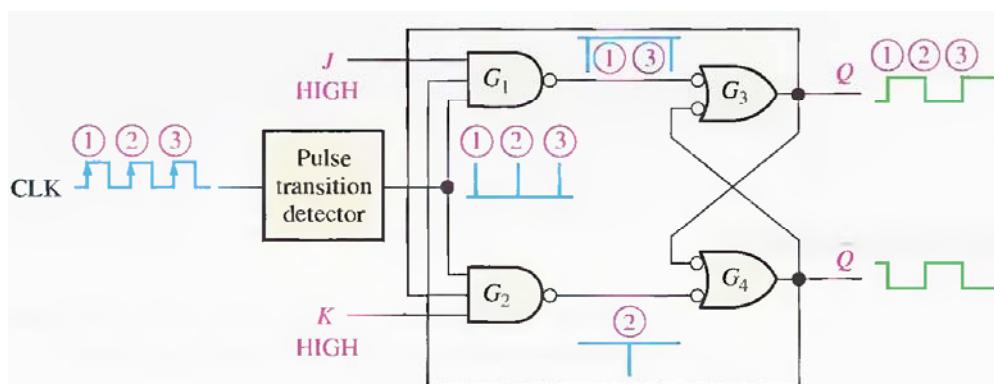
The Edge-Triggered J-K Flip-Flop



► FIGURE 7-22

A simplified logic diagram for a positive edge-triggered J-K flip-flop.

Figure 7-22 shows the basic internal logic for a positive edge-triggered J-K flip-flop. It differs from the S-R edge-triggered flip-flop in that the Q output is connected back to the input of gate G_2 , and the \bar{Q} output is connected back to the input of gate G_1 . The two control inputs are labeled J and K in honor of Jack Kilby, who invented the integrated circuit. A J-K flip-flop can also be of the negative edge-triggered type, in which case the clock input is inverted.



► FIGURE 7-23

Transitions illustrating the toggle operation when $J = 1$ and $K = 1$.

In the toggle mode, a J-K flip-flop changes state on every clock pulse.

► TABLE 7-4

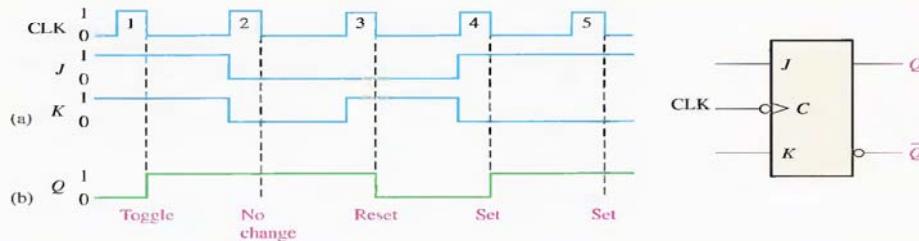
Truth table for a positive edge-triggered J-K flip-flop.

J	K	CLK	OUTPUTS		COMMENTS
			Q	\bar{Q}	
0	0	\uparrow	Q_0	\bar{Q}_0	No change
0	1	\uparrow	0	1	RESET
1	0	\uparrow	1	0	SET
1	1	\uparrow	\bar{Q}_0	Q_0	Toggle

\uparrow = clock transition LOW to HIGH

Q_0 = output level prior to clock transition

The waveforms in Figure 7–24(a) are applied to the J , K , and clock inputs as indicated. Determine the Q output, assuming that the flip-flop is initially RESET.



▲ FIGURE 7-24

Solution

- First, since this is a negative edge-triggered flip-flop, as indicated by the “bubble” at the clock input, the Q output will change only on the negative-going edge of the clock pulse.
- At the first clock pulse, both J and K are HIGH; and because this is a toggle condition, Q goes HIGH.
- At clock pulse 2, a no-change condition exists on the inputs, keeping Q at a HIGH level.
- When clock pulse 3 occurs, J is LOW and K is HIGH, resulting in a RESET condition; Q goes LOW.
- At clock pulse 4, J is HIGH and K is LOW, resulting in a SET condition; Q goes HIGH.
- A SET condition still exists on J and K when clock pulse 5 occurs, so Q will remain HIGH.

The resulting Q waveform is indicated in Figure 7–24(b).

Asynchronous Preset and Clear Inputs

$S-R$, D , and $J-K$ inputs are called *synchronous inputs* because data on these inputs are transferred to the flip-flop’s output only on the triggering edge of the clock pulse; that is, the data are transferred synchronously with the clock.

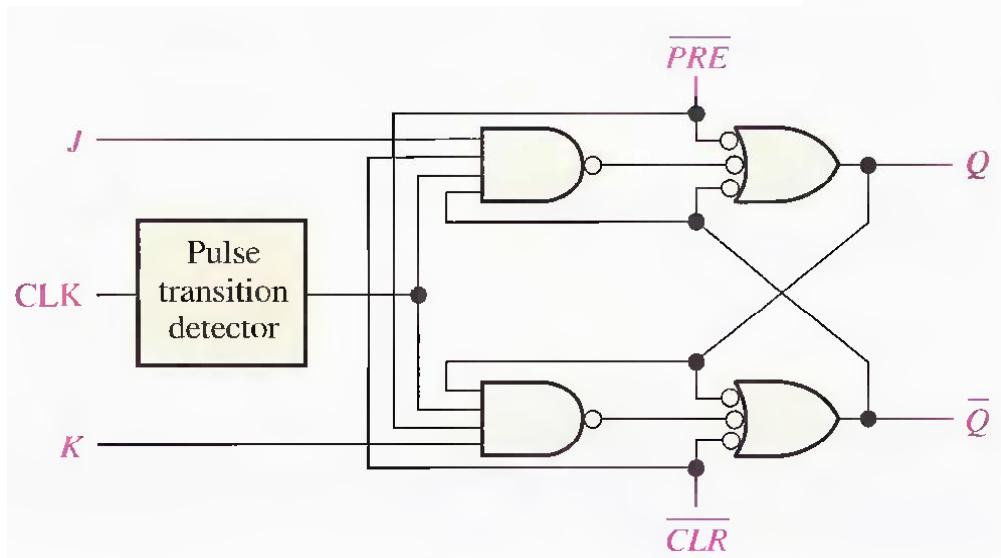
Asynchronous inputs (preset and clear) can set or reset the flip-flop regardless of the status of the clock signal.

CLOCK	J	K	SET	RESET	Q	\bar{Q}
-	-	-	0	0	Invalid	Invalid
-	-	-	0	1	1	0
-	-	-	1	0	0	1
$\overline{\text{L}}$	0	0	1	1	Q	\bar{Q}
$\overline{\text{L}}$	1	0	1	1	1	0
$\overline{\text{L}}$	0	1	1	1	0	1
$\overline{\text{L}}$	1	1	1	1	\bar{Q}	Q

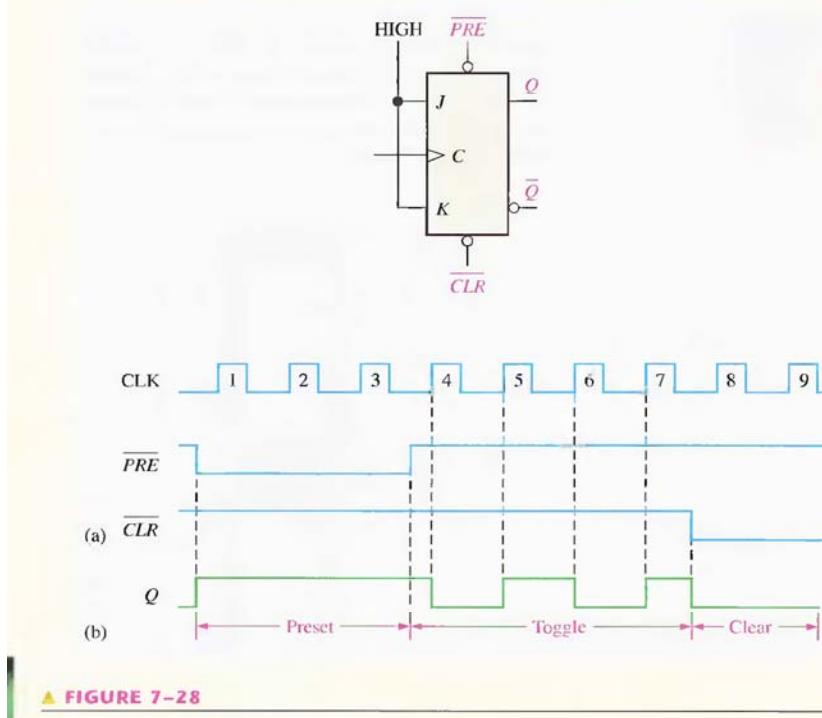
Invalid= Q and \bar{Q} goes high

◀ FIGURE 7-27

Logic diagram for a basic J-K flip-flop with active-LOW preset and clear inputs.



For the positive edge-triggered J-K flip-flop with preset and clear inputs in Figure 7-28, determine the Q output for the inputs shown in the timing diagram in part (a). Q is initially LOW.

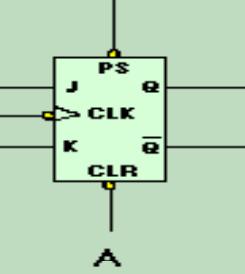


◀ FIGURE 7-28

Asynchronous Inputs

The asynchronous inputs "Preset" and "Clear" operate independently of the clock signal. More importantly, they can override the synchronous inputs. When the "Preset" or "Clear" input is active, the flip-flop's output "Q" will be either a logic 1 or 0.

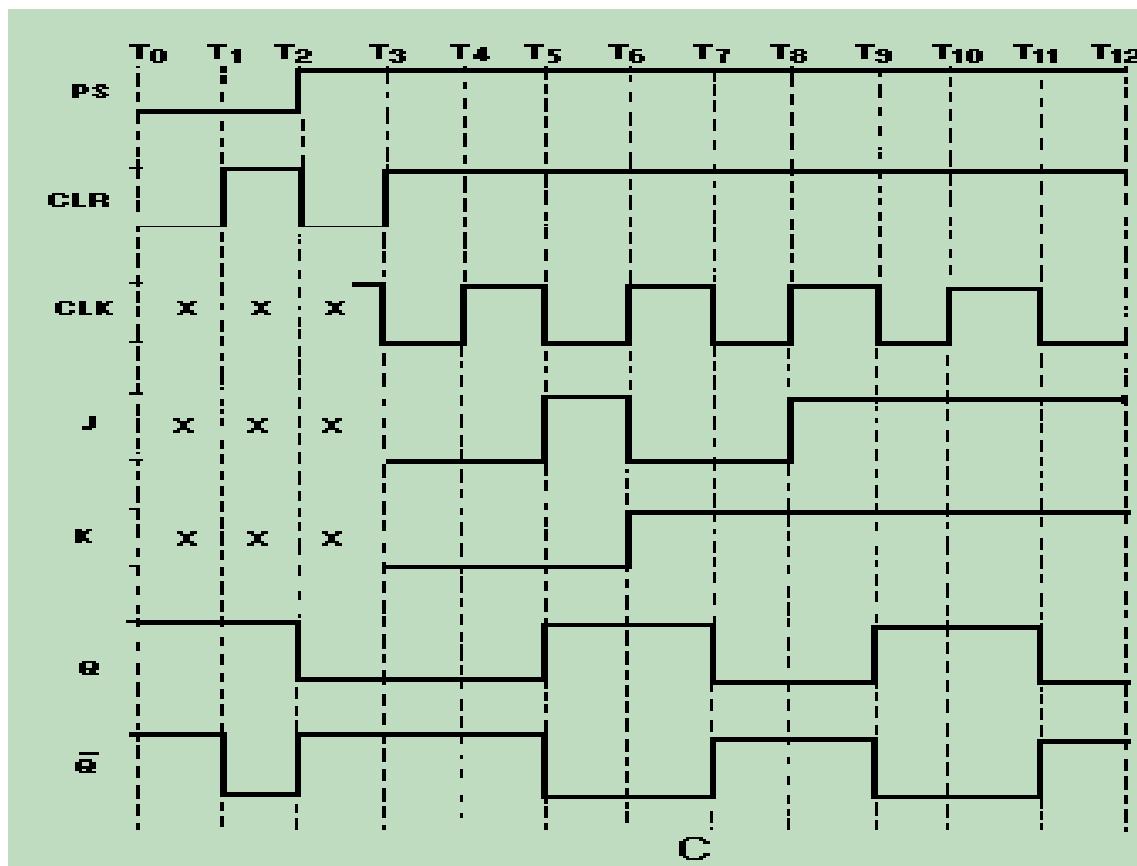
It is important to recognize that the **asynchronous inputs have priority over the synchronous inputs.**



INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	K	Q	\bar{Q}
1	0	x	x	x	1	1
2	0	x	x	x	1	0
3	1	x	x	x	0	1
4	1	x	0	0	0	\bar{Q}
5	1	x	1	0	1	0
6	1	x	0	1	0	1
7	1	x	1	1	TOGGLE	
8	1	0	x	x	Q	\bar{Q}

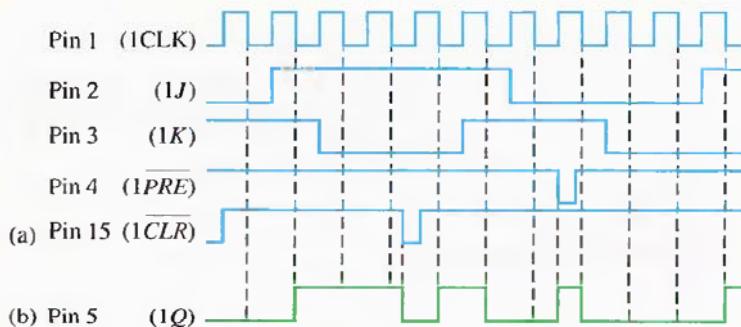
X = IRRELEVANT

B



EXAMPLE 7-9

The $1J$, $1K$, $1\overline{CLK}$, $1\overline{PRE}$, and $1\overline{CLR}$ waveforms in Figure 7-31(a) are applied to one of the negative edge-triggered flip-flops in a 74HC112 package. Determine the $1Q$ output waveform.



▲ FIGURE 7-31

Solution The resulting $1Q$ waveform is shown in Figure 7-31(b). Notice that each time a LOW is applied to the $1\overline{PRE}$ or $1\overline{CLR}$, the flip-flop is set or reset regardless of the states of the other inputs.

FLIP-FLOP OPERATING CHARACTERISTICS

The performance, operating requirements, and limitations of flip-flops are specified by several operating characteristics or parameters :

(i) Propagation Delay Times:

A propagation delay time is the interval of time required after an input signal has been applied for the resulting output change to occur.

Four categories of propagation delay times are important in the operation of a flip-flop:

1. Propagation delay t_{PLH} as measured from the triggering edge of the clock pulse to the LOW-to-HIGH transition of the output. This delay is illustrated in Figure 7–32(a).
2. Propagation delay t_{PHL} as measured from the triggering edge of the clock pulse to the HIGH-to-LOW transition of the output. This delay is illustrated in Figure 7–32(b).

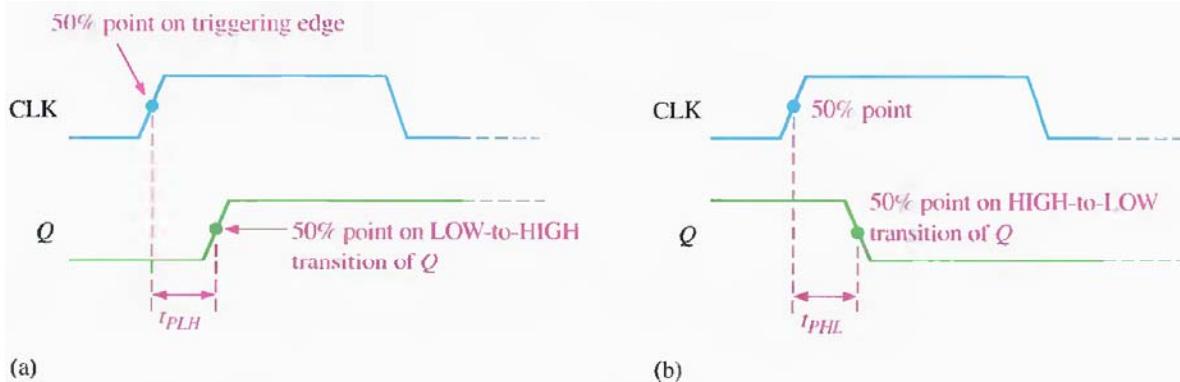


FIGURE 7-32
Propagation delays, clock to output.

3. Propagation delay t_{PLH} as measured from the leading edge of the preset input to the LOW-to-HIGH transition of the output. This delay is illustrated in Figure 7–33(a) for an active-LOW preset input.
4. Propagation delay t_{PHL} as measured from the leading edge of the clear input to the HIGH-to-LOW transition of the output. This delay is illustrated in Figure 7–33(b) for an active-LOW clear input.

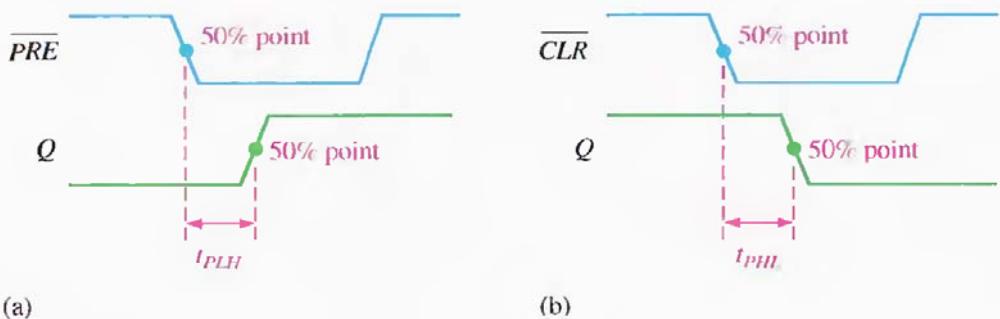
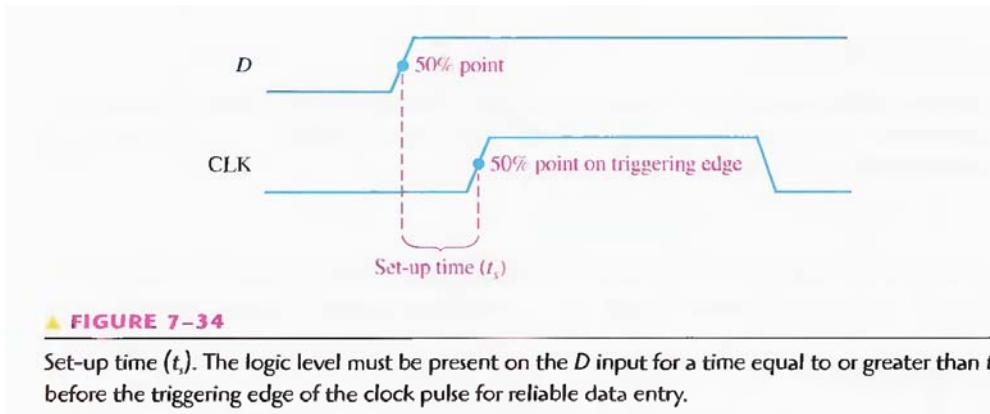


FIGURE 7-33
Propagation delays, preset input to output and clear input to output.

- **Setup time** is the minimum amount of time the data signal should be held steady **before** the clock event so that the data are reliably clocked by the clock.



- **Hold time** is the minimum amount of time the data signal should be held steady **after** the clock event so that the data are reliably clocked.

Hold Time

The **hold time** (t_h) is the minimum interval required for the logic levels to remain on the inputs after the triggering edge of the clock pulse in order for the levels to be reliably clocked into the flip-flop. This is illustrated in Figure 7-35 for a D flip-flop.

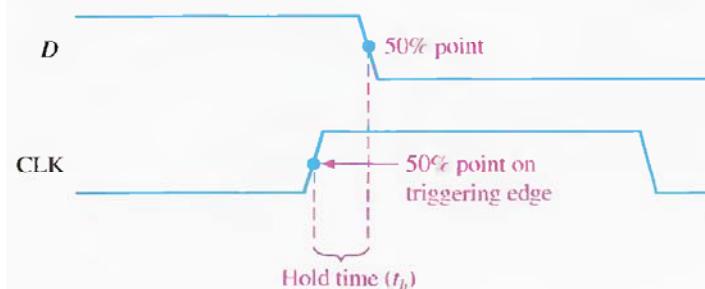


FIGURE 7-35

Hold time (t_h). The logic level must remain on the D input for a time equal to or greater than t_h , after the triggering edge of the clock pulse for reliable data entry.

Maximum Clock Frequency

The maximum clock frequency (f_{\max}) is the highest rate at which a flip-flop can be reliably triggered. At clock frequencies above the maximum, the flip-flop would be unable to respond quickly enough, and its operation would be impaired.

Pulse Widths

Minimum pulse widths (t_W) for reliable operation are usually specified by the manufacturer for the clock, preset, and clear inputs. Typically, the clock is specified by its minimum HIGH time and its minimum LOW time.

Power Dissipation

The **power dissipation** of any digital circuit is the total power consumption of the device. For example, if the flip-flop operates on a +5 V dc source and draws 5 mA of current, the power dissipation is

$$P = V_{CC} \times I_{CC} = 5 \text{ V} \times 5 \text{ mA} = 25 \text{ mW}$$

The power dissipation is very important in most applications in which the capacity of the dc supply is a concern. As an example, let's assume that you have a digital system that requires a total of ten flip-flops, and each flip-flop dissipates 25 mW of power. The total power requirement is

$$P_T = 10 \times 25 \text{ mW} = 250 \text{ mW} = 0.25 \text{ W}$$

This tells you the output capacity required of the dc supply. If the flip-flops operate on +5 V dc, then the amount of current that the supply must provide is

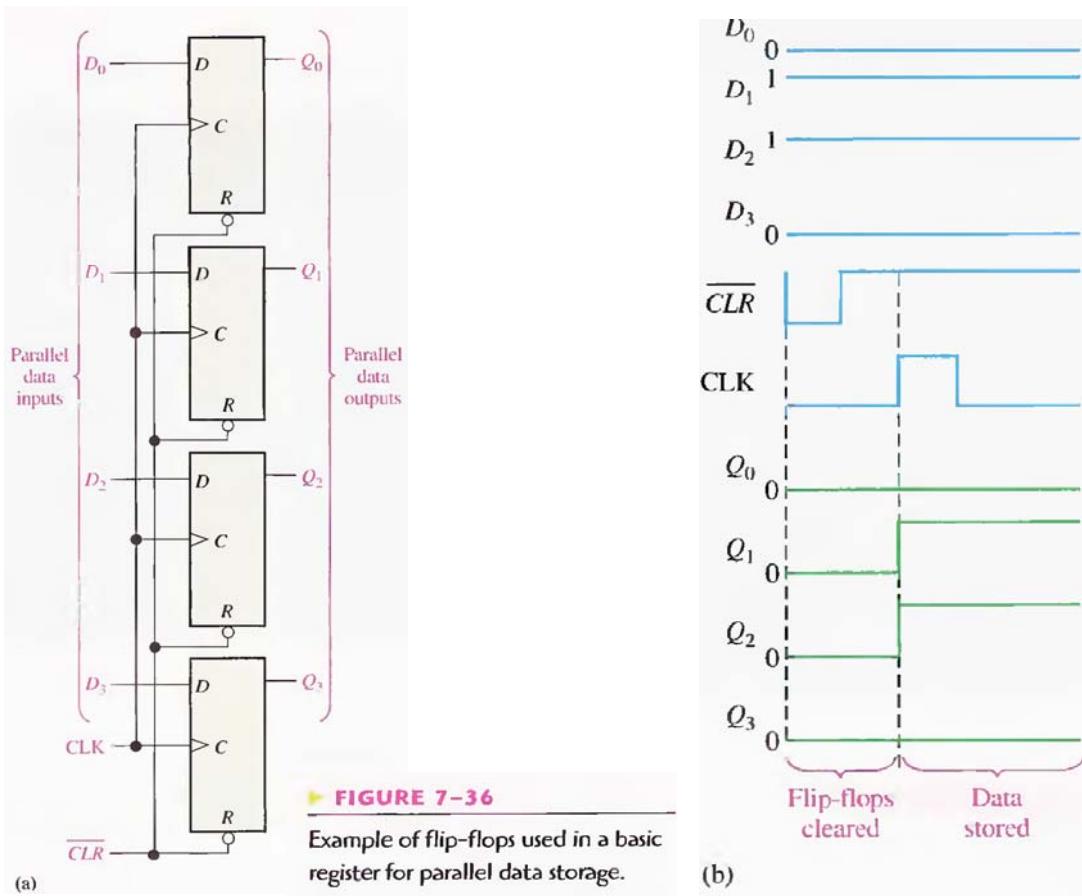
$$I = \frac{250 \text{ mW}}{5 \text{ V}} = 50 \text{ mA}$$

You must use a +5 V dc supply that is capable of providing at least 50 mA of current.

FLIP-FLOP APPLICATIONS

Parallel Data Storage

- A common requirement in digital systems is to store several bits of data from parallel lines simultaneously in a group of flip-flops.
- Each of the four parallel data lines is connected to the D input of a flip-flop.
- The clock inputs of the flip-flops are connected together, so that each flip-flop is triggered by the same clock pulse.
- In this example, positive edge-triggered flip-flops are used.
- The asynchronous reset (R) inputs are connected to a common CLR line, which resets all the flip-flops.

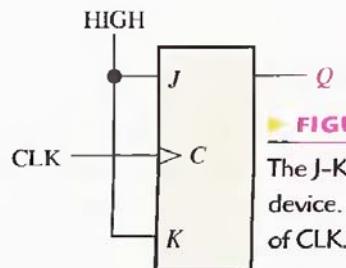


Frequency Division

Another application of a flip-flop is dividing (reducing) the frequency of a periodic waveform. When a pulse waveform is applied to the clock input of a J-K flip-flop that is connected to toggle ($J = K = 1$), the Q output is a square wave with one-half the frequency of the clock input. Thus, a single flip-flop can be applied as a divide-by-2 device, as is illustrated in Figure 7-37.

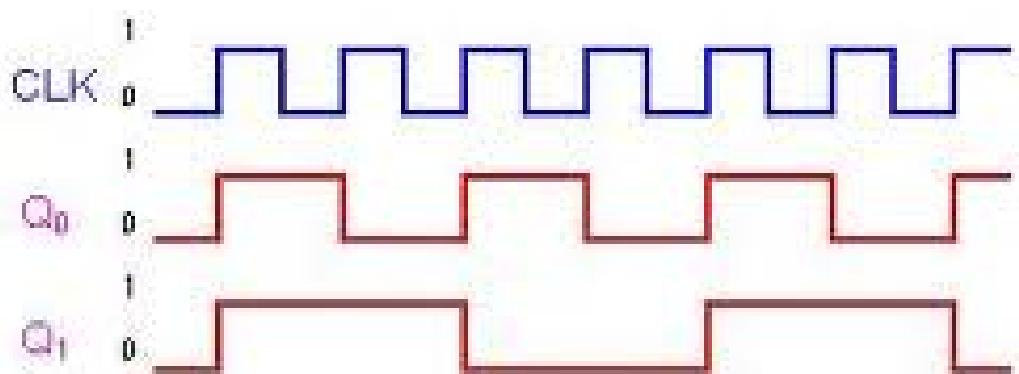
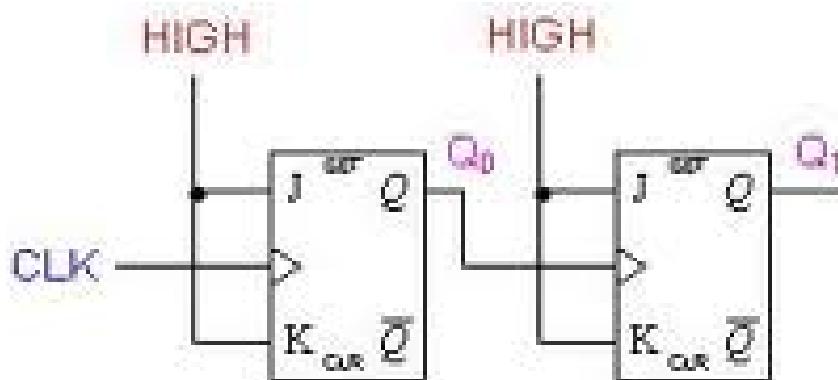
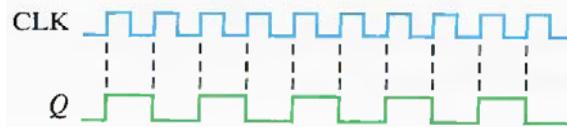
► FIGURE 7-37

The J-K flip-flop as a divide-by-2 device. Q is one-half the frequency of CLK.

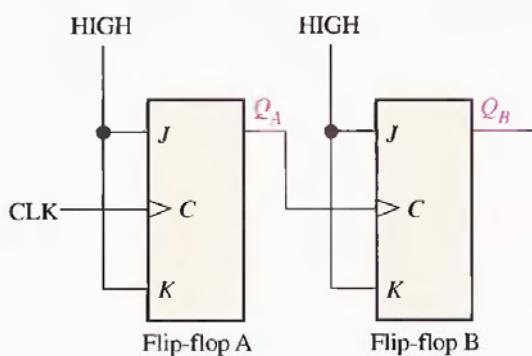


► FIGURE 7-37

The J-K flip-flop as a divide-by-2 device. Q is one-half the frequency of CLK.

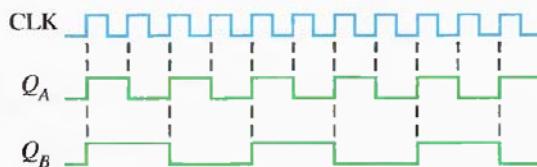


Further division of a clock frequency can be achieved by using the output of one flip-flop as the clock input to a second flip-flop, as shown in Figure 7–38. The frequency of the Q_A output is divided by 2 by flip-flop B. The Q_B output is, therefore, one-fourth the frequency of the original clock input. Propagation delay times are not shown on the timing diagrams.



◀ FIGURE 7–38

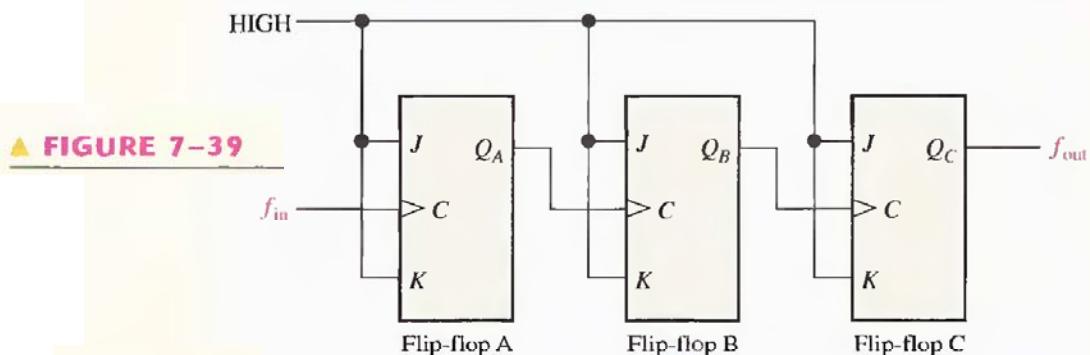
Example of two J-K flip-flops used to divide the clock frequency by 4. Q_A is one-half and Q_B is one-fourth the frequency of CLK.



By connecting flip-flops in this way, a frequency division of 2^n is achieved, where n is the number of flip-flops. For example, three flip-flops divide the clock frequency by $2^3 = 8$; four flip-flops divide the clock frequency by $2^4 = 16$; and so on.

EXAMPLE 7-10

Develop the f_{out} waveform for the circuit in Figure 7–39 when an 8 kHz square wave input is applied to the clock input of flip-flop A.



Solution

The three flip-flops are connected to divide the input frequency by eight ($2^3 = 8$) and the f_{out} waveform is shown in Figure 7–40. Since these are positive edge-triggered flip-flops, the outputs change on the positive-going clock edge. There is one output pulse for every eight input pulses, so the output frequency is 1 kHz. Waveforms of Q_A and Q_B are also shown.

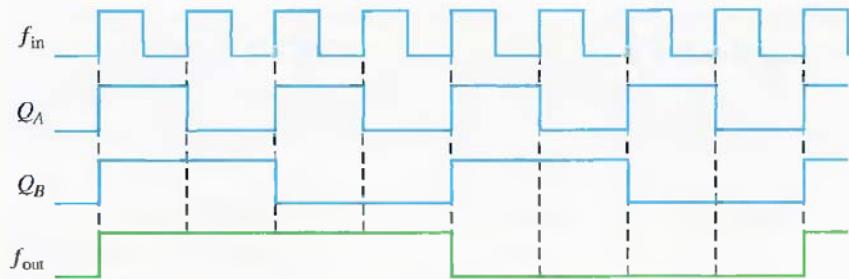


FIGURE 7-40

Related Problem How many flip-flops are required to divide a frequency by thirty-two?

Counting

Another important application of flip-flops is in digital counters,

The concept is illustrated in Figure 7-41. The flip-flops are negative edge-triggered J-Ks. Both flip-flops are initially RESET. Flip-flop A toggles on the negative-going transition of each clock pulse. The Q output of flip-flop A clocks flip-flop B, so each time Q_A makes a HIGH-to-LOW transition, flip-flop B toggles. The resulting Q_A and Q_B waveforms are shown in the figure.

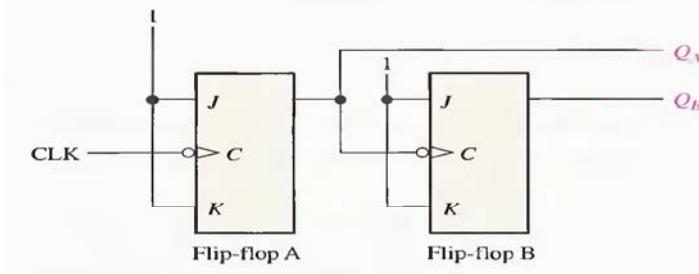
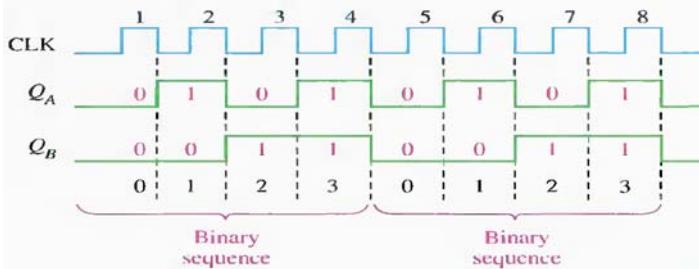
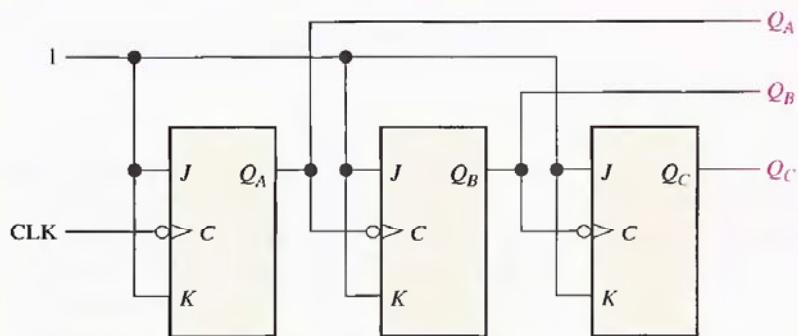


FIGURE 7-41

Flip-flops used to generate a binary count sequence. Two repetitions (00, 01, 10, 11) are shown.



EXAMPLE 7-11 Determine the output waveforms in relation to the clock for Q_A , Q_B , and Q_C in the circuit of Figure 7-42 and show the binary sequence represented by these waveforms.



▲ FIGURE 7-42

Solution The output timing diagram is shown in Figure 7-43. Notice that the outputs change on the negative-going edge of the clock pulses. The outputs go through the binary sequence 000, 001, 010, 011, 100, 101, 110, and 111 as indicated.

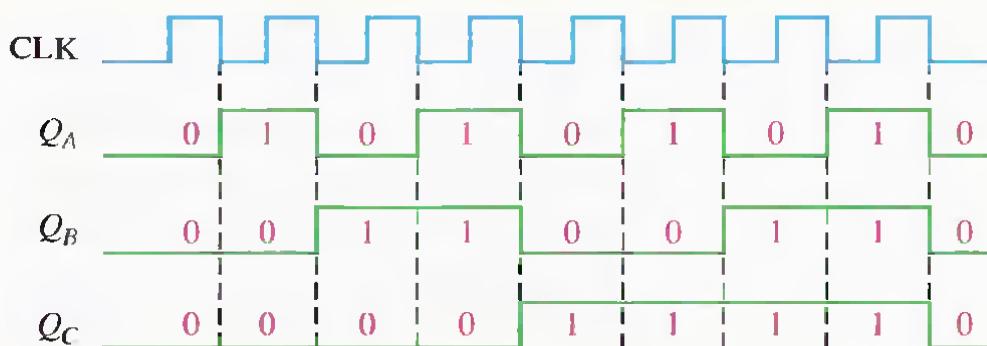


FIGURE 7-43

Related Problem How many flip-flops are required to produce a binary sequence representing decimal numbers 0 through 15?

J-K Flip-Flop

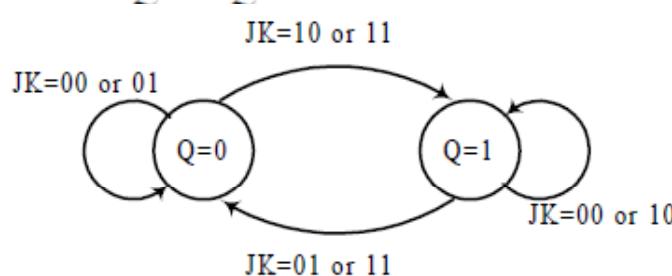
<i>J</i>	<i>K</i>	<i>Q</i>	<i>Q_{next}</i>
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

Excitation Table

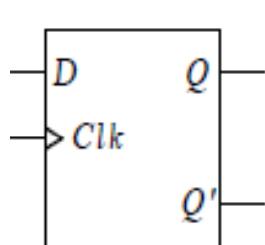
<i>Q</i>	<i>Q_{next}</i>	<i>J</i>	<i>K</i>
0	0	0	×
0	1	1	×
1	0	×	1
1	1	×	0

Characteristic Equation

$$\begin{aligned} Q_{\text{next}} &= J'K'Q + JK'Q + JK'Q' + JKQ' \\ &= K'Q(J'+J) + JQ'(K'+K) \\ &= K'Q + JQ' \end{aligned}$$

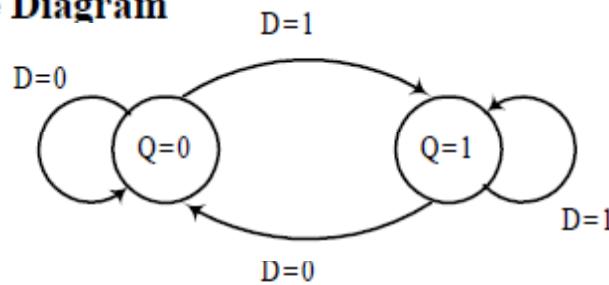


D



<i>D</i>	<i>Q</i>	<i>Q_{next}</i>
0	×	0
1	×	1

State Diagram



Characteristic Equation

$$Q_{\text{next}} = D$$

Excitation Table

<i>Q</i>	<i>Q_{next}</i>	<i>D</i>
0	0	0
0	1	1
1	0	0
1	1	1