Student Name & Roll # :_____ Do not write anything on this sheet.

Instructions	Opcode	'mod rm' Byte	Opcode Extension
ADD reg8/mem8, reg8	00	yes	
ADD reg16/mem16, reg16	01	yes	
ADD reg8, mem8	02	yes	
ADD reg16, mem16	03	yes	
ADD AL, imm8	04	no	
ADD AX, imm16	05	no	
ADD reg8/mem8, imm8	80	yes	000
ADD reg16/mem16, imm16	81	yes	000
ADD reg16/mem16, imm8	83	yes	000
CALL Selector: Offset	9A	no	
CALL Offset	E8	no	
CALL reg16/mem16	FF	yes	010
CBW	98	no	
CMP reg8/mem8, reg8	38	yes	
CMP reg16/mem16, reg16	39	yes	
CMP reg8, mem8	3A	yes	
CMP reg16, mem16	3B	yes	
CMP AL, imm8	3C	no	
CMP AX, imm16	3D	no	
CMP reg8/mem8, imm8	80	yes	111
CMP reg16/mem16, imm16	81	yes	111
CMP reg16/mem16, imm8	83	yes	111
CWD	99	no	
DEC reg16	48 + regcd		
DEC reg8/mem8	FE	yes	001
DEC reg16/mem16	FF	yes	001
DIV reg8/mem8	F6	yes	110
DIV reg16/mem16	F7	yes	110
IDIV reg8/mem8	F6	yes	111
IDIV reg16/mem16	F7	yes	111

Instructions	Opcode	'mod rm' Byte	Opcode Extension
IMUL reg8/mem8	F6	yes	101
IMUL reg16/mem16	F7	yes	101
INC reg16	40 + regcd	no	
INC reg8/mem8	FE	yes	000
INC reg16/mem16	FF	yes	000
INT 3	CC	no	
INT type imm8	CD	no	
JB/JNAE ShortOffset	72	no	
JBE/JNA ShortOffset	76	no	
JCXZ ShortOffset	E3	no	
JE/JZ ShortOffset	74	no	
JG/JNLE ShortOffset	7F	no	
JGE/JNL ShortOffset	7D	no	
JL/JNGE ShortOffset	7C	no	
JLE/JNG ShortOffset	7E	no	
JMP ShortOffset	EB	no	
JMP Offset	E9	no	
JMP reg16/mem16	FF	yes	100
JMP Selector:Offset	EA	no	
JNB/JAE ShortOffset	73	no	
JNBE/JA ShortOffset	77	no	
JNE/JNZ ShortOffset	75	no	
JNO ShortOffset	71	no	
JNP/JPO ShortOffset	7B	no	
JNS ShortOffset	79	no	
JO ShortOffset	70	no	
JP/JPE ShortOffset	7A	no	
JS ShortOffset	78	no	
LOOP ShortOffset	E2	no	
LOOPNZ/LOOPNE ShortOffset	E1	no	

Instructions	Opcode	'mod rm' Byte	Opcode Extension
LOOPZ/LOOPE ShortOffset	E0	no	
MOV reg8/mem8, reg8	88	yes	
MOV mem8, AL	A2	no	
MOV reg16/mem16, reg16	89	yes	
MOV mem16, AX	A3	no	
MOV reg8, mem8	8A	yes	
MOV AL, mem8	A0	no	
MOV reg16, mem16	8B	yes	
MOV AX, mem16	A1	no	
MOV reg8, imm8	B0 + regcd	no	
MOV reg16, imm16	B8 + regcd	no	
MOV Sreg, reg16/mem16	8E	yes	
MOV reg16/mem16, Sreg	8C	yes	
MOV mem8, imm8	C6	yes	000
MOV mem16, imm16	C7	yes	000
MUL reg8/mem8	F6	yes	100
MUL reg16/mem16	F7	yes	100
NEG mem8/reg8	F6	yes	011
NEG mem16/reg16	F7	yes	011
POP mem16	8F	yes	000
POP reg16	58 + regcd	no	
POP Sreg	000regcd111	no	
PUSH mem16	FF	yes	110
PUSH reg16	50 + regcd	no	
PUSH Sreg	000regcd110	no	
RET	C3	no	

Instructions	Opcode	'mod rm' Byte	Opcode Extension
RET imm16	C2	no	
RETF imm16	CA	no	
RETF	CB	no	
SUB mem8/reg8, reg8	28	yes	
SUB mem16/reg16, reg16	29	yes	
SUB reg8, mem8	2A	yes	
SUB reg16, mem16	2B	yes	
SUB AL, imm8	2C	no	
SUB AX, imm16	2D	no	
SUB reg8/mem8, imm8	80	yes	101
SUB reg16/mem16, imm16	81	yes	101
SUB reg16/mem16, imm8	83	yes	101
XCHG mem8/reg8, reg8	86	yes	
XCHG reg8, mem8	86	yes	
XCHG mem16, reg16	87	yes	
XCHG reg16, mem16/reg16	87	yes	
XCHG reg16, AX	90 + regcd	no	

CODE	EXPLANATION
00	Memory Mode, no displacement follows*
01	Memory Mode, 8-bit displacement follows
10	Memory Mode, 16-bit displacement follows
11	Register Mode (no displacement)

*Except when R/M = 110, then 16-bit displacement follows

(a)

Segment Override	
00	ES
01	CS
10	SS
11	DS

SOP byte 001 XX 110

REG field is used to identify the register for the first operand

REG	W = 0	W = 1
000	AL	AX
001	CL	CX
010	DL	DX
011	BL	BX
100	AH	SP
101	CH	BP
110	DH	SI
111	BH	DI

MOD = 11			EFFECTIVE ADDRESS CALCULATION			
R/M	W = 0	W = 1	R/M	MOD = 00	MOD = 01	MOD = 10
000	AL	AX	000	(BX) + (SI)	(BX) + (SI) + D8	(BX) + (SI) + D16
001	CL	CX	001	(BX) + (DI)	(BX) + (DI) + D8	(BX) + (DI) + D16
010	DL	DX	010	(BP) + (SI)	(BP) + (SI) + D8	(BP) + (SI) + D16
011	BL	BX	011	(BP) + (DI)	(BP) + (DI) + D8	(BP) + (DI) + D16
100	AH	SP	100	(SI)	(SI) + D8	(SI) + D16
101	CH	BP	101	(DI)	(DI) + D8	(DI) + D16
110	DH	SI	110	DIRECT ADDRESS	(BP) + D8	(BP) + D16
111	BH	DI	111	(BX)	(BX) + D8	(BX) + D16