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Section 01

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Lab 3: Combinational Logic Circuit

Purpose

In the investigation, the combinational circuit will aim to design by using an integrated circuit on the breadboard. Also, the research focuses on learning how to read the datasheet of electric components for use in the circuits.

Design Specifications

Multiplexer was used as a combinational circuit, which was also used in the second lab. The difference between the combinational circuit from the previous lab was the number of inputs and outputs. There were 2 data inputs (X1, X0), one selective input (S), and one output (F). The sum of products (SOP) of a 2-to-1 multiplexer was $\bar{S}X0 + SX1$. If only NAND gates were used to create the sum of products implantation of 2-to-1 multiplexer, 4 two-input NAND gates were needed. The schematic of the sum of products of a 2-to-1 multiplexer was figure 1.

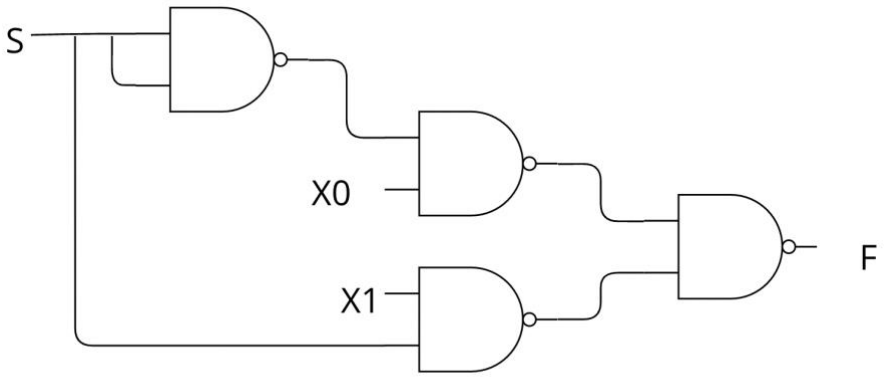

Figure 1 Schematic of SOP implantation

In the design model, the 2-to-1 multiplexer is generated by using quad 2-input NAND gates (74HC00). The input signals were generated by the 4-bit counter (74HC163). The outputs of the 4-bit counter (74HC163) were Q0, Q1, Q2, and Q3. Q1, Q2, and Q3 were used in the experiment. Q1 and Q2 were data inputs (X1, X0) in an orderly. Q3 is the selective input of the multiplexer. All outputs and inputs were observed by the LEDs in the breadboard. The truth table of the 2-to-1 multiplexer is table 1.

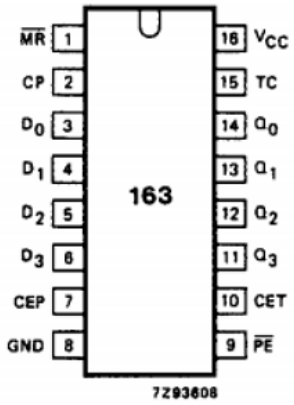

Figure 2 The pinouts of 74HC163

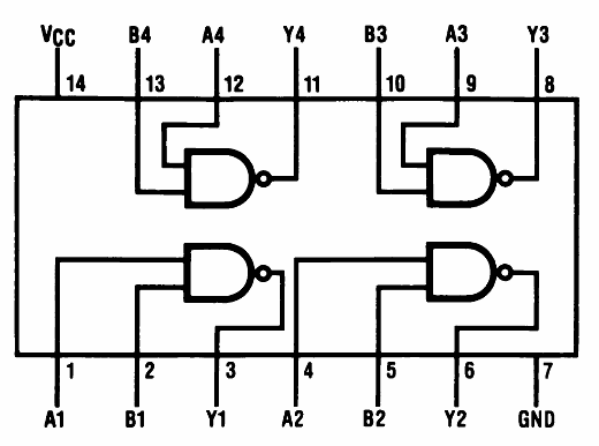

Figure 3 The pinouts of 74HC00

S	X1	X0	F
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

Table 1 Truth Table of 2-to-1 Multiplexer

Methodology

The methodology of the investigation consists of two parts. The 4-bit counter connections between the led, the power source, and the signal generator were made in the first part of the experiment. The 4-bit counter has 16 pins, which is shown in figure 2. VCC pin was connected to the positive power rail of the breadboard. The GND pin was connected to the negative power rail of the breadboard. Some pins of the 74HC163 needed to get inputs to activate the counter mode. The values of the pins were written in the datasheet. The $\overline{MR}$, CEP, CET, and $\overline{PE}$ pins were linked to the positive power rail of the breadboard. The output pins were connected to LEDs on the left side of the breadboard. The green LEDs represented the data inputs (X0, X1). The red LED was assigned to the selective input(S) of the multiplexer. All LED connections contained 1kΩ resistor in series.

A power source was fixed at 5 Volts. The power source's positive probe was put in the positive power rail. The negative probe of the power source was connected to the negative power rail. Additionally, the signal generator was arranged to create a 5 Vpp, 1.25V DC offset, 1 Hz frequency and square waveform. The positive probe of the signal generator was connected to the CP pin of 74HC163. The negative probe of the signal generator was linked to the negative power rail.

Moreover, the other part of the methodology is making the connections of 74HC00. The 74HC00 had 14 pins. The VCC pin and GND pin connection were the same as the connection 74HC163's GND and VCC pin. The sop implantation of a 2-to-1 multiplexer was applied in 74HC00. In the first NAND gate circuit, B4 and A4 were connected to the selective pin of mux. Y4 was connected to B3, and A3 was connected to the X0 pin of the multiplexer. Another NAND

gate logic circuit, A1 was connected to the selective pin, and B1 was connected to the X1. The result of it was connected to the A2 pin, and the B2 pin was connected to the Y3 pin. The final NAND gate circuit's result connected the red LED with 1kΩ in series.

Results

The final waveform generated by the circuit was observed at the oscilloscope. The graph that came from the oscilloscope was figure 4. The result was the same as expected. The type of waveform was the square waveform. For instance, the selective input was 0, and the data inputs (X1, X0) were 0 and 1 in orderly at the grey circle point in figure 4. The output(F) was high at that time.

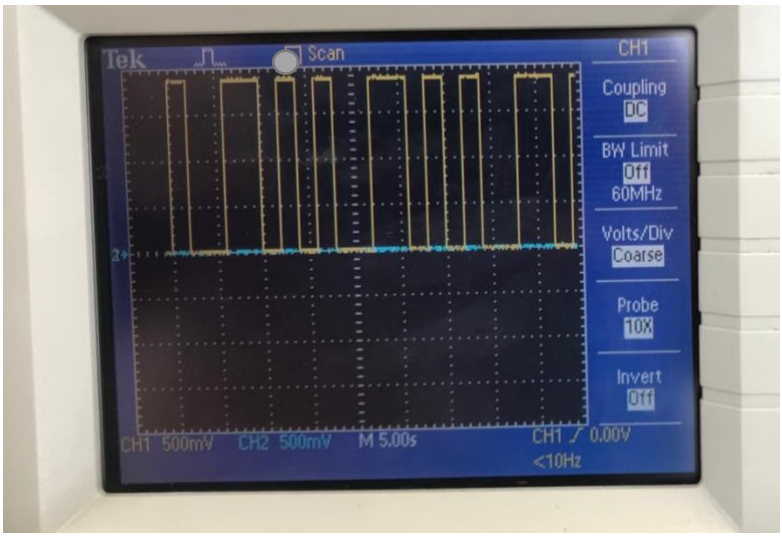

Figure 4 The output waveform of 2-to-1 Multiplexer

The result at the breadboard did not have an arbitrary result. For instance, figure 5 was one of the phases of the combinational circuit. The output LED was activated when the selective and data inputs were 1, 1, and 0 in order. There were also photos of other phases of the circuit in the breadboard in the appendix.

Conclusion

The investigation focuses on designing a combinational circuit on the breadboard. The datasheet of the integrated circuits had to be read during the design of the combinational circuit on the breadboard. The aim of the investigation was to obtain a simulation of the combinational circuit and compare the result of the simulation and the truth table of the combinational circuit. The significant problem faced in the experiment was that the 4-bit counter(74HC163) did not work properly in the initial part of the investigation. The connections of pins were not made according to the datasheet. The issue was solved when the links were made according to the datasheet. Additionally, quad 2 input NAND gate IC (74HC00) did not generate the output of $\bar{S}X0$. For troubleshooting, the location of 74HC00 was changed, and the circuit began to give the correct output.

Works Cited

Sharma, M. (2015). 74HC00-Quad 2-input NAND gate. Retrieved October 24, 2022, from https://www.bragitoff.com/wp-content/uploads/2015/01/74hc00.gif.

Appendix

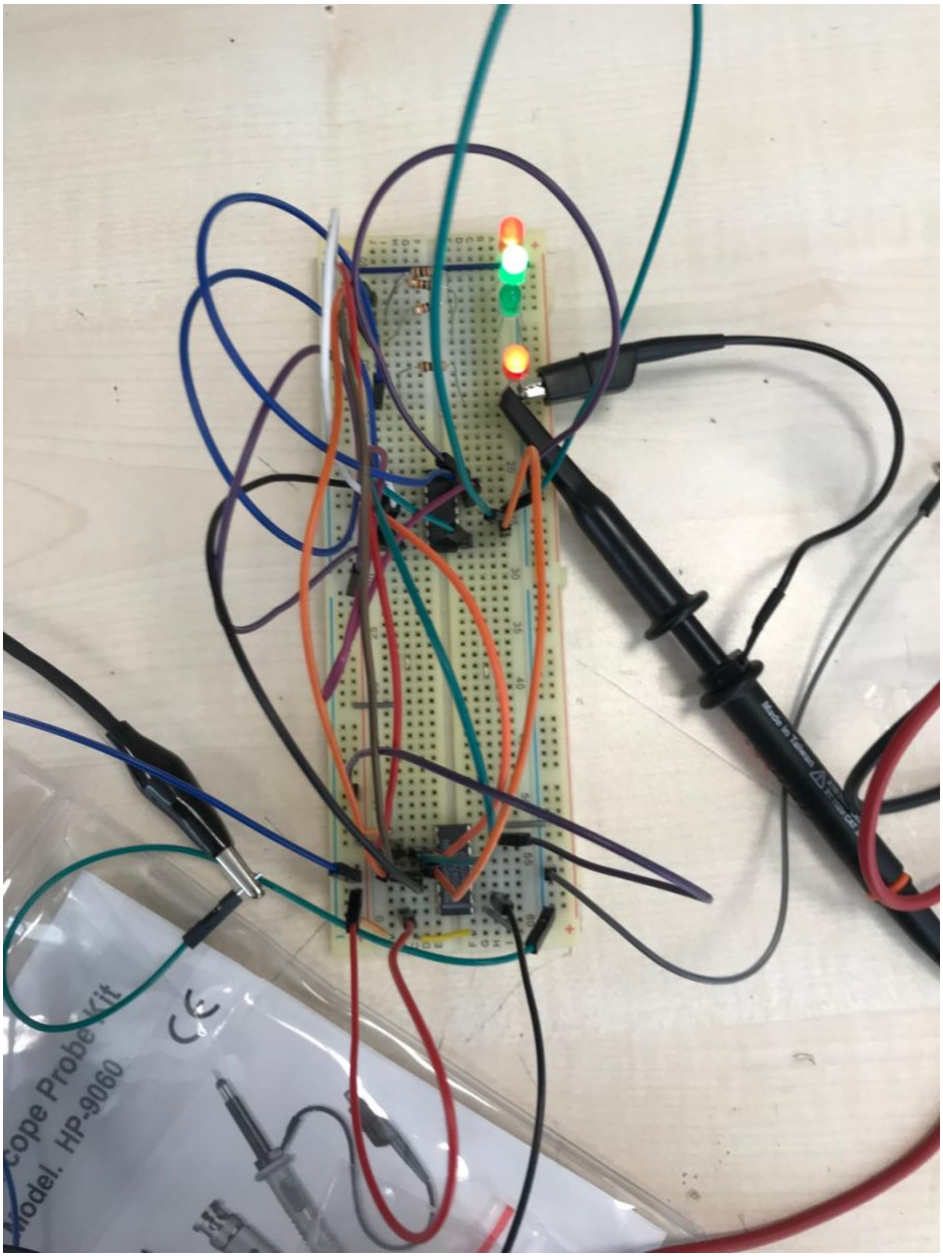

Figure 5 The output led on when S and X1 high X0 low

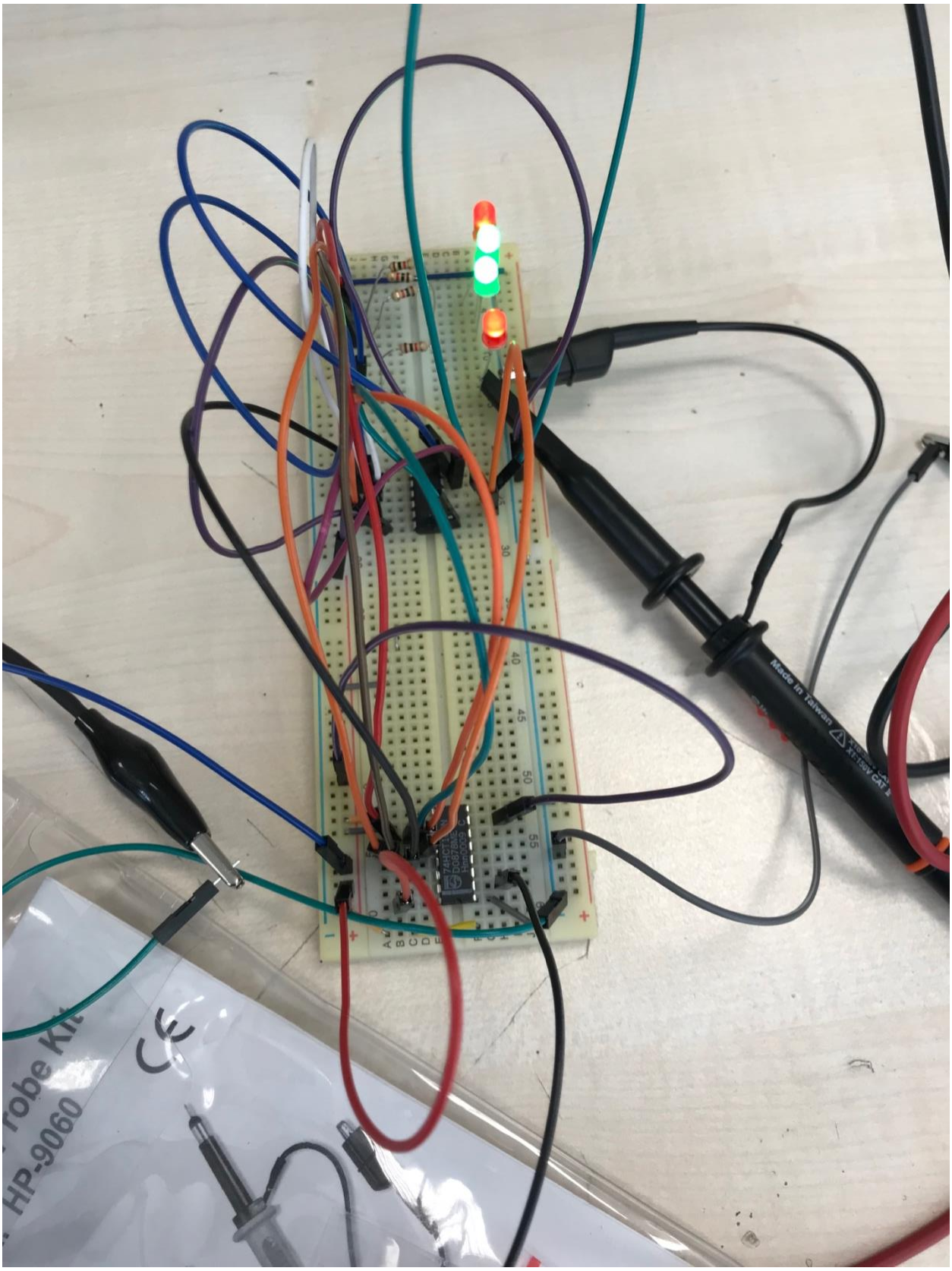

Figure 6 The output led on when S, X0 and X1 high

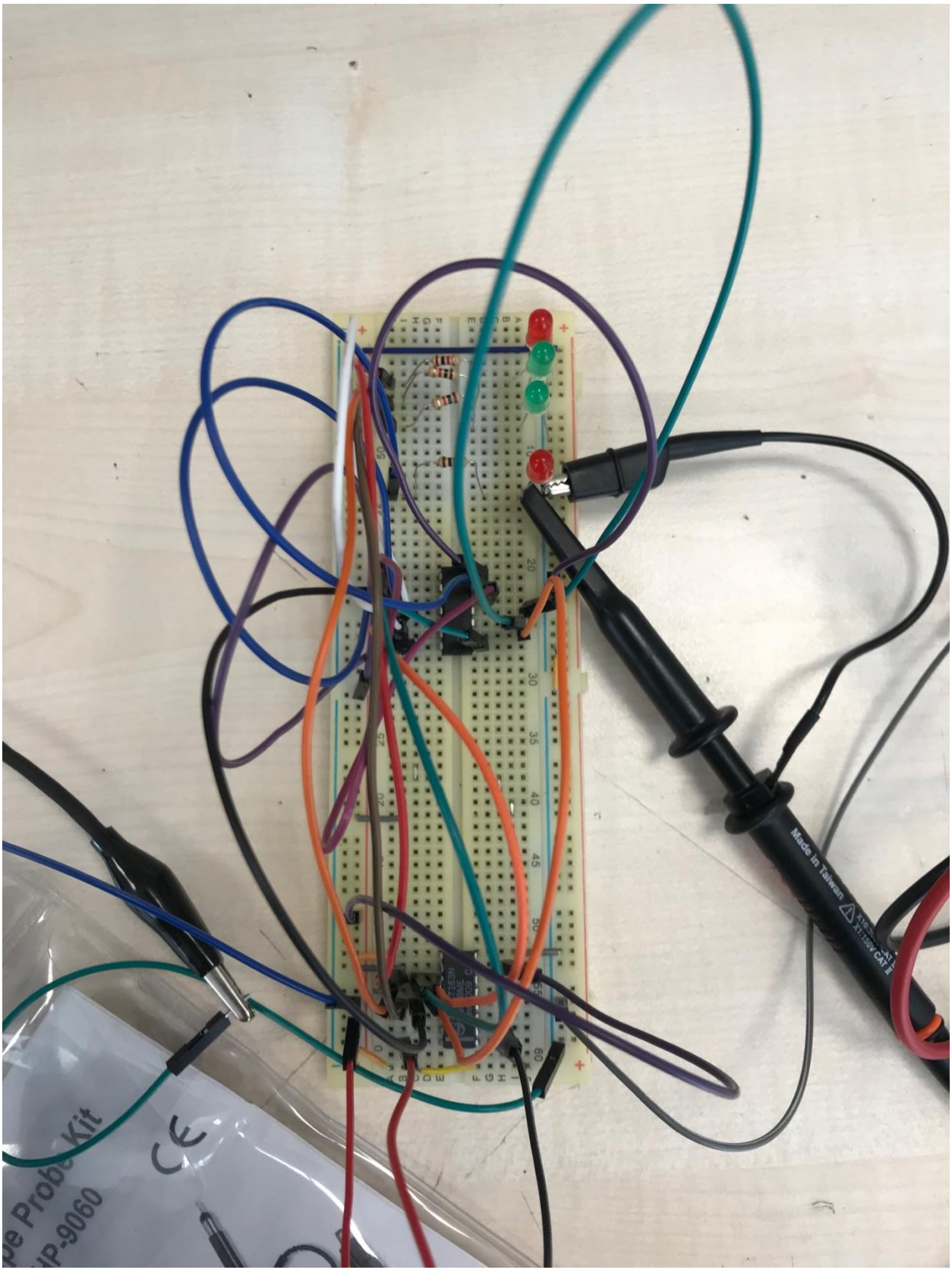

Figure 7 The output led off when S, X0 and X1 low