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Section 1

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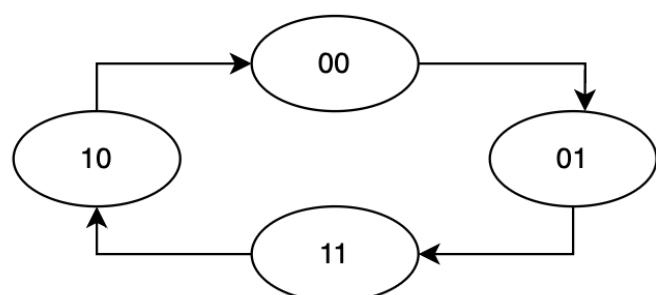
## Lab 7: Finite State Machine

### Purpose

The objective of lab is to design a Finite State Machine circuit on the breadboard by using integrated circuits.

### Design Specifications

There are four states in the Finite State Machine. The initial state is Q0 and Q1 is 0. After one clock cycle, it passes to the next state, which is Q0 is 1 and Q1 is 0. In the next state, Q1 and Q0 become 1. In the final state, Q0 becomes 0 and Q1 is 1. Finally, the final state passes to the initial condition. When the reset button is pressed, the FSM circuit returns to the initial condition and starts counting. The state diagram of the Finite State Machine is in figure 1. The output table of the FSM circuit is table 1. The state 1, 2, 3, and 4 00, 01, 11, and 10 respectively.

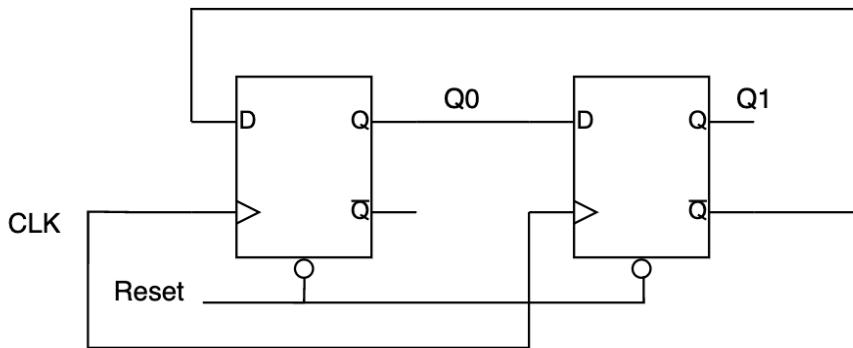


**Figure 1** State Transmission Diagram of FSM

Present State	Next State					Output
$Q_1 Q_0$	$Q_1^+ Q_0^+$	00	01	11	10	$Q_1^+ Q_0^+$
(S1)00		xx	01	xx	xx	01
(S2)01		xx	xx	11	xx	11
(S3)11		xx	xx	xx	10	10
(S4)10		00	xx	xx	xx	00

**Table 1** Output Table of FSM

The design the Finite State Machine contains two D flip flops since total number of the states is four. The output  $Q$  of the first D flip flop is connected to the D input of the second D flip flop. The output  $\bar{Q}$  of the second D flip flop is connected to the D input of the first flip flop. The circuit is synchronous, so the all d flip flops is attached to the same clock. Both clear input of D -flip flop is connected to the start button.



**Figure 2** Schematics of Experiment Circuit

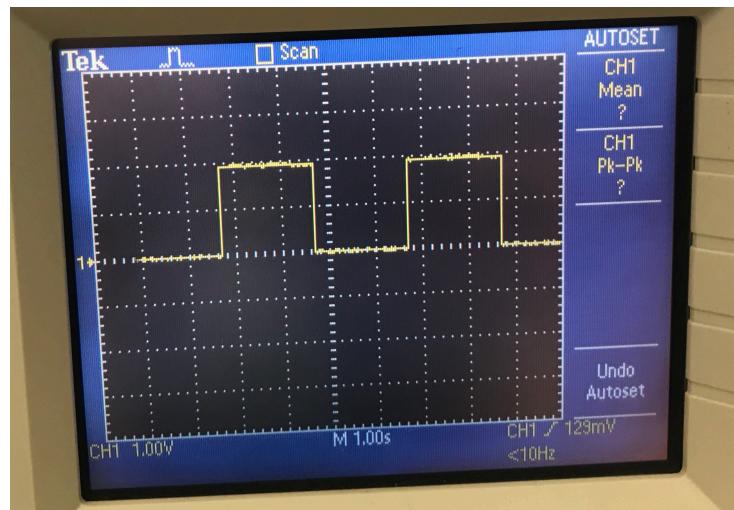
## Methodology

In the design of the experiment setup, the 2 D-flip flop integrated circuit, which is 74HC74, is used. The Vcc pin of 74HC74 is connected to the power supply that generates a 5 V DC voltage. Both of the clock pins of the D flip flop are assigned to the positive output of the signal generator. The first D flip flop is connected to the output of  $\bar{Q}$  the second D flip flop. Furthermore, the D input of the second D flip flop is defined as the output of  $Q$  the first D flip flop. The outputs are linked to LEDs which are connected with a  $1.2 \text{ k}\Omega$  resistor. The red LED represents Q1. The green LED represents Q0. The cathode pins of LEDs are connected to the negative power rail of the

breadboard. One pin of the push button is connected to the Vcc connection in the breadboard. The other pin of the push button is linked to the clear pins of the d-flip flop. The 3.3 Volt peak to peak voltage, 1 Hz frequency, 1.65 Volt DC offset and square wave are applied to the circuit by the signal generator. The ground pin of the signal generator, 74HC74, and power supply are connected to the negative power in the breadboard.

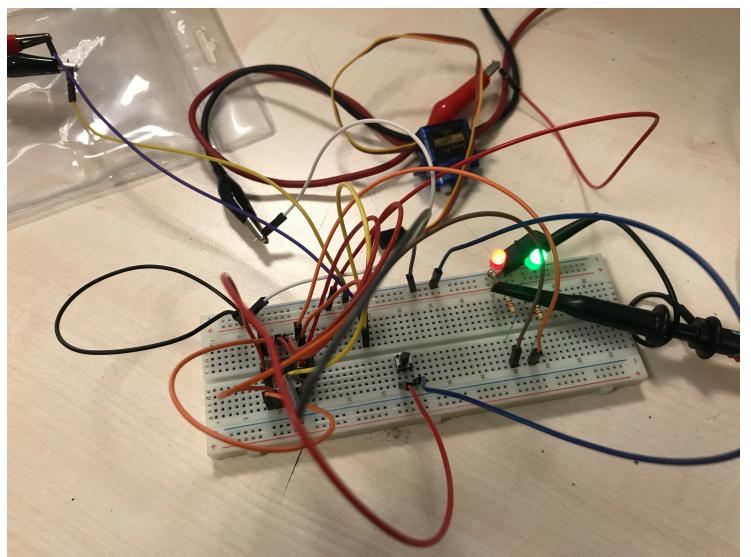
## Results

The result came from the oscilloscope same as expected. In the four clock cycles the outputs comes to their initial position. The figure 3 is the waveform graph of Q1 which is observed in the oscilloscope. The Q1 becomes high for 2 clock period and falls down to zero for 2 clock period.



**Figure 3** The waveform graph of Q1

The result at the breadboard did not have an arbitrary result. For instance, figure 4 was one of the states of the FSM circuit. The output LED was become lights in the second clock cycle. There were also photos of other states of the circuit in the breadboard in the appendix.

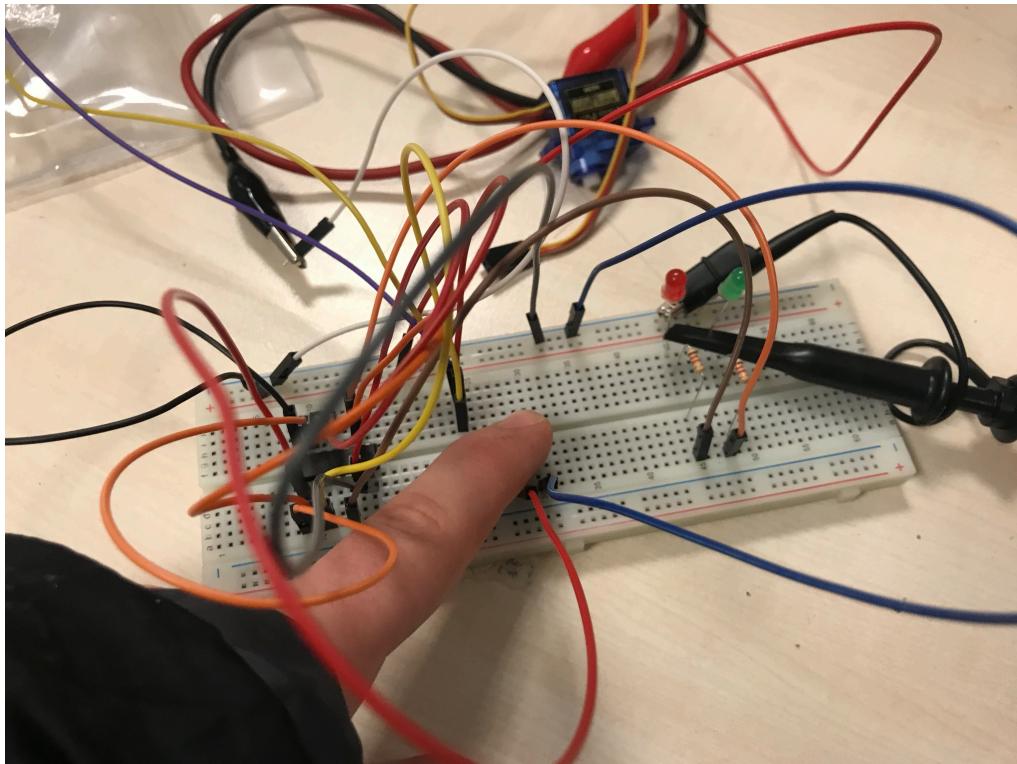


**Figure 4** Q1 and Q0 become 1 in the second clock cycle (State 3)

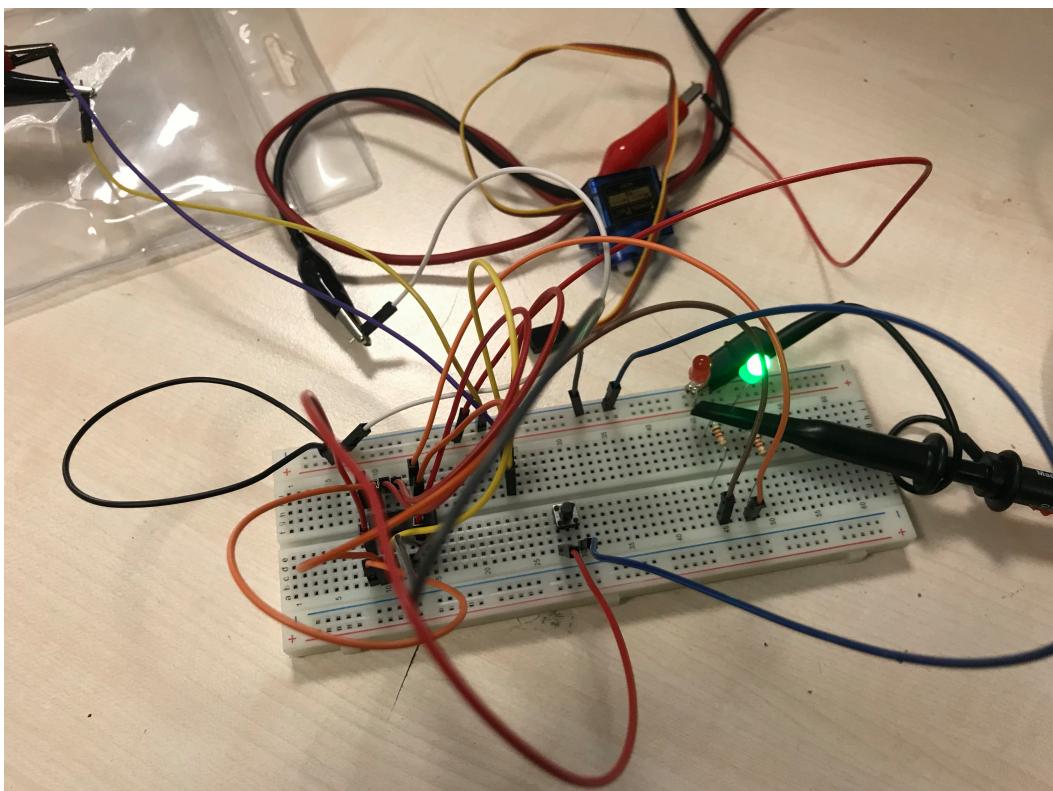
## **Conclusion**

The experiment aims to create a Finite State Machine on the breadboard via the integrated circuit. Also, the lab will aim to understand the FSM circuit design by creating the state transition diagram and output table for the FSM circuit. The type of FSM is a Moore machine. The structure of the ring structure. This circuit is called 2-bit Johnson Counter. The most challenging part of the lab is selecting the working 74HC74. Most of the ICs do not work, so it is hard to find a working one.

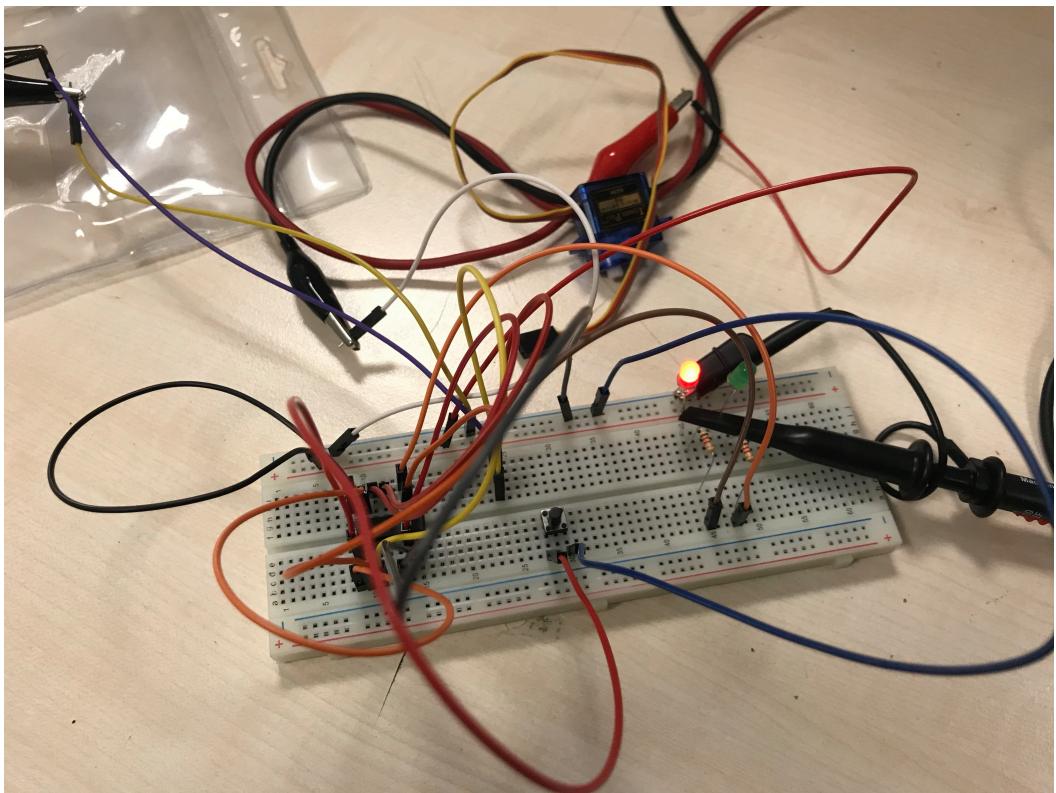
## Appendix



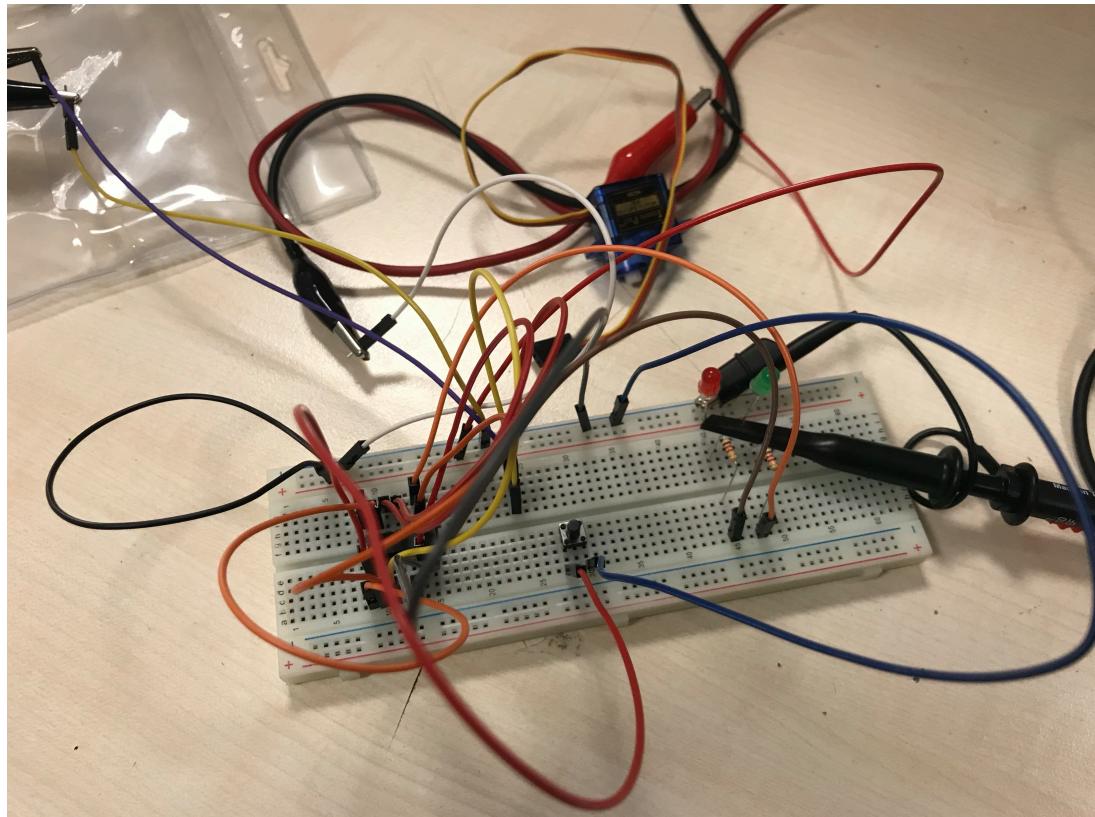
**Figure 5** When the reset button is active Q1 and Q0 becomes 0



**Figure 6** Q1 become 0 and Q0 becomes 1 in the first clock cycle (State 2)



**Figure 7** Q1 become 1 and Q0 becomes 0 in the third clock cycle (State 4)



**Figure 8** Q1 and Q0 become 0 in the fourth clock cycle (State 1)