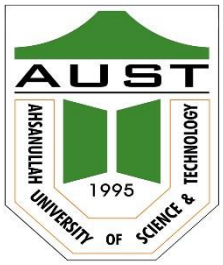

Ahsanullah University of Science and Technology (AUST)
Department of Computer Science and Engineering

LAB REPORT

Course No. : CSE2210

Course Title: Digital Electronics and Pulse Techniques Lab

Experiment Number:03

Name of the Experiment: Study of a TTL NAND gate with totem-pole output.

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Name of Experiment:

Study of a TTL NAND Gate with totem-pole output.

Objective:

Study of a TTL (Transistor-Transistor Logic) NAND gate with totem-pole output and measuring the voltages at various point for all possible input combinations and also finding noise margins.

Circuit Diagram:

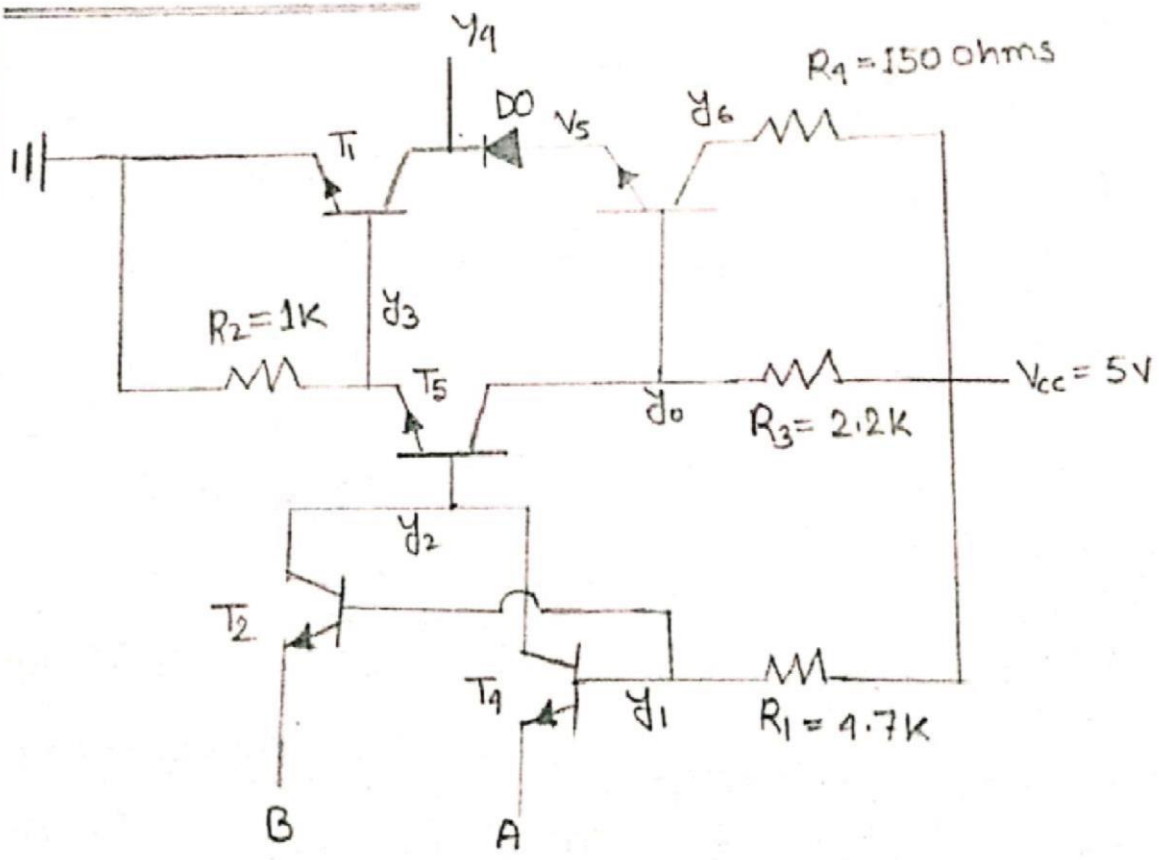

Figure: TTL NAND gate.

Answering to the Questions:

1. Analyze the operation of TTL NAND gate with the experimental data.

Answer: In this experiment, we have set a circuit to check a TTL NAND gate properties in proteous 8 software.

In this circuit we have used 5 transistors 4 registers and 1 diode. We have given input voltage A and B. For two input voltage we have four i/o combination.

A	B	V_o (volt)
0	0	5.00
0	1	5.00
1	0	5.00
1	1	0.66

When we give both input 1, it gives the output of low voltage which 0.66 volt close to 0 voltage and for other input combinations it gives high voltage output which is 5.00 volt. From this data we can say the circuit hold NAND gate properties

2. What are differences of transistors T_1 and T_2 with that of a multi-emitter transistors?

Answer: The difference of transistor T_1 and T_2 with that of a multi-emitter transistor are:

1. The Transistor in which number of emitter are more than one is called multi-emitter transistors. In T_1 and T_2 transistors there is only one emitter.

2. In multi-emitter transistors there is connection of every emitter with a diode which are acting as an input diode. But in T_1 and T_2 there is no connection of emitter and diode.

3. What is totem-pole stage? why it is used in place of passive pull-up resistor?

Answer:

Totem-pole stage: Totem pole means the addition of an active pull up the circuit in the output of the gate. The TTL output stage is rather complicated push-pull circuit known as a totem pole output. It sinks current better than it source current.

In this circuit, it is use to output delay reduce by decreasing passive pull-up resistor (R_C). But this will increase the power disipation. When the output is in it's low state. and the voltage across R_C is $V_{CC} = V_{CE(sat)}$.

To solve this problem Totem-pole stage is used in place of passive pull-up resistor.

04. What is the function of T_3?

Answer: This is a transistor T_3 which act as a phase spitter, since the emitter voltage is out of phase with the collector voltage. (for an increase in base current, the emitter voltage increases and the collector voltage decreases). So, the output is in the voltage state when T_3 is in saturation.

05. Why resistor R_4 is used?

Answer: In this experimental circuit, if the register R_4 was omitted there would result a faster change in the output from V(0) to V(1). However, the R_4 register is needed to limit the current spiles during the turn on and turn off transmmissions. In particular T_1 doesn't turn doesn't turn off as quick as T_3 turn on with both totempole transistor conducting as same time, the supply voltage would be short circuited if the R_4 resistor was missing, that's why

R_4 resistor is used.

6. Why diode D_0 is used in the circuit? Can it be placed elsewhere?

Answer: since the base of T_3 tied to the collector of T_5 then $V_{BN_3} = V_{CN_3} = 1$ V. If the output diode D_0 were missing the base to emitter voltage T_3 would be

$V_{BE} = V_{BN3} = V_{CE}(sat) = 1 - 0.2V = 0.8V$ which would put T_3 into saturation. So, if we don't use D_0, current would be wasted.

The diode D_0 can be placed from the emitter into the base of T_3. This is also used to establish TTL NAND gates.

7. Why two totem poles cannot be wire ANDed?

Answer: It should be emphasized that the wire AND connection must not be used with the totem pole driven circuit. If the output from the one gate is high while that from a second gate is low and if these two output tied together, we have exactly the situation if the R_4 resistor is not used. That's why two totem pole gates can not be wire ANDed.

8. What are the features and advantages of TTL gates?

Answer: There are some feature of of TTL gate. Those are,

(i) Noise impurity

ii) Noise margin

iii) Fan - in

IV) Fan-out

V) Power-disipation.

Advantages are:

(I) It is most rugged meaning least sysceptible to electrical damage.

II) It has strong drive capablity.

III) It is faster in some versions.

IV) It has noise immunity better than ECL but lesser than emos.

V) It has power per gate of about 1-22 mW, which is between emos and ECL.

Experimental data:

A	B	y_0 (V)	y_1 (V)	y_2 (V)	y_3 (V)	y_4 (V)	y_5 (V)	y_6 (V)
0	0	5.00	0.52	0.00	0.00	4.33	4.72	5.00
0	1	5.00	0.54	0.02	0.00	4.33	4.72	5.00
1	0	5.00	0.54	0.02	0.00	4.33	4.72	5.00
1	1	0.66	1.88	1.27	0.64	0.01	0.40	5.00

Calculation:

when the input of A and B are both high (logically high) 5.00V. T_4 and T_2 works as inverse active mode. The current I is enough for T_3 and T_1 to saturation.

In Saturation $V_{BE}(sat) = 0.8V$

Here, $V_i = 5V$

$V_0 = 0.2V$

$V_p = V_2 + V_3 + V_{BE}$

$= 1.27 + 0.64 + 0.8$

$= 2.71$

In order to take any other of the input diode to forward bias the input voltage needs to be $(2.71 - 0.6) = 2.11V$

$\therefore$ Difference $= (5 - 2.11)V$

$= 2.89V$

$\therefore NM(0) = 2.89V$

Now, Here, $\exists V_i = 0.2V$

$V_o = 5V$

V_{BE} (Cut-in) $= 0.5V$

V_p (actual) $= (0.2 + 0.7)V$

$= 0.9\ V$

V_p (req) $= V_{BE} + y_2 + y_3$

$= (0.5 + 1.27 + 0.64)$ volt

$= 2.41$ volt

Difference $= (2.41 - 0.9)$ volt

$= 1.51$ volt

$\therefore NM(1) = 1.51$ volt.

Discussion of the findings:

In this experiment we worked on a TTL NAND gate with totem pole output in proteus 8 software individually.

In this circuit when we give both input logically high then we got $y_0 = 0.65V$ as output V(0) and for others input combination we got $y_0 = 5.00V$ as output V(1).

We know that in NAND gate if both inputs are '1' the output will be '0' otherwise the output is '1'.

So, From the data we can assure that it was TTL NAND gate.

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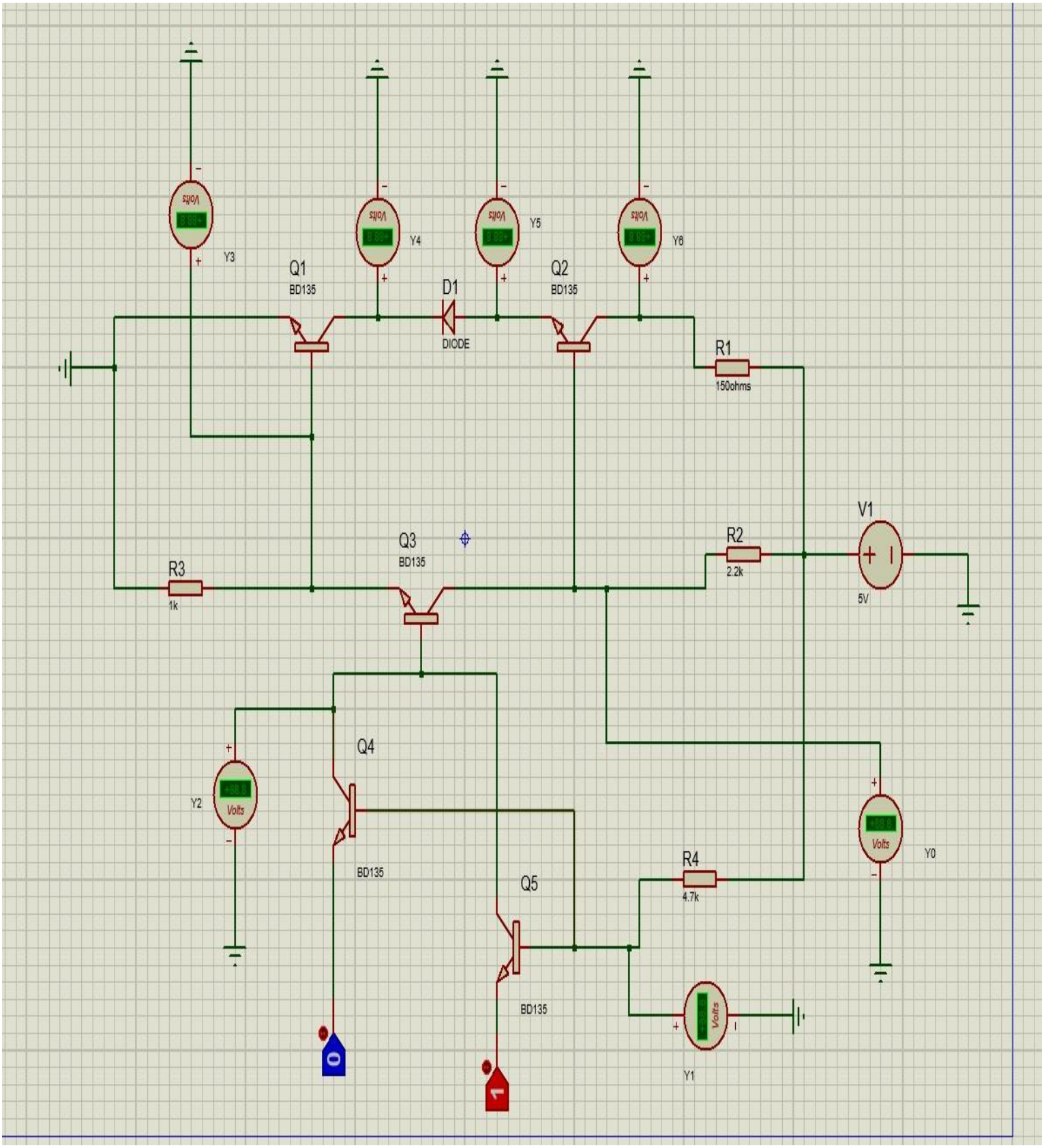

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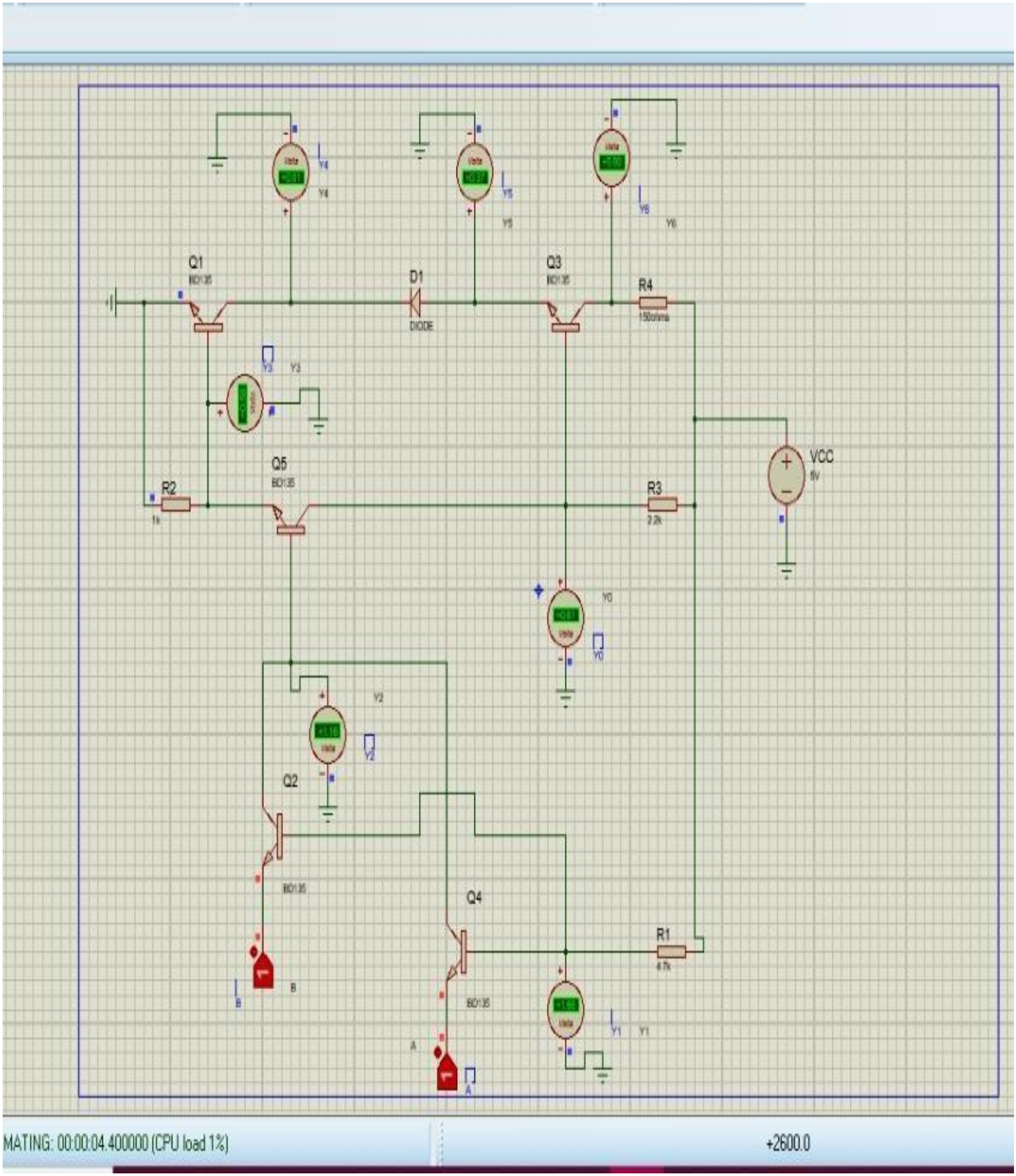

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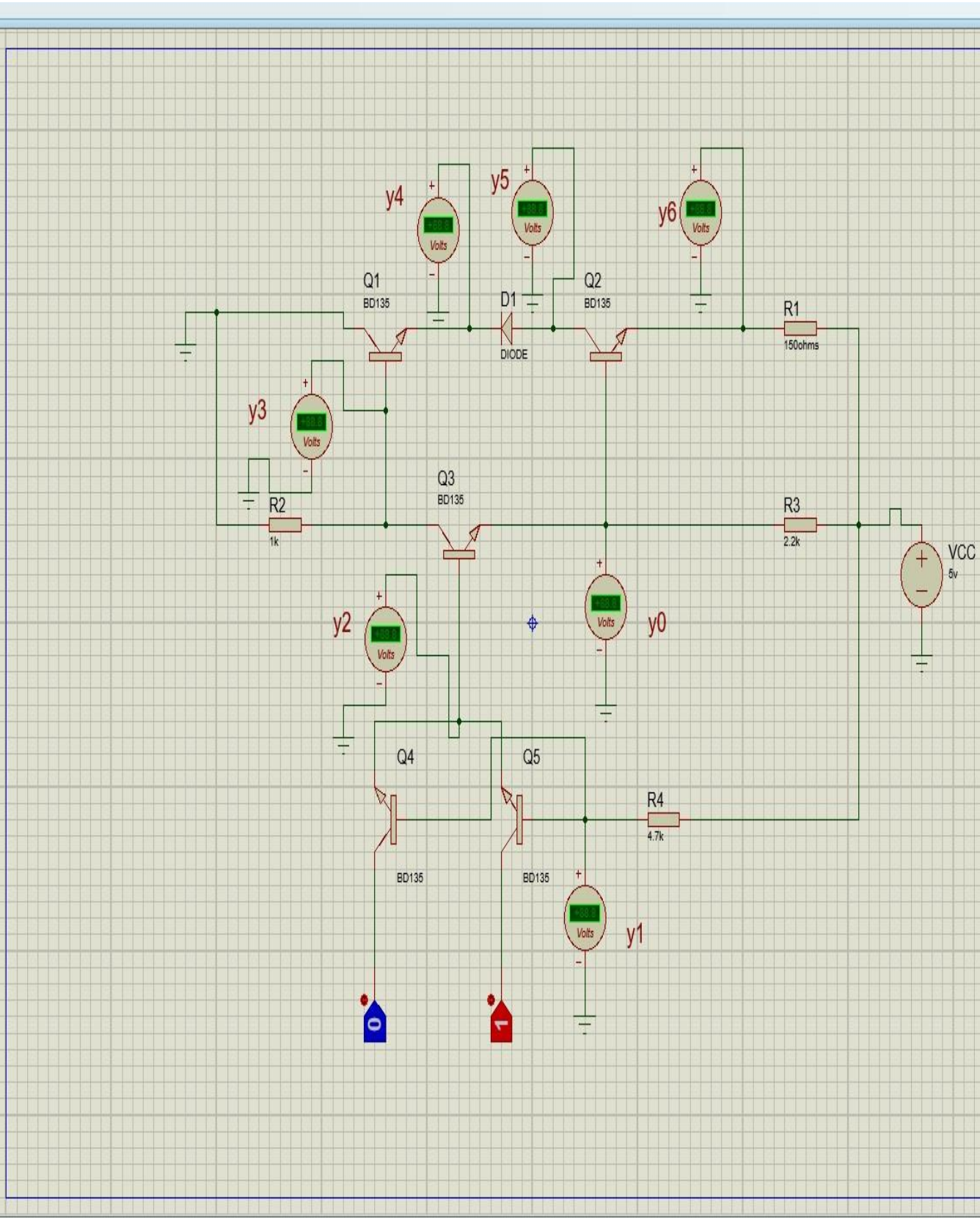

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A	B	Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6
0	0	5.00	0.53	0.01	0.00	4.31	4.71	5.00
0	1	5.00	0.55	0.03	0.00	4.31	4.71	5.00
1	0	5.00	0.55	0.03	0.00	4.31	4.71	5.00
1	1	0.61	1.66	1.16	0.58	0.01	0.37	5.00

ID: 180104006

A	B	Y0	Y1	Y2	Y3	Y4	Y5	Y6
0	0	5.00	0.53	0.01	0.00	4.31	4.71	5.00
0	1	5.00	0.55	0.03	0.00	4.31	4.71	5.00
1	0	5.00	0.55	0.03	0.00	4.31	4.71	5.00
1	1	0.61	1.66	1.16	0.58	0.01	0.37	5.00

ID: 180104007

A	B	Y0	Y1	Y2	Y3	Y4	Y5	Y6
0	0	5.00	0.52	0.00	0.00	4.33	4.72	5.00
0	1	0.54	0.54	0.02	0.00	4.33	4.72	5.00
1	0	0.54	0.54	0.02	0.00	4.33	4.72	5.00
1	1	1.88	1.88	1.27	0.64	0.01	0.40	5.00

The data Table of ID: 180104007 is considered for calculation.