Ahsanullah University of Science and Technology (AUST)

Department of Computer Science and Engineering

LAB REPORT

Course No. : CSE2210

Course Title: Digital Electronics and Pulse Techniques Lab

Experiment Number: 02

Name of the Experiment: Study of transistorized NOT gate.

Group Number: 02

Report Writer:

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Name of the experiment:

Study of a transistorized NOT gate.

Objective:

Studying transistorized NOT gate.

Circuit diagram:

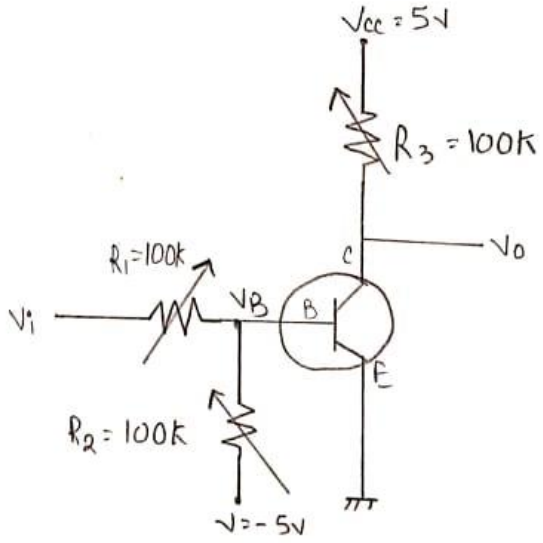

Fig: Transistorized NOT gate.

Questions

1. Which factor affect the switching speed of a transistor and how?

Answer:

Internal capacitance of the transistor affect the switching speed of a transistor. We know, $Q = CV$, so, essentially it depends on both the gate capacitance and the voltage. There is the significant capacitance between the collector and base. When turning off, the collector voltage rises (if it didn't there would be no need to turn the transistor off). This couples via the base-collector capacitance and tends to counter the turn-off or on voltage on the base, thereby making it harder to turn on or off. As the equation explains, if the total charge required (Product of both C and V) can be kept to a minimum from being an ON state to OFF state achieve a higher switching frequency. When transistor changes from saturation to cut off mode it doesn't happen immediately. It takes some time to discharge.

When it enters the cut-off mode it also takes some time to charge up.

2. What is the effect of R_1? Can it be very large?

Answer:

In the given circuit, R_1 is mainly used as a current limiter. The optimum value of this resistance such that it doesn't affect the output (characteristic of NOT gate) and the whole is between 35kΩ to 45kΩ. If it becomes very large, the circuit will loose it's NOT gate property. In the given circuit input $V_i = 5V$ and $V_o \approx 0V$ it is hold NOT gate properly.

If $R_1 = 40.9k\Omega$, $R_2 = 90.7k\Omega$ and $V = -5V$

using superposition,

$$V_B = \frac{40.9}{40.9+90.7} \times (-5V) + \frac{90.7}{40.9+90.7} \times 5V$$

$$= 1.892V$$

So, the transistor will be in saturation mode as it requires V_B to be atleast 0.8v.

As a result output will be $V_o \approx 0V$, holding NOT gate properly.

If $R_1 = 85\,k\Omega$ $R_2 = 90k\Omega$ and $V = -5$

using superposition,

$$V_B = \frac{85}{85+90.7} \times (-5V) + \frac{90.7}{85+90.7} \times 5V$$

$$= 0.162\,V$$

But in saturation mode V_B needs to be atlest 0.8V. So transistor will be in cut off mode with output $V_o = 5V$, so we get V(1) for V(1) as input. So NOT gate properly is not holding in this case.

So, R_1 cannot be very large.

3. Are there any effects of temperature on the circuit?

Answer:

The resistance of the resistors are dependent on the temperature. If the temperature increases then the resistance also increases.

There appears to be a linear relation between temperature and resistance of a resistor. Change in resistance will also cause the current in the junctions to change as well. We can see that the circuit is similar to fixed bias circuit. For fixed bias circuit, we know that the Q-point changes a values of V_{CE} changes with I_C (as resistance changes). So if there is a significant change in the temperature, the circuit might not give the output like before because the Q-point will change drastically.

Group :02
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1.

V_i	R_1	R_2	R_3	V_o	V_B
5V ✓	40.9	90.7	0.001	5.04V ✓	0.8
			0.059	4.46V ✓	0.78
			0.3	2.35V ✓	0.7
			0.86	2.01V ✓	0.61
			1.0	0.08V ✓	0.59
			2.4	0.04V ✓	0.55
			9.65	0.01V ✓	0.59
			14.22	0.01V ✓	0.58

2.

V_i	R_1	R_2	R_3	V_o	V_B
5V	40.6	0.02	2.4	5.04V ✓	0.85
		53.4		3.81V ✓	0.71
		70.5		2.69V ✓	0.69
		83.9		1.48V ✓	0.58
		90.7		0.04V ✓	0.55
		98.0		0.01V ✓	0.55

Asif 04/03/2020

3.

V_i	R_1	R_2	R_3	V_o	V_B
5V	8.6	90.7	2.7	0.00V	0.82
	18.28			0.00V	0.79
	40.9			0.04V	0.55
	55.6			1.23V	0.60
	59.2			2.98V	0.64
	63.6			3.46V	0.64
	87.5			5.04V	0.68

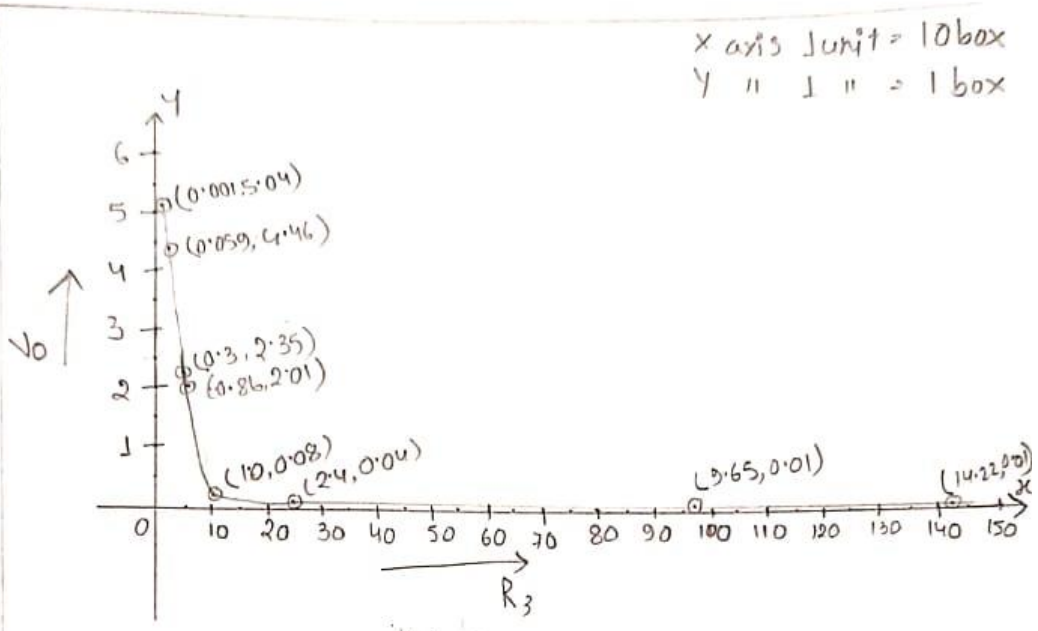

Fig: Graph For Table-1

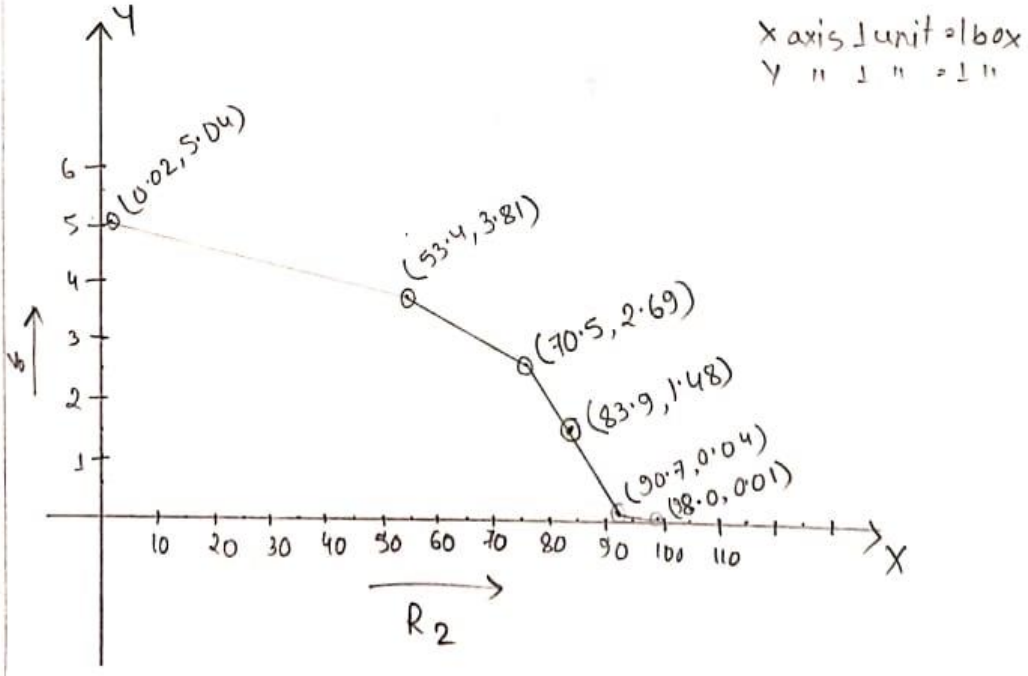

Fig: Graph For Table-2

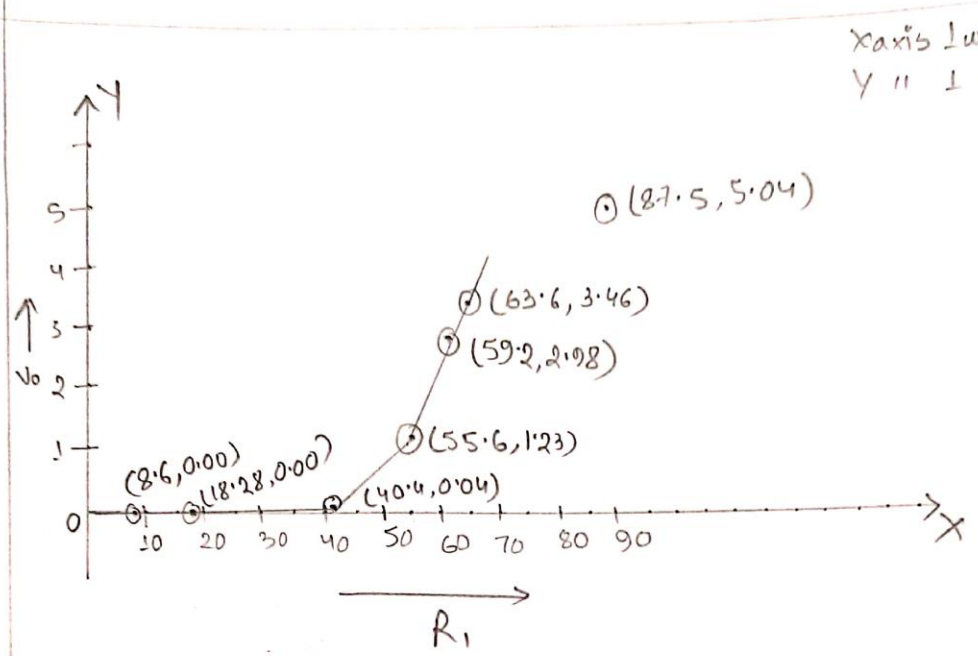

Fig: Graph For Table-3

Discuss the findings:

In this experiment we worked on a transistorized NOT gate. The resistance of the circuit were fixed in a range to study about the characteristics of NOT gate. Then we changed the value of these resistors and measured the upperbound and lowerbound of their value where the characteristics of NOT gate changed.

We measured all values but we faced some problem because of potentiometer. We plotted values for three different table and see the characteristics of NOT gate.