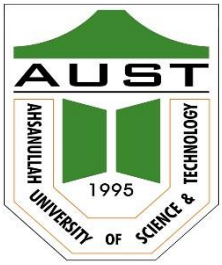

Ahsanullah University of Science and Technology (AUST)
Department of Computer Science and Engineering

LAB REPORT

Course No: CSE2210
Course Title: Digital Electronics and Pulse Techniques Lab

Experiment Number: 04

Name of the Experiment: Study of a RTL NOR gate.

Group Number: 02

Report Writer:

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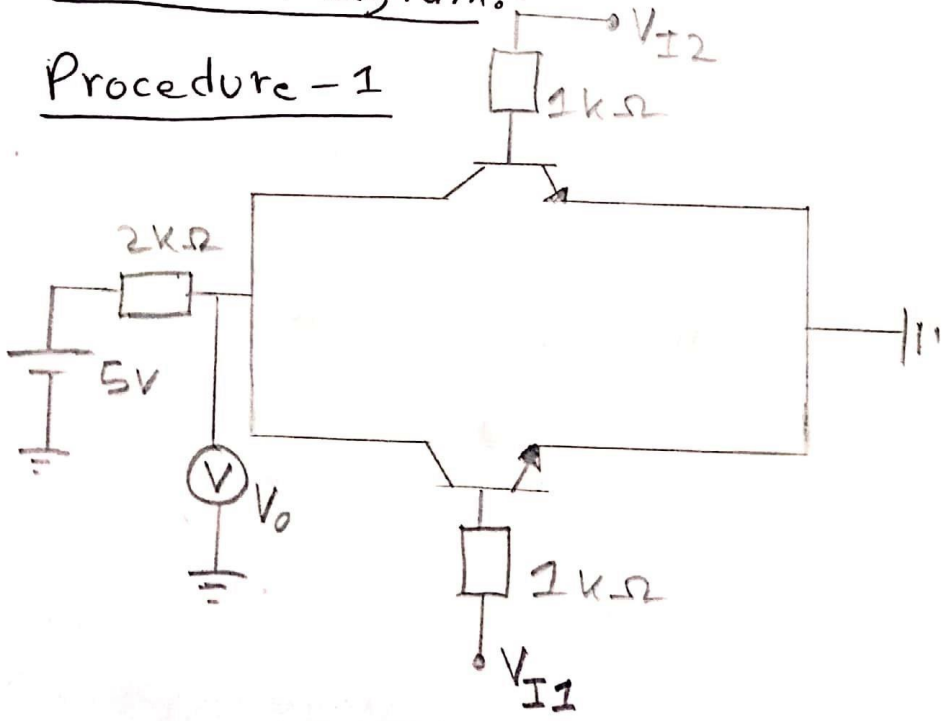
Name of the Experiment: Study of RTL NOR gate.

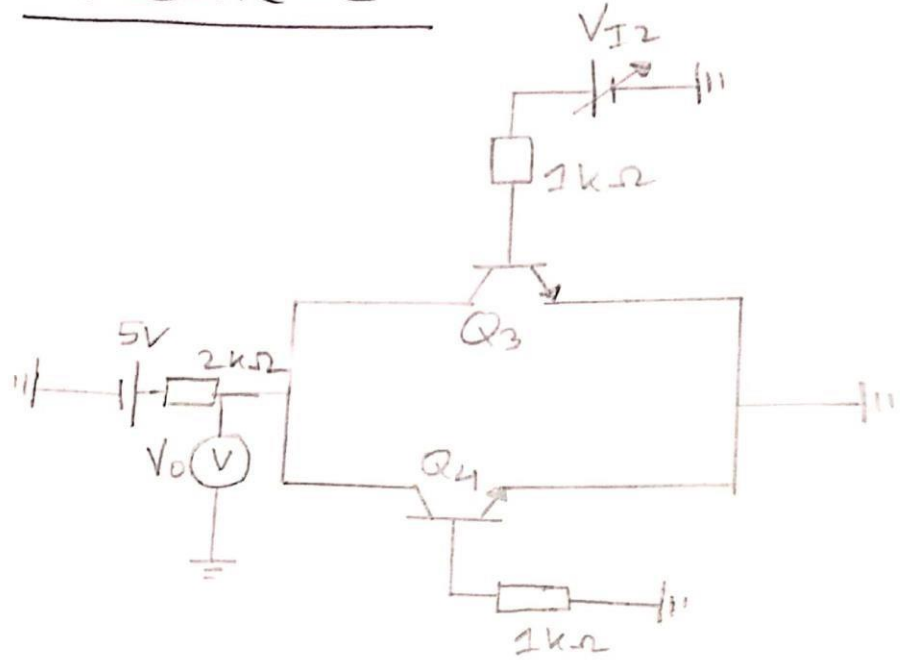
Objective: In this experiment, we are trying to construct a NOR gate using resistors and transistors. Knowing how to implement a NOR gate implies we can also construct other logic gates using this gate. We will also observe how the value of the output changes rapidly when our input is greater than a threshold value.

Circuit Diagram:

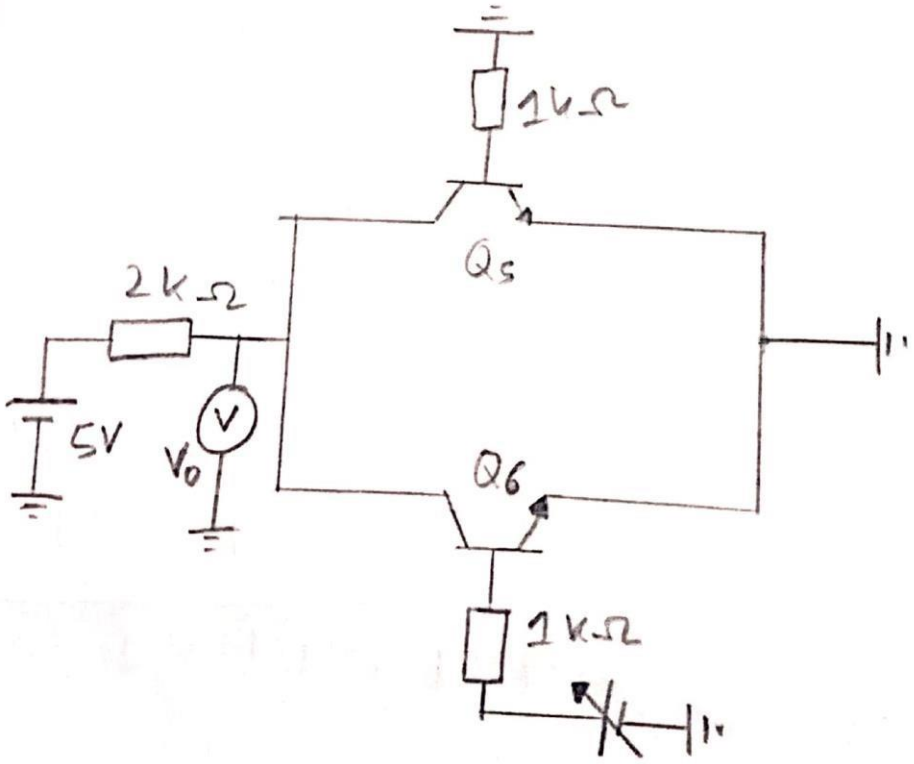
Procedure – 1



Procedure - 2



Procedure - 2



Answer to the following questions:

Q.1. Analyze the operation of RTL NOR gate with the experiment data.

Ans: As the name says it, we constructed a NOR gate using resistors and transistors (RTL). We performed an experiment and it matches with the output of a NOR gate. Which is, only all the transistors are in cut-off state, then the output would be 1 (high). For all other cases, which is, either of any of the transistors are in saturation, the output will be 0(low). From the circuit diagram, we can see that if all inputs are low voltage. None of the transistors will be turned on. So, there won't be any path for Vcc current to travel to ground. So, the Vcc will directly go to the output voltage and we will get high voltage If any of the inputs are high voltage, then the corresponding transistor will be in saturation and allow the current to pass to the ground. Hence, yielding a low voltage in the output.

V_{I1}	V_{I2}	V_O
0	0	+5.00
0	1	+0.02
1	0	+0.02
1	1	+0.02

Q2. What is the importance of studying the RTL gate?

Ans: NOR is a universal gate. Ability to construction a universal gate implies we can implement any logic using this gate. RTL is the earliest class of transistorized digital logic circuit used. RTL circuits were first constructed with discrete components, but in 1961 it became the first digital logic family to be produced as a monolithic integrated circuit. RTL integrated circuits were used in the Apollo Guidance computer, whose design was begun in 1961 and which first flew in 1966.

Resistor-Transistor Logic, or RTL, refers to the obsolete technology for designing and fabricating digital circuits that employ logic gates consisting of nothing but transistors

and resistors. RTL gates are now seldom used, if at all, in modern digital electronics design because it has several drawbacks, such as bulkiness, low speed, limited fan-out, and poor noise margin. A basic Understanding of what RTL is, however, would be helpful to any person who wishes to get familiarized with TTL, which for the past many years has become widely used in digital devices such as logic gates, latches, buffers, counters, and the like.

Resistors-transistor logic gates use Transistors to combine multiple input signals, which also amplify and invert the resulting combined signal. often an additional transistor is included to re-invert the output signal. This combination provides clean output signals and either inversion or non-inversion as needed.

Q.3 Draw the V_0 vs. V_{i1} and V_{i2} curves.

Graph of V_0 vs V_{i1}

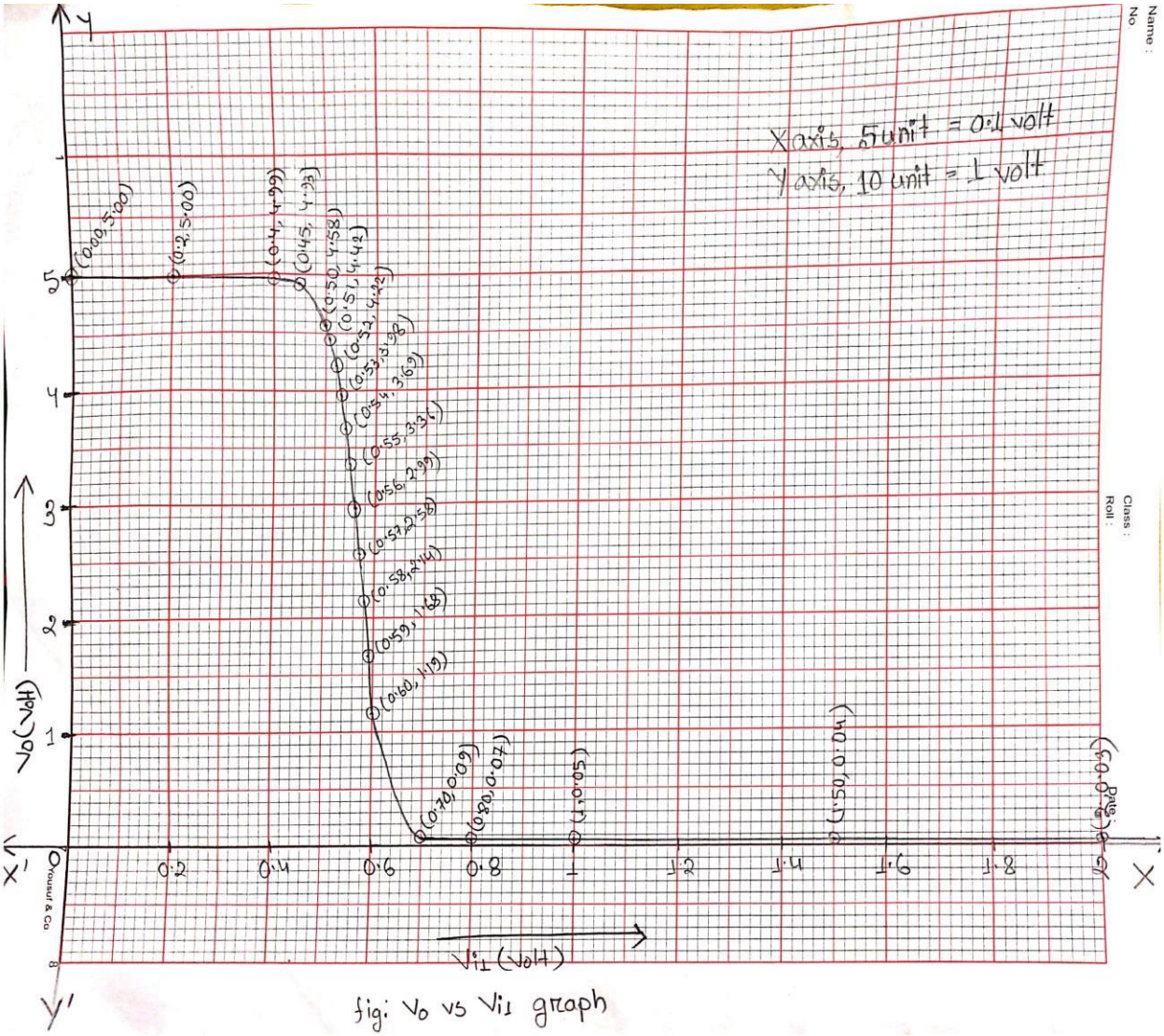


fig: V_0 vs V_{i1} graph

Graph of V_0 vs V_{i2}

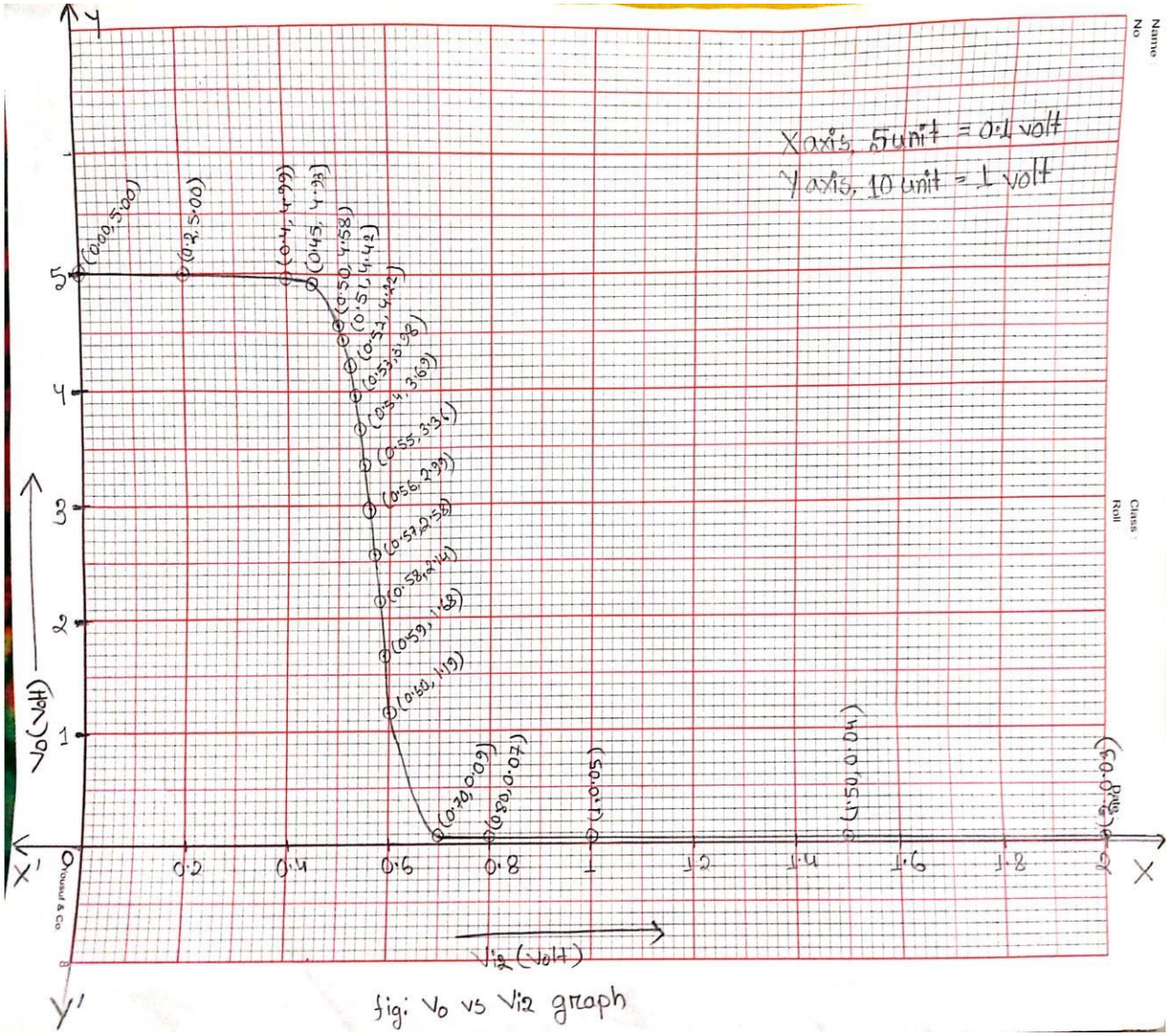


fig: V_0 vs V_{i2} graph

Discussion :

In this experiment, we constructed a NOR gate using resistors and transistors. This is one of the first transistorized digital circuit. Even though this is not widely used nowadays, but to understand the transistorized digital circuit well which are used nowadays, we need to understand the construction and how RTL circuits work. Because the ones that are used today is an improved version of RTL circuits. The experiment was performed in a proteus 8. So, this resulted in our result being very accurate. There were almost no error which conducting the experiment and measuring the values.

Experimental Data:

Procedure - 1

V_{I1}	V_{I2}	V_o
0	0	+5.00
0	1	+ 0.02
1	0	+ 0.02
1	1	+ 0.02

Procedure - 2

V_{I1}	V_{I2}	V_o
0	0.00	5.00
0	0.2	5.00
0	0.4	4.99
0	0.45	4.93
0	0.50	4.58
0	0.51	4.42
0	0.52	4.22
0	0.53	3.98
0	0.54	3.69
0	0.55	3.36
0	0.56	2.99
0	0.57	2.58
0	0.58	2.14
0	0.59	1.68
0	0.60	1.19
0	0.70	0.09
0	0.80	0.07
0	1.00	0.05
0	1.50	0.04
0	2.00	0.03
0	4.00	0.02
0	5.00	0.02

Procedure-3

V_{I1}	V_{I2}	V_O
0.00	0	5.00
0.2	0	5.00
0.4	0	4.99
0.45	0	4.93
0.50	0	4.58
0.51	0	4.42
0.52	0	4.22
0.53	0	3.98
0.54	0	3.69
0.55	0	3.36
0.56	0	2.99
0.57	0	2.58
0.58	0	2.14
0.59	0	1.68
0.60	0	1.19
0.70	0	0.09
0.80	0	0.07
1.00	0	0.05
1.50	0	0.04
2.00	0	0.03
4.00	0	0.02
5.00	0	0.02

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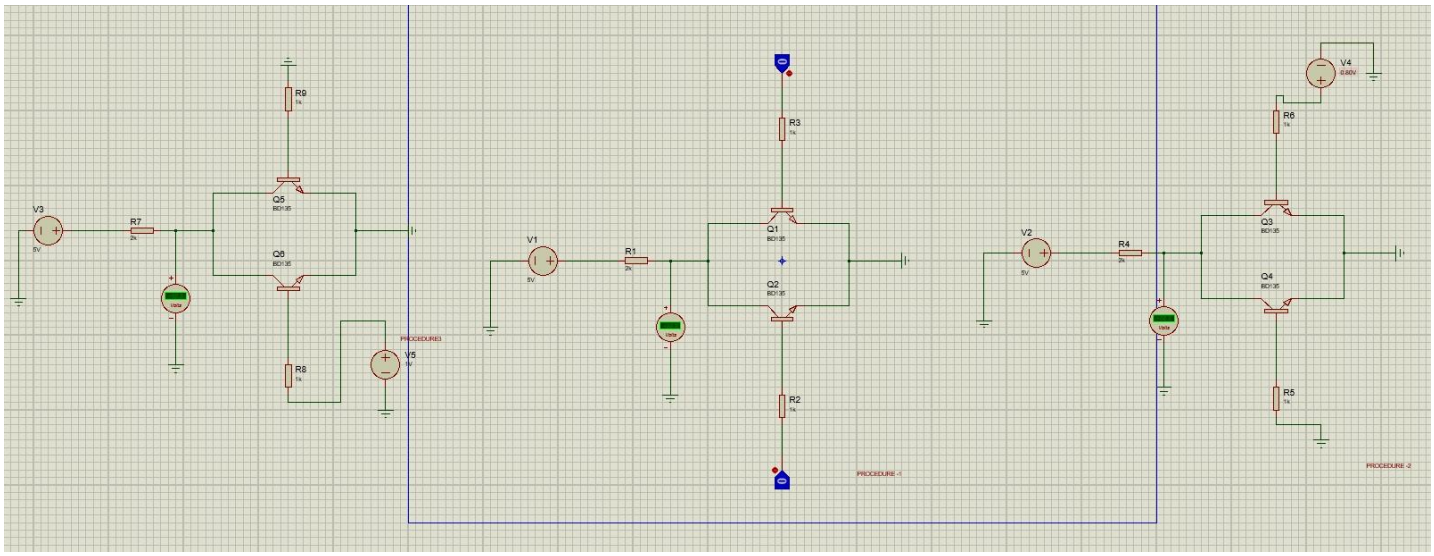

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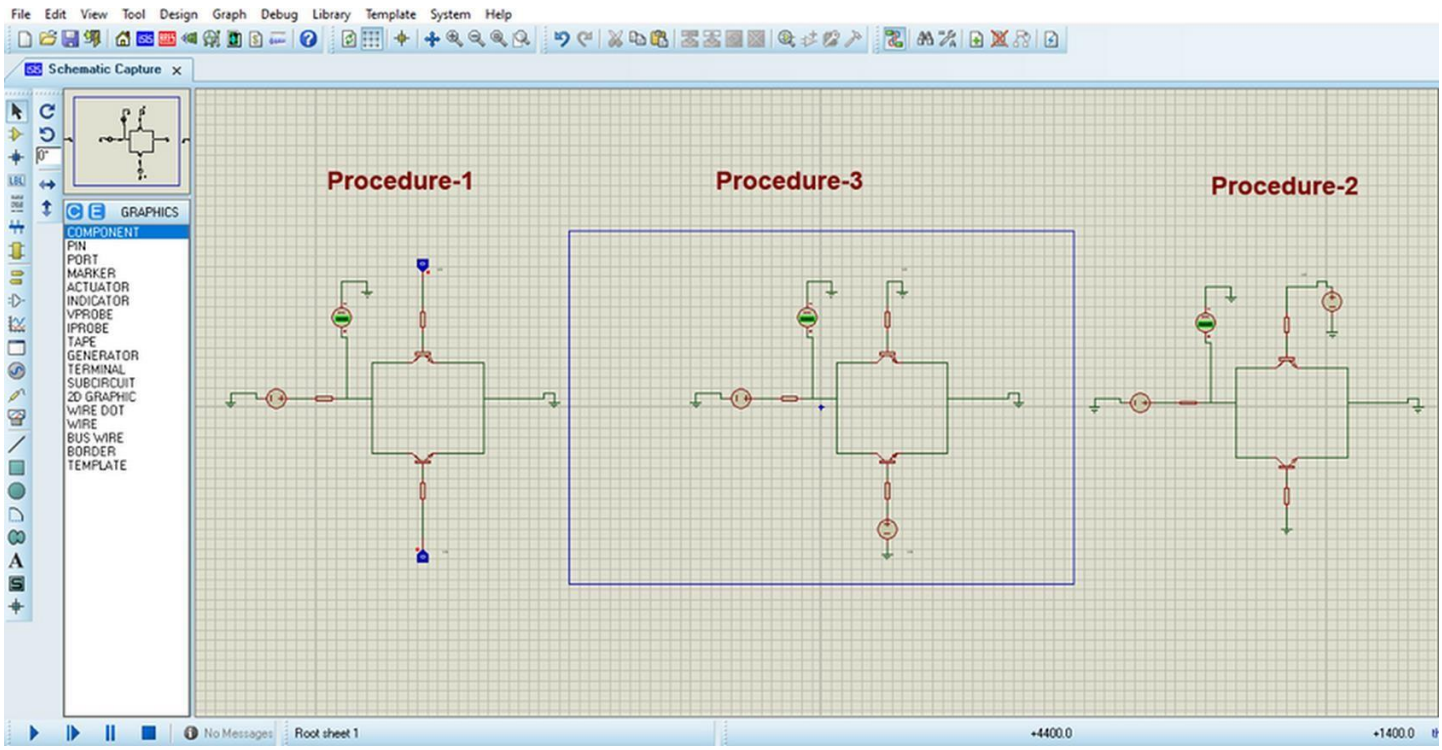

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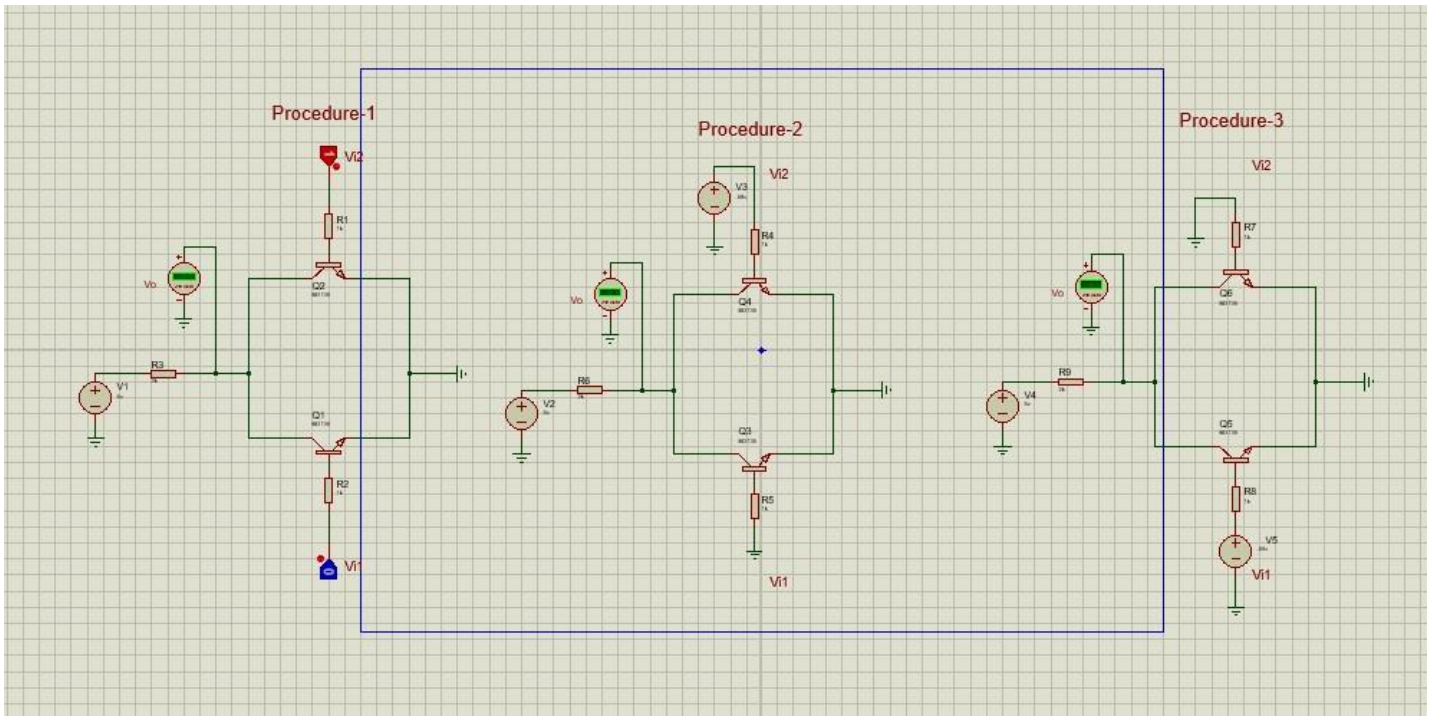

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Procedure-1

V_{I1}	V_{I2}	V_O
0	0	5.00
0	1	0.02
1	0	0.02
1	1	0.02

Procedure -2

V_{I1}	V_{I2}	V_O
0	0.00	5.00
0	0.2	5.00
0	0.4	4.99
0	0.45	4.93
0	0.50	4.58
0	0.51	4.42
0	0.52	4.22
0	0.53	3.98
0	0.54	3.69
0	0.55	3.36
0	0.56	2.99
0	0.57	2.58
0	0.58	2.14
0	0.59	1.68
0	0.60	1.19
0	0.70	0.09
0	0.80	0.07
0	1.00	0.05
0	1.50	0.04
0	2.00	0.03
0	4.00	0.02
0	5.00	0.02

Procedure - 3

V_{I1}	V_{I2}	V_O
0.00	0	5.00
0.2	0	5.00
0.4	0	4.99
0.45	0	4.93
0.50	0	4.58
0.51	0	4.42
0.52	0	4.22
0.53	0	3.98
0.54	0	3.69
0.55	0	3.36
0.56	0	2.99
0.57	0	2.58
0.58	0	2.14

0.59	0	1.68
0.60	0	1.19
0.70	0	0.09
0.80	0	0.07
1.00	0	0.05
1.50	0	0.04
2.00	0	0.03
4.00	0	0.02
5.00	0	0.02

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Procedure-1

Vi1	Vi2	V0
0	0	5.00
0	1	0.02
1	0	0.02
1	1	0.02

Procedure -2

Vi1	Vi2	V0
0	0.00	5.00
0	0.2	5.00
0	0.4	4.99
0	0.5	4.58
0	0.55	3.36
0	0.58	2.18
0	0.6	1.19
0	0.605	0.94
0	0.61	0.68
0	0.65	0.12
0	0.68	0.10
0	0.9	0.09
0	1.0	0.05
0	1.6	0.04
0	2.00	0.03

Procedure - 3

Vi1	Vi2	V0
0.00	0	5.00
0.2	0	5.00
0.4	0	4.99
0.5	0	4.58
0.55	0	3.36
0.58	0	2.18
0.6	0	1.19
0.605	0	0.94
0.61	0	0.68
0.65	0	0.12
0.68	0	0.10

0.9	0	0.09
1.0	0	0.05
1.6	0	0.04
2.00	0	0.03

ID: 18.01.04.007

Procedure-1

Vi1	Vi2	Vo
0	0	5.00
0	1	0.02
1	0	0.02
1	1	0.02

Procedure -2

Vi1	Vi2	Vo
0.00	0.2	5.00
0.00	0.4	4.99
0.00	0.48	4.78
0.00	0.49	4.69
0.00	0.5	4.58
0.00	0.55	3.36
0.00	0.58	2.14
0.00	0.6	1.19
0.00	0.62	0.21
0.00	0.65	0.12
0.00	0.7	0.09
0.00	0.8	0.07
0.00	1.01	0.05
0.00	1.5	0.04

Procedure - 3

Vi2	Vi1	Vo
0.00	0.2	5.00
0.00	0.4	4.99
0.00	0.5	4.58
0.00	0.55	3.36
0.00	0.50	1.68
0.00	0.58	2.14
0.00	0.6	1.19
0.00	0.62	0.21
0.00	0.65	0.12
0.00	0.7	0.09
0.00	0.8	0.07
0.00	1.01	0.05