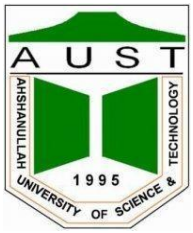

Ahsanullah University of Science & Technology

Department of Computer Science & Engineering

Course No : **CSE3310**
Course Title : **Digital System Design lab**
Assignment No : **02**

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Submitted By-
Section: A1
Group Number: A1_G1
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Id: 18.01.04.006

Introduction:

In this experiment, we implement 5-bit Booth Multiplier. Booth's multiplication algorithm is a multiplication algorithm that multiplies two signed binary numbers in two's complement notation. It is an effecient algorithm to perform to perform multiplication of two binary numbers which takes very less time. Instead of just doing addition to perform the multiplication. It perform some shifting operation along with the addition (addition with A ones) to calculate the result. We used a combination of adders, D Flip-flops, adder and basic gates. Here A is the multiplicand and M is the multiplier and both of them are 5 bits. So, our output is of 10 bits. The product of the calculation is added with some fixed value (A and S) which is set initially during input. Then using those additions and performing right shifts, the final result is calculated.

A = M(5bits) 0(6 bits)
S = -M (5 bits) 0 (6 bits)
P = 0 (5 bits) R (5 bits) 0 (1 bit)

Problem Statement:

Design a 5-bit Booth Multiplier.

Function Generation:

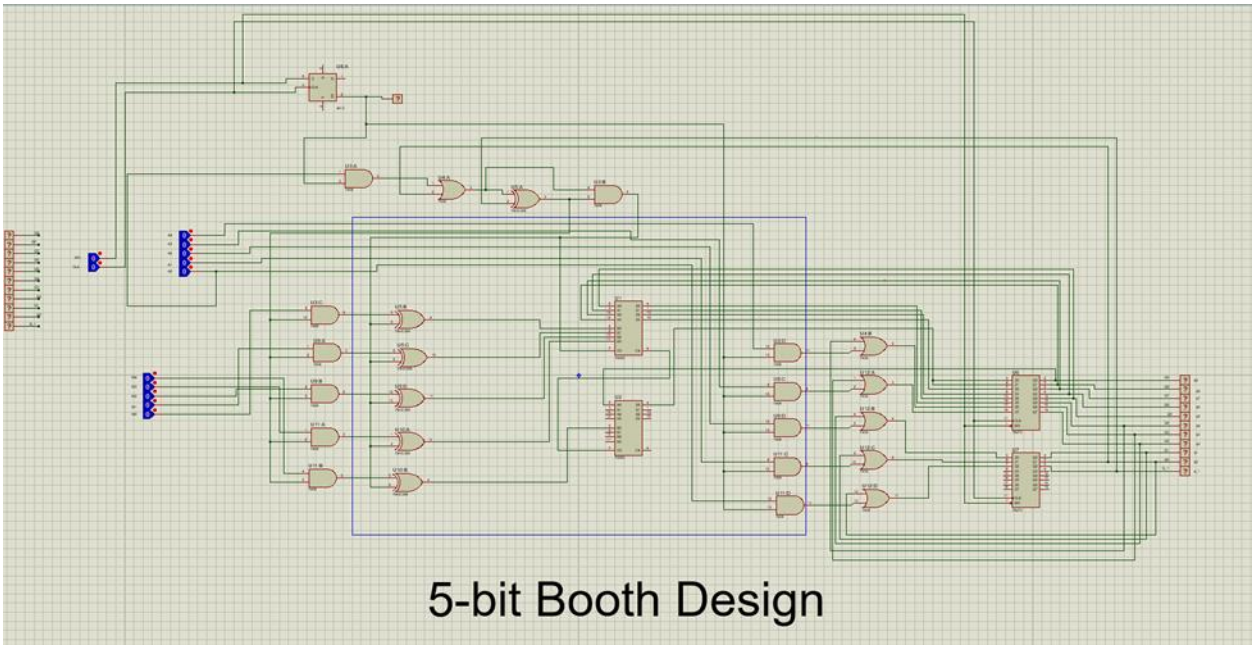
P_0	P_{-1}	Operation
0	0	Do nothing
0	1	P+A
1	0	P+S
1	1	Do nothing

Depending on the last 2 bits of the product term, the addition operation is performed accordingly as shown in the table.

Equipment and Budget:

Gate Name	IC	Amount	Price per IC (Taka)	Price (Taka)
AND	7408	3	30	90
XOR	4077	2	26	52
OR	7432	2	29	58
D flip-flop	74273	2	40	80
D flip-flop	4013	1	17	17
4bit full Adder	4008	2	40	80
			total price =	377 Taka

Simulations:



Result:

If M = 01110 and R = 11101 then

M	R	Clock pulse	P
01110	11101	CLK 1	11001011101
		CLK 2	00011101110
		CLK 3	11010110111
		CLK 4	11010110111
		CLK 5	11110101101

If M = 01100 and R = 00101 then

M	R	Clock Pulse	P
01100	00101	CLK 1	11010000101
		CLK 2	00011000010
		CLK 3	11011100001
		CLK 4	00011110000
		CLK 5	00001111000

If M = 01010 and R = 10110 then

M	R	Clock Pulse	P
01010	10110	CLK 1	00000010110
		CLK 2	11011001011
		CLK 3	11101100101
		CLK 4	00011110010
		CLK 5	11001111001

Conclusion:

In this experiment, we didn't use any shift register. Although it would've been an appropriate to use it here. But we worked around it and used D-register in way to make it work like a shift register. This circuit works for both positive and negative inputs. A combination of basic gates was used so that the final output can be generated with 5 clock pulse. Without this extra basic gates, it would take 6 clock pulse to show the final output. This circuit will show 10-bit output. Although we have shown 11 bits but LSB can be ignored. In comparison to trivial way of performing multiplication, by using addition only. This is a much more effective and quick method and requires very low number of addition when we are multiplying very large numbers.