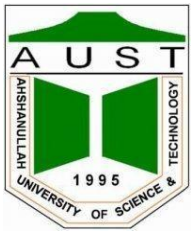


Ahsanullah University of Science & Technology

Department of Computer Science & Engineering

Course No : **CSE3310**
Course Title : **Digital System Design lab**
Assignment No : **03**

Date of Submission : **30.03.2021**

Submitted By-
Section: A1
Group Number: A1_G1
Id: 18.01.04.001
Id: 18.01.04.002
Id: 18.01.04.005
Id: 18.01.04.006

Introduction:

We implemented SAP-1 which is a bus organized computer. It is a key basic model of microprocessor which contains the basic registers for a funcational microprocessor. SAP-1 contains all the five instructions in its instruction set. The set is given through a hex file. It's primary purpose is to show how microprocessor interacts with memory and other parts of the system.

Problem Statement: Implement a SAP-1

Function Generation:

Program in Assembly		Machine Code
Address	Contents	in Hex
0H	LDA 5H	05
1H	ADD 6H	16
2H	SUB 7H	27
3H	OUT	EF
4H	HLT	FF
5H	68H	68
6H	20H	20
7H	18H	18
8H	FFH	FF
AH	FFH	FF
BH	FFH	FF
CH	FFH	FF
DH	FFH	FF
EH	FFH	FF
FH	FFH	FF

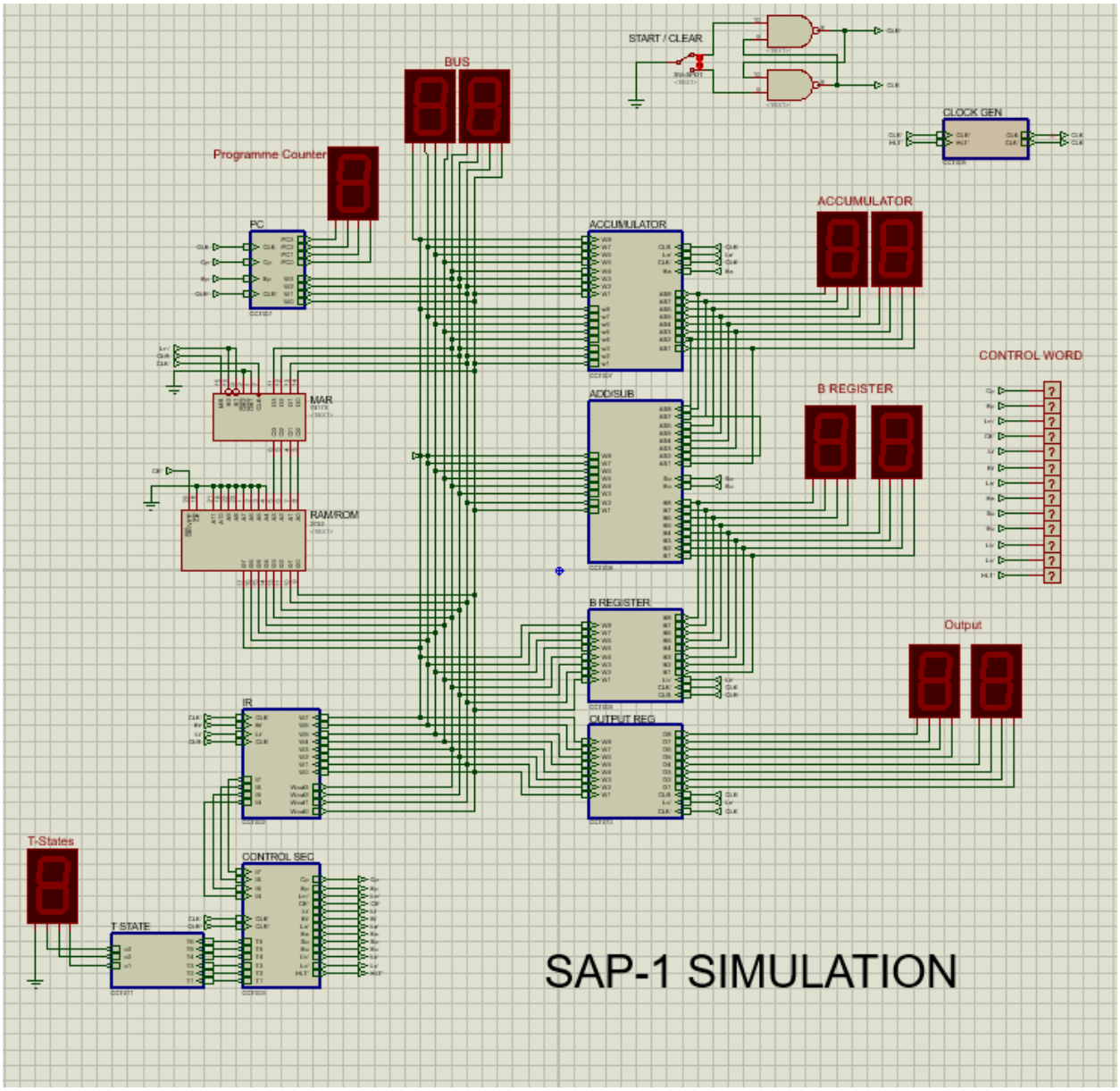
This table shows the micro-instructions and macro-instructions needed for the SAP-1. Fetch and Execute Cycle of SAP-1

Macro Inst.	T state	Micro Operation	Active	CON
All Instructions	T_1	MAR ← PC	L'_M, E_P	5E3H
	T_2	PC ← PC+1	C_P	BE3H
	T_3	IR ← RAM[MAR]	C_E', L_I'	263H
LDA	T_4	MAR ← IR(3...0)	L'_M, E_I'	1A3H
	T_5	ACC ← RAM[MAR]	C_E', L_A'	2C3H
	T_6	None	None	3E3H
ADD	T_4	MAR ← IR(3...0)	L'_M, E_I'	1A3H
	T_5	B ← RAM[MAR]	C_E', L_B'	2E1H
	T_6	ACC ← ACC+B	L_A', E_U	3C7H
SUB	T_4	MAR ← IR(3...0)	L'_M, E_I'	1A3H
	T_5	B ← RAM[MAR]	C_E', L_B'	2E1H
	T_6	ACC ← ACC-B	L_A', S_U, E_U	3CFH
OUT	T_4	OUT ← ACC	E_A, L_O'	3F2H
	T_5	None	None	3E3H
	T_6	None	None	3E3H
HLT	T_4	None	HLT'	263H

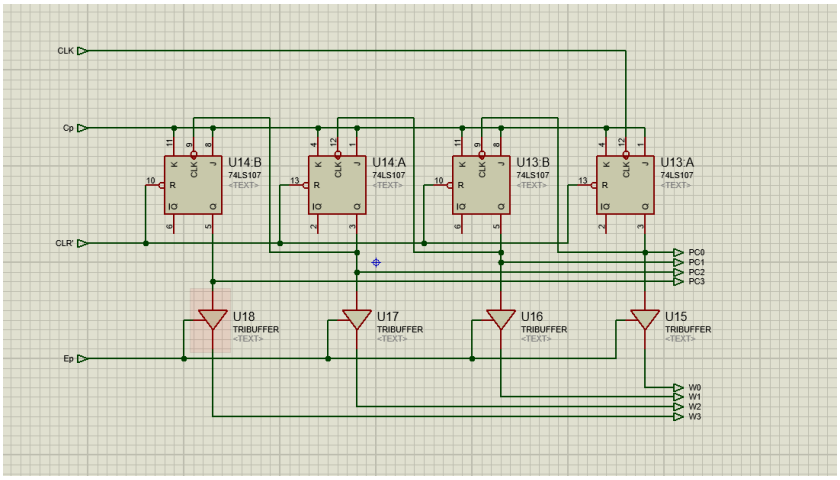
Equipment and Budget:

IC	Amount	Price per IC (Taka)	Price (Taka)
74173	1	44	44
74LS107	11	71	781
74LS173	8	127	1016
74LS00	9	15	135
74LS04	18	15	216
74LS21	5	25	125
74HC4075	3	55	165
74LS83	2	40	80
74LS86	8	81	648
2732	1	74	74
BUFFER_8	2	43	86
TRI BUFFER	4	25	100
		Total Price =	2,948 Taka

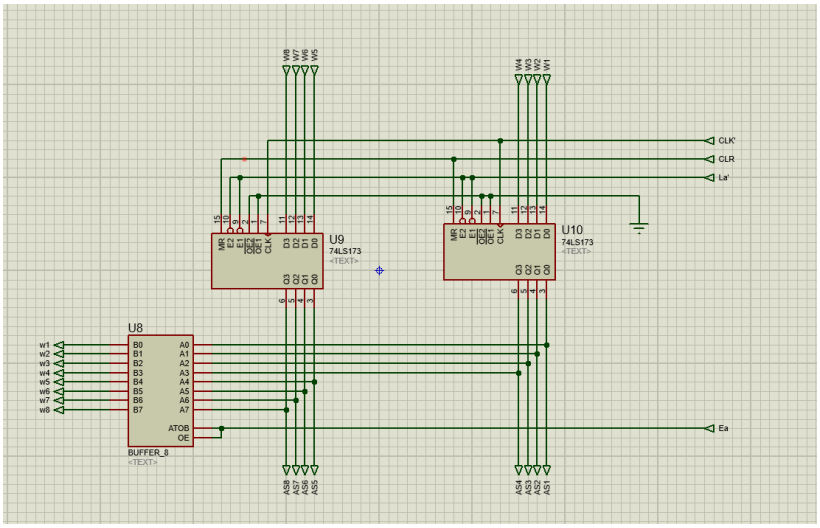
Simulations:



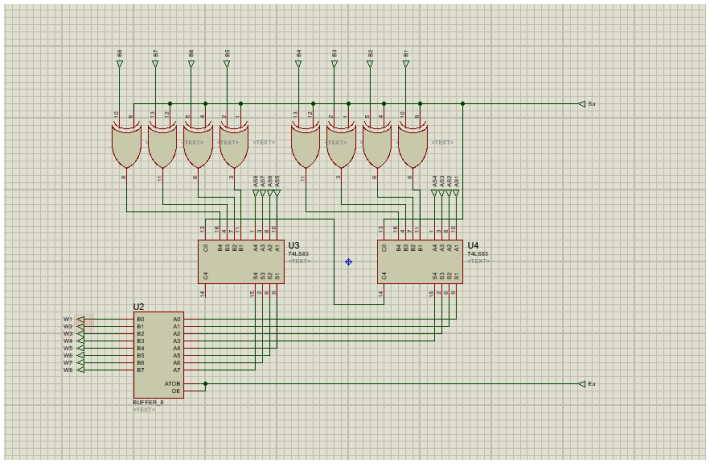
Program Counter



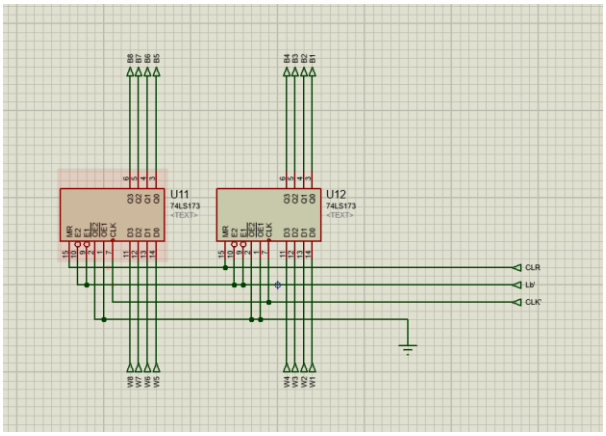
Accumulator



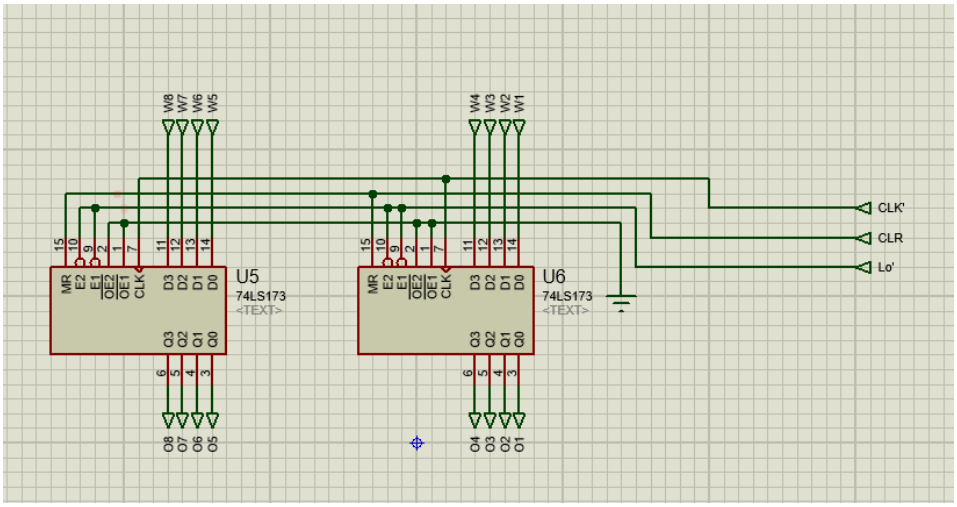
Adder/Subtractor



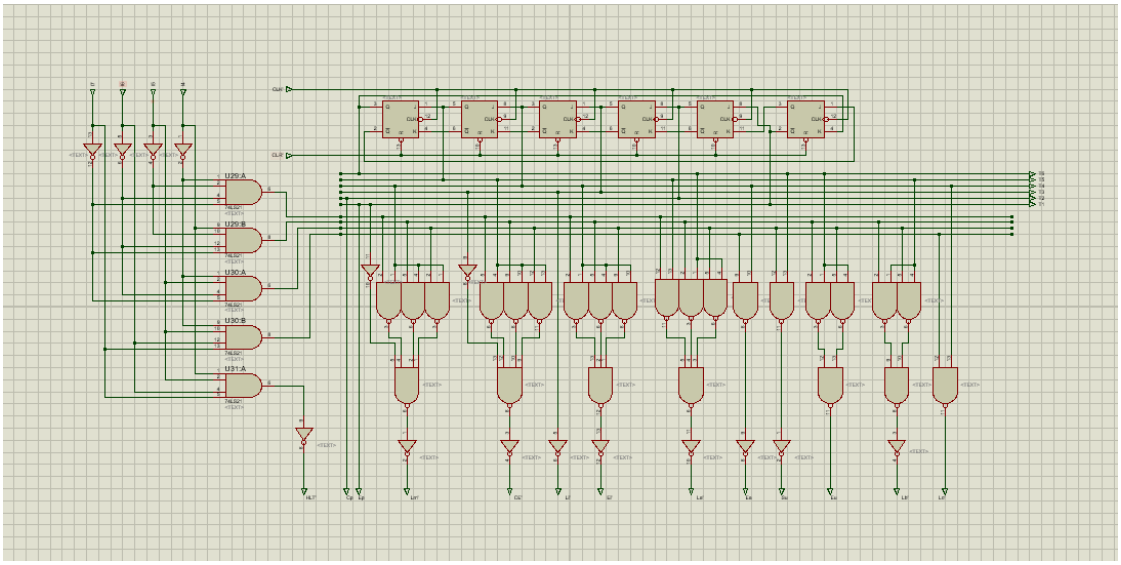
B REGISTER



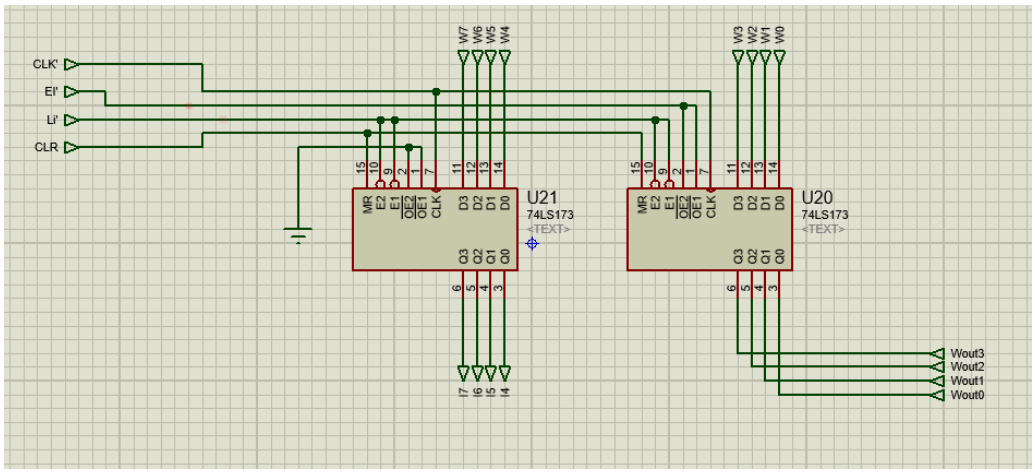
Output Register



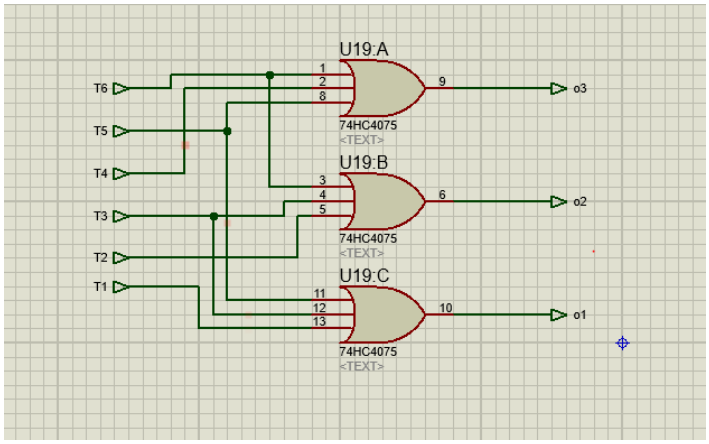
Control Sequencer



Instruction Register

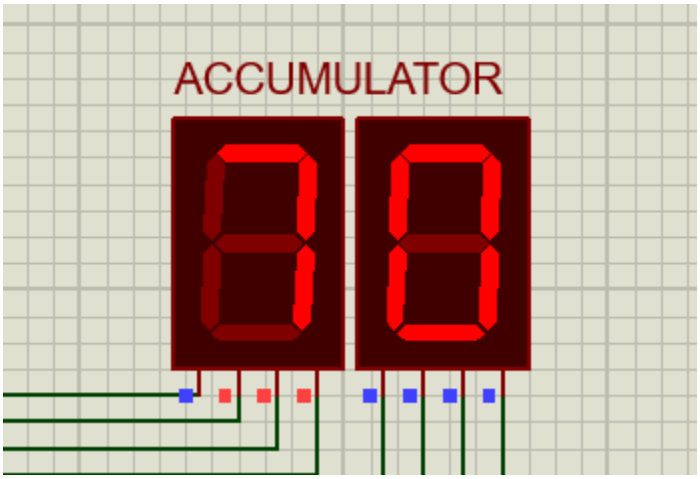


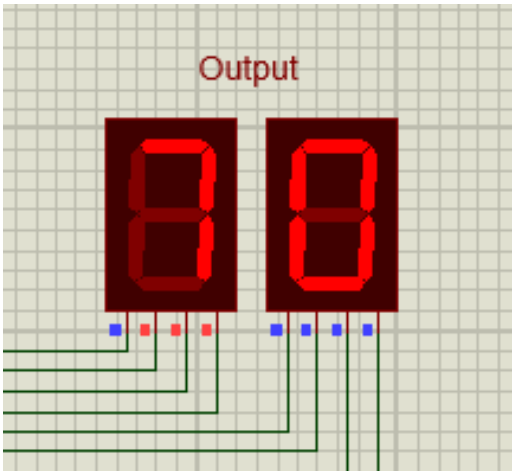
T State Display



Result:

Contents	Accumulator	OUTPUT
LDA 5H	68H	00H
ADD 6H	88H	00H
SUB 7H	70H	00H
OUT	70H	70H
HLT	70H	70H





Conclusion:

No error occurred during the implementation. But there are some advantages and disadvantages in SAP-1 circuit. The key advantages of SAP is flexibility and simplicity. It have strong workflow capabilites. It can handle different types of complex transactions – data entered one time, one place, at the source. There are some disadvantages of SAP is expensive, lengthy implementation time and only five instructions can be stored in memory.