Ahsanullah University of Science & Technology

Department of Computer Science & Engineering

Course No : CSE3310
Course Title : Digital System Design lab
Assignment No : 01

Date of Performance : 30.12.2020

Date of Submission : 13.01.2021

Submitted By-
Section: A1
Group Number: A1_G1
Id: 18.01.04.001
Id: 18.01.04.002
Id: 18.01.04.005
Id: 18.01.04.006

Introduction:

In this experiment, we designed a 4bit Arithmetic Logic Unit. First of all from the given function table we derived an equation of three input funcations and simplified it. Then we implemented this funcations in Proteus.
We used a combination of basic gates and a 4 bit full adder to create out ALU. Depending on the selector (S_0) bit, our ALU will perform the logical ($S_0=0$) or arithmetic ($S_0=1$) operation accordingly and will show it 4 bit output for logical operation and 5 bit output for arithmetic operation.

Problem Statement:

S_2	S_1	S_0	Output	Function
1	0	1	A_i-1	Decrement A
0	1	1	A_i+B_i	Add
1	1	1	A_i-B_i	Subtract
0	0	1	A_i	Transfer A
1	X	0	$A_i \mid B_i$	OR
0	X	0	$\overline{A_i}$	Complement A

Function Generation:

S_2	S_1	S_0	z	X	Y	Output	Function
1	0	1	0	A_i	1111	$A_i - 1$	Decreement A
0	1	1	0	A_i	B_i	$A_i + B_i$	Add
1	1	1	1	A_i	$\overline{B_i}$	$A_i - B_i$	Subtract
0	0	1	0	A_i	0	A_i	Transfer A
1	X	0	0	$A_i \mid B_i$	0	$A_i \mid B_i$	OR
0	X	0	0	$\overline{A_i}$	0	$\overline{A_i}$	Complement A

K-map

$S_2 \backslash S_1S_0$	0 $\bar{S_1}\bar{S_0}$	1 $\bar{S_1}S_0$	3 S_1S_0	2 $S_1\bar{S_0}$
0 $\bar{S_2}$	0	0	0	0
1 S_2	0	0	$\boxed{1}$	0

$\therefore Z = S_2 S_1 S_0$

$S_2 \backslash S_1S_0$	0 $\bar{S_1}\bar{S_0}$	1 $\bar{S_1}S_0$	3 S_1S_0	2 $S_1\bar{S_0}$
0 $\bar{S_2}$	$\overline{A_i}$	A_i	A_i	$\overline{A_i}$
1 S_2	$A_i \mid B_i$	A_i	A_i	$A_i \mid b_i$

$$\therefore X = S_0 A_i + \bar{S_2}\bar{S_0}\overline{A_i} + S_2\bar{S_0}(A_i \mid B_i)$$

$$= S_0 A_i + \bar{S_2}\bar{S_0}\overline{A_i} + S_2\bar{S_0}(A_i + B_i)$$

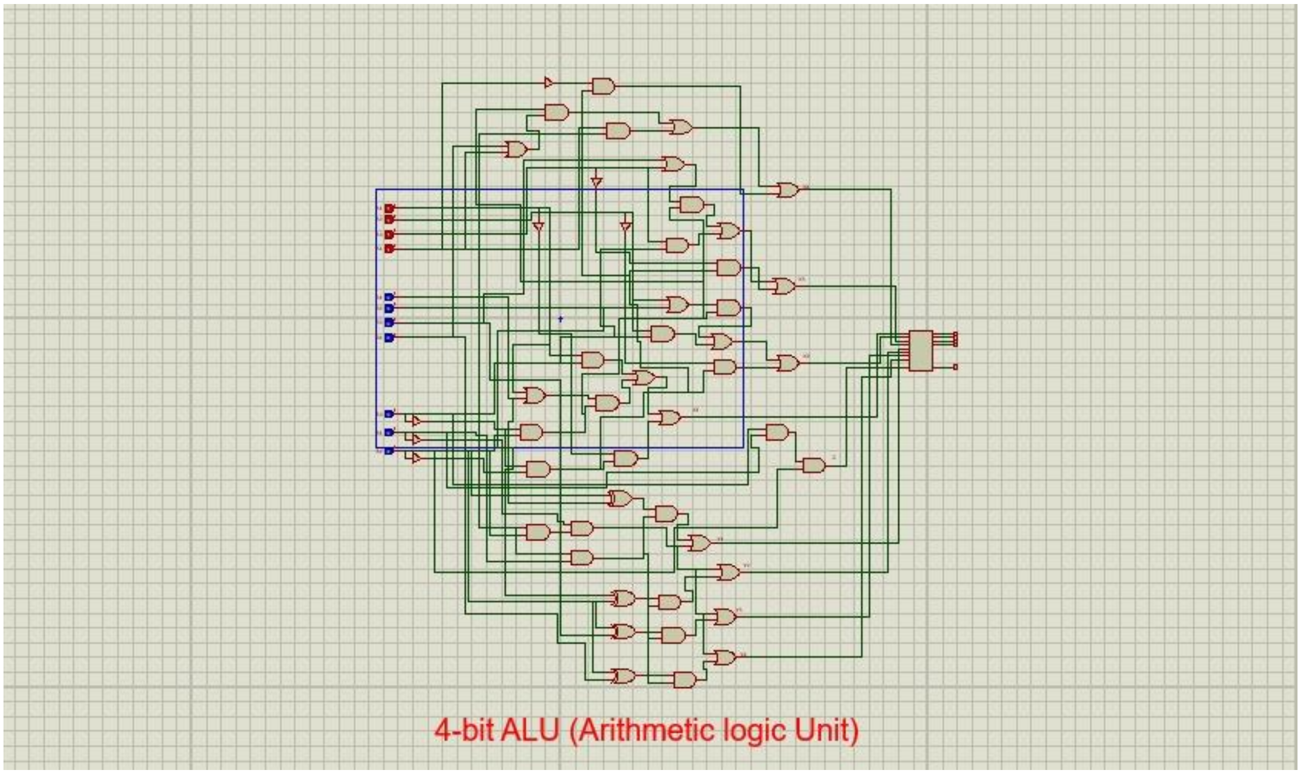
$S_2 \backslash S_1S_0$		0 $\bar{S_1}\bar{S_0}$	1 $\bar{S_1}S_0$	3 S_1S_0	2 $S_1\bar{S_0}$
0	$\bar{S_2}$	0	0	$\boxed{Bi}$	0
1	S_2	0	$\boxed{1}$	$\boxed{\bar{Bi}}$	0

$$\therefore Y = S_2\bar{S_1}S_0 + \bar{S_2}S_1S_0bi + S_2S_1S_0\bar{bi}$$
$$= S_2\bar{S_1}S_0 + S_1S_0(\bar{S_2}Bi + S_2\bar{Bi})$$
$$= S_2\bar{S_1}S_0 + S_1S_0(S_2 \oplus Bi)$$

Equipement and Budget:

Gate Name	IC	Amount	Price per IC (Taka)	Price (Taka)
NOT	7404	2	25	50
AND	7408	6	30	180
OR	7432	4	29	116
XOR	7486	1	26	26
4-bit Full Addor	4008	1	40	40
Total Cost = 412				

Simulations:



4-bit ALU (Arithmetic logic Unit)

Result:

For Decrement A operation

Input											Output				
S_2	S_1	S_0	A_4	A_3	A_2	A_1	B_4	B_3	B_2	B_1	Cout	F_3	F_2	F_1	F_0
1	0	1	1	0	0	0	1	1	1	1	1	0	1	1	1
			1	0	0	1					1	1	0	0	0
			1	1	1	0					1	1	1	0	1

For Addition Operation

Input											Output				
S_2	S_1	S_0	A_4	A_3	A_2	A_1	B_4	B_3	B_2	B_1	Cout	F_3	F_2	F_1	F_0
0	1	1	0	0	1	1	1	0	0	0	0	1	0	1	1
			1	1	0	0	1	1	0	1	1	1	0	0	1
			1	1	1	0	1	0	0	1	1	0	1	1	1

For Subtraction Operation

Input											Output				
S_2	S_1	S_0	A_4	A_3	A_2	A_1	B_4	B_3	B_2	B_1	Cout	F_3	F_2	F_1	F_0
1	1	1	1	0	0	0	0	1	1	1	1	0	0	0	1
			1	0	0	1	0	1	0	0	1	0	1	0	1
			1	1	1	0	0	0	1	1	1	1	0	1	1

For transfer A Operation

Input											Output				
S2	S1	S0	A4	A3	A2	A1	B4	B3	B2	B1	Cout	F3	F2	F1	F0
0	0	1	1	0	0	0	0	0	0	0	0	1	0	0	0
			0	0	1	1					0	0	0	1	1
			1	1	1	1					0	1	1	1	1

For OR Operation

Input											Output				
S2	S1	S0	A4	A3	A2	A1	B4	B3	B2	B1	Cout	F3	F2	F1	F0
1	X	0	0	1	1	1	0	0	1	0	0	0	1	1	1
			1	0	0	1	0	1	0	1	0	1	1	0	1
			1	1	1	1	0	0	1	0	0	1	1	1	1

For NOT Operation

Input											Output				
S2	S1	S0	A4	A3	A2	A1	B4	B3	B2	B1	Cout	F3	F2	F1	F0
0	X	0	0	1	1	1	0	0	0	0	0	1	0	0	0
			1	1	1	1					0	0	0	0	0
			1	0	0	1					0	0	1	1	0

Conclusion:

There were some issues when we implemented the circuit for the first time. At our first attempt when we derived the equation of the inputs, we simplified those input equations and minimised the equation and hence also minimised the use of ICS, making it easier to implement. However, our ALU was showing incorrect results for logical operations but was working correctly for arithmetic operations.

We implemented the circuit again using the direct equations we got from the table without simplfying it and this time the functions were working correctly. This circuit was working correctly this time but when we are going to implement this practically, there might be an issure because we have used lots of ICs and circuit becomes more prone to error.