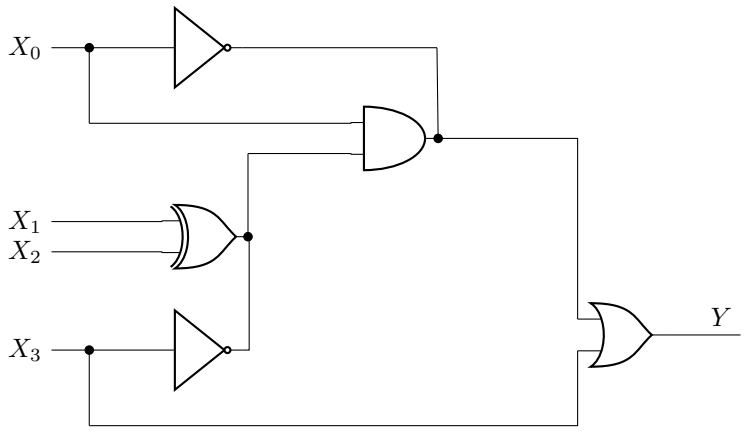
GATE QUESTION

February 9, 2024

1. The logic gates shown in the digital circuit below use strong pull-down nMOS transistors for LOW logic level at the outputs. When the pull-downs are off, high -value resistors set the output logic levels to HIGH (i.e. the pull-ups are weak). Note that some nodes are intentionally shorted to implement "wierd logic". Such shorted nodes will be HIGH only if the outputs of all the gates whose outputs are shorted are HIGH.

(GATE-EC 2018, 47)



The number of distinct values of $X_3X_2X_1X_0$ (out of the 16 possible values) that give Y=1 is ——.