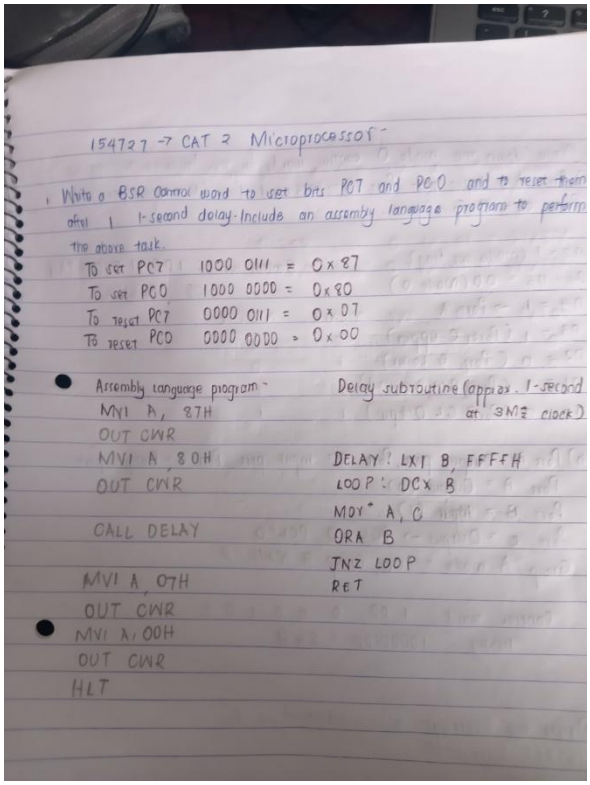


154727 → CAT 2 Microprocessor

1. Write a BSR control word to set bits PC7 and PC0 and to reset them after 1 second delay. Include an assembly language program to perform the above task.

To set PC7 1000 0111 = 0x87
To set PC0 1000 0000 = 0x80
To reset PC7 0000 0111 = 0x07
To reset PC0 0000 0000 = 0x00

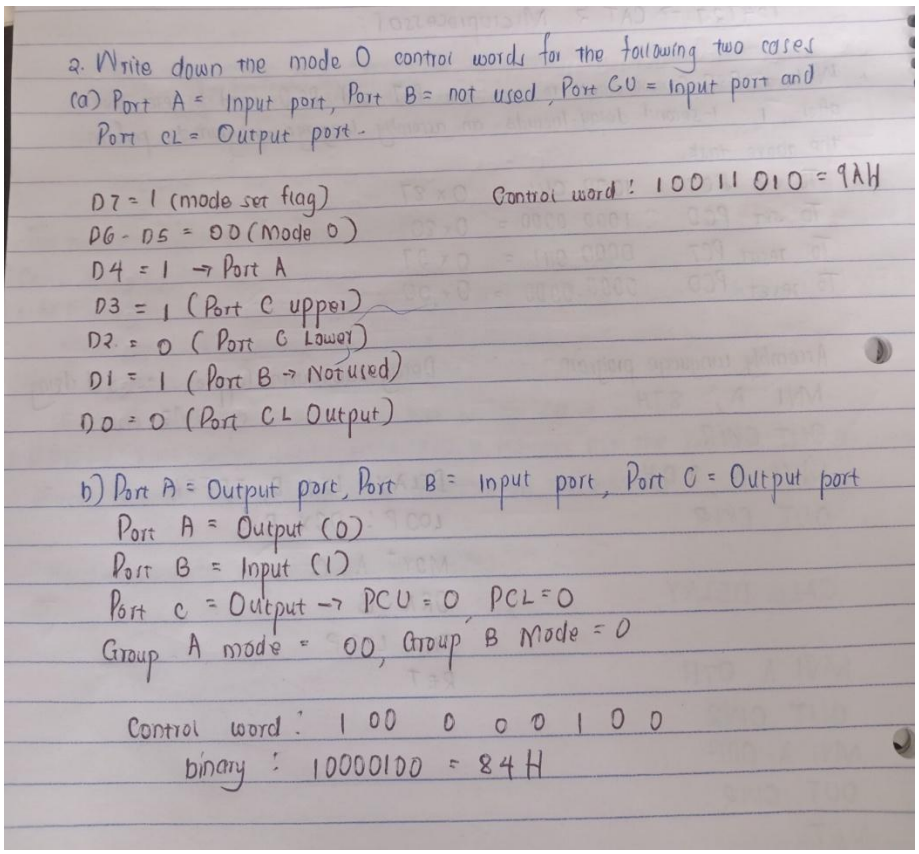
Assembly language program:

```
MVI A, 87H
OUT CWR
MVI A, 80H
OUT CWR
CALL DELAY
MVI A, 07H
OUT CWR
MVI A, 00H
OUT CWR
HLT
```

Delay subroutine (approx. 1-second at 3MHz clock)

```
DELAY: LXI B, FFFFH
LOOP: DCX B
MOV A, C
ORA B
JNZ LOOP
RET
```

Question 1



2. Write down the mode 0 control words for the following two cases

(a) Port A = Input port, Port B = not used, Port CU = Input port and Port CL = Output port.

D7 = 1 (mode set flag)
D6 - D5 = 00 (Mode 0)
D4 = 1 → Port A
D3 = 1 (Port C upper)
D2 = 0 (Port C Lower)
D1 = 1 (Port B → Not used)
D0 = 0 (Port CL Output)

Control word: 10011010 = 9AH

(b) Port A = Output port, Port B = Input port, Port C = Output port

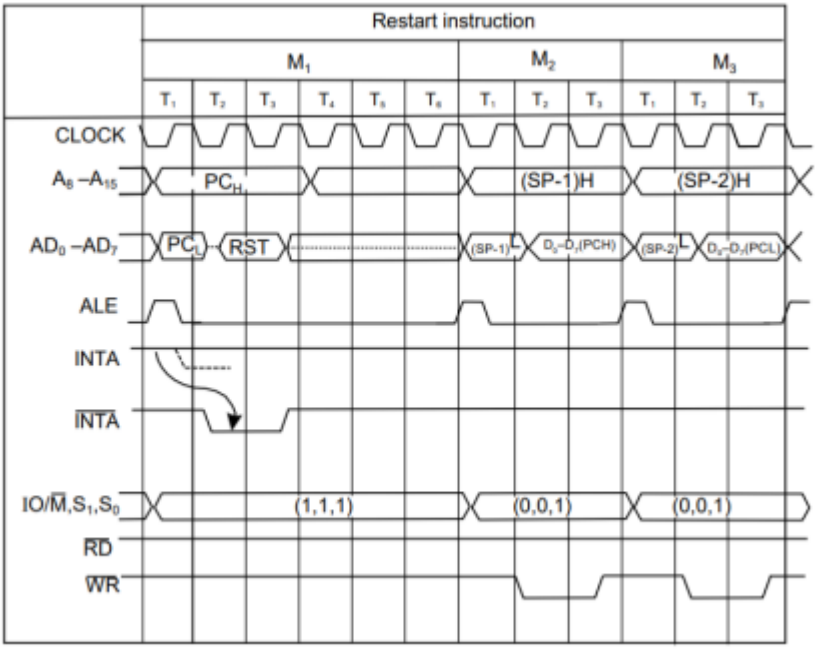
Port A = Output (0)
Port B = Input (1)
Port C = Output → PCU = 0 PCL = 0
Group A mode = 00, Group B Mode = 0

Control word: 1 00 0 0 0 1 0 0
binary: 10000100 = 84H

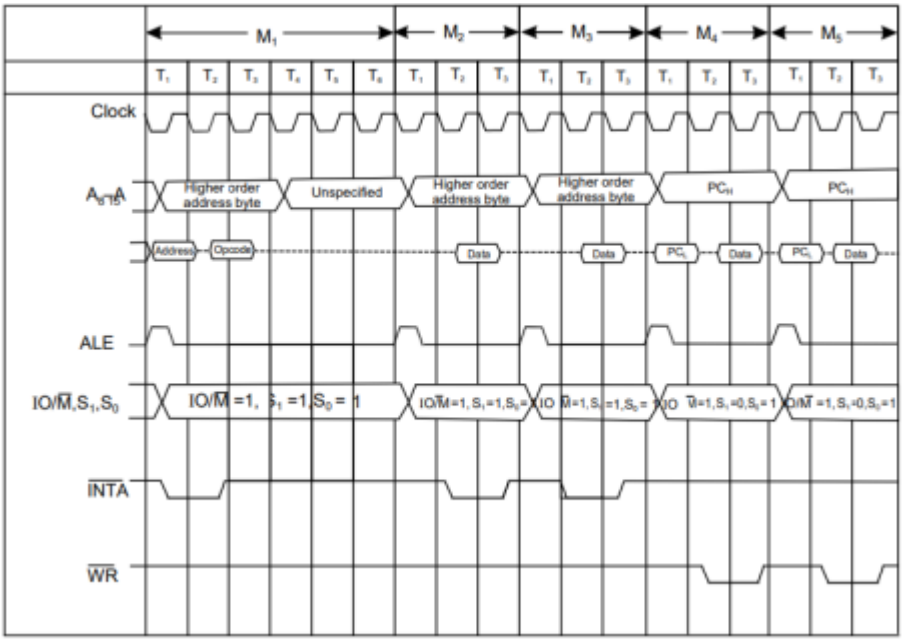
Question 2

3. Draw the Interrupt Acknowledge cycles for

(a) RST instruc on



(b) CALL instruc o



Question Number 4

5. Show how the MEMR and MEMW are derived from IO/M, RD and WR signals of PD 8085

MEMR = IO/M = 0 and RD = 0
MEMW = IO/M = 0 and WR = 0

IO/M	RD	WR	MEMR	MEMW
0	1	0	0	1
0	0	1	1	0
10	1	0	1	1
1	0	1	1	1

Question 5. Design a memory having size 16k × 8 from 4k × 4 memory modules