EGERTON UNIVERSITY

UNIVERSITY EXAMINATIONS

REGULAR, NJORO CAMPUS

FIRST SEMESTER, 2017/2018 ACADEMIC YEAR

SECOND YEAR EXAMINATION FOR THE DEGREE OF BACHELOR OF SCIENCE IN

COMPUTER SCIENCE

COMP 222 - ASSEMBLY LANGUAGE PROGRAMMING

STREAM: BSc. COMP   TIME: 2 HOURS

EXAMINATION SESSION: DECEMBER   YEAR: 2017

INSTRUCTIONS:

1. Answer question ONE [Compulsory] and any other TWO

2. DO NOT access the examination room while in possession of a smartphone.
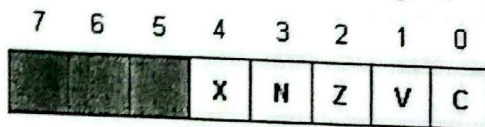
QUESTION ONE [30 Marks] – COMPULSORY

(a) What does it mean when we say that a computer is a programmable device?   [1 Mark]

(b) Give TWO main disadvantages of programming in assembly language   [1 Mark]

(c) Give TWO main advantages of programming in assembly language   [1 Mark]

(d) What is an assembler directive? What is the difference between

     (i)   P   DC.W   2 and   [2 Marks]

     (ii)   Q   DS.W   2?   [2 Marks]

(e) Explain the differences between the following lines of code.   [1 Mark]

     (i)   MOVE.B   #1101, D0,   [1 Mark]

     (ii)   MOVE.B   #%1101, D0   and   [1 Mark]

     (iii)   MOVE.B   #$1101, D0

(f) From the ASCII Table, it is seen that lowercase 'a' is represented as $61, and lowercase 'z' as $7A. Use this information to write a program that prints to the monitor the letters of the alphabet in lowercase characters.   [7 Marks]

(g) Interpret in words what the following assembly language instructions do.

    (i)   MOVE.L   #$8123, D6   **[1 Mark]**

    (ii) MOVE.W   D5, (A6)   **[1 Mark]**

    (iii) MOVE.B   (A7)+, D4   **[1 Mark]**

(h) Write an assembly language program that adds together the data bytes at memory locations $3000, $3001, & $3002 and put the result into location $3003. **[6 Marks]**

(i) Give examples of valid 68K assembly language instructions that use:

    (i)   Absolute addressing   **[1 Mark]**

    (ii) Immediate addressing   **[1 Mark]**

    (iii) Register direct addressing   **[1 Mark]**

    (iv) Address Register Indirect addressing   **[1 Mark]**

QUESTION TWO [20 Marks]

The diagram below show the CCR register.

7	6	5	4	3	2	1	0
			X	N	Z	V	C

(a) What is the CCR register? **[2 Marks]**

(b) Explain the meaning and use of the C, V, Z, N and X flags. **[10 Marks]**

(c) The assembly language instruction given below is used to store a long word in memory in the order of increasing address.

```
MOVE.L   #$81F7A3CB, $3000.
```

Given that the machines' storage format is big-endian, draw memory map that shows the precise location where each byte is stored. **[4 Marks]**

(d) Name and __EXPLAIN__ the TWO types of runtime errors you are likely to experience when executing an assembly language program? **[4 Marks]**

QUESTION THREE [20 Marks]

(a) WRITE an assembly language program that repeats an operation a known number of times using a loop counter. The program should add three bytes of data starting at $1200. The values are loaded into the memory when the program is loaded. **[10 Marks]**

(b) Write a program that produces the three line display, below: [6 Marks]

```
One

Two

Three
```

(c) Draw a flow chart for the program in (b) above. [4 Marks]

QUESTION FOUR [20 Marks]

(a) What is a Stack in the context of the 68000 processor? [1 Mark]

(b) Outline the steps in a typical fetch-execute cycle? [5 Marks]

(c) Explain your understanding of *"The Stored Program Concept"* [4 Marks]

(d) Write an assembly language program that adds three bytes stored in the memory locations 2500, 2501 and 2502. The bytes numbers are 10111010, 100011 and 1111110. The program should then access those memory locations, add them and store the result in memory 2503. Use the labels **Num1**, **Num2**, **Num3** and **Total** to refer to the memory location and also to store the data. [4 Marks]

(e) Suppose that D4 contains $A3D27534_{16}$ and D5 contains $5017C851_{16}$. Perform the operations

(i) ADD.B   D4,D5, [2 Marks]

(ii) ADD.W   D4,D5, [2 Marks]

(iii) ADD.L   D4,D5 [2 Marks]

Specifically indicate the expected state of the CCR flags in each case and comment on your answer.

QUESTION FIVE [20 Marks]

(a) What are the relative merits of the asynchronous memory access and the synchronous memory access? [4 Marks]

(b) Suppose that the bits of CCR could be connected to pins. What advantages would be derived from such an arrangement? [3 Marks]

(c) In 68000 terms, what is the difference between a clock cycle, a bus cycle and an instruction cycle? [3 Marks]

(d) What is meant by the terms partial address decoding and full address decoding? [4 Marks]

(e) A region of up to 512 Kbytes of the 68000's memory space, whose lowest address is $80000, is to be devoted solely to the 68000's supervisor stack. Design an address decoder to implement this arrangement (using 128K × 8 static RAMs). You are to make maximum use of the 68000's function code outputs in this address decoder. [6 Marks]

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