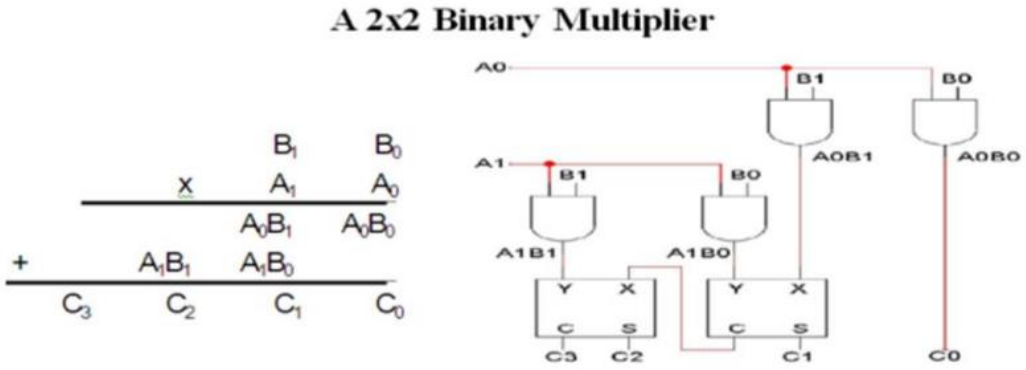
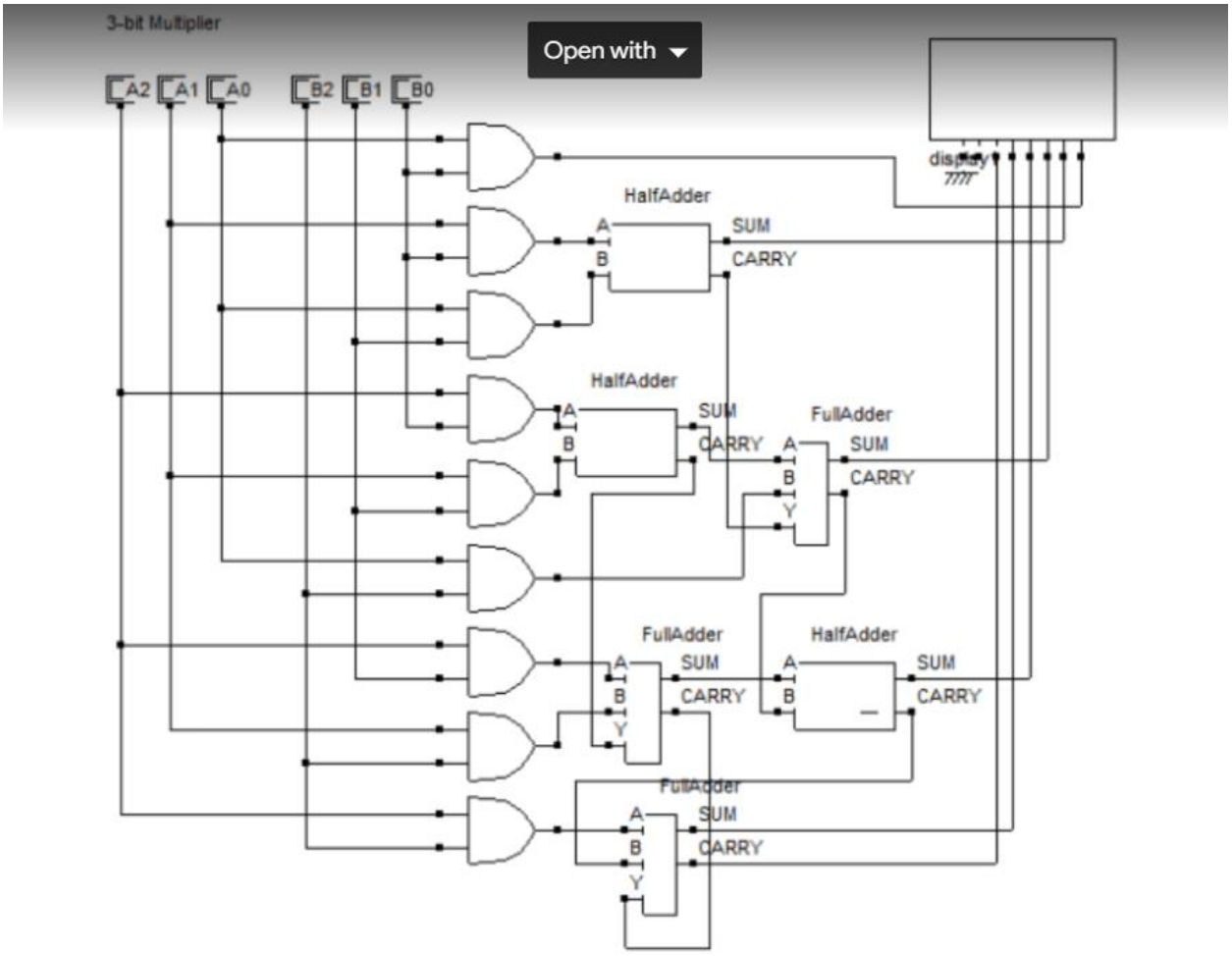
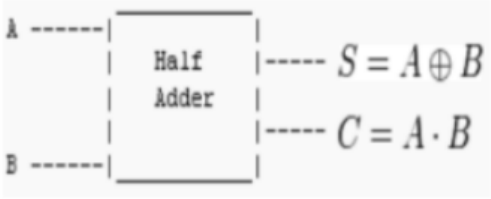
2x2 Binary Muliplier:



3x3 Binary Multiplier:



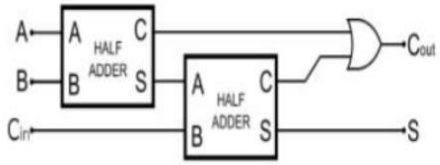
Half Adder:

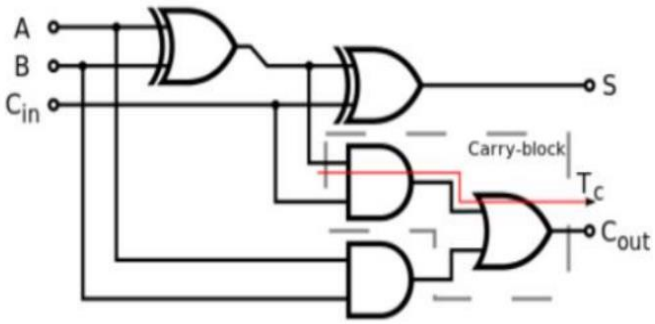


Truth Table:

A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Full Adder:



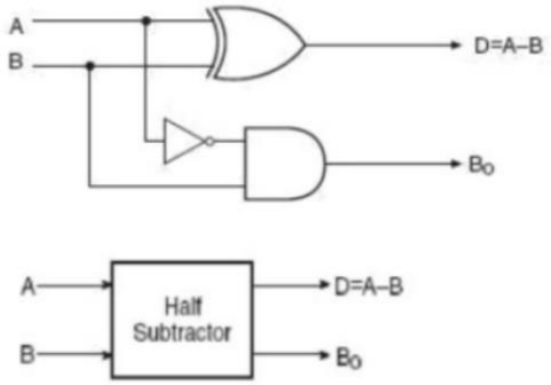


TRUTH TABLE

Inputs			Outputs	
A	B	C_{in}	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

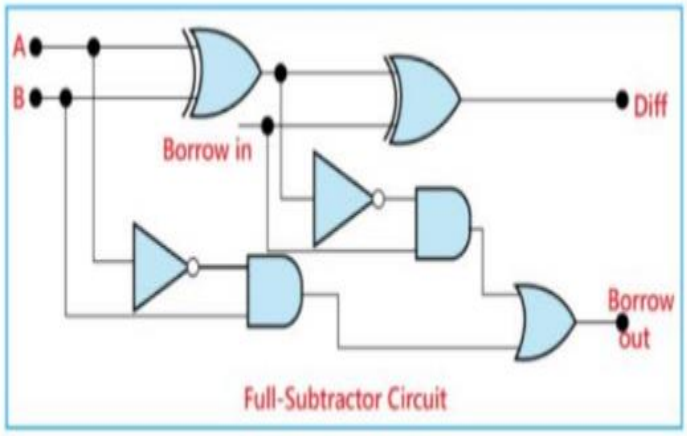
Half Subtractor:

Circuit Diagram:



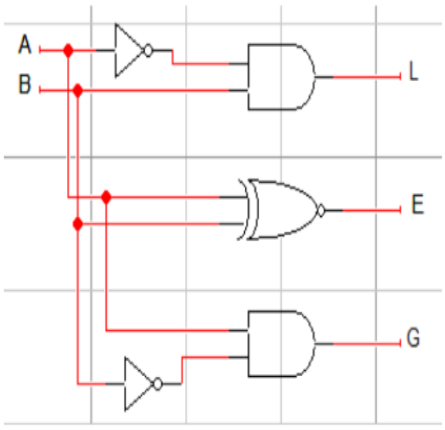
A	B	Difference	Borrow
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

Full Subtractor:



Minuend (A)	Subtrahend (B)	Borrow In (B_{in})	Difference (D)	Borrow Out (B_O)
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

one-bit comparator:

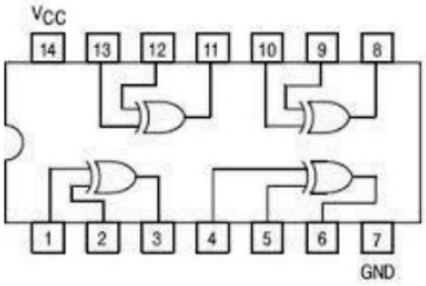


Function Table:

Inputs		Output
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

H= Logic High, L= Logic Low

Connection Diagram:



74148 (8 x 3) Octal to Binary Priority Encoder:

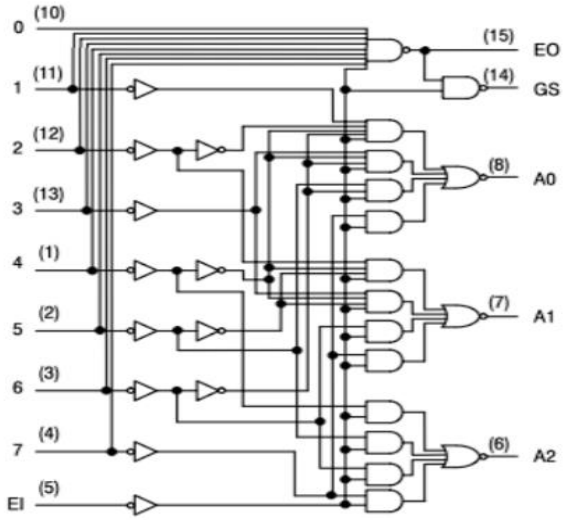


Figure 2. Functional block diagram 74LS148

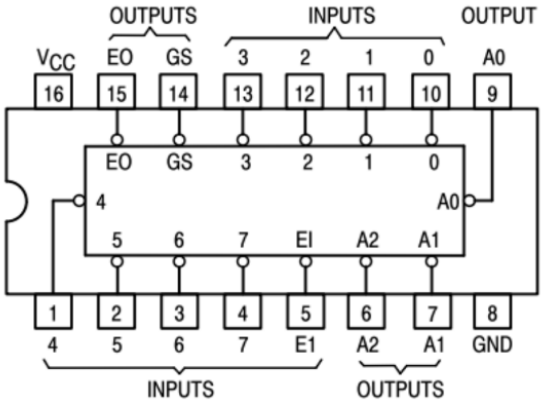


Figure 3. 8to3 Priority Encoding

Inputs								Outputs		
D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	Y_2	Y_1	Y_0
1	0	0	0	0	0	0	0	0	0	0
×	1	0	0	0	0	0	0	0	0	1
×	×	1	0	0	0	0	0	0	1	0
×	×	×	1	0	0	0	0	0	1	1
×	×	×	×	1	0	0	0	1	0	0
×	×	×	×	×	1	0	0	1	0	1
×	×	×	×	×	×	1	0	1	1	0
×	×	×	×	×	×	×	1	1	1	1

Decimal to BCD Priority Encoder (74147):

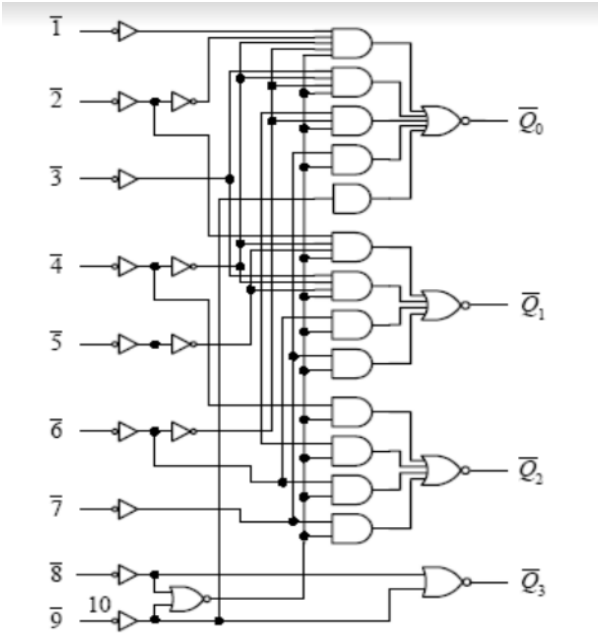
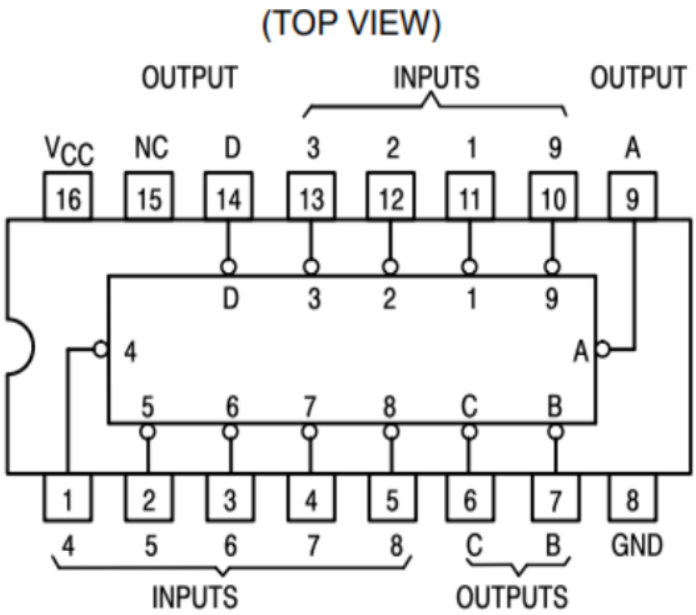
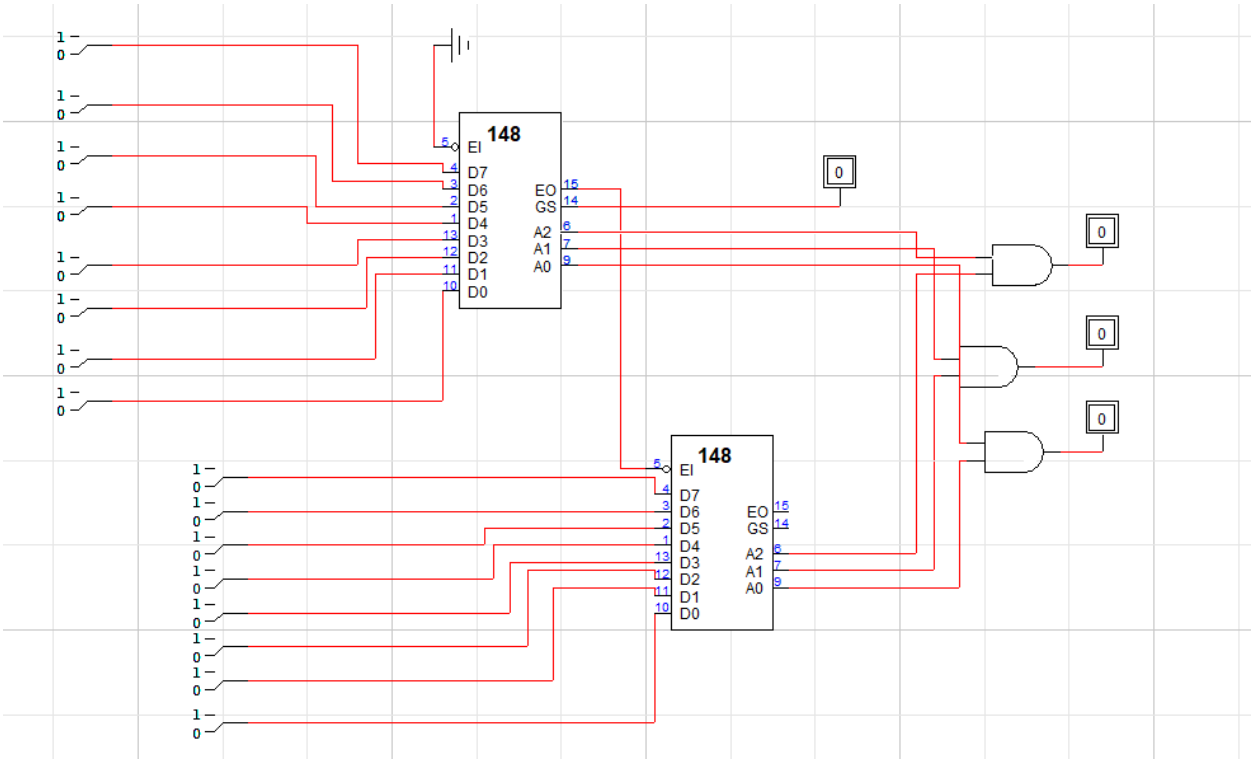


Figure 5. Functional block diagram 74LS147



Decimal Inputs									BCD Outputs			
D_1	D_2	D_3	D_4	D_5	D_6	D_7	D_8	D_9	Y_3	Y_2	Y_1	Y_0
1	1	1	1	1	1	1	1	1	1	1	1	1
×	×	×	×	×	×	×	×	0	0	1	1	0
×	×	×	×	×	×	×	0	1	0	1	1	1
×	×	×	×	×	×	0	1	1	1	0	0	0
×	×	×	×	×	0	1	1	1	1	0	0	1
×	×	×	×	0	1	1	1	1	1	0	1	0
×	×	×	0	1	1	1	1	1	1	0	1	1
×	×	0	1	1	1	1	1	1	1	1	0	0
×	0	1	1	1	1	1	1	1	1	1	0	1
0	1	1	1	1	1	1	1	1	1	1	1	0

16 bit Octal to Binary Priority Encoder using 74148 IC.:



Implementation of 3-8-line Decoder using IC 74LS138:

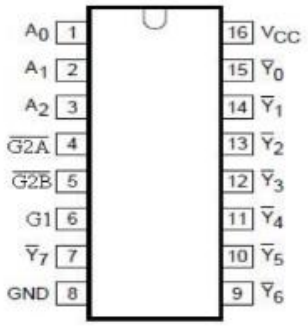


Fig 1. Pin Configuration

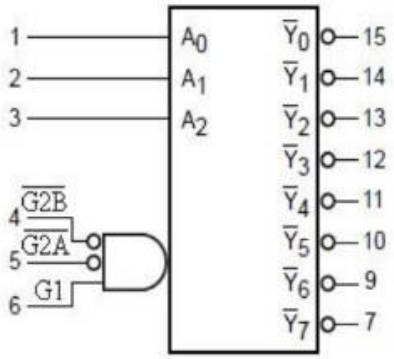


Fig 2. Logic Symbol

$A_0 - A_2$	Input Bits
G_{2A}', G_{2B}'	Enable (Active LOW) Inputs
G_1	Enable (Active HIGH) Inputs
Y_0' - Y_7'	Active LOW Outputs

Implementation of BCD to Seven Segment Decoder using IC 74LS47:

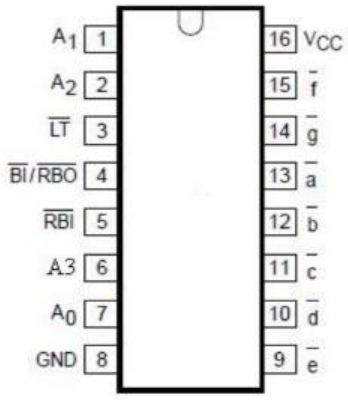


Fig 3. Pin Configuration

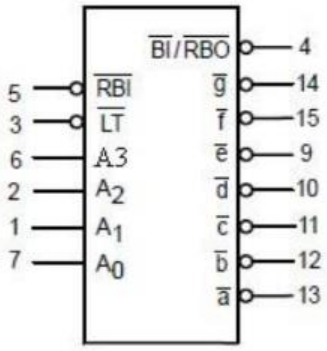


Fig 4. Logic Symbol

A0 – A3	BCD Inputs
RBI'	Ripple Blanking Input (Active LOW)
LT'	Lamp Test Input (Active LOW)
BI'/RBO'	Blanking Input or Ripple Blanking Output (Active LOW)
a' – g'	Active LOW Outputs

8x1 Multiplexer:

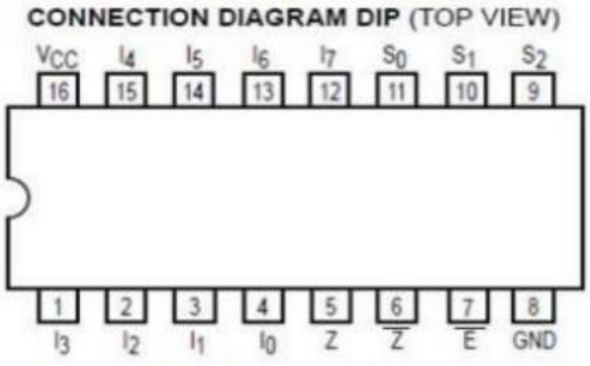


Fig 1. Pin Configuration

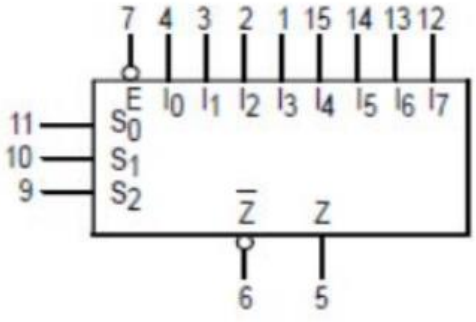


Fig 2. Logic Symbol

PIN Description:

S0–S2	**Select Inputs**
E'	**Enable (Active LOW)**
Input I0–I7	**Multiplexer Inputs**
Z	**Multiplexer Output**
Z'	**Complementary Multiplexer Output**

SR Latch Using NOR Gate:

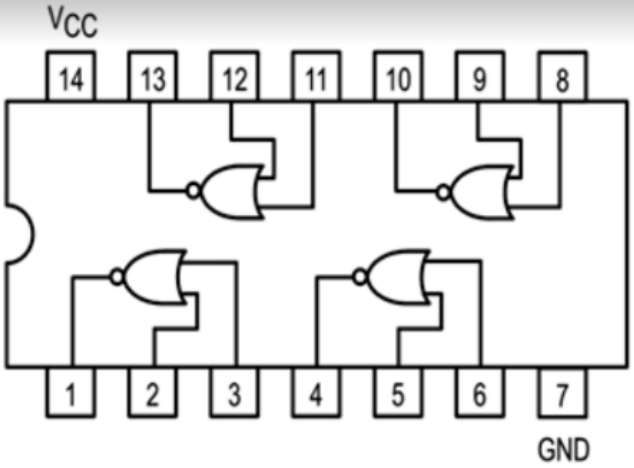


Figure. IC 74LS02 Pin Configuration

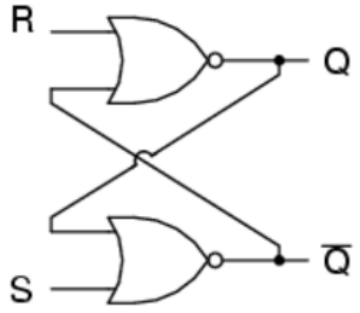


Figure. SR Latch Logic Diagram

Function Table of SR Latch

Inputs		Outputs		Comments
S	R	Q	Q'	
0	0			
0	1	0	1	
1	0	1	0	
1	1	1	1	

D Latch:

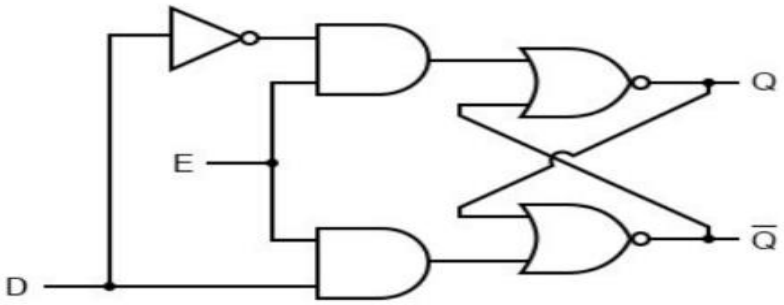
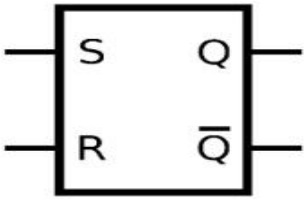
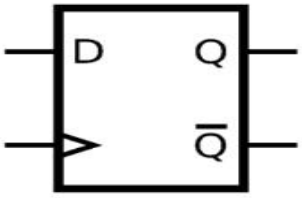


Figure. D Latch Logic Diagram





Function Table of D Latch

Inputs				Outputs		Comments
S	R	E	D	Q	Q'	
		0	0			
		0	1			
		1	0	0	1	
		1	1	1	0	

Edge Triggered D Flip-Flop:

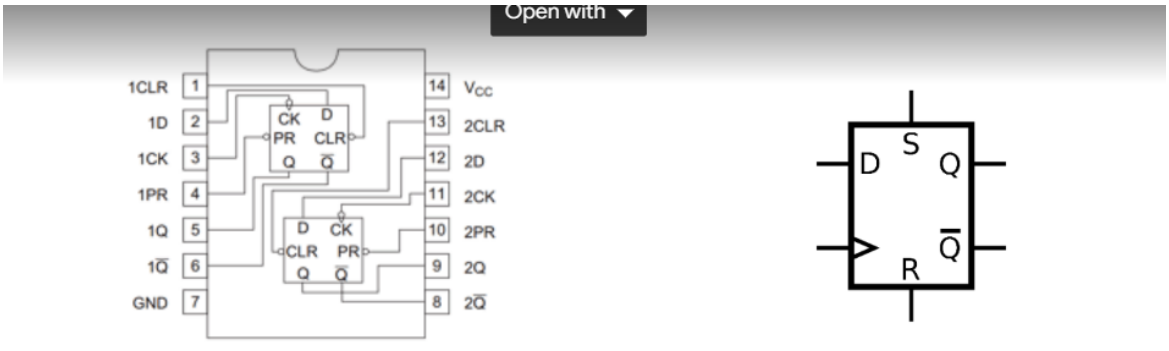


Figure. IC 74LS74 Pin Configuration

Figure. Graphic symbol D flip-flop

Function Table of D Flip-Flop

Inputs				Outputs		Comments
D	CLK	Preset	Clear	Q	Q'	

JK Flip-Flop:

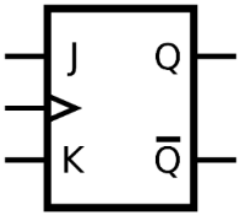


Figure. Graphic symbol JK Flip-Flop

Truth Table

J	K	CLK	Q
0	0	↑	Q_0 (no change)
1	0	↑	1
0	1	↑	0
1	1	↑	$\overline{Q}_0$ (toggles)

Figure. JK Flip-Flop Truth Table

Dual JK Flip Flop 74LS73

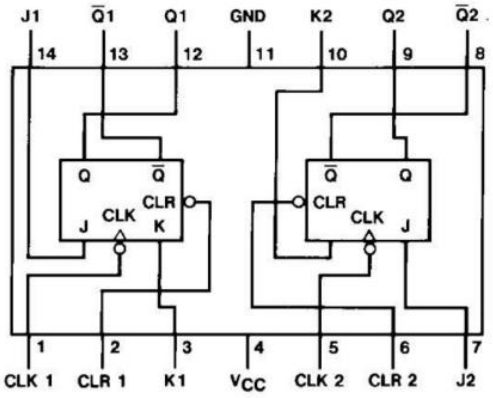


Figure. IC 74LS73 Pin Configuration

CLR	CLK	J	K	Q	$\overline{Q}$
L	X	X	X	L	H
H	↓	L	H	L	H
H	↓	H	L	H	L
H	↓	L	L	Retains previous state	
H	↓	H	H	Toggle	

Figure. Dual JK Flip-Flop Truth Table