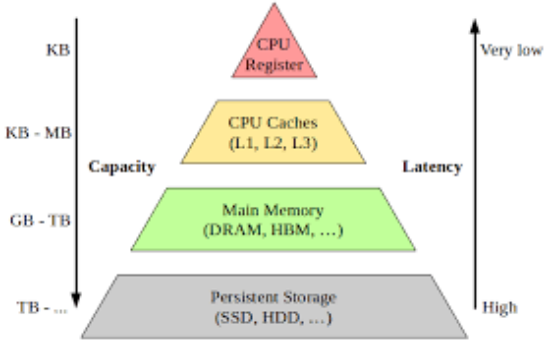
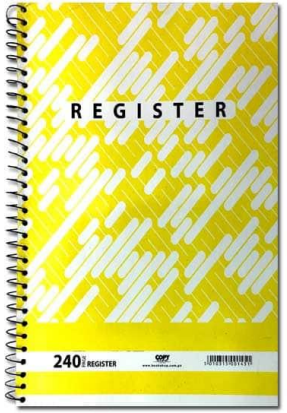


Shift Registers

Chapter 8



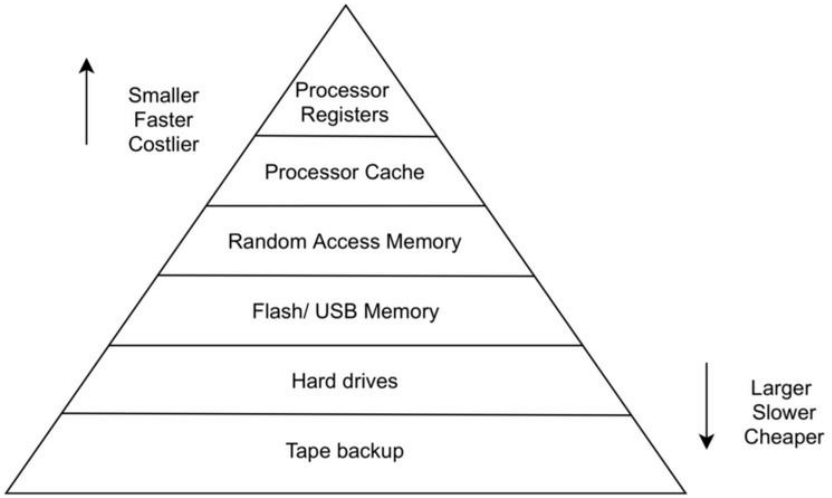
Sumaiyah Zahid

Registers

The smallest and fastest memory

It is used solely for storing and shifting data (1s and 0s)

A register can consist of one or more flip-flops used to store and shift data.



Registers

The storage capacity of a register is the total number of bits (1s and 0s) of digital data it can retain.

Each stage (flip-flop) in a shift register represents one bit of storage capacity; therefore, the number of stages in a register determines its storage capacity

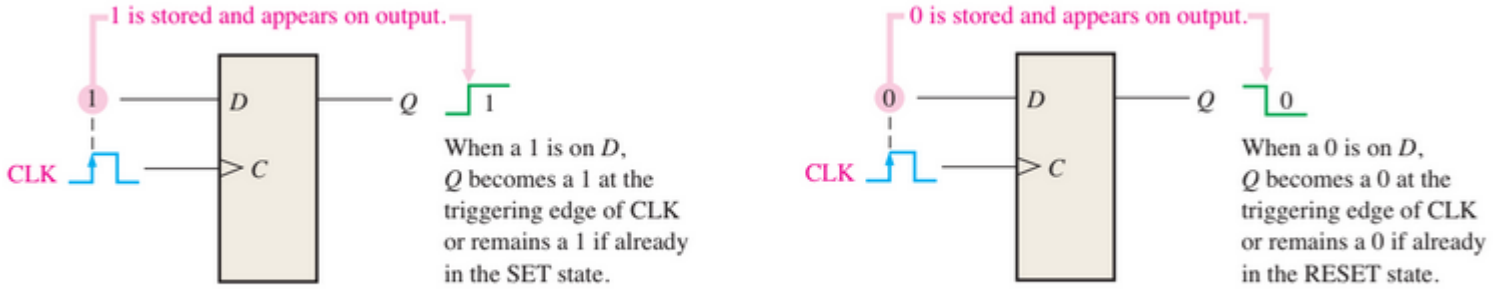


FIGURE 8–1 The flip-flop as a storage element.

Shift Registers

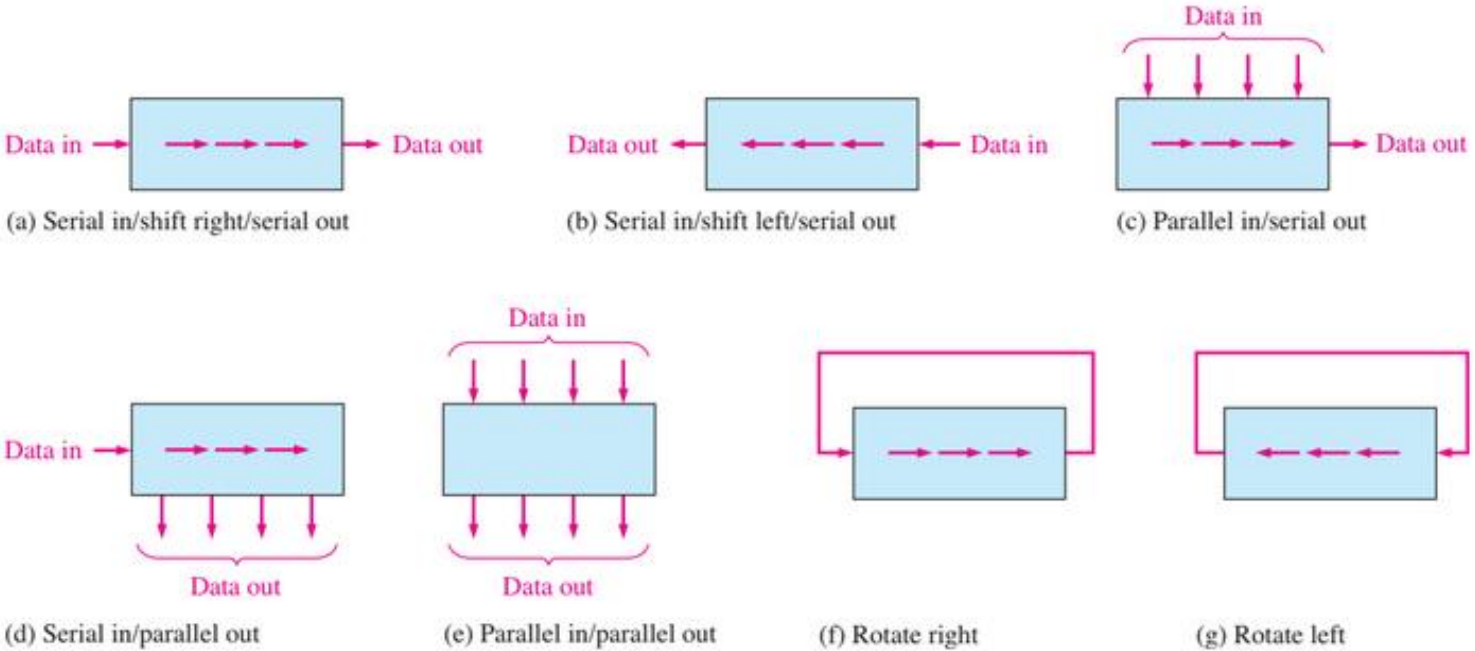


FIGURE 8–2 Basic data movement in shift registers. (Four bits are used for illustration. The bits move in the direction of the arrows.)

Serial In/Serial Out Shift Registers

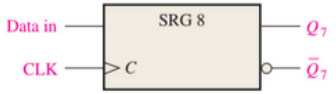


FIGURE 8–5 Logic symbol for an 8-bit serial in/serial out shift register.

4-bit Register implemented with 4 D flip-flops.

With four stages, this register can store up to four bits of data.

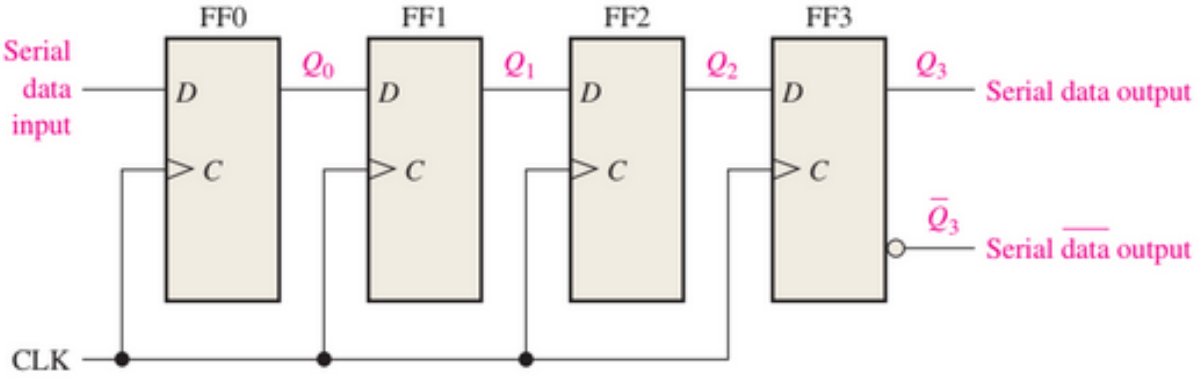


FIGURE 8–3 Serial in/serial out shift register.

Serial In/Serial Out Shift Registers

For serial data, one bit at a time is transferred.

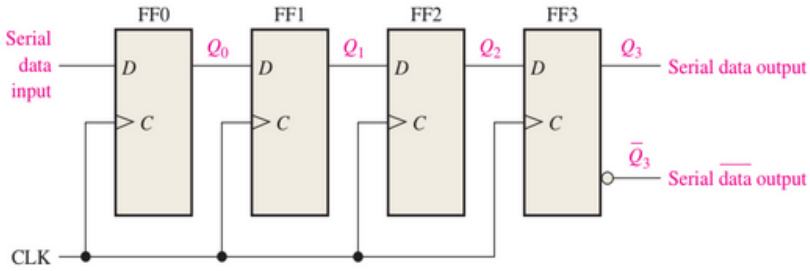


FIGURE 8–3 Serial in/serial out shift register.

TABLE 8–1

Shifting a 4-bit code into the shift register in Figure 8–3. Data bits are indicated by a beige screen.

CLK	FF0 (Q_0)	FF1 (Q_1)	FF2 (Q_2)	FF3 (Q_3)
Initial	0	0	0	0
1	**0**	0	0	0
2	**1**	**0**	0	0
3	**0**	**1**	**0**	0
4	**1**	**0**	**1**	**0**

Serial In/Serial Out Shift Registers

For serial data, one bit at a time is transferred.

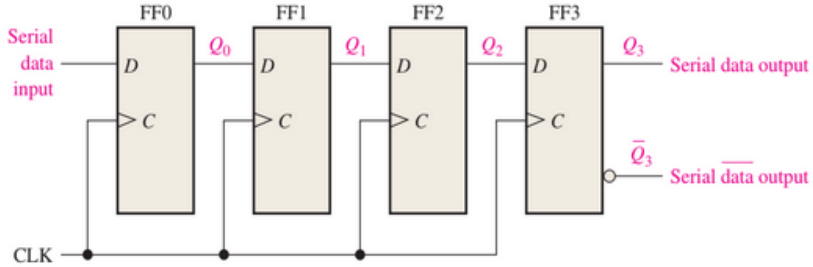


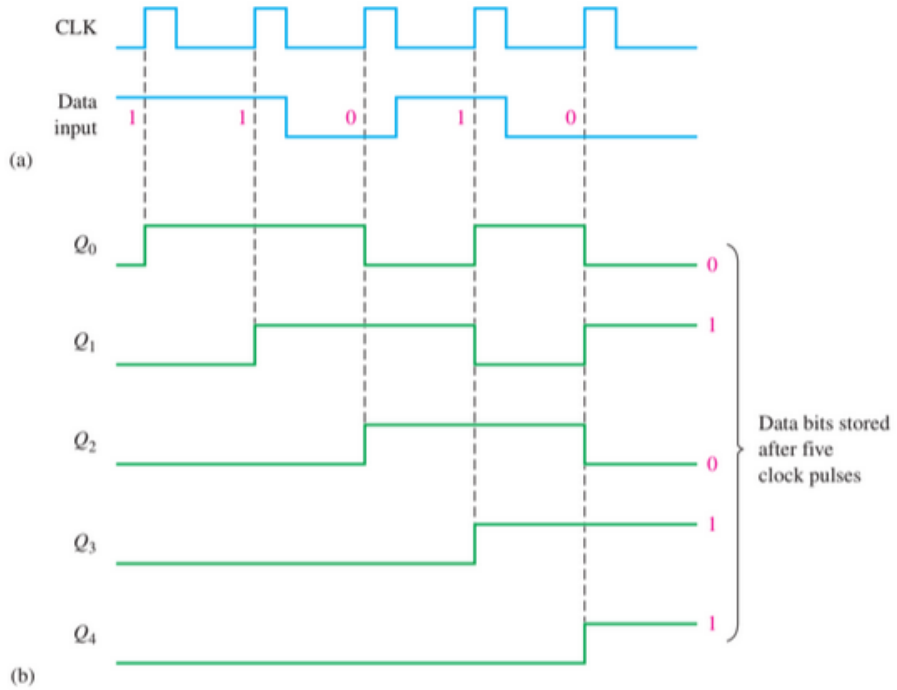
FIGURE 8–3 Serial in/serial out shift register.

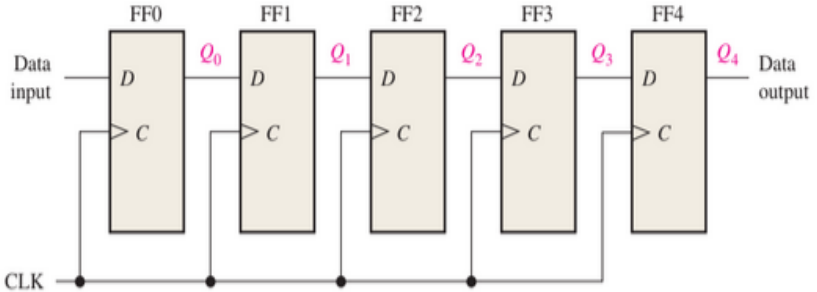
TABLE 8–2

Shifting a 4-bit code out of the shift register in Figure 8–3. Data bits are indicated by a beige screen.

CLK	FF0 (Q_0)	FF1 (Q_1)	FF2 (Q_2)	FF3 (Q_3)
Initial	**1**	**0**	**1**	**0**
5	0	**1**	**0**	**1**
6	0	0	**1**	**0**
7	0	0	0	**1**
8	0	0	0	0

Serial In/Serial Out Shift Registers





Serial In/Parallel Out Shift Registers

Data bits are entered serially least-significant bit first

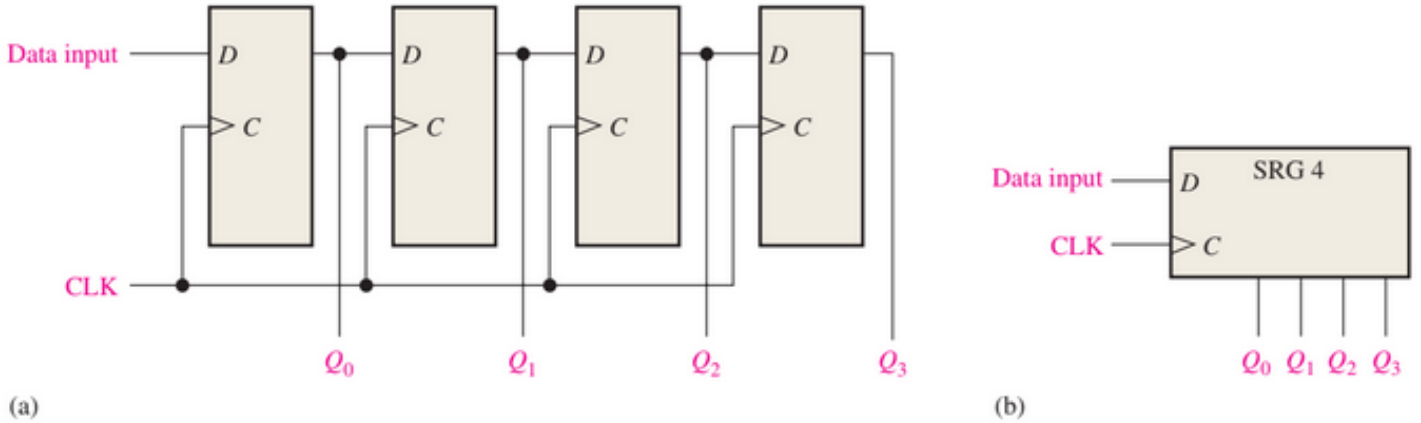
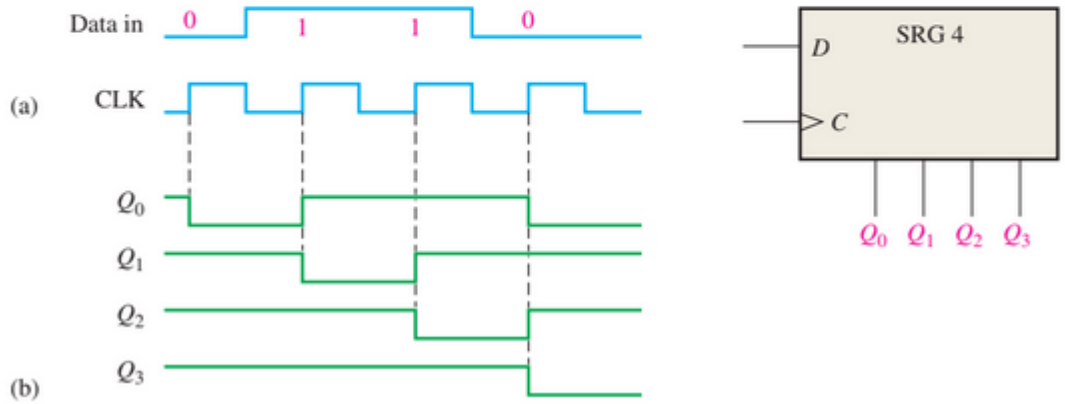


FIGURE 8–6 A serial in/parallel out shift register.

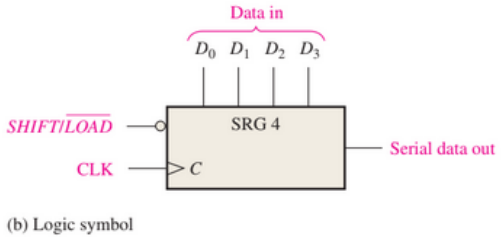
Serial In/Parallel Out Shift Registers

EXAMPLE 8–2

Show the states of the 4-bit register (SRG 4) for the data input and clock waveforms in Figure 8–7(a). The register initially contains all 1s.

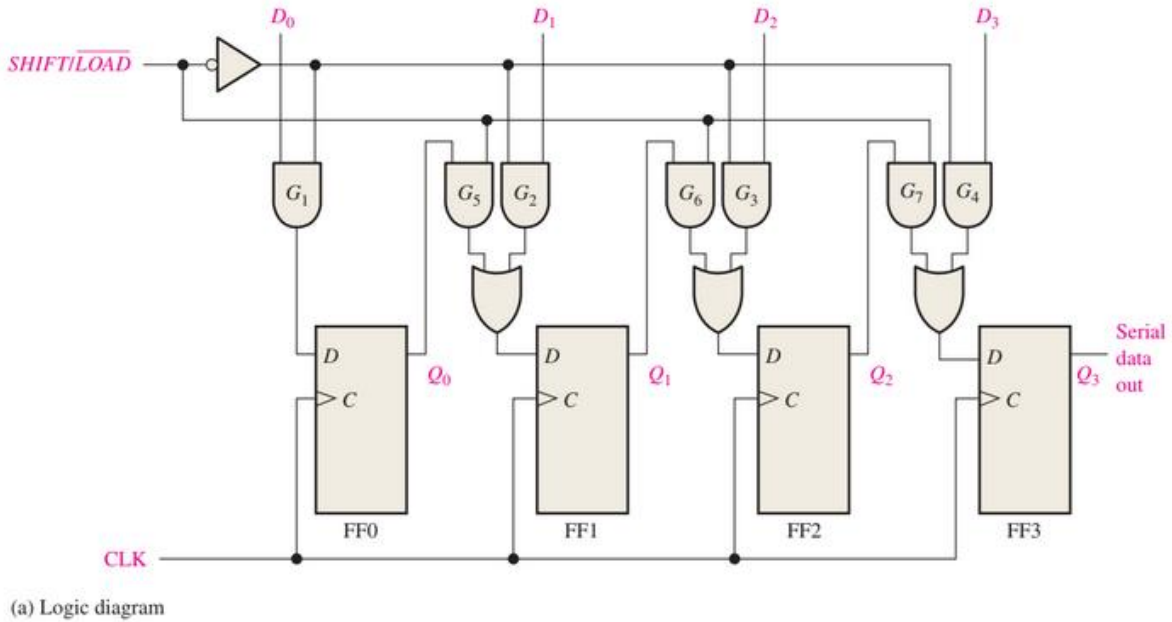


Parallel In/Serial Out Shift Registers



(b) Logic symbol

For parallel data, multiple bits are transfe



(a) Logic diagram

Parallel In/Serial Out Shift Registers

EXAMPLE 8–3

Show the data-output waveform for a 4-bit register with the parallel input data and the clock and *SHIFT*/$\overline{LOAD}$ waveforms given in Figure 8–11(a). Refer to Figure 8–10(a) for the logic diagram.

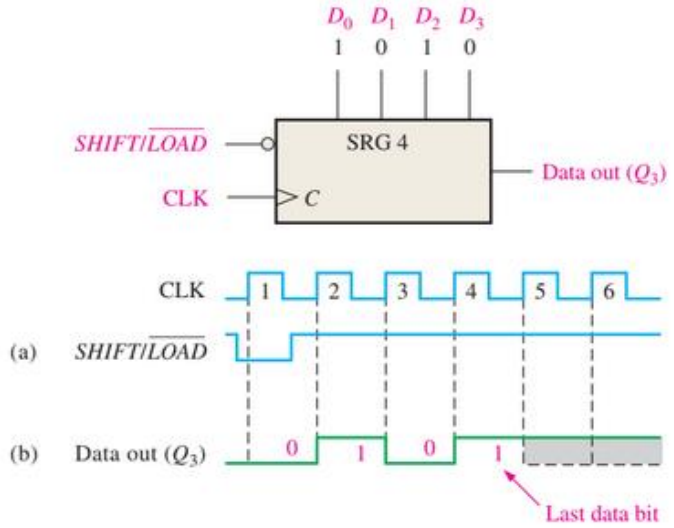


FIGURE 8–11

Parallel In/Parallel Out Shift Registers

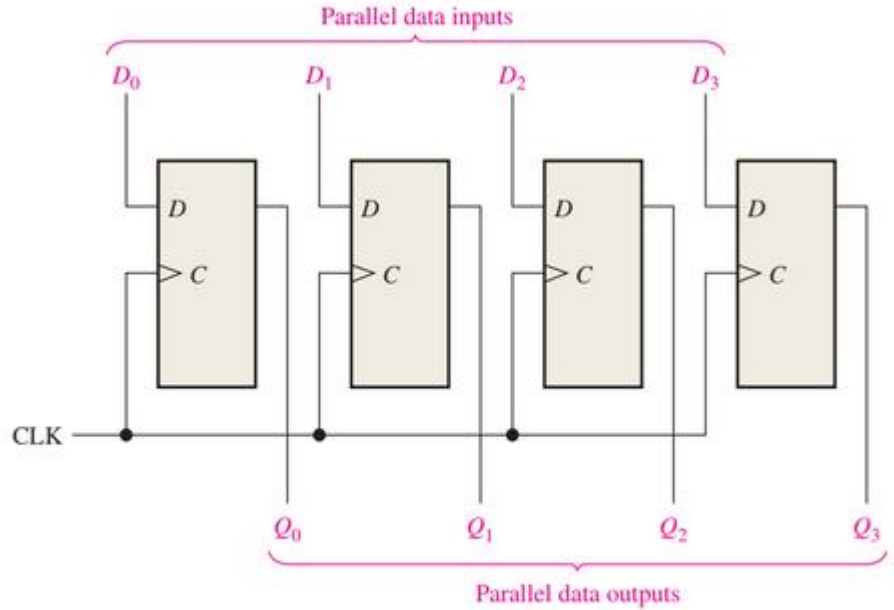


FIGURE 8–14 A parallel in/parallel out register.

Home Tasks

1. Develop the logic diagram for the shift registers using J-K flip-flops to replace the D flip-flops.

2. How many clock pulses are required to enter a byte of data serially into an 8-bit shift register?

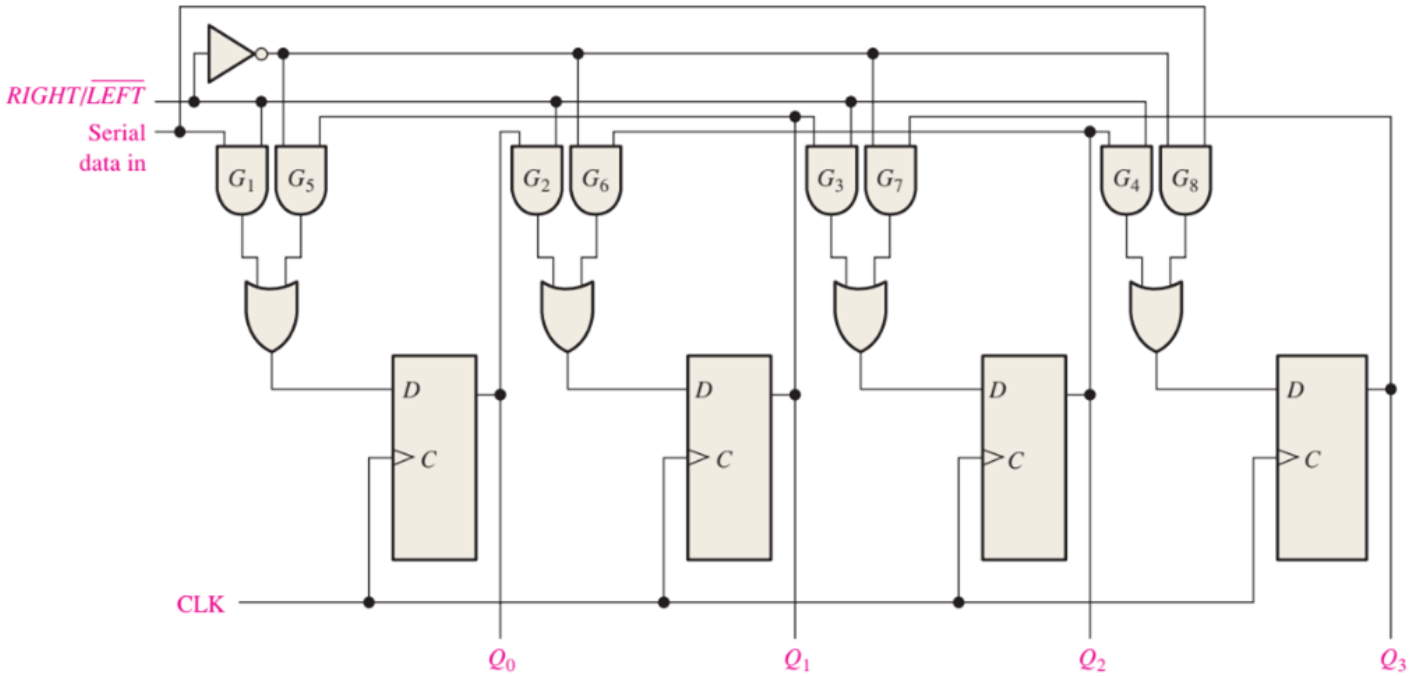
3. The bit sequence 1101 is serially entered (least-significant bit first) into a 4-bit parallel out shift register that is initially clear. What are the Q outputs after two clock pulses?

4. How can a serial in/parallel out register be used as a serial in/serial out register?

5. Explain the function of the SHIFT/LOAD input.

6. Is the parallel load operation in Parallel in Serial Out shift register synchronous or asynchro nous? What does this mean?

Bidirectional Shift Registers

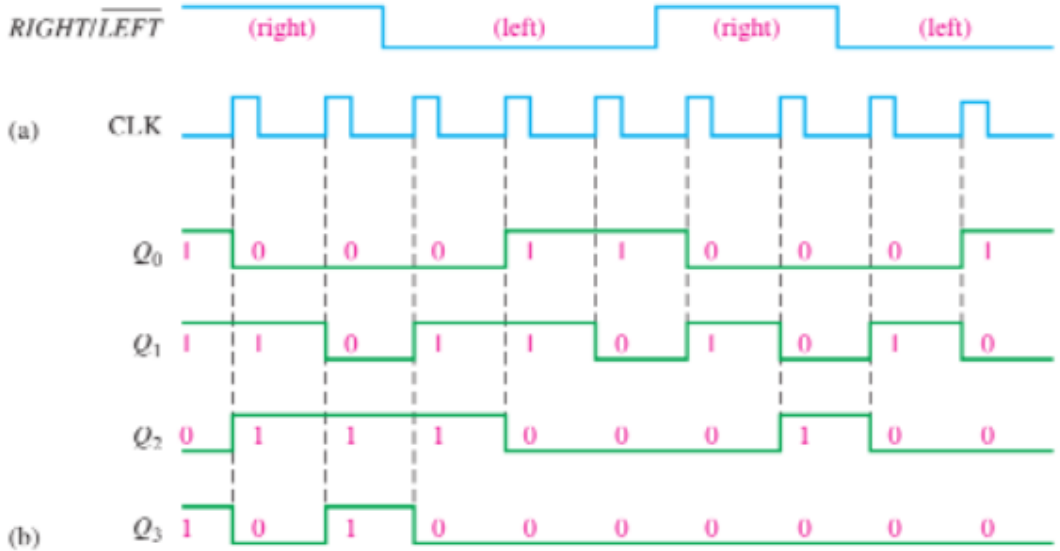


MultiSim **FIGURE 8–17** Four-bit bidirectional shift register. Open file F08-17 to verify the operation.

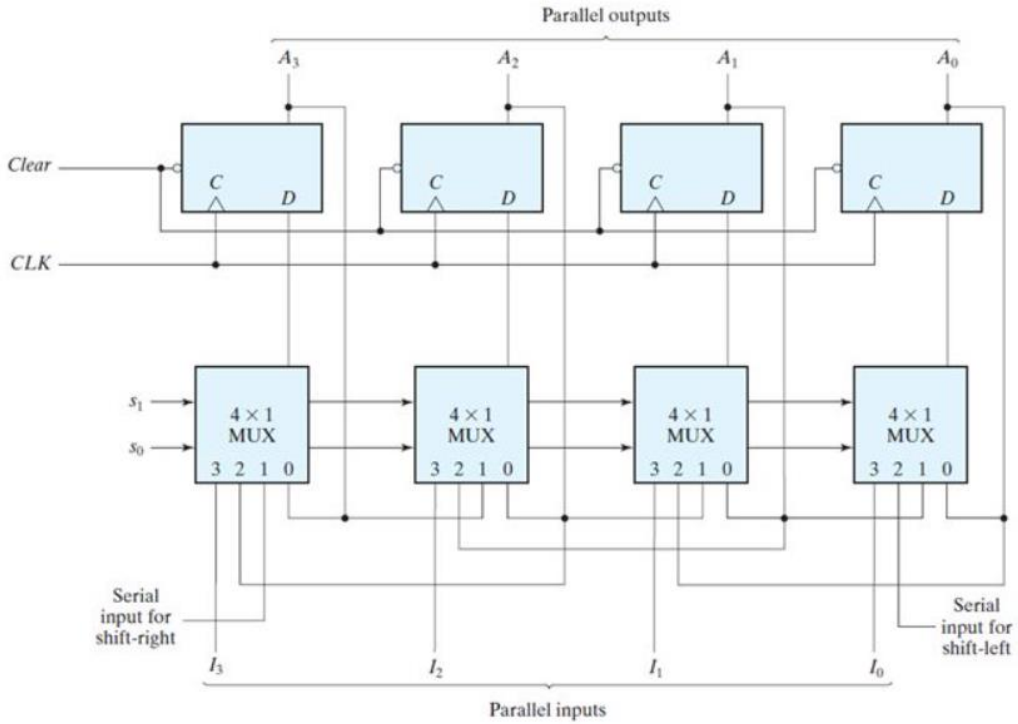
Bidirectional Shift Registers

EXAMPLE 8–4

Determine the state of the shift register of Figure 8–17 after each clock pulse for the given *RIGHT*/$\overline{LEFT}$ control input waveform in Figure 8–18(a). Assume that $Q_0 = 1$, $Q_1 = 1$, $Q_2 = 0$, and $Q_3 = 1$ and that the serial data-input line is LOW.



Universal Shift Register



Univ

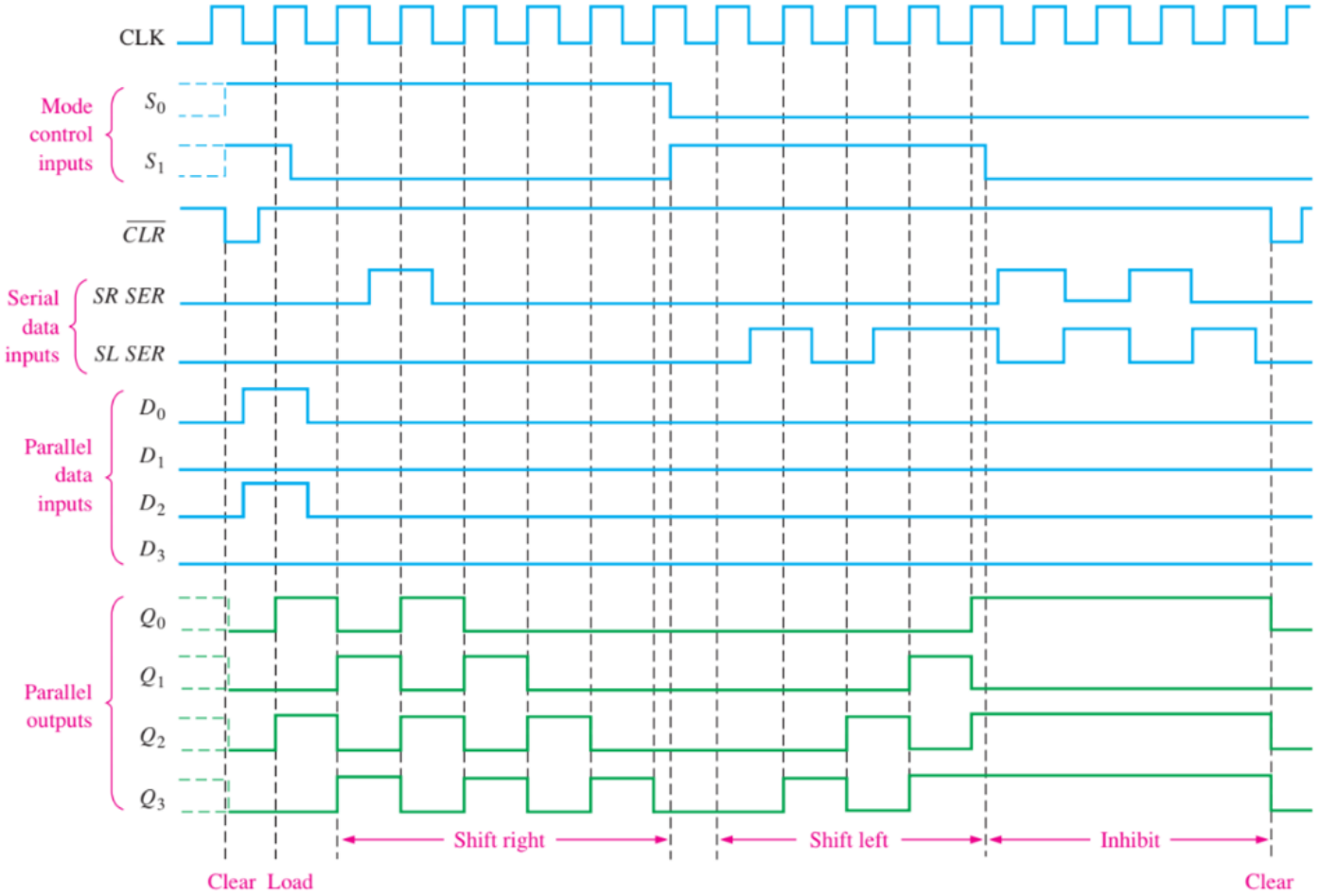


FIGURE 8–20 Sample timing diagram for a 74HC194 shift register.

Shift Register Counter

The Johnson Counter

4-bit sequence has a total of eight states, or bit patterns.
5-bit sequence has a total of ten states

In general, a Johnson counter will produce a modulus of 2n, where n is the number of stages in the counter.

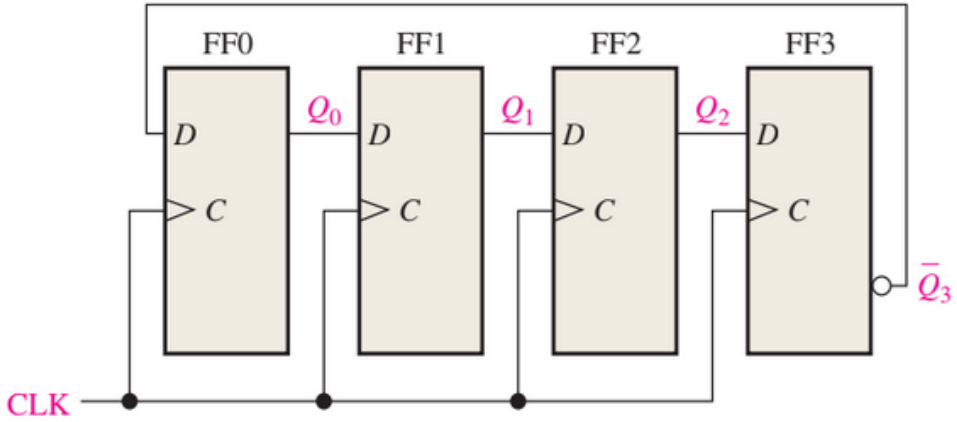
Extensively used as frequency dividers and pattern recognizers.

Shift Register Counter ~ The Johnson Counter

TABLE 8–3

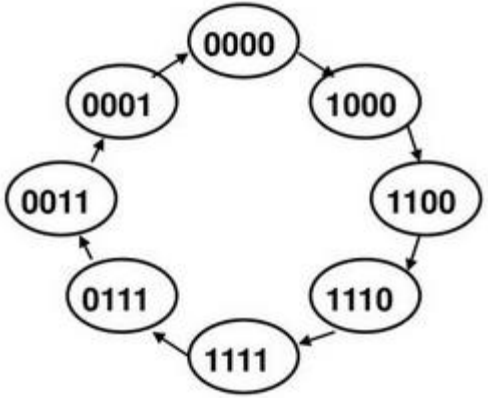
Four-bit Johnson sequence.

Clock Pulse	Q_0	Q_1	Q_2	Q_3
0	0	0	0	0
1	1	0	0	0
2	1	1	0	0
3	1	1	1	0
4	1	1	1	1
5	0	1	1	1
6	0	0	1	1
7	0	0	0	1



(a) Four-bit Johnson counter

Shift Register Counter ~ The Johnson Counter



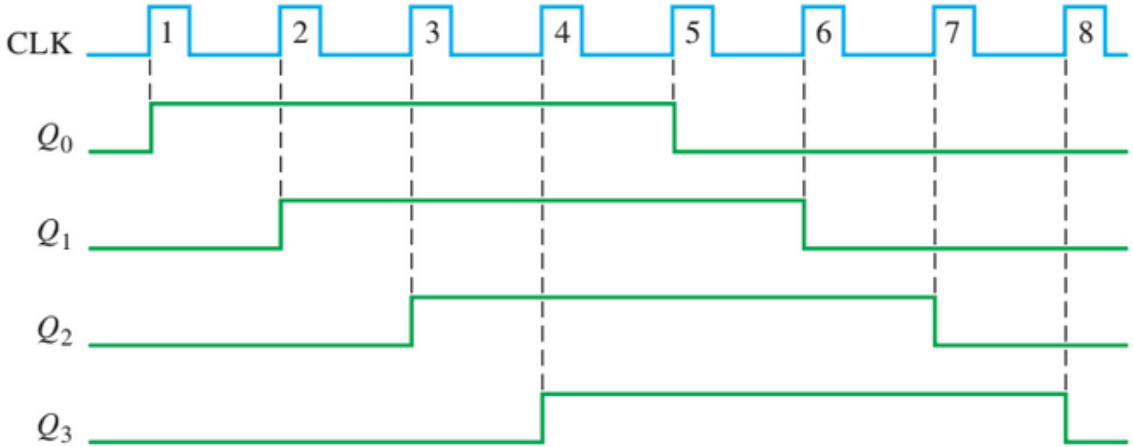


FIGURE 8–22 Timing sequence for a 4-bit Johnson counter.

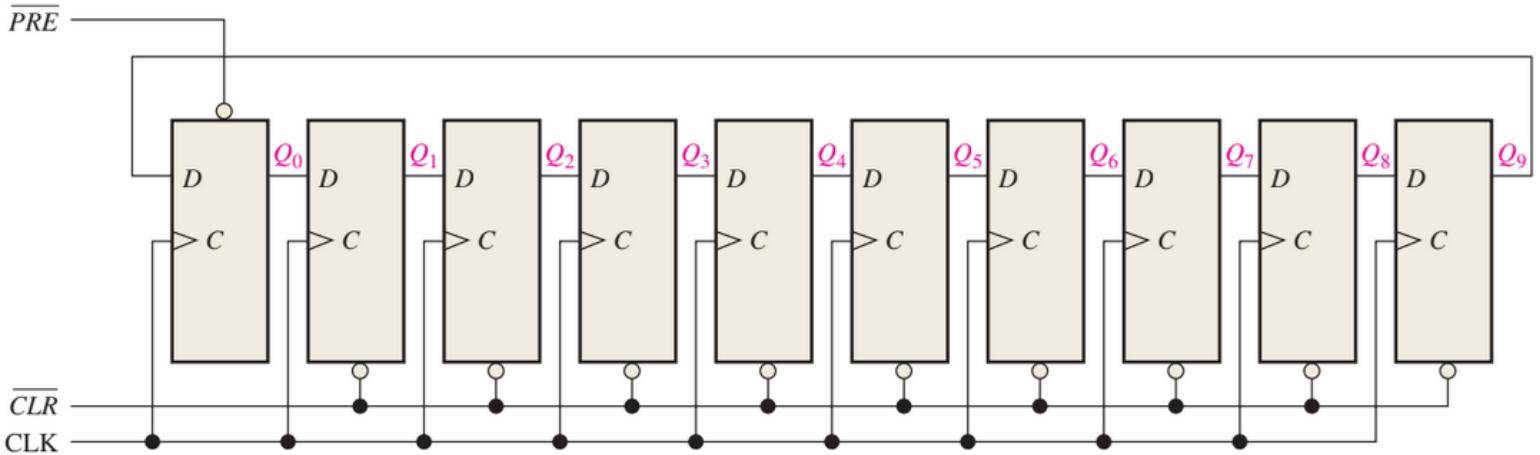
Johnson counters are used as frequency dividers and pattern recognizers.

It can be used to create complicated finite state machines in hardware logic design.

Shift Register Counter

The Ring Counter

A ring counter utilizes one flip-flop for each state in its sequence. For 10-bit ring counter, there is a unique output for each decimal digit.



Shift Register Counter ~ The Ring Counter

TABLE 8–5

Ten-bit ring counter sequence.

Clock Pulse	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	Q_8	Q_9
0	1	0	0	0	0	0	0	0	0	0
1	0	1	0	0	0	0	0	0	0	0
2	0	0	1	0	0	0	0	0	0	0
3	0	0	0	1	0	0	0	0	0	0
4	0	0	0	0	1	0	0	0	0	0
5	0	0	0	0	0	1	0	0	0	0
6	0	0	0	0	0	0	1	0	0	0
7	0	0	0	0	0	0	0	1	0	0
8	0	0	0	0	0	0	0	0	1	0
9	0	0	0	0	0	0	0	0	0	1

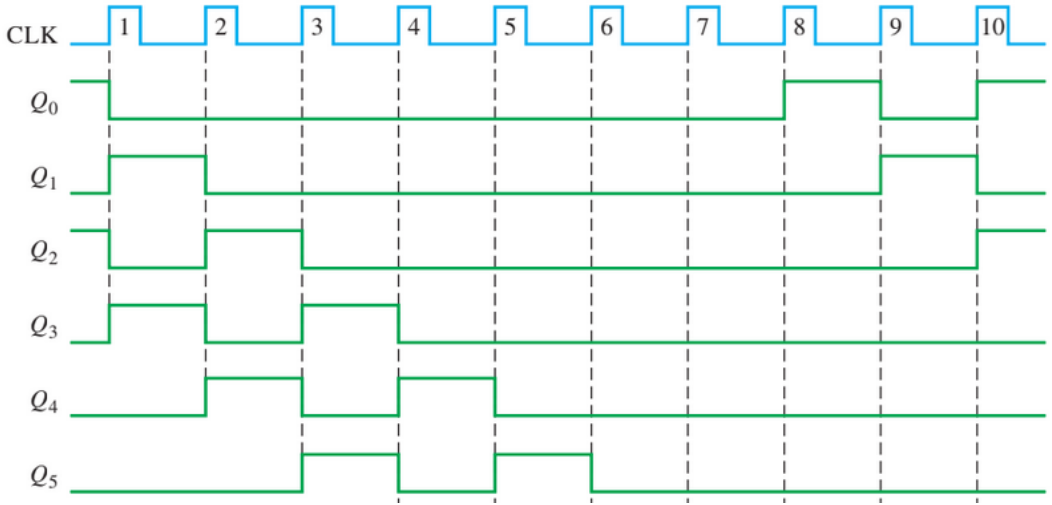
Shift Register Counter ~ The Ring Counter

EXAMPLE 8–5

If a 10-bit ring counter similar to Figure 8–24 has the initial state 1010000000, determine the waveform for each of the Q outputs.

Solution

See Figure 8–25.



Shift Register Applications

Time Delay

An 8-bit serial in/serial out shift register is used with a clock frequency of 1 MHz to achieve a time delay (td) of 8 micro sec (8 * 1 micro sec).

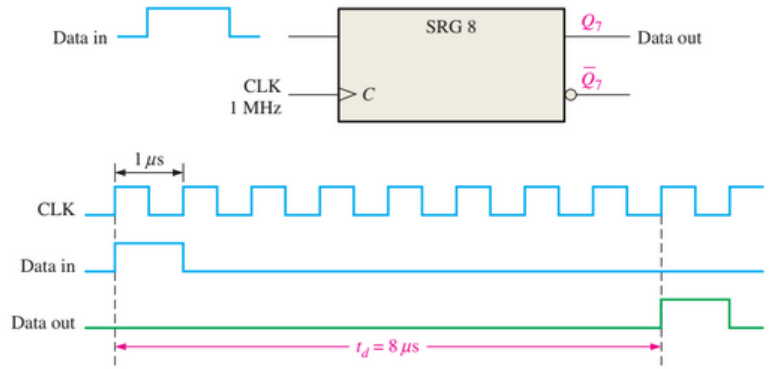


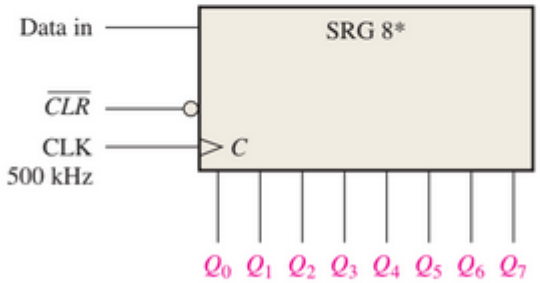
FIGURE 8–26 The shift register as a time-delay device.

Shift Register Applications

Time Delay

EXAMPLE 8–6

Determine the amount of time delay between the serial input and each output in Figure 8–27. Show a timing diagram to illustrate.



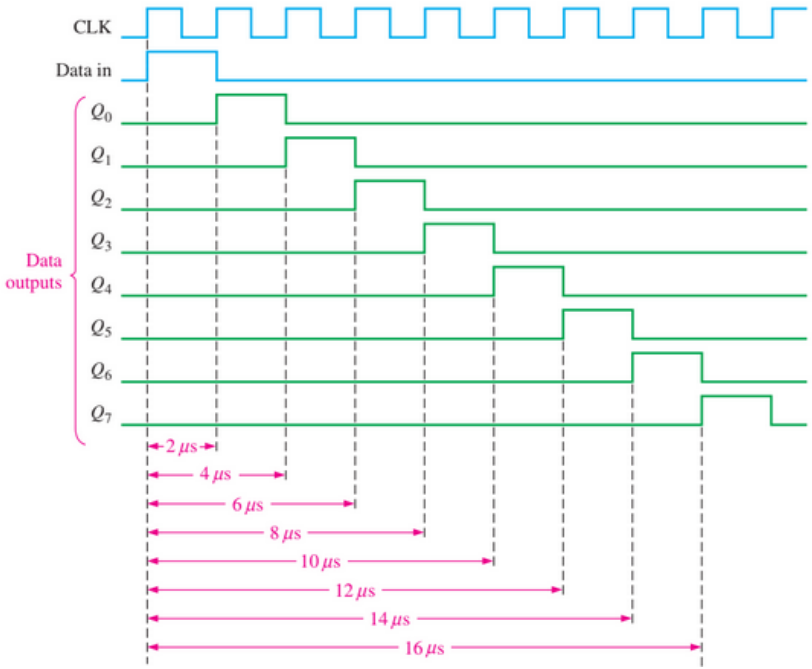
* Data shifts from Q_0 toward Q_7.

Shift Register Applications

Time Delay

Solution

The clock period is 2 μs. Thus, the time delay can be increased or decreased in 2 μs increments from a minimum of 2 μs to a maximum of 16 μs, as illustrated in Figure 8–28.



Shift Register Applications

Serial-to-Parallel Data Converter

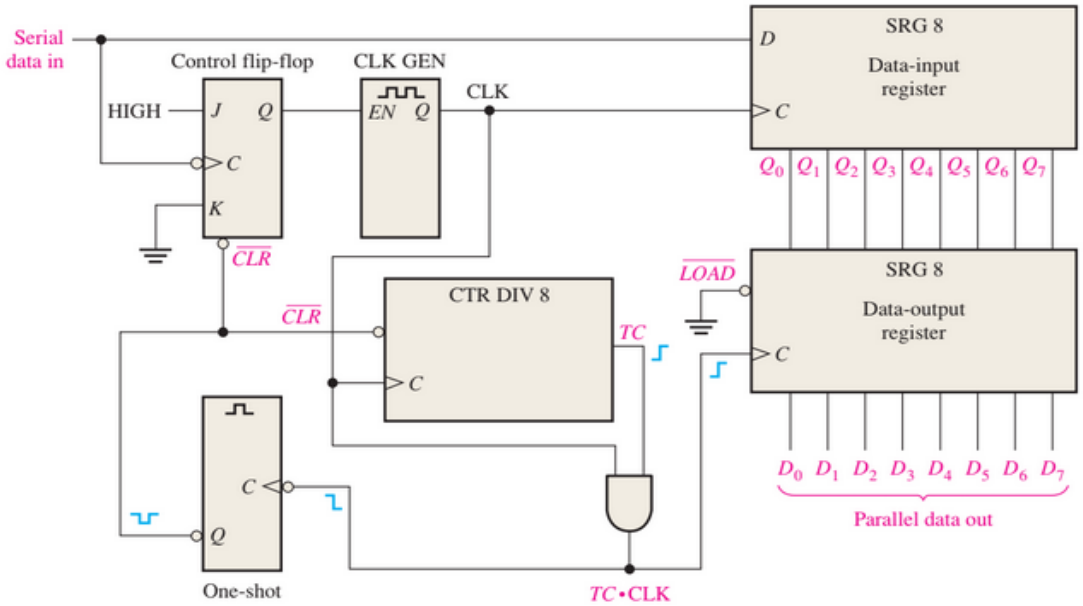
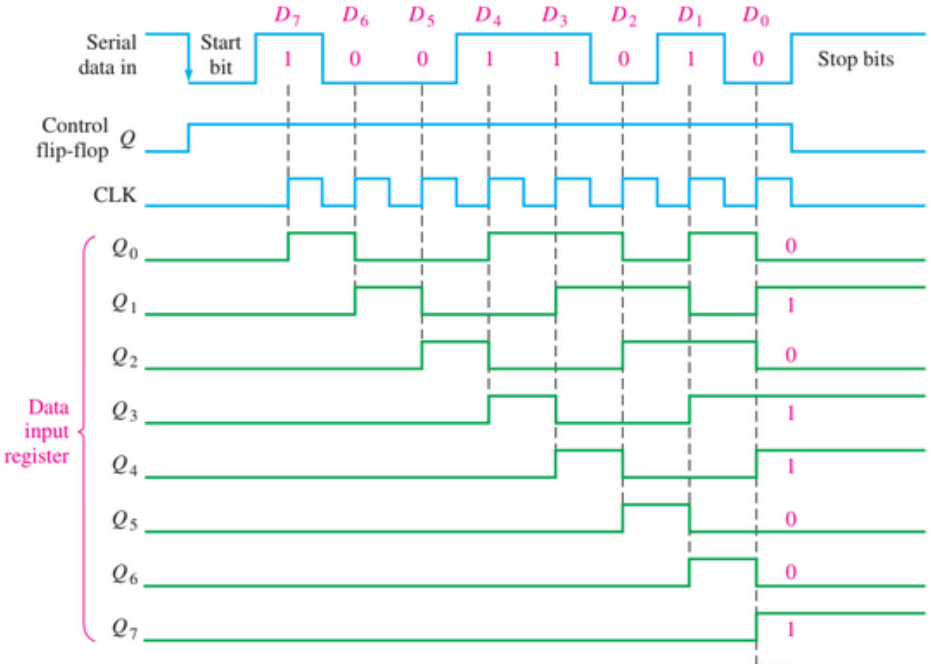


FIGURE 8–31 Simplified logic diagram of a serial-to-parallel converter.

Shift Register Applications

Serial-to-Parallel Data Converter



Shift Register Applications

Serial-to-Parallel Data Converter

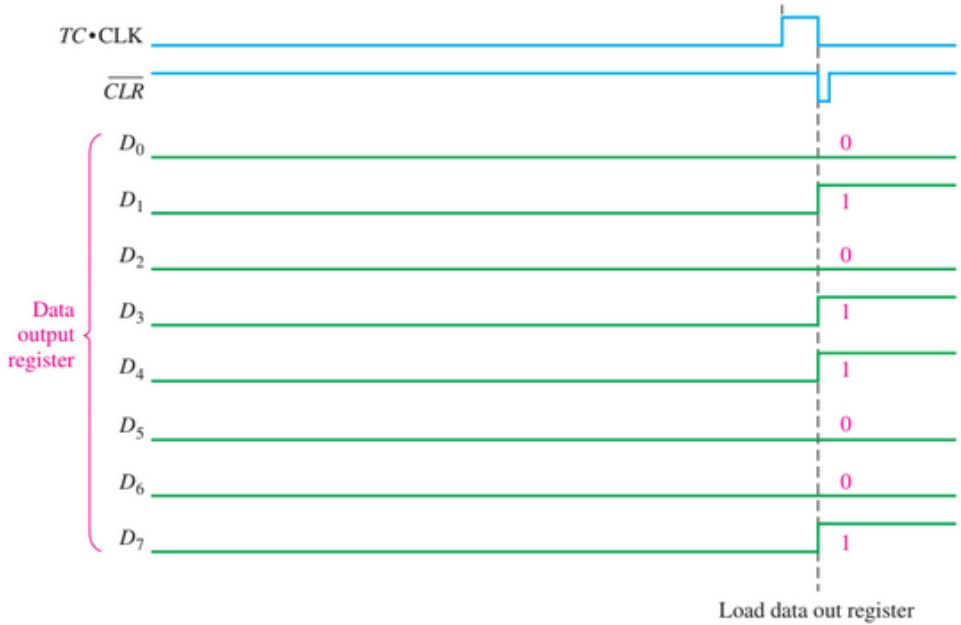


FIGURE 8–33 Timing diagram illustrating the operation of the serial-to-parallel data converter in Figure 8–31.

Shift Register Applications

Universal Asynchronous Receiver Transmitter (UART)

The UART receives data in serial format, converts the data to parallel format, and places them on the data bus.

The UART also accepts parallel data from the data bus, converts the data to serial format, and transmits them to an external device.

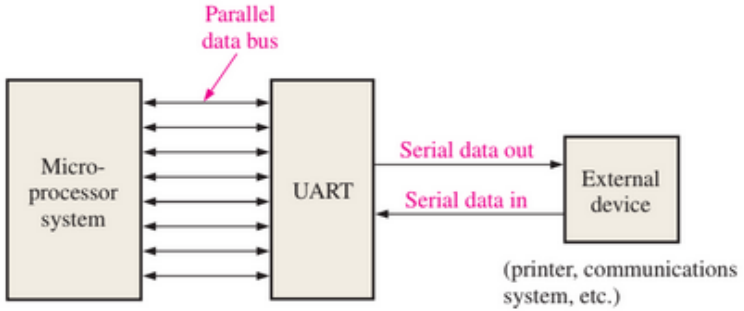


FIGURE 8–34 UART interface.

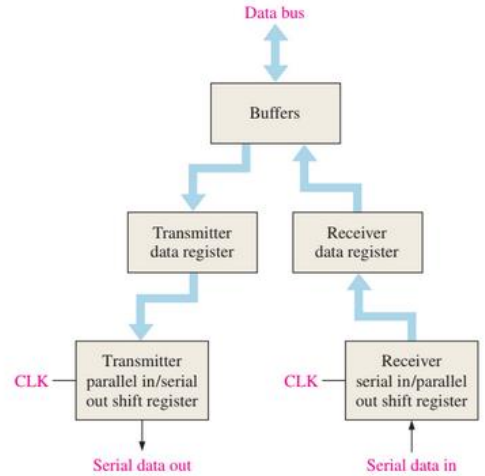


FIGURE 8–35 Basic UART block diagram.

Practice Questions

https://www.allaboutcircuits.com/worksheets/shift-registers/

https://www.allaboutcircuits.com/worksheets/flip-flop-circuits/