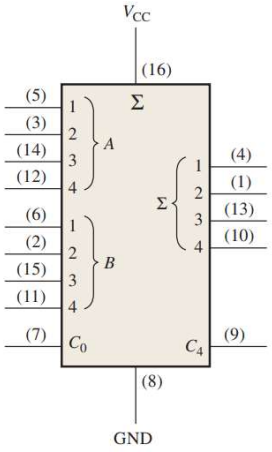
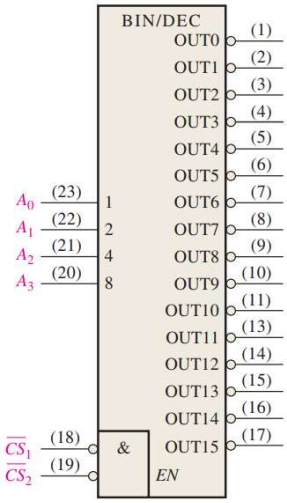
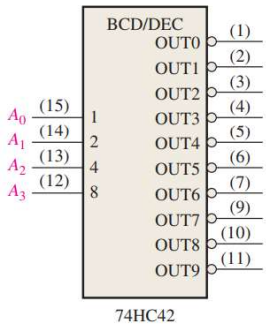
74HC283 (Full Adder - 4bit)



74HC154 (4-to-16 line decoder - active low)

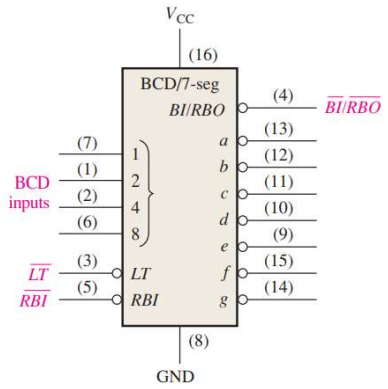


74HC42 (Active low - BCD to DEC decoder)

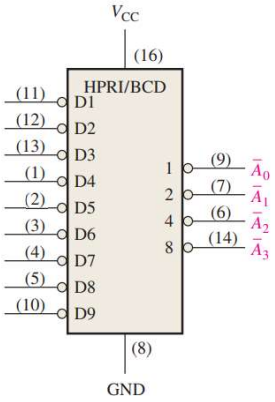


74HC42

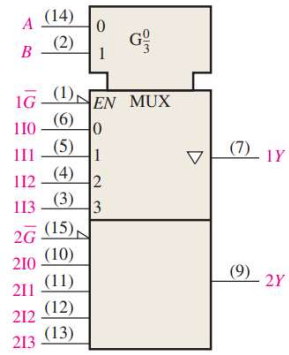
74HC47 (Active low - BCD to 7 seg decoder)



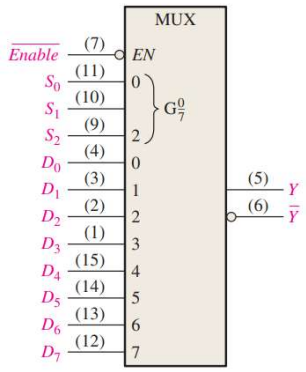
74HC147 (priority encoder)



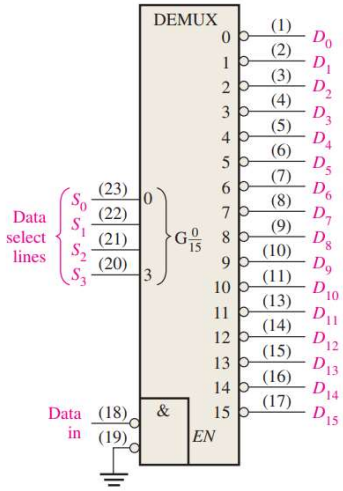
74HC153 (4 input MUX)



74HC151 (8 input MUX)

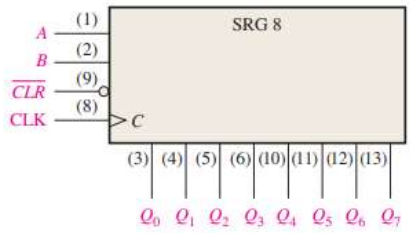


IC ??? (4-to-16 line DEMUX- active low)
(4 mar vali IC)



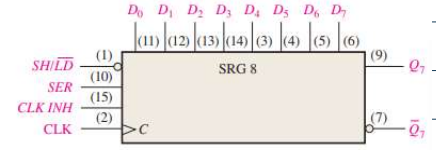
input data is also active low

74 HC 164 (Serial in/Parallel - 8 bits)



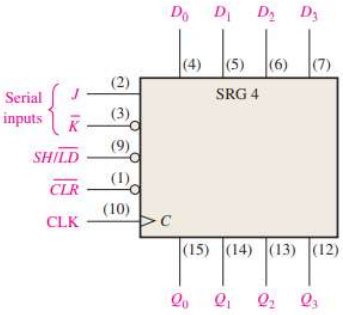
only input data 1 when A.B = 1

74HC 165 (Parallel in/Serial out - 8 bit)



SER is to load serial data
CLK INH inhibits data
SH/$\overline{LD}$ to shift and load

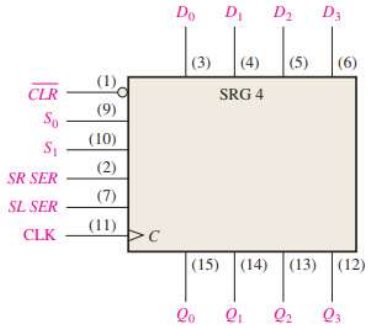
74HC195 (Parallel in/Parallel out - 4 bit)



don't forget $\overline{K}$!

es ist wirklich wichtig
denn ich habe es auch einmal vergessen! ^^

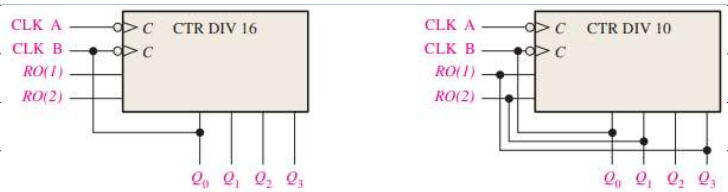
74HC194 (Pin/Pout - bi-directional - 4bit)



SR is Serial in RIGHT
SL " " " LEFT

S_1	S_0	Mode
0	0	Inhibit
0	1	SR active
1	0	SL active
1	1	Loading

74HC93 (Async counter - 4 bit)



(a) 74HC93 connected as a modulus-16 counter

(b) 74HC93 connected as a decade counter

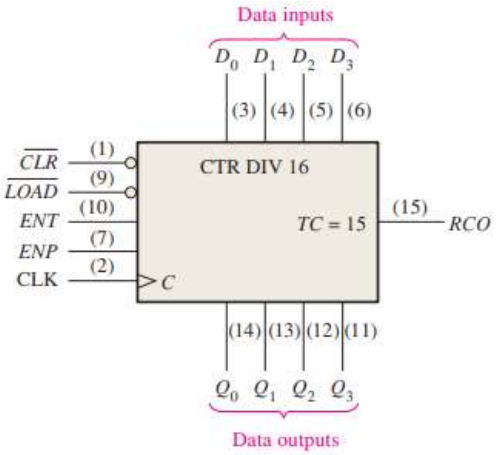
RO(1) and RO(2) act as CLR only when RO(1) · RO(2) = 1

This is a 1 + 3 bit counter.
Q_0 is the output of the 1 bit (divide-by-2) counter.
rest are for the 3 bit

CLKA is for the 1 bit
CLKB is for the 3 bit

By connecting Q_0 to CLKB, we extend the counter.

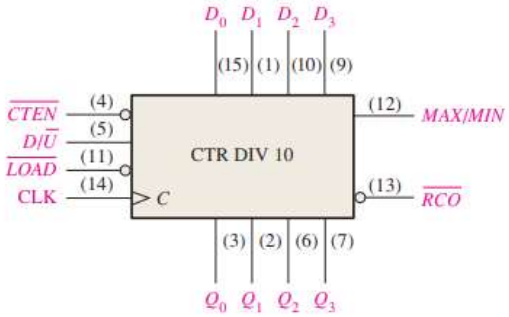
74HC163 (Sync - 4bit)



Counter enables only when ENT. ENP = 1 otherwise inhibits.

RCO gives high when $Q_0 \cdot Q_1 \cdot Q_2 \cdot Q_3 = 1$ (when 15)

74HC190 (up/down - 10 modulus)



$D/\bar{U}$ for down/up mode
$\overline{CTEN}$ for enable (active low)

MAX/MIN gives 1 when

$Q_3Q_2Q_0Q_1 + \overline{Q_3}\,\overline{Q_2}\,\overline{Q_1}\,\overline{Q_0} = 1$
(when 0 or 15)