National University of Computer and Emerging Sciences

Karachi Campus

Digital Logic Design

(EE1005)

Date: May 27th , 2024

Course Instructor(s)

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Final Exam

Total Time (Hrs):	3
Total Marks:	50
Total Questions:	6

Roll No Section Student Signature

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Attempt all the questions.

CLO # 1 Understand the knowledge of number systems and their operations [5 marks]

Q1: Perform the following operations.

a) Subtract the 8-bit signed number (-33) from (+33) using 2's complement. [2 marks]

b) Convert the decimal nos. into BCD code and then add 299 + 167 [2 marks]

c) Convert the octal number 1027 into its equivalent hexadecimal number [1marks]

CLO # 2 Techniques to design logic circuits. [10 marks]

Q2: a) Implement the following Boolean function f, using the two-level forms. [4 marks]

(i) NAND-NOR → NAND NAND (ii) NOR-NAND → NOR NOR

$F(A,B,C,D)=\sum(m(1,4,5,9,12) + d(0,2,3,6,14))$ (Hint: d represent don't care)

b) Simplify the output expression of the Fig-1. Modify the input conditions needed to cause the output to go to active low state. [3 marks]

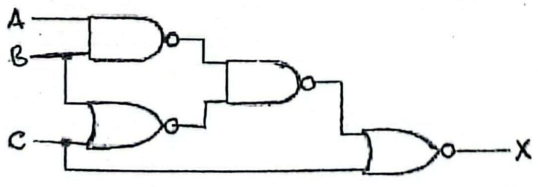


Fig-1

c) A BCD-to-seven segment decoder, is a combinational logic circuit that converts a coded decimal number to a suitable code for the input of a seven segment display. The decoder has four inputs (A, B,

C, D) and seven outputs (a, b, c, d, e, f, g). The seven segment display consists of seven LEDs (Light Emitting Diode), each of which is called a segment, to display the decimal numbers. When an output of the decoder becomes a logical 1, the corresponding LED lights. For the output **a**, obtain the simplified Boolean functions using Karnaugh map. [3 marks]

CLO # 3 Analyze small –scale combinational digital circuits. [10 marks]

Q3. a) In the given Fig-2, 8-bit parallel adder is formed by cascading the two 4-bit parallel adders. The carry input of the low-order adder (C0) is connected to ground because there is no carry into the least significant bit position, and the carry output of the low-order adder is connected to the carry input of the high order adder. Find the output of the adder (∑1 to ∑8 and C8) when two 8-bit numbers A & B are applied on this 8-bit parallel adder. [3 marks]

Input A = $A_8\ A_7\ A_6\ A_5\ A_4\ A_3\ A_2\ A_1$ = 1 0 1 0 1 1 0 1
Input B = $B_8\ B_7\ B_6\ B_5\ B_4\ B_3\ B_2\ B_1$ = 0 1 1 1 1 0 0 1

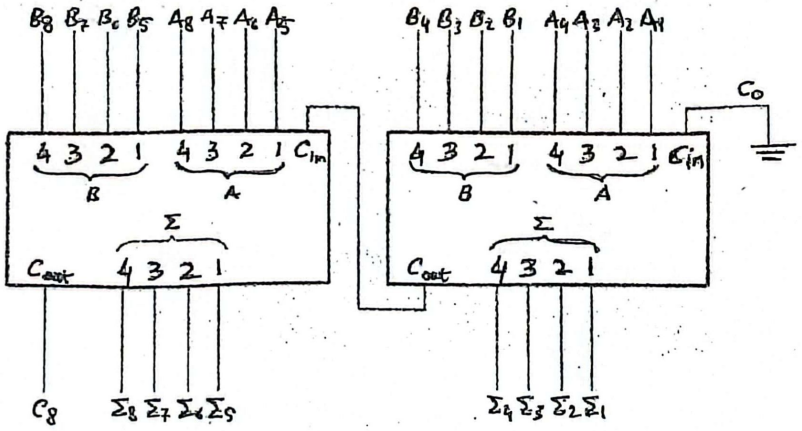


Fig-2

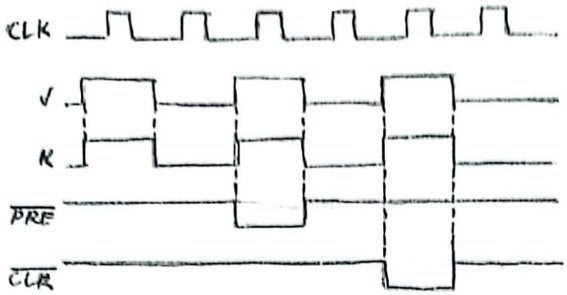
b) Use a 4-to-16 bit Decoder and basic logic gates to implement the following function F of Q2(a).
F(A,B,C,D)=∑(m(1,4,5,9,12) + d(0,2,3,6,14)) (Hint: d represent don't care) [1 marks]

c) Use a (8x1) multiplexer to implement the function: **F(A,B,C,D)=∑(m(2,5,6,7, 9,12, 13).** [3 marks]

d) Design a comparator circuit which has its outputs operated through a 8x1 multiplexer . By using the select pins of the multiplexer, the user should be able to switch to observe any one of the outputs from the comparator. [3 marks]

CLO # 4 Analyze Sequential Circuits to utilize in different applications. [5 marks]

Q4: a) Determine the Q waveform relative to the clock if the signals shown in Fig-3 are applied to the inputs of the J-K flip-flop. Assume that Q is initially LOW. Assume PRE and CLR remain HIGH. [2 marks]



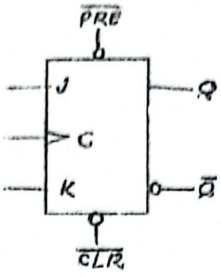


Fig-3

b) The Q output of an edge-triggered D flip-flop is shown in relation to the clock signal in Fig-4. Determine the input waveform on the D input that is required to produce this output if the flip-flop is a positive edge-triggered type. [1 marks]

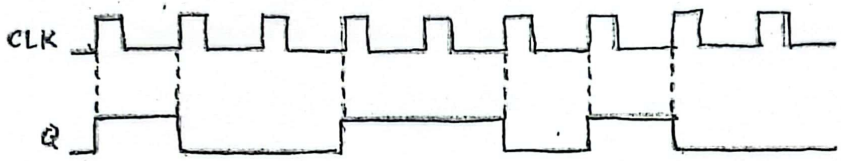


Fig-4

c) For the circuit in Fig-6, complete the timing diagram in Fig-5 by showing the Q output (which is initially LOW). Assume PRE and CLR remain HIGH. (Also determine waveform of J and K). [2 marks]

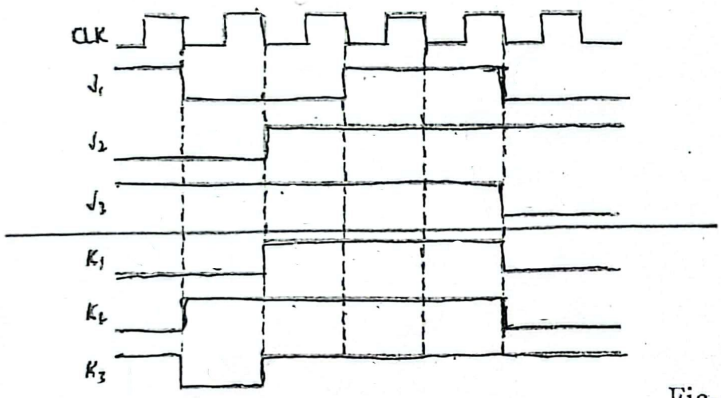


Fig-5

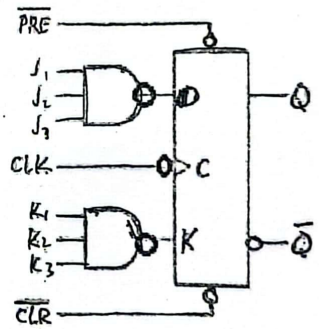


Fig-6

CLO # 4 Analyze Sequential Circuits to utilize in different applications. [12 marks]

Q5.a) Using D flip flop design a synchronous counter that counts the sequence **1-0-2-6-8-11-13-9**. [4 marks]

b) Design an Up/Down counter with the sequence **0-2-1-3** using a JK flip flop. [4 marks]

c) Determine the sequence of the counter in Fig-7. Also, implement the decoding of binary states 2 and 4 in the following 3-bit counter. [2 marks]

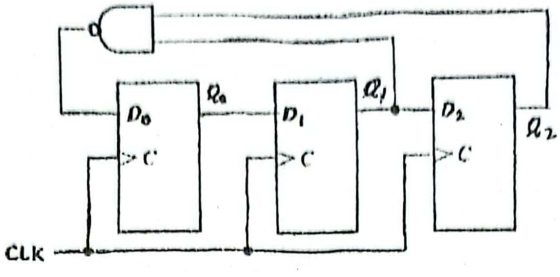


Fig-7

d) Design an asynchronous counter of modulus 13 using a J-K flip flop. The clock of J-K flip flop is negative edge triggered, CLR and PRE are active low. [2 marks]

CLO # 4 Analyze Sequential Circuits to utilize in different applications. [8 marks]

Q6: a) Consider a 4-bit serial in/serial out shift register. Draw the complete timing diagram showing the parallel outputs for the designed serial in/parallel out shift register. Assume that the registers are initially cleared (all 0s). (using data sequence 0011 and clock pulses 1 to 10). [3 marks]

b) Draw the logic diagram for a modulus-8 Johnson counter. Show the timing diagram and write the sequence in tabular form.(initially all cleared) [2 marks]

c) If a 5-bit ring counter has an initial state 11100, determine the waveform for each *Q* output. [1 marks]

d) Show the data-output waveform for a 4-bit register with parallel input data (1010) and CLK and SHIFT/LOAD waveforms given in Fig-8 . [2 marks]

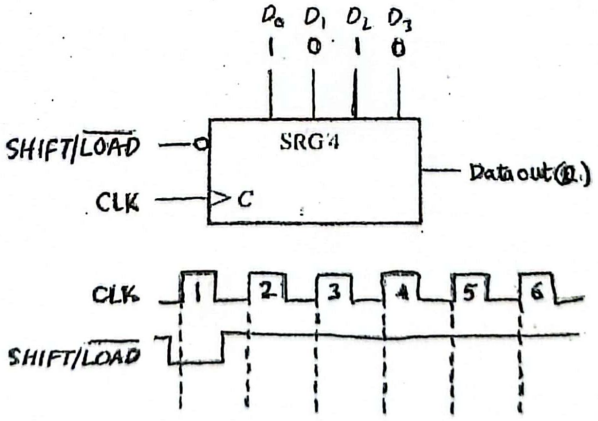


Fig-8