

Digital Logic Design

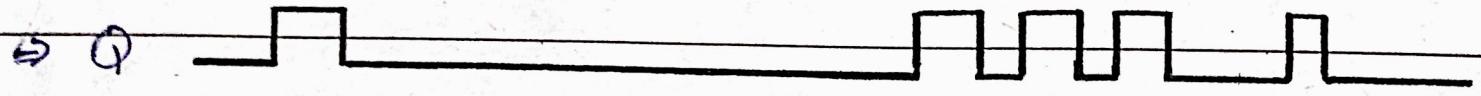
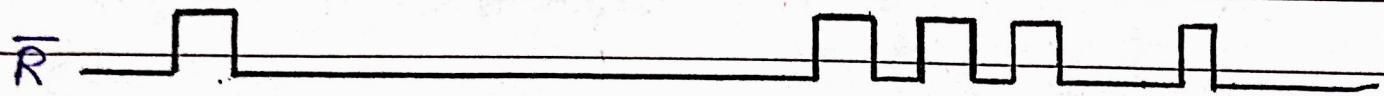
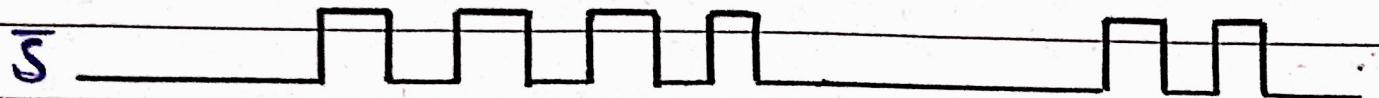
Assignment: 03

23K-2001

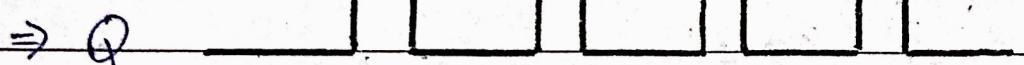
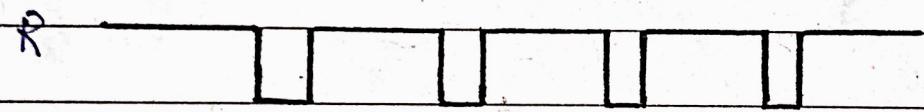
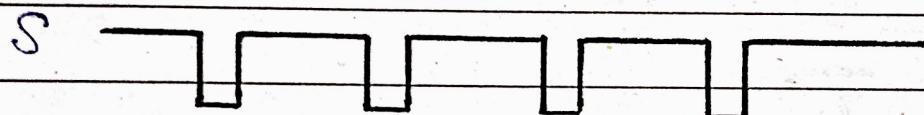
BCS-2J

Date: _____

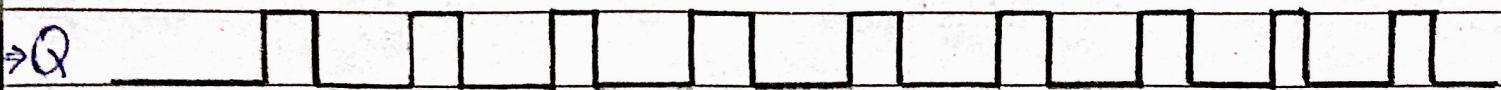
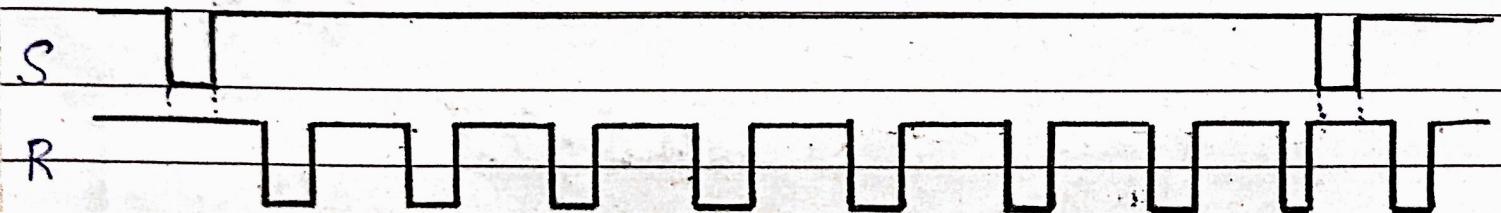
Answer #1: (Active low SR latch)



Answer #2: (Active High SR latch)

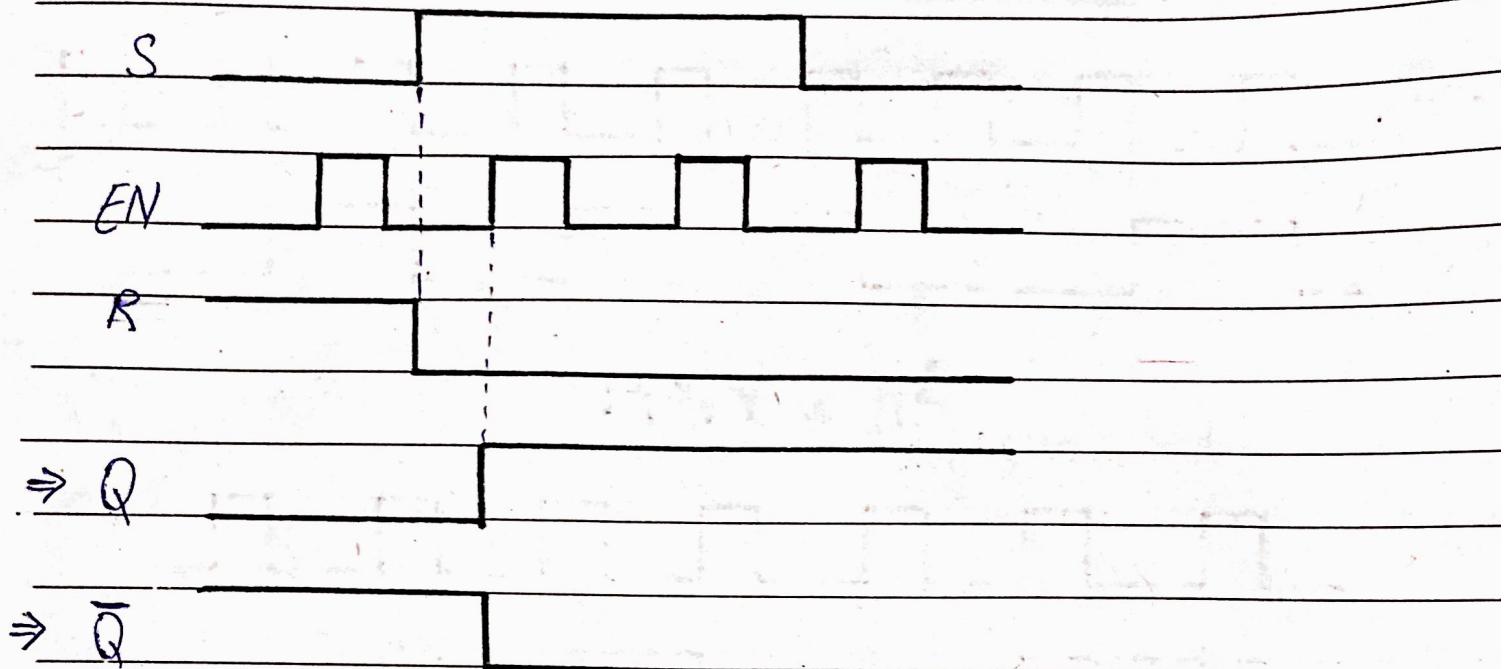


Answer #3: (Active High SR latch)

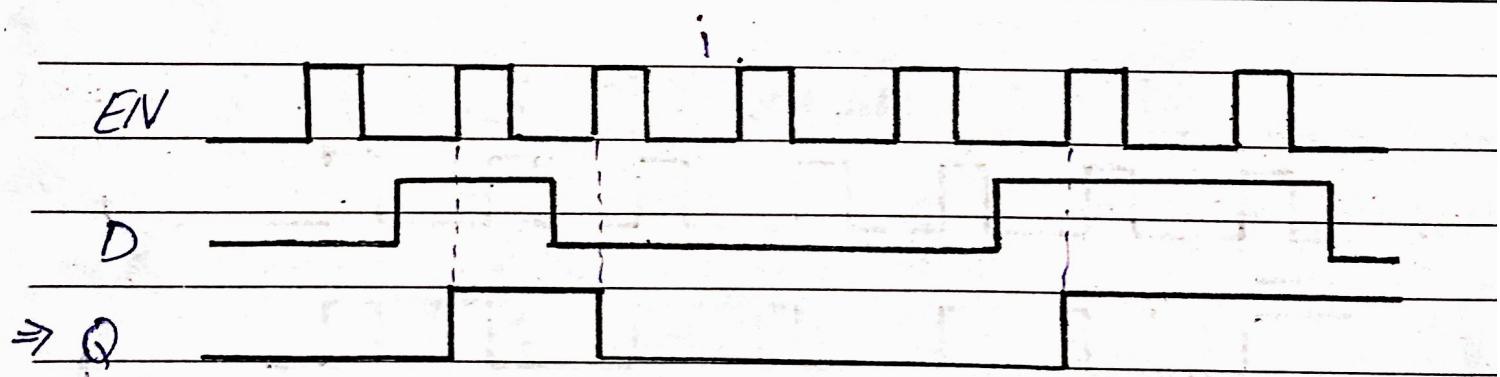


Date: _____

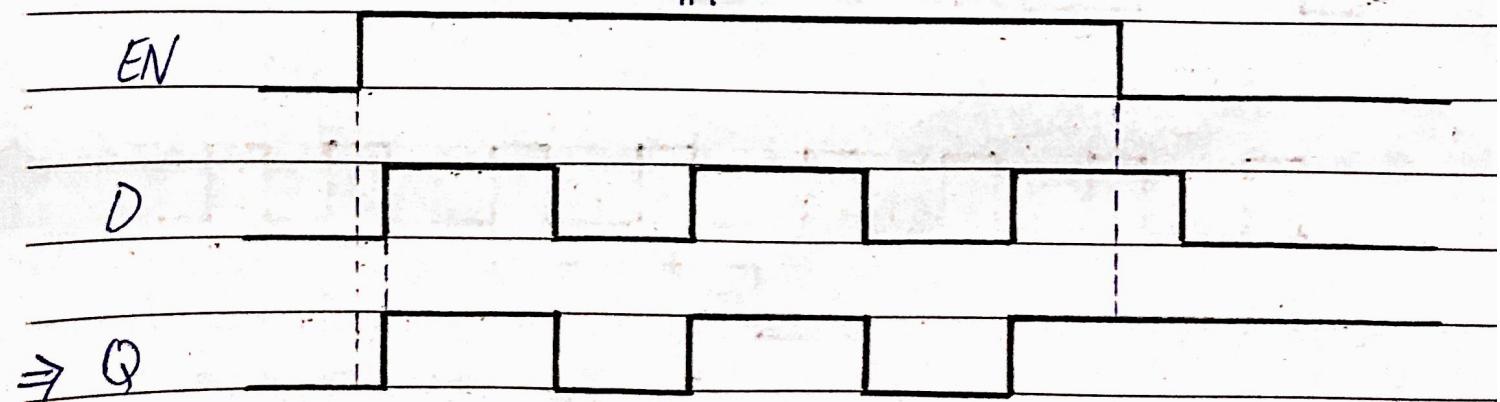
Answer #4: (Active High Gated SR latch)



Answer #5: (Gated D-latch)



ii.



Date: _____

Answer #6: (Positive-edge D flipflop)

$\Rightarrow D$

$\Rightarrow \text{CLK}$

$\Rightarrow Q$

Answer #7: (Positive-edge D flipflop)

CLK

D

$\Rightarrow Q$

Answer #8: (Positive-edge D flipflop)

i.

CLK

D

$\Rightarrow Q$

ii.

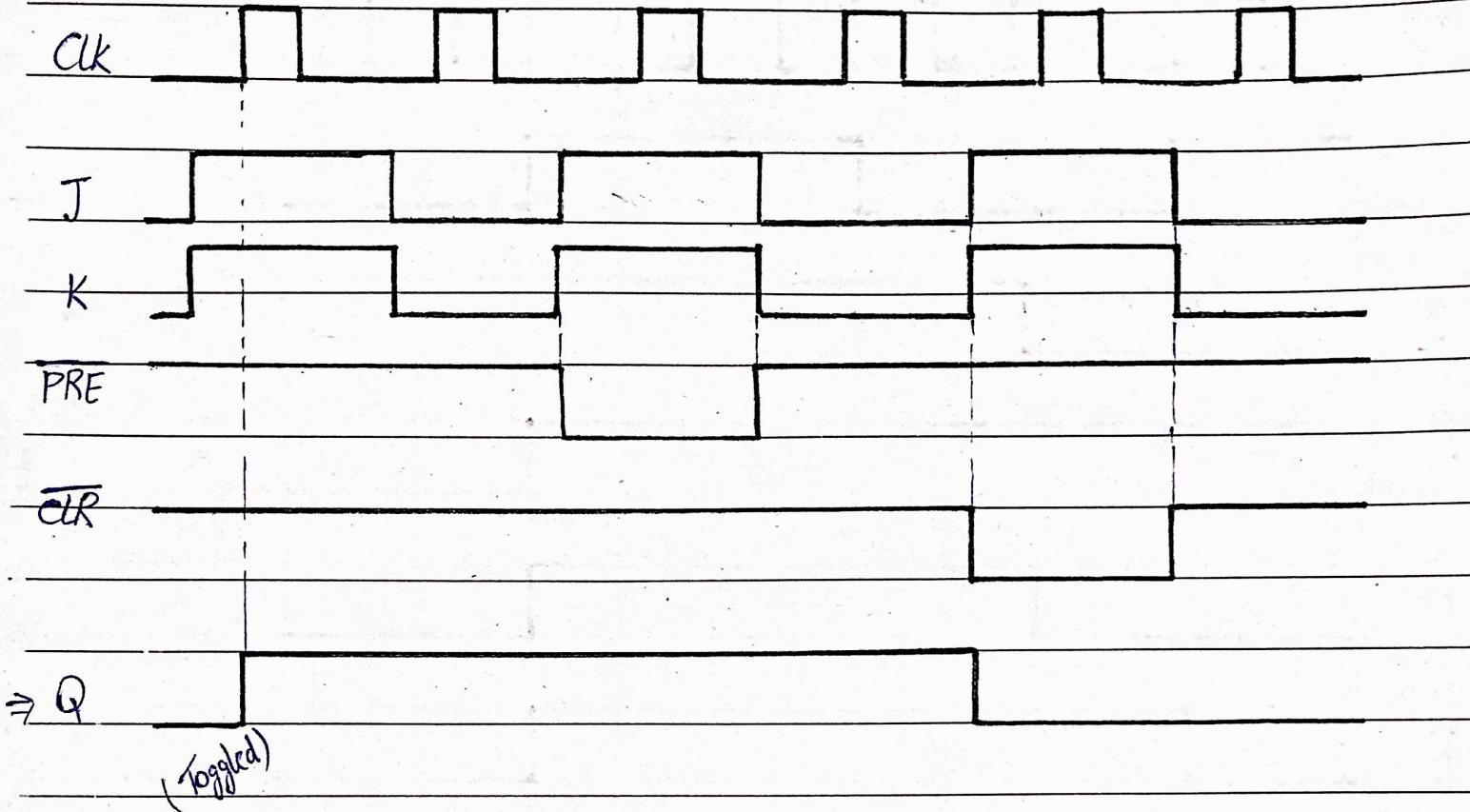
CLK

D

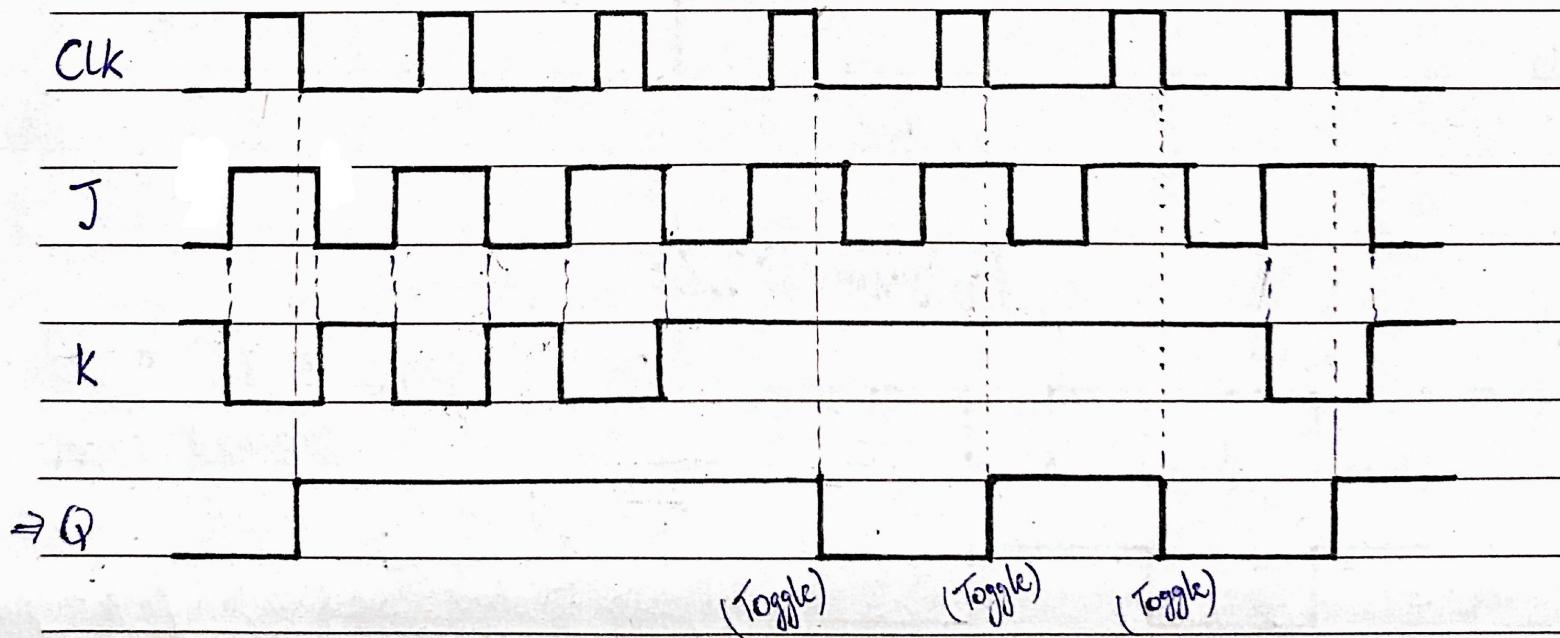
$\Rightarrow Q$

Date: _____

Answer #9: (JK Flip flop)

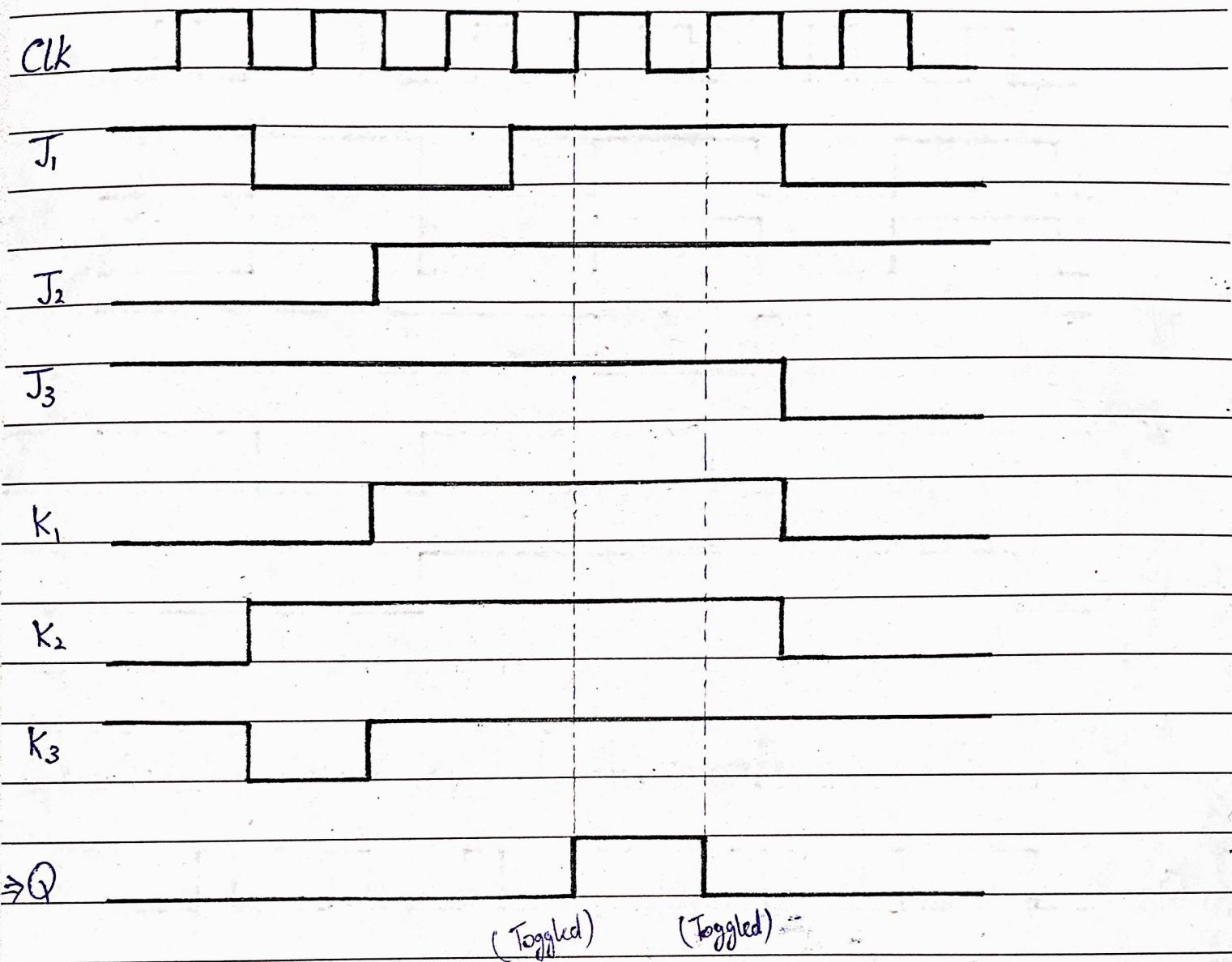


Answer #10: (Negative-edge JK flip flop)

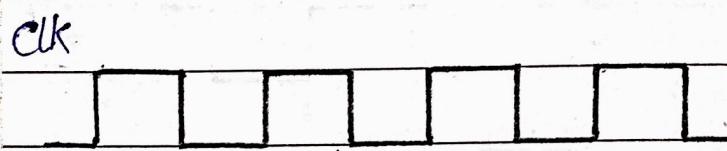


Date: _____

Answer#11: (Positive-edge JK flip flop)



Answer#12:



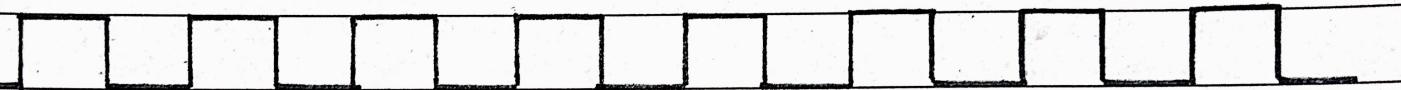
The flip flop circuit toggles at every positive edge, this kind of device can be used for reducing frequency of clock as \bar{Q} feeds back onto the data line D.

The output frequency is half of the original.

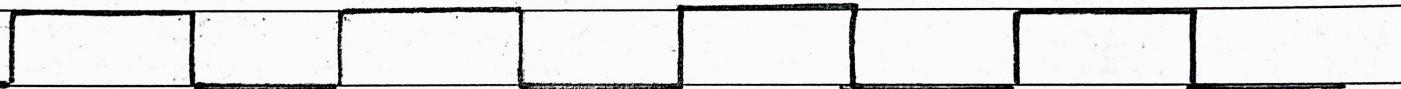
Date: _____

Answer #13:

CLK



QA



QA



QB



QB

