

Practice Problems Chapter - 8

1. Sequence : $\begin{matrix} 1 & 0 & 1 & 1 \\ D_0 & D_1 & D_2 & D_3 \end{matrix}$

After 3 clock pulses : $\begin{matrix} 0 & 1 & 1 & 0 \\ \uparrow & \uparrow & \uparrow & \uparrow \\ Q_0 & Q_1 & Q_2 & Q_3 \end{matrix}$

	Q_0	Q_1	Q_2	Q_3
Init :	0	0	0	0
CLK1:	1	0	0	0
CLK2:	1	1	0	0
CLK3:	0	1	1	0
CLK4:	1	0	1	1

Date: [M T W T F S S]

Q₀



Q₉



2. Initial State: 0101001111

CLK 1 2 3 4 5 6 7 8 9

Q₀ 0 1 1 1 1 0 0 1 0 1

Q₁ 1 0 1 1 1 1 0 0 1 0

Q₂ 0 1 0 1 1 1 1 0 0 1

Q₃ 1 0 1 0 1 1 1 1 0 0

Q₄ 0 1 0 1 0 1 1 1 1 0

Q₅ 0 0 1 0 1 0 1 1 1 1

Q₆ 1 0 0 1 0 1 0 1 1 1

Q₇ 1 1 0 0 1 0 1 0 1 1

Q₈ 1 1 1 0 0 1 0 1 0 1

Q₉ 1 1 1 1 0 0 1 0 1 0

3. 8-bit Johnson counter

$$2(8) = 16 \text{ states}$$

Q7

Initial State: 101001111000

Initial State Column

Date: _____
MTWTFSS



Q_0	1	0	0	0	0	1	1	1	0	0	0	1	1
Q_1	0	1	0	0	0	0	1	1	1	0	0	0	1
Q_2	1	0	1	0	0	0	0	1	1	1	0	0	0
Q_3	0	1	0	1	0	0	0	0	1	1	1	0	0
Q_4	0	0	1	0	1	0	0	0	0	1	1	1	0
Q_5	1	0	0	1	0	1	0	0	0	0	1	1	1
Q_6	1	1	0	0	1	0	1	0	0	0	0	1	1
Q_7	1	1	1	1	0	0	1	0	1	0	0	0	1
Q_8	1	1	1	1	1	0	0	1	0	1	0	0	0
Q_9	0	1	1	1	1	0	0	1	0	1	0	0	0
Q_{10}	0	0	1	1	1	1	0	0	1	0	1	0	0
Q_{11}	0	0	0	1	1	1	1	0	0	1	0	1	0

Initial State: 1010011110000

After:

CLK1: 010100111100

CLK2: 001010011110

CLK3: 000101001111

CLK4: 000010100111

CLK5: 100001010011

" 6: 110000101001

" 7: 111000010100

" 8: 011100001010

" 9: 001110000101

" 10: 000111000010

" 11: 100011100001

" 12: 110001110000

Date:

MTWTFSS

Q13.

CLK | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |

A | 1 1 | 0 0 | 1 1 | 1 1 | 0 0 |

B | 0 0 | 1 1 | 1 0 0 0 | 1 1 |

CLR | | | | | | | | |

Q₀ | | | | | | | | |

Q₁ | | | | | | | | |

Q₂ | | | | | | | | |

Q₃ | | | | | | | | |

Q₄ | | | | | | | | |

Q₅ | | | | | | | | |

Q₆ | | | | | | | | |

Q₇ | | | | | | | | |

Clear

Clear

LOW

LOW

LOW

LOW

LOW

Dairy

MITWTFSS

10

CLK	1	2	3	4	5	6
-----	---	---	---	---	---	---

SHIFT
LOAD

D₀ ————— HIGH

D₁ | | | | | low

D₃ 4164

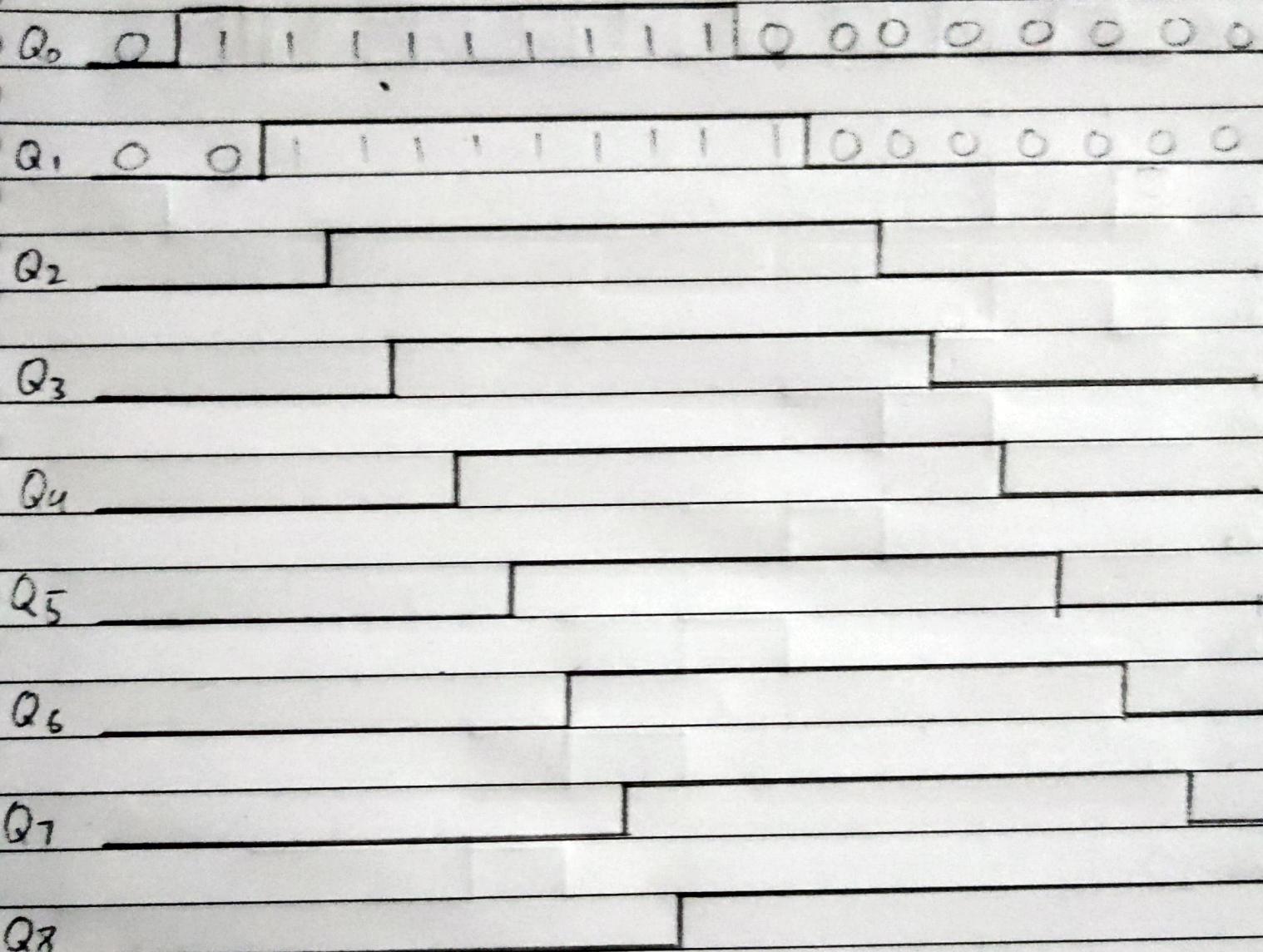
D₃ | | | | Low

The diagram illustrates the timing sequence for a 3-to-8 decoder. The top row shows the **Data in** signal with binary values 0, 1, 0, 0, 0, 1, 0. The bottom row shows the **Data out** signal with binary values 1, 0, 1, 0, 1, 0, 1. Below the inputs, arrows indicate transitions: D_3 goes high at the first bit, D_2 goes high at the second bit, D_1 goes low at the third bit, and D_3 goes high again at the fifth bit. The output bits Y_0 through Y_7 are shown as vertical lines, with horizontal arrows indicating their active states corresponding to the input transitions.

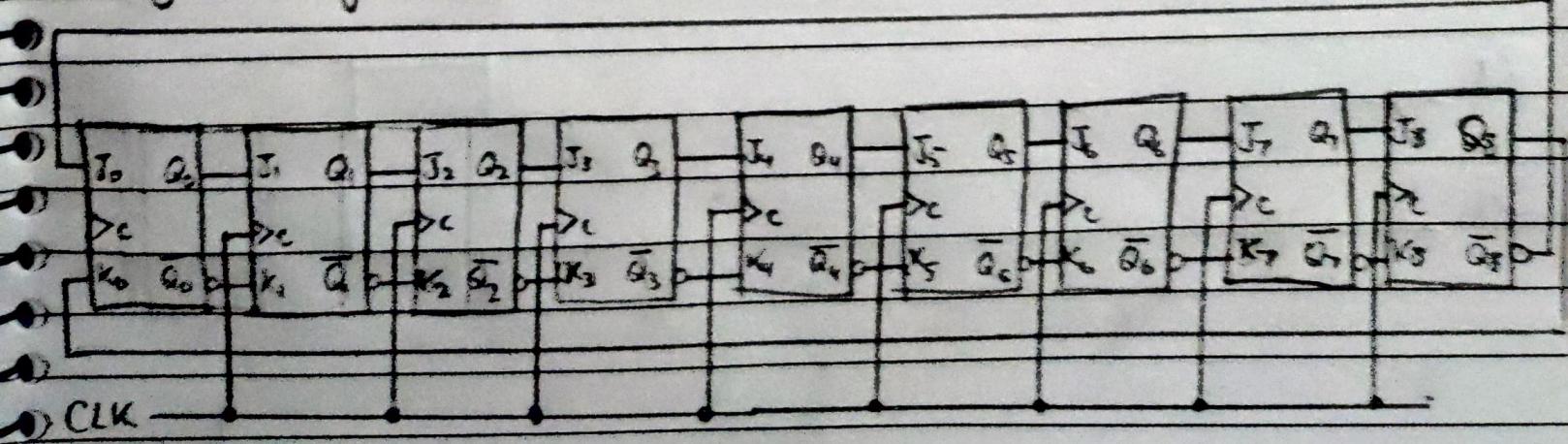
Q26;

MOD - 18 Johnson counter \Rightarrow 9 Flip Flops to be used (18 states).

TIMING DIAGRAM:



→ logic Diagram:



Date:

M T W T F S S

Q271

CLK

