National University of Computer & Emerging Sciences, Karachi
Spring -2022 CS-Department
13th June , 2022
Final Exam

Course Code: EE1005	Course Name: Digital Logic Design (DLD)
Instructor Name / Names: Mr. Aamir , Mr Aashir , Mr. Behraj , Mr. Hamza, Ms. Rabia Tabassum, Ms. Rukhsar , Ms. Sumaiyah , Mr. Zakir	
Student Roll No:	Section No:

Instructions:.

- All the answers must be solved according to the sequence given in the question paper.
- The paper consists of 4 questions on 2 pages. This paper is subjective.

Time: 120 minutes. **Max Marks:** 50 points

Question 1: (CLO-1) [5 Points]

(a) Determine the decimal value of signed binary number in the 1's complement form: [2.5]

10111000

-128 64 32 16 8 4 2 1
10111000
$-128+32+16+8=-72$ For 1's Comp. $-72+1=$ **-71**

(b) Add the following BCD numbers: **10010110 + 10011001** [2.5]

1001 0110
1001 1001
10010 1111
0110 0110
1 1001 0101

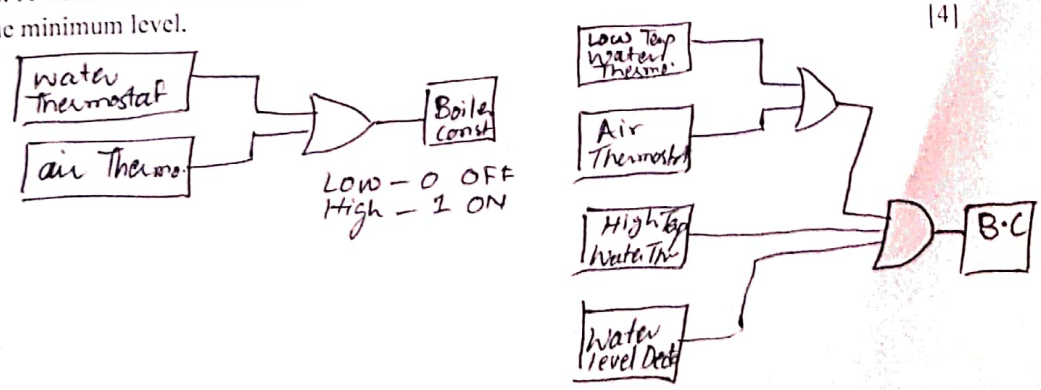
0001 1001 0101

Question 2: (CLO-2) [10 Points]

(a) For the waveforms given in Fig-1 , *A* and *B* are ORed with output *X*, *D* and *E* are ORed with output *Y*, and *C*, *X*, and *Y* are ANDed. Draw the net output waveform(1 tot 18). [2]

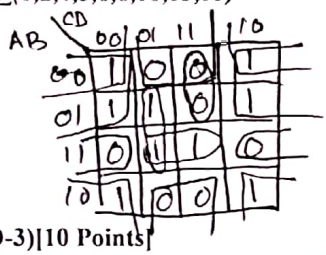
Fig-1

(b) Design a circuit using Logic gates for a hot-water space heating system. The boiler used for this system should turn 'ON' when the room temperature falls below a preset value. After drawing this circuit further modified it to include the following safety features: The boiler must switch 'OFF' if the water temperature exceeds a prescribed maximum. A second thermostat should cut off the heat when the required room temperature is reached. The system must also cutoff the heat when the quantity of water in the tank falls below a minimum level. A water level transducer must also be included, producing a HIGH output while the water remains above the minimum level. [4]



(c) Use Karnaugh map to simplify POS and SOP expressions for the Boolean function. [4]

$F(A,B,C,D) = \sum(0,2,4,5,6,8,10,13,15)$



$SOP = \bar{A}\bar{D} + \bar{B}\bar{D} + B\bar{C}D + AB\bar{D}$

$POS = (B + \bar{D})(A + \bar{C} + \bar{D})(\bar{A} + \bar{B} + D)$

Question 3: (CLO-3)[10 Points]

(a) BCD numbers are applied sequentially to the BCD-to-decimal decoder in Fig-2. Draw a timing diagram, showing each output in the proper relationship with the others and with the inputs. [2]

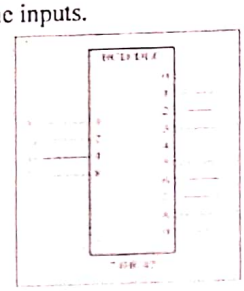
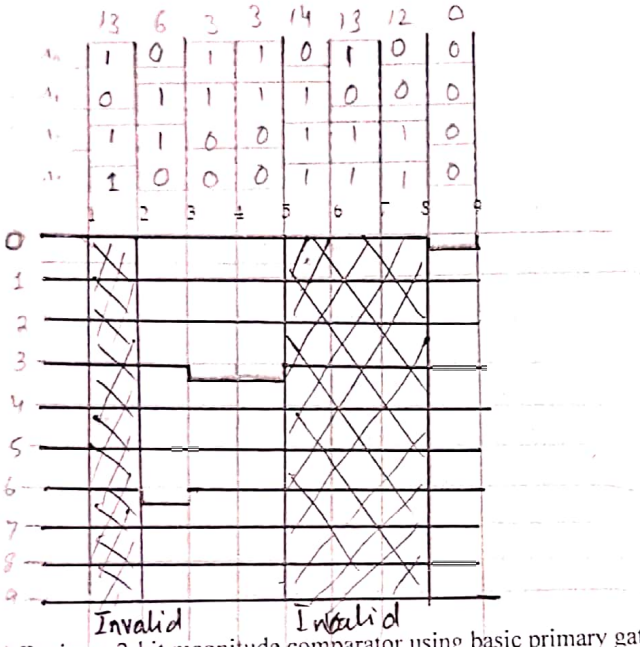
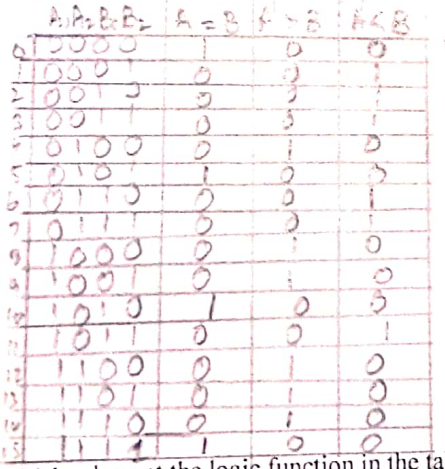
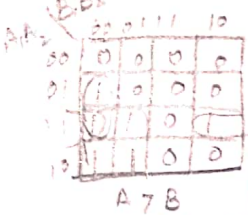


Fig-2



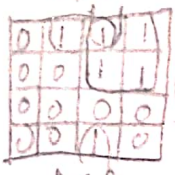
(b) Design a 2-bit magnitude comparator using basic primary gates. [2]





$A > B = A_1\bar{B}_1 + A_2\bar{B}_1\bar{B}_2 + A_1A_2\bar{B}_2$

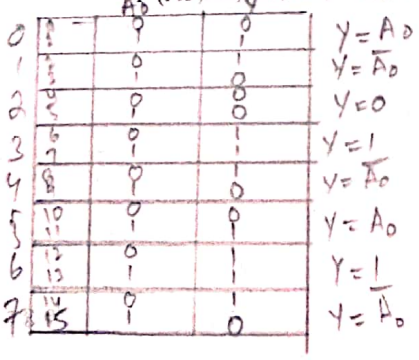
$A = B = (A_1 \oplus B_1)(A_0 \oplus B_0)$



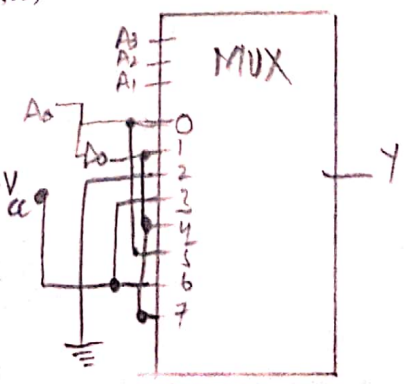
$A < B = \bar{A}_1B_1 + \bar{A}_1\bar{A}_2B_2 + \bar{A}_2B_1B_2$

(c) Implement the logic function in the table by using a (74S151) 8 input data selector/multiplexer. [2]

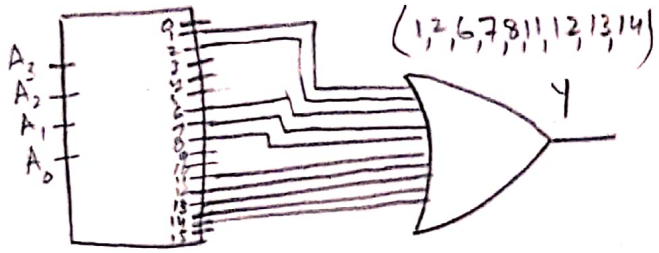
$F(A3,A2,A1,A0) = \prod(0,3,4,5,9,10,15)$



$Y = A_0$
$Y = \bar{A}_0$
$Y = 0$
$Y = 1$
$Y = \bar{A}_0$
$Y = A_0$
$Y = 1$
$Y = \bar{A}_0$



(d) Implement above function using 4 to 16 line decoder. [2]



(e) The input waveforms in Figure are applied to a 2-bit adder. Determine the waveforms for the sum and the output carry in relation to the inputs by constructing a timing diagram. [2]

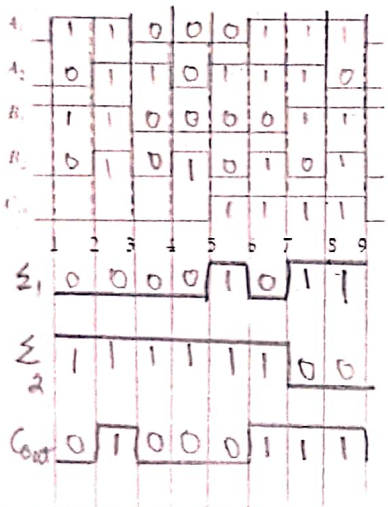
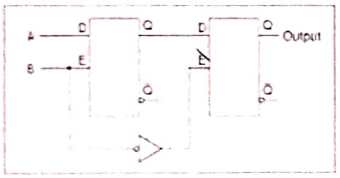


Fig-3

Question 4: (CLO-4) [25 Points]

(a) Determine the final output states over time for the following circuit (Fig-3), built from D-type gated latches: [2]



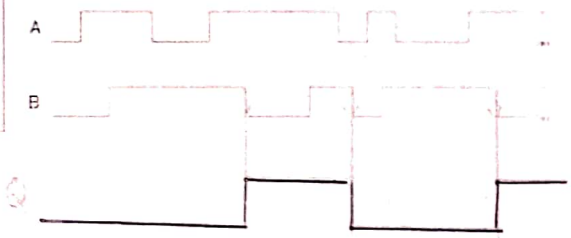


Fig-3

(b) Determine the sequence of the counter in Fig-4 [2]

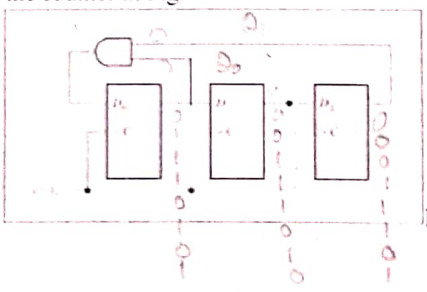
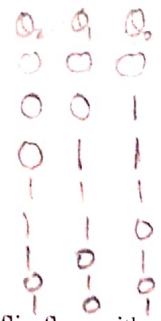


Fig-4



(c)Determine the output frequency for a frequency division circuit that contains 12 flip-flops with an input clock frequency of 20.48 MHz. [1]

$$f_{out} = f_{in} / 2^n$$

$$= 20.48 / 2^{12}$$

$$f_{out} = 5\ kHz$$

(d) For the circuit in Figure, develop a timing diagram for eight clock pulses, showing the Q_A and Q_B outputs in relation to the clock. [3]

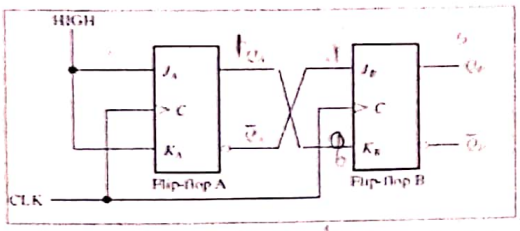
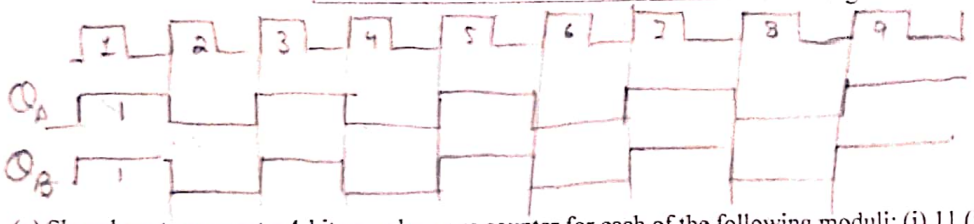
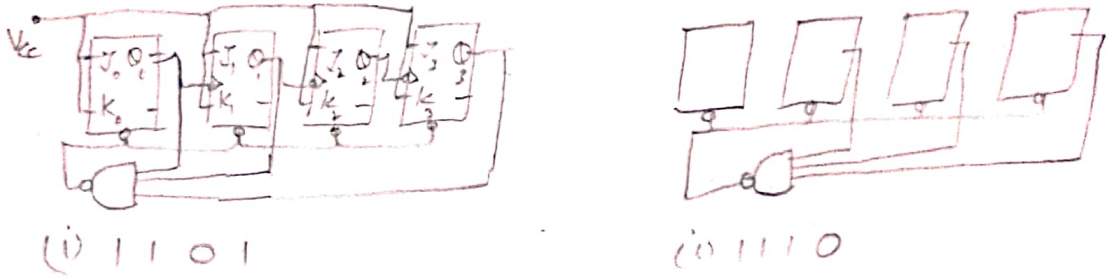


Fig-5



(e) Show how to connect a 4-bit asynchronous counter for each of the following moduli: (i) 11 (ii) 14 [3]



(f) If a 6-bit ring counter has an initial state 110001, determine the waveform for each Q output. [2]

Q_5	Q_4	Q_3	Q_2	Q_1	Q_0
1	1	0	0	0	1
1	0	0	0	1	1
0	0	0	1	1	1
0	0	1	1	1	0
0	1	1	1	0	0
1	1	1	0	0	0
1	1	0	0	0	1

(g)What is the state of the register in fig- after each clock pulse if it starts in the 101001100010 states? [3]

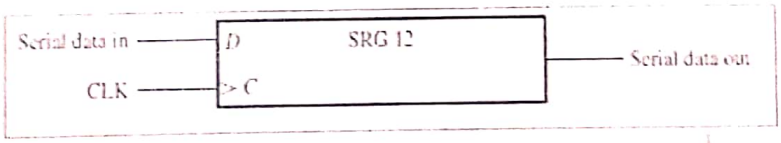


Fig-6

clk	1	2	3	4	5	6	7	8	9	10	11	12
Q_0	0	1	0	0	0	1	1	0	0	1	0	1
Q_1	0	0	1	0	0	0	1	1	0	0	1	0
Q_2	0	0	0	1	0	0	0	1	1	0	0	1
Q_3	0	0	0	0	1	0	0	0	1	1	0	0
Q_4	0	0	0	0	0	1	0	0	0	1	1	0
Q_5	0	0	0	0	0	0	1	0	0	0	1	1
Q_6	0	0	0	0	0	0	0	1	0	0	0	1
Q_7	0	0	0	0	0	0	0	0	1	0	0	0
Q_8	0	0	0	0	0	0	0	0	0	1	0	0
Q_9	0	0	0	0	0	0	0	0	0	0	1	0
Q_{10}	0	0	0	0	0	0	0	0	0	0	0	1
Q_{11}	0	0	0	0	0	0	0	0	0	0	0	0