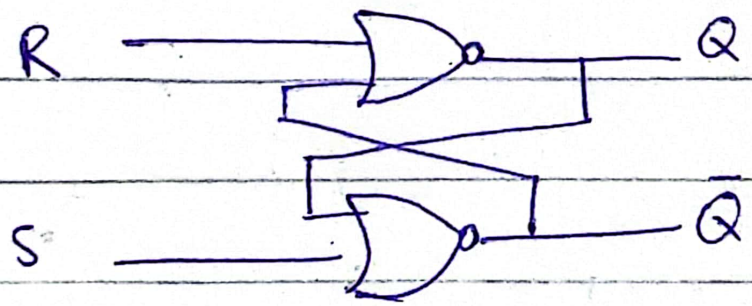
chap # 07

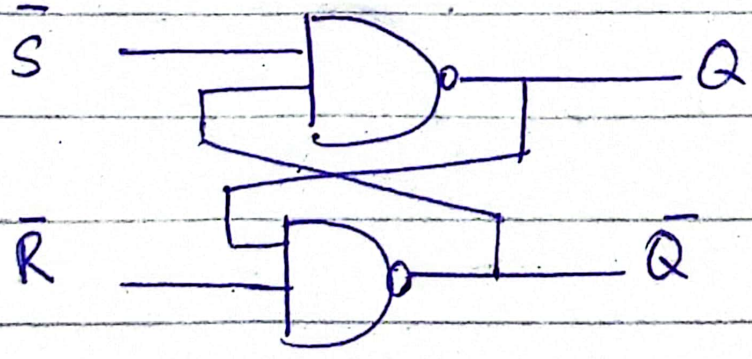
7-1 Latches

The S-R latch :



SET means Q=1

RESET means Q=0

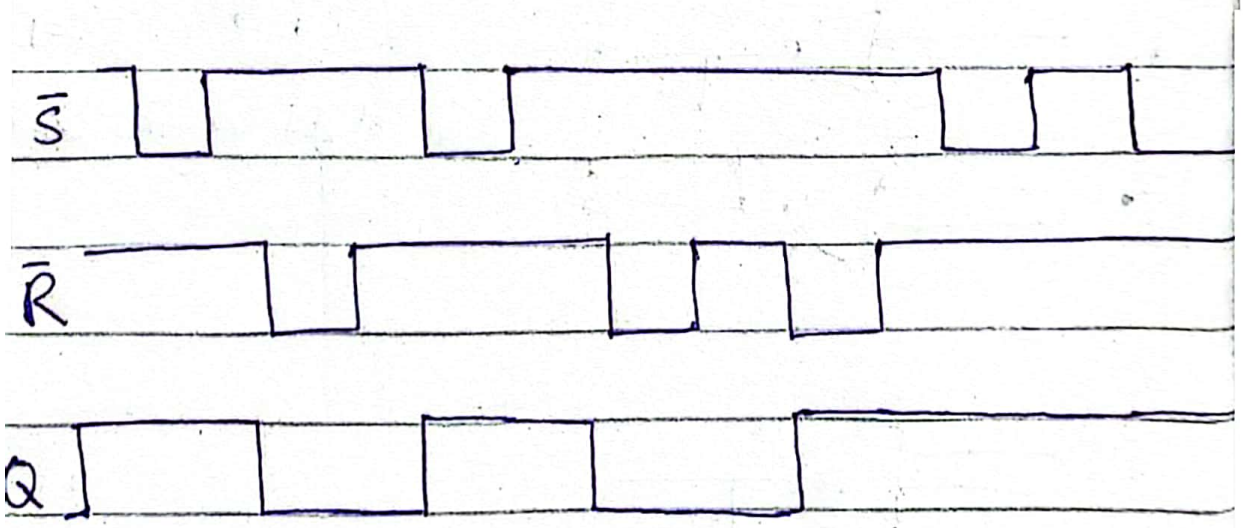


Truth Table

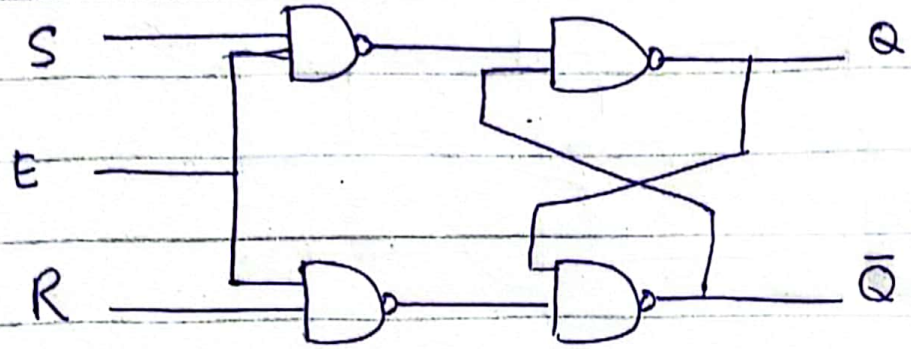
$\bar{S}$	$\bar{R}$	Q	$\bar{Q}$
0	0	invalid	
0	1	1	0
1	0	0	1
1	1	no change	

S	R	Q	$\bar{Q}$
0	0	no change	
0	1	0	1
1	0	1	0
1	1	invalid	

Example 7-1



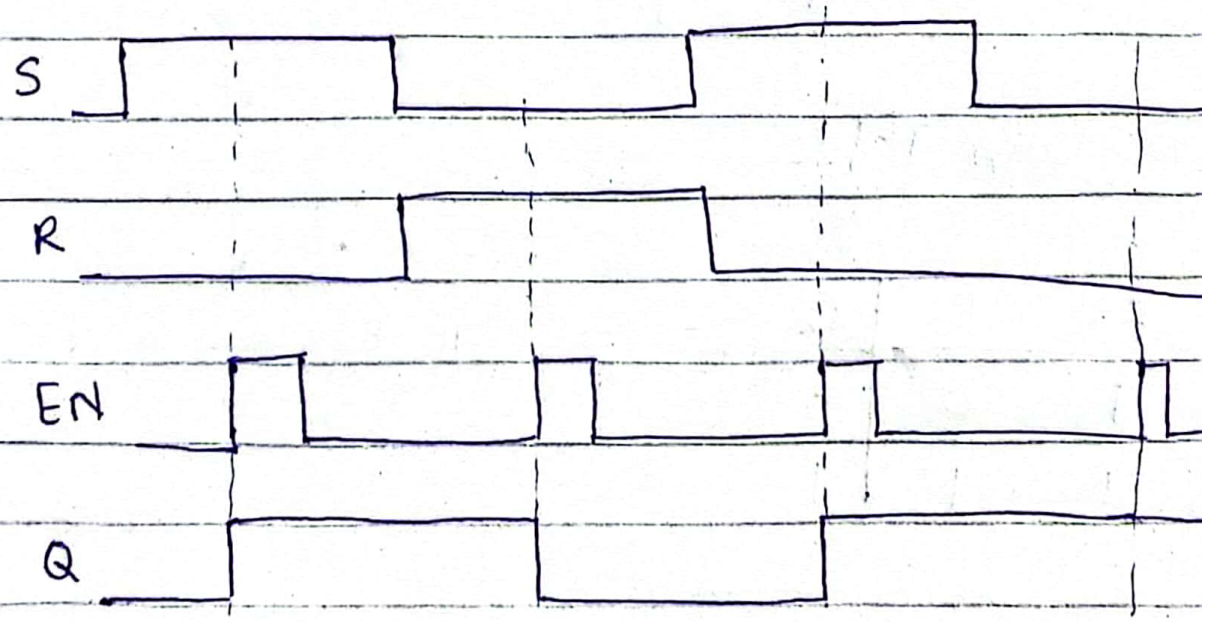
The Gated SR Latch



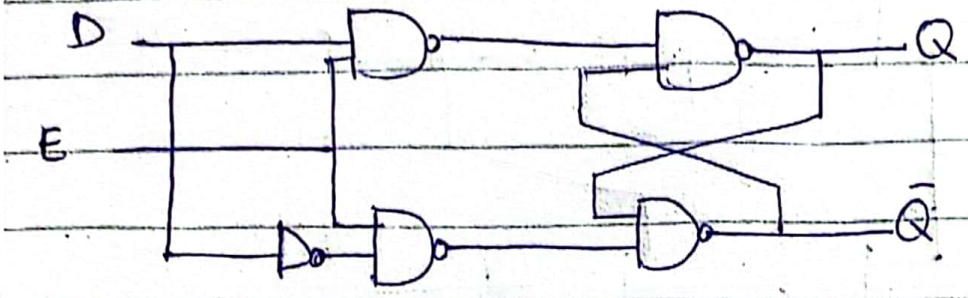
logic diagram

logic symbol

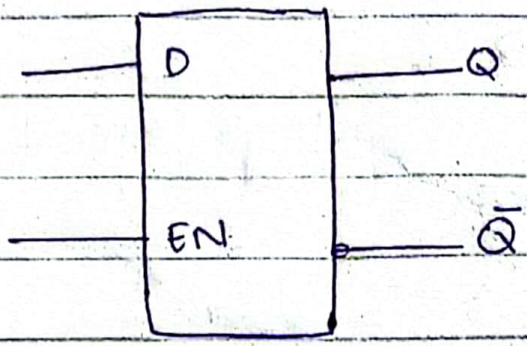
Example 7-2



The Gated D Latch



logic diagram

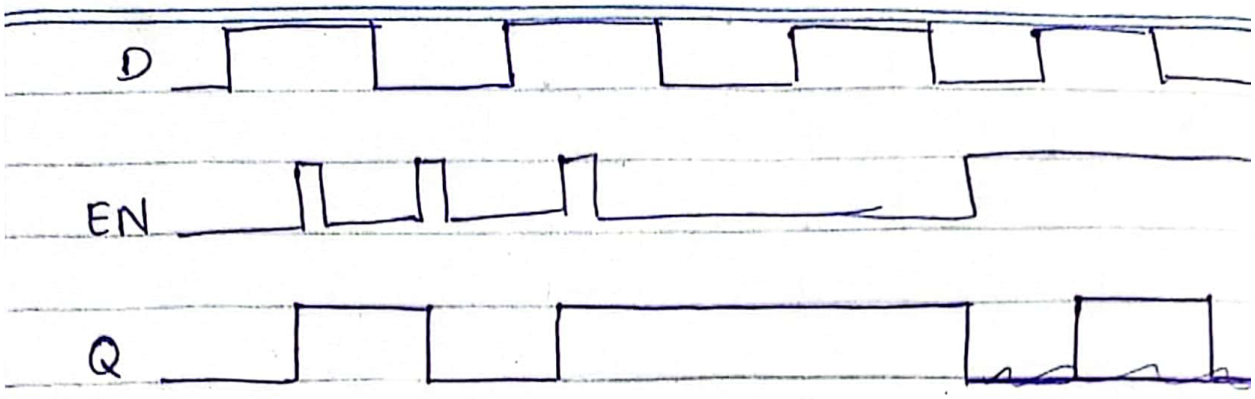


logic symbol

Truth Table

E	D	Q
1	0	0
1	1	1

if E = 0 → Q = previous output



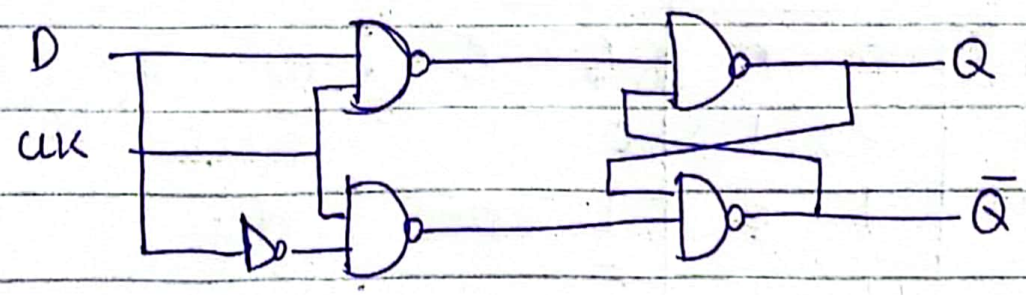
7-2 Flip Flops

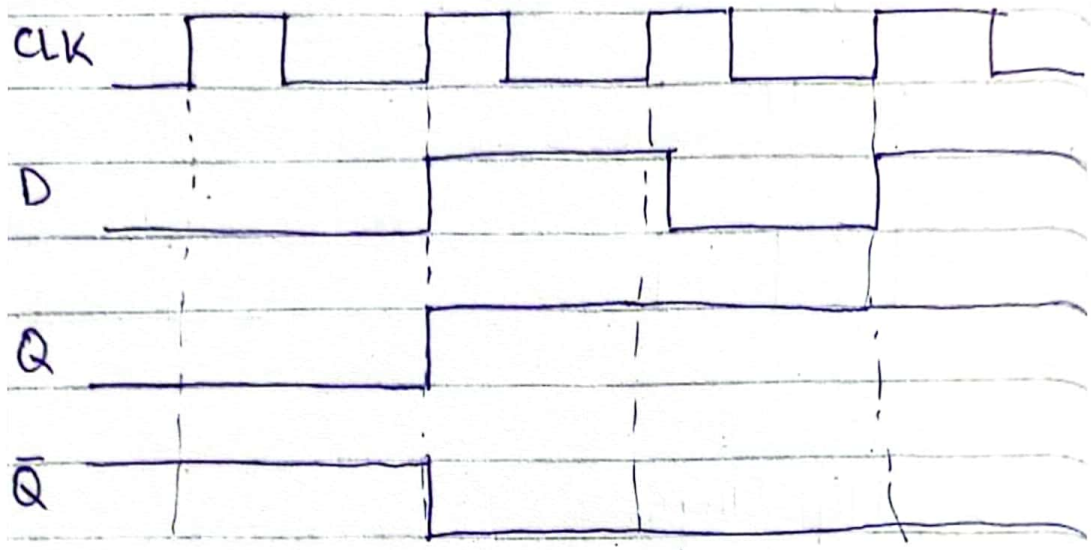
- edge triggered flip flop changes state either at the positive edge or at the negative edge.

The D flip flop

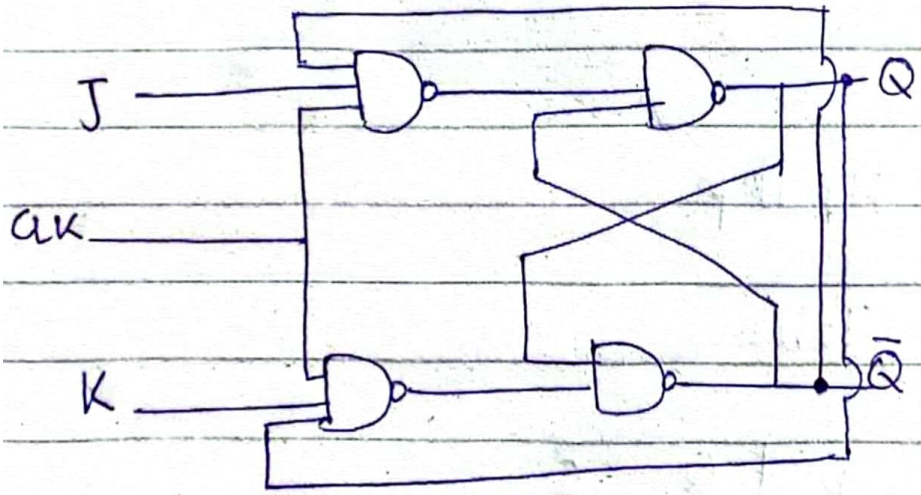
Truth Table.

CLK	D	Q	$\bar{Q}$	
↑	0	0	1	reset
↑	1	1	0	set



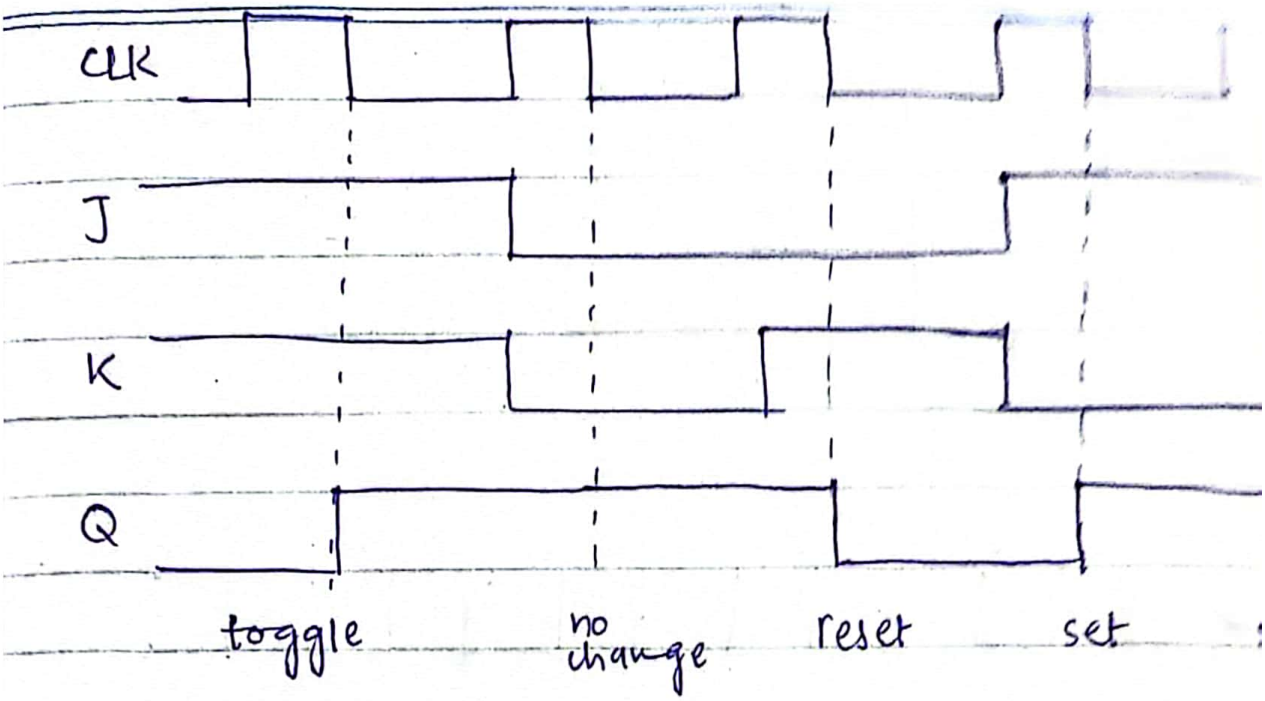


The JK Flip Flop

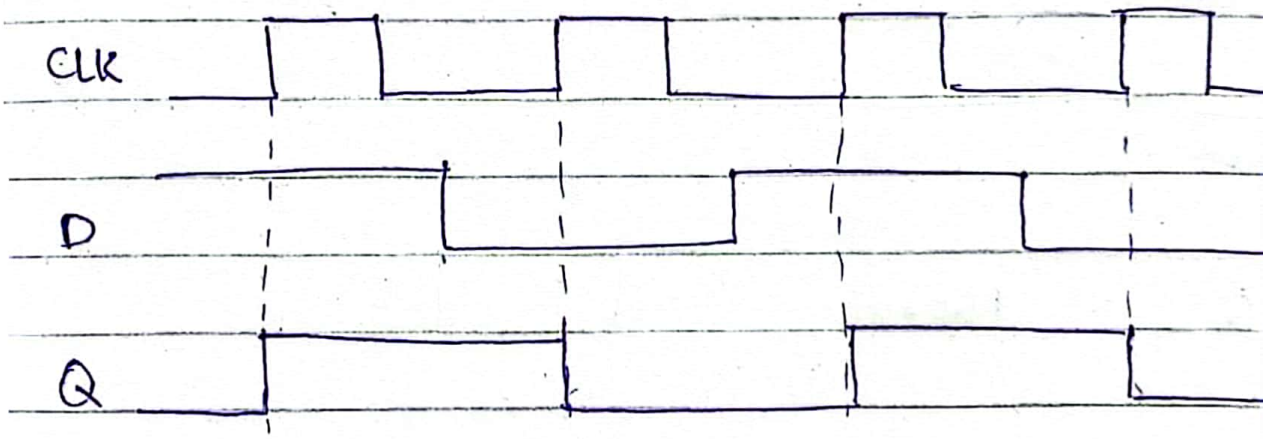


Truth Table

CLK	J	K	Q	$\bar{Q}$	
↑	0	0	Q	$\bar{Q}$	no change
↑	0	1	0	1	reset
↑	1	0	1	0	set
↑	1	1	$\bar{Q}$	Q	toggle

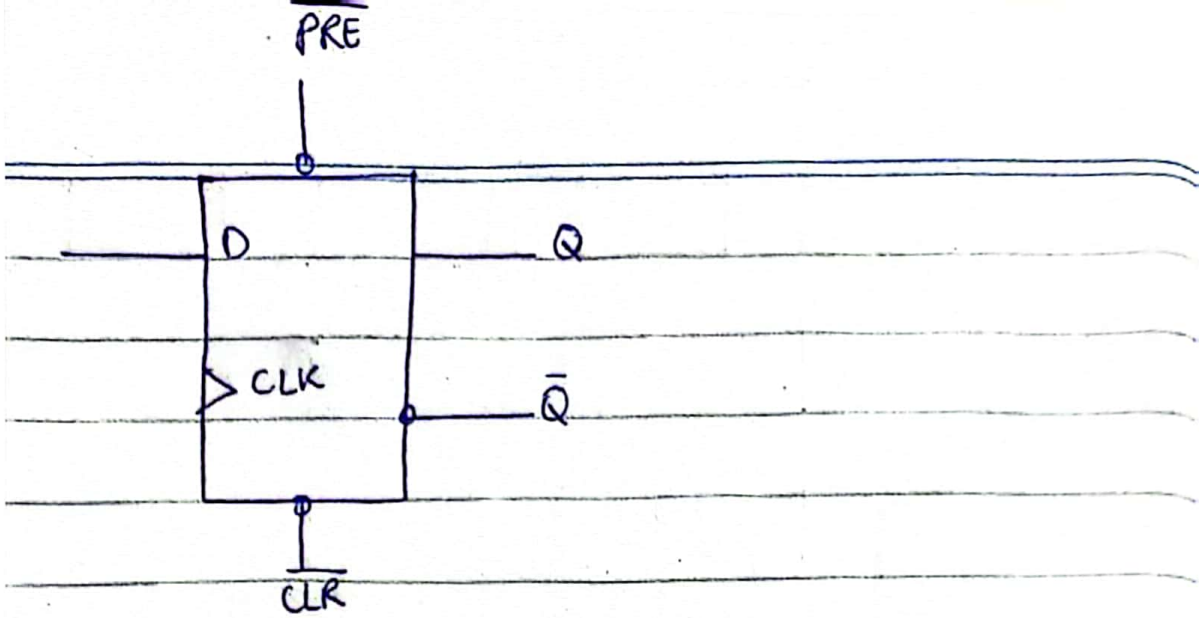


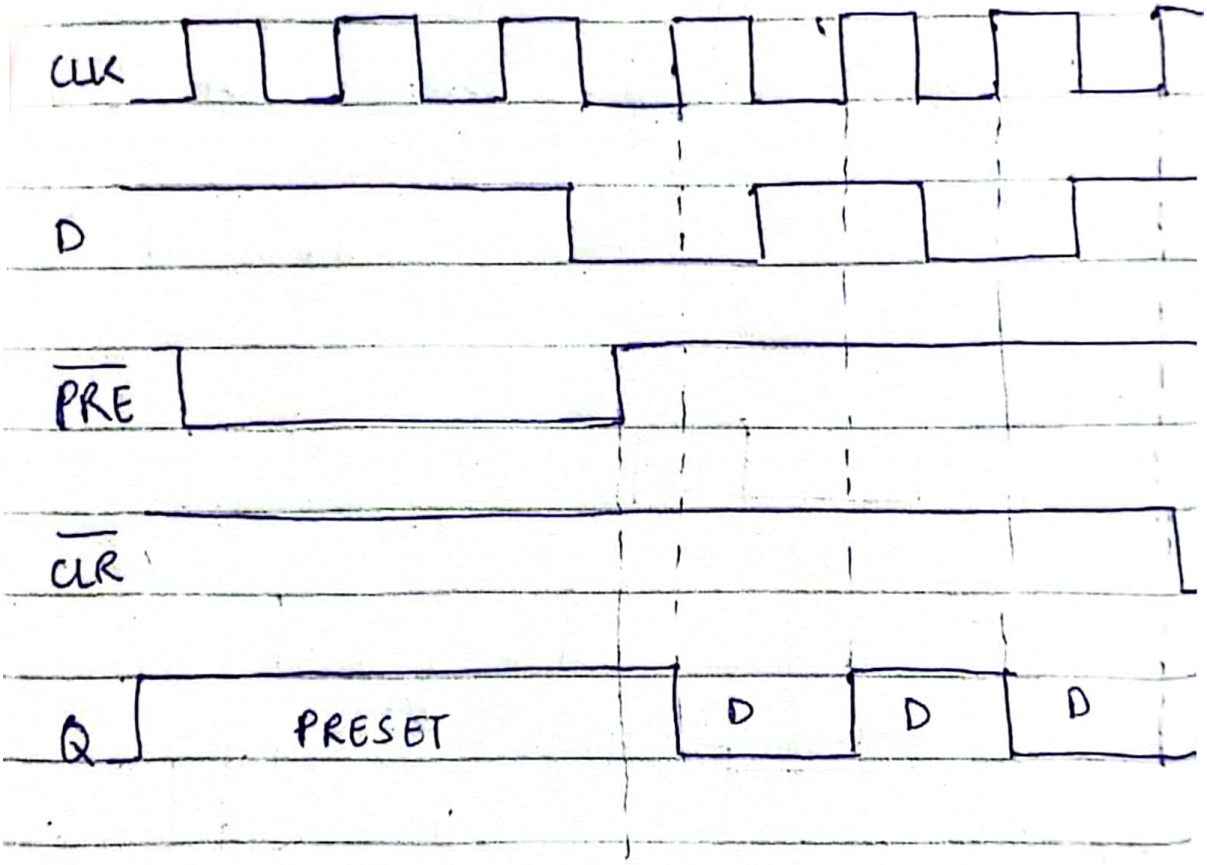
Example 7-6 :



Asynchronous Preset and Clear Inputs

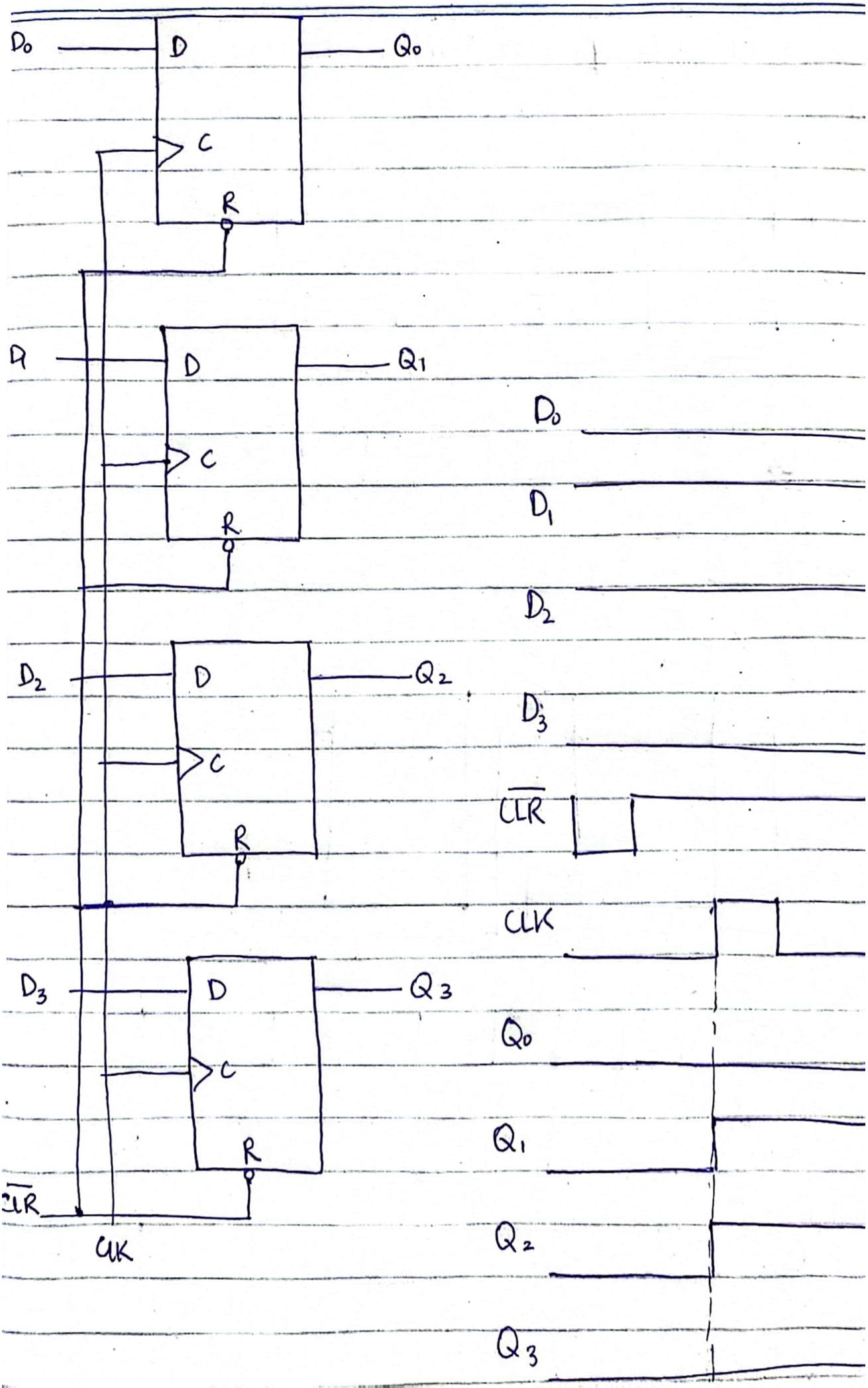
- an active preset input makes the Q output "HIGH" (set)
- an active clear input makes the Q output "LOW" (reset)



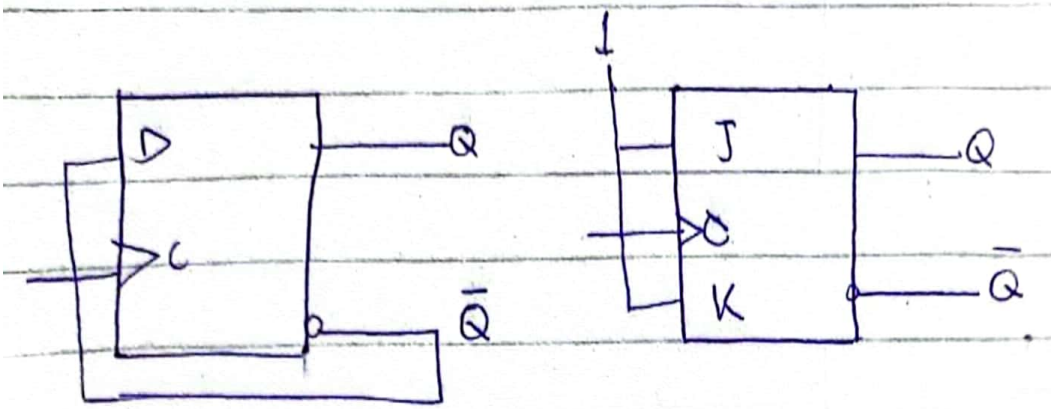


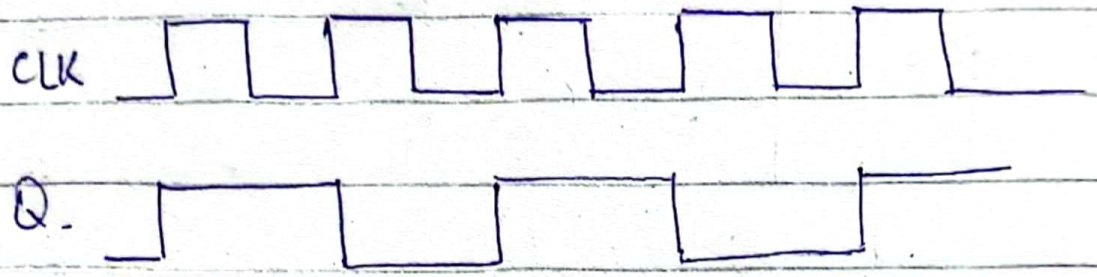
7-4 Flip Flop Applications

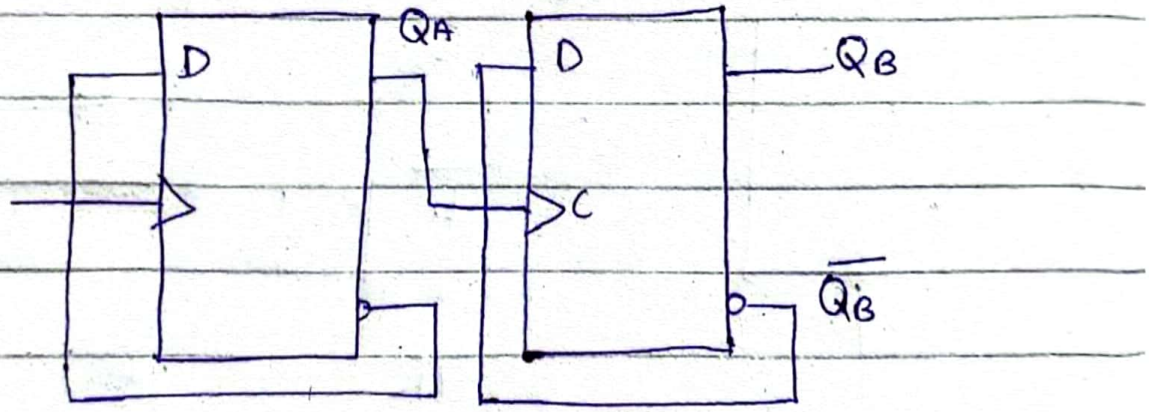
Parallel Data Storage

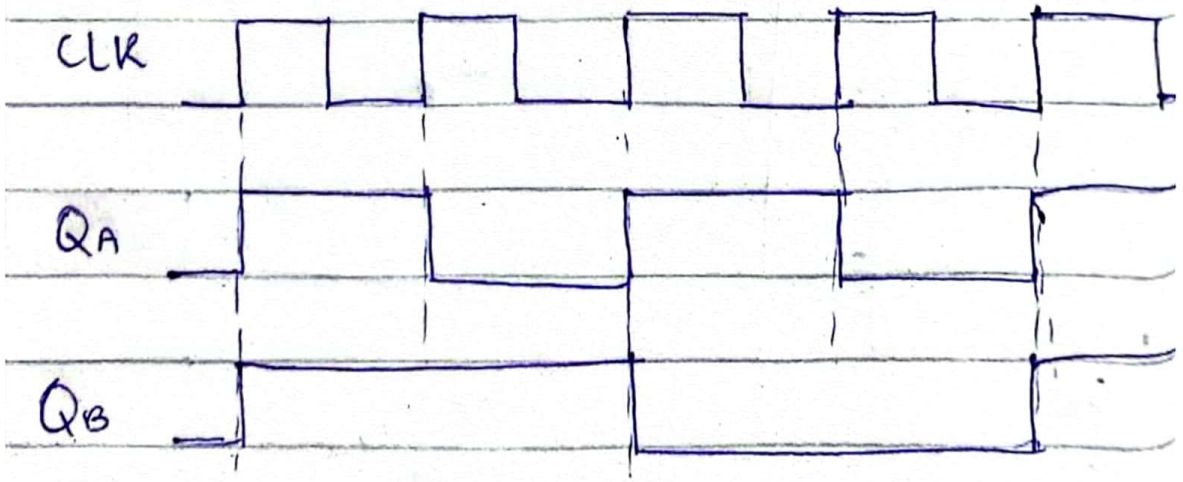

D0
D
Q0
C
R
A
D
Q1
C
R
D2
D
Q2
C
R
D3
D
Q3
C
R
CLR
CLK
D0
D1
D2
D3
CLR
CLK
Q0
Q1
Q2
Q3

Frequency Division

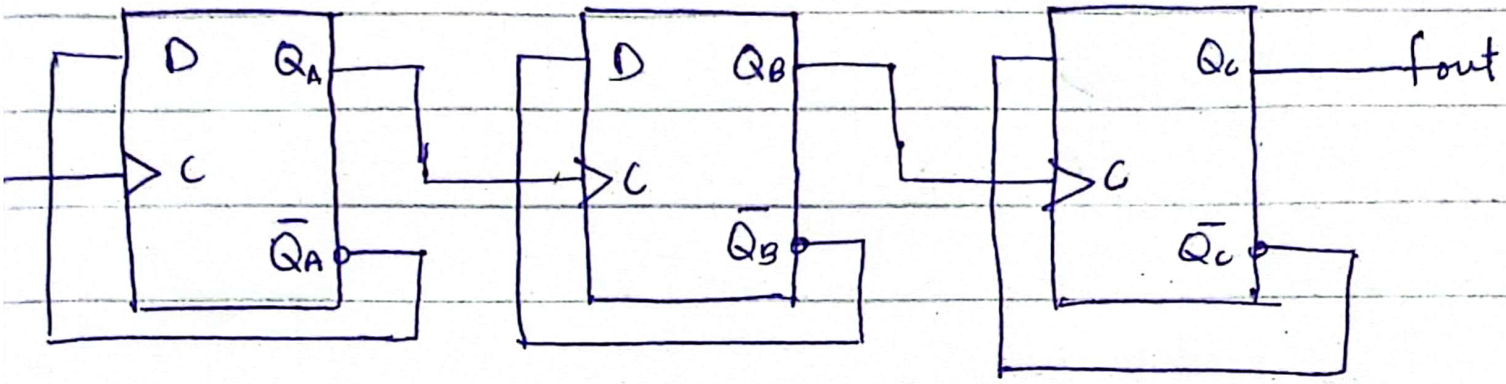


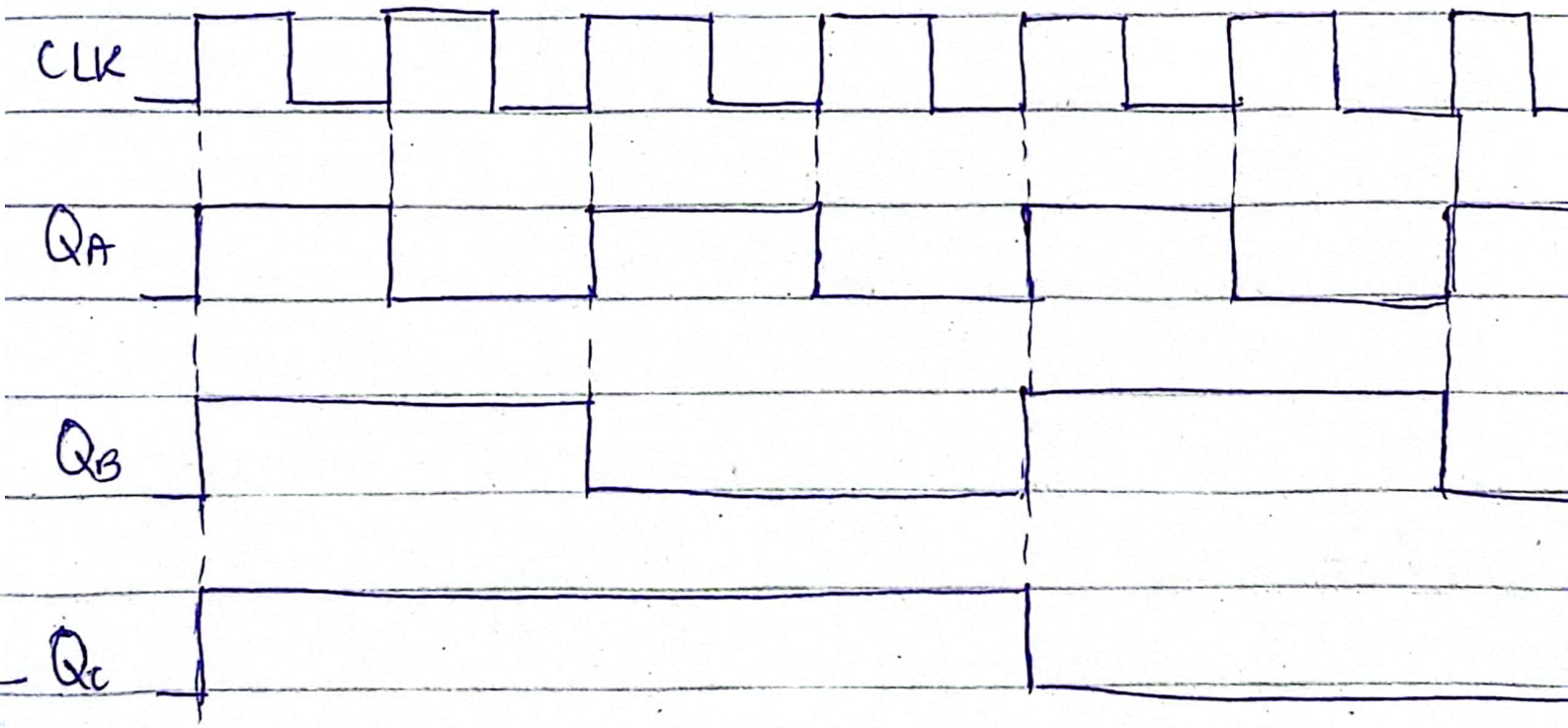






Develop the fout waveform:





fout.