

Assignment:- 2S.D. Hadi

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Q.1 Input waveforms in figure are applied to a 2 bit adder. Determine the waveforms for the sum and the output carry in relation to the inputs by constructing a timing diagram.

| <u>A₁</u> | <u>B₁</u> | <u>C_{in}</u> | <u>Sum</u> | <u>C_{in}</u> <u>out</u> | <u>A₂</u> | <u>B₂</u> | <u>Sum₂</u> | <u>C_{out}</u> |
|----------------------|----------------------|-----------------------|------------|-------------------------------------|----------------------|----------------------|------------------------|------------------------|
| 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |
| 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 |
| 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1 |
| 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 1 |
| 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 1 |

Sum₁ :-Sum₂ :-

Cout :-

Q.2 For the 4-bit comparator in figure, plot each output waveform for the inputs shown. The outputs are active high.

$A > B$

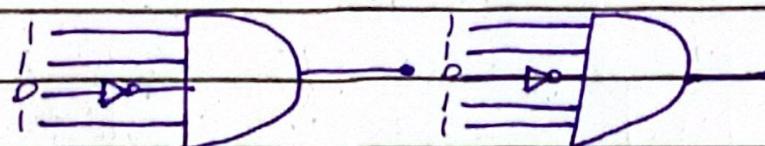
$A = B$

$A < B$

Q.3 Show the decoding logic for each of the following codes if an active-high (1) output is required:

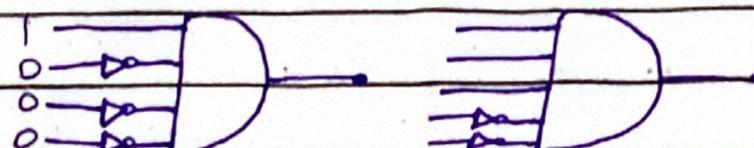
(a) 1101

(c) 11011



(b) 1000

(d) 11100

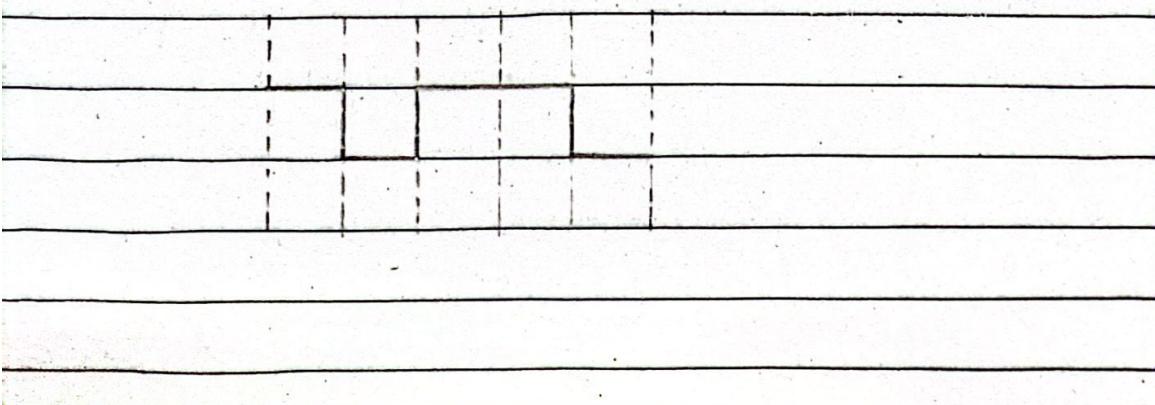


Q.4 You wish to detect only the presence of the codes 1010, 1100, 0001, and 1011. An active high input is required to indicate their presence. Develop the minimum decoding logic with a single output that will indicate when any one of these codes ~~are~~ on the inputs. For any other code, the output must be low.

| $A_2 A_3$ | 00 | 01 | 11 | 10 |
|-----------|----|----|----|----|
| $A_1 A_0$ | 00 | 01 | 10 | 00 |
| | 00 | 01 | 10 | 00 |
| | 01 | 00 | 00 | |
| | 11 | 10 | 00 | |
| | 10 | 00 | 11 | |

$$X = A_0 \bar{A}_1 A_2 + A_0 A_1 \bar{A}_2 \bar{A}_3 + \bar{A}_0 \bar{A}_1 \bar{A}_2 A_3.$$

Q.5 If the ~~wave~~ input waveforms are applied to the decoding logic as indicated in figure, sketch the output waveform in proper relation to the inputs.



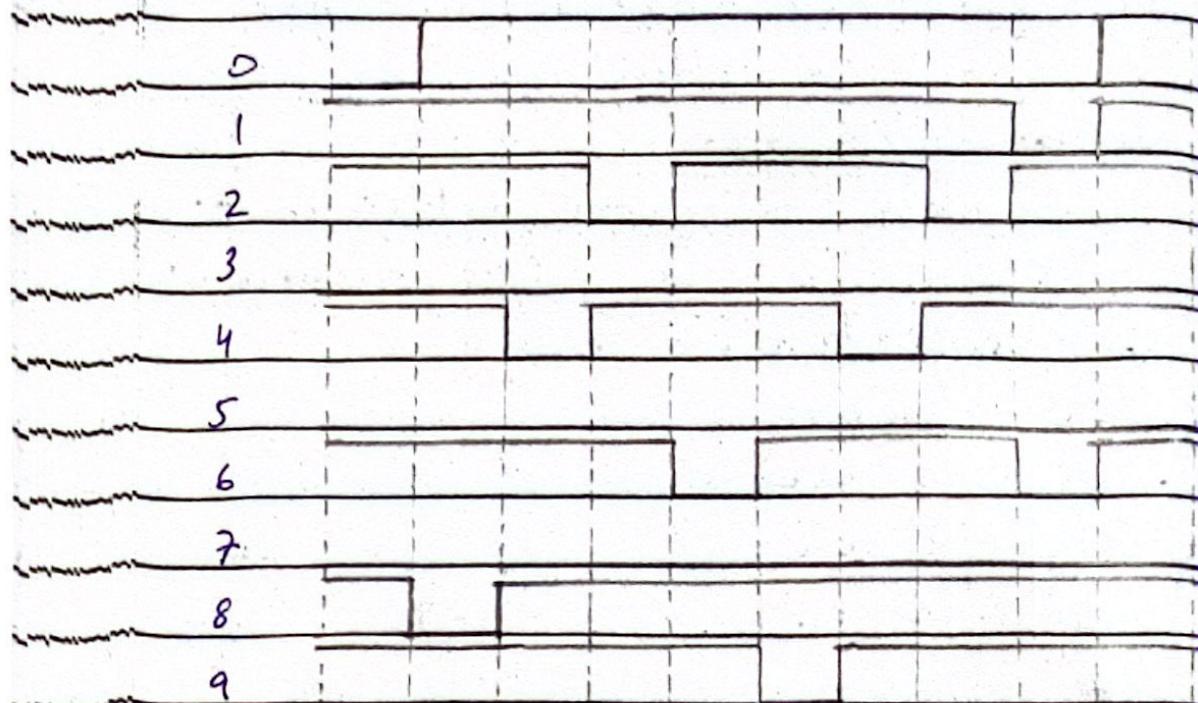
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~~Ali Hadi~~

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Q. 6 BCD numbers are applied sequentially to the BCD-to-decimal decoder in figure. Draw a timing diagram, showing each output in a proper relationship with others and with the inputs.



Q.7 For the decimal to BCD encoder logic of figure, assume that the g input and the s input are both high. What is the output code? Is it a valid BCD (8421) code?

$A_3A_2A_1A_0 = 1011$, which is not valid!

Q.8 The notation x_1, x_0 represents a two-bit binary number that can have any value (00, 01, 10, 11); for example, when $x_1=1, x_0=0$, the binary number is 10, and so on. Similarly, y_1 and y_0 represents another two-bit binary number. Design a logic circuit, using x_1, x_0, y_1 and y_0 inputs, whose output will be high only when the two binary numbers x_1, x_0 , and y_1, y_0 are opposite.

| x_1 | x_0 | y_1 | y_0 | X |
|-------|-------|--------------|-------|---|
| 0 | 0 | (Don't care) | | |
| 0 | 1 | 1 | 0 | 0 |
| 1 | 0 | 0 | 1 | 1 |
| 1 | 1 | 0 | 0 | 1 |

~~Q7.0 For TruthTable~~

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| | x_1 | x_2 | y_1 | y_2 | X | |
|--|-------|-------|-------|-------|-----|--|
| | 0 | 0 | 0 | 0 | 0 | |
| | 0 | 0 | 0 | 1 | 0 | |
| | 0 | 0 | 1 | 0 | 0 | |
| | 0 | 0 | 1 | 1 | 1 | |
| | 0 | 1 | 0 | 0 | 0 | |
| | 0 | 1 | 0 | 1 | 0 | |
| | 0 | 1 | 1 | 0 | 1 | |
| | 0 | 1 | 1 | 1 | 0 | |
| | 1 | 0 | 0 | 0 | 0 | |
| | 1 | 0 | 0 | 1 | 1 | |
| | 1 | 0 | 1 | 0 | 0 | |
| | 1 | 0 | 1 | 1 | 0 | |
| | 1 | 1 | 0 | 0 | 1 | |
| | 1 | 1 | 0 | 1 | 0 | |
| | 1 | 1 | 1 | 0 | 0 | |
| | 1 | 1 | 1 | 1 | 0 | |

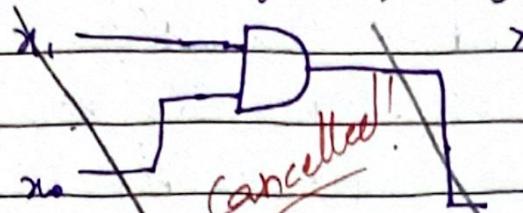
| x_1x_2 | y_1y_2 | 00 | 01 | 11 | 10 |
|----------|----------|----|----|----|----|
| 00 | | | 1 | | |
| 01 | | | | 1 | |
| 11 | | 1 | | | |
| 10 | | | 1 | | |

$$\begin{aligned} & x_1 \bar{x}_2 y_1 \bar{y}_2 + x_1 \bar{x}_2 \bar{y}_1 y_2 + \bar{x}_1 x_2 y_1 \bar{y}_2 + \bar{x}_1 \bar{x}_2 y_1 y_2 \\ & x_1 x_2 (\bar{y}_1 \bar{y}_2) + x_1 \bar{x}_2 (\bar{y}_1 y_2) + (\bar{x}_1 x_2) y_1 \bar{y}_2 + x_1 \bar{y}_1 (\bar{x}_2 + y_2) \end{aligned}$$

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$$x = x_1 \bar{y}_1 (x_0 y_0 + \bar{x}_0 y_0) + \bar{x}_1 y_1 (x_0 y_0 + x_0 \bar{y}_0)$$

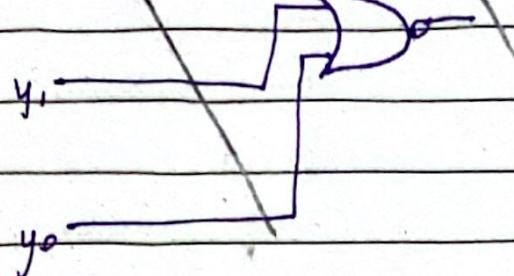


$$x = x_1 \bar{y}_1 (x_0 \oplus y_0)$$

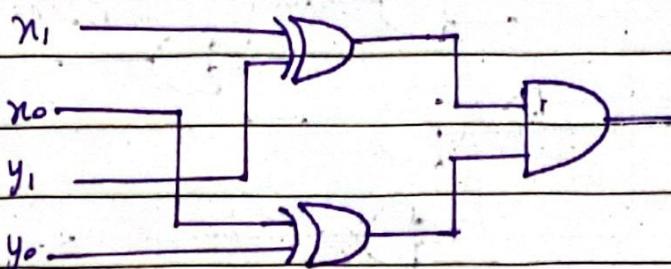
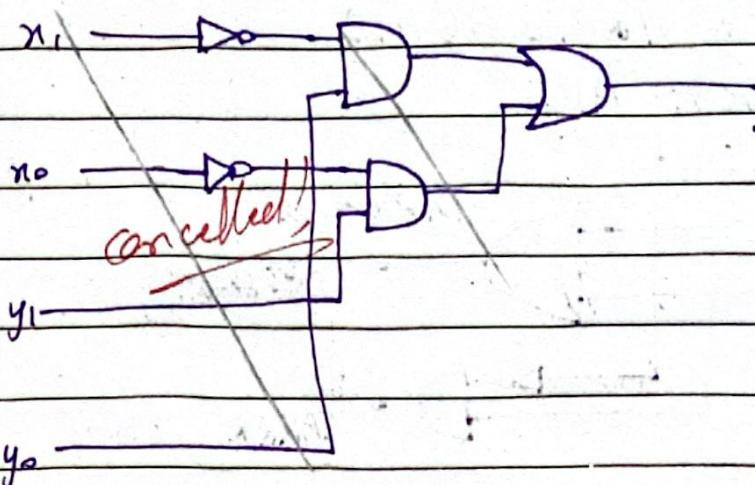
$$+ \bar{x}_1 y_1 (x_0 \oplus \bar{y}_0)$$

$$x = (x_0 \oplus y_0)(x_1 \bar{y}_1 + \bar{x}_1 y_1)$$

$$x = (x_0 \oplus y_0)(x_1 \oplus y_1)$$



$$(x_0 \oplus y_0)(x_1 \oplus y_1)$$

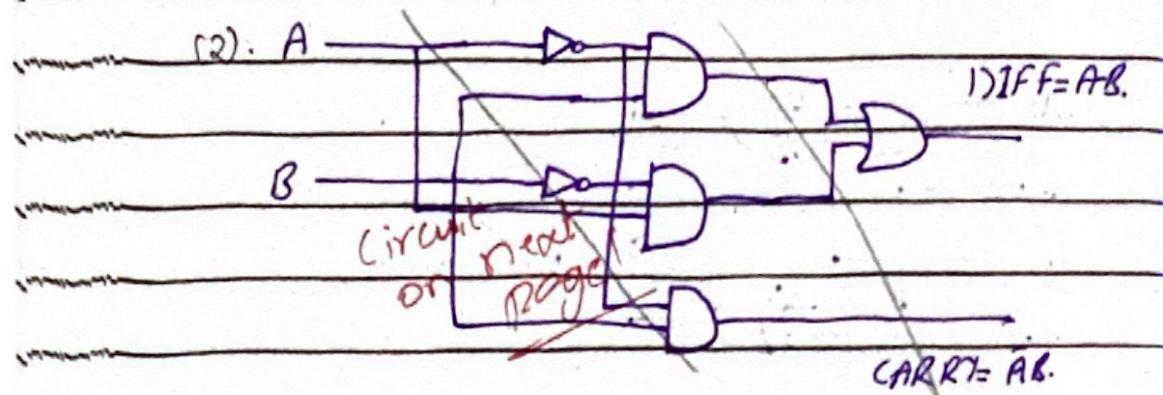
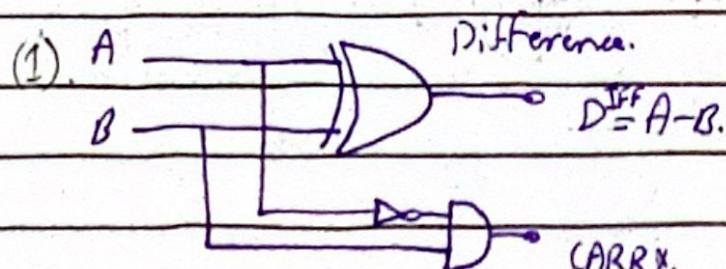
Simplified SOP: - ~~$x_1 y_0 + x_1 y_1$~~ .

Q.9 Write the function table for a half subtractor (input A and B, output DIFF and CARRY). From the function table, design two logic circuits that will act as half subtractor.

| | | DIFF | |
|---|---|------------|-------|
| A | B | Difference | CARRY |
| 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 |

$$\text{DTFF: } A \bullet B \Leftrightarrow \bar{A}B + A\bar{B}$$

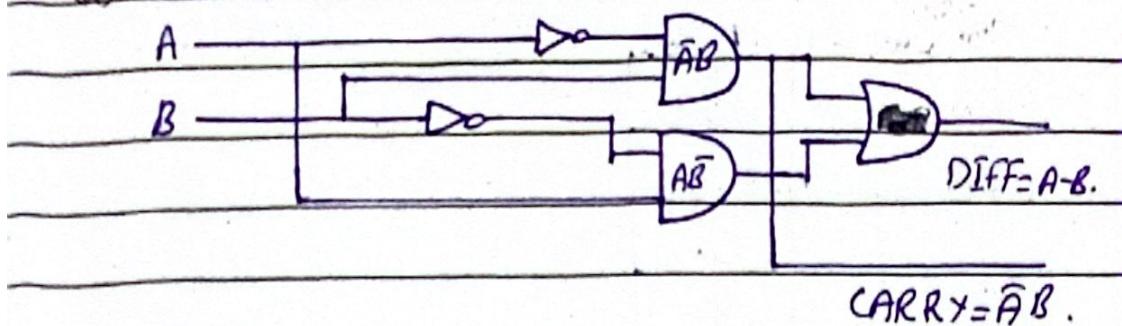
$$(\text{CARRY: } \bar{A}B)$$



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(2).



Q.10 Derive an expression for a 2-bit magnitude comparator using Table.

| A_2 | A_1 | B_2 | B_1 | $A > B$ | $A < B$ | $A = B$ |
|-------|-------|-------|-------|---------|---------|---------|
| 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 0 | 1 | 0 | 1 | 0 |
| 0 | 0 | 1 | 0 | 0 | 1 | 0 |
| 0 | 0 | 1 | 1 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 | 1 | 0 | 0 |
| 0 | 1 | 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 1 | 0 | 0 | 1 | 0 |
| 0 | 1 | 1 | 1 | 0 | 1 | 0 |
| 1 | 0 | 0 | 0 | 1 | 0 | 0 |
| 1 | 0 | 0 | 1 | 1 | 0 | 0 |
| 1 | 0 | 1 | 0 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 | 1 | 0 | 0 |
| 1 | 1 | 0 | 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 | 0 | 0 | 1 |

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Muhammad Ali Hadi

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$A < R$.

$A_1 A_0 \quad B_1 B_0$

00 01 10 10

00 1 1 1 1

01 1 1 1 1

11 1 1 1 1

10 1 1 1 1

$$\Rightarrow \bar{A}_1 B_1 + \bar{A}_1 \bar{A}_0 B_0 + \bar{A}_0 R_1 B_0$$

$$\Rightarrow \bar{A}_1 (B_1 + \bar{A}_0 B_0 (\bar{A}_0 + B_1)) \cdot A_1 R_1 + \bar{A}_0 B_0 (\bar{A}_1 + B_1).$$

$A > R$.

$A_1 A_0 \quad B_1 B_0$

00 01 11 10

00 1 1 1 1

01 1 1 1 1

11 1 1 1 1

10 1 1 1 1

$$\Rightarrow A_1 \bar{B}_1 + A_0 \bar{B}_0 \bar{B}_1 + A_1 A_0 \bar{B}_0$$

$$\Rightarrow A_1 \bar{B}_1 + A_0 \bar{B}_0 (\bar{B}_1 + A_1).$$

$A = R$.

$A_1 A_0 \quad B_1 B_0$

00 01 11 10

00 1 1 1 1

01 1 1 1 1

11 1 1 1 1

10 1 1 1 1

$$\Rightarrow \bar{A}_1 \bar{A}_0 \bar{B}_1 \bar{B}_0 + \bar{A}_1 \bar{A}_0 \bar{B}_1 B_0$$

$$+ A_1 \bar{A}_0 B_1 \bar{B}_0 + A_1 A_0 B_1 B_0$$

$$\Rightarrow \bar{A}_1 \bar{B}_1 (\bar{A}_0 \bar{B}_0 + A_0 B_0)$$

$$+ A_1 B_1 (\bar{A}_0 \bar{B}_0 + A_0 B_0).$$

$$\Rightarrow \bar{A}_1 \bar{B}_1 (\bar{A}_0 \oplus B_0) + A_1 B_1 (\bar{A}_0 \oplus B_0)$$

$$\Rightarrow (\bar{A}_1 \bar{B}_1 + A_1 B_1) (\bar{A}_0 \oplus B_0) \Rightarrow (\bar{A}_0 \oplus B_0) (\bar{A}_1 \oplus B_1)$$

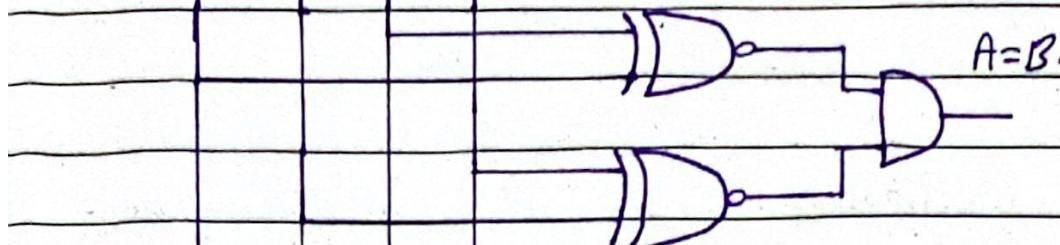
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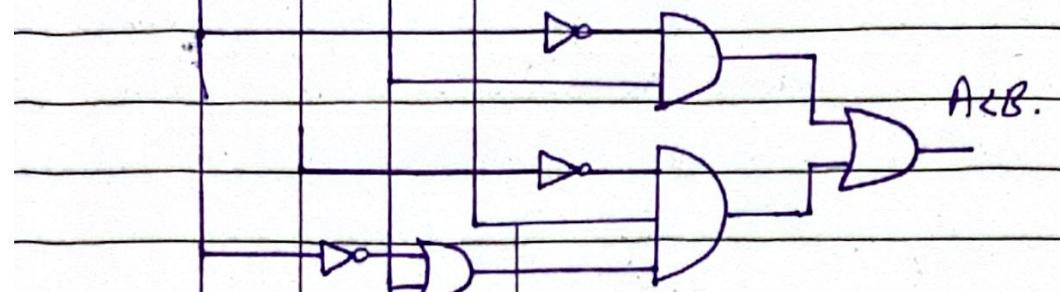
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Circuit Diagram.

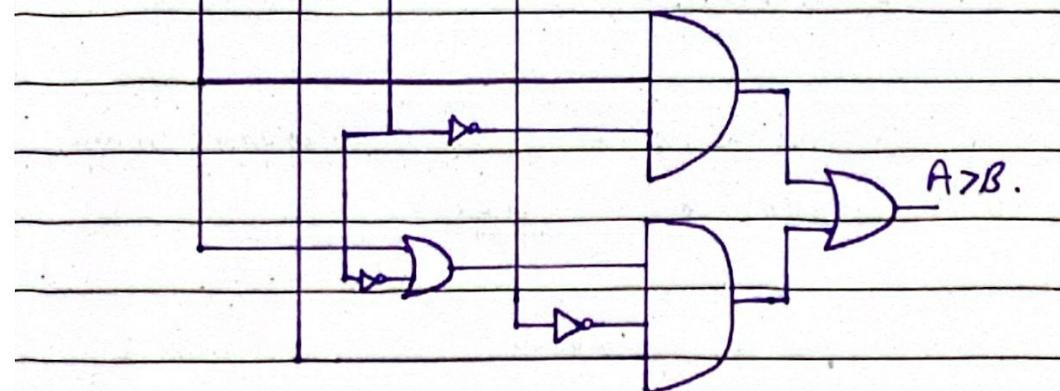
$A_1 \ A_0 \ B_1 \ B_0$



$$A=B.$$



$$A < B.$$



$$A > B.$$

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Q.11 For the multiplexer in Figure 1, determine the output for the following input states: $D_0=1, D_1=0, D_2=0, D_3=1$.

(a) $S_0=0, S_1=1$

| S_1 | S_0 | y |
|-------|-------|-------|
| 0 | 0 | D_0 |
| 0 | 1 | D_1 |
| 1 | 0 | D_2 |
| 1 | 1 | D_3 |

Type Error in Question.

(b) $S_1=0, S_0=1$

Output = D_1 .

Q.12 If the data inputs to the multiplexer in the above Figure 1 are sequenced as shown by the wave form in Figure 2, determine the output waveform with the data inputs specified.

y

$D_0 \ D_2 \ D_1 \ D_3 \ D_3 \ D_1 \ D_2 \ D_0 \ D_1 \ D_2 \ D_2 \ D_0$

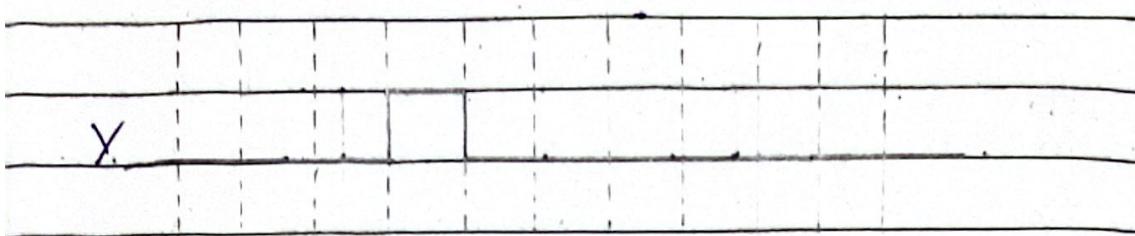
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Q.13 The waveforms in figure are observed on the inputs of a 74HC151-8-input multiplexer. Sketch the y-output waveform.



Q.14 Develop the total timing diagram (inputs and outputs) for a 74HC154 used in a demultiplexing application in which the inputs are as follows: The data-select inputs are repetitively sequenced through a straight binary count beginning with 0000, and the data input is serial data stream carrying BCD data representing the decimal number 2468. The least significant digit (8) is the first in sequence, with its LSB first, and it should appear in the first 4-bits positions of the output.

~~Ali Hadi~~ Muhammad Ali Hadi
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~~Ali Hadi~~ Muhammad Ali Hadi
Date: 23-K-O65.

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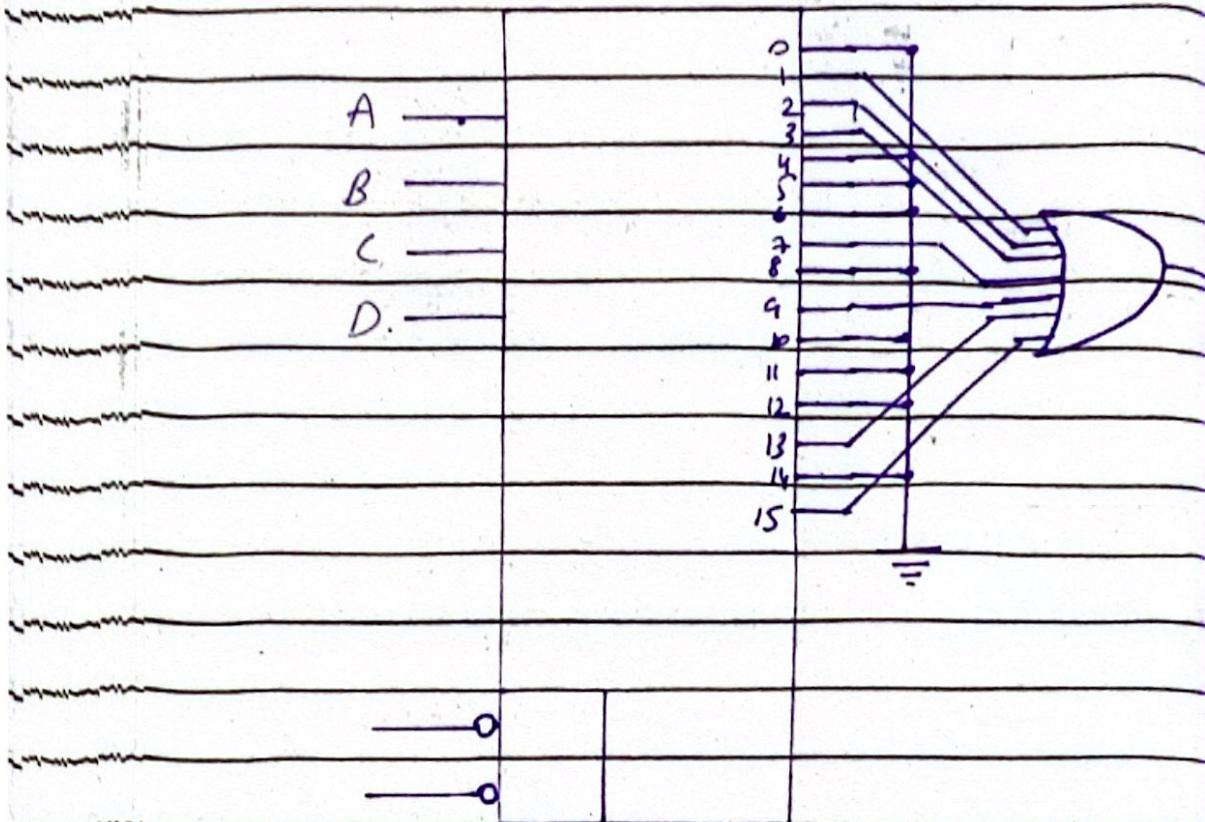
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Q.15 Implement the following Boolean function using the decoder.

$$F(A, B, C, D) = \sum(1, 2, 3, 7, 9, 13, 15)$$



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S.B.Hadi 23K-0663.

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Q.16 Implement the logic function in
the table by using a 74S151 8 input
data selector/multiplexer. $\chi(A_3, A_2, A_1, A_0)$
 $= \Sigma(2, 3, 4, 8, 9, 10, 11, 15)$.

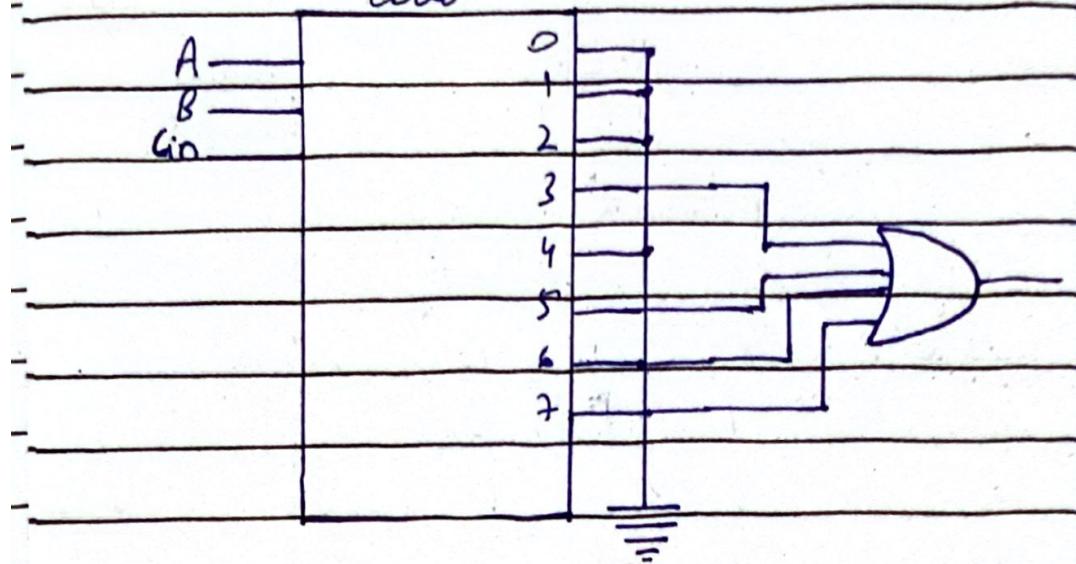
| | A ₃ | A ₂ | A ₁ | A ₀ | X | | |
|----|----------------|----------------|----------------|----------------|---|------------------|--|
| 0 | 0 | 0 | 0 | 0 | 0 | x=0. | |
| 1 | 0 | 0 | 0 | 1 | 0 | | |
| 2 | 0 | 0 | 1 | 0 | 1 | x=1. | |
| 3 | 0 | 0 | 1 | 1 | 1 | | |
| 4 | 2 | 0 | 1 | 0 | 0 | x=A ₃ | |
| 5 | 0 | 1 | 0 | 1 | 0 | | |
| 6 | 1 | 0 | 0 | 0 | 1 | x=A ₂ | |
| 7 | 1 | 0 | 0 | 1 | 1 | | |
| 8 | 1 | 1 | 0 | 0 | 0 | x=0. | |
| 9 | 1 | 1 | 0 | 1 | 0 | | |
| 10 | 1 | 1 | 1 | 0 | 1 | x=A ₁ | |
| 11 | 1 | 1 | 1 | 1 | 1 | | |
| 12 | 1 | 1 | 1 | 1 | 1 | x=A ₀ | |
| 13 | 1 | 1 | 1 | 1 | 1 | | |
| 14 | 1 | 1 | 1 | 1 | 1 | | |
| 15 | 1 | 1 | 1 | 1 | 1 | | |
| 16 | 1 | 1 | 1 | 1 | 1 | | |

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Ali Haider

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Qout



(b) 4x1 Multiplexers.

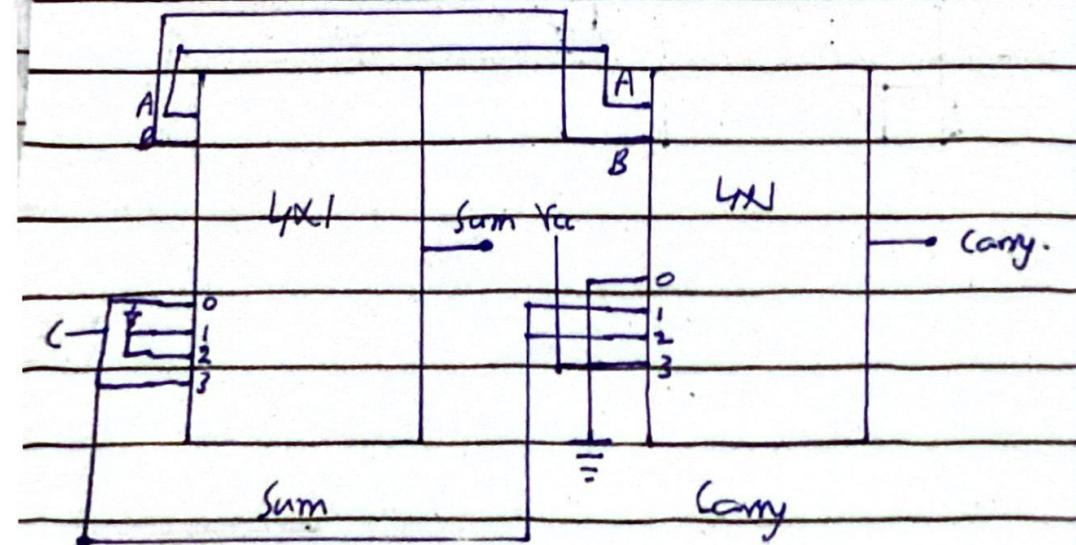
A B Cin Σ Qout

0 0 0 0 0 0 $x=0$
0 0 1 1 0 $x=0$

0 1 0 1 0 $x=c$
0 1 1 0 1

1 0 0 1 0 $x=c$
1 0 1 0 1

1 1 0 0 1 $x=1$
1 1 1 1 1



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SH. Hadi

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Q.17. Implement a full adder circuit by using:

(a). 3-to-8 line decoder.

A B cin sum cout

0 0 0 0 0

0 0 1 1 0

0 1 0 1 0

0 1 1 0 1

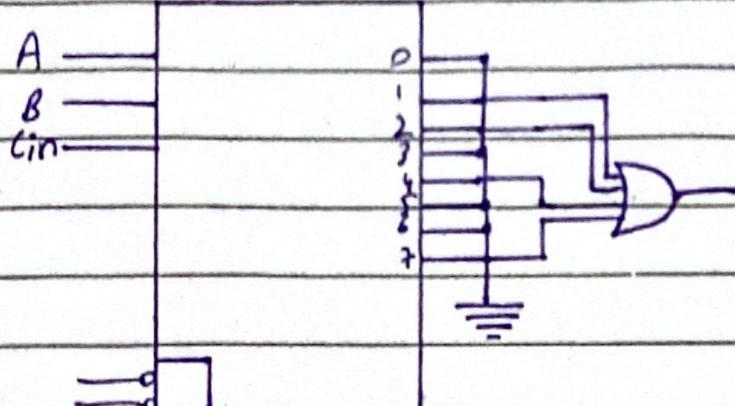
1 0 0 1 0

1 0 1 0 1

1 1 0 0 1

1 1 1 1 1

Sum



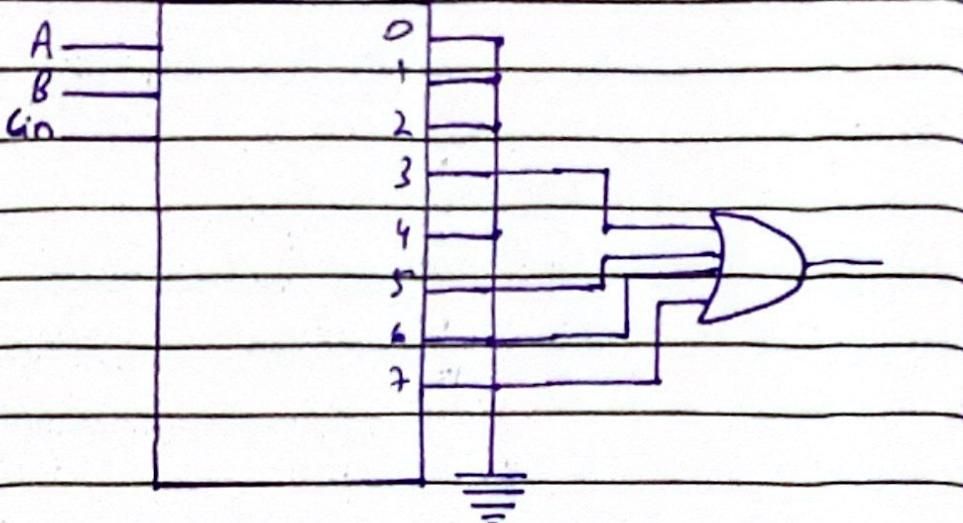
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Cout



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Q18 Construct a 16×1 multiplexer with two 8×1 and 2×1 multiplexers. Use block diagrams.

