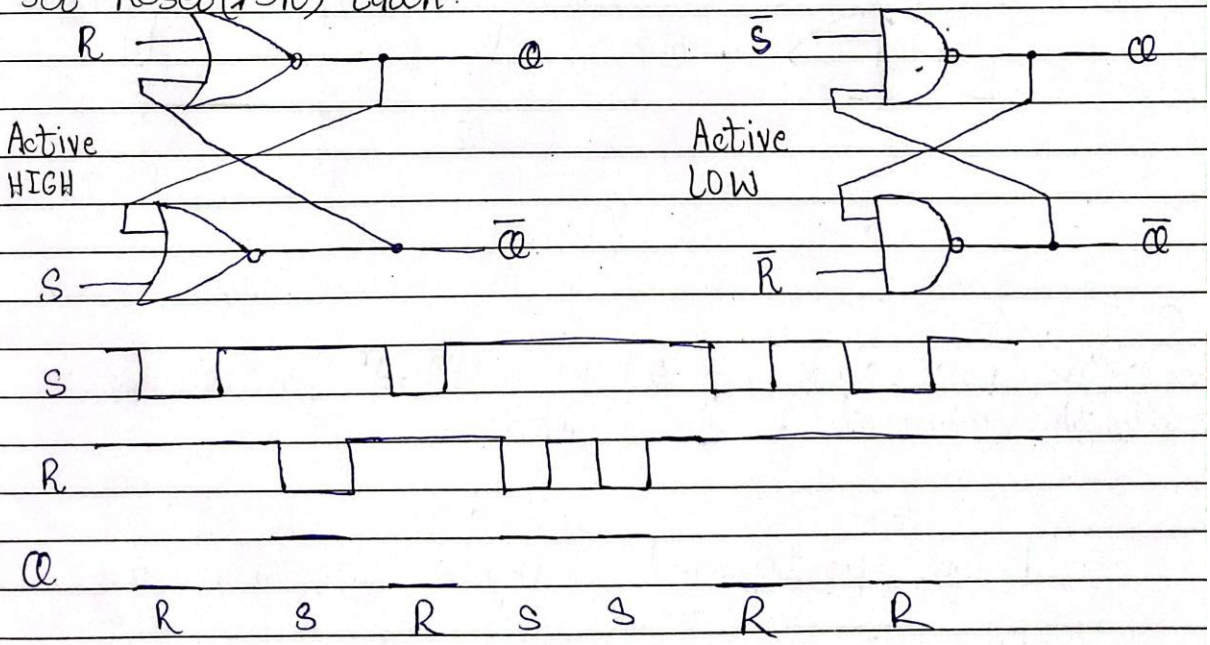
Date: _____

Latches and Flip Flops

- Flip flops are building blocks of sequential circuits.
- Astable don't have stable 0s and 1s; non-stop change in values 202020
- Monostable have single stable state (not in course)
- Bistable have two stable states 111001111000
  - Flip flops are bistable multivibrators.

- Latches and flip flops store data.
  - Latches manually operated, flip flops automatic through clock (CLK)

Set-Reset (SR) Latch:



Date: _____

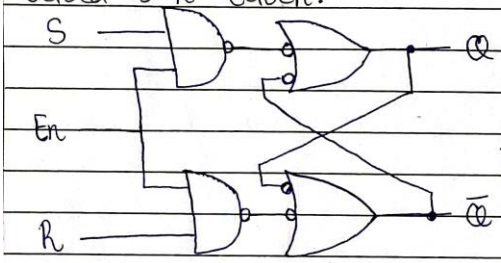
Active HIGH S-R

S	R	Q	$\overline{Q}$	
0	0	NC	NC	No Change
0	1	0	1	Reset
1	0	1	0	Set
1	1	0	0	Invalid

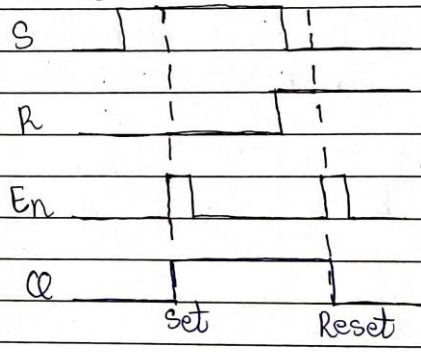
Active LOW S-R

$\overline{S}$	$\overline{R}$	Q	$\overline{Q}$	
0	0	1	1	Invalid
0	1	1	0	Set
1	0	0	1	Reset
1	1	NC	NC	No Change

Gated S-R Latch:



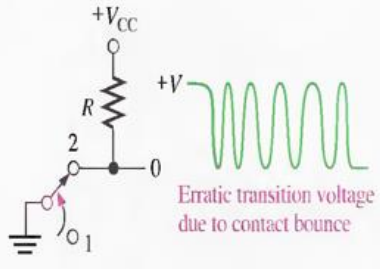
Initially Reset



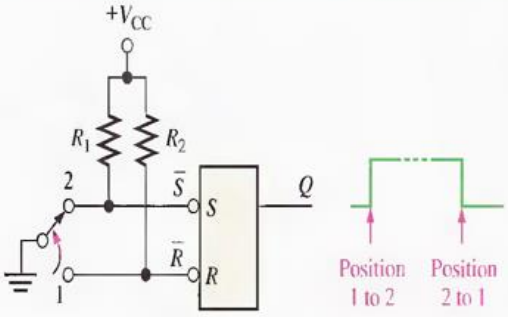
An Application

The Latch as a Contact-Bounce Eliminator

SR



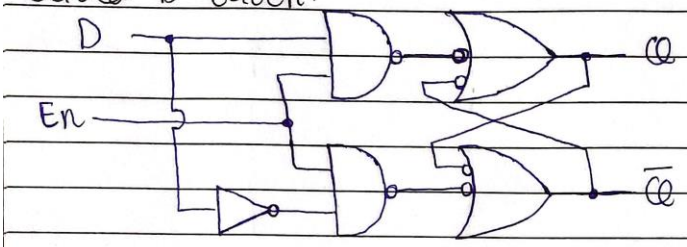
(a) Switch contact bounce



(b) Contact-bounce eliminator circuit

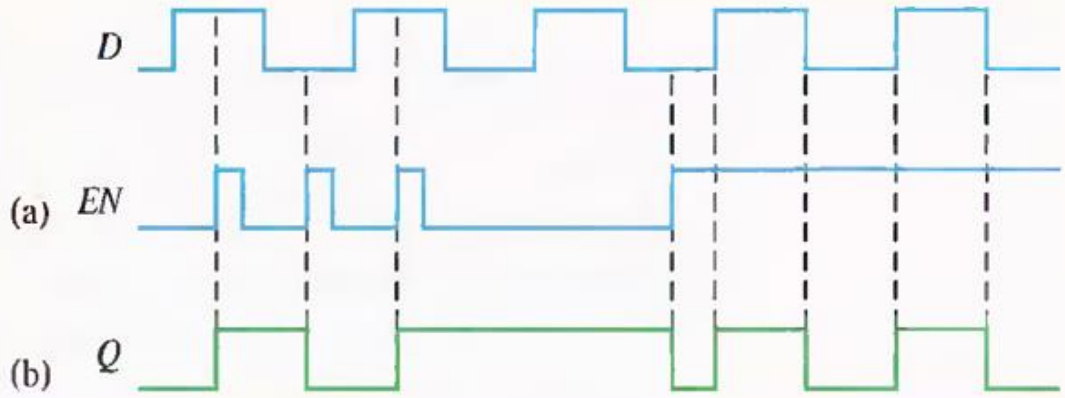
Date: _____

Gated D Latch:



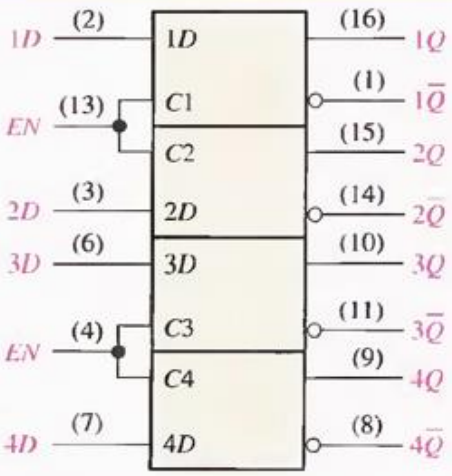
When En is HIGH,
$Q = D$
When En is LOW,
NC(No Change)

Determine the Q output waveform if the inputs shown in Figure 7–11(a) are applied to a gated D latch, which is initially RESET.



THE 74LS75 D LATCH

The 74LS75 quad gated D latches.



(a) Logic symbol

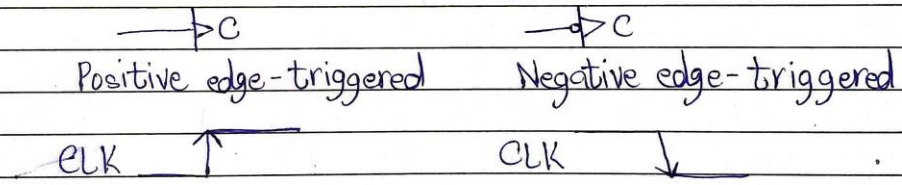
Inputs		Outputs		
D	EN	Q	$\overline{Q}$	Comments
0	1	0	1	RESET
1	1	1	0	SET
X	0	Q_0	$\overline{Q}_0$	No change

Note: Q_0 is the prior output level before the indicated input conditions were established.

(b) Truth table (each latch)

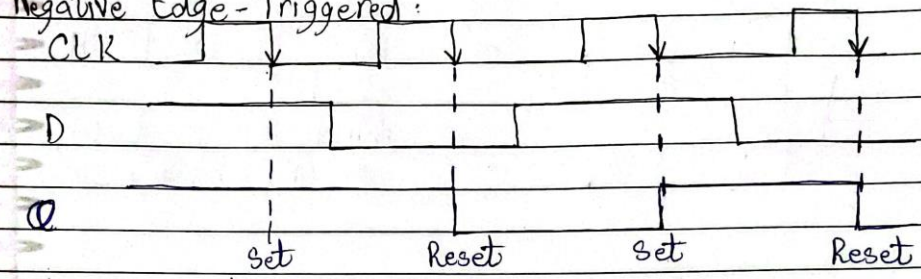
Clock:

- Positive pulse(clock goes ⊕ LOW to HIGH); positive edge triggered
  At this moment IC is enabled

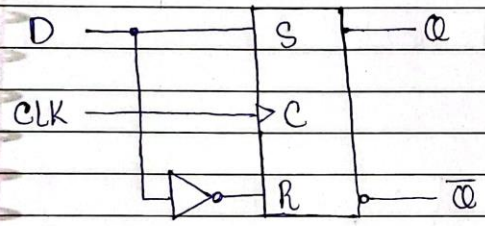


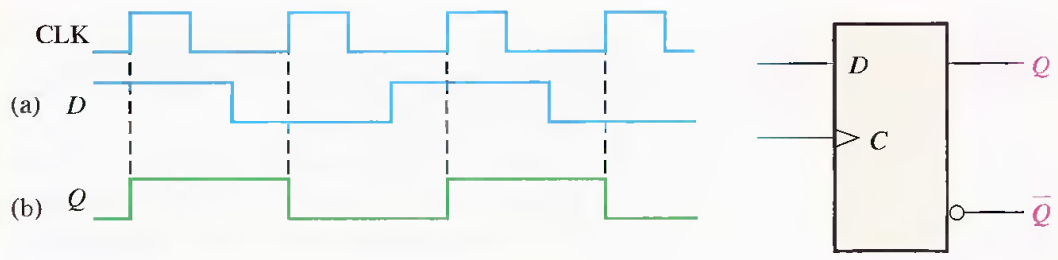
Date: _____

Negative Edge-Triggered:

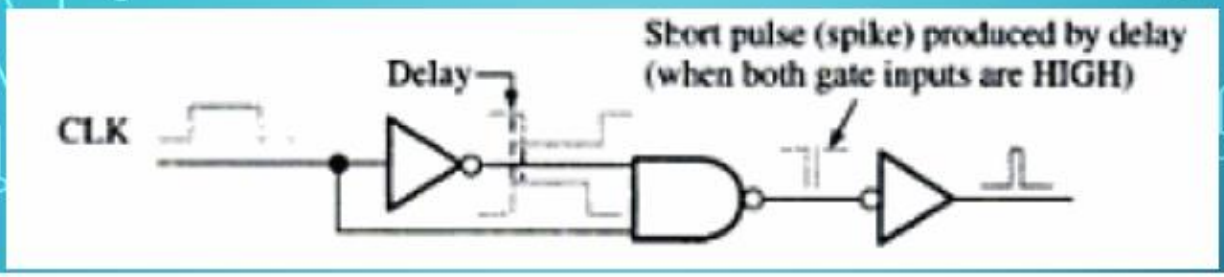


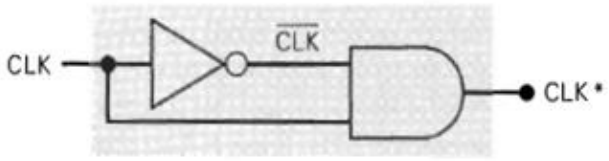
Edge-Triggered D Flip Flop:

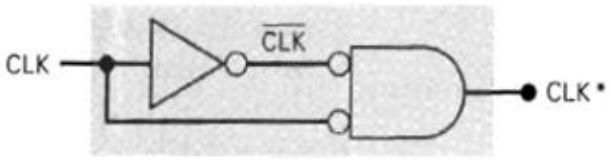


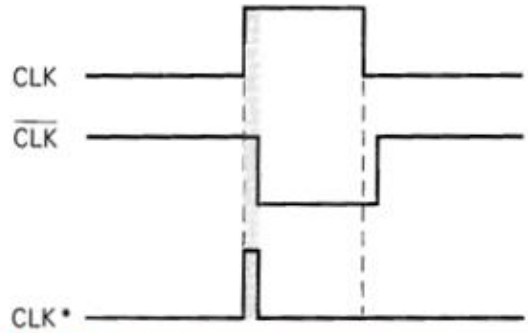


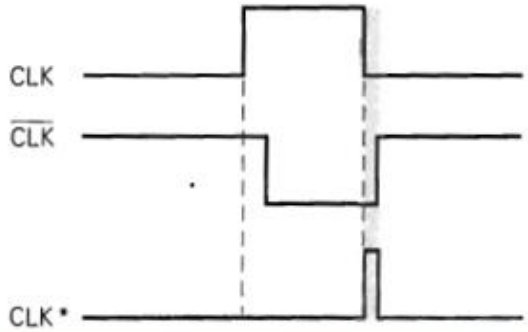
A type of Pulse Transition detector







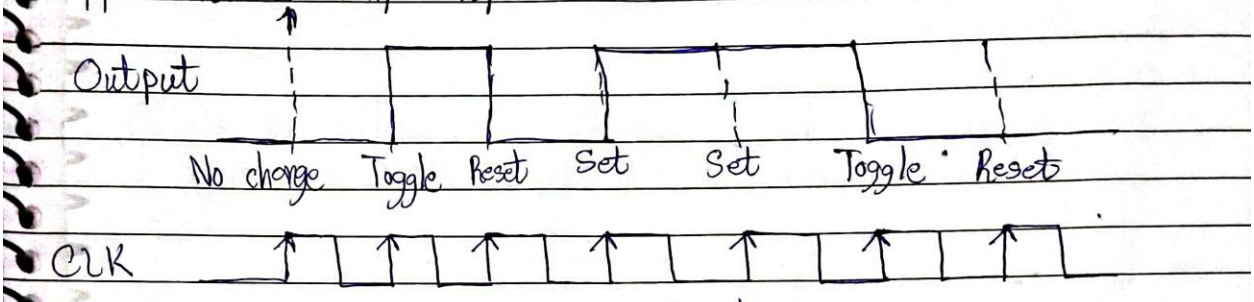




J-K

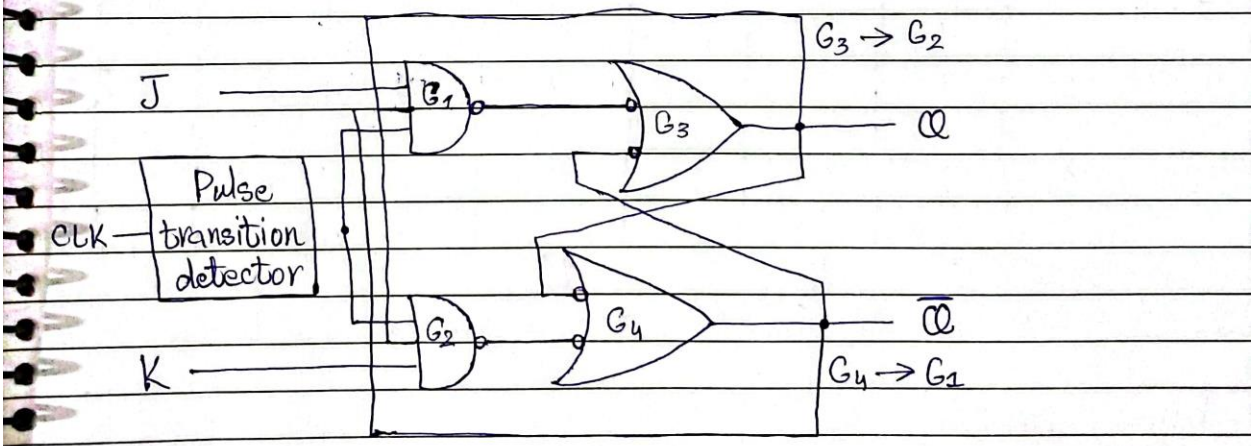
Date: _____

~~Application of~~ Flip Flops:



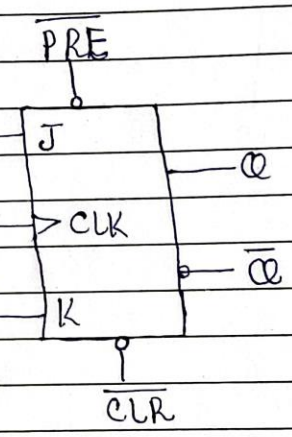
JK flip flop are synchronous (synchronised with clock) inputs

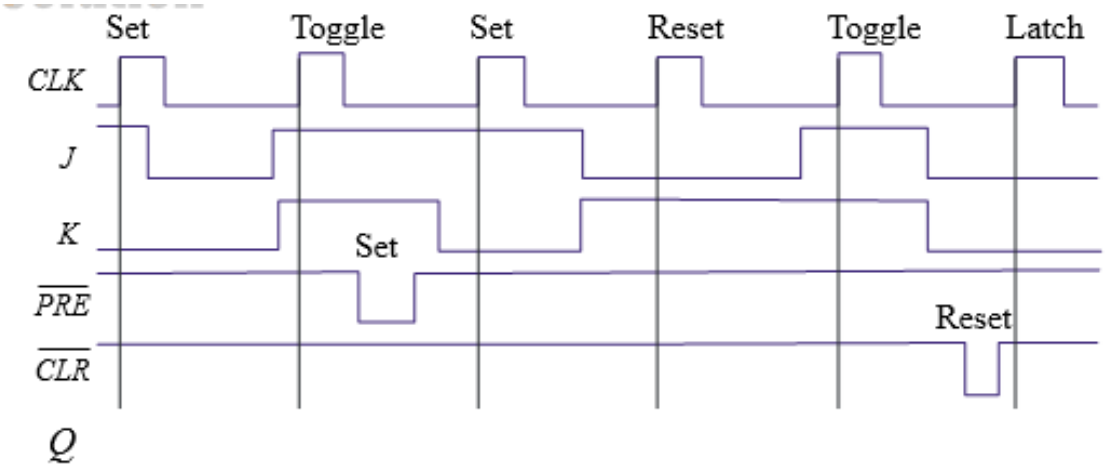
J	K	Q_n	$\overline{Q}_n$		
0	0	~~NC~~ Q_n	$\overline{Q}_n$	No Change	
0	1	0	1	Reset	No invalid condition
1	0	1	0	Set	
1	1	$\overline{Q}_{n-1}$	Q_{n-1}	Toggle	



Asynchronous Inputs:

- Affect output independent of the clock.
- Preset (PRE) and clear (CLR) are usually active LOW.
  - By default HIGH
  - Will modify output when set to LOW
  - PRE will make output HIGH
  - CLR → output LOW

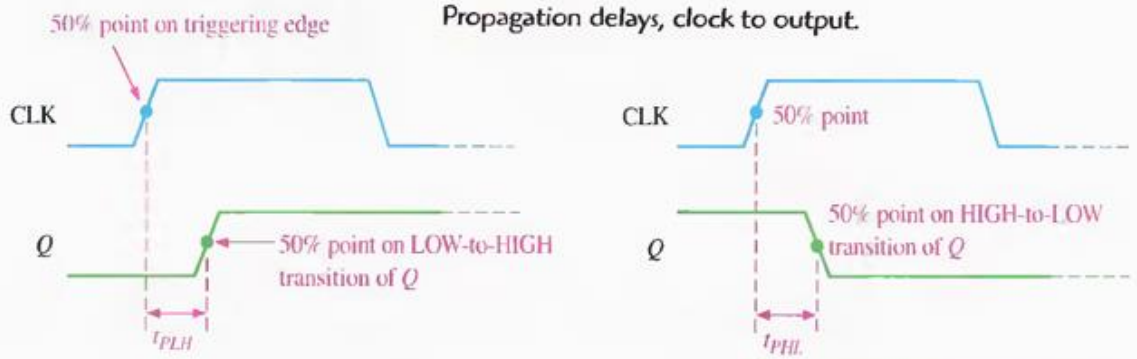




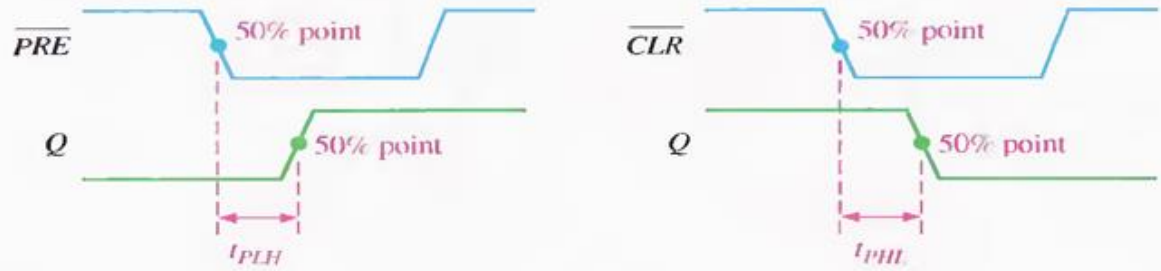
FLIP-FLOP OPERATING CHARACTERISTICS

Propagation Delay Times

Propagation delays, clock to output.

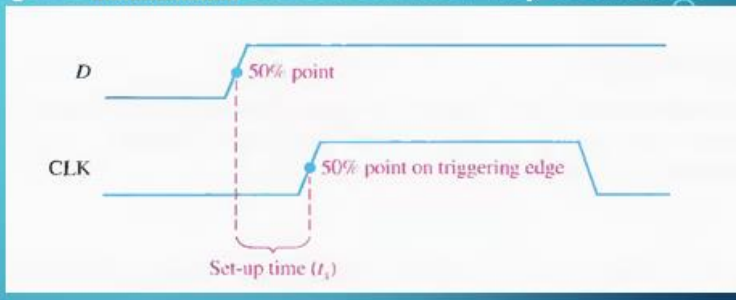


Propagation delays, preset input to output and clear input to output.



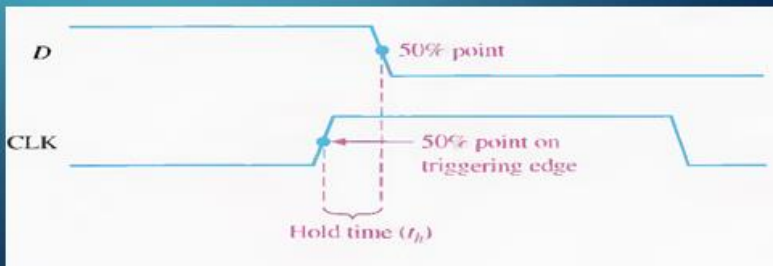
Set-up Time

The set-up time (ts) is the minimum interval required for the logic levels to be maintained constantly on the inputs (J and K, or Sand R, or D) prior to the triggering edge of the clock pulse in order for the levels to be reliably clocked into the flip-flop.
for a D flip-flop.



Hold Time

The hold time (th) is the minimum interval required for the logic levels to remain on the inputs after the triggering edge of the clock pulse in order for the levels to be reliably clocked into the flip-flop. for a D flip-flop.



Maximum Clock Frequency

The maximum clock frequency (f_{max}) is the highest rate at which a flip-flop can be reliably triggered. At clock frequencies above the maximum, the flip-flop would be unable to respond quickly enough, and its operation would be impaired.

Pulse Widths

Minimum pulse widths (t_W) for reliable operation are usually specified by the manufacturer for the clock, preset, and clear inputs. Typically, the clock is specified by its minimum HIGH time and its minimum LOW time.

Power Dissipation

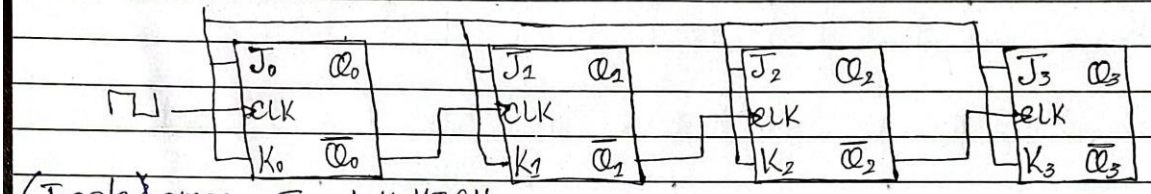
The **power dissipation** of any digital circuit is the total power consumption of the device. For example, if the flip-flop operates on a +5 V dc source and draws 5 mA of current, the power dissipation is

$$P = V_{CC} \times I_{CC} = 5\text{ V} \times 5\text{ mA} = 25\text{ mW}$$

Date: _____

Applications of JK Flip Flop:

- Data storage / ~~no~~ transfer
- Frequency divider
  - Frequency divided by 2^n where n = number of JK flip flops.
  - If input f = 8 kHz and 2 flip flops, output frequency = $\frac{8}{2^2}$ = 2kHz



(Toggle since J and K HIGH

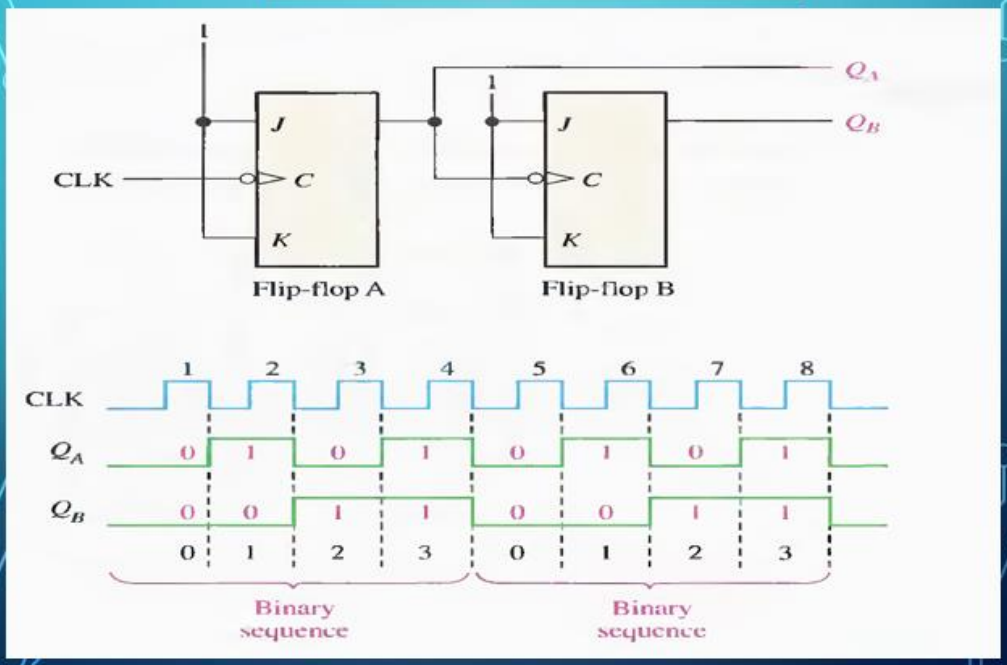
CLK	1	2	3	4	5	6	7	8
$\overline{Q_0}$	1 0	1 0	1 0	1 0	1 0	1 0	1 0	1
$\overline{Q_1}$	1 1	0 0	1 1	0 0	1 1	0 0	1 1	
$\overline{Q_2}$	1 1	1 1	0 0	0 0	0 0	0 0	1 1	
$\overline{Q_3}$	1 1	1 1	1 1	1 1	1 1	1 1	1 0	
	15	14	13	12	11	10	9	8 7

Q_0 is 1/2 and Q_1 is 1/4 the frequency of CLK and so on

- Binary counter
  - Pattern of binary count sequence is same as initialisation of truth table inputs

Counting

Flip-flops used to generate a binary count sequence. Two repetitions (00, 01, 10, 11) are shown.

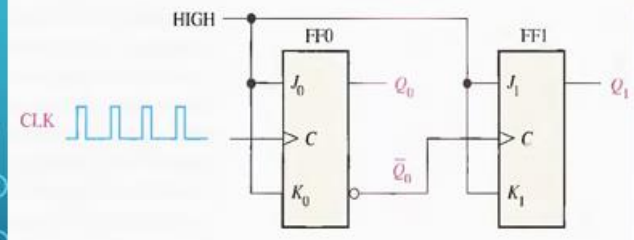


ASYNCHRONOUS COUNTER OPERATION

The term **asynchronous** refers to events that do not have a fixed time relationship with each other and, generally, do not occur at the same time. An **asynchronous counter** is one in which the flip-flops (FF) within the counter do not change states at exactly the same time because they do not have a common clock pulse.

A 2-Bit Asynchronous Binary Counter

Asynchronous counters are also known as ripple counters.



CLOCK PULSE	Q_1	Q_0
Initially	0	0
1	0	1
2	1	0
3	1	1
4 (recycles)	0	0