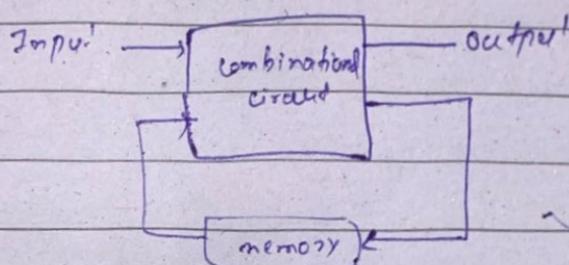


Ch#03

present input
full adder, etc
propagation delay = the amount of time required for a signal to be received after it has been sent.

Sequential circuit → output depends on the present input and past output



memory element in addition to combinational circuit Two types of sequential circuit

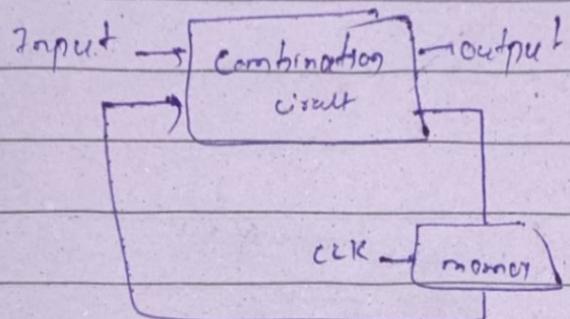
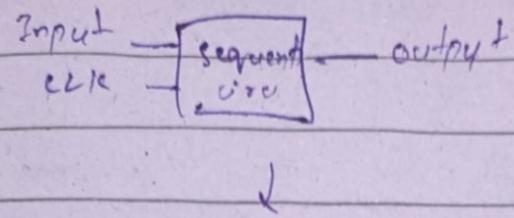
Synchronous
↳ circuit responds to the input only at the discrete time intervals

Asynchronous
↳ circuit immediately responds to the input level change

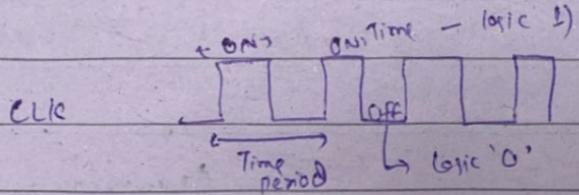
Synchronous Seq: Circuit → circuit responds to input only at the discrete intervals of time

↳ to respond at the discrete time this circuit has one more input signal (clock signal)

Clock :- It is the periodic train of pulses, where values changes b/w two voltage levels.
 logic "0" & "1"



Time period :- time after which the clock signal repeats itself is known as time period.



Duty cycle :- $\left(\frac{T_{on}}{T_{time period}} \right) \times 100\%$

$$\text{if } D.C = 50\% \rightarrow \text{ON Time} = \text{OFF Time}$$

$$D.C < 50\% \rightarrow \text{ON Time} < \text{OFF Time}$$

$$D.C > 50\% \rightarrow \text{ON Time} > \text{OFF Time}$$

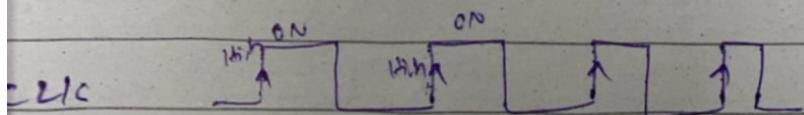
④ There are some sequential circuit which responds to the input during the entire ON time of the clock signal, so this sequential circuit are called level triggered circuit.

↳ sensitive to clock signal

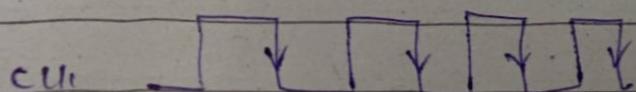
↳ means the seq:circ: responds to the input when clk signal is high

⑤ The sequential circuit which responds to the input at the CLK transition are known as edge triggered circuit.

↳ So these edge triggered circuit which responds on rising edge of the clk are called positive edge triggered s.c



which responds on falling edge are called
Negative edge triggered s.c



① The memory element will respond to each input (output of the combinational circuit) at either rising or falling edge of the clock in the edge triggered sequential circuit.

if rising or falling edge pass then the memory element will not respond to the coming input , it will respond again during next transition.

② In these synchronous sequential circuit the propagation delay of the logic gate will decide the maximum clock frequency :

when $P.D < \text{Time period of the CLK signal}$.

Basic functions

Latches ← of Memory → Flip Flops
 element

Both stores 1

← bit in formation →
(0,1)

Their output is
only 1 or 0

since both have only
two stable states so

← They are also known as →
Bistable multivibrator.

Latch

=

Transistor

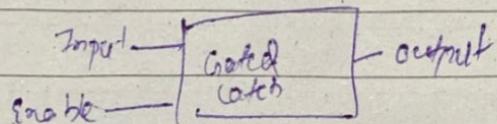
Input → latch → output

↳ asynchronous type of memory
element.

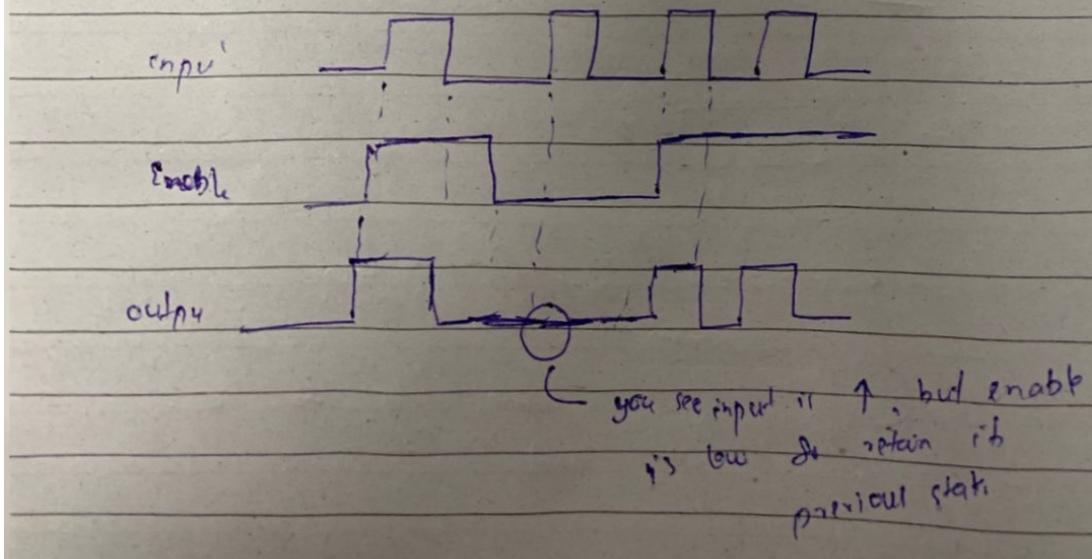
↳ b/c it responds immediately to the
input signal.

(v) The latch which immediately responds to the change in the input are called Transparent Latch.

(vi) Another type of Latch which became transparent based on the control input (enable) so this latch is called gated latch

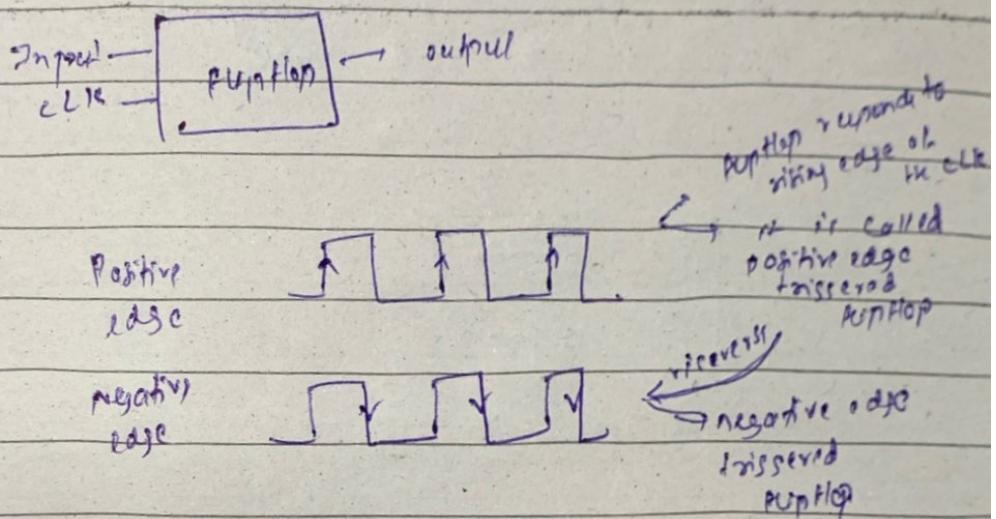


(vii) If the enable is high then the gated latch will immediately responds to its output but if the enable (clock signal is low), the output will retain the previous state of output

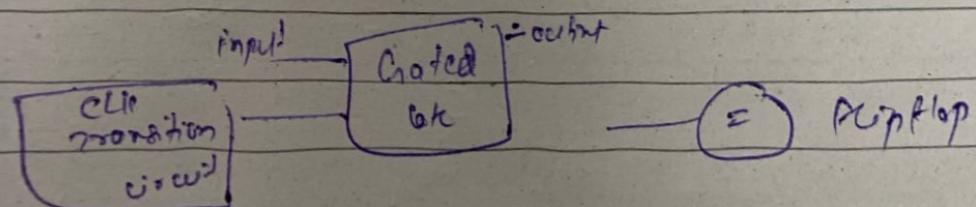


Flip Flops

• flip flops have CLK signal input means it only responds to the clock transition, that means the flip flops is an edge triggered memory element



- ③ in case of positive edge triggered flip flop, at the time of rising the flip flop will respond to the input and on the time of falling, flip flop will retain its previous state (vice versa for negative)



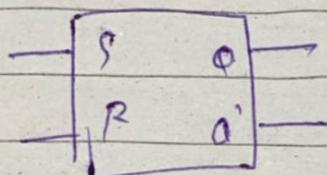
if any input
on NOR is
1 non output
it is 0

NOR

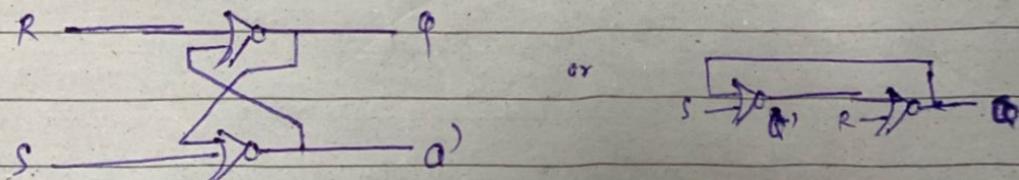
$$\begin{bmatrix} A & B & Y \\ 1 & 1 & 0 \\ 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix}$$

SR-latch.

⑥ or latch and flipflop both are made of logic gate, but logic gates itself doesn't have the memory, and they can't store the binary information. but using the feedback from the output to the input side.



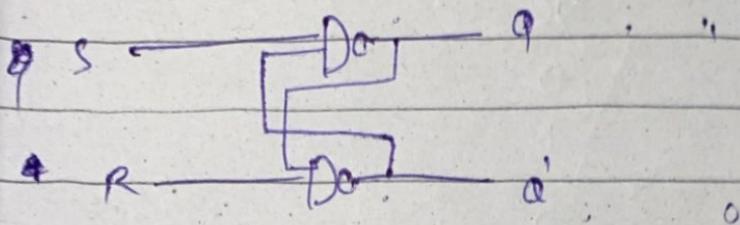
Active High SR-latch.



S	R	Q	next state	Q	Q	next state
0	0	1	1	1	1	invalid or forbidden state
0	1	0	0	0	1	
1	0	1	0	1	0	
1	1	NC	NC	NC	NC	next state of a RO

Active low SR latch

AND		Y
A	B	
0	0	0
0	1	0
1	0	0
1	1	1

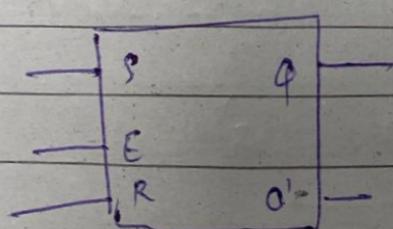


S	R	Q	Q'
0	0	NC	NC
0	1	1	0
1	0	0	1
1	1	0	0

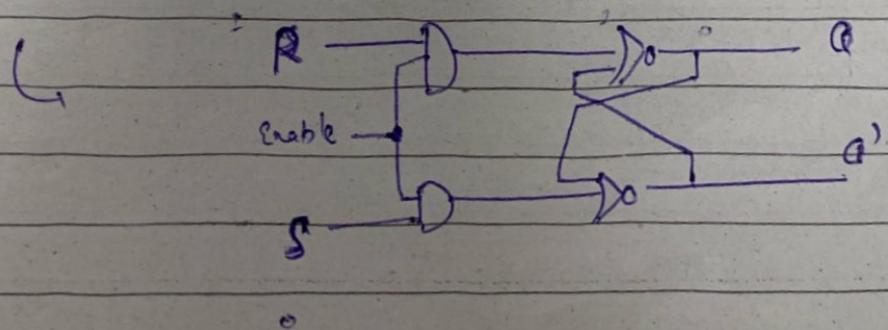
Invalid

Enabled SR latch

when enable is
low the latch
will retain its
previous state.



Active low



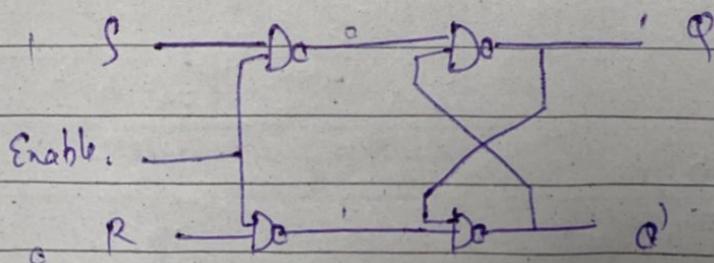
preinitiat

E	S	R	a	a'
0	X	X	NC	NC
1	0	0	NC	NC
1	0	1	0	1
1	0	0	1	0
1	1	1	0	0

\rightarrow Invalid

Coated catch using NANA
SR

Active High

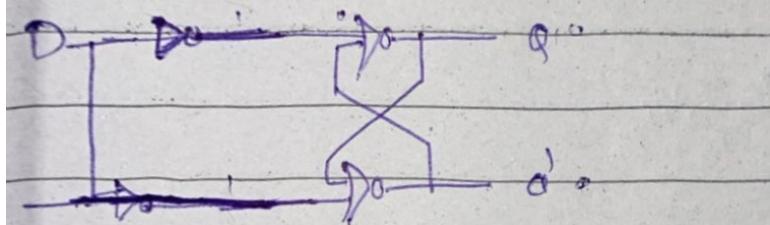
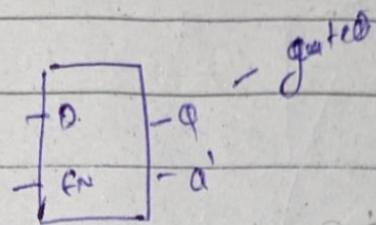
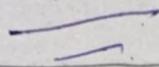


E S R a a'

some truth
table

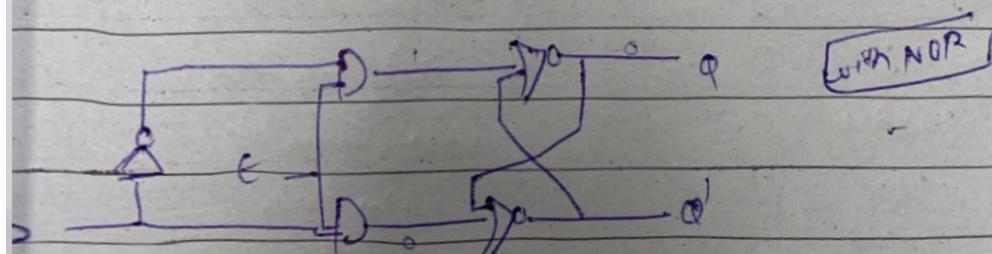
on Active low,

D-latch.



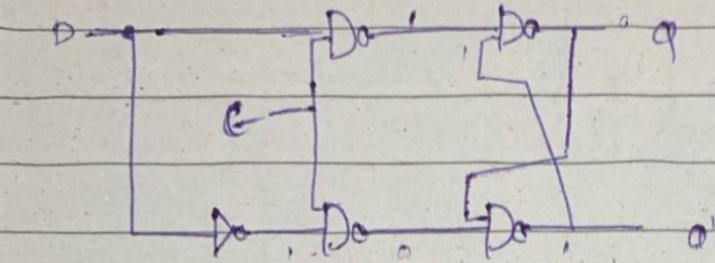
D	Q	Q'
0	0	1
1	1	0

Gated



E	D	Q	Q'
0	X	NC	NC
1	0	0	1
1	1	1	0

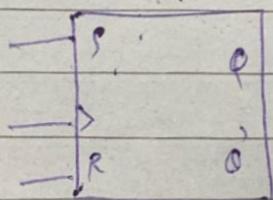
with NAND



Same truth table.

SR flip flops

small triangle
represent that it is
an edge triggered
flip flop



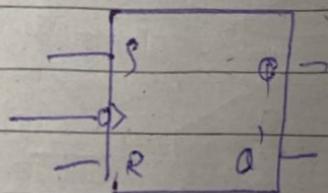
↓
if edge with no bubble

↓
positive
edge
triggered
flip flop

↓
if it is a negative

edge triggered

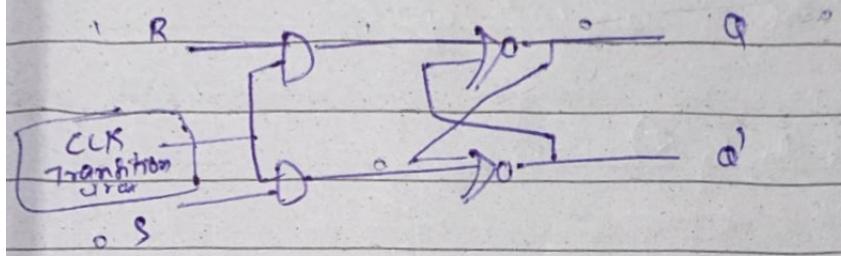
↑
flip flop



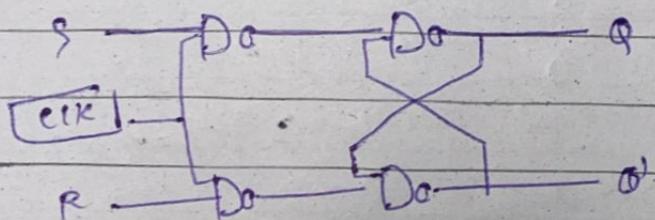
↓
negative
edge
triggered
flip flop

② Any circuit in place of enable at SR-gated can be converted into SR-flip flop

③ When there is no clk transition then output holds the present state.



Or,



positive edge triggered present state
negative edge triggered present state

clk	s	r	Qn	Qn+1	state
0	x	x	0	0	NC
↑	0	0	1	1	

↑	0	0	0	1	0 1	NC
---	---	---	---	---	--------	----

↑	0	1	0	1	0 0	RESET
---	---	---	---	---	--------	-------

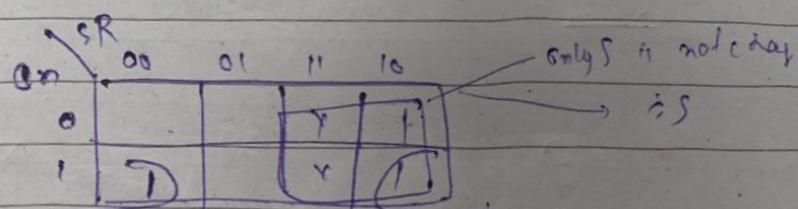
↑	1	0	0	1	1 1	SET
↓	1	1	0	0	0 1	INVALID

④ characteristic eq: of SR flip flop.

This eq shows the next state of the flip flop, in terms of the present state of the flip flop and the current input

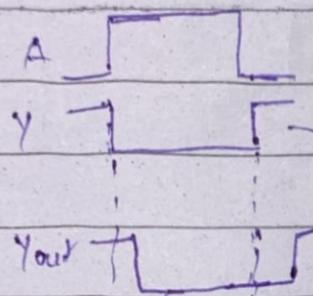
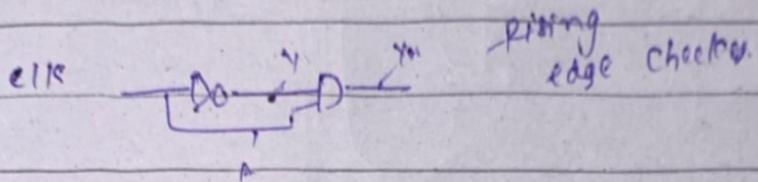
$$Q_{n+1} = F(Q_n, S, R)$$

Q_n	S	R	Q_{n+1} (Next state)
0	0	0	0] NC
1	0	0	1]
0	0	1	0] RESET
1	0	1	0]
0	1	0	1] SET
1	1	0	1]
0	1	1	X] X
1	1	1	don't care.

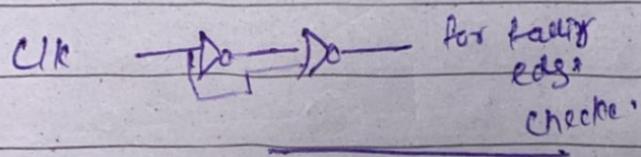


$$Q_{n+1} = S + Q_n R'$$

clock transition detector circuit



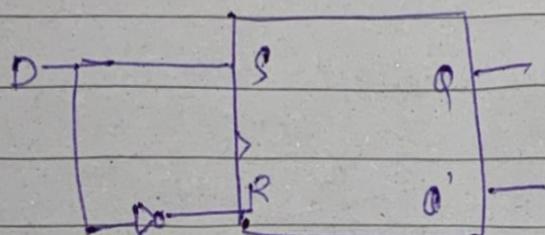
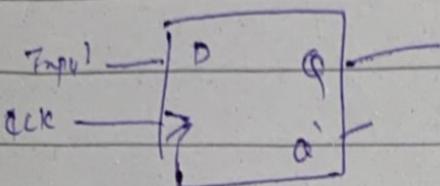
Yout will get shift little bit.



② for using this flip flop we need to ensure that the inputs S & R both do not become 1 at a time because if will then lead to indeterminate case, (which is not possible in SR) that's why this is preferred in sequential circuit, else D, JK or T flip flops are preferred

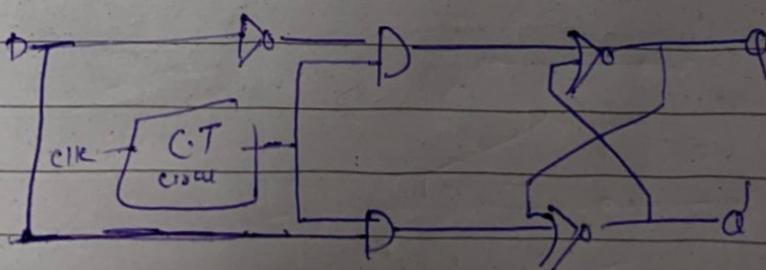
used in registers & counters

D-flip flop

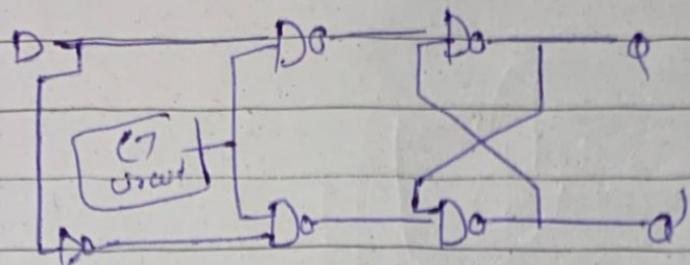


clk	D	S	R	Qn	Qn+1
0	x	x	x	0	0
				1	1
↑	0	0	1	0	0
↑	1	1	0	1	1

D-flip flop



Q2



Characteristic Eqn:

$$Q_{n+1} = F(Q_n, D)$$

Q_n	D	Q_{n+1}
0	0	0
1	0	0
0	1	1
1	1	1

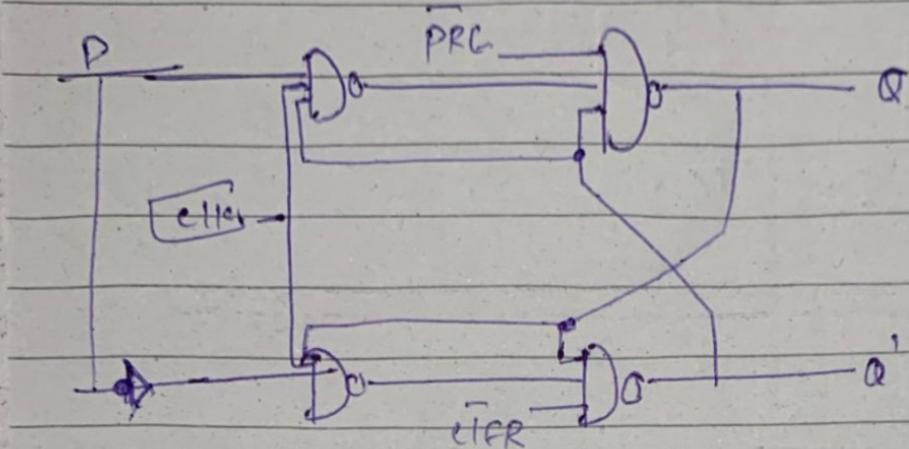
$$Q_{n+1} = D$$

PRE & CLR activation
both can't become
low simultaneously.

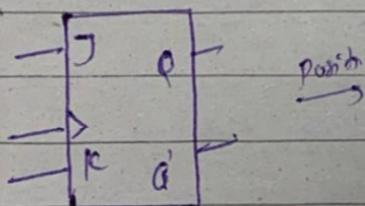
D-Flipflop with preset & clear input

D	Clk	PRE	CLR	α	Q'	Q	Notes
-	-	↓	↓	1	1	1	Error state
-	-	↑	↓	0	1	1	Defined state
-	-	↓	↑	1	0	0	0
0	↓	↑	↑	x	x	x	NO change
0	↑	↑	↑	0	1	1	RESET
1	↑	↑	↑	1	0	0	SET

④ if clear input is 0 then state is RESET
 if PRC input is 0 then state is SET
 ↓
 clear = 1

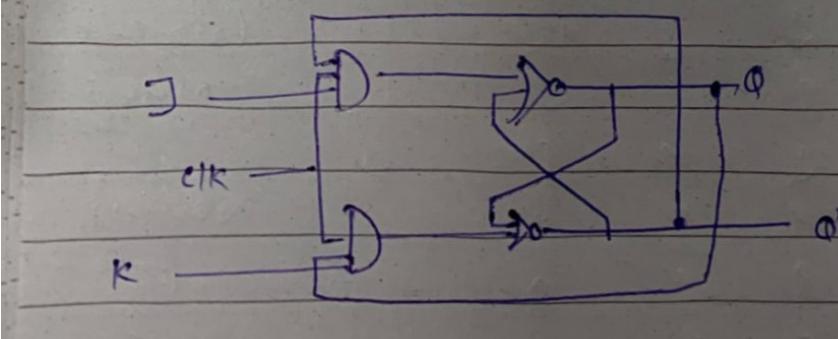


JK flip flop.

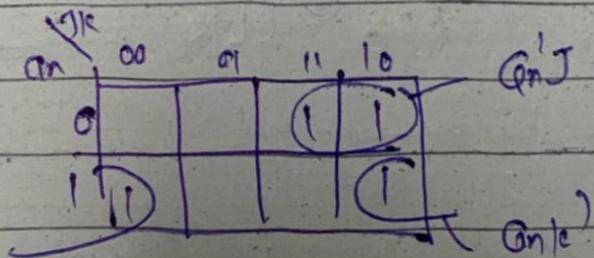


clk	J	K	Q _{n+1}
0	0	1	Q _n
1	0	0	Q _n
↑	0	1	Q _{n+1}
↑	1	0	1
↑	1	1	Q _{n+1}

Toggle state



α_n	J	K	α_{n+1}
0	0	0	0
1	0	0	\underline{I}_{m_1}
0	0	1	0
1	0	1	0
0	1	0	\underline{I}_{m_2}
1	1	0	\underline{I}_{m_3}
0	1	1	\underline{I}_{m_3}
1	1	1	0



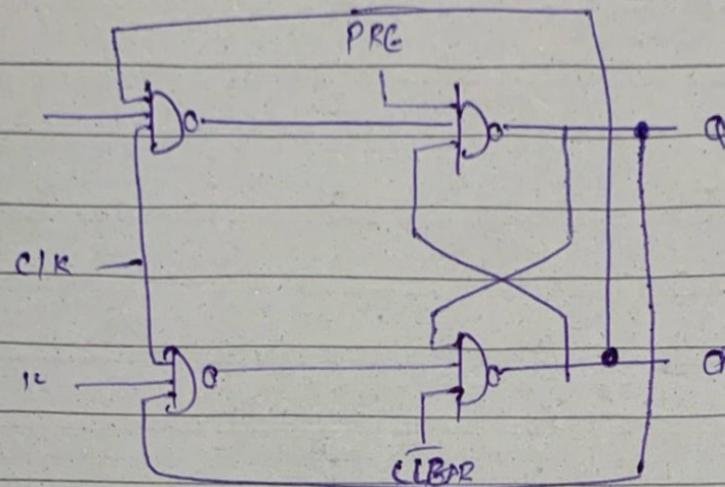
characteristic eq = $\alpha_n^J + \alpha_{n+1}^J$

alpha_{n+1}

↑
↓
↓

↓ all 10th of
in 74-73 (JK)
if have only CLR

④ JK flip flop with clear input & PRF



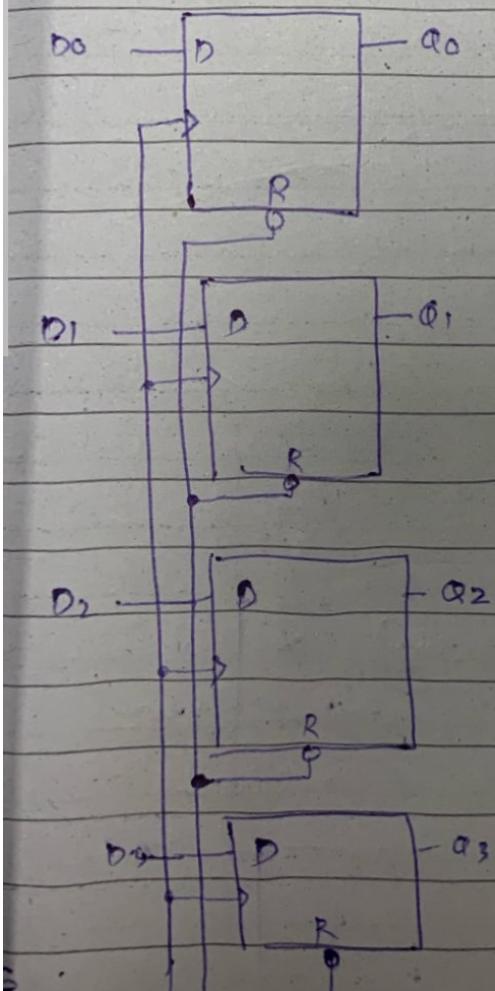
~~J K CLR PRF CLK Q_{n+1}~~

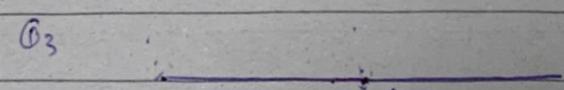
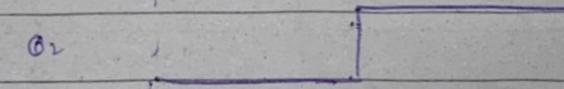
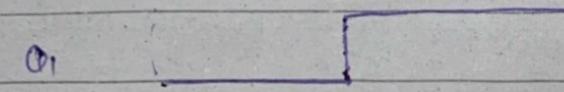
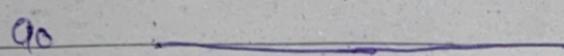
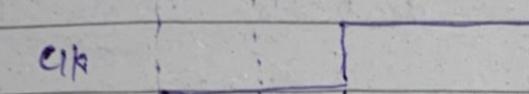
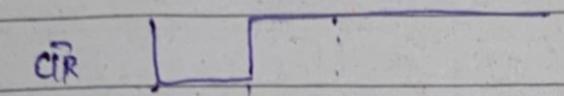
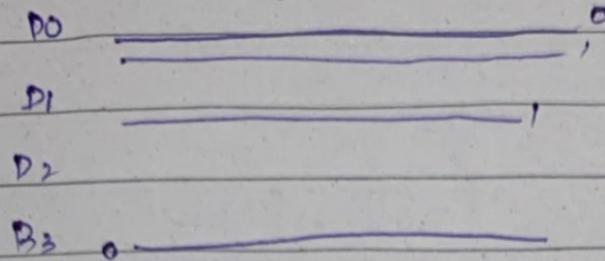
PRF	CLEAR	CLK	J	K	cont	Q _{n+1}
0	1	x	x	x	1	0
1	0	x	x	x	0	1
0	0	x	x	x	-	-
1	1	1	0	0	Q _n	Q _n
1	1	1	0	1	0	1
1	1	1	1	0	1	0
1	1	1	1	1	<u>Q_n</u>	<u>Q_n</u>
1	1	0	x	x	Q _n Lossless	Q _n

Flip Flop Applications.

① Parallel Data Storage.

- ① 4 bit parallel device using 4 D flipflops (can be extended)
- ② asynchronous reset R inputs are connected to a common CLR to reset all flipflops (deutned) CLK
- ③ each flipflop triggered by same CLK pulses, all outputs are acquired simultaneously





→ Clk edges
→ Data stored.

⑧ Frequency Divider

- ① Flip flop is dividing (reducing) the frequency of a periodic wave form, when a pulse waveform is applied to the clock input

of a D or JK flip flop that is connected to totole ($D = \bar{Q}$ or $J = K = 1$). the Q output is square wave with one half the frequency of the clock input. Thus, a single flip flop can be applied on a divide by 2 device.

