INFORMATION TECHNOLOGY UNIVERSITY, LAHORE, PAKISTAN

Department of Computer Engineering

# Digital Logic Design (CE-201T)

## Final Exam, Fall 2022

Time Allowed: 3 Hours | December, 2022 | Marks: 100

Name: Zainab Bashir Roll Number: BSCE21013

**Instructions:**

- **This Midterm Exam will access your CLOs as per OBE.**
- Use only BLACK or BLUE ink pen.
- Write down your roll number on each page at the top in the given space.
- Use only the given space to solve the problem and write down your answers.
- Use pencils to draw the circuit diagrams.
- Manage your allotted time with care as you have limited time to solve the paper.
- It is a **closed book/closed notes exam**; so you must not have any material with you during this exam.
- If any student is found cheating or helping any other student, his/her exam will be cancelled and the case will be forwarded to Disciplinary Committee for further action.

**CLOs**

1. Apply the concept of different number systems and representations, to perform number system conversions and arithmetic operations.
2. Apply the concepts of Boolean algebra and logic simplification to realize simplified designs of combinational and sequential circuits.
3. Demonstrate the design of sequential circuits from their respective finite state machine representations.

**Marks Distribution**

| Q. No. | CLO | Marks | Marks Obtained |
|---|---|---|---|
| 1 | 1 | 20 | 20 |
| 2 | 2 | 20 | 20 |
| 3 | 2 | 20 | 20 |
| 4 | 3 | 20 | 18 |
| 5 | 3 | 20 | 19 |
| 6 | 3 | 20 | 20 |
| 7 | 3 | 20 | 19 |
| Total | - | 140 | 136 |

Instructor's Name: Aftab Alam Signature: Aftab Alam

1. [CLO1]

(a) Convert the hexadecimal number $(4AC)_{16}$ into binary, octal and decimal. Show your work. [6]

base 2 | base 8 | base 10

4 A C | 010010101100 | $(4\times16^2)+(10\times16^1)+(12\times16^0)$

0100 1010 1100 | 2 2 5 4 | $=1196$

A 10
B 11
C 12
D 13
E 14
F 15

$(4AC)_{16} = (010010101100)_2 = (2254)_8 = (1196)_{10}$

(b) What is the decimal equivalent of the binary number 10010110 if it has been encoded as [6]

i. an 8-bit unsigned number

$(10010110)_2$

$=(150)_{10}$

ii. an 8-bit signed number (represented in 2's complement form).

128 64 32 16 8 4 2 1

10010110
01101001
+1
01101010 $=106$

128 − 127

$=(-106)_{10}$

iii. a BCD number

1001 0110

9 6

$=96$

(c) A digital system uses even parity for error detection. What parity bit will be appended to the 7-bit number 1101001 using this scheme? [2]

1101001

parity bit $=0$

8-bit num $=01101001$

2

(d) Show the addition of the two hexadecimal numbers 3999 and A803. [2]

2/

```
 3999
 A803
------
 E19C
```

14745
43011
57756
E19C

rough.

(e) The following arithemtic operation is correct in at least one number system. Determine the possible radices of the numbers in each operation. [4]

i. $\sqrt{41} = 5$
ii. $\frac{41}{3} = 13$

4/

(i) $\sqrt{41} = 5$

$(4r+1)^{1/2} = 5$

$\Rightarrow \sqrt{4r+1} = 5$

$4r+1 = 5^2$

$4r+1-5^2 = 0$

$4r-24 = 0$

$r = 6$

it is in base 6 number system

$(4\times6)+1 = 25$

$5 = 5$

(ii) $(41) = (13\times3)$

$4\times r+1 = ((1\times r)+3)(3)$

$4r+1 = (r+3)(3)$

$4r+1 = 3r+9$

$4r-3r = 9-1$

$r = 8$

it is in octal number system.

2. [CLO2]

(a) Write down the function F (Figure 1(a)) in Π notation (Product of Maxterms form) and the function G (Figure 1(b)) in Σ notation (Sum of Minterms form). [10]

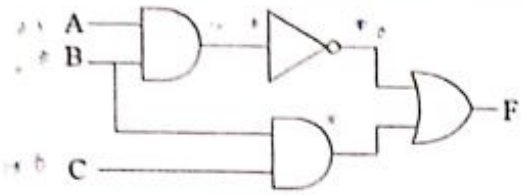



Figure 1(a)

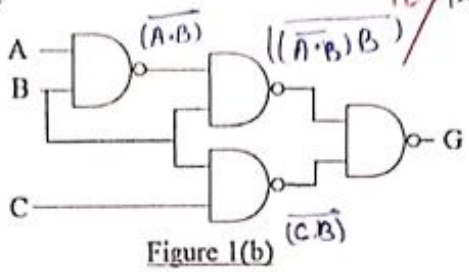



Figure 1(b)

$F = (\overline{AB}) + (BC)$

| A | B | C | F |
|---|---|---|---|
| 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 |

$F = \Pi M(6)$

$F = (\overline{A} + \overline{B} + C)$

$G = \left(\overline{((\overline{AB})B)(\overline{CB})}\right)$

| A | B | C | $\overline{AB}$ | $\overline{\overline{AB}B}$ | $(\overline{CB})$ | G |
|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 1 | 1 | 1 | 0 |
| 0 | 0 | 1 | 1 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 1 | 0 | 0 | 1 |
| 1 | 0 | 0 | 1 | 1 | 1 | 0 |
| 1 | 0 | 1 | 1 | 1 | 1 | 0 |
| 1 | 1 | 0 | 0 | 1 | 0 | 0 |
| 1 | 1 | 1 | 0 | 1 | 1 | 1 |

$G = \overline{A}B + CB$ (After simplification)

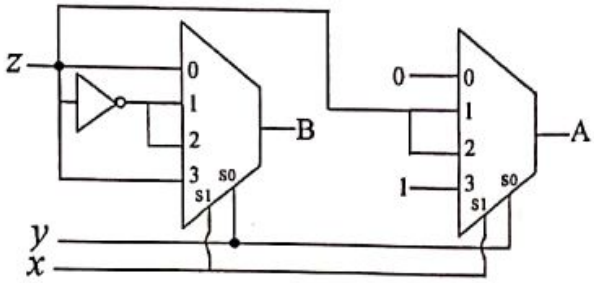
$G = \Sigma m(2,3,7)$

$G = (\overline{A}B\overline{C}) + (\overline{A}BC) + (ABC)$

(b) Draw the truth table for the circuit shown in Figure 2 with $x, y$ and $z$ as the inputs and A and B as the outputs. Which device is implemented using MUXs in Figure 2? Justify. [6+4]

10

Figure 2




| x | y | z | A | B |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 1 |
| 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 1 | 1 |

The function implemented is a full adder with B as the sum and A as the carry out.

e.g m(4)

x y z
1 0 0

S = 1 | B = 1
C = 0 | A = 0

m(7)

x y z
1 1 1

sum = 1 | B = 1
cout = 1 | A = 1

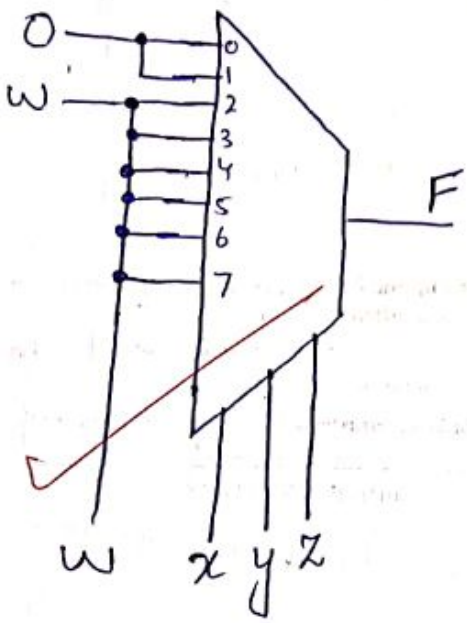
5

3. [CLO2]

(a) A BCD code is being transmitted to a remote receiver. The bits are $w, x, y and z$ with $w$ as the Most Significand Bit. Design a BCD error detector circuit at the receiver that examines the BCD code to see if it is a legal BCD code. Implement your circuit using 8 x 1 Multiplexer. [10]

10

| W | x | y | z | F |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 1 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 0 | 1 | 1 | 1 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 0 | 1 | 1 |
| 1 | 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 |




$F = wx + wy$

The output alerts if the BCD code is illegal.

| x | y | z | F |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 3 |
| 0 | 1 | 1 | 3 |
| 1 | 0 | 0 | 3 |
| 1 | 0 | 1 | 3 |
| 1 | 1 | 0 | 3 |
| 1 | 1 | 1 | 2 |

(b) What are the values of F1 and F2 in the PLA of Figure 3 in Sum of Products form. Show the ROM Implementation of F1 and F2. What is the size of the ROM used? [4+4+2]

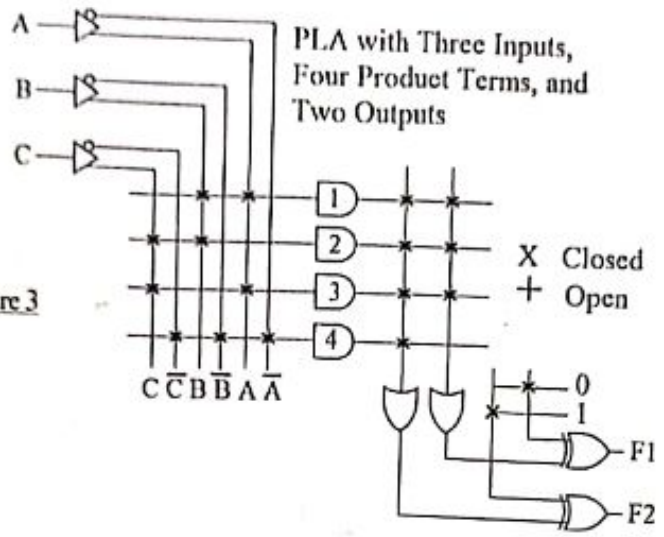



Figure 3

$F_1 = AB + CB + CA$

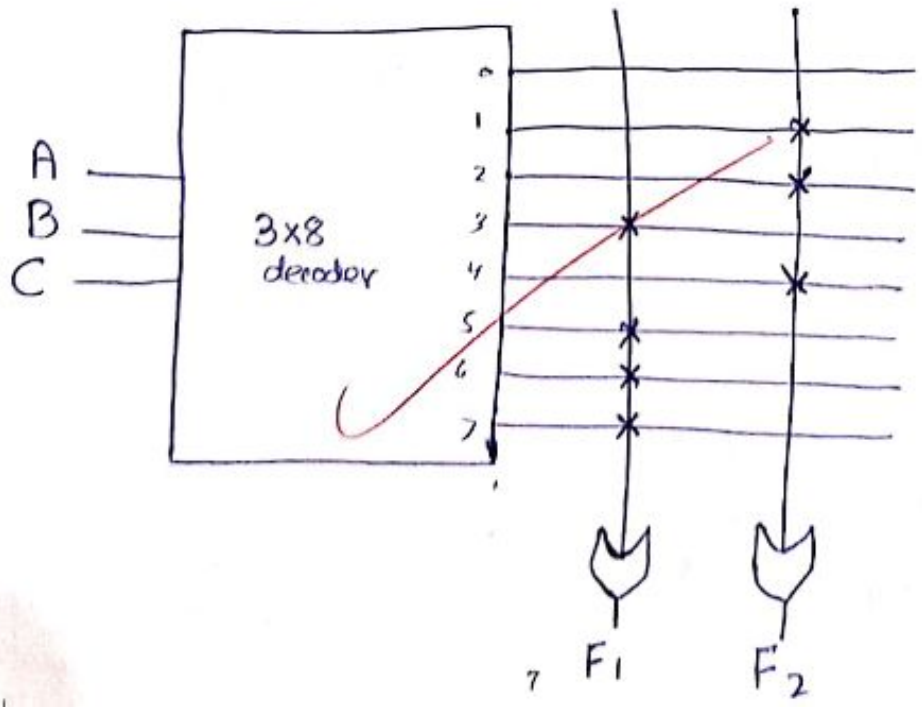
$F_1 = \Sigma m(3,5,6,7)$

$F_2 = (AB) + (CB) + (CA) + (\bar{C}\bar{B}\bar{A})$

$F_2 = (\bar{A}\bar{B}C) + (A\bar{B}\bar{C}) + (\bar{A}B\bar{C})$

$F_2 = \Sigma m(1,2,4)$

ROM implementation




=> A rom of size 8x2 is required to implement these 2 Functions.

4. [CLO3]

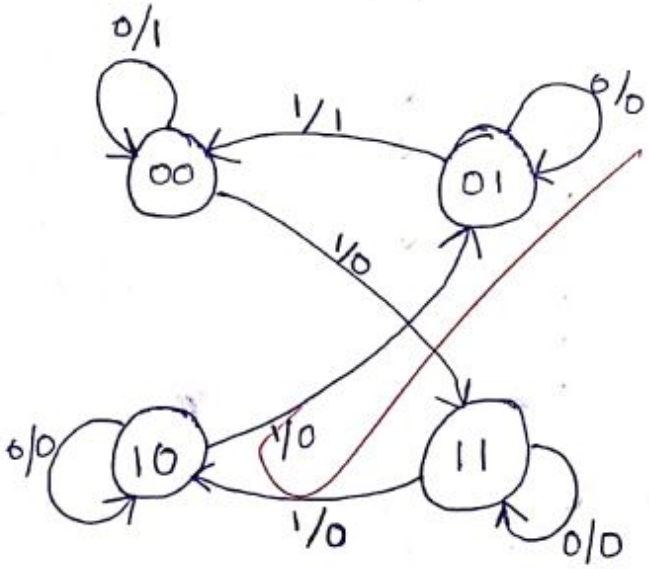
(a) A sequential circuit with two JK flip-flops A and B and one input X, and one output Z is specified by the following input and output equations:

$J_A = \overline{B}X, \quad K_A = \overline{B}X, \quad J_B = X, \quad K_B = X, \quad Z = \overline{A}.(\overline{B \oplus X})$

i. Derive the state table. [4]
ii. Derive the state diagram. [4]
iii. What is the function of the circuit? Describe in your words. [2]

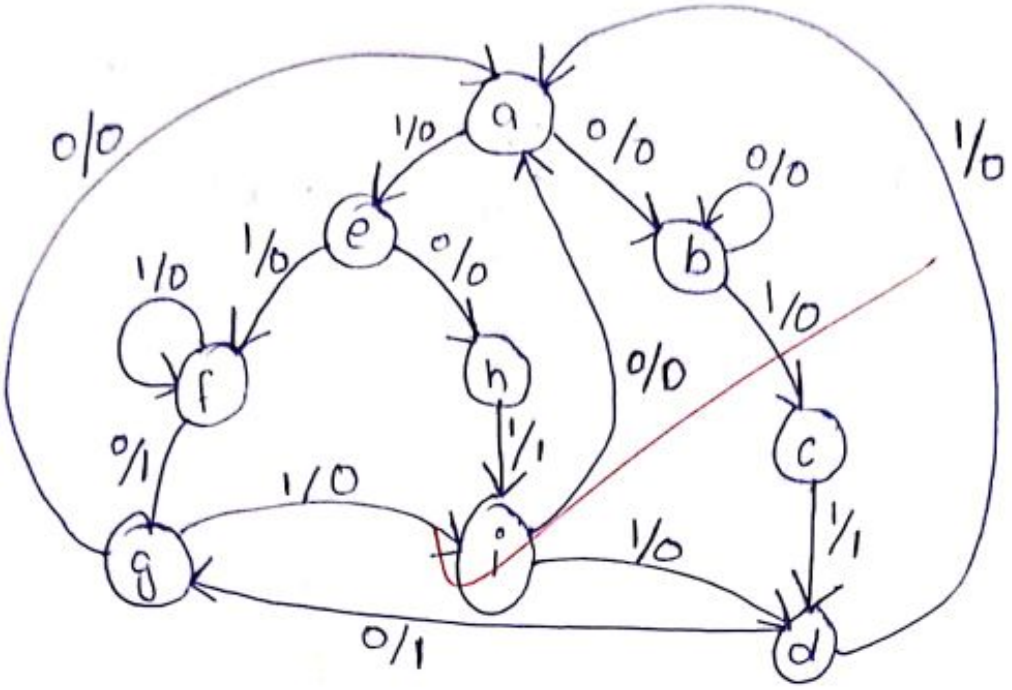
10

| P.S | | input | inp A f/F | | inp B F/F | | N. S | | output |
|---|---|---|---|---|---|---|---|---|---|
| A(t) | B(t) | X | $J_A$ | $K_A$ | $J_B$ | $K_B$ | A(t+1) | B(t+1) | Z |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| 1 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |
| 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 |




The Function is a reverse counter it counts for the sequence 3,2,1,0 with every input is 1. when input is 1 the counter count downwards and when the sequence is completed 3,2,1,0 and 0 state is reached again it gives output 1 and untill the new sequence is started. it gives 1 on output only when next state is 0 again.

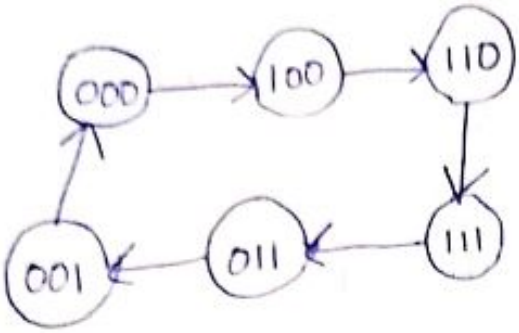
(b) Draw the state diagram of a circuit that outputs a 1 when exactly two of the last three serial inputs are 1. e.g., the input sequence of 011011100 produces an output sequence of 001111010. [10]



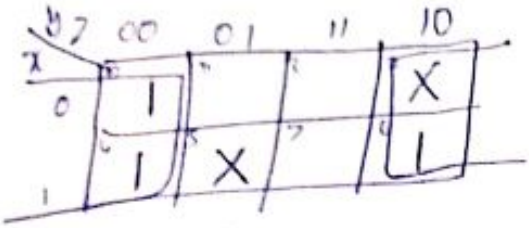

No. of states can be reduced as these are redundant states.

5. [CLO3]

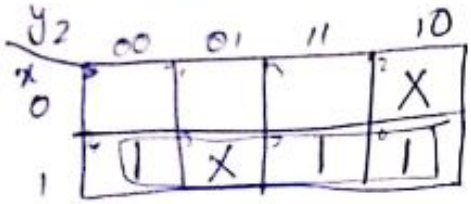
(a) The Johnson counter advances through the sequence 000, 100, 110, 111, 011, 001 and repeat. Design Johnson counter using D flip-flops. Consider unused states as don't cares. Is your counter self-starting? (Show your work) [10]



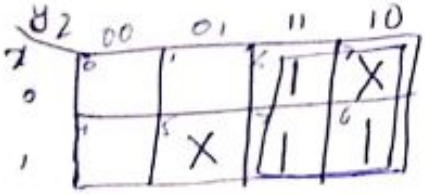

| P.S | | | N.S | | | F/F ipts | | |
|---|---|---|---|---|---|---|---|---|
| x | y | z | x+ | y+ | z+ | $D_A$ | $D_B$ | $D_C$ |
| 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | x | x | x | x | x | x |
| 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 1 |
| 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | x | x | x | x | x | x |
| 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |
| 1 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 |



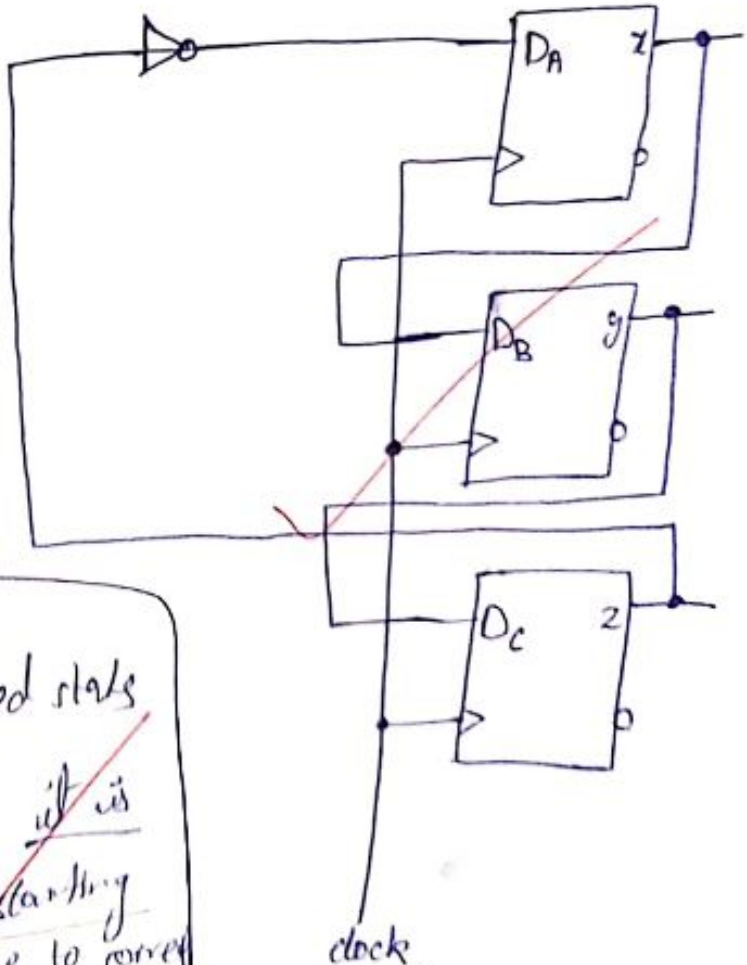

$D_A = \overline{z}$




$D_B = x$




$D_C = y$




if $xyz = 010$

$x^+y^+z^+ = 101$

$xyz = 101$

$x^+y^+z^+ = 010$

so for unused state


if it is not a self starting counter we have to correct it by taking valid input instead of don't cares.

(b) Design a register cell of an 8-bit register B having following register transfer functions: [10]

$C_0 : B \leftarrow A \wedge B$

$C_1 : B \leftarrow A \vee \overline{B}$

$C_2 : B \leftarrow \overline{B}$

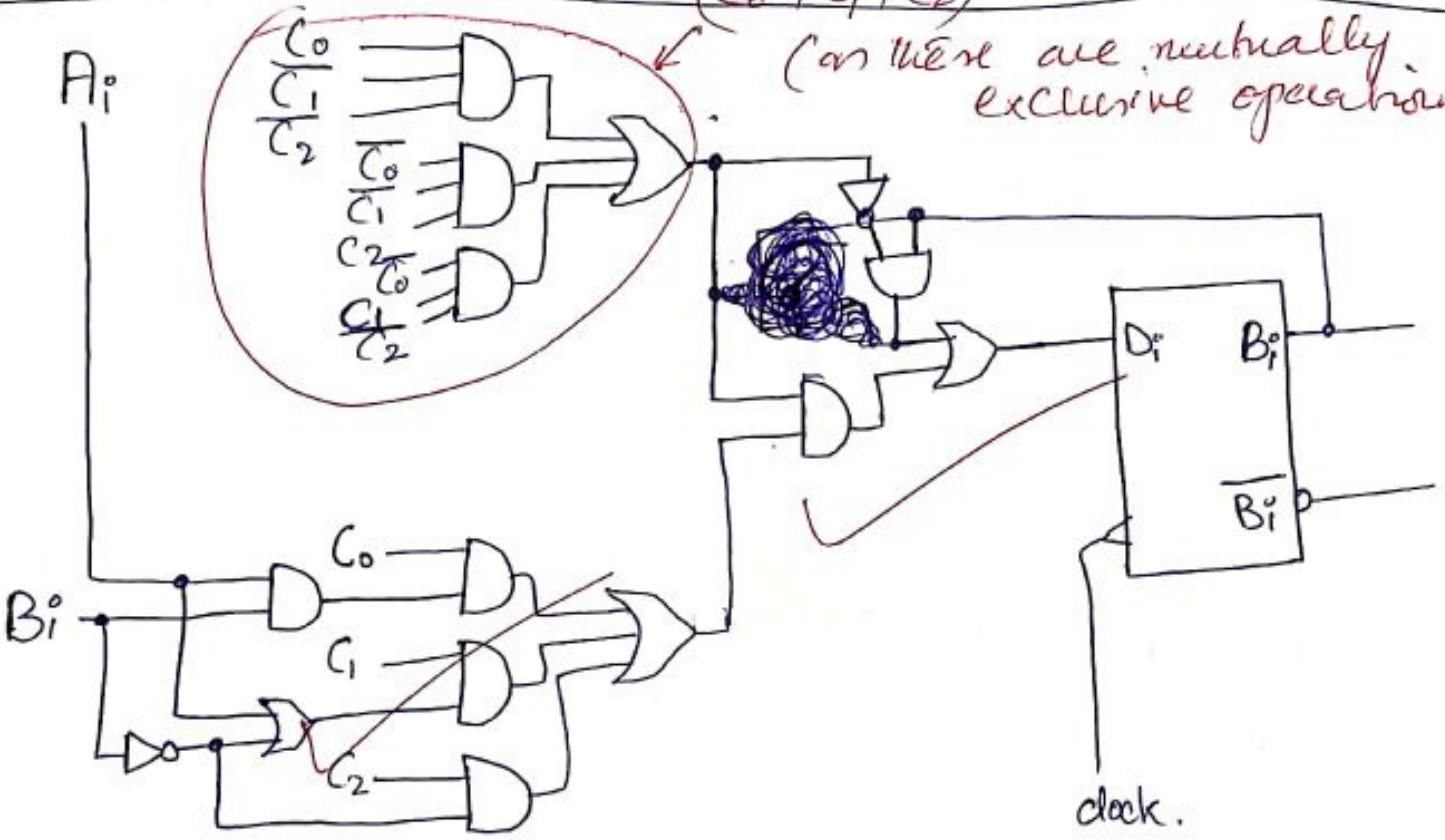
transfer operation is performed only when when of th three control inputs is one other wise data remain same.

$$B_i = C_0(A_i B_i) + C_1(A + \overline{B}) + C_2(\overline{B})$$

$$load = C_0\overline{C_1}\,\overline{C_2} + \overline{C_0}\,\overline{C_1}C_2 + \overline{C_0}C_1\overline{C_2}$$

$(C_0 + C_1 + C_2)$

(as there are mutually exclusive operations).



6. [CLO3]

(a) How many address lines and how many data lines a 64M x 8 DRAM chip has? [5]

5/

As $2^{26} = 64M$

So a 64M x 8 DRAM has 26 address lines and 8 data lines

(b) A 4 GB DRAM uses 4-bit data and has equal-length row and column addresses. How many address pins does the DRAM have? [5]

5/

32G bits where 4bit data

so $\frac{2^{35}}{2^2} = 2^{33}$

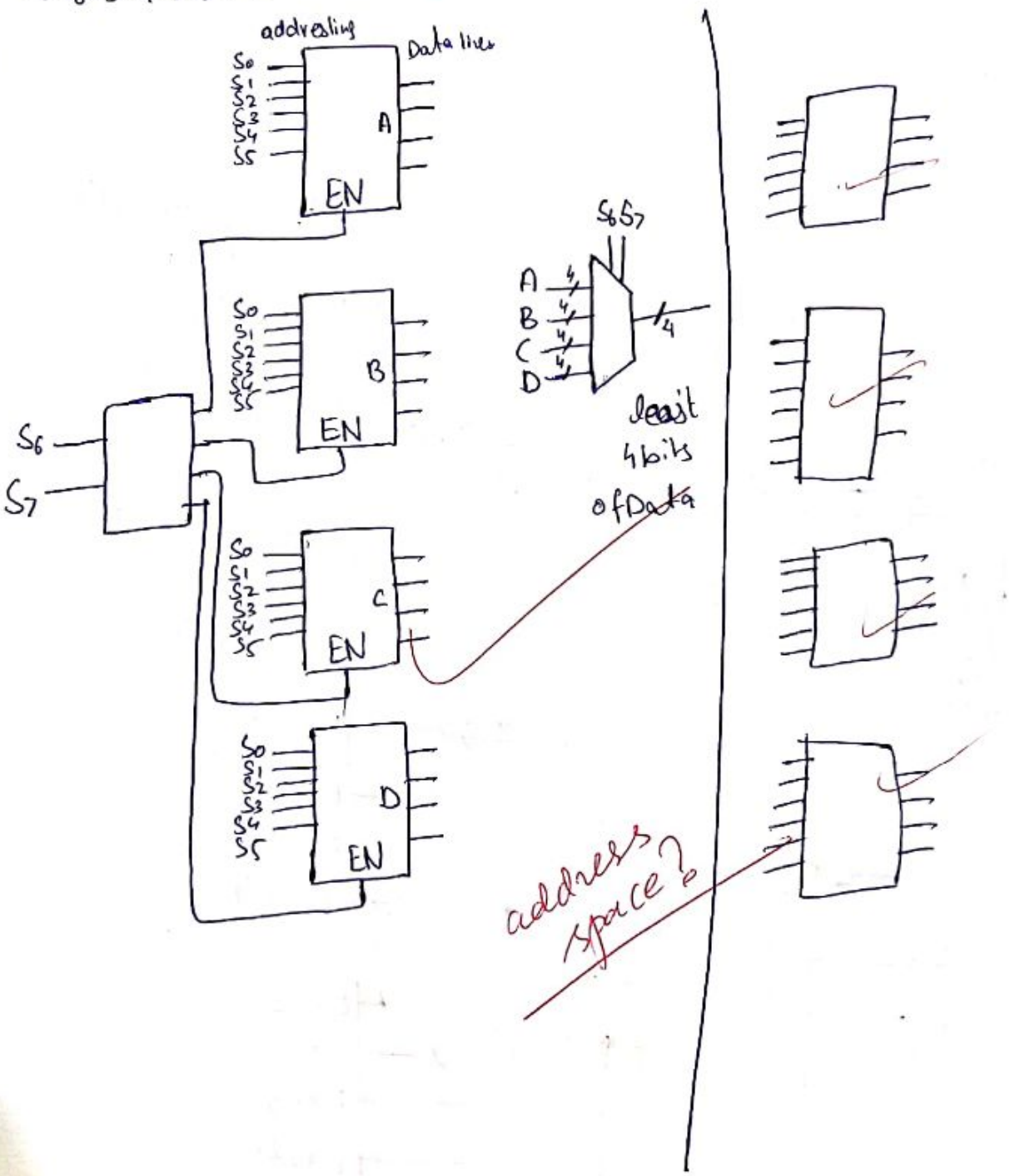
so it have 33 address lines each address having 4 bit of data.

(c) How many 64■ × 4 RAM chips (with enable input) are needed to construct a 256 × 8 RAM? Show the external connections. Also mention the address space of each RAM chip. [10]
**Hint:** Use decoder.

10

total 8 64x4 RAM chips would be used.

$S_7\ S_6\ S_5\ S_4\ S_3\ S_2\ S_1\ S_0$



7. [CLO3]

(a) The following register transfer operations will be implemented where K1, K0 are two input Boolean variables: [10]

$\overline{K1}.\overline{K0}$: $R1 \leftarrow R2$

$\overline{K1}.K0$: $R2 \leftarrow R3$

$K1.\overline{K0}$: $R3 \leftarrow R2$

$K1.K0$ : $R1 \leftarrow R4$

All four n-bit registers R1, R2, R3, and R4 have three-state bi-directional input/output lines connecting to a single shared bus as shown in the Figure 4 below. Find the values of the the control signals Loads and ENs of the registers (i.e., Load1, Load2, Load3, Load4, EN1, EN2, EN3 and EN4) so that the above conditional register transfer operations can be realized. Note that Loads and ENs are functions of K1 and K0.

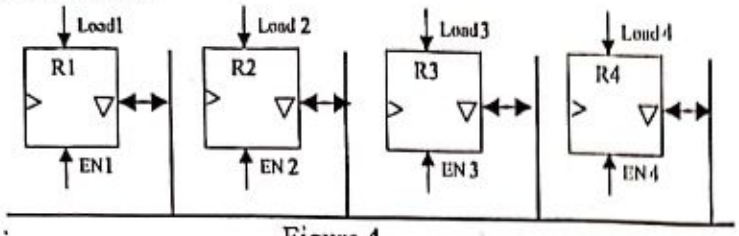



Figure 4

Load1 = $(\overline{K_0}\overline{K_1}) + (K_0K_1)$
$= \overline{(K_0 \oplus K_1)}$

Load2 = $\overline{K_1}K_0$

Load3 = $K_1\overline{K_0}$

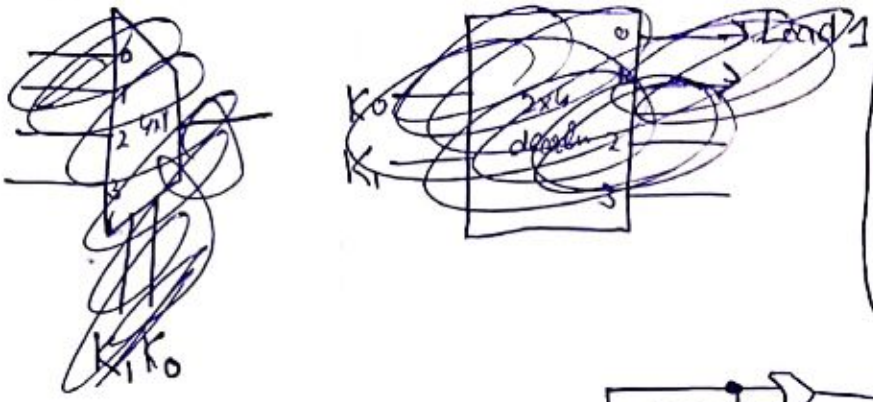
Load4 = 0

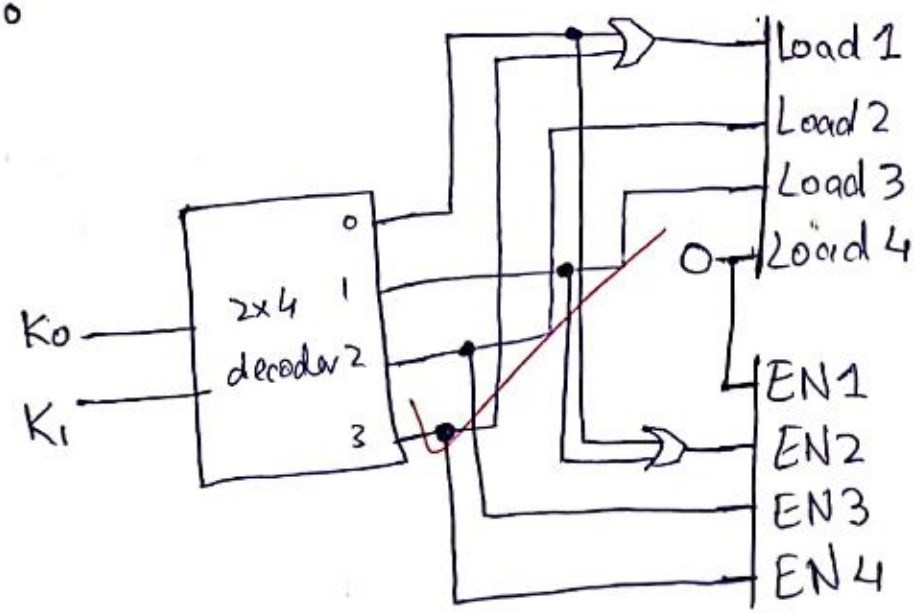
EN1 = 0 $= \overline{K_0}$

EN2 = $(\overline{K_1}\,\overline{K_0}) + (K_1\overline{K_0})$

EN3 = $(\overline{K_1}K_0)$

EN4 = $(K_1K_0)$



(b) Draw the logic diagram of a 4-bit register (using D flip-flops) with mode selection inputs S1 and S0. The register is to be operated according to the following function table: [10]

10

| S1 | S0 | Register Operation |
|---|---|---|
| 0 | 0 | Complement Output |
| 0 | 1 | Clear Register to 0 |
| 1 | 0 | No Change |
| 1 | 1 | Load Parallel Data |