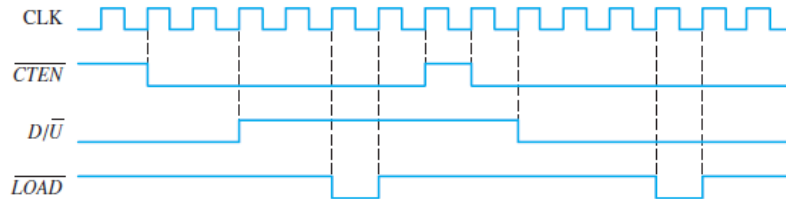
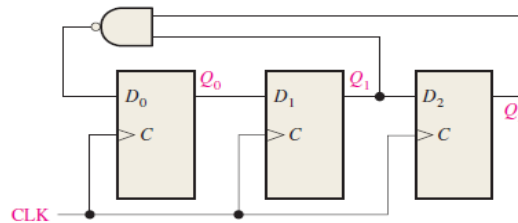


(Practice Questions)

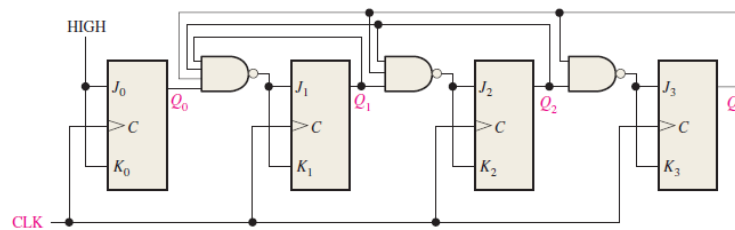
1. Show a complete timing diagram for a 3-bit up/down counter that goes through the following sequence. Indicate when the counter is in the UP mode and when it is in the DOWN mode. Assume positive edge-triggering. 0, 1, 2, 3, 2, 1, 2, 3, 4, 5, 6, 5, 4, 3, 2, 1, 0
2. Develop the Q output waveforms for a 74HC190 up/down counter with the input waveforms shown in Figure. A binary 0 is on the data inputs. Start with a count of 0000.



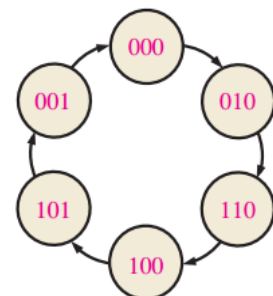
3. Repeat above Problem if the CTEN is inverted with the other inputs the same.
4. Determine the sequence of the counter in Figure.



5. Determine the sequence of the counter in Figure 9–74. Begin with the counter cleared.



6. Design a counter to produce the following sequence. Use J-K flip-flops. 00, 10, 01, 11, 00,
7. Design a counter to produce the following binary sequence. Use J-K flip-flops. 1, 4, 2, 5, 1, 6, 2, 1,
8. Design a counter to produce the following binary sequence. Use J-K flip-flops. 0, 9, 2, 8, 1, 5, 3, 7, 4, 5, 0, ...
9. Design a counter by using D -flip flop only with the irregular binary count sequence shown in the state diagram of Fig. Include Next-state table, transition table, Karnaugh maps and final circuit.



10. If a 5-bit ring counter has an initial state 10101, determine the waveform for each Q output
11. Design a modulus-10 Johnson counter using J K flip flop. Write the sequence in tabular form.