Digital Logic & Design

Assignment : 02

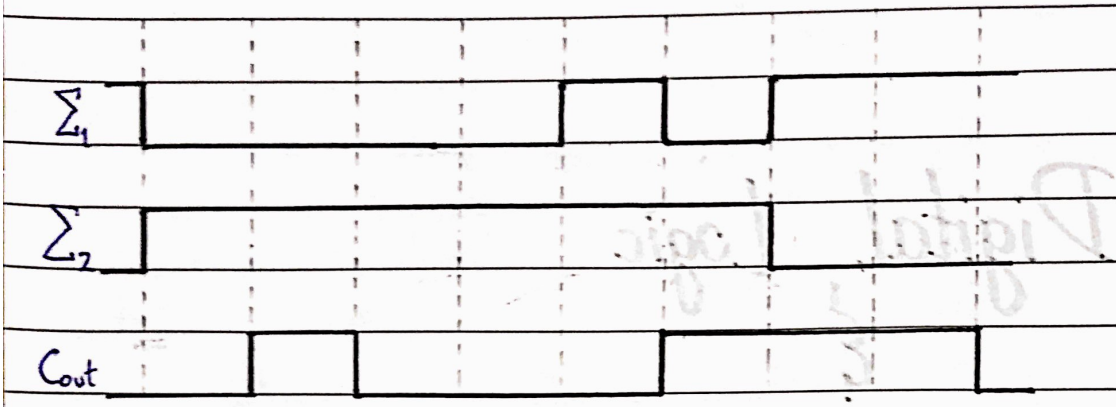
23K-2001

BCS-2J

Date _____

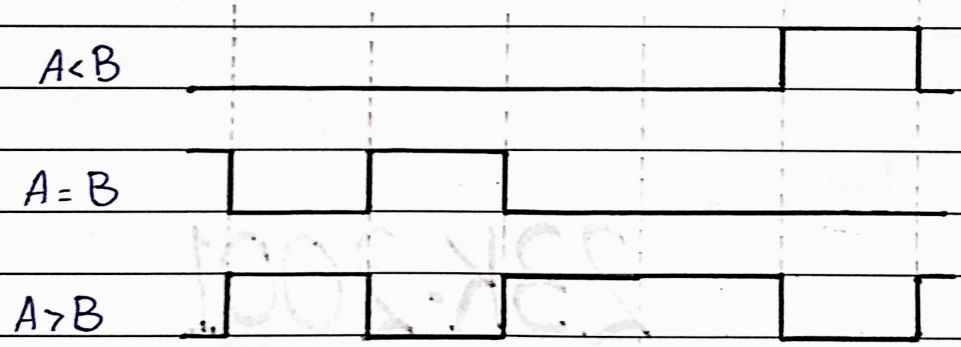
Answer #01:

Timing Diagram:



Answer #02:

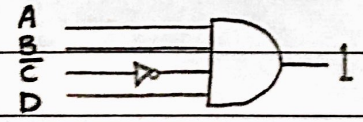
Timing Diagram:



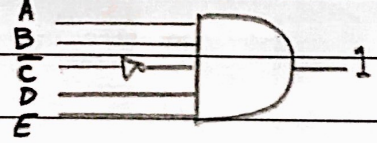
Answer #03:

Active High (1) Decoding logic

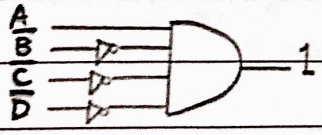
a. 1101



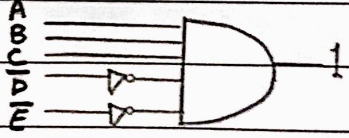
c. 11011



b. 1000



d. 11100



Date _____

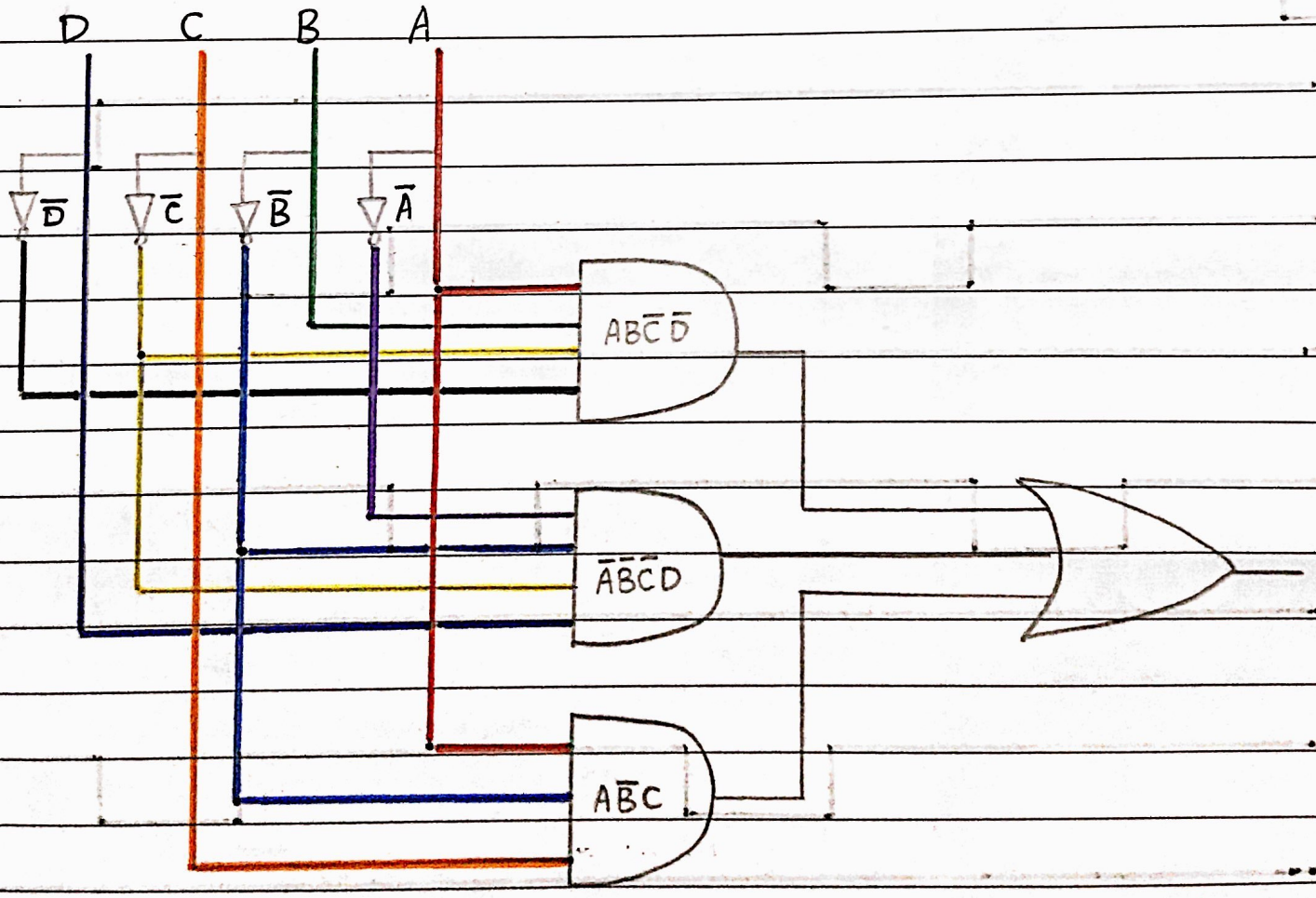
Answer #4:

Required: 1010, 1100, 0001, 1011

→ $A\bar{B}C\bar{D}$, $AB\bar{C}\bar{D}$, $\bar{A}\bar{B}\bar{C}D$, $A\bar{B}CD$

AB \ CD	00	01	11	10
00		1		
01				
11	1			
10			1	1

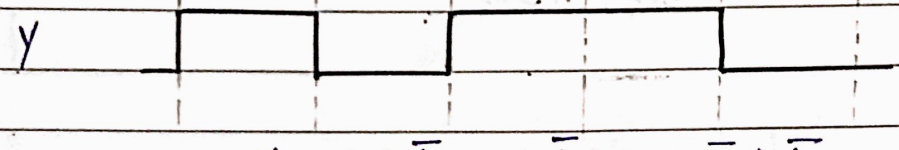
Minimized: $AB\bar{C}\bar{D} + \bar{A}\bar{B}\bar{C}D + A\bar{B}C$



Date _____

Answer #05

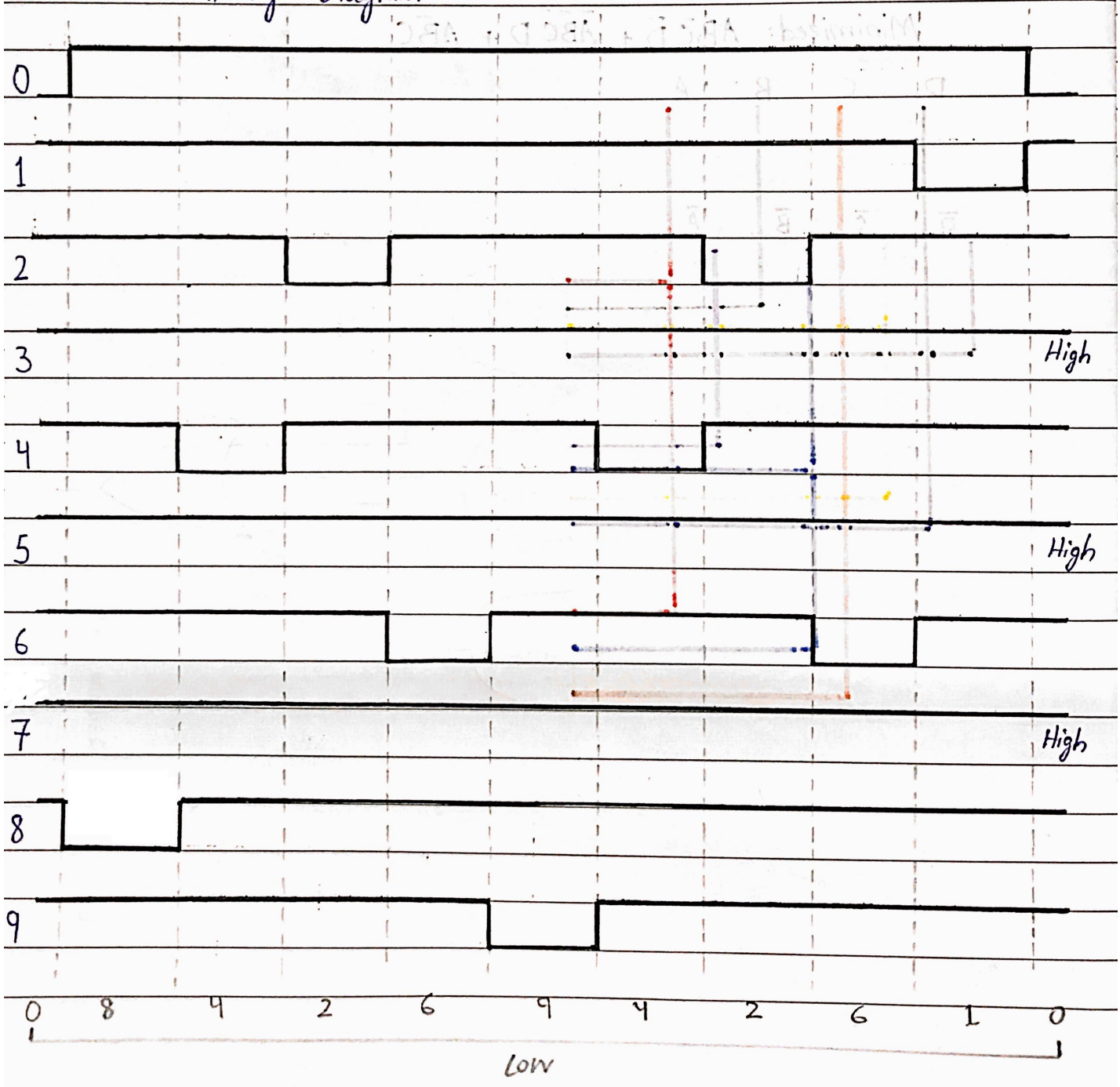
Timing Diagram:



$$Y = A_2 A_1 \overline{A_0} + A_2 \overline{A_1} A_0 + \overline{A_2} A_1 \overline{A_0}$$

Answer #06

Timing Diagram



Date _____

Answer #07

Output:

$A_3 A_2 A_1 A_0 = (1011)_2 \longrightarrow (11)_{10}$

$(1011)_2$ is an invalid BCD code.

Ans.

Answer #08

Only High outputs are :

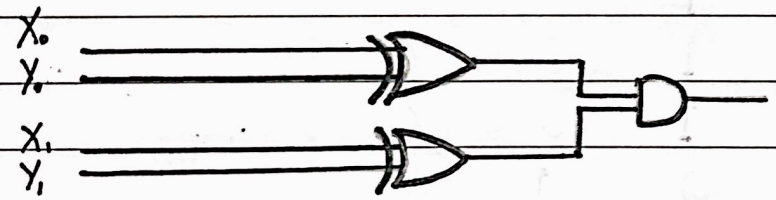
$A_1 A_0 \rightarrow X_1 X_0$	01	10	00	11
$B_1 B_0 \rightarrow Y_1 Y_0$	10	01	11	00

$\rightarrow \quad \bar{X}_1 X_0 Y_1 \bar{Y}_0 + X_1 \bar{X}_0 \bar{Y}_1 Y_0 + \bar{X}_1 \bar{X}_0 Y_1 Y_0 + X_1 X_0 \bar{Y}_1 \bar{Y}_0$

$X_1 \bar{Y}_1 (X_0 \bar{Y}_0 + \bar{X}_0 Y_0) + \bar{X}_1 Y_1 (X_0 \bar{Y}_0 + \bar{X}_0 Y_0)$

$(X_1 \bar{Y}_1 + \bar{X}_1 Y_1)(X_0 \bar{Y}_0 + \bar{X}_0 Y_0)$

$(X_1 \oplus Y_1)(X_0 \oplus Y_0)$, $\because [A \oplus B = \bar{A}B + A\bar{B}]$

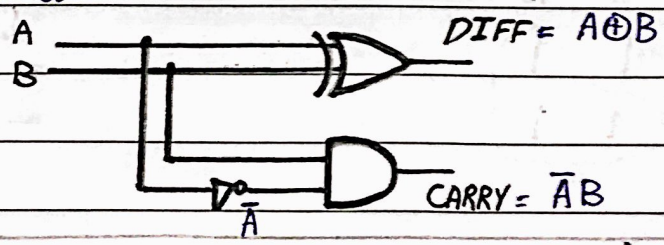


Answer #09

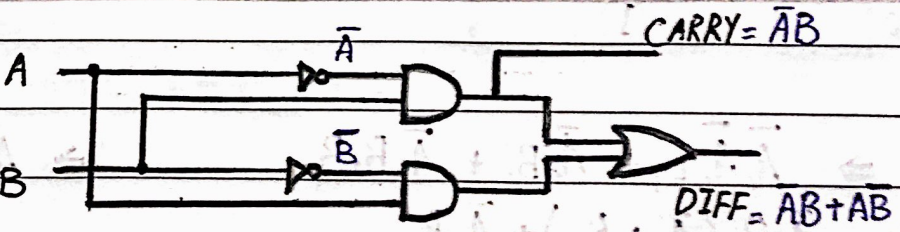
Half Subtractor:

A	B	DIFF	CARRY
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

i.



ii.



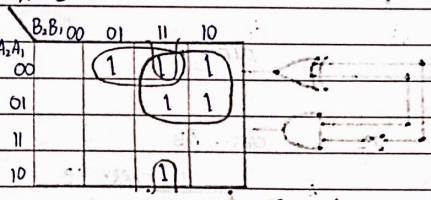
Date _____

Answer #10:

2-Bit Comparator

A_2	A_1	B_2	B_1	A>B	A=B	A<B
0	0	0	0	0	1	0
0	0	0	1	0	0	1
0	0	1	0	0	0	1
0	0	1	1	0	0	1
0	1	0	0	1	0	0
0	1	0	1	0	1	0
0	1	1	0	0	0	1
0	1	1	1	0	0	1
1	0	0	0	1	0	0
1	0	0	1	1	0	0
1	0	1	0	0	1	0
1	0	1	1	0	0	1
1	1	0	0	1	0	0
1	1	0	1	1	0	0
1	1	1	0	1	0	0
1	1	1	1	0	1	0

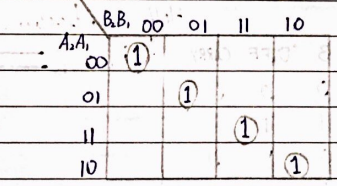
A < B :



$\Rightarrow \overline{A_2}\,\overline{A_1}B_1 + \overline{A_2}B_2 + \overline{A_1}B_2B_1$

$\Rightarrow \overline{A_1}B_1(\overline{A_2}+B_2) + \overline{A_2}B_2$

A = B :



$\Rightarrow A_1A_1B_2B_1 + \overline{A_2}\,\overline{A_1}\,\overline{B_2}\,\overline{B_1} + \overline{A_2}A_1\overline{B_2}B_1 + A_2\overline{A_1}B_2\overline{B_1}$

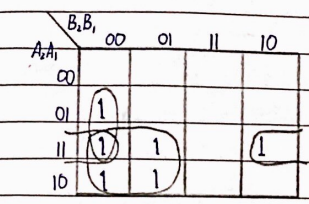
$\Rightarrow \overline{A_2}\,\overline{B_2}(\overline{A_1}\,\overline{B_1} + A_1B_1) + A_2B_2(A_1B_1 + \overline{A_1}\,\overline{B_1})$

$\Rightarrow (\overline{A_1}\,\overline{B_1} + A_1B_1)(\overline{A_2}\,\overline{B_2} + A_2B_2)$

$\Rightarrow (\overline{A_1 \oplus B_1})\,(\overline{A_2 \oplus B_2})$

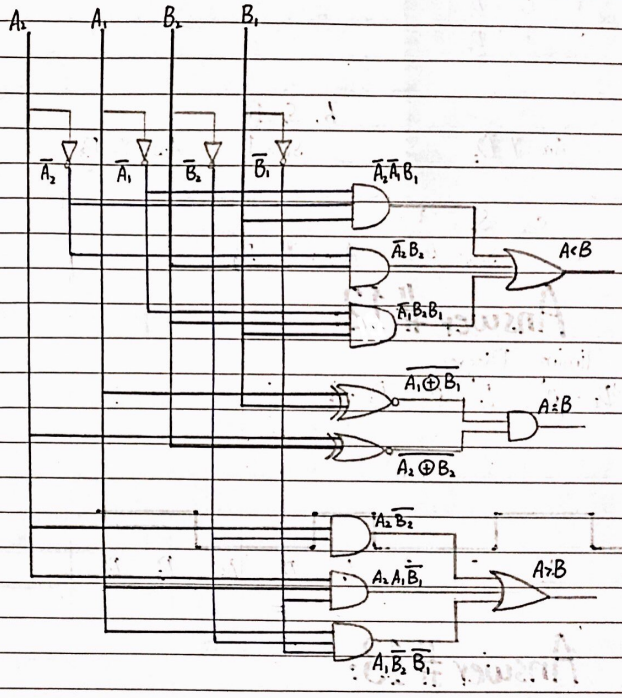
Date _____

A > B :



$\Rightarrow A_2\overline{B_2} + A_2A_1\overline{B_1} + A_1\overline{B_2}\,\overline{B_1}$

$\Rightarrow A_1\overline{B_1}(A_2 + \overline{B_2}) + A_2\overline{B_2}$



2 Bit Comparator

Answer # 11:

Multiplexer

S_1	S_0	Y
0	0	D_0
0	1	D_1
1	0	D_2
1	1	D_3

a. $S_0 = 0$, $S_1 = 1$ Ans: $Y = D_2 = 0$

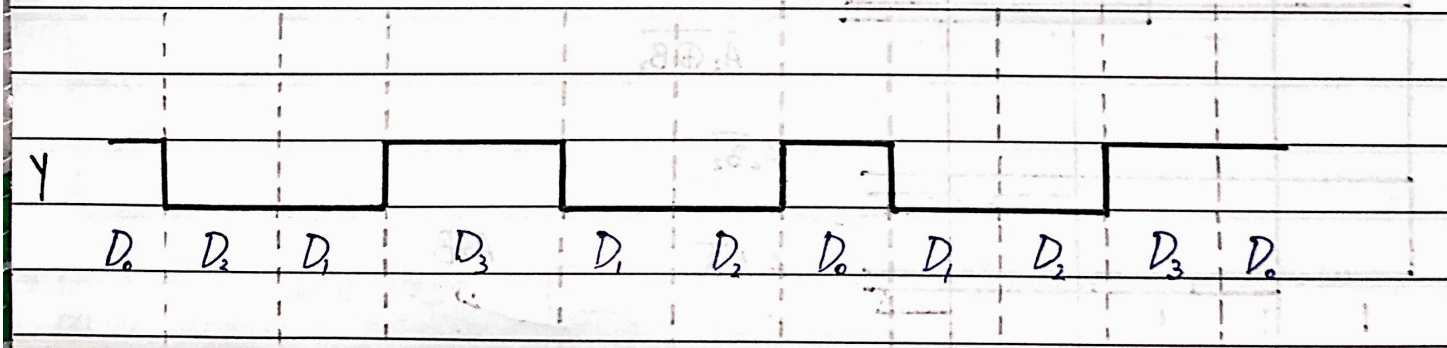
b. $S_0 = 1$, $S_1 = 1$ Ans: $Y = D_3 = 1$

c. $S_0 = 1$, $S_1 = 0$ Ans: $Y = D_1 = 0$

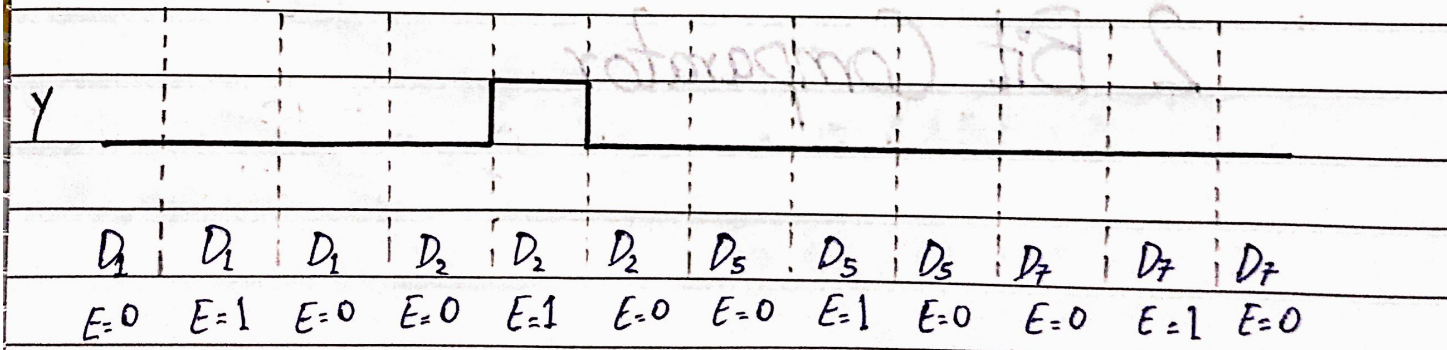
Answer # 12:

Timing Diagram

$D_0 = 1$, $D_1 = 0$, $D_2 = 0$, $D_3 = 1$

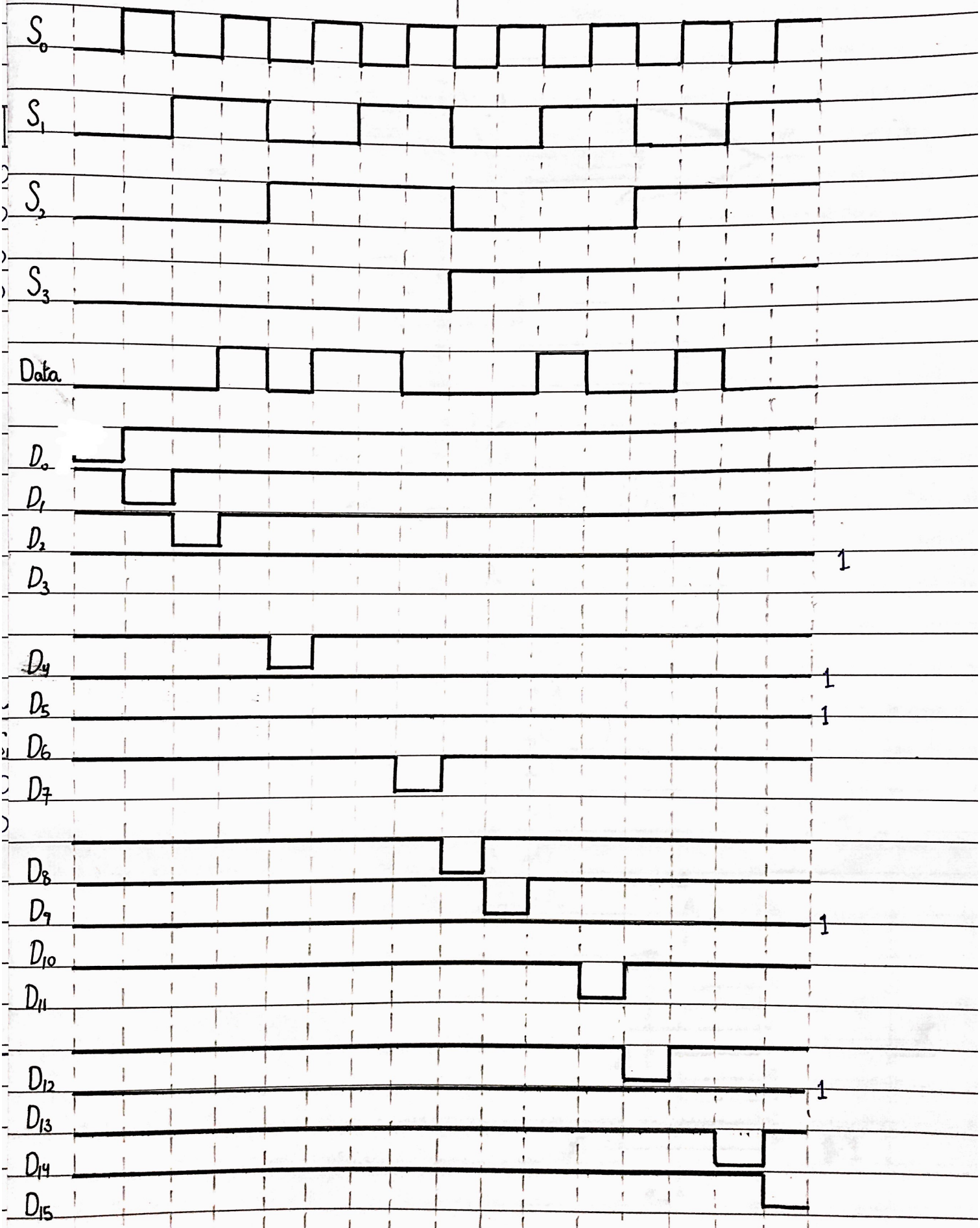


Answer # 13:



Date

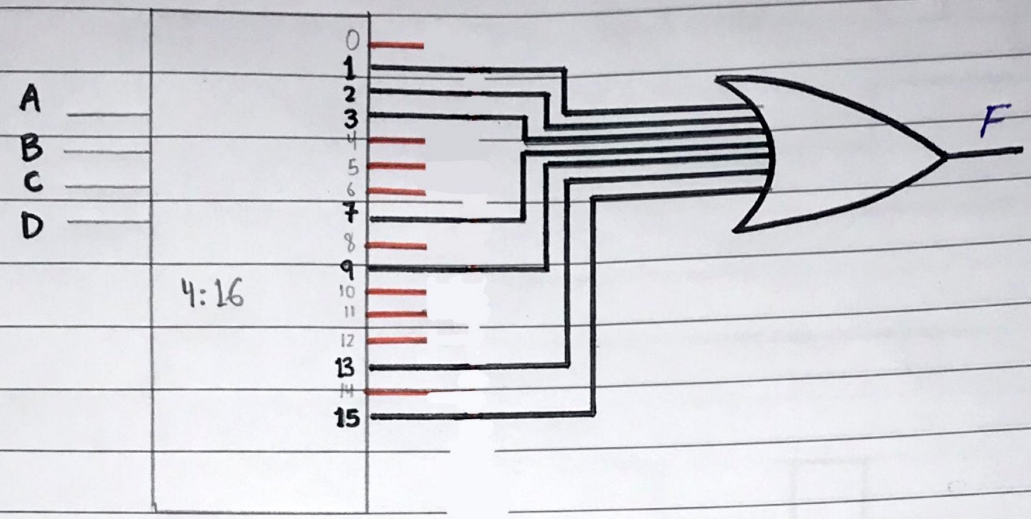
Answer #14: Demultiplexer Timing Diagram



Date

Answer #15

$F(A,B,C,D) = \Sigma(1,2,3,7,9,13,15)$



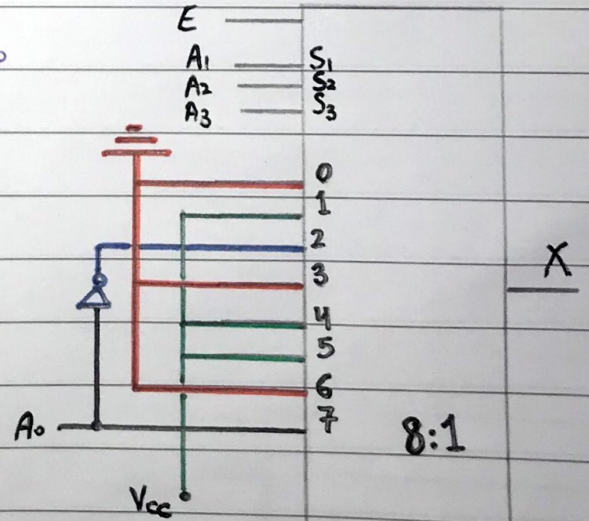
Answer #16

$X(A_3, A_2, A_1, A_0) = \Sigma(2,3,4,8,9,10,11,15)$

A_3	A_2	A_1	A_0	X
0	0	0	0	0
0	0	0	1	0
0	0	1	0	1
0	0	1	1	1
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

	$\bar{A}_0$	A_0	
D_0	0	1	→ 0
D_1	2	3	→ 1
D_2	4	5	→ $\bar{A}_0$
D_3	6	7	→ 0
D_4	8	9	→ 1
D_5	10	11	→ 1
D_6	12	13	→ 0
D_7	14	15	→ A_0

Multiplexer



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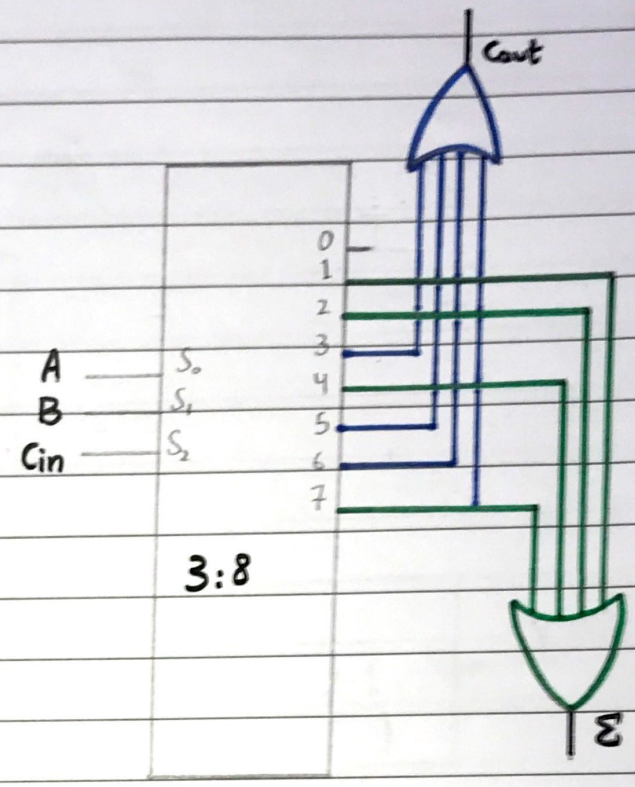
Answer #17:

Full Adder

a. By 3:8 Decoder:

A_2	X	A_1	Y	A_0	Cin	Σ	Cout
0		0		0		0	0
0		0		1		1 (D_1)	0
0		1		0		1 (D_2)	0
0		1		1		0	1 (D_3)
1		0		0		1 (D_4)	0
1		0		1		0	1 (D_5)
1		1		0		0	1 (D_6)
1		1		1		1 (D_7)	1 (D_7)



b. By 4:1 MUX:

$\Sigma = (1, 2, 4, 7)$

$Cout = (3, 5, 6, 7)$

MUX Table:

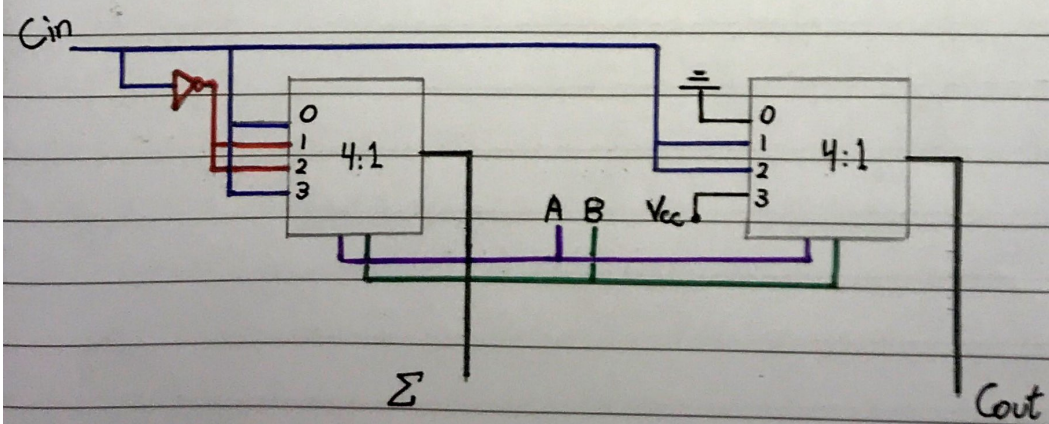
S_1	S_0	X
0	0	D_0
0	1	D_1
1	0	D_2
1	1	D_3

For sum:

	$\overline{Cin}$	Cin	
0	0	①	→ Cin
1	②	3	→ $\overline{Cin}$
2	④	5	→ $\overline{Cin}$
3	6	⑦	→ Cin

For carry:

	$\overline{Cin}$	Cin	
0	0	1	→ 0
1	2	③	→ Cin
2	4	⑤	→ Cin
3	⑥	⑦	→ 1



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Answer #18:

16x1 Multiplexer