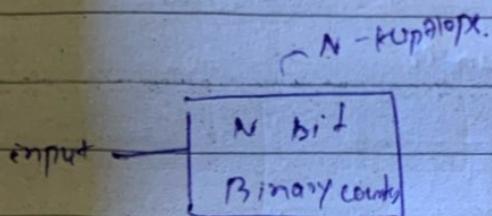


chp E09.

## Counters

- ① The counter counts the no. of times the specific event has been occurred.



and it can count upto

$$0 - 2^n - 1$$

if we have a 4 bit counter so it has 4 flip-flops and it can count from 0 to

15  
0000, 0001, 0010 ... 1111

- ② if the count of the counter goes from 0000 to 1111 then that counter is known as up-counter

- ③ if the counter counts from 1111 to 0000 then that counter is known as a down-counter

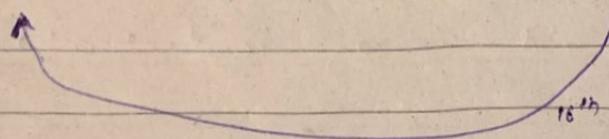
## Modulus of the counter.

↳ Number of different states through which counter goes through before returning to its first state is known as the Modulus of the counter

If we have

a 4-bit binary counter → then it takes 16 cells pulses to come back to the specific sequence.

0000, 0001, 0010, 0011, ..., 1111



4-bit BC = Mod-16 counter

- ④ Sometimes the counter doesn't utilize all the different possible output states and in such cases the modulus of the counter can be less than the maximum possible value

If we take a 4 bit counter then the maximum possible value of the modulus is equal to 16 but if you see <sup>4 bits</sup> BCD counter it counts from 0000 to 1000  
 $\underbrace{\hspace{1cm}}$   
 $1 \text{ MOD } 10$

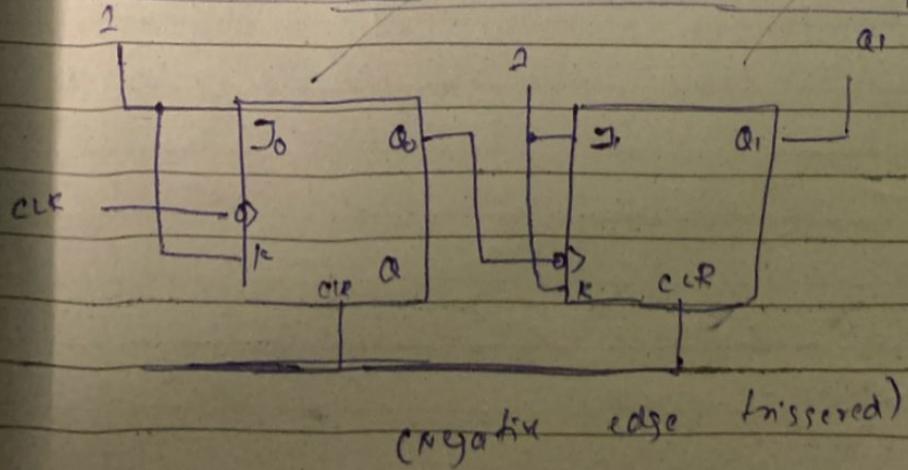
### Types of counters.

- (1) Asynchronous (Ripple counters)
- (2) Synchronous counters

### Asynchronous (Ripple counter)

Counters → does not have a common clock.  
 Let see, a  $\overbrace{\hspace{1cm}}$   
 LSR (which receives CLK)  $\overbrace{\hspace{1cm}}$  MSB count from  $(0 - N)$

~~2 bit binary asynchronous up-counter.~~



~~Negative edge triggered  $\rightarrow Q$   $\xrightarrow{\text{clock}}$  up counter  
Positive edge triggered  $\rightarrow \bar{Q}$   $\xrightarrow{\text{clock}}$  down counter  
Negative edge triggered  $\rightarrow \bar{Q}$   $\xrightarrow{\text{clock}}$  down counter~~

### Important points

Negative edge triggered  $\rightarrow Q$  is clock  $\rightarrow$  up counter

Positive edge triggered  $\rightarrow \bar{Q}$  is clock  $\rightarrow$  up counter

Negative edge triggered  $\rightarrow \bar{Q}$  is clock  $\rightarrow$  down counter

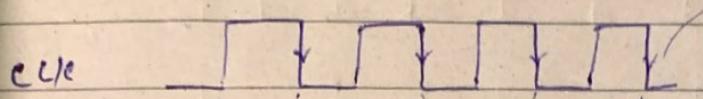
Positive edge triggered  $\rightarrow Q$  is clock  $\rightarrow$  down counter

④ In Asynchronous counters, flip flops respond on the basis of their previous output transition (h/c clk is connected)

⑤ To get these transitions in the output of the flip flop, we need to use those flip flops in the toggle mode ( $J=K=1$ ), that means at every clock pulse the output of the flip flop should toggle, then and then only the next flip flop will be able to receive the clock signal.

Truth table of 2 bit up.

N.E.T.



$Q_0$

$Q_1$

positive

0	1	0	1
0	1	1	1

$Q_1$

0 0 1 1

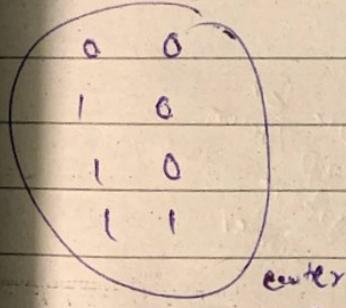
more numbers  
we are  
writing

on the  
lower  
of clk's

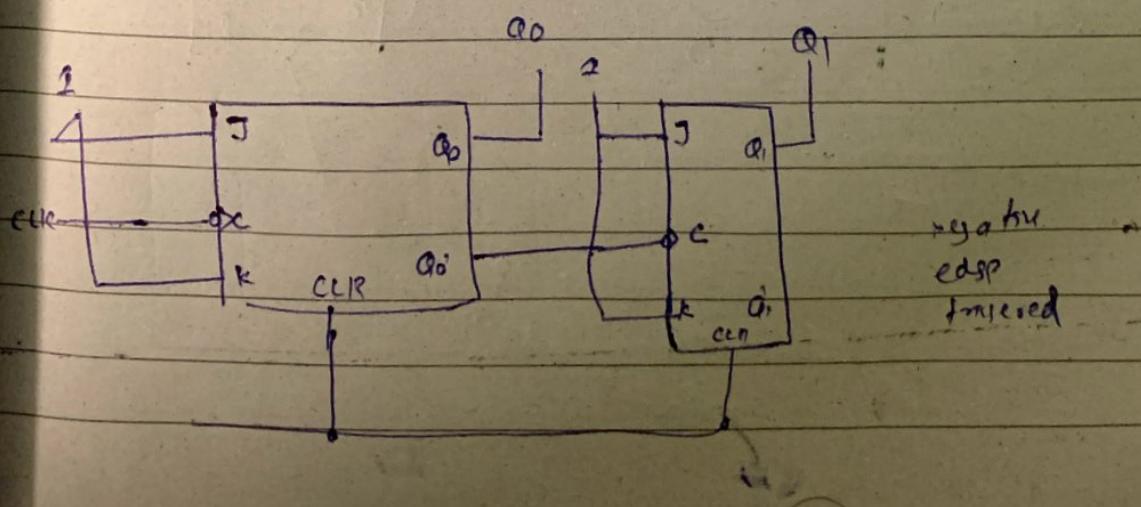
falling edge

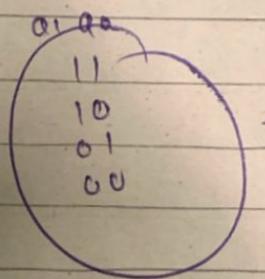
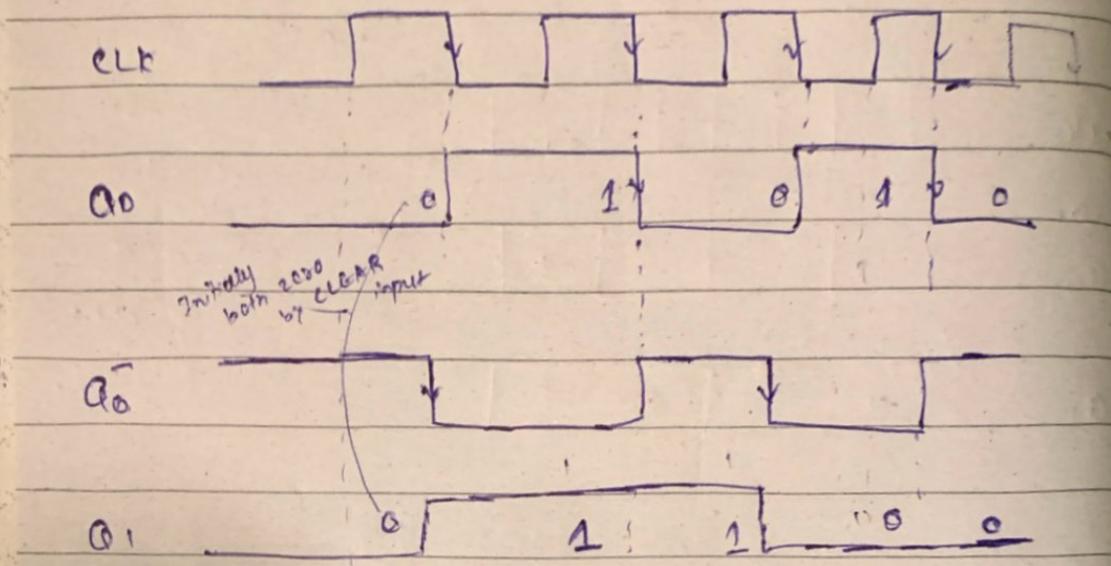
$Q_1 Q_0$

MISLUB

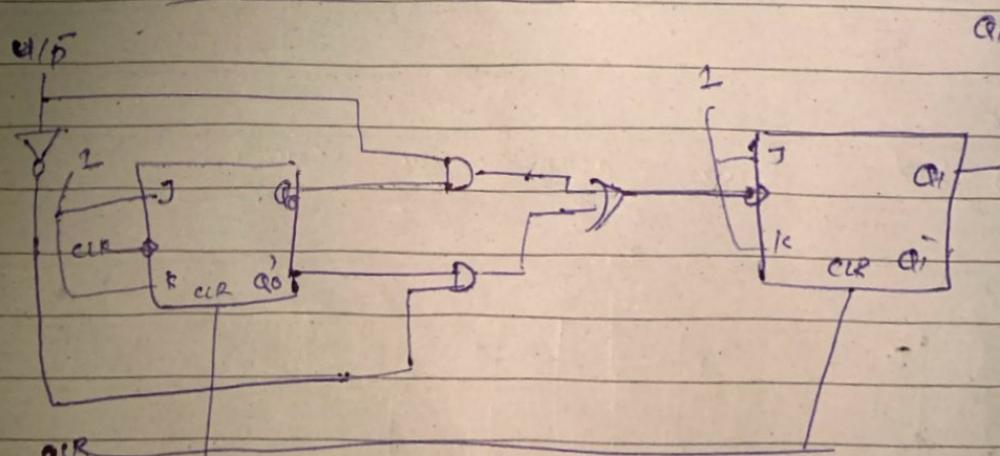


2-bit down asynchronous counter



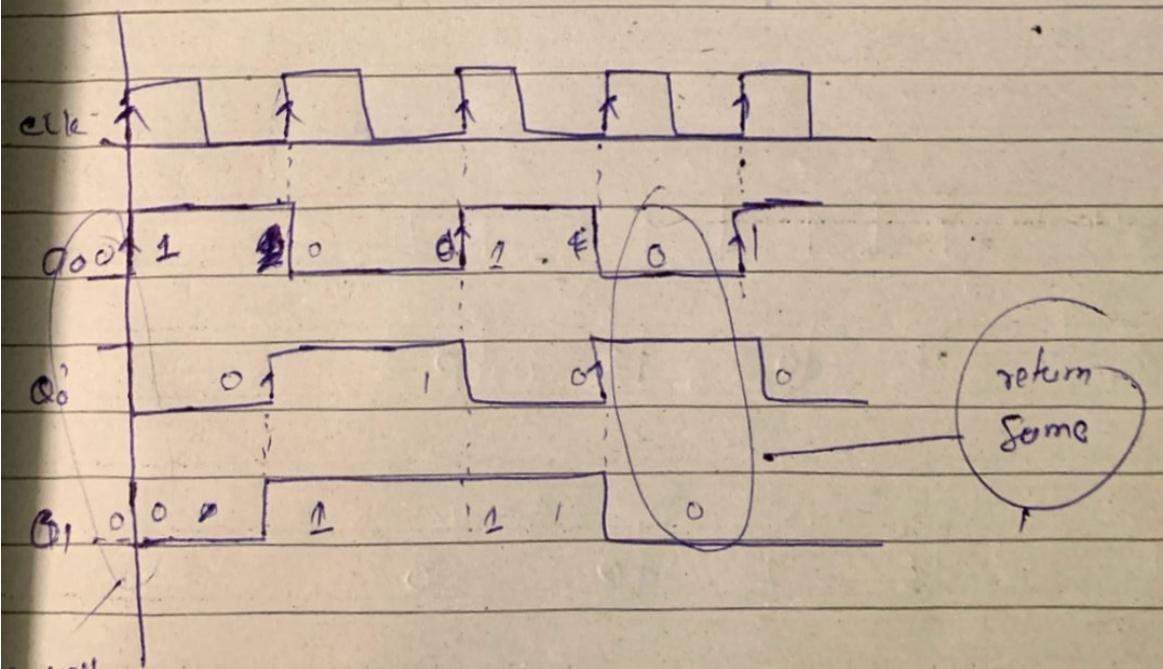
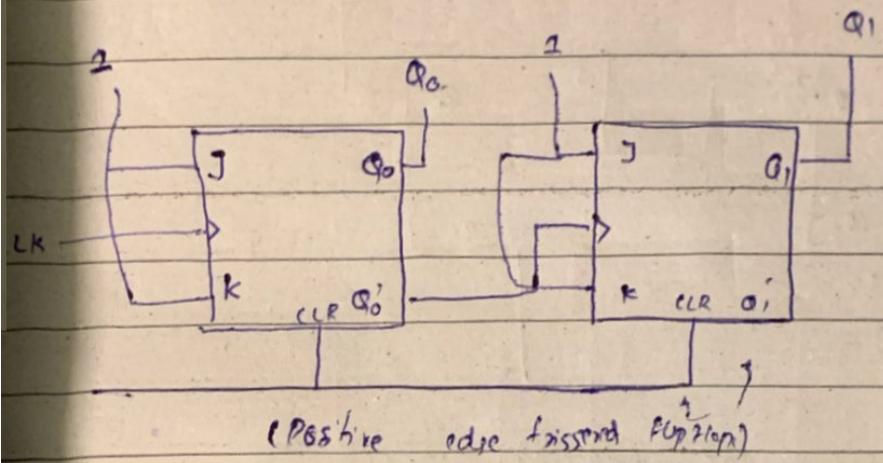


with some modifications



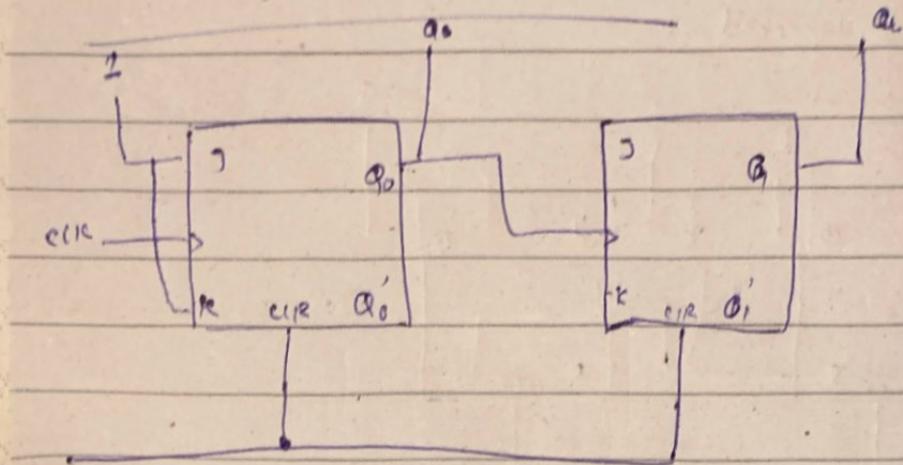
when  $u/d = 1$  up  
 $u/d = 0$  down

2-bit up counter  
with Positive  
edge triggered CLK



Initial state	Q1	Q0
Q1 Q0	0	0
	0	1
	1	0
	1	1

2-bit binary counter  
with negative edge triggered clk.



(Positive edge triggered flip-flops.)

clk . f f f f f

$Q_0$  . 1 0 1 0

$Q_1$  . 1 1 0 0

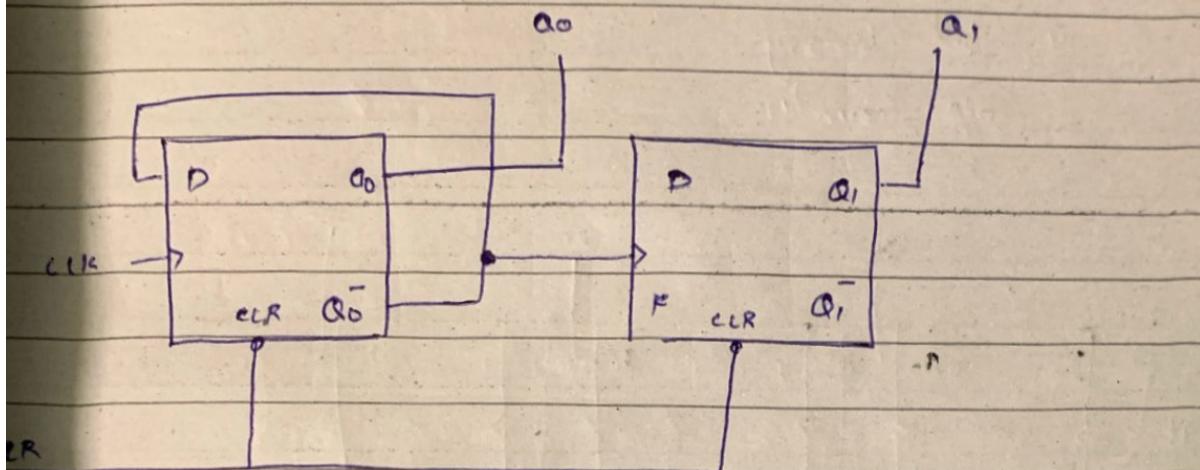
down  
counter



+ve up -  
-ve up Q + clk

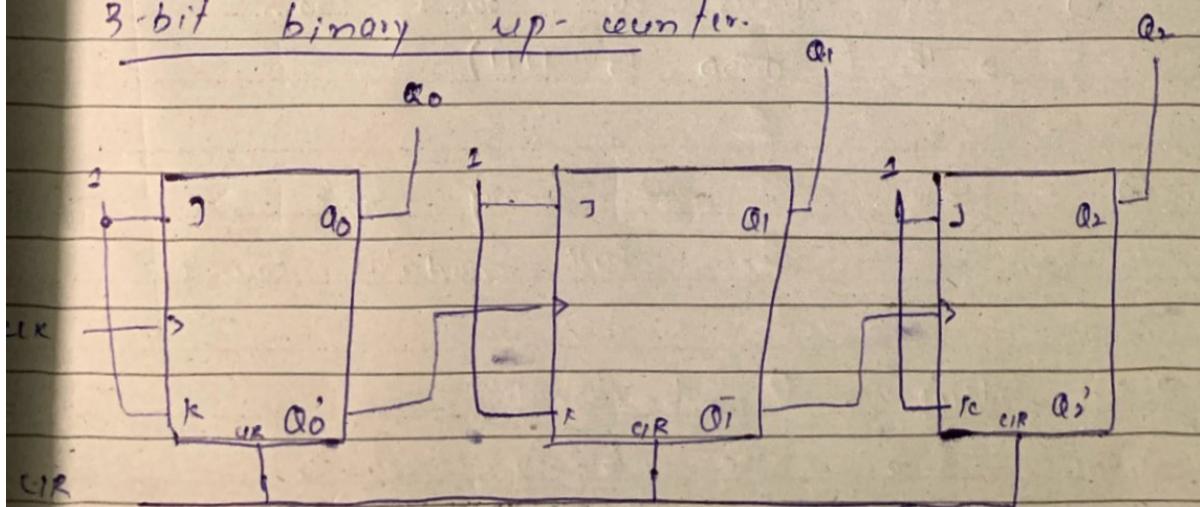
.. to use D-up flop in toggle mode we need to connect the D-input with  $(\bar{Q})$   $\leftarrow \bar{Q}$ -bar

① we can also make the 2 bit binary up/down counters with D-up flop.



(Positive edge triggered D-upflops  
- 2-bit up counter)

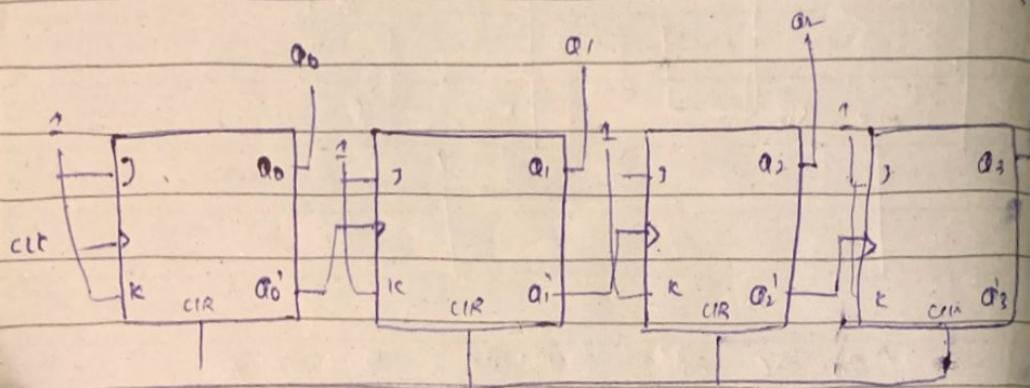
3-bit binary up-counter.



(Positive edge triggered  
upflops)

so this counter will count from  
0-7 (000 to 111)

4-bit binary  
up counter



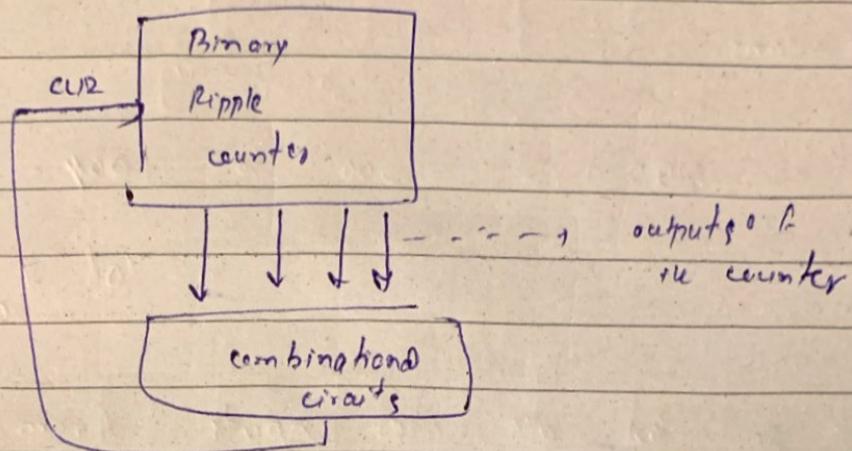
(Positive edge triggered flip-flops)

② This counter will counts from  
0-15 (0000 to 1111)

① Since all ~~can't~~ binary ripple  
counters are full modulus counters

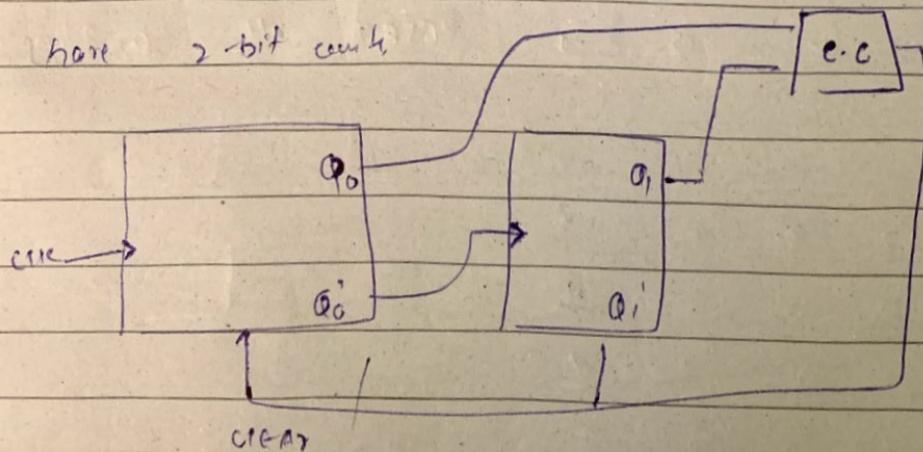
② By adding a combinational logic  
circuit to the binary counter  
we can design the counter of  
specific modulus (of our own choice)

①



In second if we

have 2-bit units



(active low input pattern)

This signal is output of 10 combination  
circuit is low then it will reset  
all the flip flops to zero)

④ to decide minimum number of flipflops required we follow the inequality  $N \leq 2^m$   $\rightarrow$  your choice.  
 modulus  $[n = \text{flipflops}]$

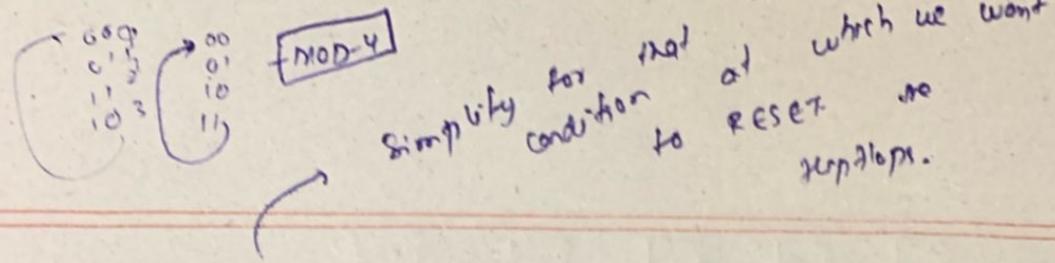
⑤ let's if we want to create a MOD-5 counter means

$(a = 4)$   
 MOD-5 : 000 to 100  
 at 101 it will reset;

so for all the inputs from 000 to 100 (the output of the combinational circuit that we are making) should be 1 and at 101 it should be 0 to RESET all flipflops.

$Q_2$	$Q_1$	$Q_0$	R
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	$x$
1	1	1	$x$

$(x)$ , don't care terms

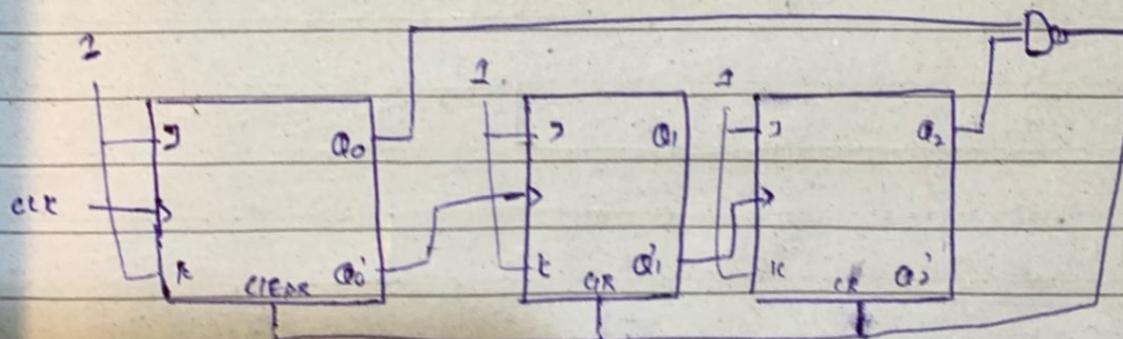


Let's simplify it with K-MAP

				$\bar{Q}_2 \bar{Q}_0$			
				00	01	11	10
$Q_1$	0	0	1	1	0		
	1	0	X	X	1		

$$R = \overline{\bar{Q}_2 \bar{Q}_0}$$

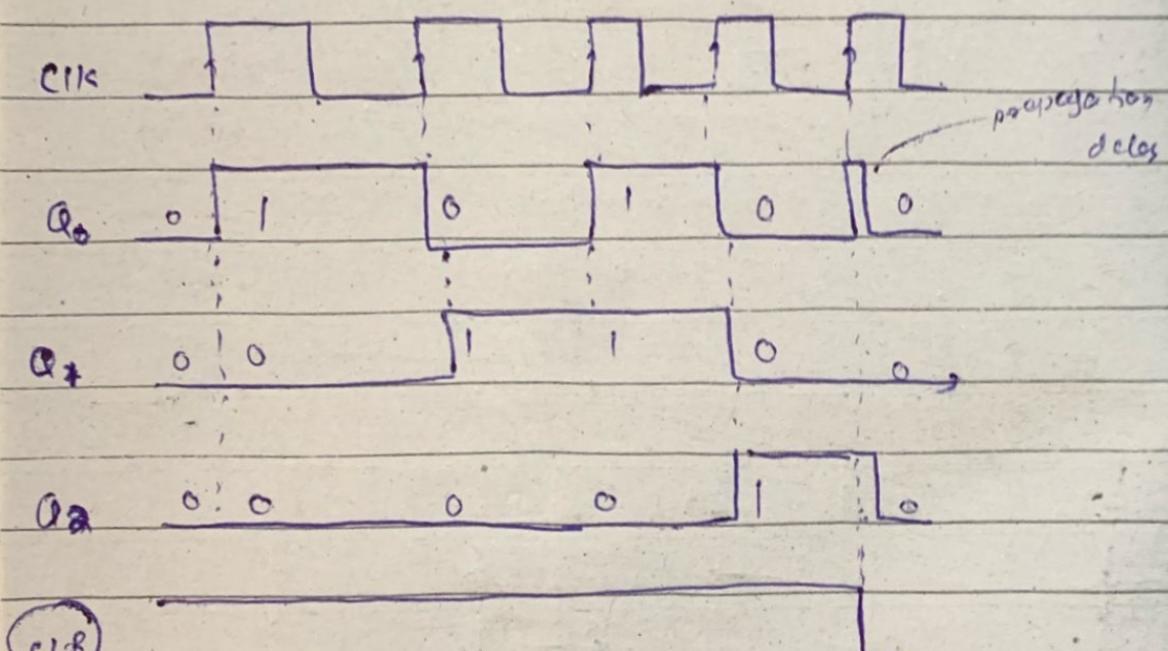
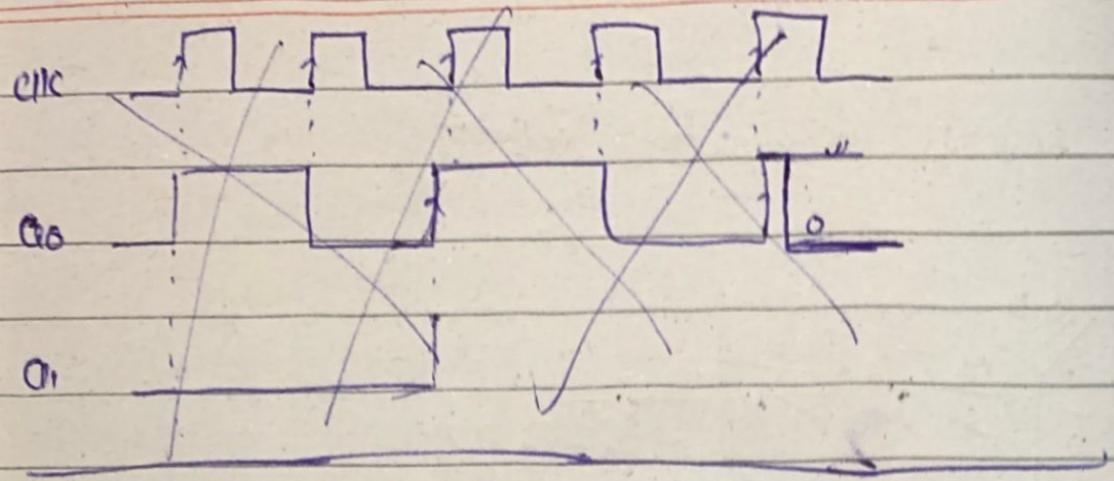
R or because of  
zero & don't  
care  
term.  
 $\overline{\text{and}} = \text{NAND}$



at 1st state  $Q_2 = 1$   $Q_1 = 0$   $Q_0 = 1$  arrive

$$Q_2 = 1 \quad \overline{Q_2 Q_1} = 0 - \text{RESET}$$

at clock.



CLR

NAND of  $Q_2 \& Q_1$

CLR 2nd all  
reset

BCD - ripple counter

↳ MOD-10 counter.

$$N \leq 2^n$$

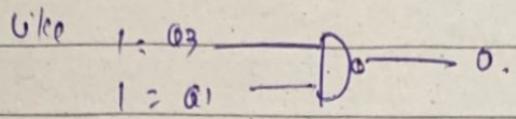
$$10 \leq 2^n$$

$n=4$  (Pupulations)

	$Q_3$	$Q_2$	$Q_1$	$Q_0$	R
0	0	0	0	0	1
1	0	0	0	1	1
2	0	0	1	0	1
3	0	0	1	1	1
4	0	1	0	0	1
5	0	1	0	1	1
6	0	1	1	0	1
7	0	1	1	1	1
8	1	0	0	0	1
9	1	0	0	1	1
reset	1	0	1	0	0
	1	0	1	1	X
	1	1	0	0	X
0 <sup>2</sup>	1010		1	1	X
$Q_3 = 1$			1	1	X
$Q_2 = 0$			1	1	X
$Q_1 = 1$			1	1	X
$Q_0 = 1$			0		

So by connecting  $Q_3$  &  $Q_1$  to  
we can get that  
to NAND gate

~~bc~~



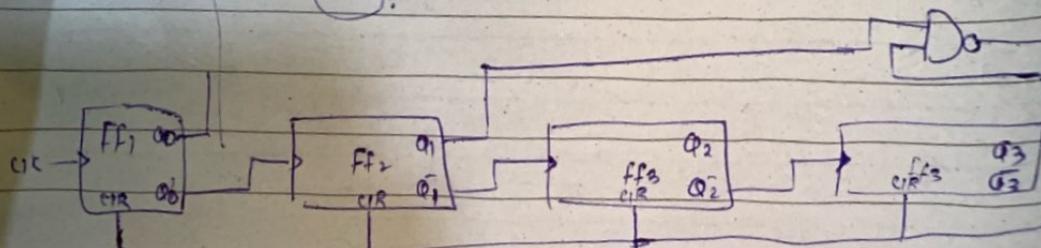
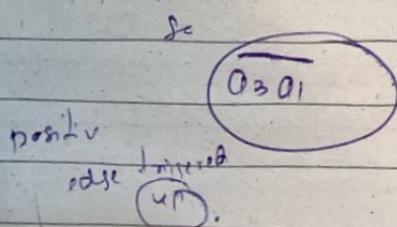
before  $I = Q_3$  &  $Q_1$  are not logic high at the same time.

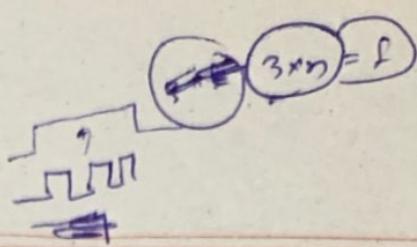
we can also get this with K-MAP

		Q <sub>1</sub>			
		00	01	11	10
Q <sub>3</sub>	Q <sub>2</sub>	00	.	1	1
		01	u	s	z
Q <sub>3</sub>	Q <sub>2</sub>	11	y	x	10
		10	r	a	x

$$= G^3 Q_1$$

Since there are zero R don't care





④ if  $f$  is the frequency of input clock signal, then the output frequency of the output ( $\text{Q}_{n-1}$ ) is equal to  $f$  divided by  $n$

$n = \text{no. of steps}$

if we have MOD-20 counters

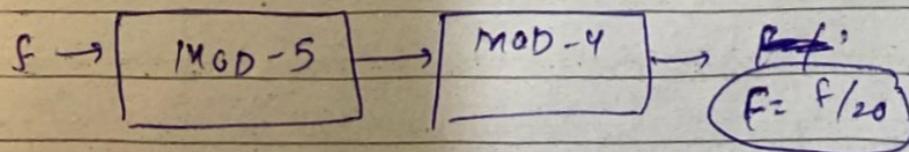
$$\text{Out } f = \frac{f}{20} \quad \text{input frequency of clk signal.}$$

in this way ~~frequency~~ <sup>ripple</sup> counters can be used as a frequency divider.

2) Moreover we can also increase the modulus of the counter by cascading the multiple such counters of the different modulus.

for e.g.

if we want to design a MOD-20 counter we can do so by cascading the MOD-5 counter ~~and~~ and the MOD-4 counter.

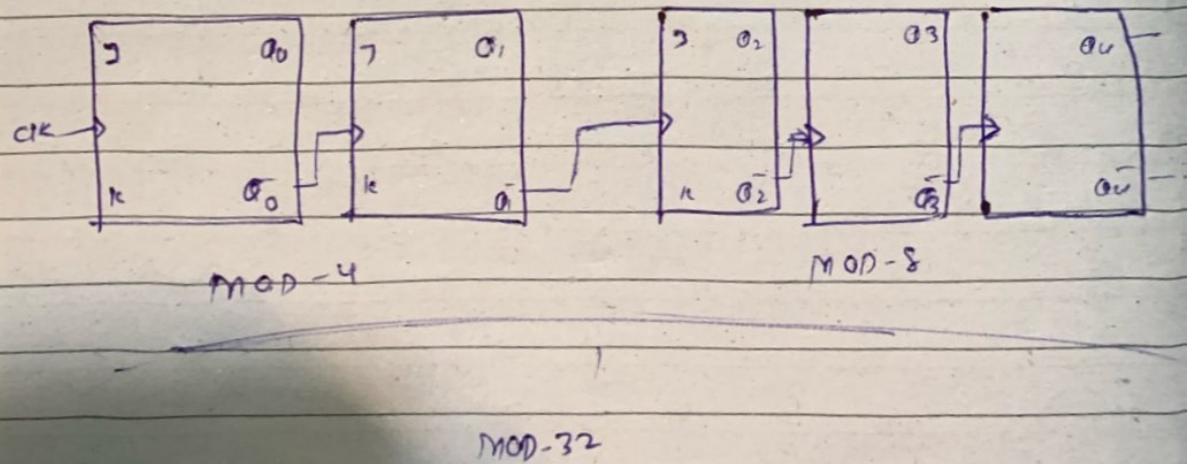


④ generally if we cascade MOD-M counters with MOD-N counters then the overall modulus of the counter will be equal to MOD-MN (independent of the positions of the counters to cascade MOD-M → MOD-N or MOD-N → MOD-M)  $\Rightarrow$  MOD-MN

e) but if order of context  
Sequence is different we  
get different output sequence.

for e.g if we take full modulus

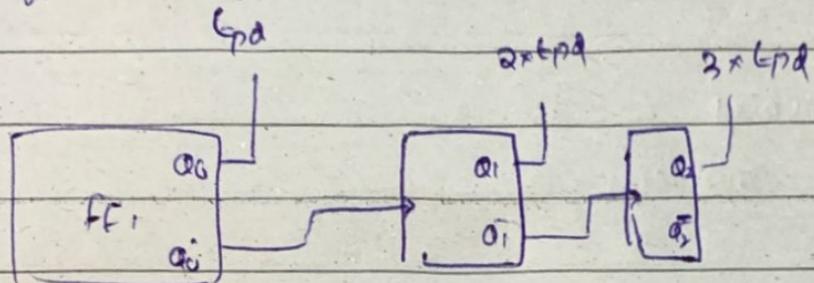
2-bit up → 3bit up



③ effects of propagation delay in ripple

counters.

propagation  
delay



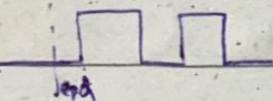
for n-bit  
ripple counter

For ex.

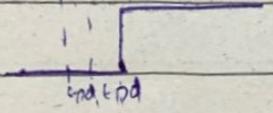
the maximum

④

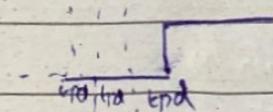
Q<sub>0</sub>



Q<sub>1</sub>



Q<sub>2</sub>



propagation

$$\text{delay} = n \times C_{pd}$$

no. of  
replications

## Synchronous Counters.

In all the flip flops receive a common clock

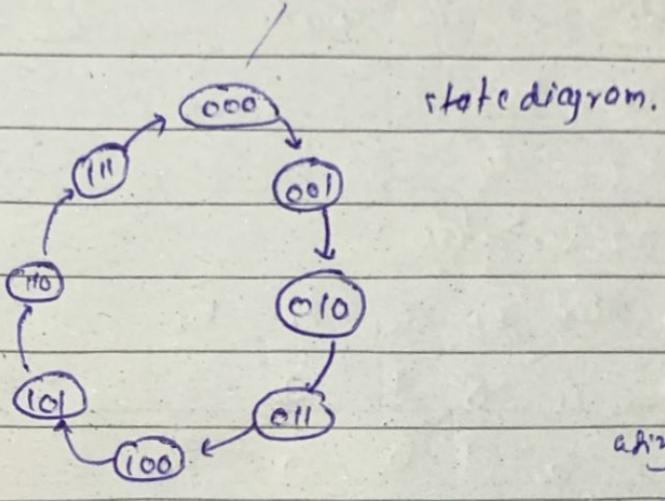
steps for designing  
synchronous counters:

- ① Find the required number of flip flops
- ② Draw the state diagram
- ③ select the flip flops and draw excitation table (transition)
- ④ Find minimal expressions for the excitation of each flip flop. (K-MAP)
- ⑤ Draw the logic counter

### → 3-bit up counter

- ① Flip flops = 3 — b/c it's a 3-bit
- ② State diagram → will show the sequence in which the output state of the counter will change and it shows that if the counter is in specific state, then what will be the next state of the counter

Let say for present state  
so  $001 \rightarrow$  in the next state.



ability to make  
7 counts

### Excitation / Transition table of JK flip flop

output transitions.

$Q_n$	$Q_{n+1}$	$J$	$K$	(input)
0	0	0	X	
1	0	X	1	
0	1	1	X	
1	1	X	0	

$Q_n$ : present state

$Q_{n+1}$ : Next state

X : don't care

based  
on state  
diagram

transition table

of the counter

Find it by  
examining the  
transition table  
of JK-flipflop

Ex:  $0 \rightarrow 0$  transition  
 $J=0, K=0$

Required transitions

$Q_2$	$Q_1$	$Q_0$	$Q_2 + Q_1 + Q_0$	$J_2$	$K_2$	$J_1$	$K_1$	$J_0$	$K_0$
0	0	0	0 0 0	0	1	0	x	0	x 1 x
0	0	1	0 0 1	0	0	0	x	1	x x 1
0	1	0	0 1 0	0	1	0	x	0 1	x
0	1	1	1 0 0	1	0	x	1	x 1	
1	0	0	1 0 1	0	1	x	0	0 1	x
1	0	1	1 1 0	x	0	1	x	x 1	
1	1	0	1 1 1	x	0	x	0	1	x
1	1	1	0 0 0	x	1	x	1	x	1

(\*)

① now to  
find minimal  
for each  
using K-maps (only map 1 is & x is)

$J_2$

$Q_1 Q_0$	00	01	11	10
0	0			
1	*	x		x

$$J_2 = Q_1 \bar{Q}_0$$

~~Q1 Q0~~

$Q_2$   
 00 - state same  
 11 - state toggle.  
 10 - SET.  
 01 - RFSFT.

$K_2$  don't care terms can  
 be assumed either  
 zero or 1.

		00	01	11	10
		0	X	X	X
		1	X	1	0
$Q_2$	00				
	01				
	11				
	10				

$$K_2 = Q_1 Q_0$$

$$J_2 = K_2 = Q_1 Q_0$$

try to form  
longer as possible.

$J_1$

		00	01	11	10
		0	1	X	X
		1	1	X	X
$Q_2$	00				
	01				
	11				
	10				

$K_1$

		00	01	11	10
		0	X	X	1
		1	X	X	1
$Q_2$	00				
	01				
	11				
	10				

$$J_1 = Q_0$$

$$I_1 = Q_0$$

$$J_1 = K_1 = 00$$

$J_0$

		00	01	11	10
		0	1	X	X
		1	1	X	X
$Q_2$	00				
	01				
	11				
	10				

$K_0$

		00	01	11	10
		0	*	1	1
		1	X	1	1
$Q_2$	00				
	01				
	11				
	10				

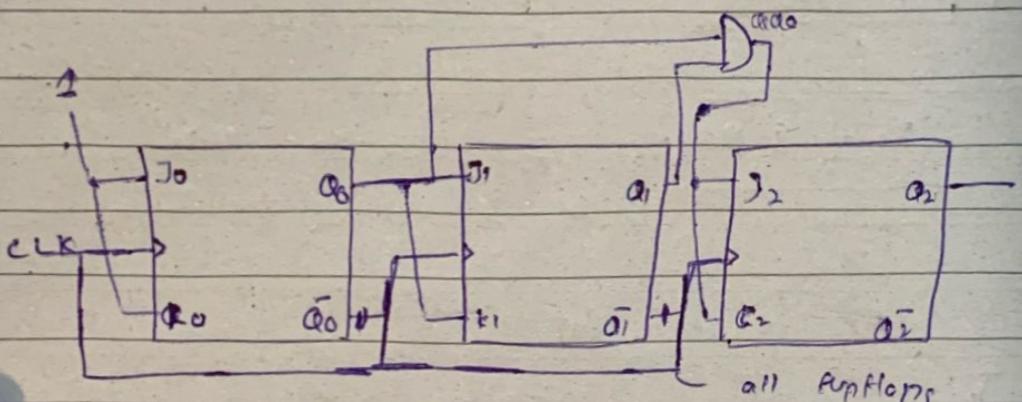
But if we say  $X = 1$  then

$$J_0 = K_0 = 1$$

$$J_0 = K_0 = 1$$

$$J_1 = K_1 = Q_0$$

$$J_2 = K_2 = Q_1 \bar{Q}_0.$$



3-bit synchronous up counter

like a simple  
3-bit, valid number  
sequence

only applies when  
the sequence is correct

④ u can also get the idea of inputs from  
the 3-bit truth table like you see

$Q_0$  is changing everytime (means toggle  
so  $J_0 = K_0 = 1$ ) and if you see  $Q_1$  is  
changing whenever  $Q_0$  becomes 1  
means,  $J_1 = K_1 = Q_0$  (i.e. toggle)

and  $Q_2$  is changing whenever both  
 $Q_1$  &  $Q_0$  becomes 1 to 0 AND  $Q_1 = 1$

$J_2 = K_2 = Q_1 \bar{Q}_0$  i.e. toggle.

saving some pattern  
we can create a 4 bit up counter

Synchronous

$Q_3 \ Q_2 \ Q_1 \ Q_0$

0 0 0 0

0 0 0 1

0 0 1 0

0 0 1 1

0 1 0 0

0 1 0 1

0 1 1 0

0 1 1 1

1 0 0 0

1 0 0 1

1 0 1 0

1 0 1 1

1 1 0 0

1 1 0 1

1 1 1 0

1 1 1 1

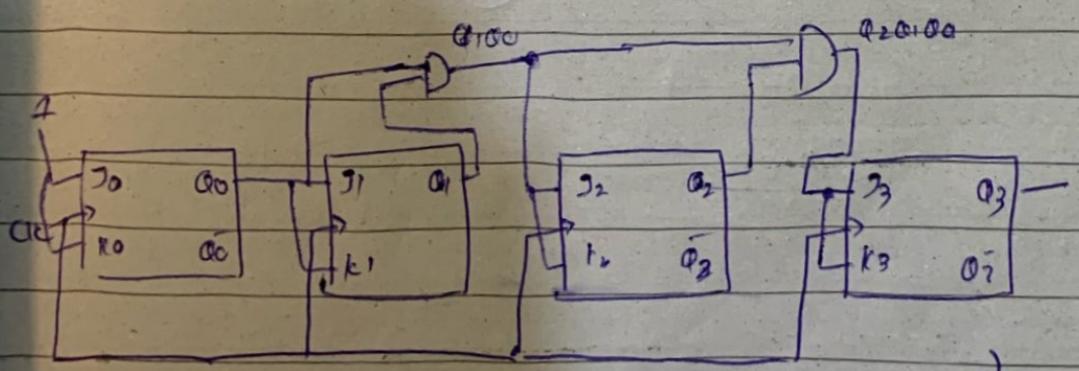
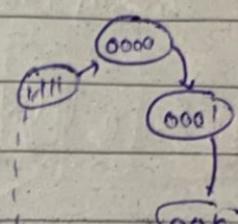
$$J_0 = k_0 = 1$$

(b/c output changing)

$$J_1 = k_1 = Q_0$$

$$J_2 = k_2 = Q_1 Q_0$$

$$J_3 = k_3 = Q_2 Q_1 Q_0.$$



(4-bit up counter) (Synchronous)

⑤ For  $N$ -bit up synchronous counter

Max-propagation delay =  $T_{pd}(\text{FF}) + (n-2)T_{pd}(\text{AND gate})$

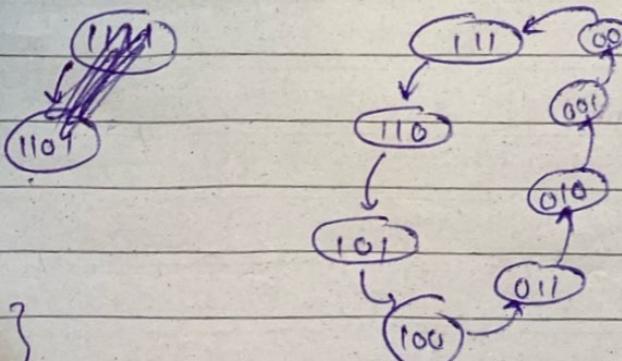
$\uparrow (A^{n-1})$   
output

3-bit down counter.

same steps followed as up-counter

$$\text{FCNTHops} = 3 \rightarrow \text{b/c 3-bit}$$

state diagram.



$Q_2$	$Q_1$	$Q_0$
1	1	1
1	1	0
1	0	1
1	0	0
0	1	1
0	1	0
0	0	1
0	0	0

down counter

Using J-K flip-flops for a logic circuit.

J	K
0	0
0	X
1	1
0	X
1	0

Present state | Next state | Required excitation table

$Q_2\ Q_1\ Q_0$	$Q_2 + Q_1 + Q_0 +$	$J_2\ K_2$	$J_1\ K_1$	$J_0\ K_0$
1 1 1	1 1 0	X 0	X 0	X 1
1 1 0	1 0 1	X 0	X 1	1 X
1 0 1	1 0 0	X 0	0 X	X 1
1 0 0	0 1 1	X 1	1 X	1 X
0 1 1	0 1 0	0 X	X 0	X 1
0 1 0	0 0 1	0 X	X 1	1 Y
0 0 1	0 0 0	0 X	0 X	X 1
0 0 0	1 1 1	1 X	1 X	1 X

$J_2$

$Q_2 \backslash Q_1 Q_0$	00	01	11	10
00	1			
1	X	X	X	X

$K_2 \backslash Q_1 Q_0$	00	01	11	10
0	X	X	X	X
1	1			

$$J_2 = \bar{Q}_1 \bar{Q}_0$$

$$K_2 = \bar{Q}_1 \bar{Q}_0$$

$$J_2 = K_2 = \bar{Q}_1 \bar{Q}_0$$

$J_1$	$K_1$
$Q_2 \backslash Q_1$	$Q_2 \backslash Q_1$
00 01 11 10	00 01 11 10
0 1   1   X   X	0 1   X   X   1

$J_1$	$K_1$
$Q_2 \backslash Q_1$	$Q_2 \backslash Q_1$
00 01 11 10	00 01 11 10
0 1   X   X   1	0 1   X   X   1

$$J_1 = \bar{Q}_0$$

$$K_1 = \bar{Q}_0$$

$$J_1 = K_1 = \bar{Q}_0$$

$J_0$	$K_0$
$Q_2 \backslash Q_1$	$Q_2 \backslash Q_1$
00 01 11 10	00 01 11 10
0 1   2   X   X   1	0 1   Y   1   1   X

$J_0$	$K_0$
$Q_2 \backslash Q_1$	$Q_2 \backslash Q_1$
00 01 11 10	00 01 11 10
0 1   2   X   *   2	0 1   Y   1   1   X

Y: don't care  $\rightarrow$  considered as 1

$$J_0 = 1$$

$$Q_0 = 1$$

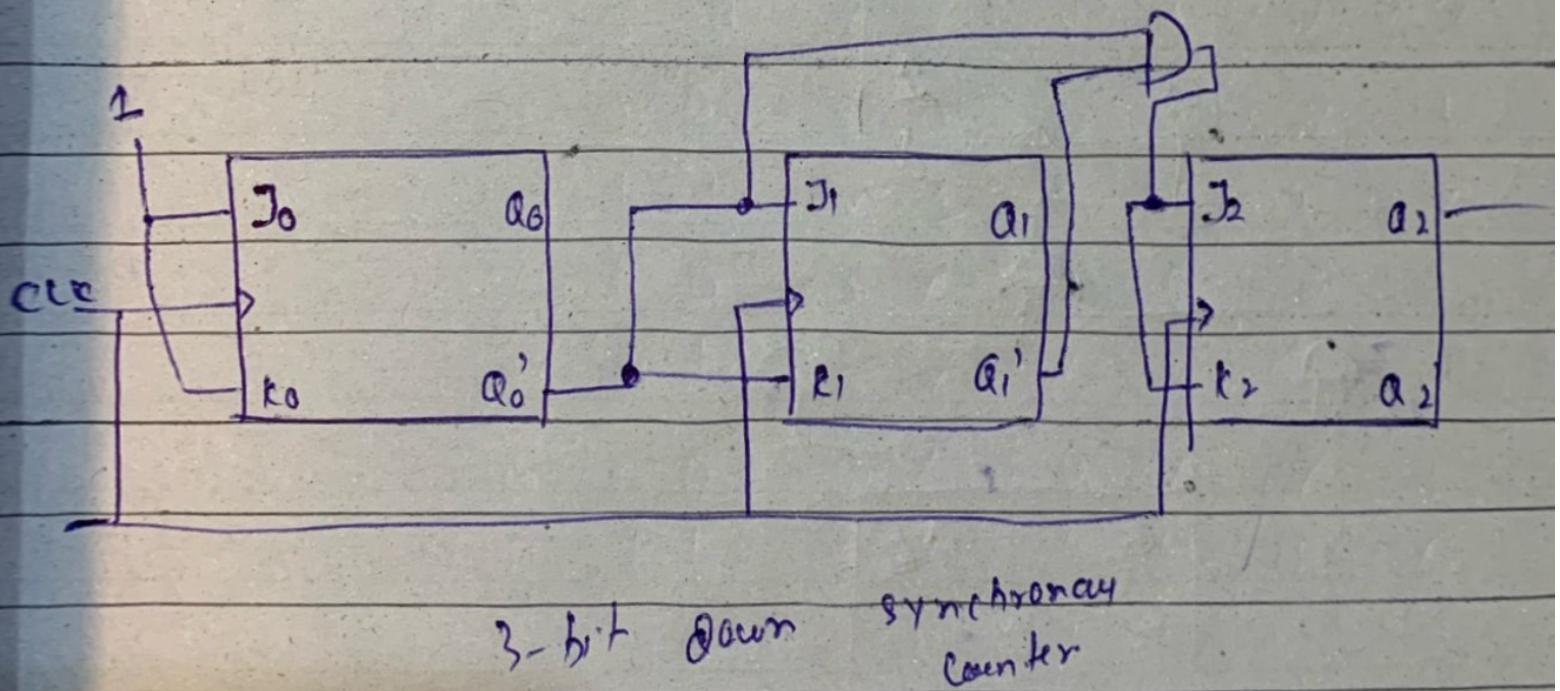
$$J_0 = Q_0 = 1$$

$$\overline{A} - \overline{B} = \cancel{X} \quad (\overline{A+B})$$

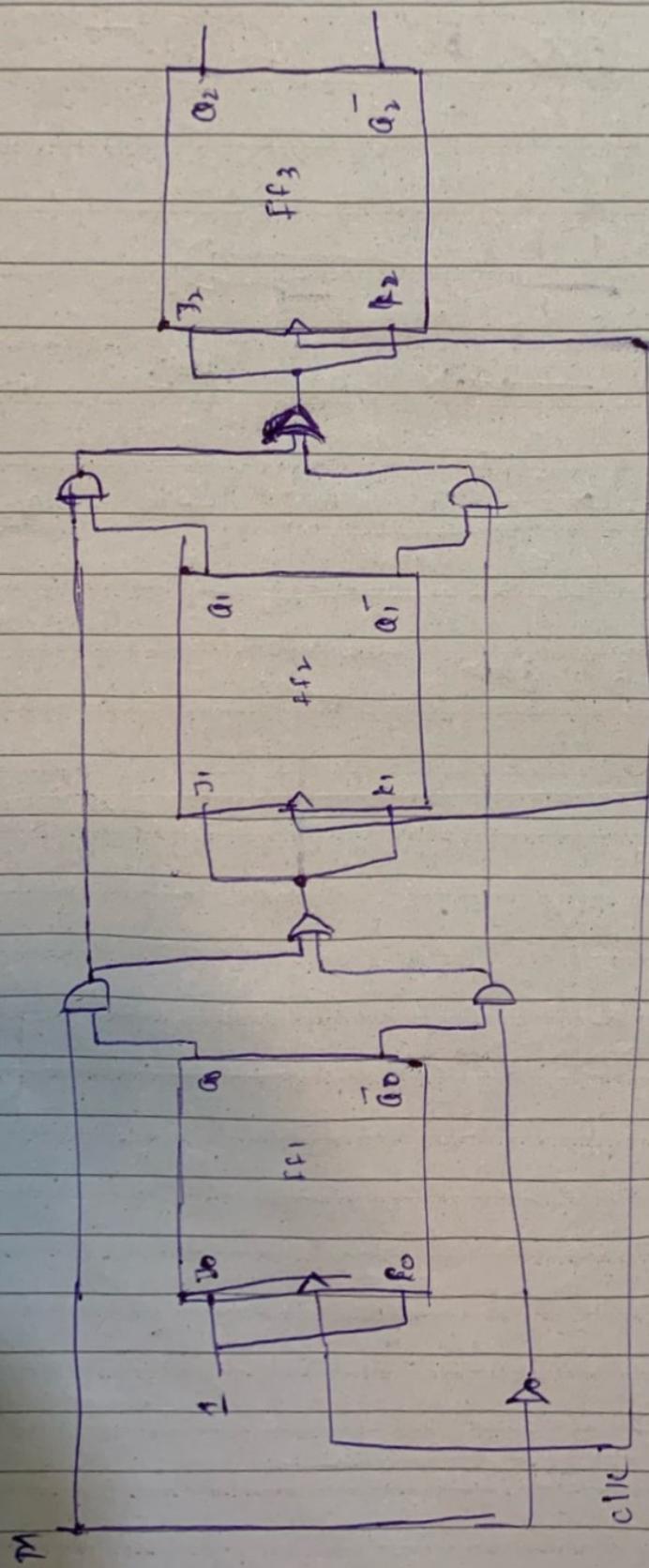
$$J_0 = K_0 = 1$$

$$J_1 = K_1 = Q_0$$

$$J_2 = K_2 = \bar{Q}_1 \bar{Q}_0 \rightarrow (Q_1 + \bar{Q}_0)$$



3-bit up / down counter.  
synchronous



⑧ Binary counters  
are full modulus  
counters.

⑨ Here M is a mode signal

when  $M=1 \rightarrow$  circuit works as  
a up counter

⑩ when  $M=0 \rightarrow$  circuit works as  
a down counter.

Synchronous BCD counter. MOD-10

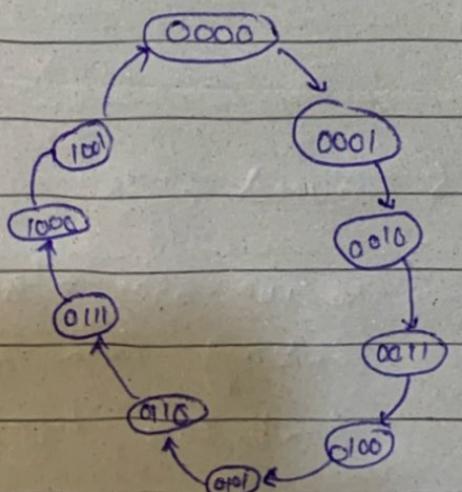
all inputs same just one more  
⑪ enable lock-out condition  $n \leq 2^n$

⑫ require 4 flip-flops

$10 \leq 2^n$

$n=4$   
no. of flip-flops.

⑬ state diagram



for our  
specific  
Modulus  
counter.

⑭

Present state	Next state
$Q_3\ Q_2\ Q_1\ Q_0$	$Q_3+Q_2+Q_1+Q_0$
0 0 0 0	0 0 0 1
0 0 0 1	0 0 1 0
0 0 1 0	0 0 1 1
0 0 1 1	0 1 0 0
0 1 0 0	0 1 0 1
0 1 0 1	0 1 1 0
0 1 1 0	0 1 1 1
0 1 1 1	1 0 0 0
1 0 0 0	1 0 0 1
1 0 0 1	0 0 0 0

④ we also have 6 unused states

1010 to 111 → so we are 9/8  
considering them as  
don't care terms.

1010  
1011  
1100  
1101  
1110  
1111

$$\begin{array}{|c|c|} \hline 0 & 0 \\ \hline 0 & 0 \\ \hline J=0 & K=0 \\ \hline J=0 & K=1 \\ \hline J=0 & K=2 \\ \hline \end{array} = 0$$

$$\begin{array}{|c|c|} \hline 0 & 1 \\ \hline J=1 & K=0 \\ \hline J=1 & K=1 \\ \hline J=1 & K=2 \\ \hline \end{array}$$

$$\begin{array}{|c|c|} \hline 1 & 0 \\ \hline J=0 & K=1 \\ \hline J=1 & K=1 \\ \hline J=x & K=1 \\ \hline \end{array}$$

$$\begin{array}{|c|c|} \hline 1 & 2 \\ \hline J=1 & K=0 \\ \hline J=0 & K=0 \\ \hline J=x & K=0 \\ \hline \end{array}$$

Required Excitation:

$J_3$	$k_3$	$J_2$	$k_2$	$J_1$	$k_1$	$J_0$	$k_0$
0	x	0	x	0	x	1	x
0	x	0	x	1	x	x	1
0	x	0	x	x	0	1	x
0	x	1	x	x	1	x	1
0	x	y	0	0	x	1	x
0	x	x	0	1	x	x	1
0	x	x	0	x	0	1	x
1	x	x	1	x	1	x	1
x	0	0	x	0	x	1	x
x	1	0	x	0	x	x	1

$J_3$

Q1 Q0		Q1 Q0	
00	01	11	10
00			
01			
11	x	x	x
10	x	x	x

$$J_3 = Q_2 Q_1 Q_0$$

$K_3$

Q1 Q0		Q1 Q0	
00	01	11	10
00	x	x	x
01	x	*	x
11	x	x	x
10	1	x	x

6 unpaired bits

group of 8

$$I_{C3} = Q_2 Q_1 Q_0$$

$$K_3 = Q_0$$

includes 6  
unused terms.  
[don't care]

$J_2$

$\bar{Q}_3 Q_2 \rightarrow 0100$		00 01 11 10			
00	01				
00	X	Y	Y	X	
01	X	Y	Y	X	
11	X	Y	Y	X	
10			X	X	

$K_2$

$\bar{Q}_3 Q_2 \rightarrow 0100$		00 01 11 10			
00	01				
00	X	Y	Y	X	
01					
11	X	X	X	X	
10	X	Y	Y	X	

$$K_2 = 0100$$

$$J_2 = \bar{Q}_3 Q_2$$

$$J_2 = K_2 = 0100$$

$J_1$

$\bar{Q}_3 Q_2 \rightarrow 0100$		00 01 11 10			
00	01				
00	1	X	X		
01	1	X	X		
11	Y	Y	Y	X	
10			X	X	

$K_1$

$\bar{Q}_3 Q_2 \rightarrow 0100$		00 01 11 10			
00	01				
00	X	X	1		
01	X	X	1		
11	*	Y	X	X	
10	X	X	Y	X	

$$J_1 = \bar{Q}_3 Q_2$$

$$K_1 = Q_0$$

$J_0$

$\bar{Q}_3 Q_2 \rightarrow 0100$		00 01 11 10			
00	01				
00	1	Y	Y	1	
01	1	Y	Y	1	
11	Y	Y	Y	X	
10	1	Y	Y	1	

$K_0$

$\bar{Q}_3 Q_2 \rightarrow 0100$		00 01 11 10			
00	01				
00	X	1	1	X	
01	X	1	1	X	
11	Y	Y	Y	X	
10	X	1	Y	1	

$$J_0 = 1$$

$$K_0 = 1$$

$$J_3 = Q_2 Q_1 Q_0$$

$$k_3 = Q_0$$

$$J_2 = Q_1 Q_0$$

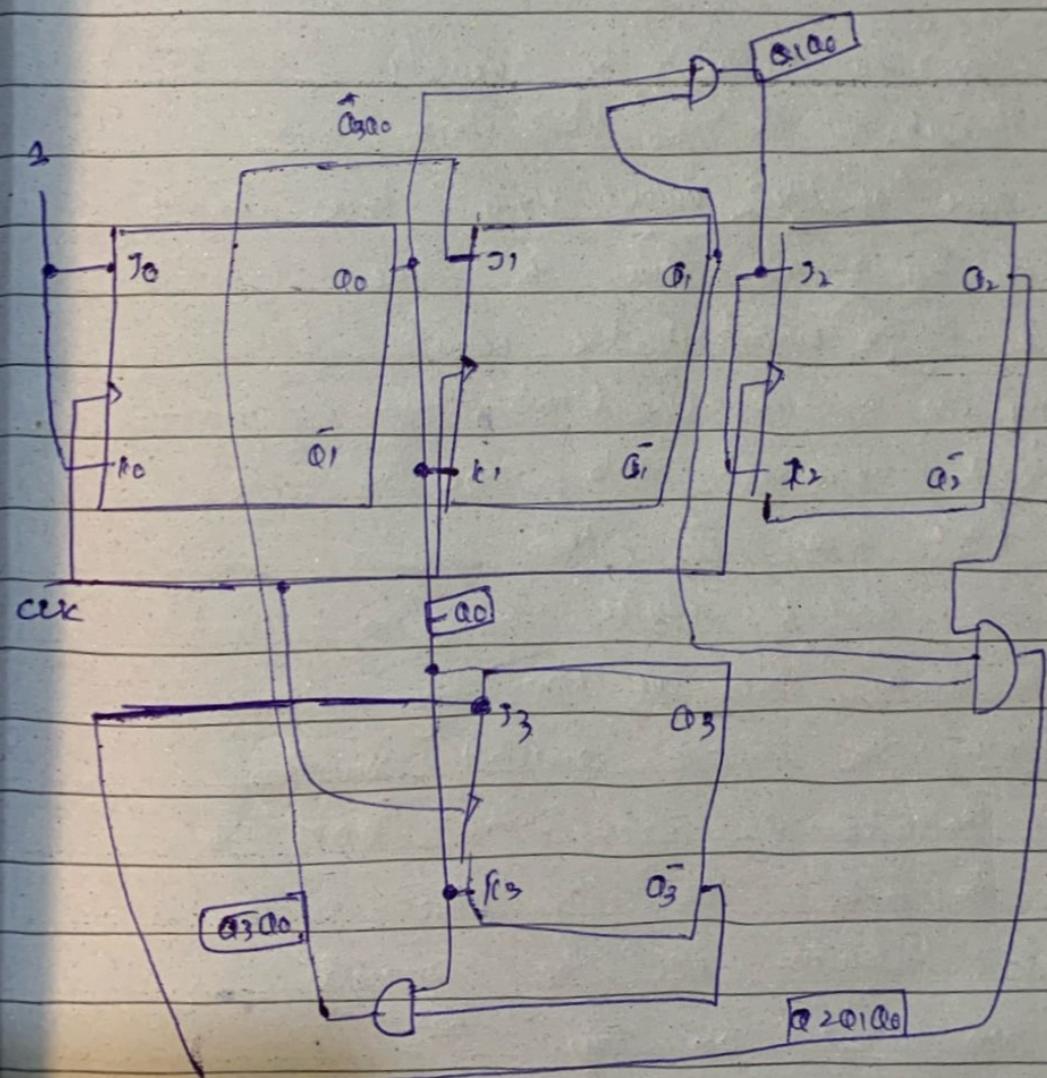
$$k_2 = Q_1 Q_0$$

$$J_1 = \bar{Q}_3 Q_0$$

$$k_1 = Q_0$$

$$J_0 = 1$$

$$k_0 = 1$$



Q) in lock-out condition we see whether the counter is self correcting or not.

Q) why we need to check the lock-out condition?

A, bcz as you know the counter is not going through all the possible states and here some of the output states are unused states. so, by chance due to some external interference if the output of the counter goes into the any one of the unused state, then automatically it should comeback into one of the valid state and if the counter comes out of this unused state in the next few clock cycles, then we can say that the counter is the self correcting counter and if the counter is not able to comeback ~~to~~ after the few clock cycles and if it still remains in the unused state, then we can say that the counter is in the lockout condition. meaning that the counter got locked in the unused state and it is not able to come out of it.

For this we need to modify our circuit.

### ② lock-out condition.

we have our current present state and on the basis of inputs we find the next state.

$$J_3 = Q_2 Q_1 Q_0 \quad J_2 = K_2 = Q_1 Q_0$$

$$K_3 = Q_0$$

$$J_1 = Q_3 Q_0 \quad K_1 = Q_0$$

$$J_0 = K_0 = 1$$

ie: follows JK rule

means next state remains same  
since  $J_3 = K_3 = 0$   $\rightarrow$  find by using 4 equations

Present state

next state

~~Present input~~

$Q_3 Q_2 Q_1 Q_0$	$Q_3 + Q_2 + Q_1 + Q_0 + \text{pulse}$	$J_3 \quad K_3 \quad J_2 \quad K_2 \quad J_1 \quad K_1 \quad J_0 \quad K_0$
1 0 1 0	1 0 1 1	0 0 0 0 0 0 1 1
1 0 1 1	0 1 0 0	0 1 0 0 0 1 1 1
1 1 0 0	1 1 0 1	0 0 0 0 0 0 1 1
1 1 0 1	0 1 0 0	0 1 0 0 0 1 1 1
1 1 1 0	1 1 1 1	0 0 0 0 0 0 1 1
1 1 1 1	0 0 0 0	1 1 1 1 0 1 1 1

$10 \rightarrow 11 \rightarrow 4$

~~4~~

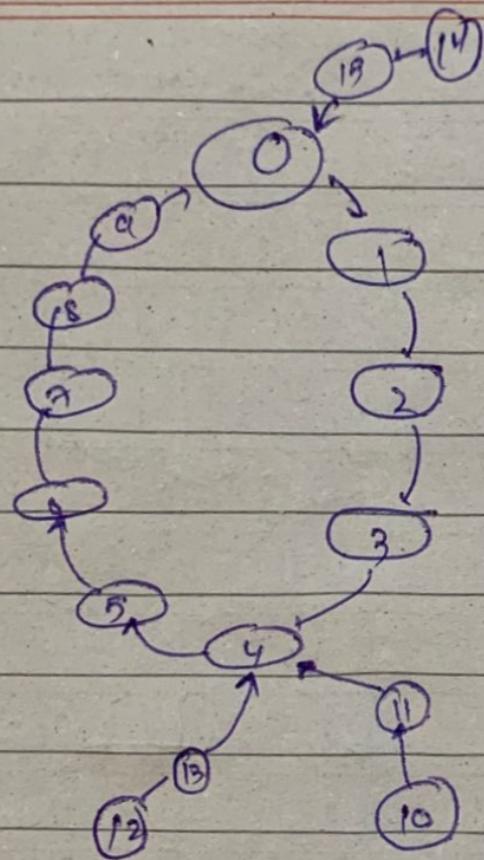
$12-13 \rightarrow 4$

$14-15 \rightarrow 0$

Let's represent them in state diagram.

diagram.

0 0  
↓ ↓  
0 0



① as we can see the count  
when the counter is in any unused  
state & after few cycles if it is going  
in to the used state (valid state) means  
counter is self correcting

Q<sub>0</sub> Q<sub>1</sub>

000 → 000

001 → 001

Q<sub>1</sub> / Q<sub>0</sub>

010

011

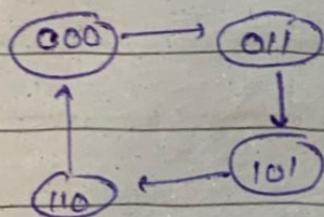
Eg. 2

- make a synchronous counter which counts from the following  
0, 3, 5, 6, 0, ... etc.

2

① 3-flipflop - (0-7)

② State Diagram.



Q<sub>2</sub>    Q<sub>1</sub>    Q<sub>0</sub>

0    0    0

0    1    1

1    0    1

1    1    0

0    0    1

0    1    0

1    0    0

1    1    1

don't care

+ unused output state

J

clock

111

001

010

② using D flipflop.

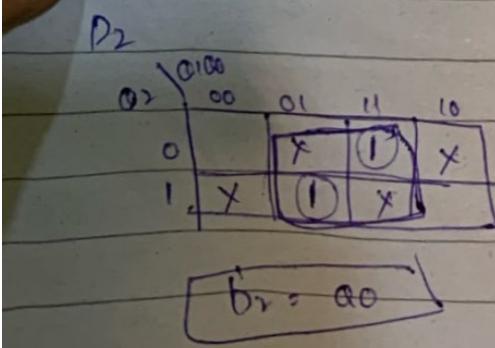
Excitation table of D-flipflop.

$Q_n$	$Q_{n+1}$	D
0	0	0
0	1	1
1	0	0
1	1	1

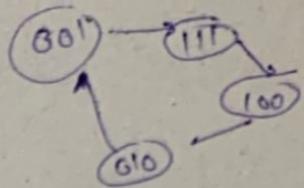
~~$Q_2 \ Q_1 \ Q_0 = D$~~

Present state	Next state	Required excitation
$Q_2 \ Q_1 \ Q_0$	$Q_2 \ Q_1 \ Q_0$	$D_2 \ D_1 \ D_0$
0 0 0	0 1 1	0 1 1
0 1 1	1 0 1	1 0 1
1 0 1	1 1 0	1 1 0
1 1 0	0 0 0	0 0 0

: 4 don't care terms



000 - X  
001 - X  
010 - X  
100 - X  
111 - X



$D_1$	$Q_{10}$	$Q_{00}$	$Q_{11}$	$Q_{11}$
$Q_2$	00	01	11	10
0	1	x		x
1	x	1	x	

$$D_1 = \bar{Q}_1$$

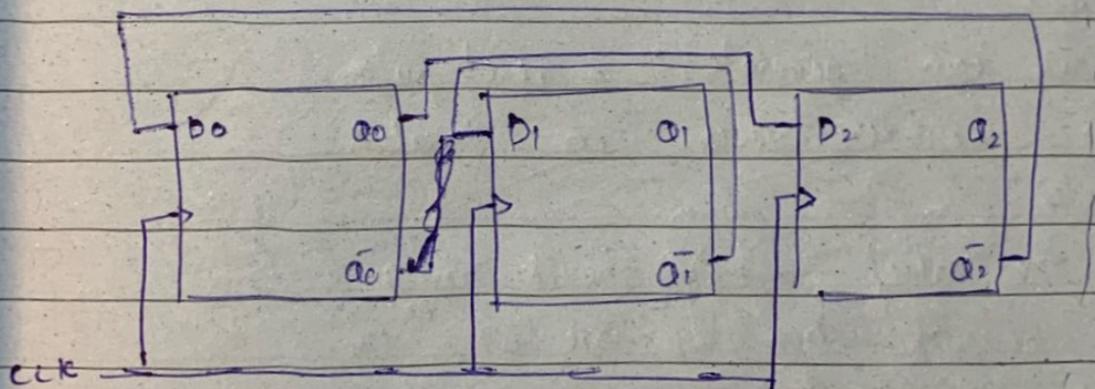
$D_0$	$Q_{10}$	$Q_{00}$	$Q_{11}$	$Q_{11}$
$Q_2$	00	01	11	10
0	1	x	1	x
1	x	1	x	

$$D_0 = \bar{Q}_2$$

$$D_0 = \bar{Q}_2$$

$$D_1 = \bar{Q}_1$$

$$D_2 = \bar{Q}_0$$

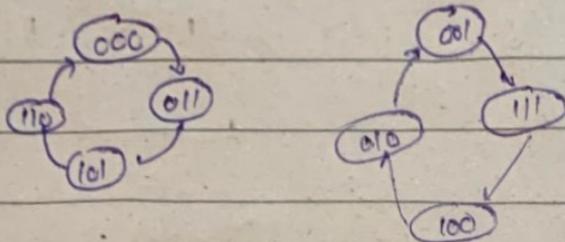


② check the lock-out condition

for  $Q_2 = 1$

Present state	Present input	Next state
$Q_2 \ Q_1 \ Q_0$	$D_2 \ D_1 \ D_0$	$Q_2+ \ Q_1+ \ Q_0+$
0 0 1	1 1 1	1 1 1
0 1 0	0 0 1	0 0 1
1 0 0	0 1 0	0 1 0
1 1 1	1 0 0	1 0 0

lock-out state dry



counter is  
not  
self  
correcting

bcz  
if it

not  
going back

to invalid  
state after  
few cycles.

- Now
- ② we can generate a reset pulse when counter goes in invalid state
- The reset input should bring the counter in any one of the valid state (000)

2. Elimination of

lock-out condition

any invalid

state

$Q_2$	$Q_1$	$Q_0$	R
0	0	1	1
0	1	0	1
1	0	0	1
1	1	1	1

J K

$$\begin{aligned}
 & (A \bar{B}) \bar{C} \\
 & (\bar{A} \bar{B} + A \bar{B}) \bar{C} \\
 & \bar{A} \bar{B} \bar{C} + \bar{A} B \bar{C} \\
 & \bar{A} B \bar{C} + \bar{A} \bar{B} C \\
 & \bar{A} B \bar{C} + \bar{A} \bar{B} \bar{C}
 \end{aligned}$$

Q<sub>2</sub>

	00	01	11	10
0	1			
1		1	1	1

$$R = Q_2 \bar{Q}_1 \bar{Q}_0 + \bar{Q}_2 Q_1 \bar{Q}_0 + Q_2 Q_1 \bar{Q}_0 + Q_2 \bar{Q}_1 Q_0$$

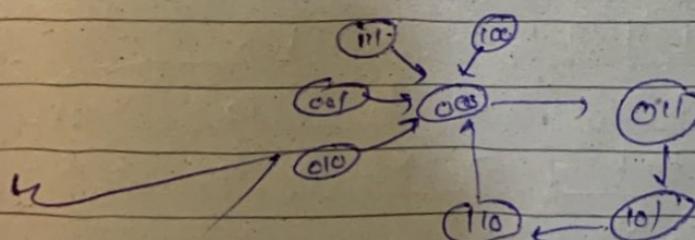
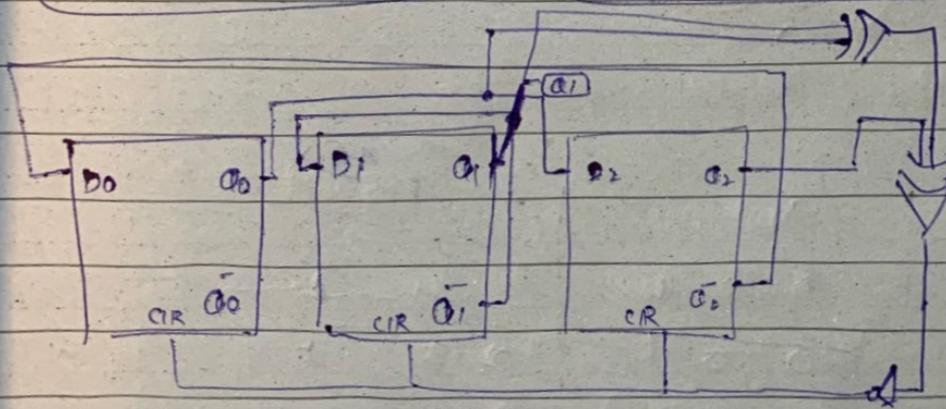
$$R = Q_2 (\bar{Q}_1 \bar{Q}_0 + Q_1 \bar{Q}_0) + Q_2 (Q_1 \bar{Q}_0 + Q_1 Q_0)$$

$$Q_2 (\bar{Q}_1 \oplus \bar{Q}_0) + Q_2 (\bar{Q}_1 \oplus Q_0)$$

$$R = \boxed{Q_2 \oplus Q_1 \oplus Q_0}$$

$$\overline{R} = \boxed{Q_2 \oplus Q_1 \oplus Q_0} \quad \text{or} \quad R = \boxed{Q_2 \oplus Q_1 \oplus Q_0}$$

if any individual state comes it will give one by parity it through NO. we can take it to CLR



③ Design counter to count

seq: ~~2, 0, 1, 2,~~

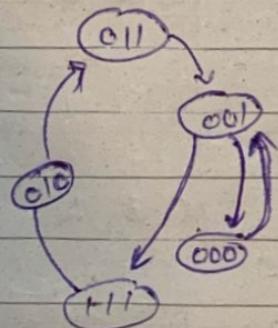
2, 1, 0, 1, 2, 2

using 74161

There are 3 diff. states

so a MOD-3 counter i.e. 3-flipflops.

④ State diagram



P-S	N-S	Required excitation
000, 001, 010	001 + 010 + 000	J <sub>2</sub> K <sub>2</sub> J <sub>1</sub> K <sub>1</sub> J <sub>0</sub> K <sub>0</sub>
001	000	0 X X 1 X 0
000	001	0 X 0 X X 1
000	111	1 X 1 X X 0
111	010	X 1 X 0 X 1
010	0+1	0 X X 0 1 X
100	X X*	V Y Y
101	X XX	Y Y Y
110	XX <sup>don't care</sup>	V V Y

$$\begin{array}{l} \theta = -1 \\ J_2 = 1 \text{ Kc} \\ J_2 = 1 \text{ Kc} \end{array}$$

$J_2$

		00	01	11	10
		00	01	11	10
Q2	0	(1)			
	1	x	x	x	x

$K_2$

		00	01	11	10
		00	01	11	10
Q2	0	x	x	x	y
	1	x	1	x	x

$$J_2 = \bar{Q}_1 Q_0$$

$$K_2 = 1$$

$J_1$

		00	01	11	10
		00	01	11	10
Q2	0	(1)	x	x	x
	1	x	x	x	x

$K_1$

		00	01	11	10
		00	01	11	10
Q2	0	x	x	1	
	1	x	x		x

$$J_1 = Q_0$$

$$K_1 = \bar{Q}_2 Q_0$$

$J_0$

		00	01	11	10
		00	01	11	10
Q2	0	1	y	y	1
	1	x	x	x	y

$K_0$

		00	01	11	10
		00	01	11	10
Q2	0	x	1		x
	1	x	x	1	x

$$J_0 = 1$$

$$\cancel{K_0 = Q_2}$$

$$K_0 = \cancel{Q_1} + Q_2$$

$$J_2 = \bar{Q}_1 Q_0$$

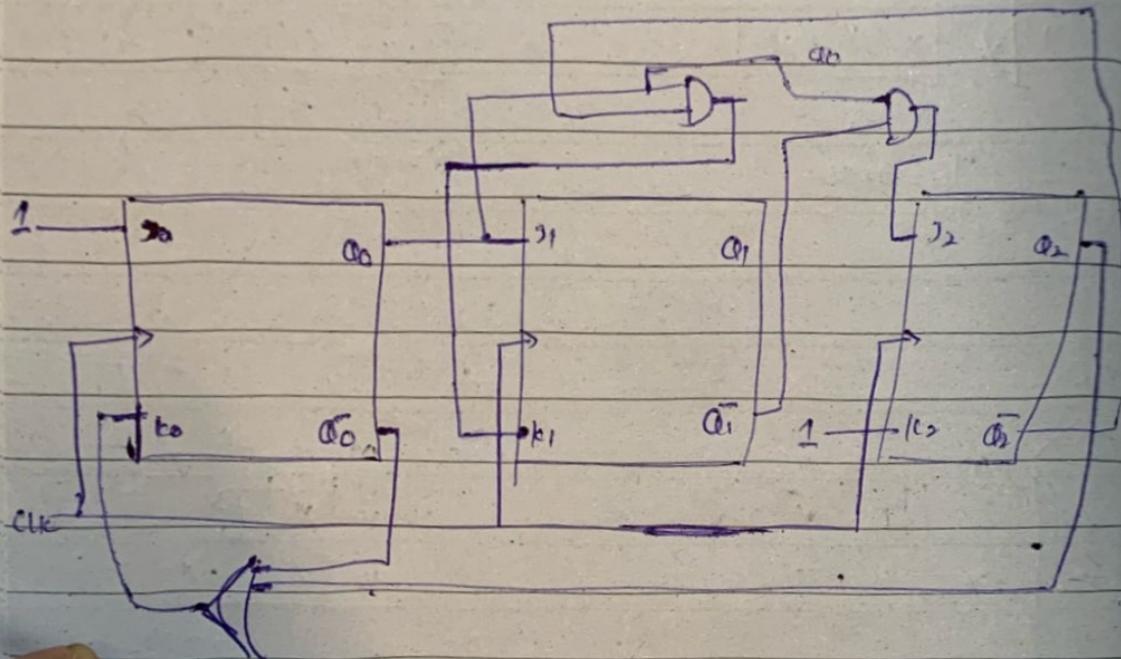
$$K_2 = 1$$

$$J_1 = Q_0$$

$$K_1 = \bar{Q}_2 Q_0$$

$$J_0 = 1$$

$$K_0 = \bar{Q}_1 + Q_2$$



⑥ checking lockout condition

P.S	P. Input	Next stat
Q2 Q1 Q0	J2 K2 J1 K1 J0 K0	Q2' Q1' Q0'
1 0 0	0 1 0 0 1 1	0 0 1
1 0 1	1 1 1 0 1 1	0 1 0
1 1 0	0 1 0 0 , 1	0 1 1

