

DLD Lab 11

(Software)

23K-2001

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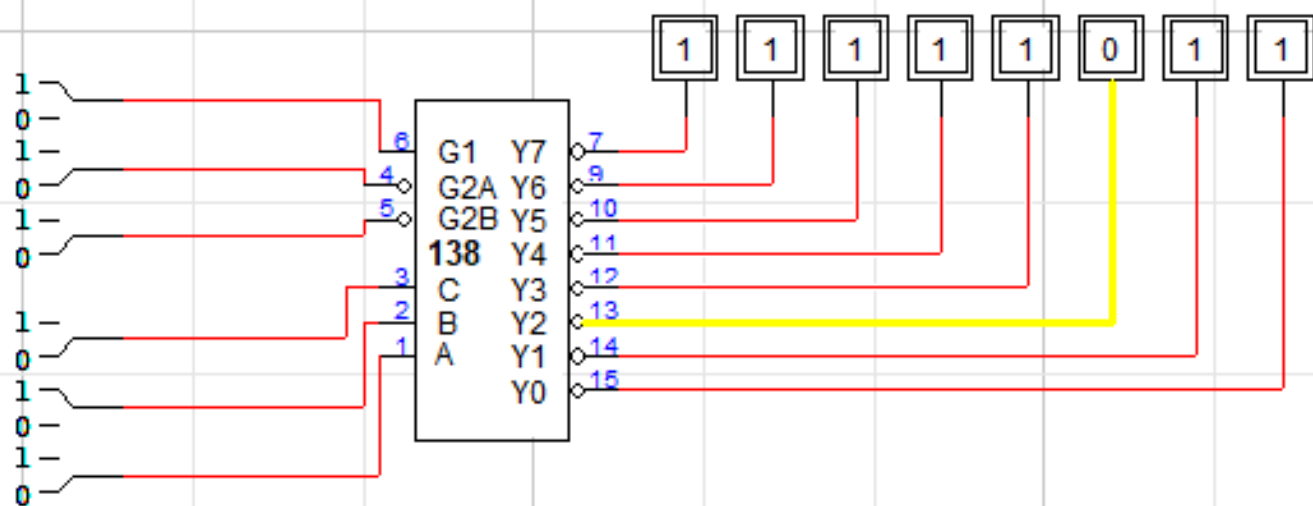
BCS 2-J

Exercise#1:

[illegible]

Exercise#1

Implementation of 3-8-line Decoder using IC 74LS138



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Exercise#2:

Inputs (LT)'=1 , (RBI)'=1				Outputs						
A3	A2	A1	A0	a'	b'	c'	d'	e'	f'	g'
0	0	0	0	1	1	1	1	1	1	0
0	0	0	1	0	1	1	0	0	0	0
0	0	1	0	1	1	0	1	1	0	1
0	0	1	1	1	1	1	1	0	0	1
0	1	0	0	0	1	1	0	0	1	1
0	1	0	1	1	0	1	1	0	1	1
0	1	1	0	0	0	1	1	1	1	1
0	1	1	1	1	1	1	0	0	0	0
1	0	0	0	1	1	1	1	1	1	1
1	0	0	1	1	1	1	0	0	1	1

Digit
0
1
2
3
4
5
6
7
8
9

Exercise#2

Implementation of BCD to Seven Segment Decoder using IC 74LS47

