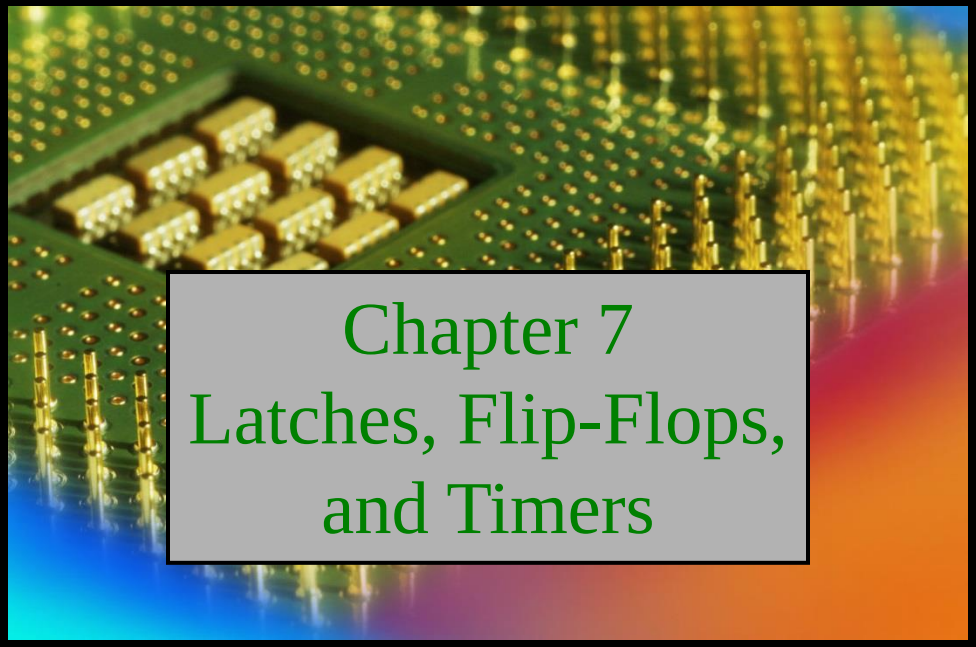
EE-227
Digital Logic Design

Fall-2018



Chapter 7
Latches, Flip-Flops, and Timers

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Latches

The latch is a type of temporary storage device that has two stable states (*bistable*) and is normally placed in a category separate from that of flip-flops.

Latches are similar to flip-flops because they are bistable devices that can reside in either of two states using a feedback arrangement, in which the outputs are connected back to the opposite inputs.

The main difference between latches and flip-flops is in the method used for changing their state.

InfoNote

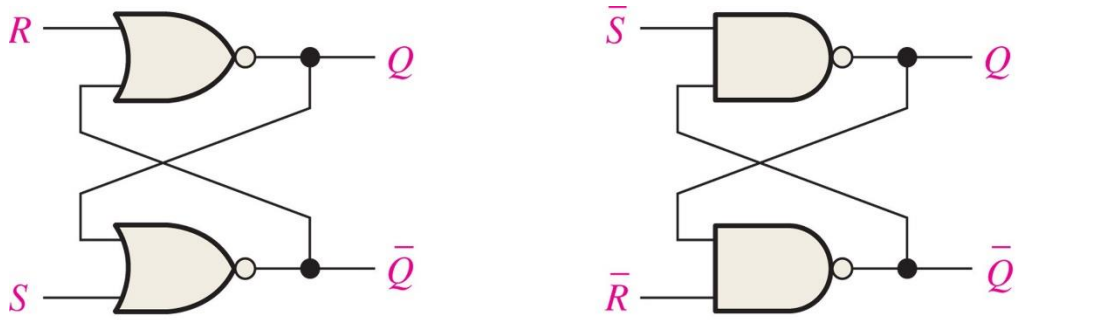
Latches are sometimes used for multiplexing data onto a bus.

For example, data being input to a computer from an external source have to share the data bus with data from other sources.

When the data bus becomes unavailable to the external source, the existing data must be temporarily stored, and latches placed between the external source and the data bus may be used to do this.

The S-R (SET-RESET) Latch

A latch is a type of bistable logic device or **multivibrator**. An active-HIGH input S-R (SET-RESET) latch is formed with two cross-coupled NOR gates, as shown in Figure 7–1(a); an active-LOW input $\overline{S}$. $\overline{R}$ latch is formed with two cross-coupled NAND gates, as shown in Figure 7–1(b). Notice that the output of each gate is connected to an input of the opposite gate. This produces the regenerative **feedback** that is characteristic of all latches and flip-flops.



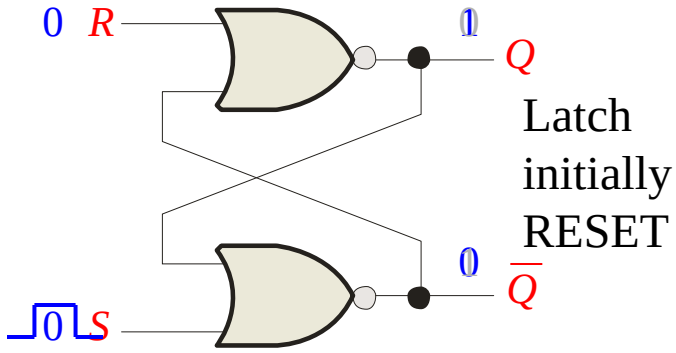
(a) Active-HIGH input S-R latch (b) Active-LOW input $\overline{S}$-$\overline{R}$ latch

FIGURE 7–1 Two versions of SET-RESET (S-R) latches.

Latches

The active-HIGH *S*-*R* latch is in a stable (latched) condition when both inputs are LOW.

Assume the latch is initially RESET ($Q = 0$) and the inputs are at their inactive level (0). To SET the latch ($Q = 1$), a momentary HIGH signal is applied to the *S* input while the *R* remains LOW.

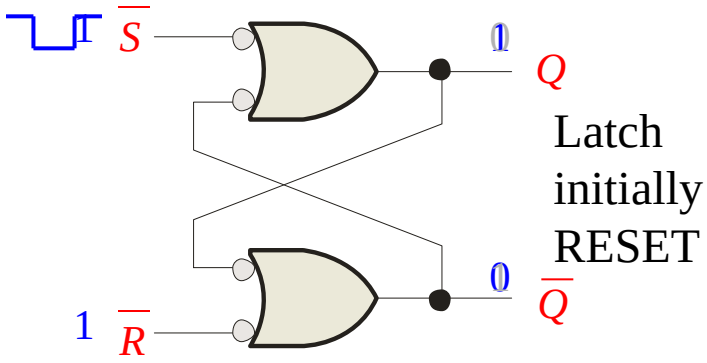


To RESET the latch ($Q = 0$), a momentary HIGH signal is applied to the *R* input while the *S* remains LOW.

Latches

The active-LOW $\overline{S}$-$\overline{R}$ latch is in a stable (latched) condition when both inputs are HIGH.

Assume the latch is initially RESET ($Q = 0$) and the inputs are at their inactive level (1). To SET the latch ($Q = 1$), a momentary LOW signal is applied to the $\overline{S}$ input while the $\overline{R}$ remains HIGH.



To RESET the latch a momentary LOW is applied to the $\overline{R}$ input while $\overline{S}$ is HIGH.

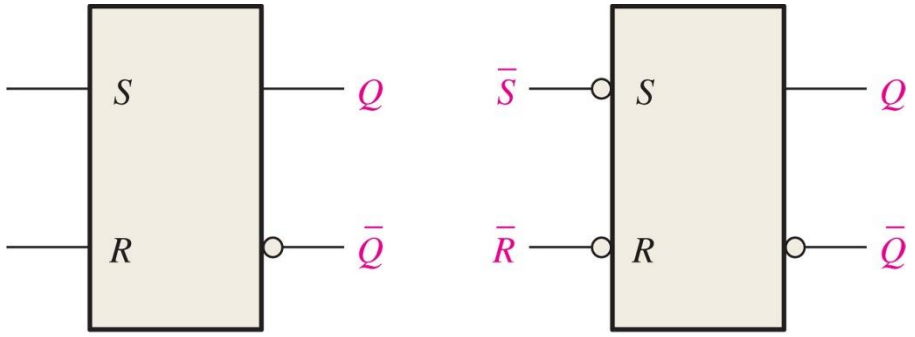
Never apply an active set and reset at the same time (invalid).

TABLE 7–1

Truth table for an active-LOW input $\overline{S}$-$\overline{R}$ latch.

Inputs		Outputs		
$\overline{S}$	$\overline{R}$	Q	$\overline{Q}$	Comments
1	1	NC	NC	No change. Latch remains in present state.
0	1	1	0	Latch SET.
1	0	0	1	Latch RESET.
0	0	1	1	Invalid condition

Logic symbols for both the active-HIGH input and the active-LOW input latches are shown in Figure 7–4.



(a) Active-HIGH input S-R latch

(b) Active-LOW input $\overline{S}$-$\overline{R}$ latch

Figure 7–4

EXAMPLE 7–1

If the $\overline{S}$ and $\overline{R}$ waveforms in Figure 7–5(a) are applied to the inputs of the latch in Figure 7–4(b), determine the waveform that will be observed on the Q output. Assume that Q is initially LOW.

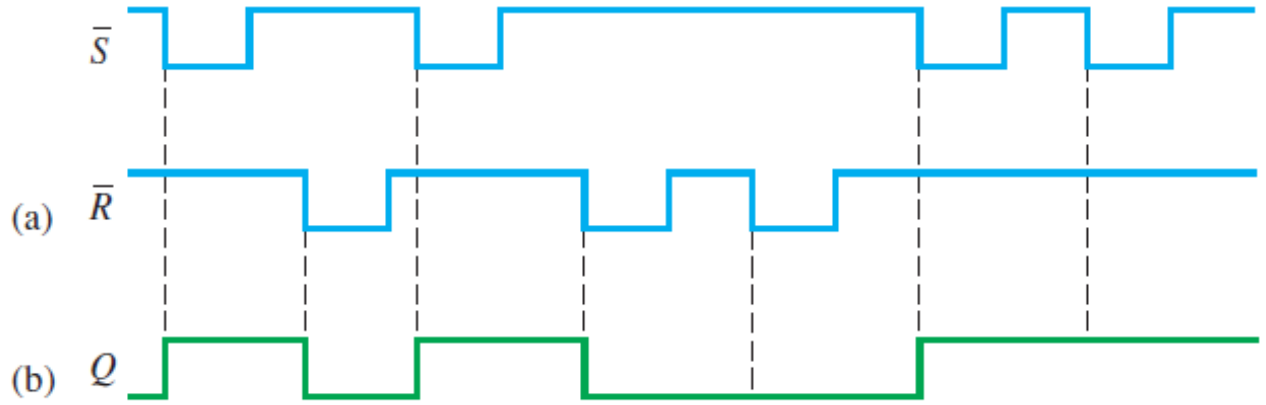


FIGURE 7–5

Solution

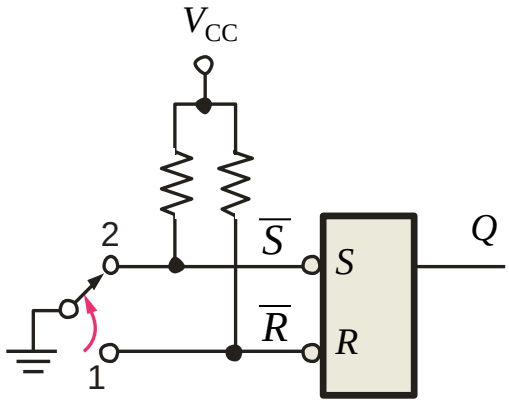
See Figure 7–5(b).

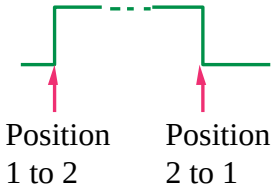
Latches

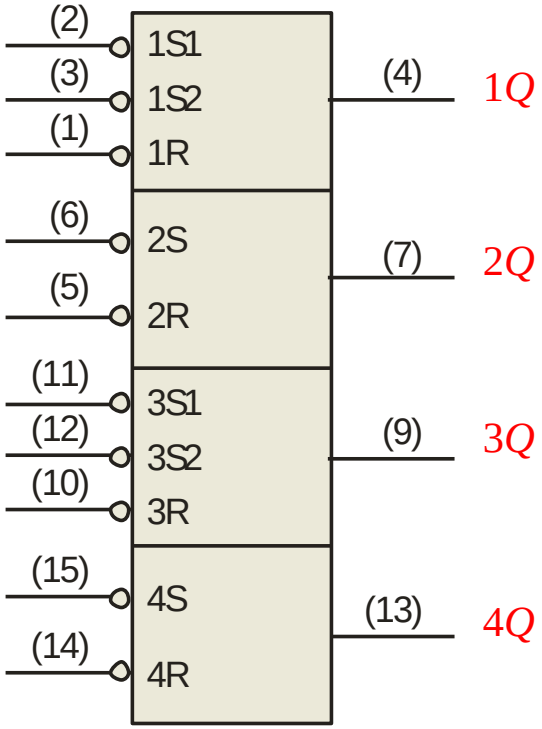
The active-LOW $\overline{S}$-$\overline{R}$ latch is available as the 74LS279A IC.

It features four internal latches with two having two $\overline{S}$ inputs. To SET any of the latches, the $\overline{S}$ line is pulsed low. It is available in several packages.

$\overline{S}$-$\overline{R}$ latches are frequently used for switch debounce circuits as shown:





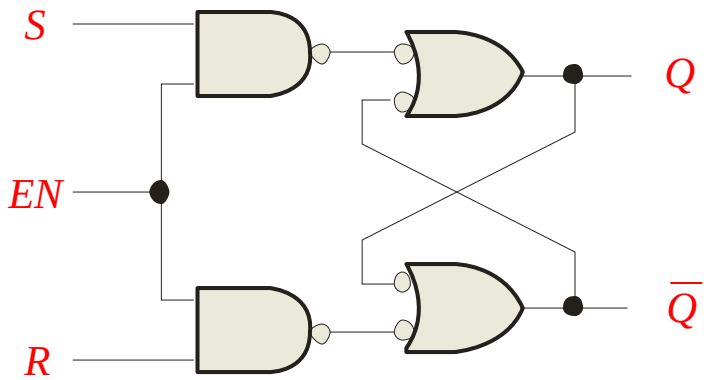


74LS279A

Latches

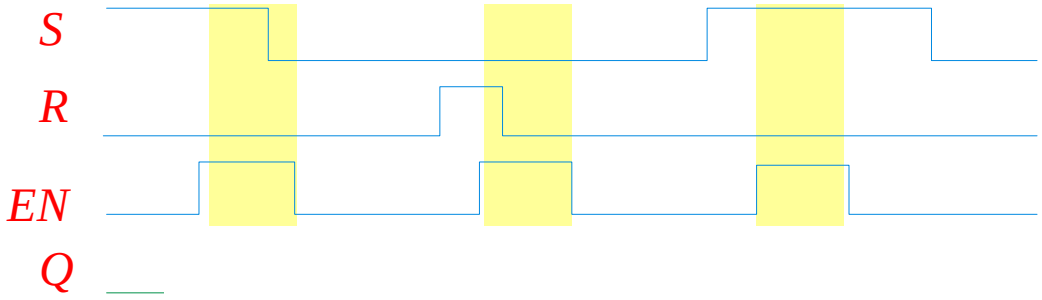
A gated latch is a variation on the basic latch.

The gated latch has an additional input, called enable (*EN*) that must be HIGH in order for the latch to respond to the *S* and *R* inputs.



Example Show the *Q* output with relation to the input signals. Assume *Q* starts LOW.

Solution Keep in mind that *S* and *R* are only active when *EN* is HIGH.



EXAMPLE 7–2

Determine the *Q* output waveform if the inputs shown in Figure 7–9(a) are applied to a gated S-R latch that is initially RESET.

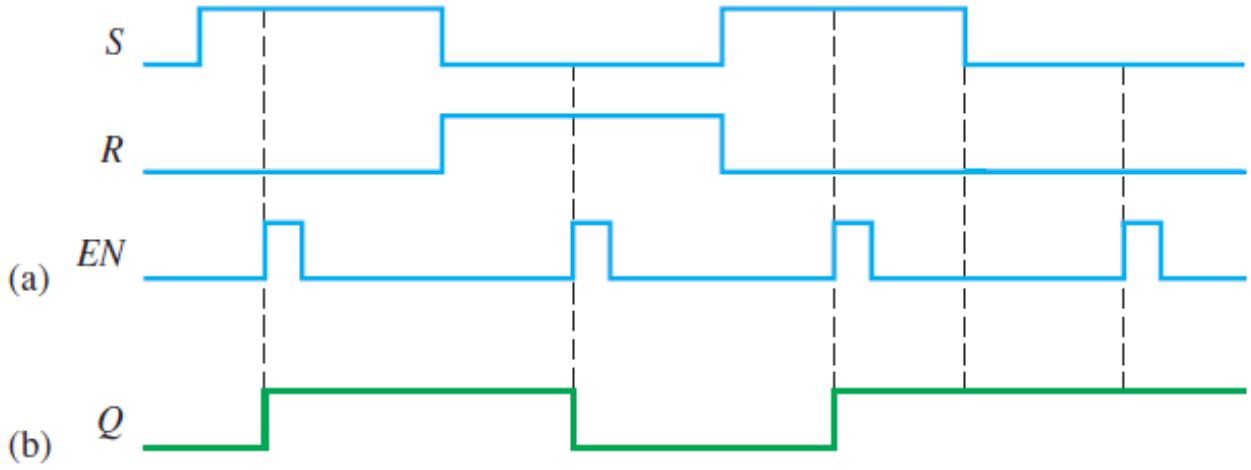


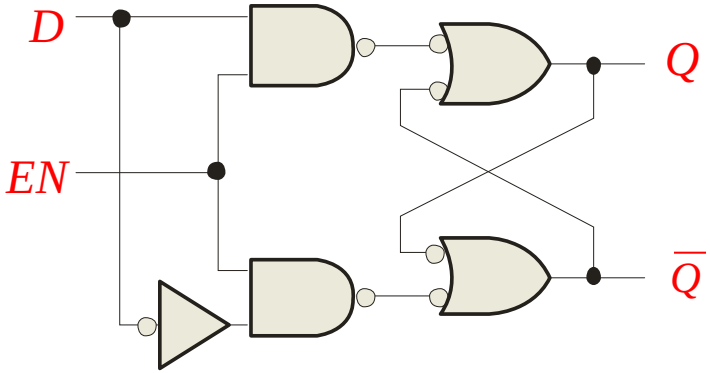
FIGURE 7–9

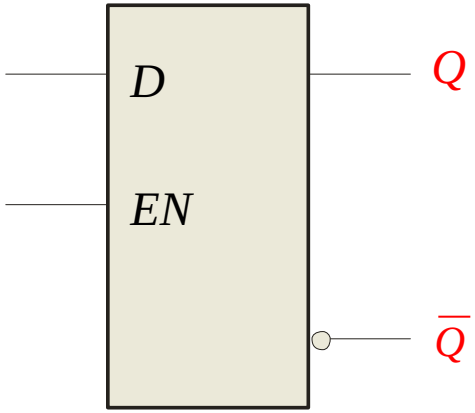
Solution

The *Q* waveform is shown in Figure 7–9(b). When *S* is HIGH and *R* is LOW, a HIGH on the *EN* input sets the latch. When *S* is LOW and *R* is HIGH, a HIGH on the *EN* input resets the latch. When both *S* and *R* are LOW, the *Q* output does not change from its present state.

Latches

The *D* latch is a variation of the *S*-*R* latch but combines the *S* and *R* inputs into a single *D* input as shown:





A simple rule for the *D* latch is:

Q follows *D* when the Enable is active.

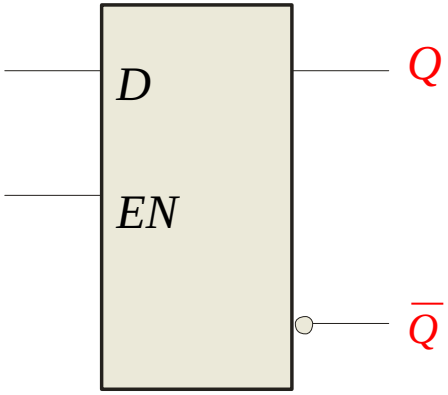
Latches

The truth table for the *D* latch summarizes its operation. If *EN* is LOW, then there is no change in the output and it is latched.

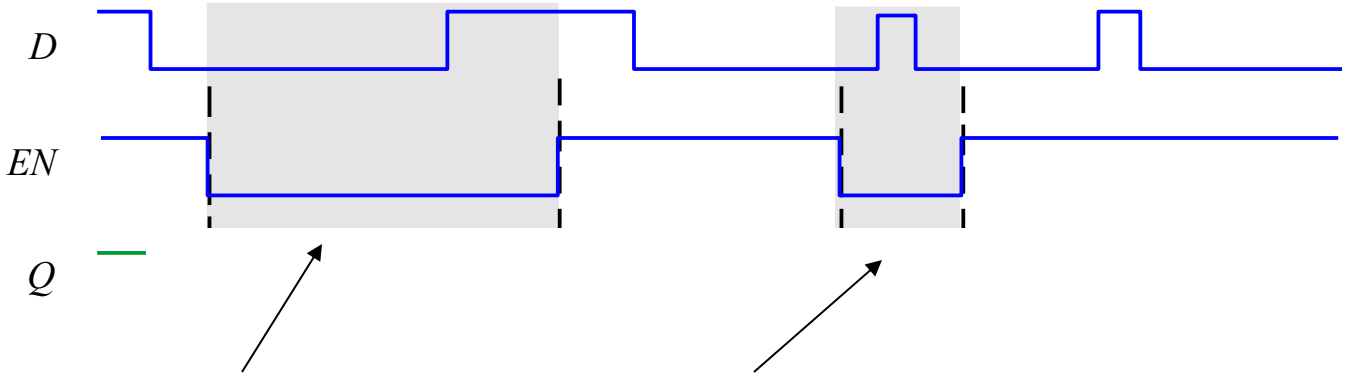
Inputs		Outputs		
D	*EN*	*Q*	$\bar{Q}$	Comments
0	1	0	1	RESET
1	1	1	0	SET
X	0	Q_0	$\bar{Q}_0$	No change

Latches

Example



Determine the *Q* output for the *D* latch, given the inputs shown.



Notice that the Enable is not active during these times, so the output is latched.

InfoNote

Semiconductor memories consist of large numbers of individual cells. Each storage cell holds a 1 or a 0.

One type of memory is the Static Random Access Memory or SRAM, which uses flip-flops for the storage cells because a flip-flop will retain either of its two states indefinitely as long as dc power is applied, thus the term *static*.

This type of memory is classified as a volatile memory because all the stored data are lost when power is turned off.

Another type of memory, the Dynamic Random Access Memory or DRAM, uses capacitance rather than flip-flops as the basic storage element and must be periodically refreshed in order to maintain the stored data.

Flip-flops

Flip-flops are synchronous bistable devices, also known as *bistable multivibrators.*

In this case, the term *synchronous* means that the output changes state only at a specified point (leading or trailing edge) on the triggering input called the **clock** (CLK), which is designated as a control input, *C*; that is, changes in the output occur in synchronization with the clock.

Flip-flops are edge-triggered or edge-sensitive whereas gated latches are level-sensitive.

Flip-flops

An **edge-triggered flip-flop** changes state either at the positive edge (rising edge) or at the negative edge (falling edge) of the clock pulse and is sensitive to its inputs only at this transition of the clock.

Two types of edge-triggered flip-flops are covered in this section: D and J-K. The logic symbols for these flip-flops are shown in Figure 7–13.

Notice that each type can be either positive edge-triggered (no bubble at *C* input) or negative edge-triggered (bubble at *C* input).

The key to identifying an edge-triggered flip-flop by its logic symbol is the small triangle inside the block at the clock (*C*) input. This triangle is called the *dynamic input indicator.*

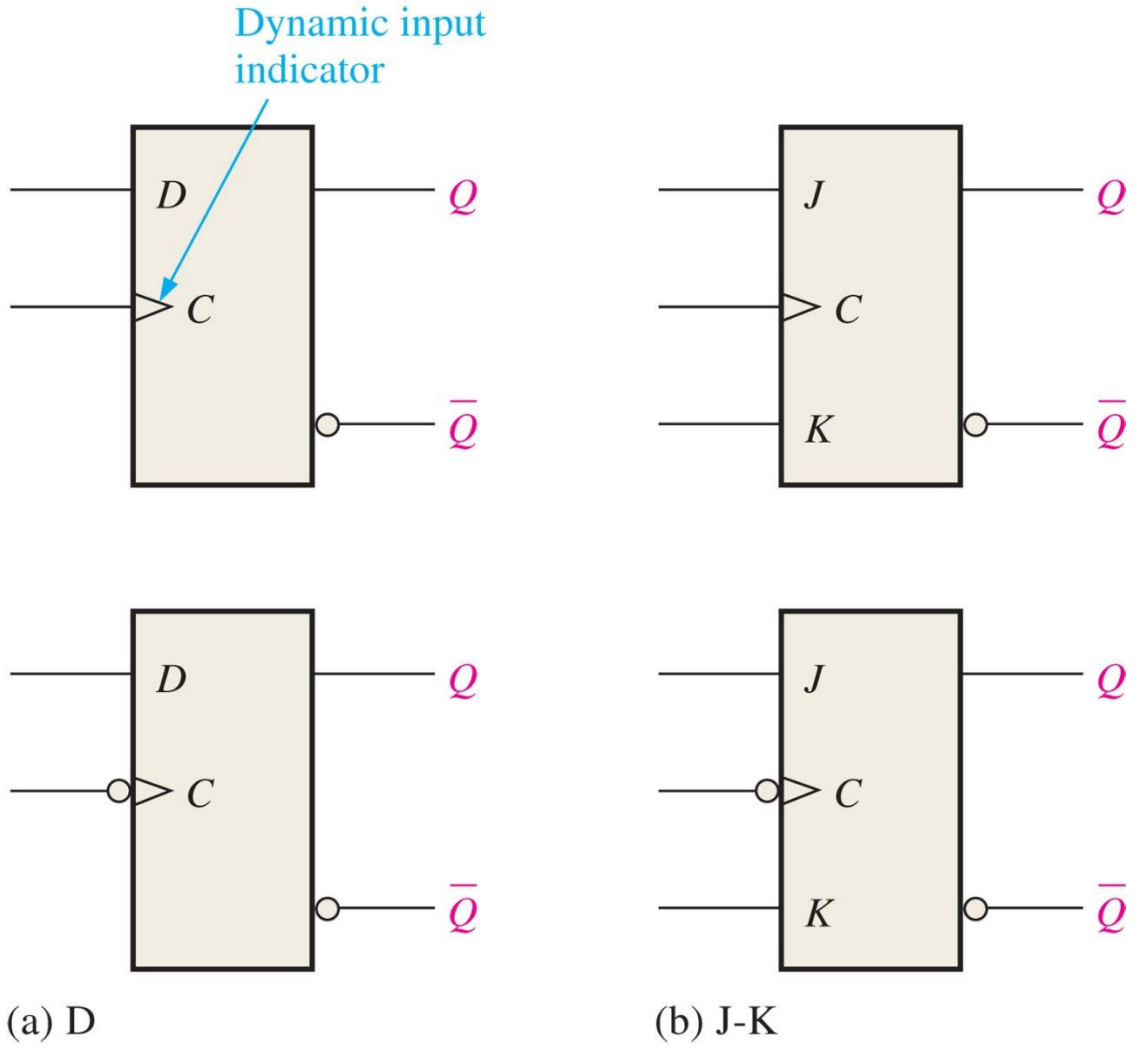
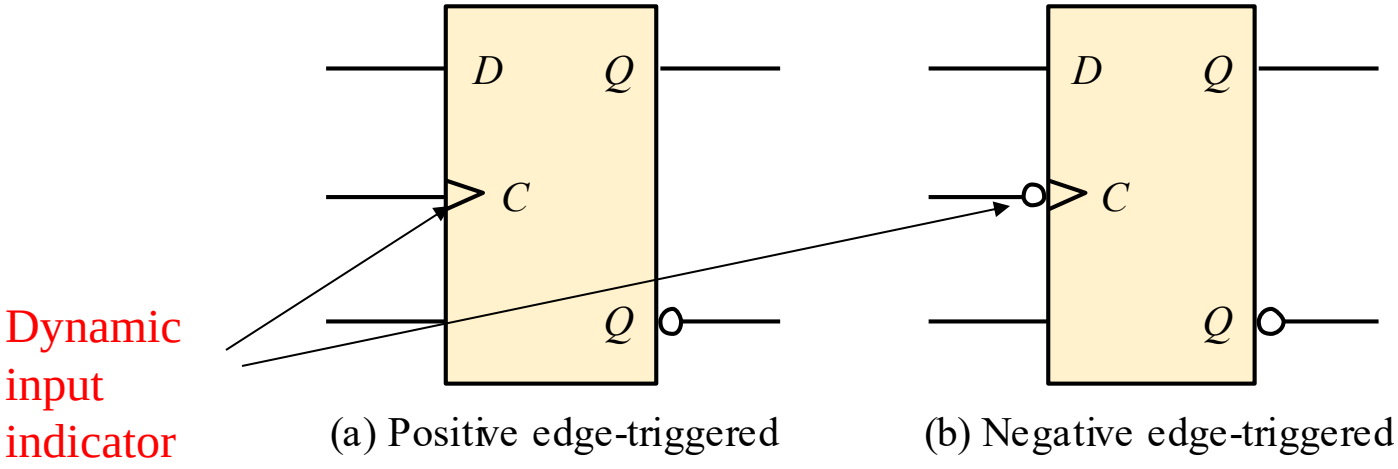


FIGURE 7-13 Edge-triggered flip-flop logic symbols (top: positive edge-triggered; bottom: negative edge-triggered).

Flip-flops

A flip-flop differs from a latch in the manner it changes states. A flip-flop is a clocked device, in which only the clock edge determines when a new bit is entered.

The active edge can be positive or negative.



Flip-flops

The truth table for a positive-edge triggered D flip-flop shows an up arrow to remind you that it is sensitive to its *D* input only on the *rising edge* of the clock; otherwise it is latched. The truth table for a negative-edge triggered D flip-flop is identical except for the direction of the arrow.

Inputs		Outputs		
D	CLK	*Q*	$\overline{Q}$	Comments
1	↑	1	0	SET
0	↑	0	1	RESET

(a) Positive-edge triggered

Inputs		Outputs		
D	CLK	*Q*	$\overline{Q}$	Comments
1	↓	1	0	SET
0	↓	0	1	RESET

(b) Negative-edge triggered

EXAMPLE 7–4

Determine the Q and $\overline{Q}$ output waveforms of the flip-flop in Figure 7–15 for the D and CLK inputs in Figure 7–16(a). Assume that the positive edge-triggered flip-flop is initially RESET.

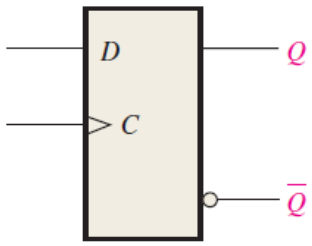


FIGURE 7–15

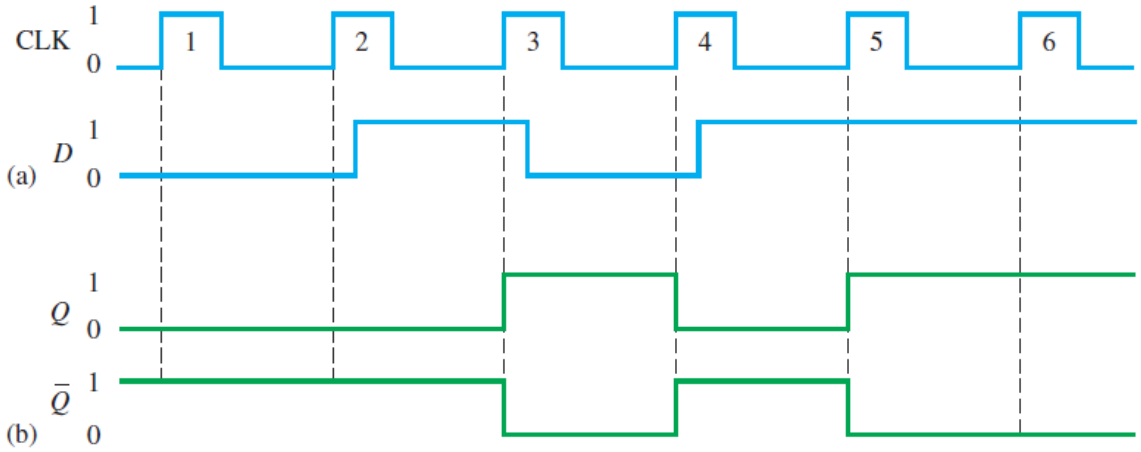


FIGURE 7–16

Solution

1. At clock pulse 1, D is LOW, so Q remains LOW (RESET).
2. At clock pulse 2, D is LOW, so Q remains LOW (RESET).
3. At clock pulse 3, D is HIGH, so Q goes HIGH (SET).
4. At clock pulse 4, D is LOW, so Q goes LOW (RESET).
5. At clock pulse 5, D is HIGH, so Q goes HIGH (SET).
6. At clock pulse 6, D is HIGH, so Q remains HIGH (SET).

Once Q is determined, $\overline{Q}$ is easily found since it is simply the complement of Q. The resulting waveforms for Q and $\overline{Q}$ are shown in Figure 7–16(b) for the input waveforms in part (a).

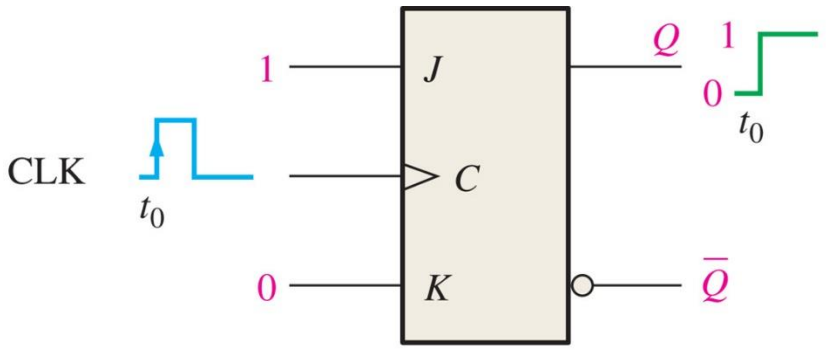
J-K Flip-flop

The *J* and *K* inputs of the ***J-K* flip-flop** are synchronous inputs because data on these inputs are transferred to the flip-flop's output only on the triggering edge of the clock pulse.

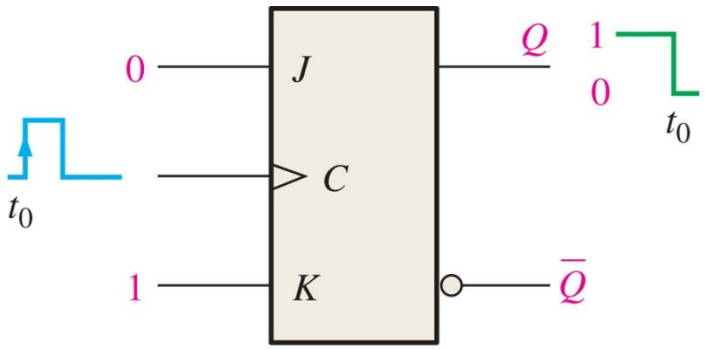
When *J* is HIGH and *K* is LOW, the *Q* output goes HIGH on the triggering edge of the clock pulse, and the flip-flop is SET.

When *J* is LOW and *K* is HIGH, the *Q* output goes LOW on the triggering edge of the clock pulse, and the flip-flop is RESET.

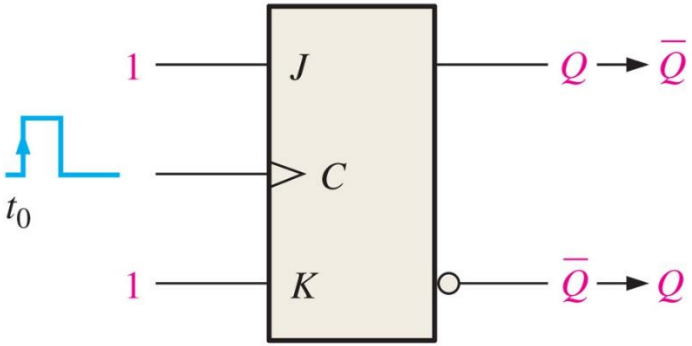
When both *J* and *K* are LOW, the output does not change from its prior state. When *J* and *K* are both HIGH, the flip-flop changes state. This is called the **toggle** mode.



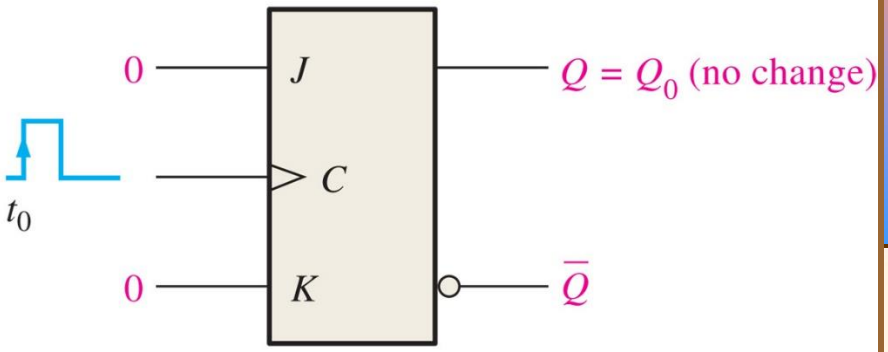
(a) $J = 1$, $K = 0$ flip-flop SETS on positive clock edge. (If already SET, it remains SET.)



(b) $J = 0$, $K = 1$ flip-flop RESETS on positive clock edge. (If already RESET, it remains RESET.)



(c) $J = 1$, $K = 1$ flip-flop changes state (toggle).



(d) $J = 0$, $K = 0$ flip-flop does not change. (If SET, it remains SET; if RESET, it remains RESET.)

FIGURE 7-17 Operation of a positive edge-triggered J-K flip-flop.

Flip-flops

The J-K flip-flop is more versatile than the D flip flop. In addition to the clock input, it has two inputs, labeled *J* and *K*. When both *J* and *K* = 1, the output changes states (toggles) on the active clock edge (in this case, the rising edge).

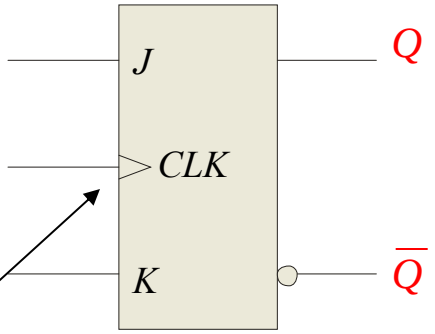
Inputs			Outputs		
J	*K*	CLK	*Q*	$\overline{Q}$	Comments
0	0	↑	Q_0	$\overline{Q}_0$	No change
0	1	↑	0	1	RESET
1	0	↑	1	0	SET
1	1	↑	$\overline{Q}_0$	Q_0	Toggle

The two control inputs are labeled J and K in honor of Jack Kilby, who invented the integrated circuit.

Flip-flops

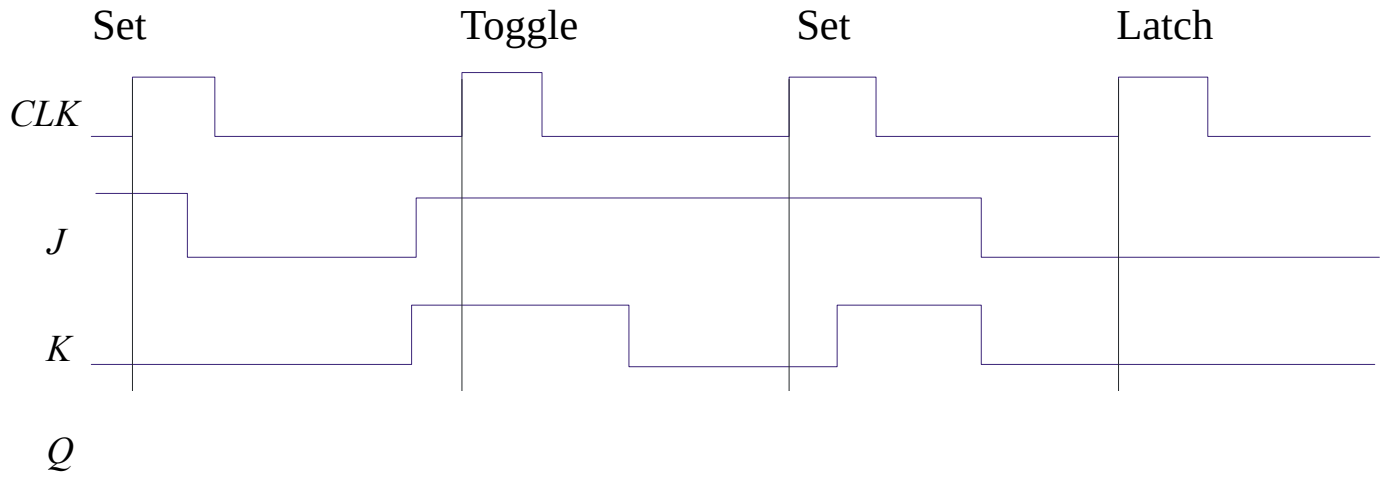
Example

Determine the *Q* output for the *J-K* flip-flop, given the inputs shown.



Notice that the outputs change on the leading edge of the clock.

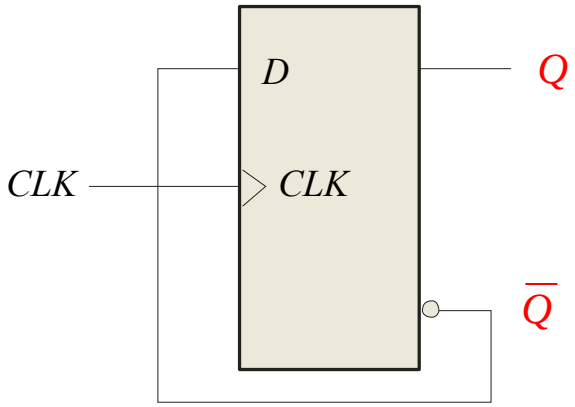
Solution



Flip-flops

A D-flip-flop does not have a toggle mode like the J-K flip-flop, but you can hardwire a toggle mode by connecting $\overline{Q}$ back to *D* as shown. This is useful in some counters as you will see in Chapter 8.

For example, if *Q* is LOW, $\overline{Q}$ is HIGH and the flip-flop will toggle on the next clock edge. Because the flip-flop only changes on the active edge, the output will only change once for each clock pulse.



D flip-flop hardwired for a toggle mode

Asynchronous Preset & Clear Inputs

For the flip-flops discussed, the *D* and *J-K* inputs are called ***synchronous inputs*** because data on these inputs are transferred to the flip-flop's output only on the triggering edge of the clock pulse; that is, the data are transferred synchronously with the clock.

Most integrated circuit flip-flops also have **asynchronous** inputs. These are inputs that affect the state of the flip-flop *independent of the clock*. They are normally labeled **preset** ($\overline{PRE}$) and **clear** ($\overline{CLR}$), or *direct set* (S_D) and *direct reset* (R_D) by some manufacturers.

Asynchronous Preset & Clear Inputs

An active level on the preset input will *set* the flip-flop, and an active level on the clear input will *reset* it. A logic symbol for a D flip-flop with preset and clear inputs is shown in Figure 7–25.

These inputs are active-LOW, as indicated by the bubbles. These *preset* and *clear* inputs must both be kept HIGH for synchronous operation. In normal operation, *preset* and *clear* would not be LOW at the same time.

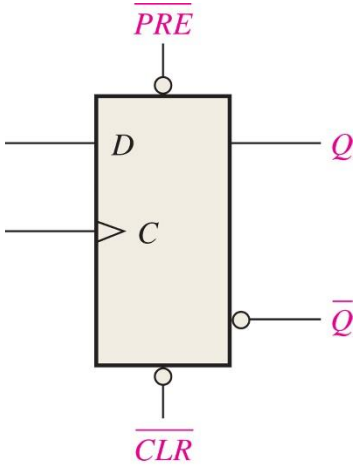


FIGURE 7-25 Logic symbol for a D flip-flop with active-LOW preset and clear inputs.

Asynchronous Preset & Clear Inputs

Figure 7–26 shows the logic diagram for an edge-triggered D flip-flop with active-LOW preset ($\overline{PRE}$) and clear ($\overline{CLR}$) inputs.

This figure illustrates basically how these inputs work. As you can see, they are connected so that they override the effect of the synchronous input, *D* and the clock

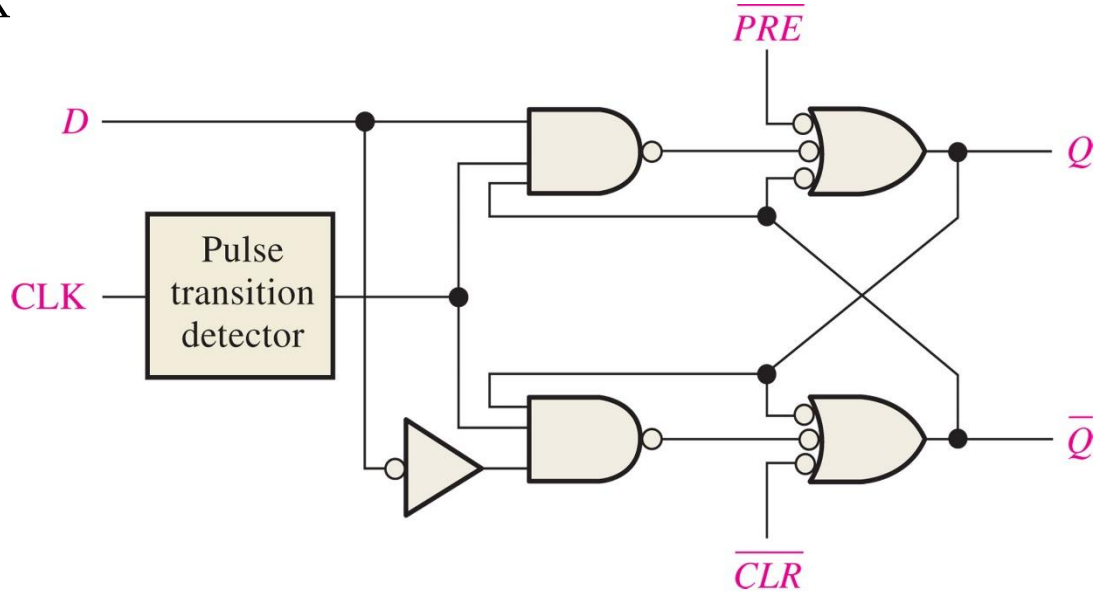
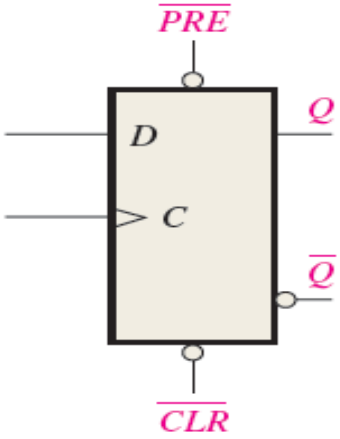
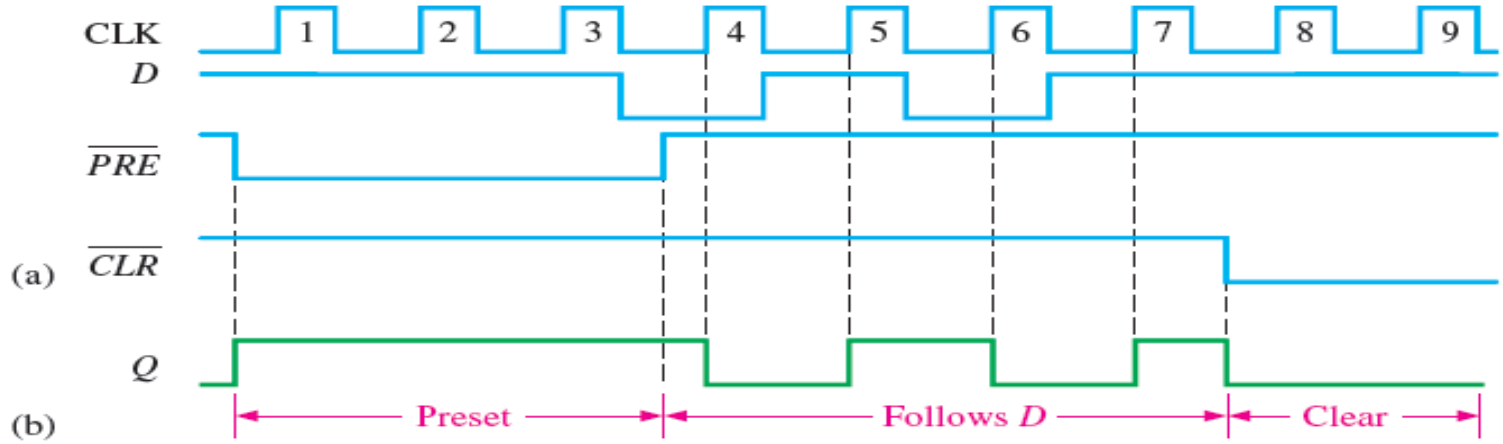


FIGURE 7-26
Logic diagram for a basic D flip-flop with active-LOW preset and clear inputs.

EXAMPLE 7–7

For the positive edge-triggered D flip-flop with preset and clear inputs in Figure 7–27, determine the Q output for the inputs shown in the timing diagram in part (a) if Q is initially LOW.





Solution

1. During clock pulses 1, 2, and 3, the preset ($\overline{PRE}$) is LOW, keeping the flip-flop SET regardless of the synchronous *D* input.

2. For clock pulses 4, 5, 6, and 7, the output follows the input on the clock pulse because both $\overline{PRE}$ and $\overline{CLR}$ are HIGH.

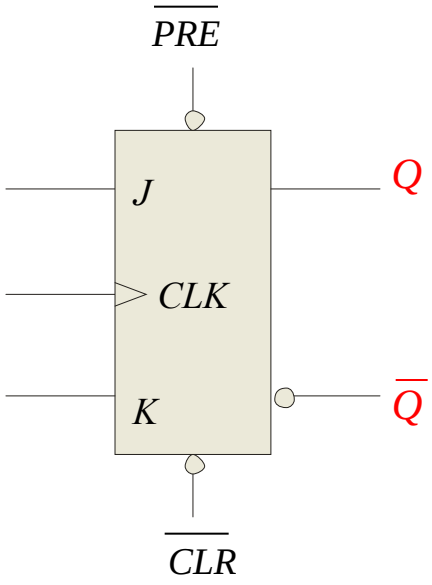
3. For clock pulses 8 and 9, the clear ($\overline{CLR}$) input is LOW, keeping the flip-flop RESET regardless of the synchronous inputs.

The resulting *Q* output is shown in Figure 7–27(b).

J-K Flip-flops

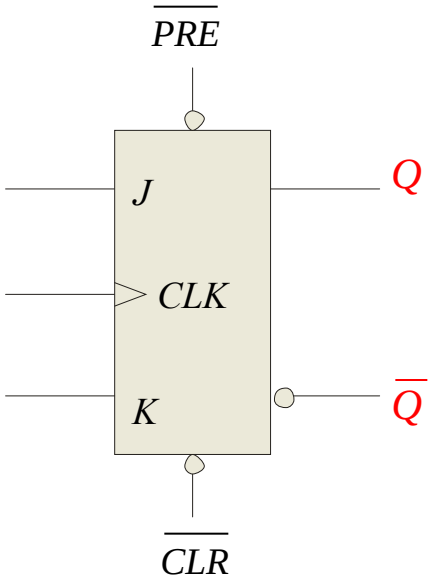
Synchronous inputs are transferred in the triggering edge of the clock (for example the *D* or *J-K* inputs). Most flip-flops have other inputs that are *asynchronous*, meaning they affect the output independent of the clock.

Two such inputs are normally labeled preset ($\overline{PRE}$) and clear ($\overline{CLR}$). These inputs are usually active LOW. A J-K flip flop with active LOW preset and CLR is shown.

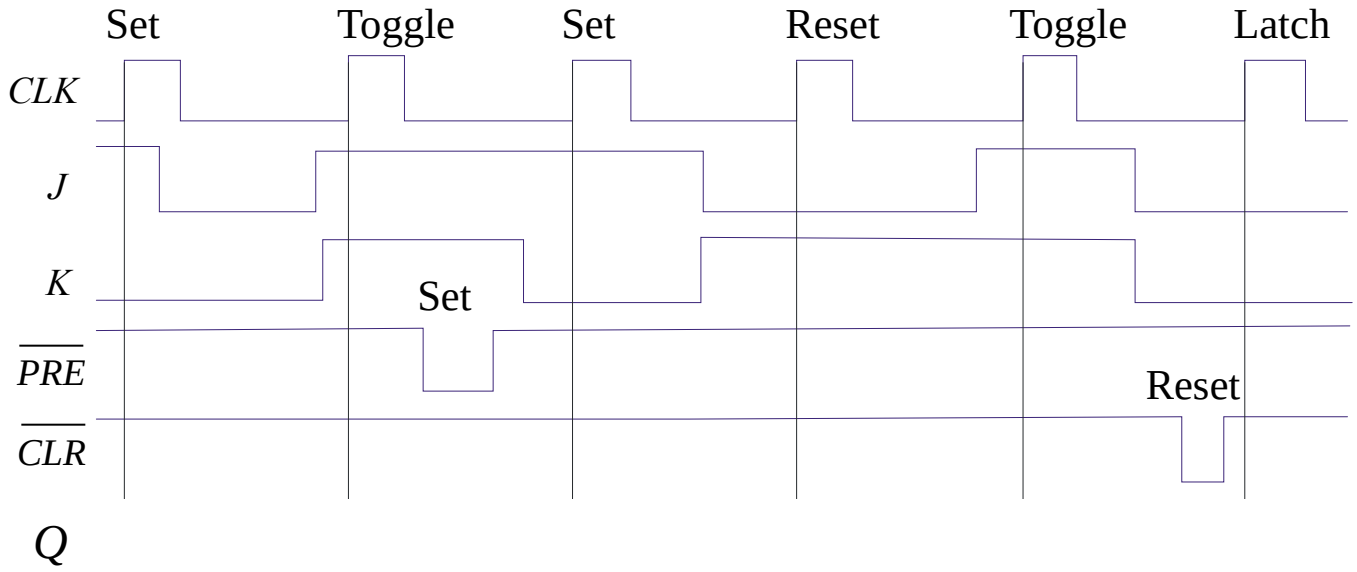


Example

Determine the *Q* output for the *J-K* flip-flop, given the inputs shown.



Solution



Flip-flop Characteristics

The performance, operating requirements, and limitations of flip-flops are specified by several operating characteristics or parameters found on the data sheet for the device.

Generally, the specifications are applicable to all CMOS and bipolar (TTL) flip-flops.

Propagation delay

A **propagation delay time** is the interval of time required after an input signal has been applied for the resulting output change to occur. Four categories of propagation delay times are important in the operation of a flip-flop:

1. Propagation delay t_{PLH} as measured from the triggering edge of the clock pulse to the LOW-to-HIGH transition of the output. This delay is illustrated in Figure 7–31(a).

2. Propagation delay t_{PHL} as measured from the triggering edge of the clock pulse to the HIGH-to-LOW transition of the output. This delay is illustrated in Figure 7–31(b).

Propagation delay

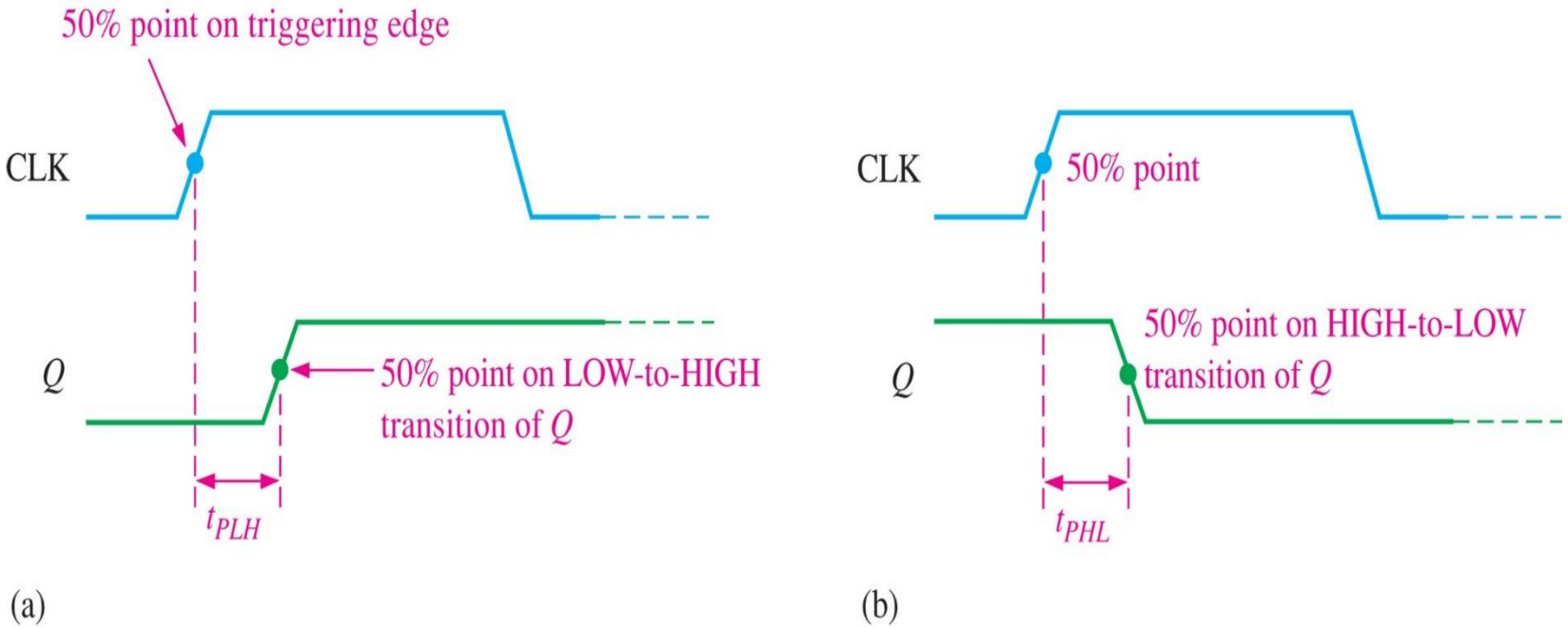


FIGURE 7-31 Propagation delays, clock to output.

The typical propagation delay time for the 74AHC family (CMOS) is 4 ns. Even faster logic is available for specialized applications.

3. Propagation delay t_{PLH} as measured from the leading edge of the preset input to the LOW-to-HIGH transition of the output. This delay is illustrated in Figure 7–32(a) for an active-LOW preset input.

4. Propagation delay t_{PHL} as measured from the leading edge of the clear input to the HIGH-to-LOW transition of the output. This delay is illustrated in Figure 7–32(b) for an active-LOW clear input. The 74AHC family has specified delay times under 5 ns.

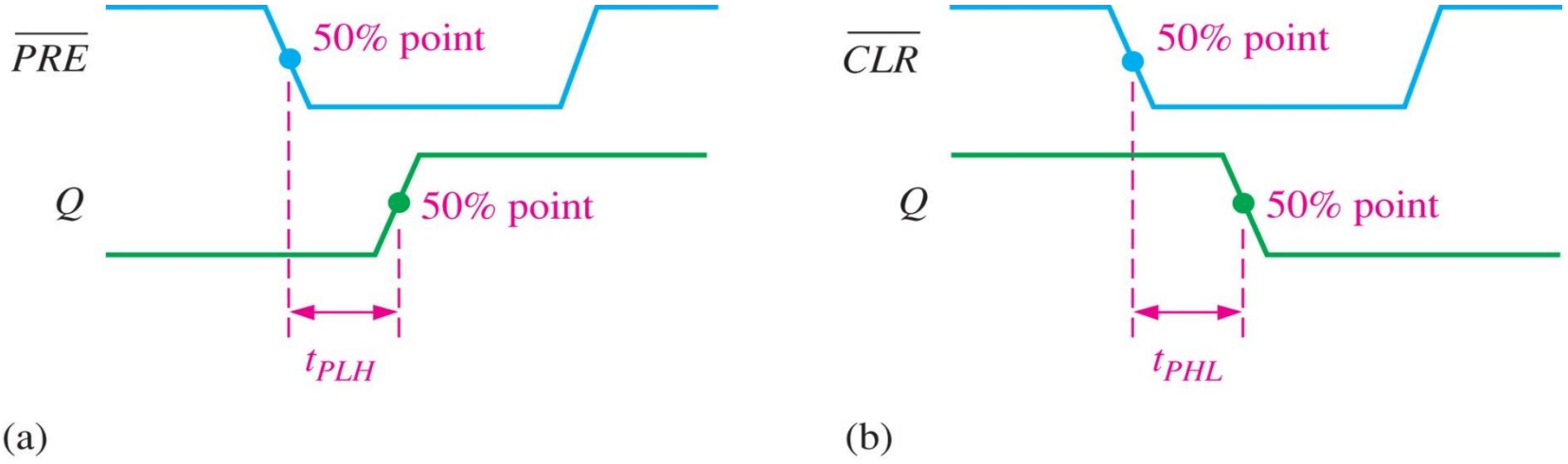


FIGURE 7-32 Propagation delays, preset input to output and clear input to output.

Set-up time

The set-up time (t_s) is the minimum interval required for the logic levels to be maintained constantly on the inputs (*J* and *K*, or *D*) prior to the triggering edge of the clock pulse in order for the levels to be reliably clocked into the flip-flop. This interval is illustrated in Figure 7–33 for a D flip-flop.

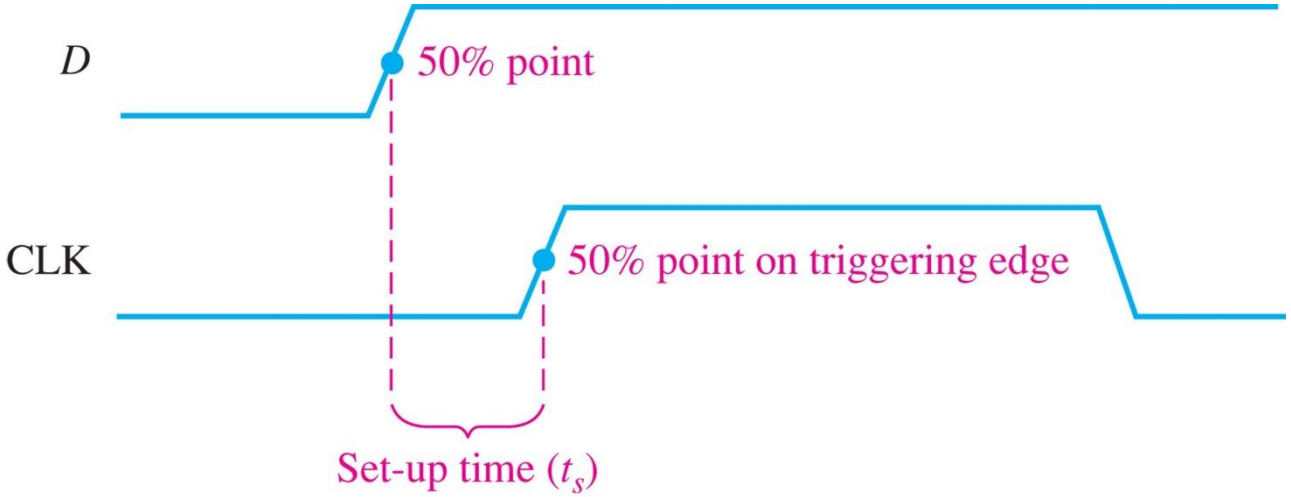


FIGURE 7-33 Set-up time (t_s).

Hold Time

The **hold time** (t_h) is the minimum interval required for the logic levels to remain on the inputs after the triggering edge of the clock pulse in order for the levels to be reliably clocked into the flip-flop. This is illustrated in Figure 7–34 for a D flip-flop.

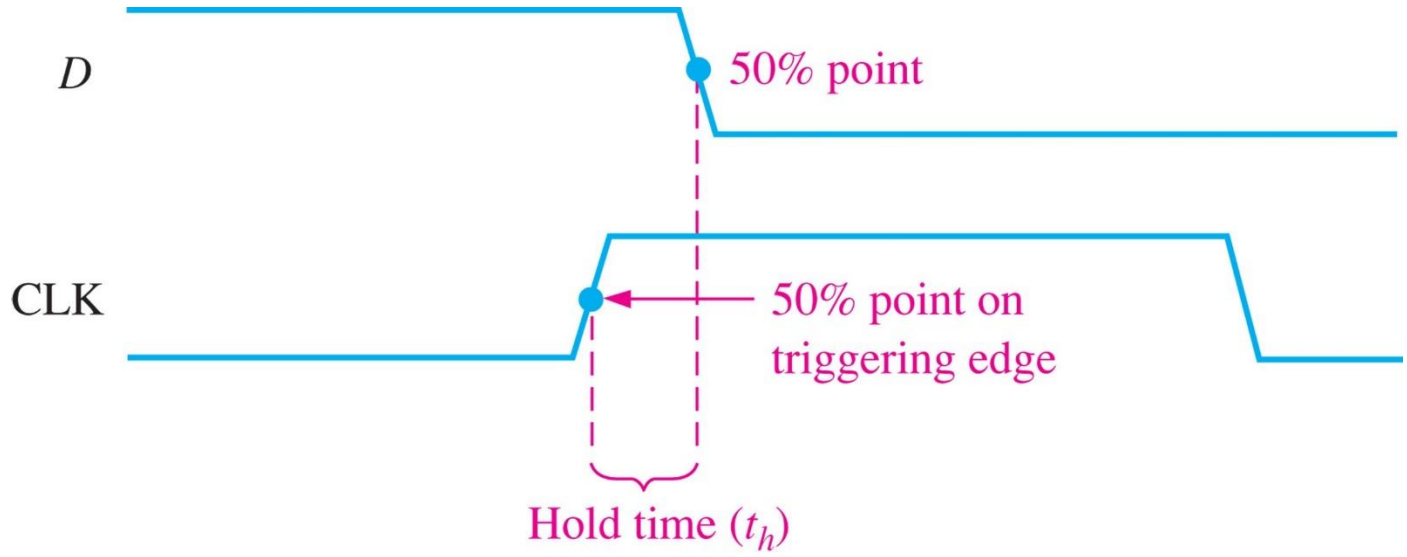


FIGURE 7-34 Hold time (t_h).

Max Clock Frequency & Pulse Widths

Maximum Clock Frequency

The maximum clock frequency (f_{max}) is the highest rate at which a flip-flop can be reliably triggered. At clock frequencies above the maximum, the flip-flop would be unable to respond quickly enough, and its operation would be impaired.

Pulse Widths

Minimum pulse widths (t_W) for reliable operation are usually specified by the manufacturer for the clock, preset, and clear inputs. Typically, the clock is specified by its minimum HIGH time and its minimum LOW time.

Power Dissipation

The **power dissipation** of any digital circuit is the total power consumption of the device. For example, if the flip-flop operates on a +5 V dc source and draws 5 mA of current, the power dissipation is:

$$P = V_{CC} \text{ x } I_{CC} = 5 \text{ V x } 5 \text{ mA} = 25 \text{ mW}$$

A useful comparison between logic families is the **speed-power product** which uses two of the specifications discussed: the average propagation delay and the average power dissipation. The unit is energy.

Example What is the speed-power product for 74AHC74A? Use the data from Table 7-5 to determine the answer.

Solution From Table 7-5, the average propagation delay is 4.6 ns. The quiescent power dissipated is 1.1 mW. Therefore, the speed-power product is **5 pJ** [Where pJ is Pico Joules]

Flip-Flop Applications

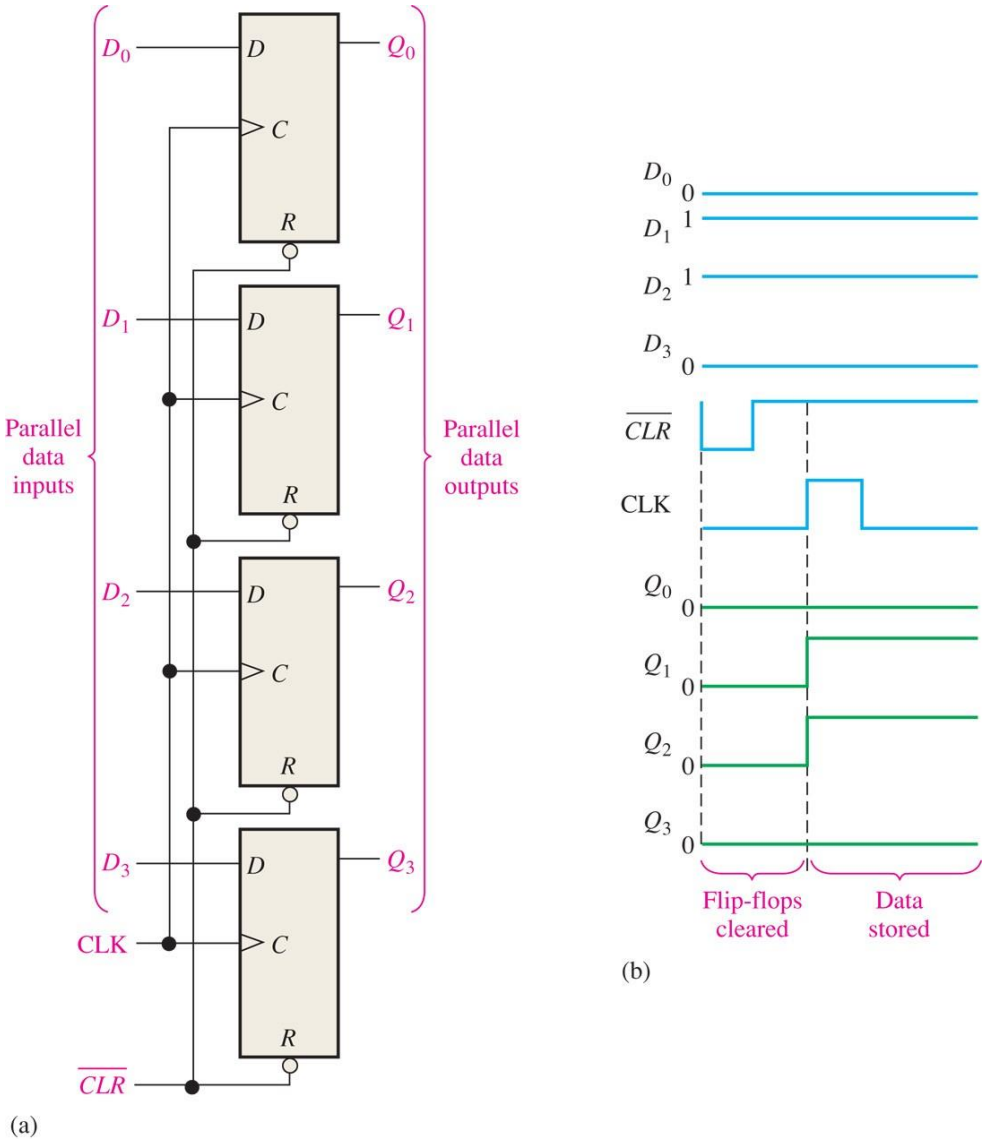
Parallel Data Storage

A common requirement in digital systems is to store several bits of data from parallel lines simultaneously in a group of flip-flops. This operation is illustrated in Figure 7–35(a) using four flip-flops.

Each of the four parallel data lines is connected to the *D* input of a flip-flop. The clock inputs of the flip-flops are connected together, so that each flip-flop is triggered by the same clock pulse.

In this example, positive edge-triggered flip-flops are used, so the data on the *D* inputs are stored simultaneously by the flip-flops on the positive edge of the clock, as indicated in the timing diagram in Figure 7–35(b). Also, the asynchronous reset (*R*) inputs are connected to a common *CLR* line, which initially resets all the flip-flops.

FIGURE 7-35
Example of flip-flops used in a basic register for parallel data storage.



Flip-Flop Applications

Frequency Division

Another application of a flip-flop is dividing (reducing) the frequency of a periodic waveform. When a pulse waveform is applied to the clock input of a D or J-K flip-flop that is connected to toggle ($D = Q$ or $J = K = 1$), the Q output is a square wave with one-half the frequency of the clock input.

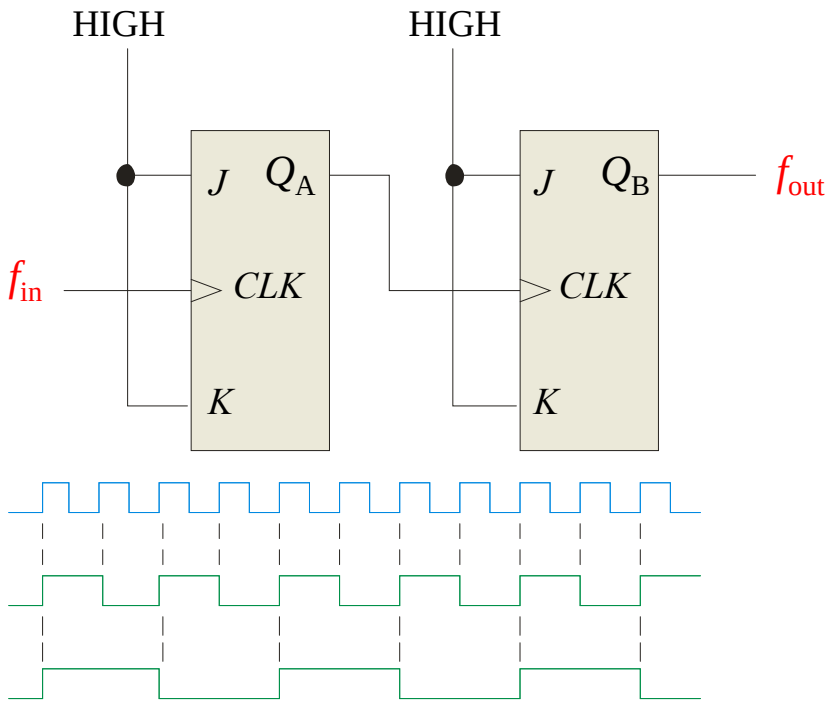
Thus, a single flip-flop can be applied as a divide-by-2 device, as is illustrated in Figure 7–36 for both a D and a J-K flip-flop. As you can see in part (c), the flip-flop changes state on each triggering clock edge (positive edge-triggered in this case). This results in an output that changes at half the frequency of the clock waveform.

Flip-flop Applications

For **frequency division**, it is simple to use a flip-flop in the toggle mode or to chain a series of toggle flip flops to continue to divide by two.

One flip-flop will divide f_{in} by 2, two flip-flops will divide f_{in} by 4 (and so on). A side benefit of frequency division is that the output has an exact 50% duty cycle.

Waveforms:



EXAMPLE 7–9

Develop the f_{out} waveform for the circuit in Figure 7–38 when an 8 kHz square wave input is applied to the clock input of flip-flop A.

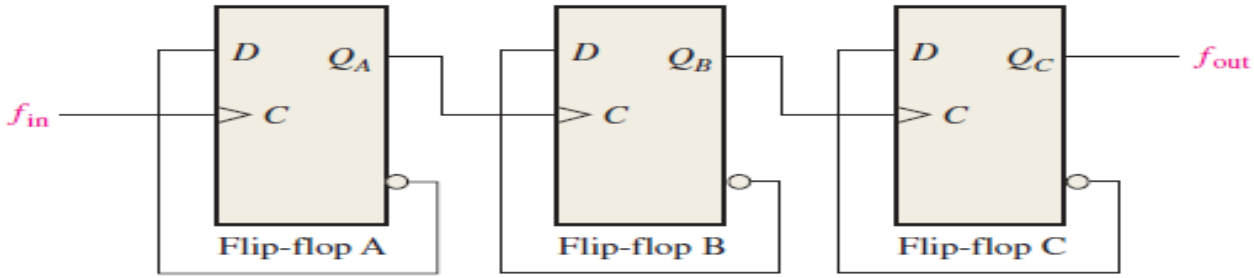


FIGURE 7–38

Solution

The three flip-flops are connected to divide the input frequency by eight ($2^3 = 8$) and the Q_C (f_{out}) waveform is shown in Figure 7–39. Since these are positive edge-triggered flip-flops, the outputs change on the positive-going clock edge. There is one output pulse for every eight input pulses, so the output frequency is 1 kHz. Waveforms of Q_A and Q_B are also shown.

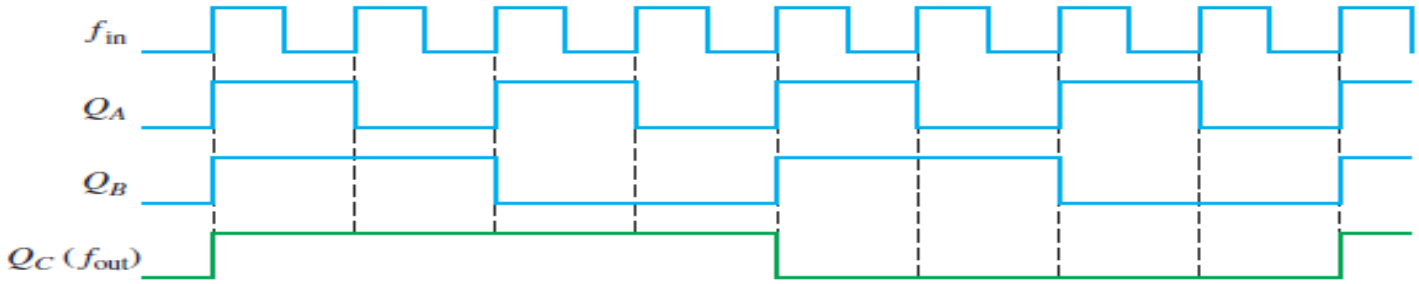
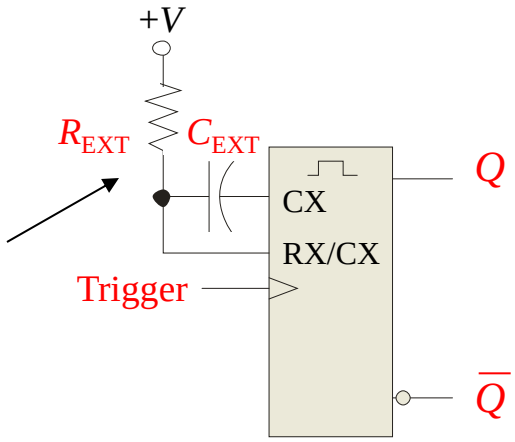


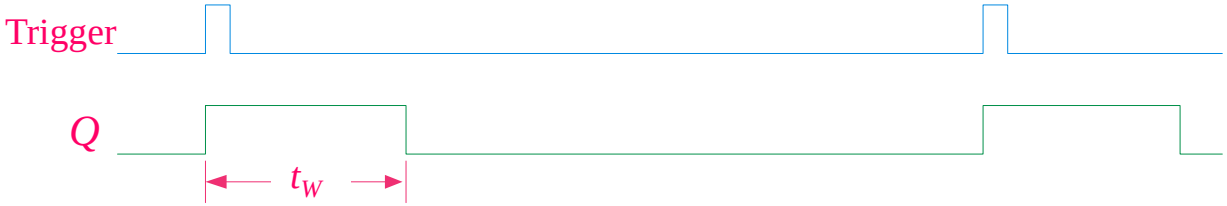
FIGURE 7–39

One-Shots

The **one-shot** or **monostable** multivibrator is a device with only one stable state. When triggered, it goes to its unstable state for a predetermined length of time, then returns to its stable state.

For most one-shots, the length of time in the unstable state (t_W) is determined by an external *RC* circuit.



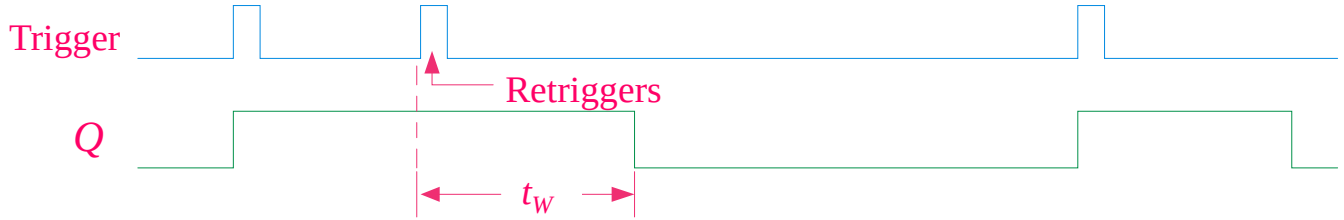


One-Shots

Nonretriggerable one-shots do not respond to any triggers that occur during the unstable state.

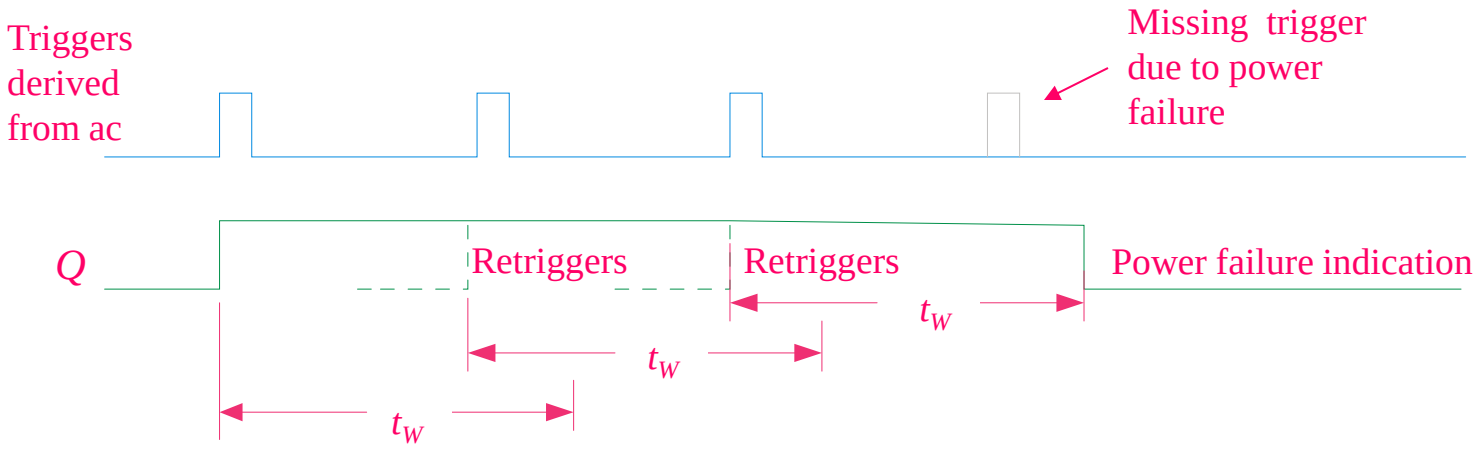
Retriggerable one-shots respond to any trigger, even if it occurs in the unstable state. If it occurs during the unstable state, the state is extended by an amount equal to the pulse width.

Retriggerable one-shot:



One-Shots

An application for a retriggerable one-shot is a power failure detection circuit. Triggers are derived from the ac power source, and continue to retrigger the one shot. In the event of a power failure, the one-shot is not triggered and an alarm can be initiated.



InfoNote

Most systems require a timing source to provide accurate clock waveforms. The timing section controls all system timing and is responsible for the proper operation of the system hardware.

The timing section usually consists of a crystal-controlled oscillator and counters for frequency division. Using a high-frequency oscillator divided down to a lower frequency provides for greater accuracy and frequency stability.

The 555 timer

The 555 timer is a versatile and widely used IC device because it can be configured in two different modes as either a monostable multivibrator (one-shot) or as an astable multivibrator (pulse oscillator).

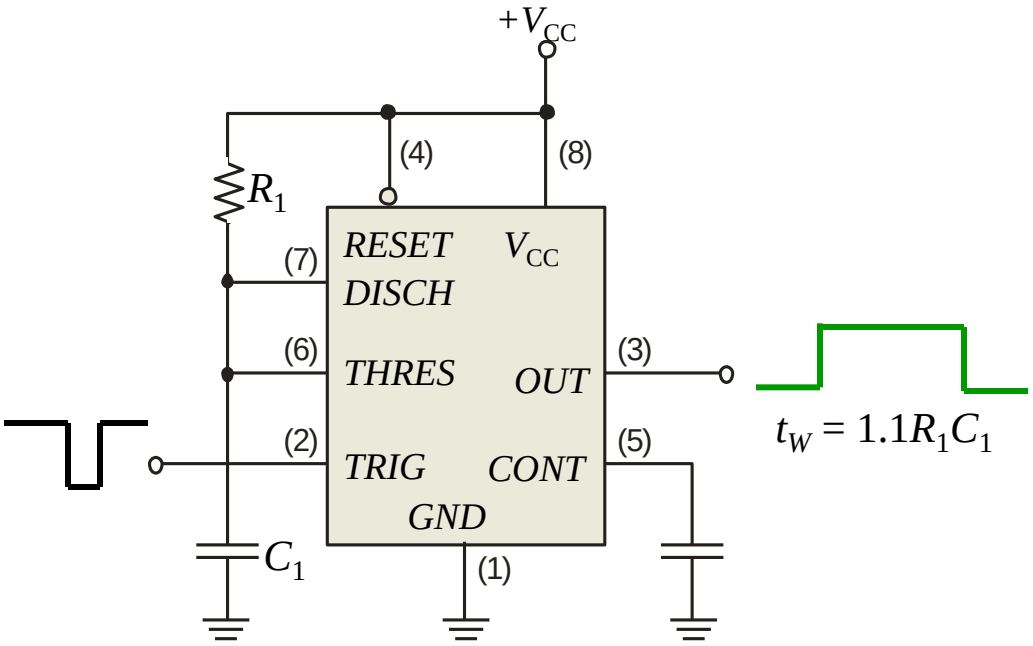
The IC was designed by Hans R. Camenzind in 1970 and brought to market in 1971 by Signetics and It was called “The IC Time Machine”.

The 555 Timer IC is called a 555 because of the 3 - 5K internal resistor divider network which are used to set comparator levels.

The 555 timer

The 555 timer can be configured in various ways, including as a one-shot. A basic one shot is shown. The pulse width is determined by R_1C_1 and is approximately $t_W = 1.1R_1C_1$.

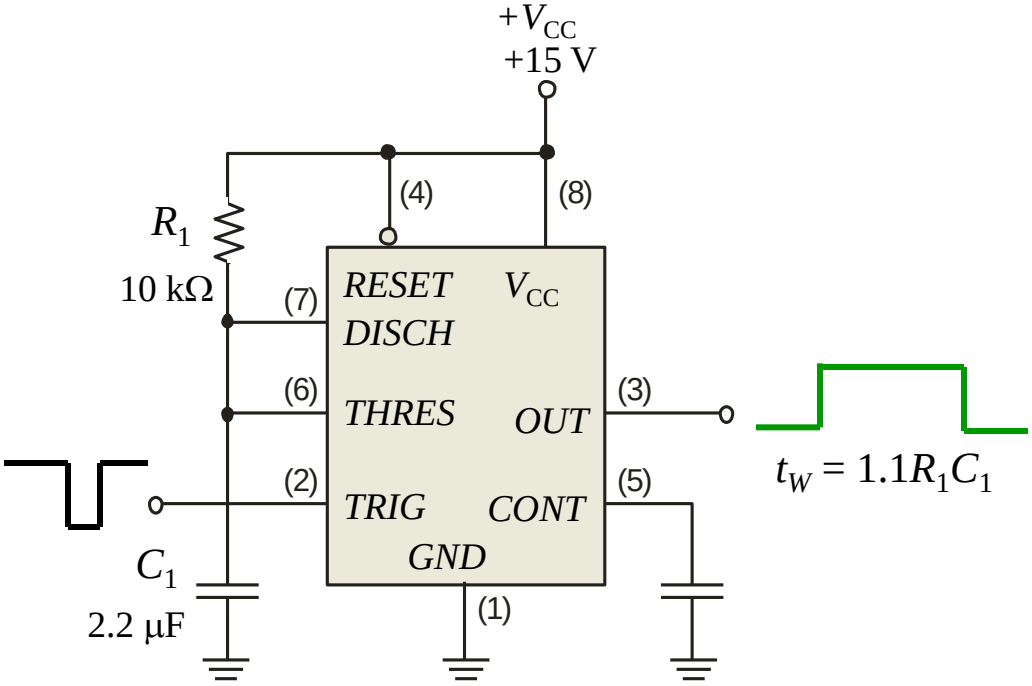
The trigger is a negative-going pulse.



The 555 timer

Example Determine the pulse width for the circuit shown.

Solution $t_W = 1.1R_1C_1 = 1.1(10\ \text{k}\Omega)(2.2\ \mu\text{F}) = 24.2\ \text{ms}$

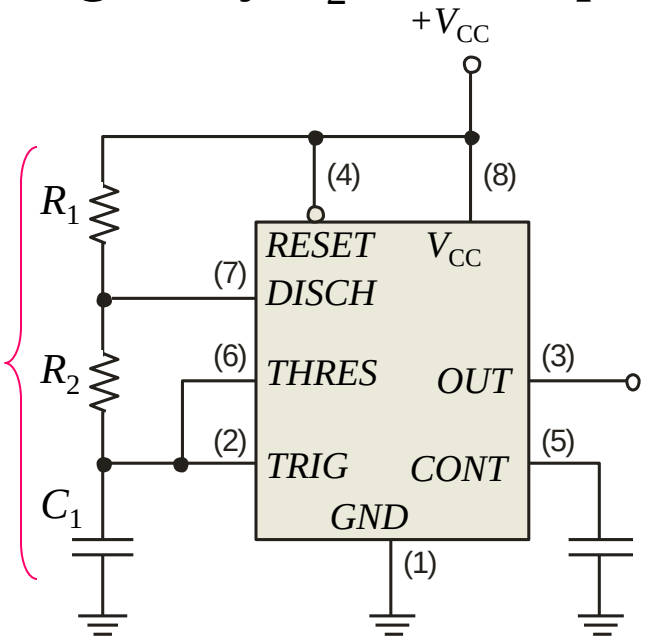


The 555 timer

The 555 can be configured as a basic astable multivibrator with the circuit shown. In this circuit C_1 charges through R_1 and R_2 and discharges through only R_2. The output frequency is given by:

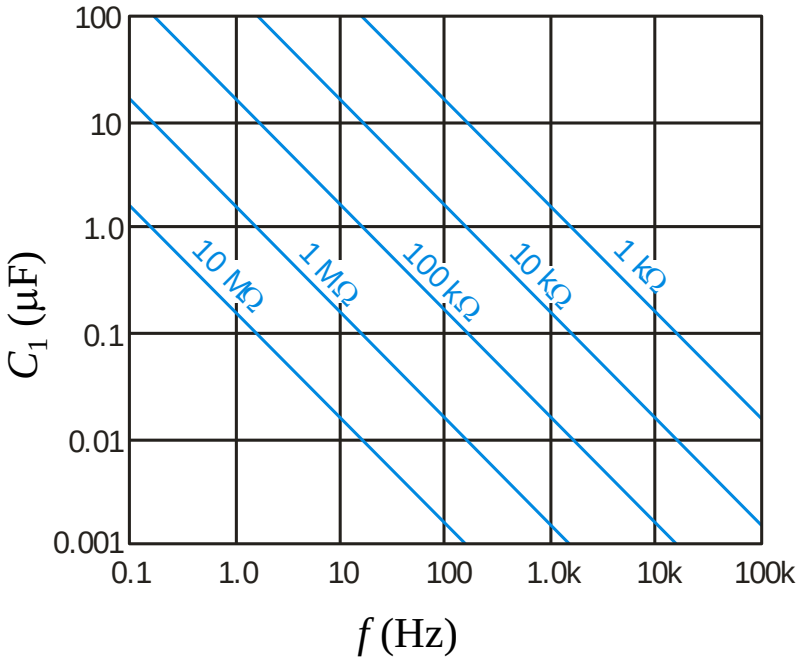
$$f = \frac{1.44}{(R_1 + 2R_2)C_1}$$

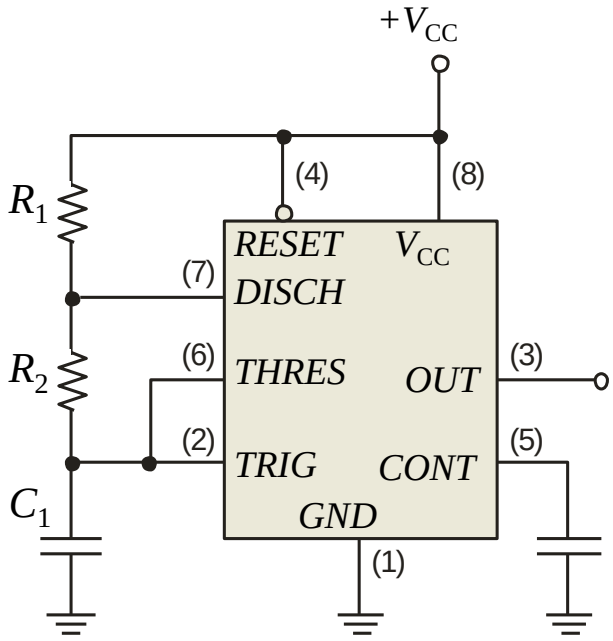
The frequency and duty cycle are set by these components.



The 555 timer

Given the components, you can read the frequency from the chart. Alternatively, you can use the chart to pick components for a desired frequency.





The 555 timer Applications

The 555 timer IC is used in a variety of timer, pulse generation, and oscillator applications.

The 555 can be used to provide time delays, as an oscillator, and as a flip-flop element.

Derivatives provide two or four timing circuits in one package.

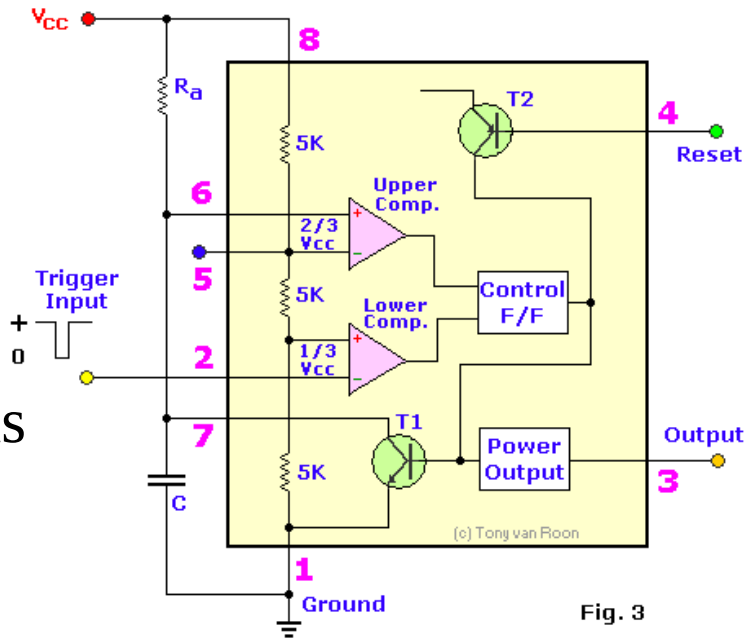


Fig. 3

Selected Key Terms

Latch	A bistable digital circuit used for storing a bit.
Bistable	Having two stable states. Latches and flip-flops are bistable multivibrators.
Clock	A triggering input of a flip-flop.
D flip-flop	A type of bistable multivibrator in which the output assumes the state of the *D* input on the triggering edge of a clock pulse.
J-K flip-flop	A type of flip-flop that can operate in the SET, RESET, no-change, and toggle modes.

Selected Key Terms

Propagation delay time	The interval of time required after an input signal has been applied for the resulting output signal to change.
Set-up time	The time interval required for the input levels to be on a digital circuit.
Hold time	The time interval required for the input levels to remain steady to a flip-flop after the triggering edge in order to reliably activate the device.
Timer	A circuit that can be used as a one-shot or as an oscillator.

Quiz

1. The output of a D latch will not change if

    a. the output is LOW

    b. Enable is not active

    c. D is LOW

    d. all of the above

Quiz

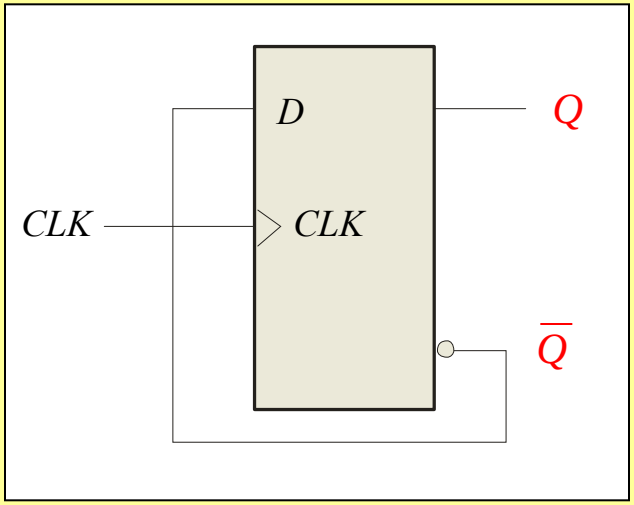
2. The D flip-flop shown will

a. set on the next clock pulse

b. reset on the next clock pulse

c. latch on the next clock pulse

d. toggle on the next clock pulse



Quiz

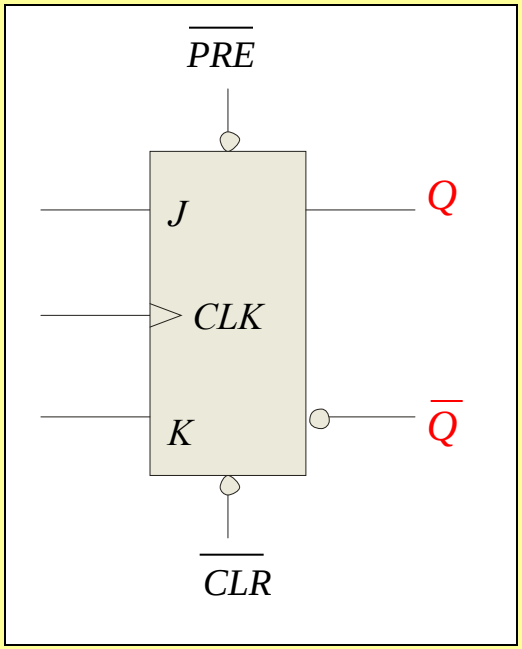
3. For the J-K flip-flop shown, the number of inputs that are asynchronous is

a. 1

b. 2

c. 3

d. 4



Quiz

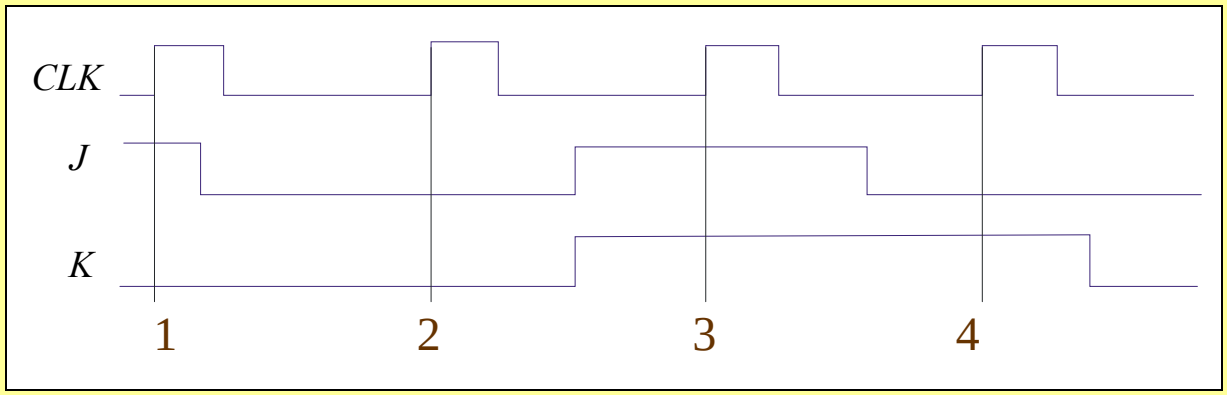
4. Assume the output is initially HIGH on a leading edge triggered J-K flip flop. For the inputs shown, the output will go from HIGH to LOW on which clock pulse?

a. 1

b. 2

c. 3

d. 4



Quiz

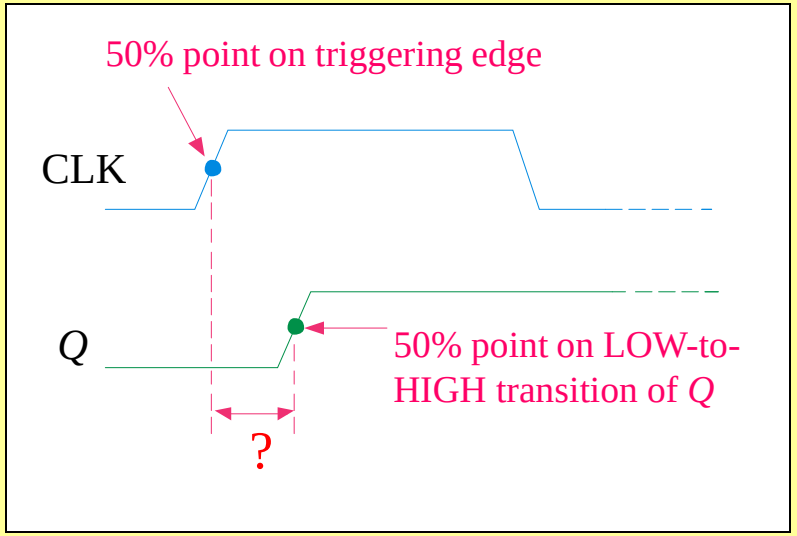
5. The time interval illustrated is called

a. t_{PHL}

b. t_{PLH}

c. set-up time

d. hold time



Quiz

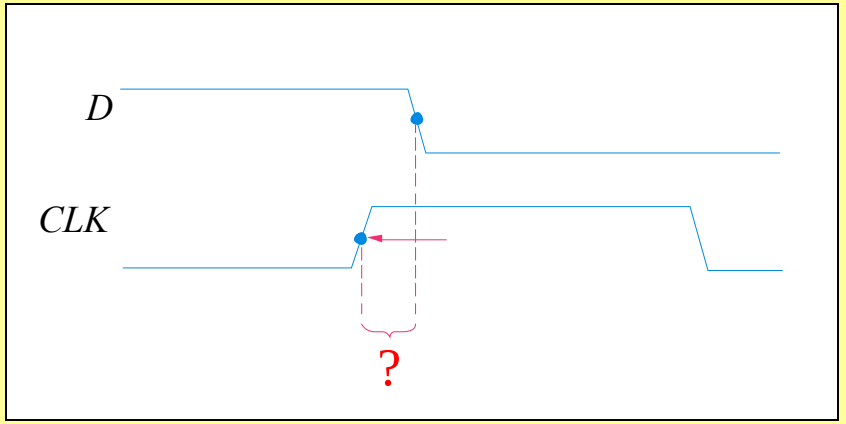
6. The time interval illustrated is called

a. t_{PHL}

b. t_{PLH}

c. set-up time

d. hold time



Quiz

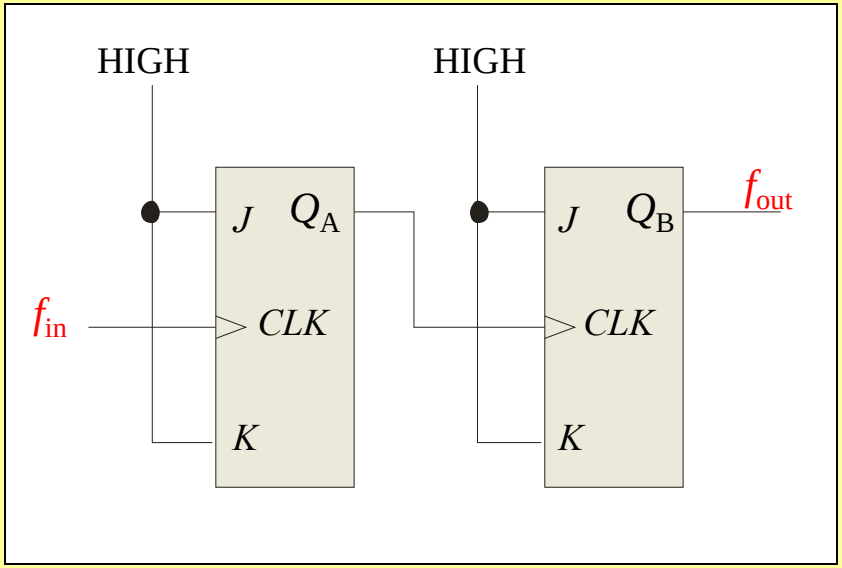
7. The application illustrated is a

a. astable multivibrator

b. data storage device

c. frequency multiplier

d. frequency divider



Quiz

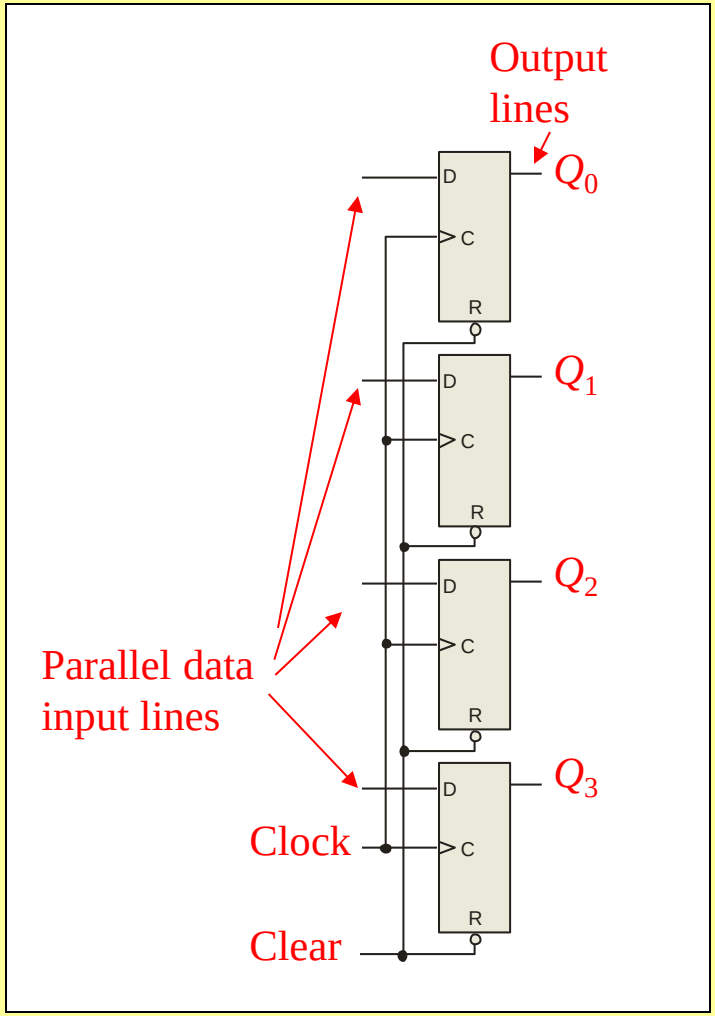
8. The application illustrated is a

a. astable multivibrator

b. data storage device

c. frequency multiplier

d. frequency divider



Quiz

9. A retriggerable one-shot with an active HIGH output has a pulse width of 20 ms and is triggered from a 60 Hz line. The output will be a

a. series of 16.7 ms pulses

b. series of 20 ms pulses

c. constant LOW

d. constant HIGH

Quiz

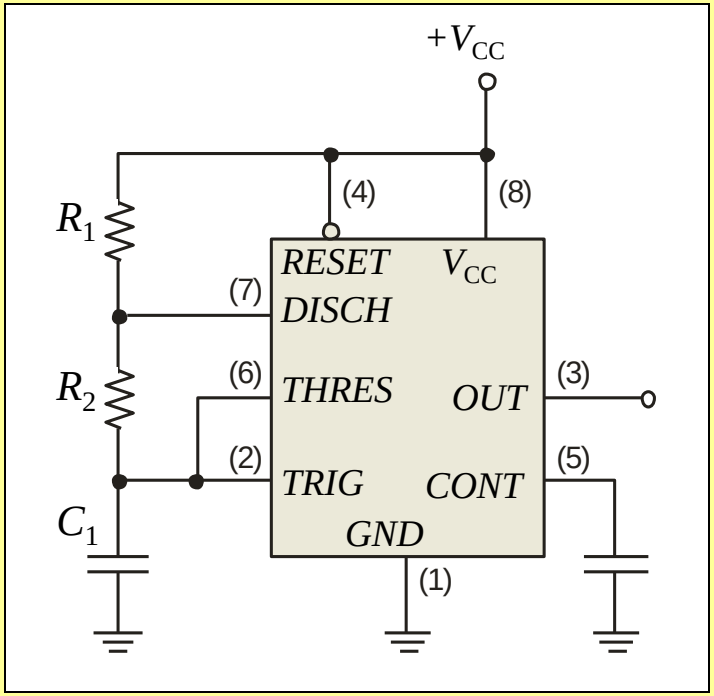
10. The circuit illustrated is a

a. astable multivibrator

b. monostable multivibrator

c. frequency multiplier

d. frequency divider



Quiz

Answers:

1. b
2. d
3. b
4. c
5. b
6. d
7. d
8. b
9. d
10. a