National University of Computer and Emerging Sciences

Karachi Campus

Digital Logic Design

(EE1005)

Date: April 4th , 2024

Course Instructor(s)

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Sessional-II Exam

Total Time (Hrs): 1
Total Marks: 30
Total Questions: 6

Roll No _____ Section _____ Student Signature _____

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Attempt all the questions.

CLO # 3 Analyze small –scale combinational digital circuits.

Q1: A four-bit binary number is represented as $X_3X_2X_1X_0$, where X_3, X_2, X_1 , X_0 represent the individual bits and X_0 is the LSB. Design a logic circuit (using NAND Gate only) that will produce a HIGH output (Y) whenever the binary number is greater than 0010_2 and less than1010_2. **[6]**

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Q2: The circuit in **Fig-1** is supposed to be a simple digital combination lock whose output will generate an active–Low signal for only one combination of inputs. Modify the circuit diagram for active High output. Also determine the input conditions needed to cause the output to go to its active low state **[3]**

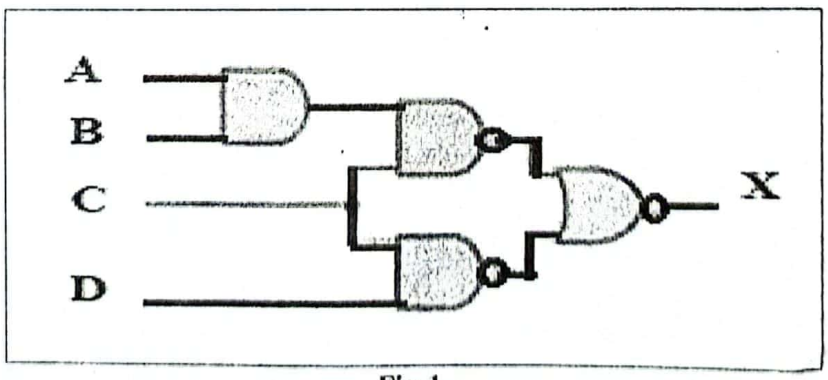

Fig-1

CLO # 3 Analyze small –scale combinational digital circuits.

Q3: The input waveforms in **Fig-2** are applied to a 4-bit adder. Determine the waveforms for the sum and the carry output in relation to the inputs by constructing a timing diagram. **[4]**

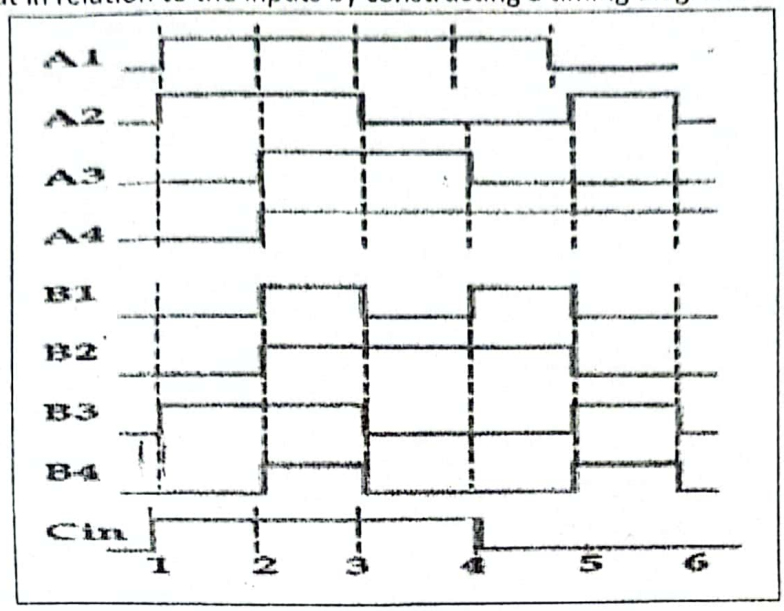

Fig-2

CLO # 3 Analyze small –scale combinational digital circuits.

Q4: Implement the following Boolean function using (a) NAND-NAND representation (b) NOR-NOR representation **[6]**

$$F(A,B,C,D) = \prod (2, 3, 4, 5, 10, 12, 13, 14, 15)$$

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Q5: Implement the above Boolean function of **Q4** using an 8x1 Multiplexer. **[6]**

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Q6: Implement a Full Adder Circuit using a 3 to 8 line Decoder. **[5]**