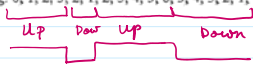
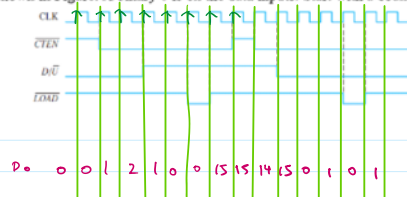


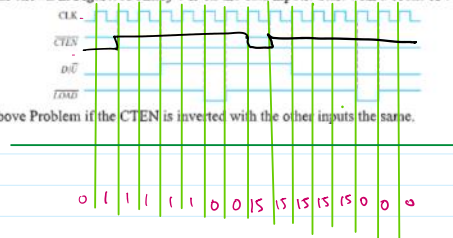
1. Show a complete timing diagram for a 3-bit up/down counter that goes through the following sequence. Indicate when the counter is in the UP mode and when it is in the DOWN mode. Assume positive edge-triggering. 0, 1, 2, 3, 2, 1, 2, 3, 4, 5, 6, 5, 4, 3, 2, 1, 0



2. Develop the Q output waveforms for a 74HC190 up/down counter with the input waveforms shown in Figure. A binary 0 is on the data inputs. Start with a count of 0000.

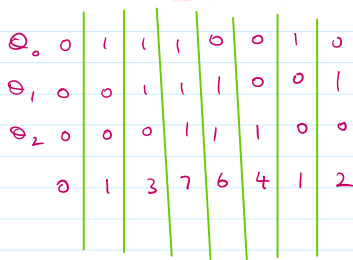
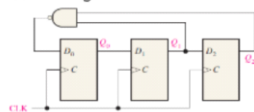


2. Develop the Q output waveforms for a 74HC190 up/down counter with the input waveforms shown in Figure. A binary 0 is on the data inputs. Start with a count of 0000.

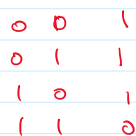
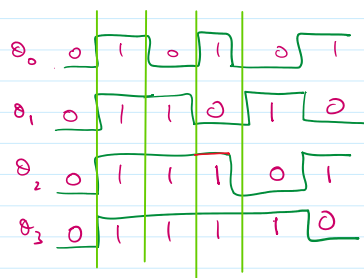
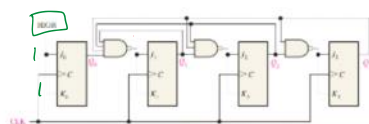


3. Repeat above Problem if the CTEN is inverted with the other inputs the same.

4. Determine the sequence of the counter in Figure.



5. Determine the sequence of the counter in Figure 9-74. Begin with the counter cleared.



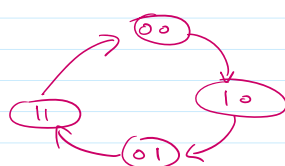
$$J_0 = 1$$

$$J_1 = \overline{Q_0 Q_2 Q_3}$$

$$J_2 = \overline{Q_1 Q_2 Q_3}$$

$$J_3 = \overline{Q_2 Q_3}$$

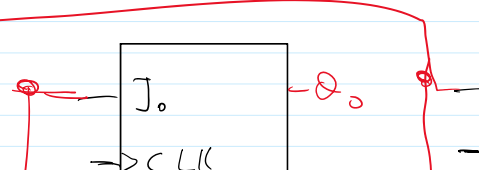
6. Design a counter to produce the following sequence. Use J-K flip-flops. 00, 10, 01, 11, 00, ....



P state

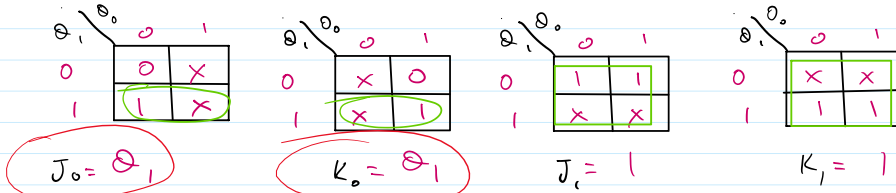
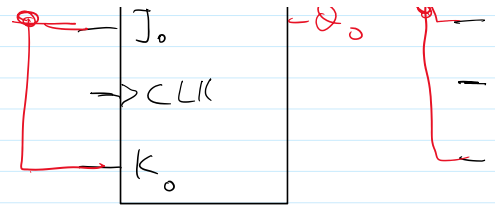
N state

High

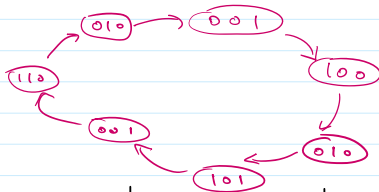




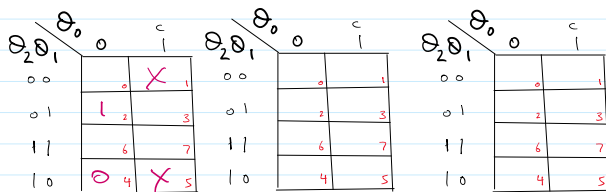
P state		N state		$Q_n$ $Q_{n+1}$	
$Q_1$	$Q_0$	$Q_1$	$Q_0$	$Q_n$	$Q_{n+1}$
0	0	1	0	0	0
1	0	0	1	0	1
0	1	1	1	1	0
1	1	0	0	1	1



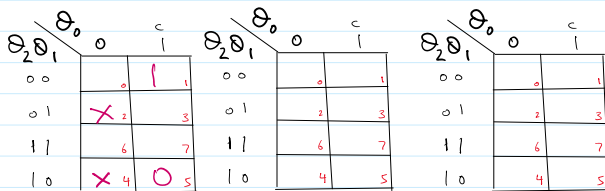
7. Design a counter to produce the following binary sequence. Use J-K flip-flops. 1, 4, 2, 5, 1, 6, 2, 1, ...



Present			Next state			$Q_n$ $Q_{n+1}$		
$Q_2$	$Q_1$	$Q_0$	$Q_2$	$Q_1$	$Q_0$	$Q_n$	$Q_{n+1}$	
0	0	1	1	0	0	0	0	0
1	0	0	0	1	0	0	1	0
0	1	0	1	0	1	0	1	1
1	0	1	0	0	1	1	0	1
0	0	1	1	1	0	1	1	0
1	1	0	0	1	0	1	1	0
0	1	0	0	0	1	1	1	0

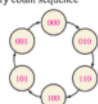


$J_0 =$   $J_1 =$   $J_2 =$



$K_0 =$   $K_1 =$   $K_2 =$

9. Design a counter by using D-flip flop only with the irregular binary count sequence shown in the state diagram of Fig. Include Next-state table, transition table, Karnaugh maps and final circuit.



P			N			$Q_n$ $Q_{n+1}$		
$Q_2$	$Q_1$	$Q_0$	$Q_2$	$Q_1$	$Q_0$	$Q_n$	$Q_{n+1}$	
0	0	0	0	1	0	0	0	0
0	1	0	1	1	0	0	1	0



**Matrix 1 (Initial State):**

	$\theta_0$	0	1
0	0	0	1
1	0	2	X
2	0	6	X

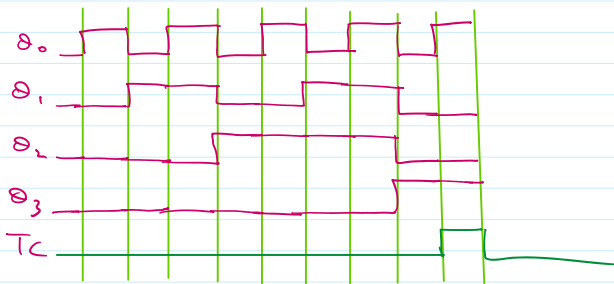
**Matrix 2 (Row 1 scaled by 1/2):**

	$\theta_0$	0	1
0	0	1	0
1	0	1	X
2	0	6	X

**Matrix 3 (Row 2 and Row 3 updated):**

	$\theta_0$	0	1
0	0	1	0
1	0	1	X
2	0	4	0

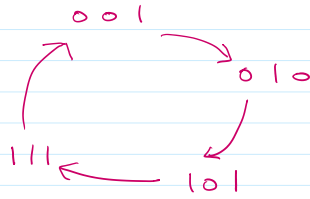
A hand-drawn diagram of a 5-qubit quantum circuit. The qubits are labeled  $Q_0, Q_1, Q_2, Q_3, Q_4$ . The circuit consists of several gates: a CNOT from  $Q_0$  to  $Q_1$ , a CNOT from  $Q_1$  to  $Q_2$ , a CNOT from  $Q_2$  to  $Q_3$ , a CNOT from  $Q_3$  to  $Q_4$ , and a CNOT from  $Q_4$  to  $Q_0$ . There are also several single-qubit rotation gates (represented by circles with 'R' and a subscript) on each qubit.



[10]

001 → 010





Present state	Down 0 Next state	Up 1 Next state
$Q_2 \ Q_1 \ Q_0$	$Q_2 \ Q_1 \ Q_0$	$Q_2 \ Q_1 \ Q_0$
0 0 1	1 1 1	0 1 0
0 1 0	0 0 1	1 0 1
1 0 1	0 1 0	1 1 1
1 1 1	1 0 1	0 0 1

$Q_0 \ Y \ 00 \ 01 \ 11 \ 10$

$Q_2 \ Q_1$	00	01	11	10
00	X	X	0	1
01	1	1	X	X
11	X	X	1	1
10	X	X	1	0

$$D_0 = \overline{Q_0} + Q_2 Q_1 + Q_2 Q_0 Y + \overline{Q_2} Q_0 \overline{Y}$$

$Q_0 \ Y \ 00 \ 01 \ 11 \ 10$

$Q_2 \ Q_1$	00	01	11	10
00	X	X	1	1
01	0	1	X	X
11	X	X	0	0
10	X	X	1	1

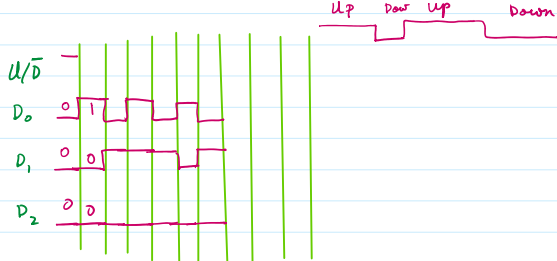
$$D_1 = \overline{Q_1} + Q_2 Q_1 Y$$

$Q_0 \ Y \ 00 \ 01 \ 11 \ 10$

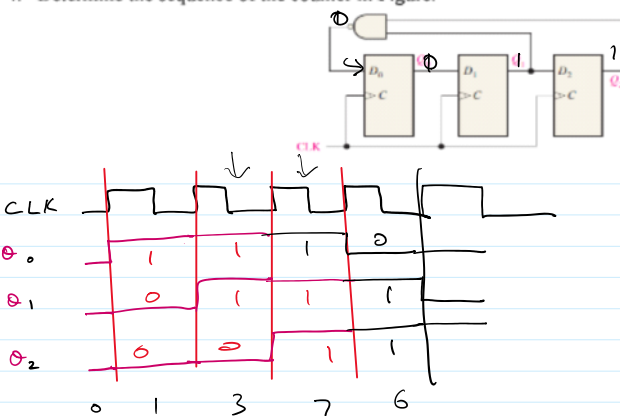
$Q_2 \ Q_1$	00	01	11	10
00	X	X	0	1
01	0	1	X	X
11	X	X	0	1
10	X	X	1	0

$$D_2 = \overline{Q_2} \overline{Q_0} Y + \overline{Q_2} Q_0 \overline{Y} + Q_1 Q_0 \overline{Y} + Q_2 \overline{Q_1}$$

1. Show a complete timing diagram for a 3-bit up/down counter that goes through the following sequence. Indicate when the counter is in the UP mode and when it is in the DOWN mode. Assume positive edge-triggering. 0, 000, 2, 1, 2, 3, 4, 5, 6, 5, 4, 3, 2, 1, 0



4. Determine the sequence of the counter in Figure.



✓



23. Design a binary counter with the sequence shown in the state diagram of Figure 9-75.

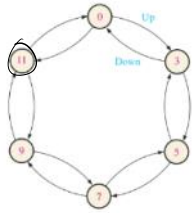
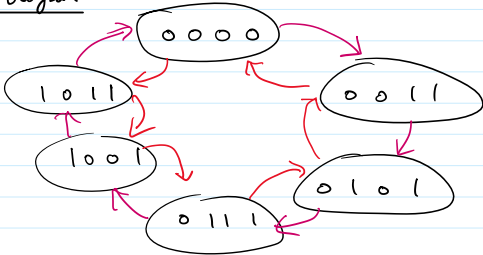


FIGURE 9-75

State Diagram



PRESENT STATE			NEXT STATE				Y
$Q_2$	$Q_1$	$Q_0$	$Y = 0$ (DOWN)			$Q_2$	
0	0	0	1	0	0	0	0
0	0	1	0	0	0	0	0
0	1	1	0	0	1	0	0
0	1	0	0	1	1	1	1
1	1	0	0	1	0	1	1
1	1	1	1	1	0	1	1
1	0	1	1	1	1	1	1
1	0	0	1	0	1	0	0

$Y = \text{UP/DOWN control input.}$

Truth Table

Present state			
$Q_3$	$Q_2$	$Q_1$	$Q_0$
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1

Up = 0 Next state			
$Q_3$	$Q_2$	$Q_1$	$Q_0$
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
0	0	0	0

Down = 1 Next state			
$Q_3$	$Q_2$	$Q_1$	$Q_0$
1	0	1	1
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1

Transition Table

$Q_n$	$Q_{n+1}$	J	K
0	0	0	x
0	1	1	x
1	0	x	1
1	1	x	0

$Q_3 Q_2$	$Q_1 Q_0$	00	01	11	10
00	00	1	x	x	x
00	01	x	x	x	x
01	00	x	x	x	x
01	01	x	x	x	x
10	00	x	x	x	x
10	01	x	x	x	x

$J_0$

$Q_3 Q_2$	$Q_1 Q_0$	00	01	11	10
00	00	1	x	x	x
00	01	x	1	x	x
01	00	x	x	x	x
01	01	x	x	x	x
10	00	x	1	x	x
10	01	x	x	x	x

$J_1$

$Q_3 Q_2$	$Q_1 Q_0$	00	01	11	10
00	00	0	x	1	x
00	01	x	x	x	x
01	00	x	x	x	x
01	01	x	x	x	x
10	00	x	0	0	x
10	01	x	x	x	x

$J_2$

$Q_3 Q_2$	$Q_1 Q_0$	00	01	11	10
00	00	x	x	0	x
00	01	x	x	x	x
01	00	x	x	x	x
01	01	x	x	x	x
10	00	x	x	x	x
10	01	x	x	x	x

$Q_3 Q_2$	$Q_1 Q_0$	00	01	11	10
00	00	x	x	1	x
00	01	x	x	x	x
01	00	x	x	x	x
01	01	x	x	x	x
10	00	x	x	x	x
10	01	x	x	x	x

$Q_3 Q_2$	$Q_1 Q_0$	00	01	11	10
00	00	x	x	x	x
00	01	x	x	x	x
01	00	x	x	x	x
01	01	x	x	x	x
10	00	x	x	x	x
10	01	x	x	x	x

$\Sigma = 1 \text{ (UP)}$

$Q_1$	$Q_0$
0	1
1	1
1	0
1	0
1	1
0	1
0	0
0	0

$\theta_3 \theta_2$	$\theta_1 \theta_0$	00	01	11	10
00		0	X	0	X
01		X	0	X	X
11		X	X	X	X
10		X	X	X	X

$J_3$

$\theta_3 \theta_2$	$\theta_1 \theta_0$	00	01	11	10
00		X	X	X	X

$\theta_3 \theta_2$	$\theta_1$	$\theta_0$	0	1	1	0
0 0			X	X	0	X
0 1			X	0	0	X
1 1			X	X	X	X
1 0			X	0	1	X

$\theta_3 \theta_2$	$\theta_1$	$\theta_0$	0	1	1	0
0 0			X	X	1	X
0 1			X	X	1	X
1 1			X	X	X	X
1 0			X	X	1	X

$\theta_3 \theta_2$	$\theta_1$	$\theta_0$	0	1	1	0
0 0			X	X	X	X
0 1			X	0	1	X
1 1			X	X	X	X
1 0			X	X	X	X

$\theta_3 \backslash \theta_2$	00	01	11	10
00	X	X	X	X
01	X	X	X	X
11	X	X	X	X
10	X	0	1	X