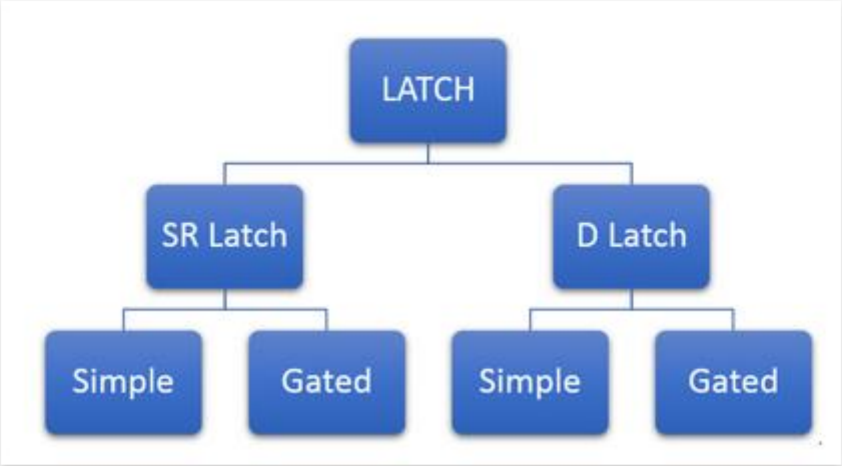
Latches, Flips Flops & Timers

Chapter 7

Sumaiyah Zahid

LATCHES

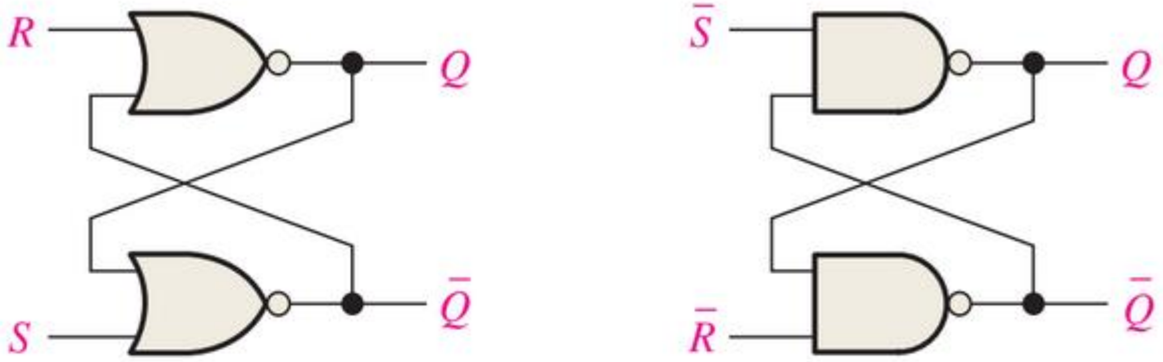
Memory storage device



S-R (SET-RESET) Latch

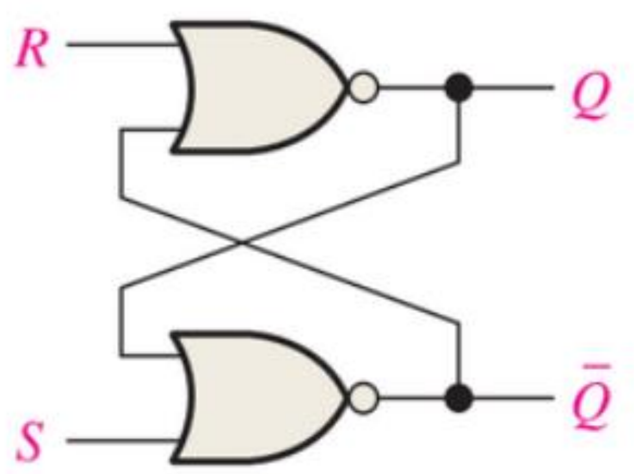
SET means that the Q output is HIGH.

RESET means that the Q output is LOW.



(a) Active-HIGH input S-R latch (b) Active-LOW input $\bar{S}$-$\bar{R}$ latch

S-R (Set-Reset) Latch



(a) Active-HIGH input S-R latch

S-R (SET-RESET) LATCH

Case 1: S=1, R=0, Q=1, Q’=0

S=0, R=0, Q=1, Q’=0 (Memory)

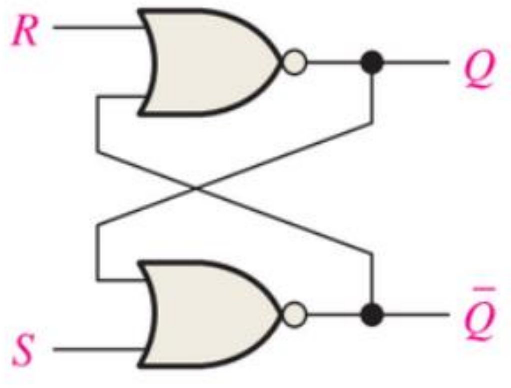
Case 2: S=0, R=1, Q=0, Q’=1

S=0, R=0, Q=0, Q’=1 (Memory)

Case 3: S=1, R=1, Q=0, Q’=0 (Invalid)

S=0, R=0, Q=0, Q’=1

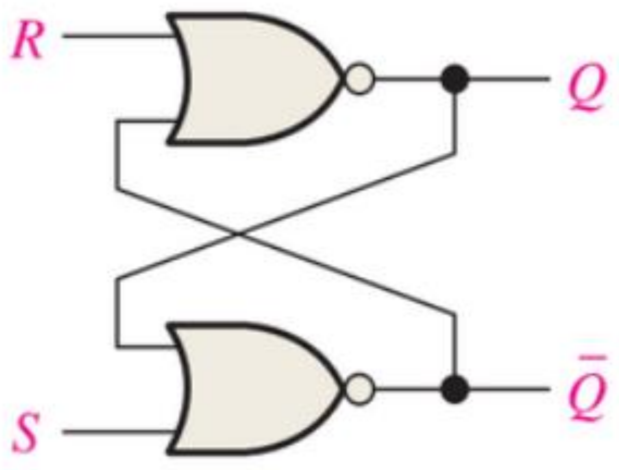
S=0, R=0, Q=1, Q’=0



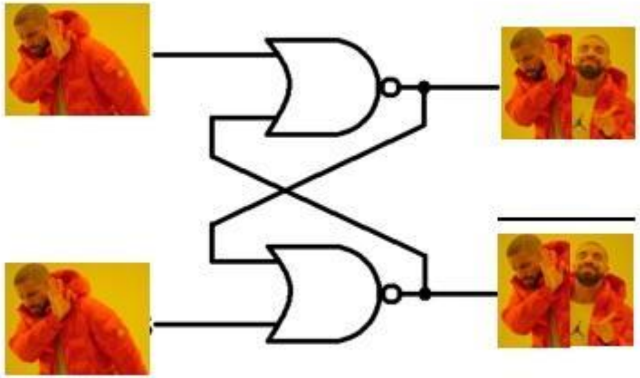
(a) Active-HIGH input S-R latch

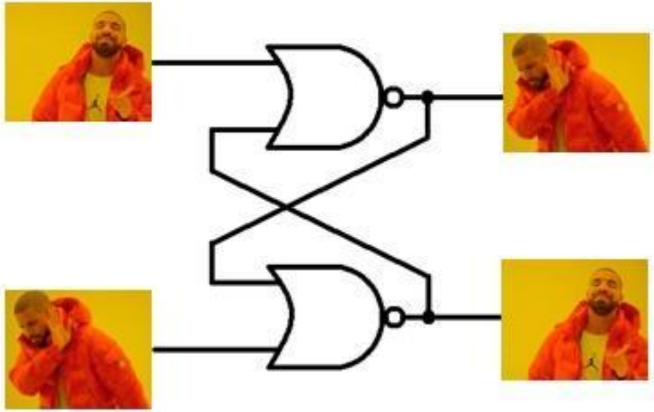
S-R (Set-Reset) Latch

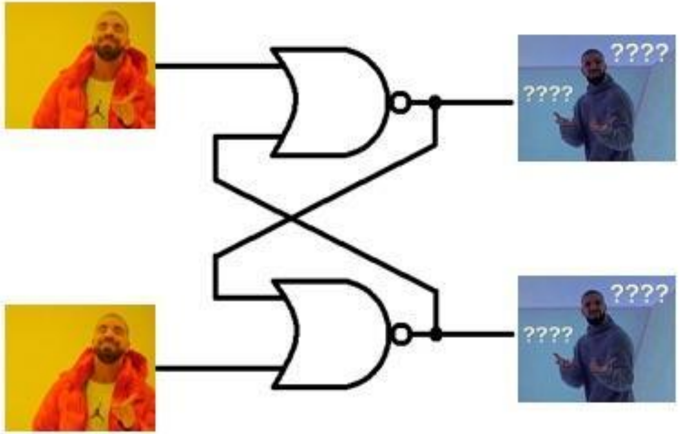
S	R	Q	Q’
0	0	No Change	No Change
0	1	0	1
1	0	1	0
1	1	Invalid	Invalid

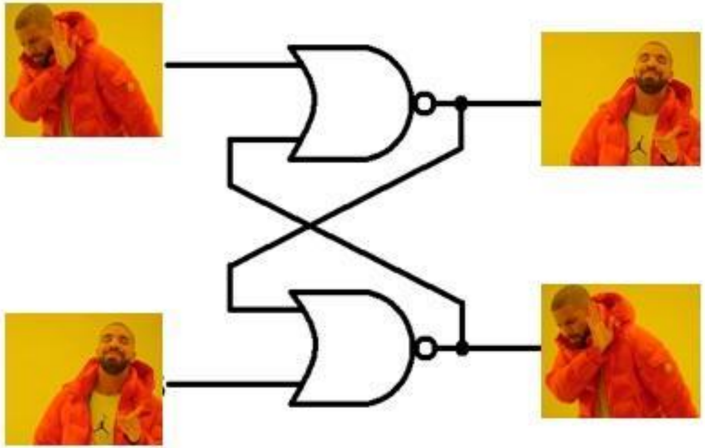


(a) Active-HIGH input S-R latch



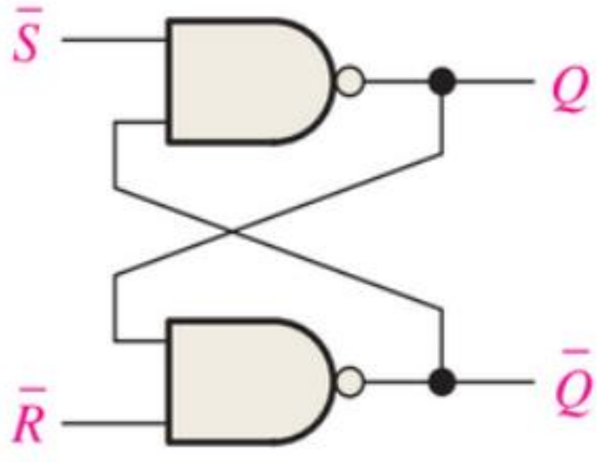






S-R (Set-Reset) Latch

S	R	Q	Q'
0	0	Invalid	Invalid
0	1	1	0
1	0	0	1
1	1	No Change	No Change



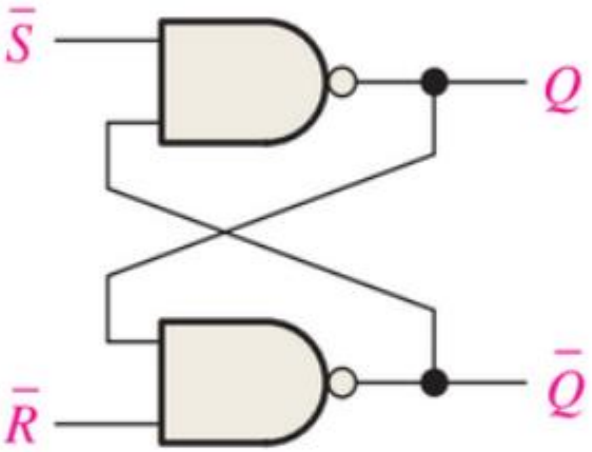
(b) Active-LOW input $\bar{S}$-$\bar{R}$ latch

S-R (SET-RESET) LATCH

Home Task:

Verify all the cases for Active Low SR Latch.

https://www.youtube.com/watch?v=kt8d
CYWGH4

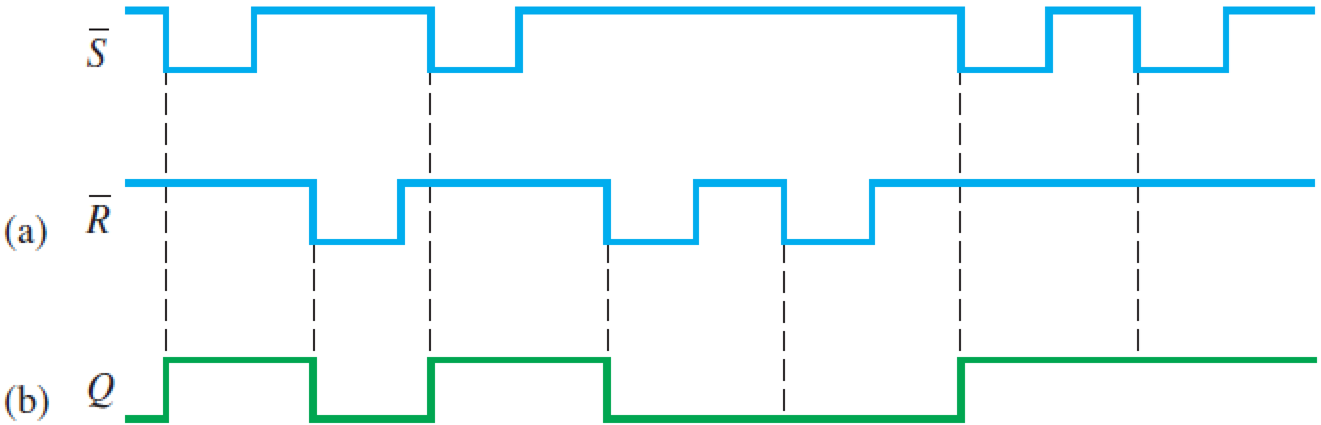


(b) Active-LOW input $\bar{S}$-$\bar{R}$ latch

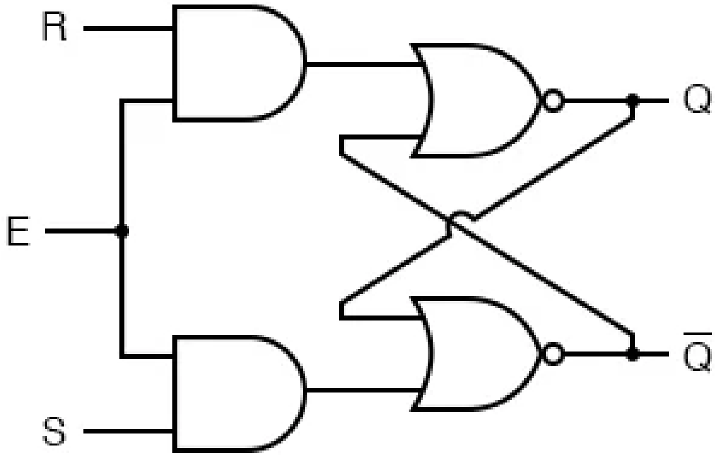
S-R (Set-Reset) Latch

EXAMPLE 7–1

If the $\overline{S}$ and $\overline{R}$ waveforms in Figure 7–5(a) are applied to the inputs of the latch in Figure 7–4(b), determine the waveform that will be observed on the Q output. Assume that Q is initially LOW.



Gated SR Latch (Active High)



E	S	R	Q	$\overline{Q}$
0	0	0	latch	latch
0	0	1	latch	latch
0	1	0	latch	latch
0	1	1	latch	latch
1	0	0	latch	latch
1	0	1	0	1
1	1	0	1	0
1	1	1	0	0

Gated SR Latch (Active High)

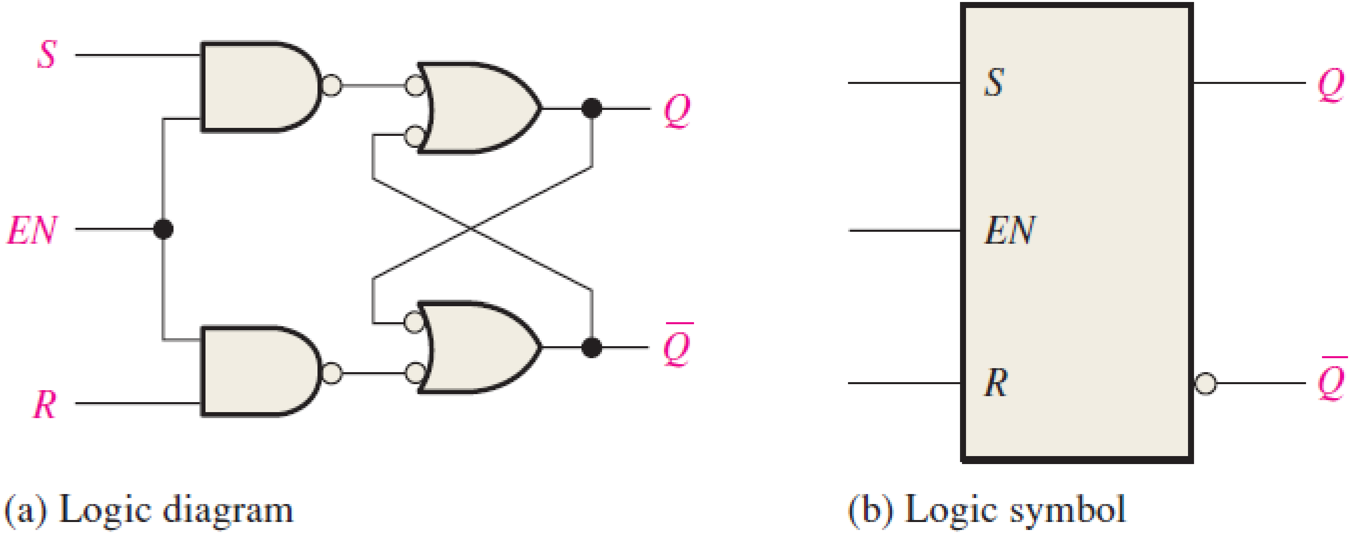


FIGURE 7–8 A gated S-R latch.

Gated SR Latch (Active High)

EXAMPLE 7–2

Determine the Q output waveform if the inputs shown in Figure 7–9(a) are applied to a gated S-R latch that is initially RESET.

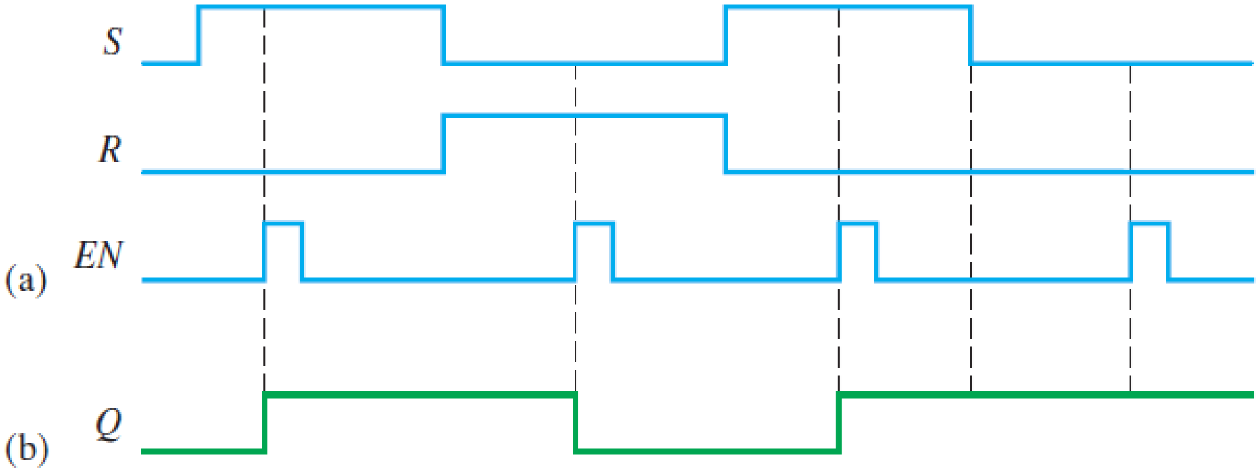
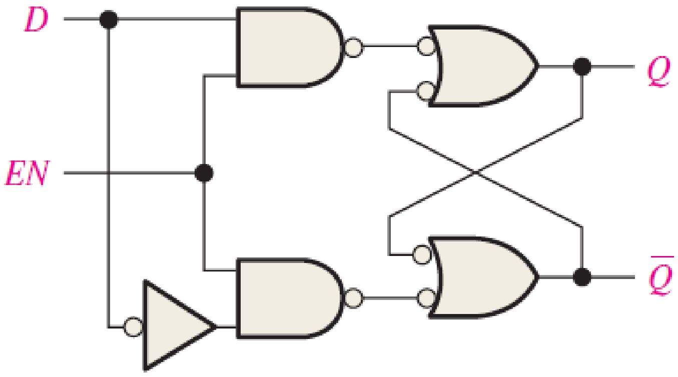
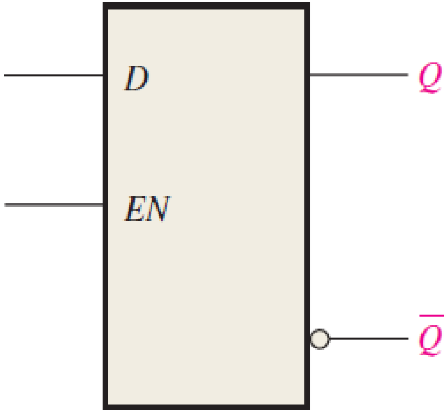


FIGURE 7–9

Gated D Latch



(a) Logic diagram



(b) Logic symbol

D = HIGH & EN = HIGH, the latch will set.

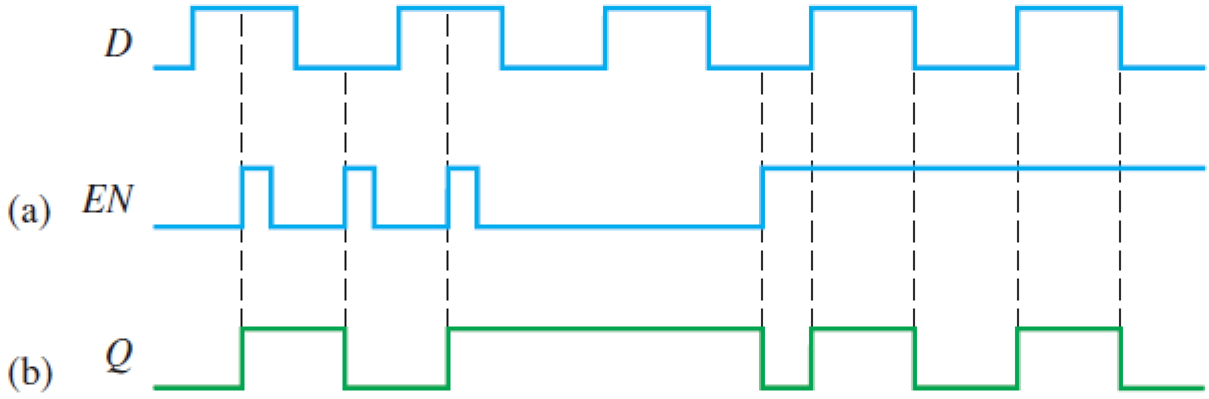
D = LOW & EN = HIGH, the latch will reset.

Stated another way, the output Q follows the input D when EN is HIGH.

Gated D Latch

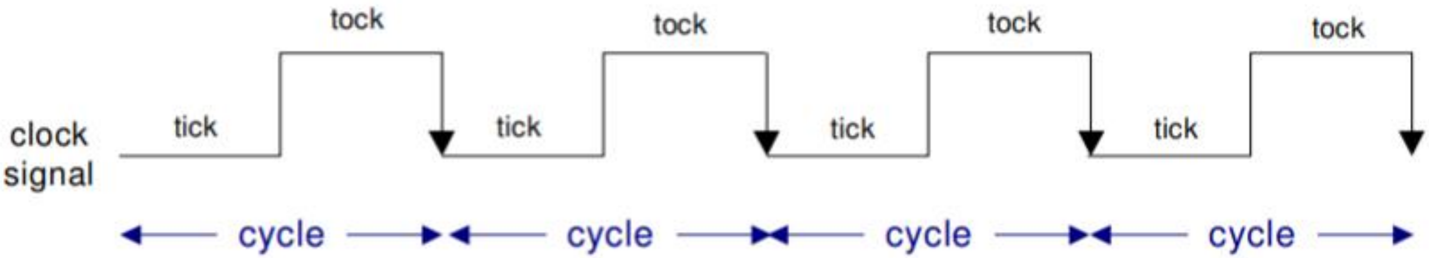
EXAMPLE 7–3

Determine the Q output waveform if the inputs shown in Figure 7–11(a) are applied to a gated D latch, which is initially RESET.



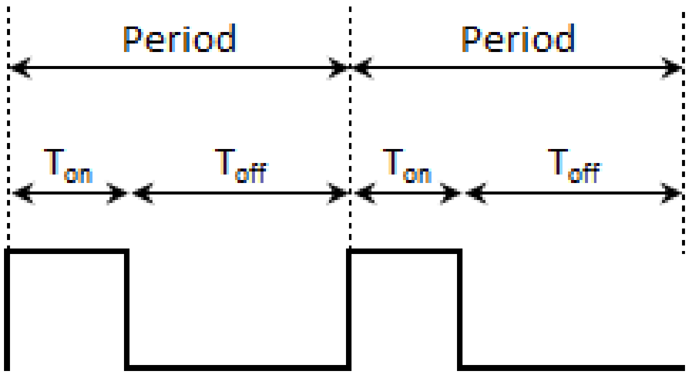
Clock

A periodic signal.



- In our jargon, a clock cycle = *tick*-phase (low), followed by a *tock*-phase (high)

Clock

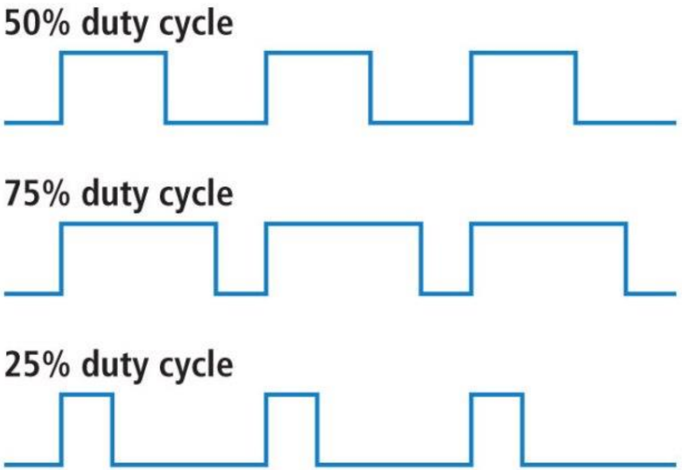


$$\text{Period} = 1 / \text{Frequency}$$

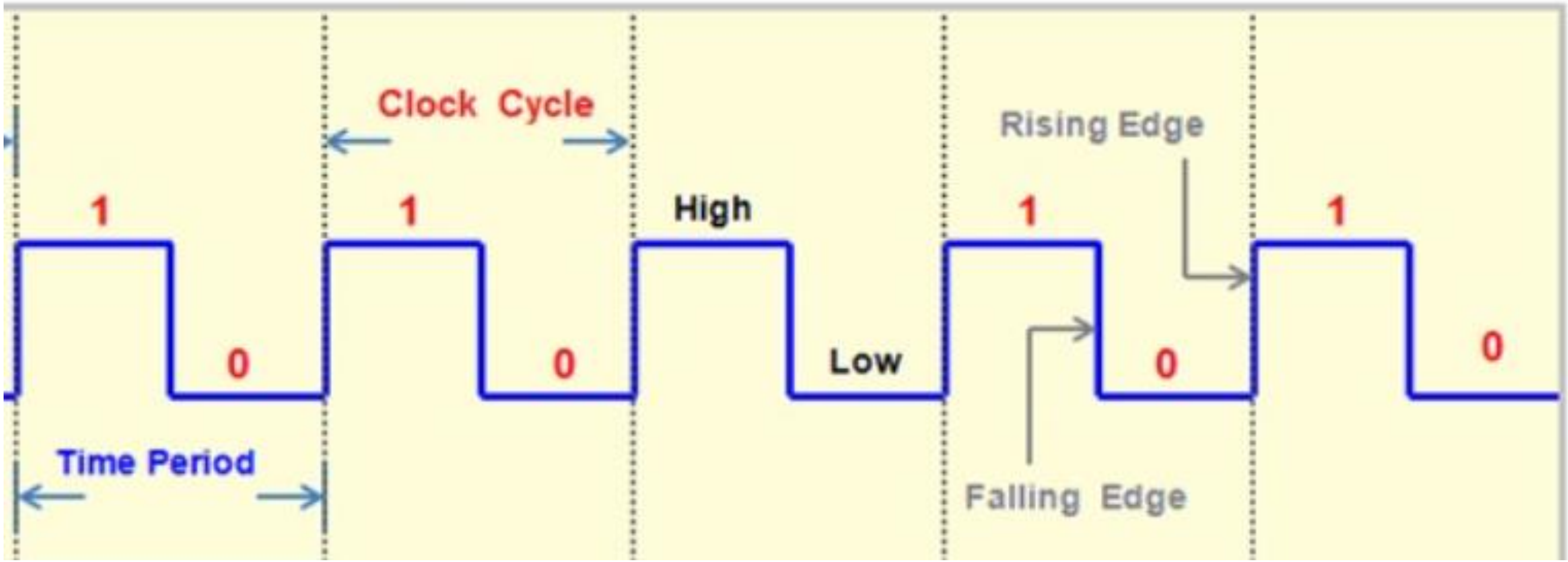
$$\text{Period} = T_{on} + T_{off}$$

$$\text{Duty Cycle} = T_{on} / (T_{on} + T_{off}) * 100$$

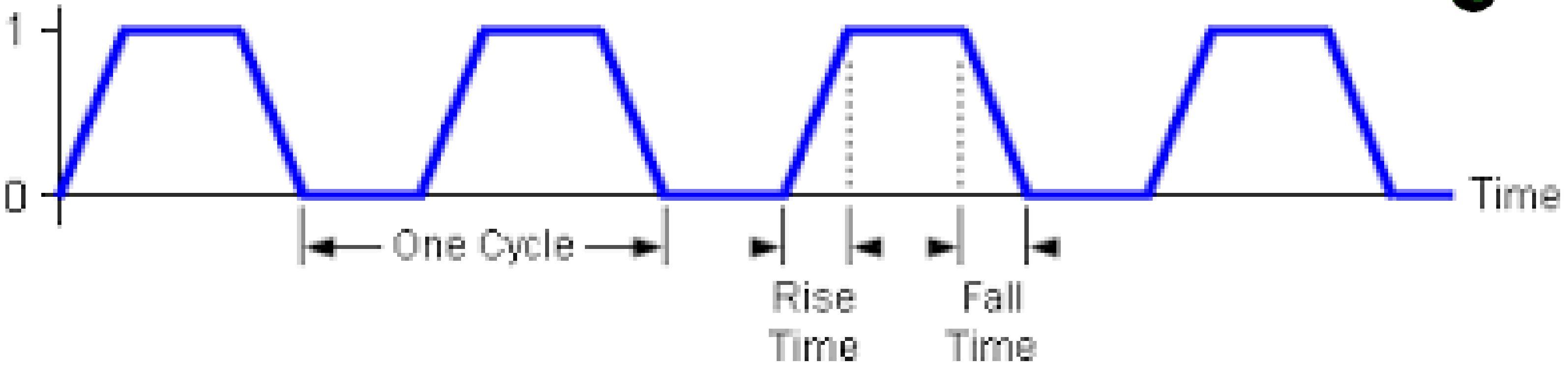
(On Percentage)



Clock


Clock Cycle
Rising Edge
1
1
High
1
1
0
0
Low
0
0
Time Period
Falling Edge

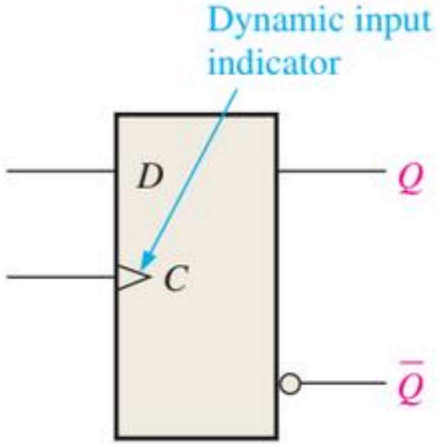
Clock

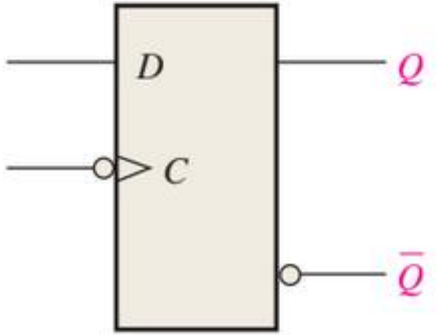


Flips Flops

Flip-flops are edge-triggered or edge-sensitive devices.

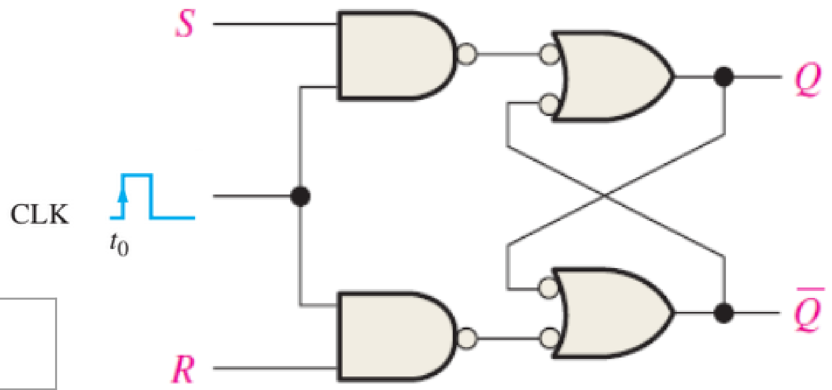
Output changes state only at a specified point (leading or trailing edge) on the triggering input called the clock (CLK).

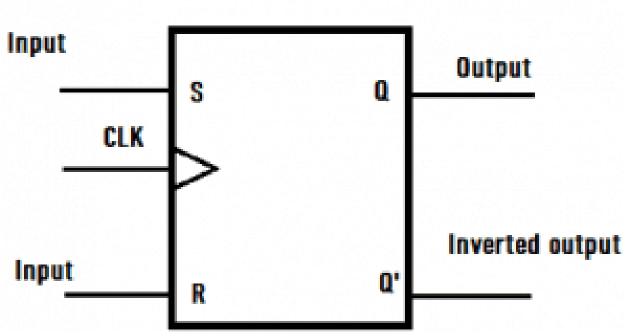




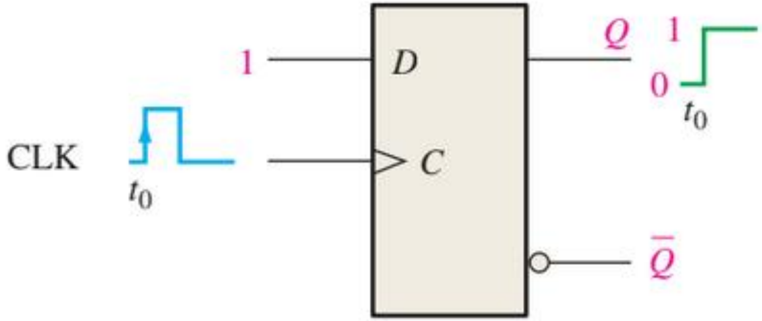
SR Flip Flop

CLK	S	R	Q	Q’
↓	X	X	Q(n-1)	Q’(n-1)
↑	0	0	Q’(n-1)	Q’(n-1)
↑	0	1	0	1
↑	1	0	1	0
↑	1	1	Invalid	Invalid

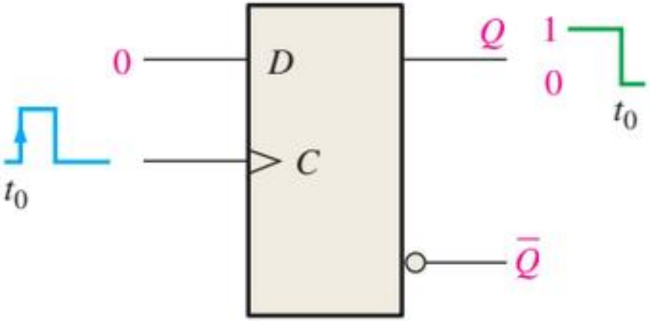




D Flip Flop



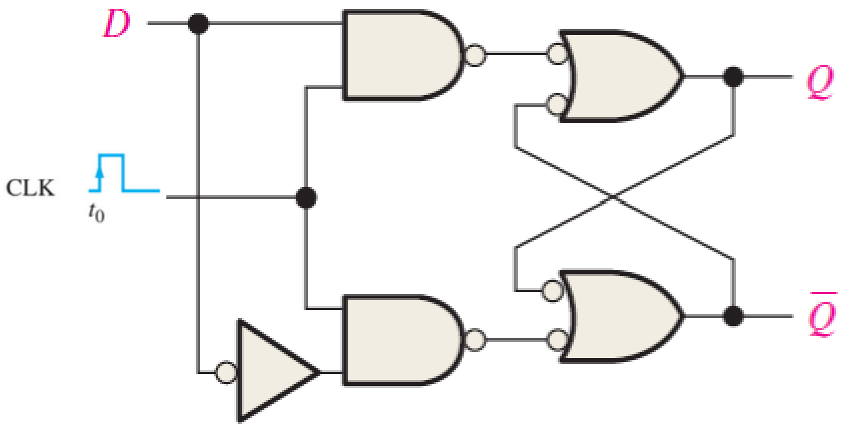
(a) $D = 1$ flip-flop SETS on positive clock edge. (If already SET, it remains SET.)



(b) $D = 0$ flip-flop RESETS on positive clock edge. (If already RESET, it remains RESET.)

D Flip Flop

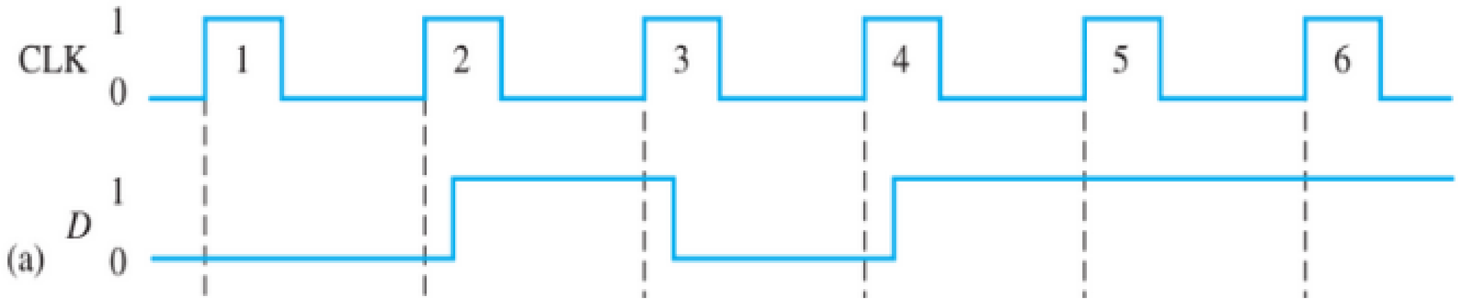
CLK	D	Q	Q'
↓	X	Q(n-1)	Q'(n-1)
↑	1	1	0
↑	0	0	1



D Flip Flop

EXAMPLE 7–4

Determine the Q and $\overline{Q}$ output waveforms of the flip-flop in Figure 7–15 for the D and CLK inputs in Figure 7–16(a). Assume that the positive edge-triggered flip-flop is initially RESET.

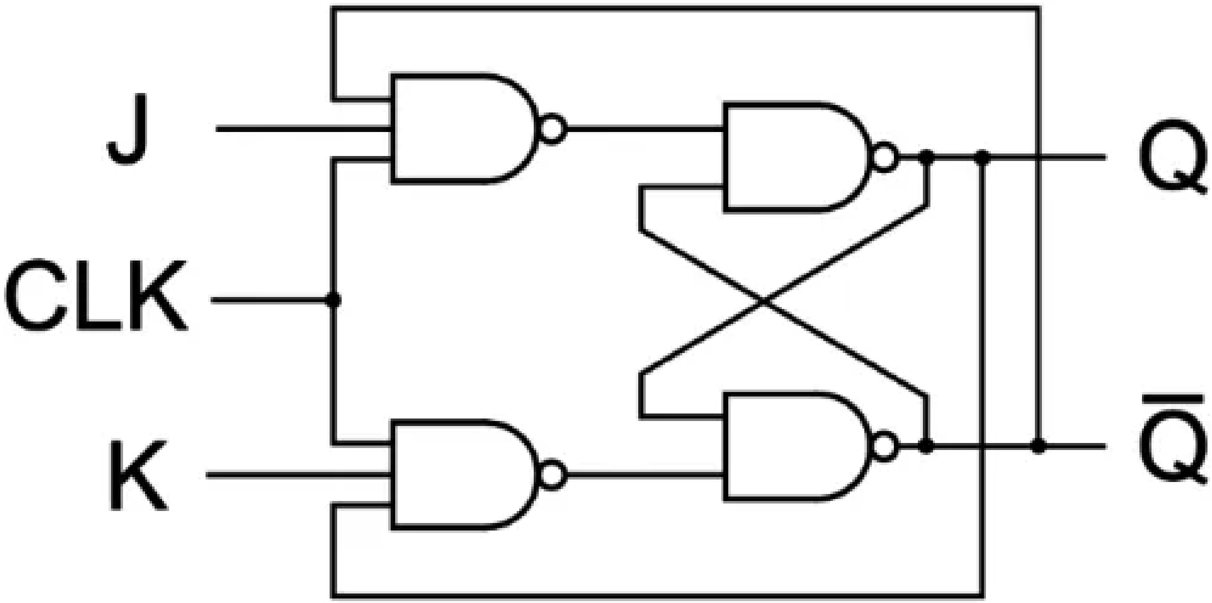


Limitations of D and SR Flip Flop

D has only single input.

SR flip flop has an invalid state.

JK Flip Flop



JK Flip Flop

Case 1: CLK=0 (Memory)

Case 2: CLK=1, J=1, K=0, Q=1, Q’=0

Case 3: CLK=1, J=0, K=1, Q=0, Q’=1

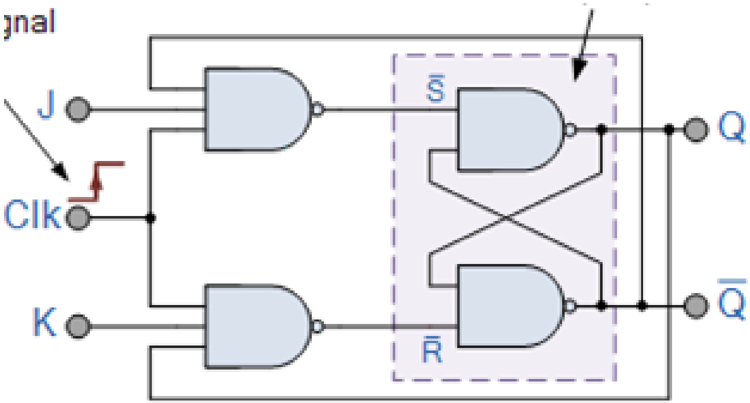
Case 4: CLK=1, J=1, K=1,

Q(n)=0, Q’(n)=1, Q(n+1)=1, Q’(n+1)=0

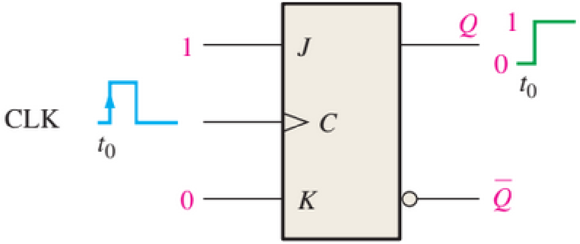
Q(n)=1, Q’(n)=0, Q(n+1)=0, Q’(n+1)=1

JK Flip Flop

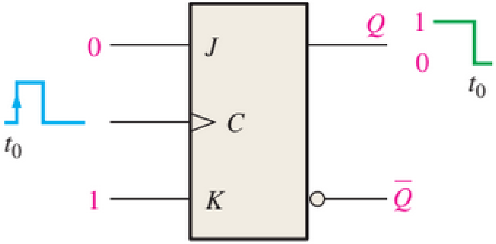
CLK	J	K	Q	Q’
↓	X	X	Q(n-1)	Q’(n-1)
↑	0	0	Q’(n-1)	Q’(n-1)
↑	0	1	0	1
↑	1	0	1	0
↑	1	1	Toggles	Toggles



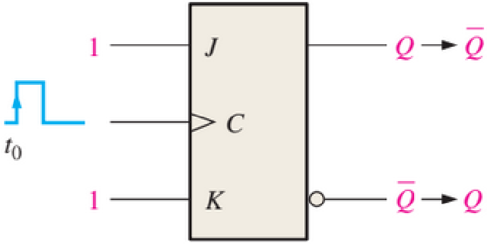
JK Flip Flops



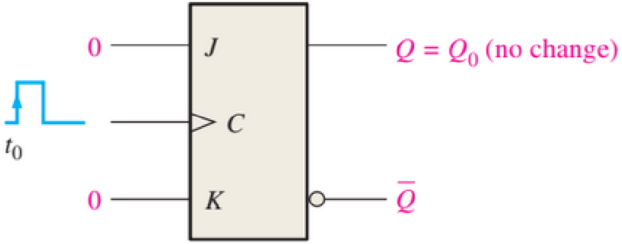
(a) $J = 1$, $K = 0$ flip-flop SETS on positive clock edge. (If already SET, it remains SET.)



(b) $J = 0$, $K = 1$ flip-flop RESETS on positive clock edge. (If already RESET, it remains RESET.)



(c) $J = 1$, $K = 1$ flip-flop changes state (toggle).



(d) $J = 0$, $K = 0$ flip-flop does not change. (If SET, it remains SET; if RESET, it remains RESET.)

JK Flip Flops

TABLE 7–3

Truth table for a positive edge-triggered J-K flip-flop.

Inputs			Outputs		
J	K	CLK	Q	$\overline{Q}$	Comments
0	0	$\uparrow$	Q_0	$\overline{Q}_0$	No change
0	1	$\uparrow$	0	1	RESET
1	0	$\uparrow$	1	0	SET
1	1	$\uparrow$	$\overline{Q}_0$	Q_0	Toggle

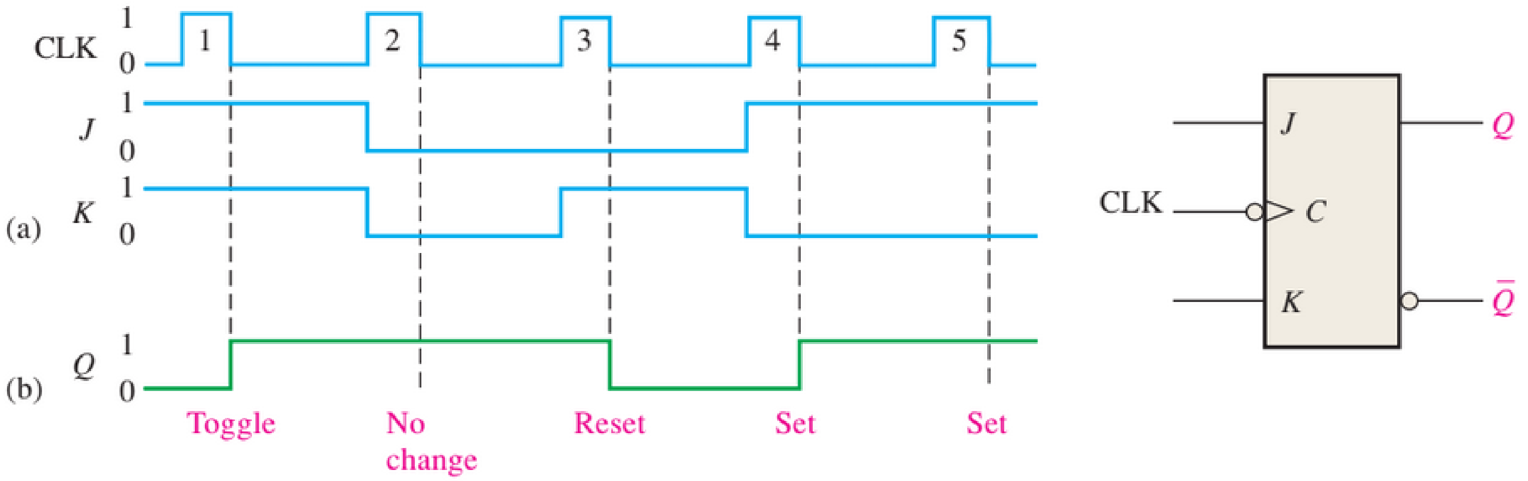
$\uparrow$ = clock transition LOW to HIGH

Q_0 = output level prior to clock transition

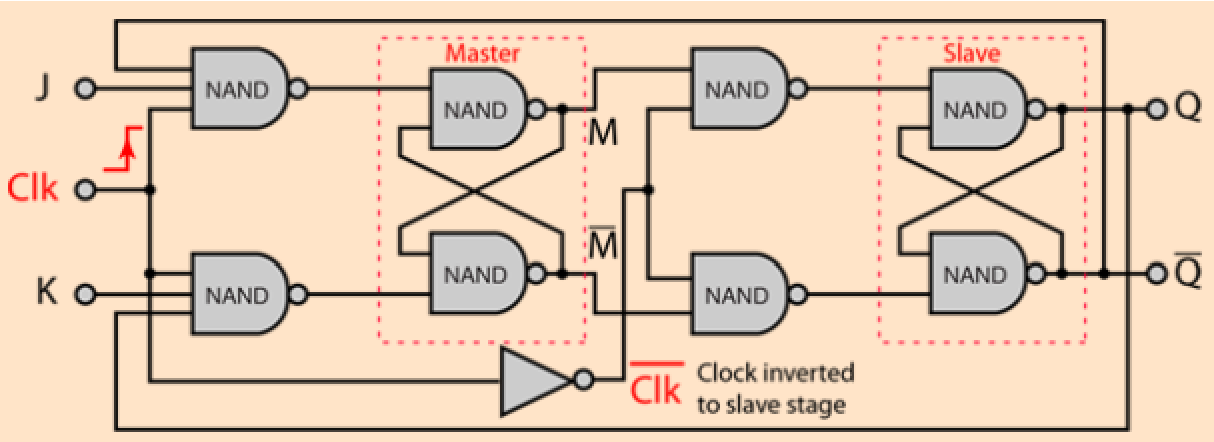
JK Flip Flop

EXAMPLE 7–5

The waveforms in Figure 7–18(a) are applied to the *J*, *K*, and clock inputs as indicated. Determine the *Q* output, assuming that the flip-flop is initially RESET.

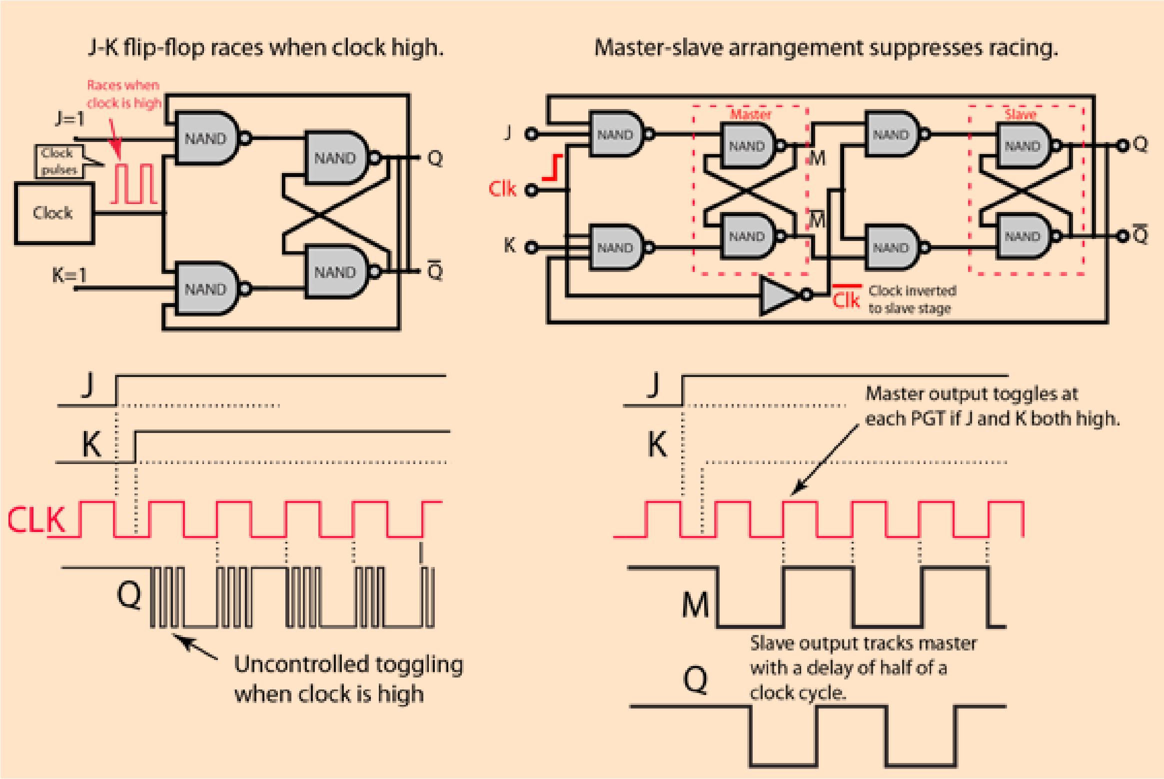


Master Slave JK Flip Flop



Master Slave JK Flip Flop

Master Slave JK Flip Flop



Edge Triggering

D Flip FLop

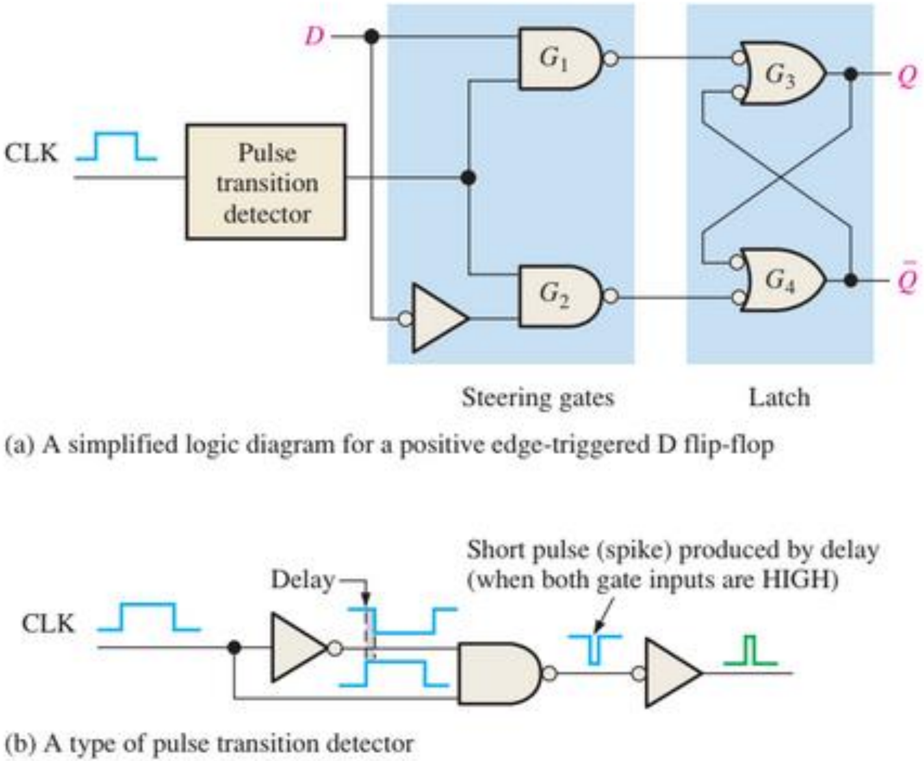


FIGURE 7–19 Edge triggering.

Edge Triggered - D Flip Flop

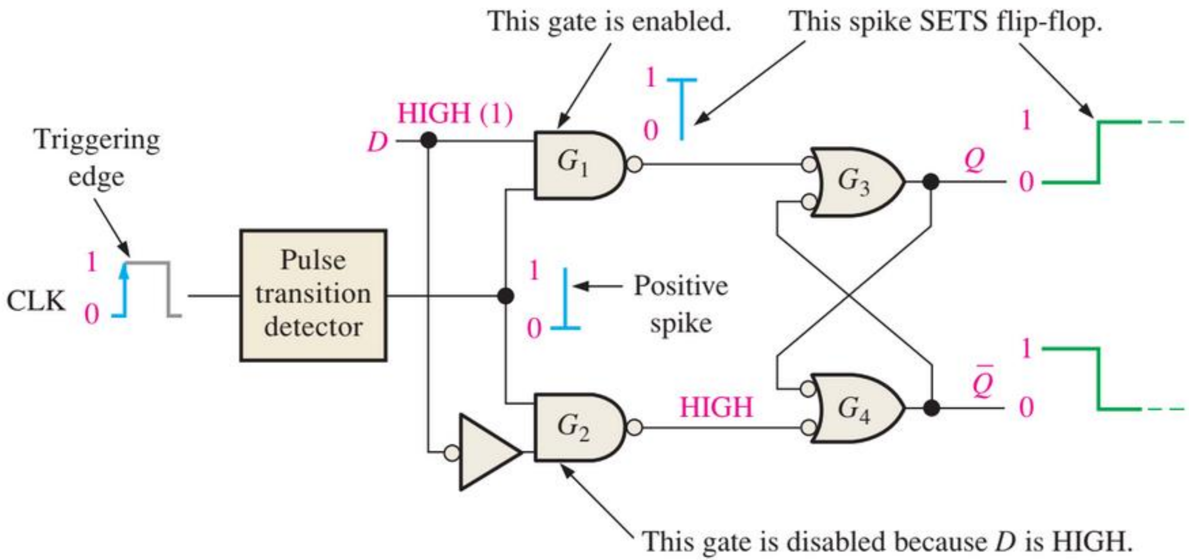


FIGURE 7–20 Flip-flop making a transition from the RESET state to the SET state on the positive-going edge of the clock pulse.

Edge Triggered - D Flip Flop

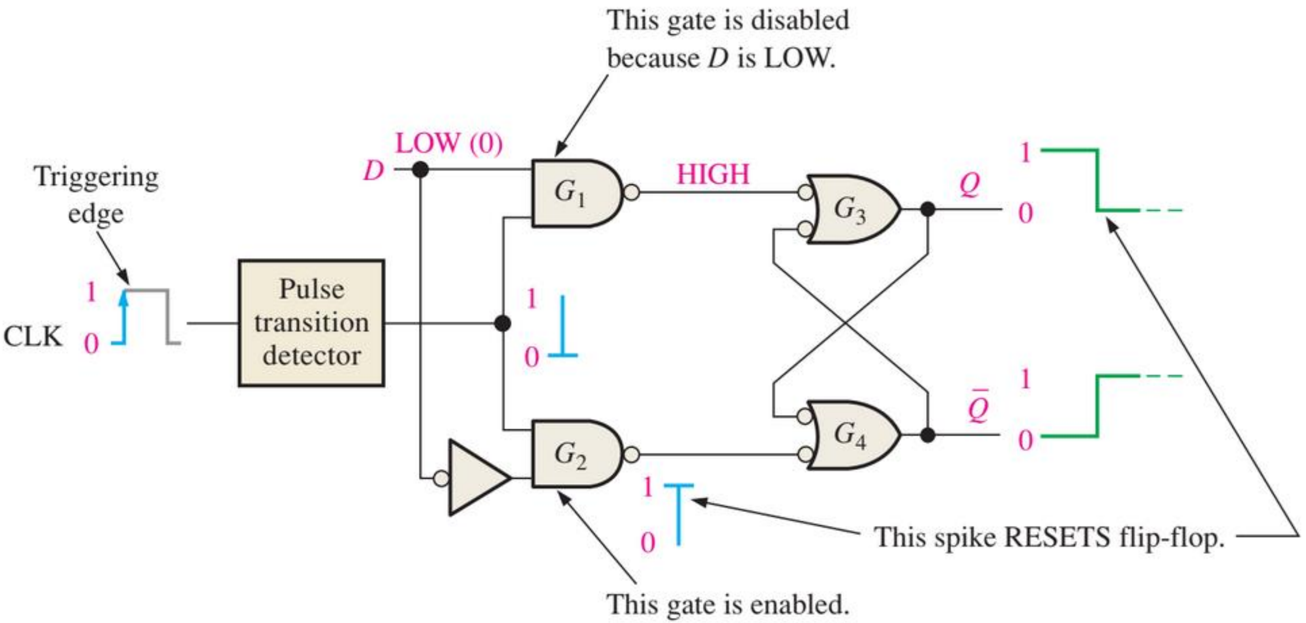


FIGURE 7–21 Flip-flop making a transition from the SET state to the RESET state on the positive-going edge of the clock pulse.

Edge Triggered - JK Flip Flop

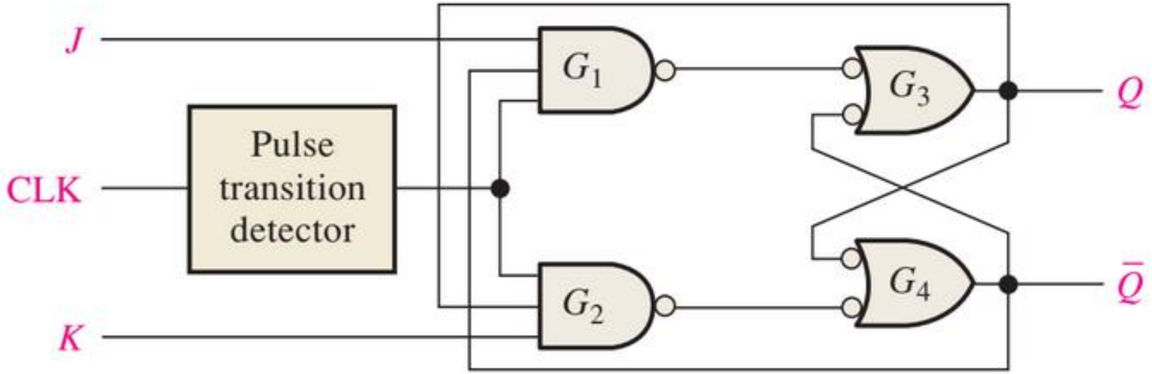


FIGURE 7–23 A simplified logic diagram for a positive edge-triggered J-K flip-flop.

Edge Triggered - JK Flip Flop

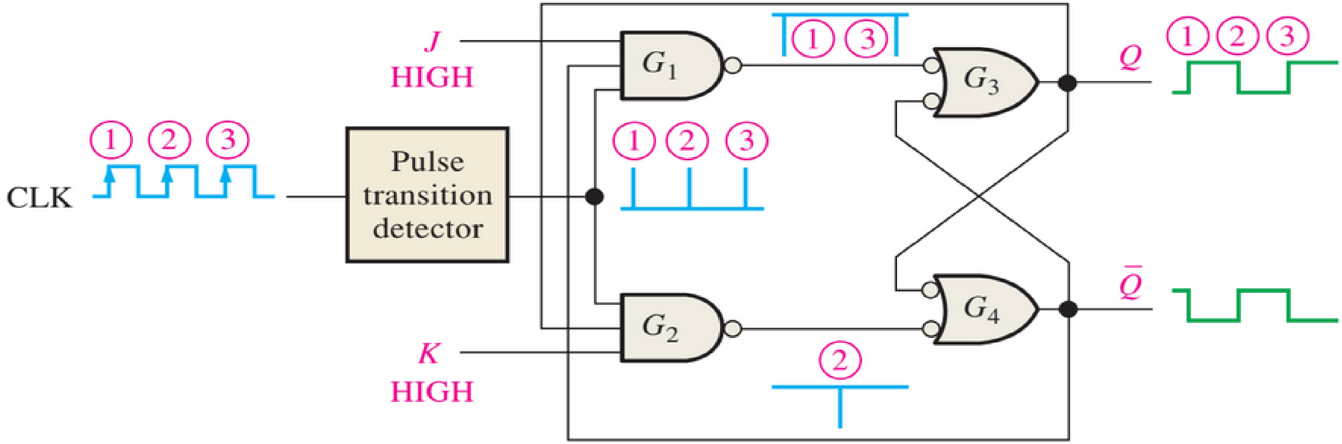


FIGURE 7–24 Transitions illustrating flip-flop operation.

A J-K flip-flop connected for toggle operation is sometimes called a T flip-flop.

Synchronous Vs Asynchronous Inputs

D and J-K inputs are called synchronous inputs, because the data transferring is synchronised with the clock.

Asynchronous inputs affect the state of the flip-flop independent of the clock.

Preset (PRE) and Clear (CLR)

OR

Direct set (SD) and Direct reset (RD)

Synchronous Vs Asynchronous Inputs

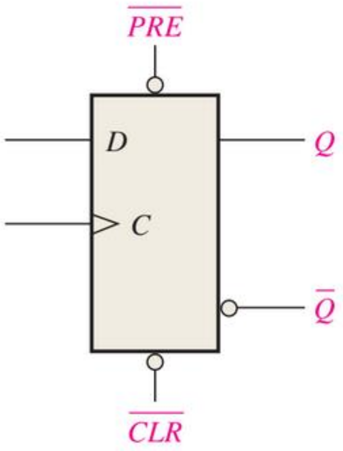


FIGURE 7–25 Logic symbol for a D flip-flop with active-LOW preset and clear inputs.

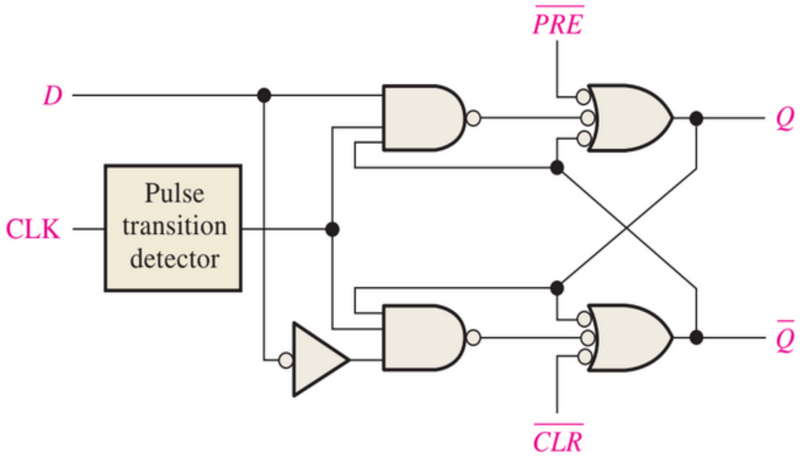
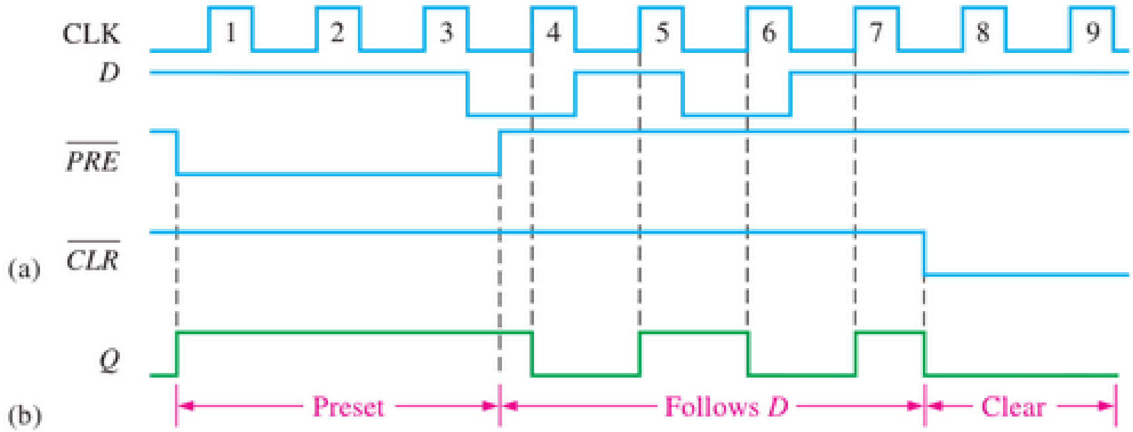
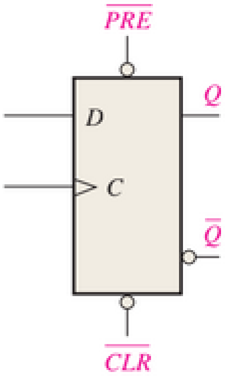


FIGURE 7–26 Logic diagram for a basic D flip-flop with active-LOW preset and clear inputs.

Synchronous Vs Asynchronous Inputs

For the positive edge-triggered D flip-flop with preset and clear inputs in Figure, determine the Q output for the inputs shown in the timing diagram in part (a) if Q is initially LOW.





Flip Flop Applications

Parallel Data Storage

This group of four flip-flops is an example of a basic register used for data storage

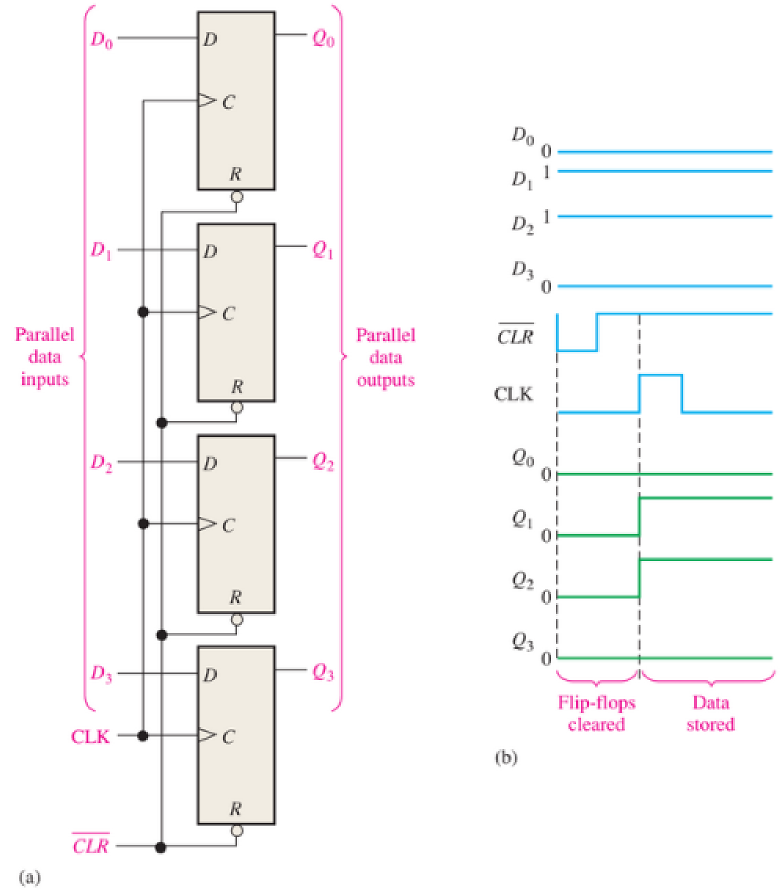


FIGURE 7–35 Example of flip-flops used in a basic register for parallel data storage.

Flip Flop Applications

Frequency Division

A single flip-flop can be applied as a divide-by-2 device.

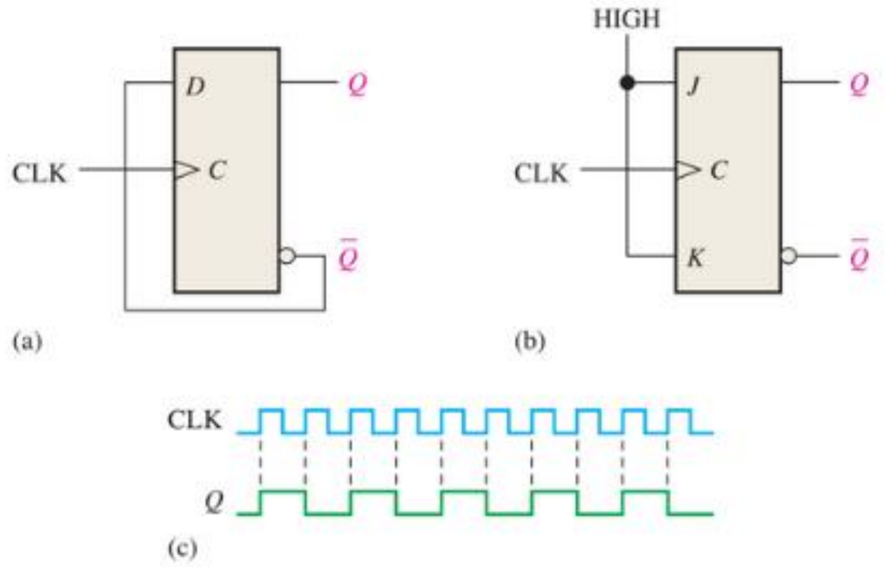
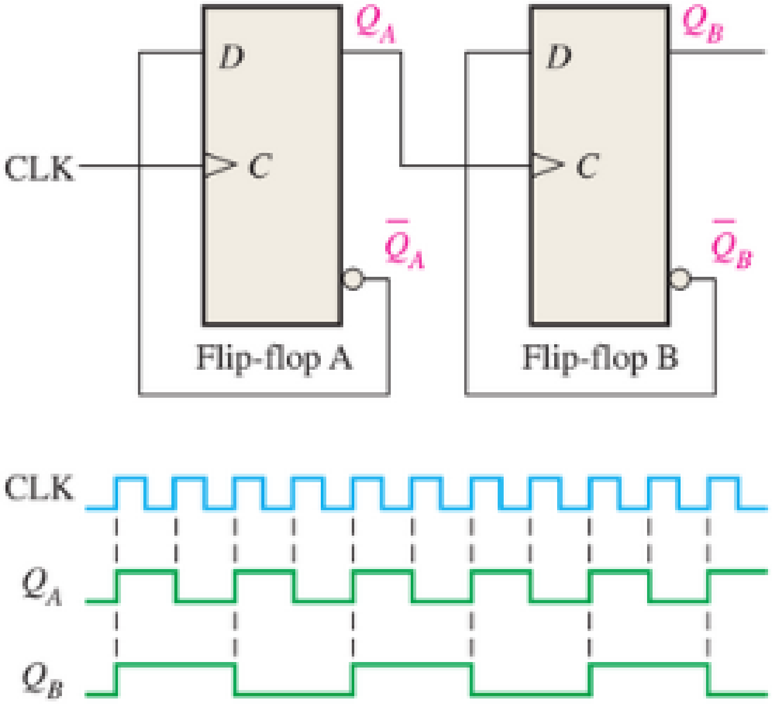


FIGURE 7–36 The D flip-flop and J-K flip-flop as a divide-by-2 device. *Q* is one-half t
frequency of CLK. Open file F07-36 and verify the operation.

Flip Flop Applications

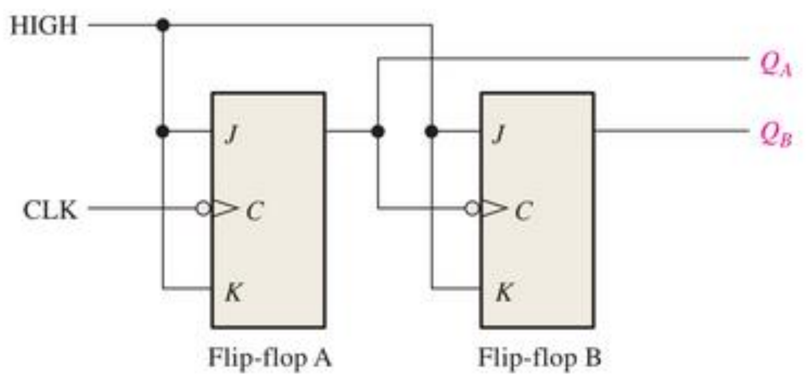
Frequency Division

Further division of a clock frequency can be achieved by using the output of one flip-flop as the clock input to a second flip-flop.



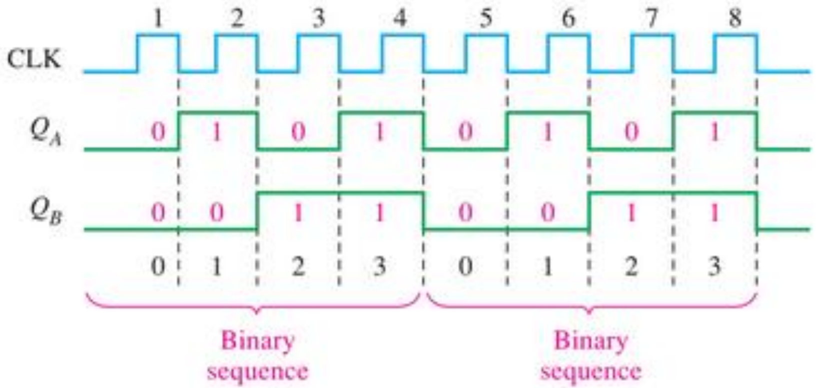
Flip Flop Applications

Counters



J-K flip-flops used to generate a binary count sequence (00,01,10,11).

Two repetitions are shown.



Home Task

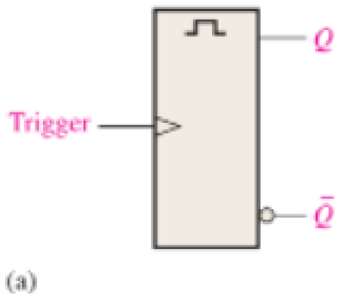
Design a counter which can count from 0 through 15.

Reading Task : 7-3 Flip-Flop Operating Characteristics

One Shots

Also known as a monostable multivibrator is a device with only one stable state.

The time that the device stays in its unstable state determines the pulse width of its output.



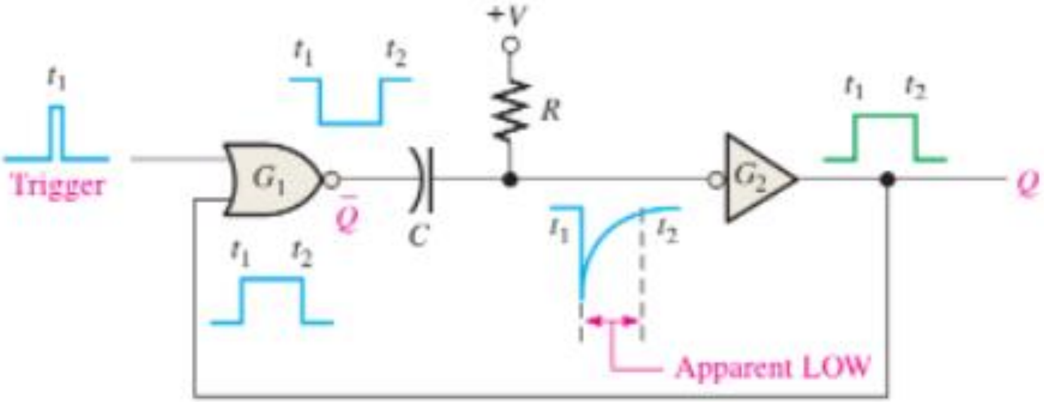


FIGURE 7–43 A simple one-shot circuit.

One Shots

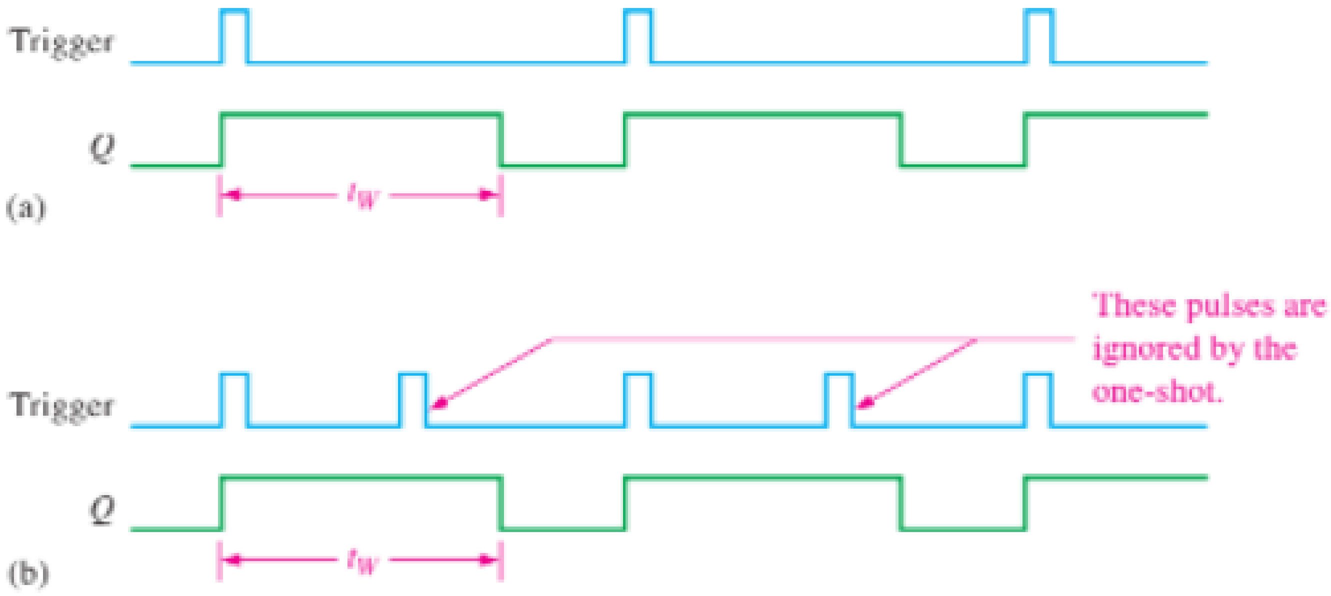


FIGURE 7–45 Nonretriggerable one-shot action.

One Shots

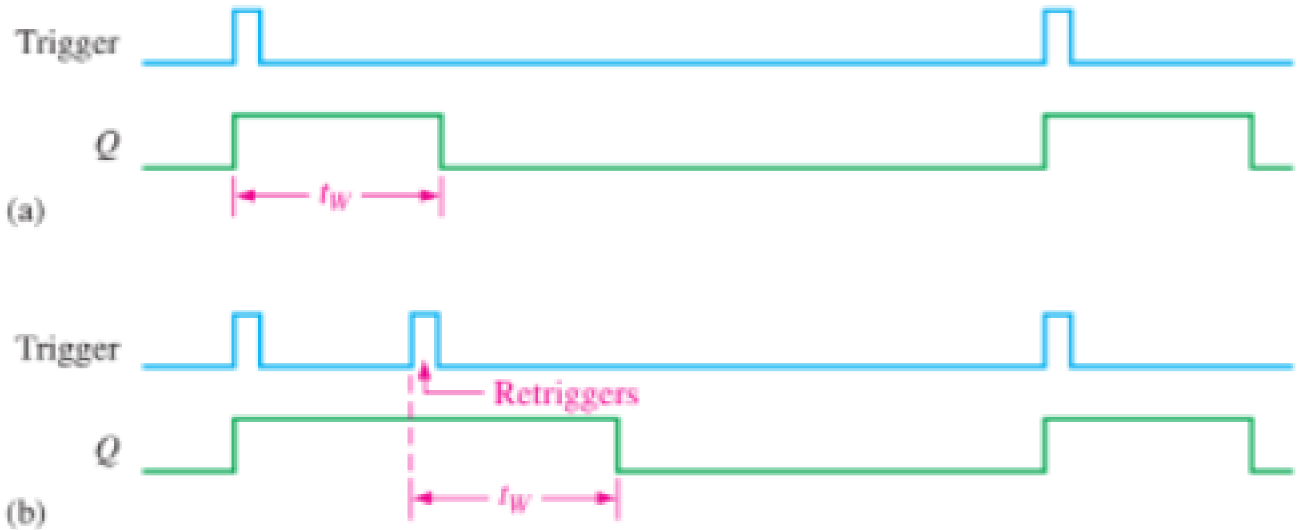


FIGURE 7–46 Retriggerable one-shot action.

The Astable Multivibrator

Has no stable states

It changes back and forth (oscillates) between two unstable states without any external triggering.

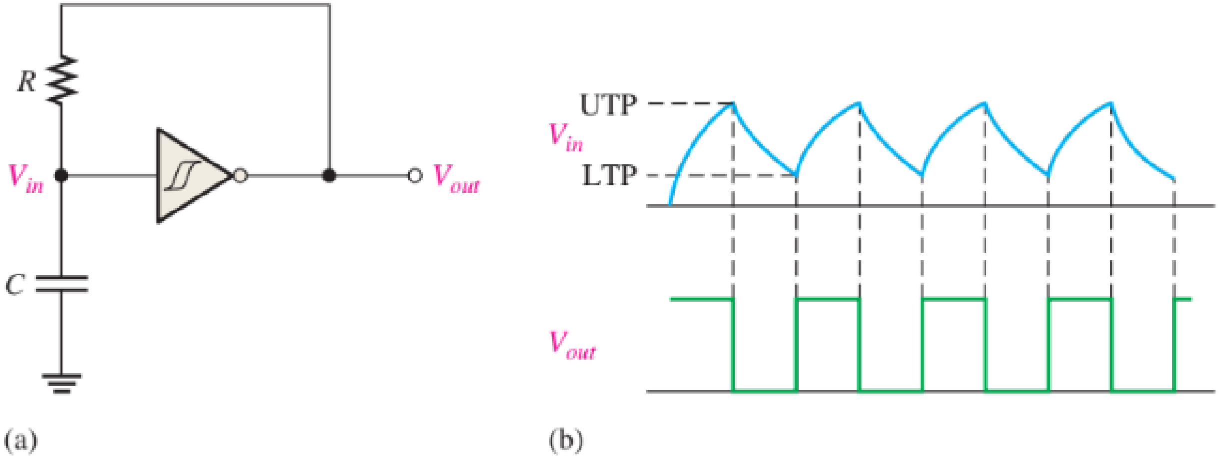


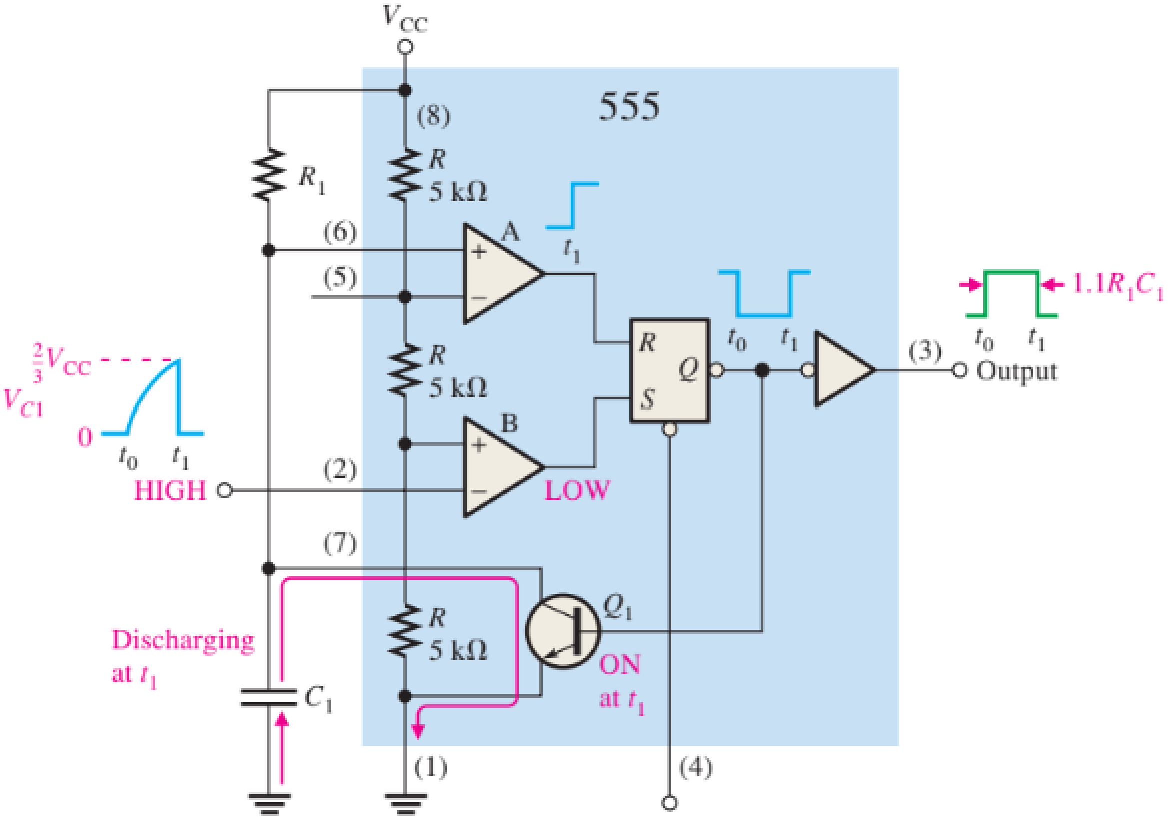
FIGURE 7–55 Basic astable multivibrator using a Schmitt trigger.

The Astable Multivibrator

The resulting output is typically a square wave that is used as a clock signal in many logic circuits.

Also known as pulse oscillators.

555 Timer



V_{CC}
555
(8)
(6)
(5)
(2)
(7)
(1)
(4)
(3)
R_1
R 5 kΩ
R 5 kΩ
R 5 kΩ
A
B
t_1
R
Q
S
t_0 t_1
$1.1R_1C_1$
t_0 t_1
Output
$\frac{2}{3}V_{CC}$
V_{C1}
0
t_0 t_1
HIGH
LOW
Q_1
ON
at t_1
Discharging
at t_1
C_1

555 Timer

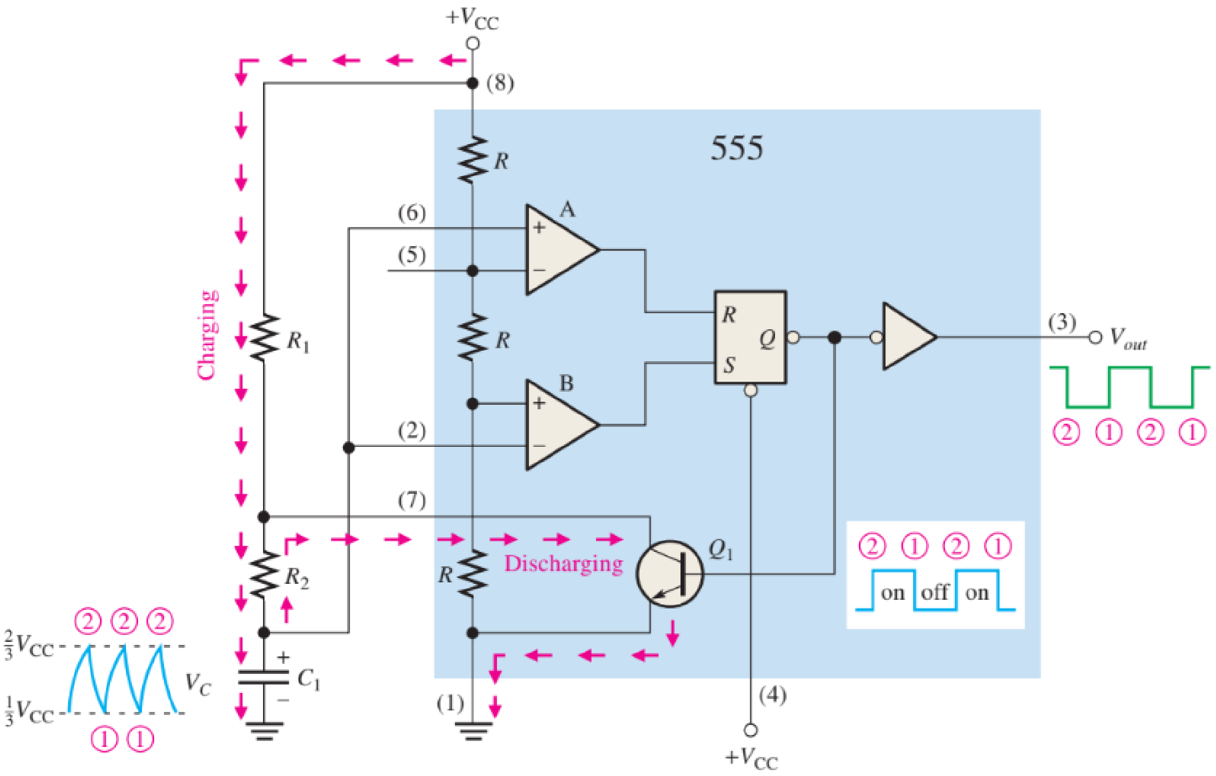


FIGURE 7–57 Operation of the 555 timer in the astable mode.