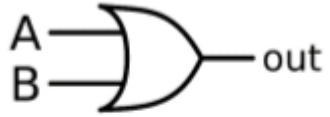


OR gate



AND gate



COL gate



BILL gates



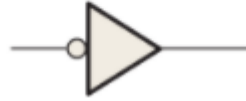
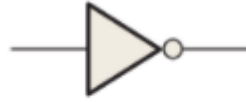
# LOGIC GATES

CHAPTER 3

**Sumaiyah Zahid**

# INVERTER OR NOT GATE

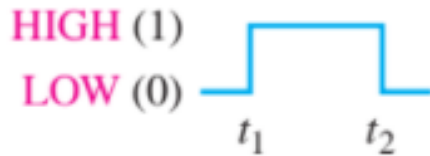
## Complementation



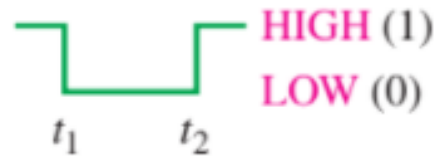
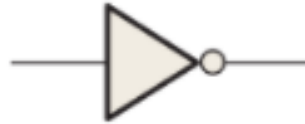
**TABLE 3-1**

Inverter truth table.

Input	Output
LOW (0)	HIGH (1)
HIGH (1)	LOW (0)



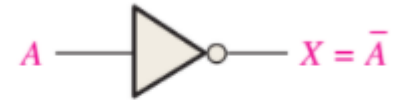
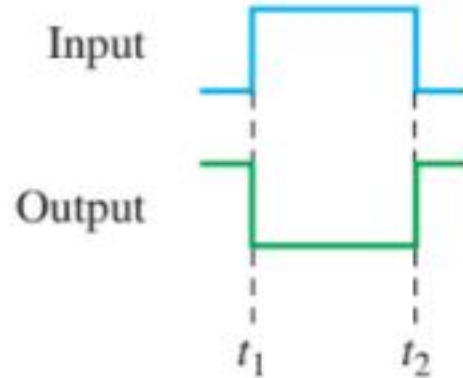
Input pulse



Output pulse

# INVERTER TIMING DIAGRAM

A timing diagram shows how two or more waveforms relate in time.



**FIGURE 3-6** The inverter complements an input variable.

# AND GATE

A	B	
0	0	0
1	0	0
0	1	0
1	1	1

AND Gate = Boolean Multiplication



# AND GATE

- (a) Develop the truth table for a 3-input AND gate.
- (b) Determine the total number of possible input combinations for a 4-input AND gate.

# AND GATE

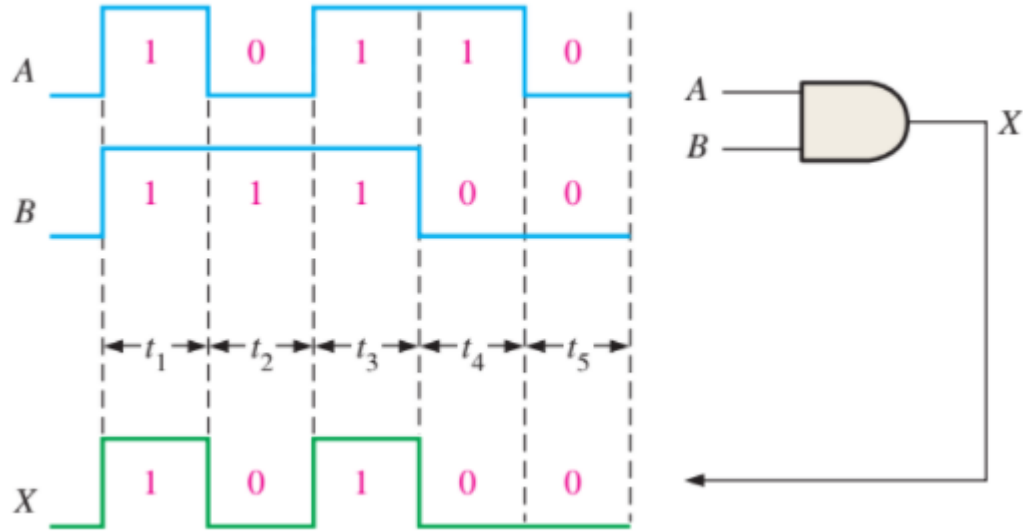
(a) Develop the truth table for a 3-input AND gate.

(b) Determine the total number of possible input combinations for a 4-input AND gate.

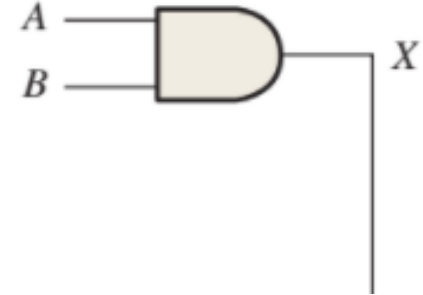
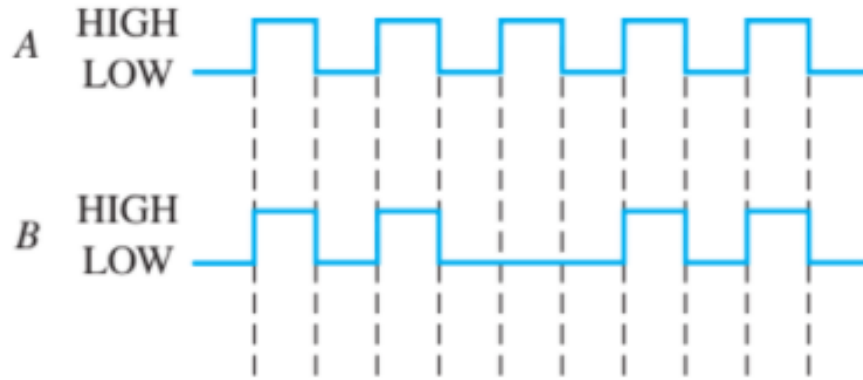
**TABLE 3-3**

Inputs			Output
<i>A</i>	<i>B</i>	<i>C</i>	<i>X</i>
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

# AND GATE TIMING DIAGRAM

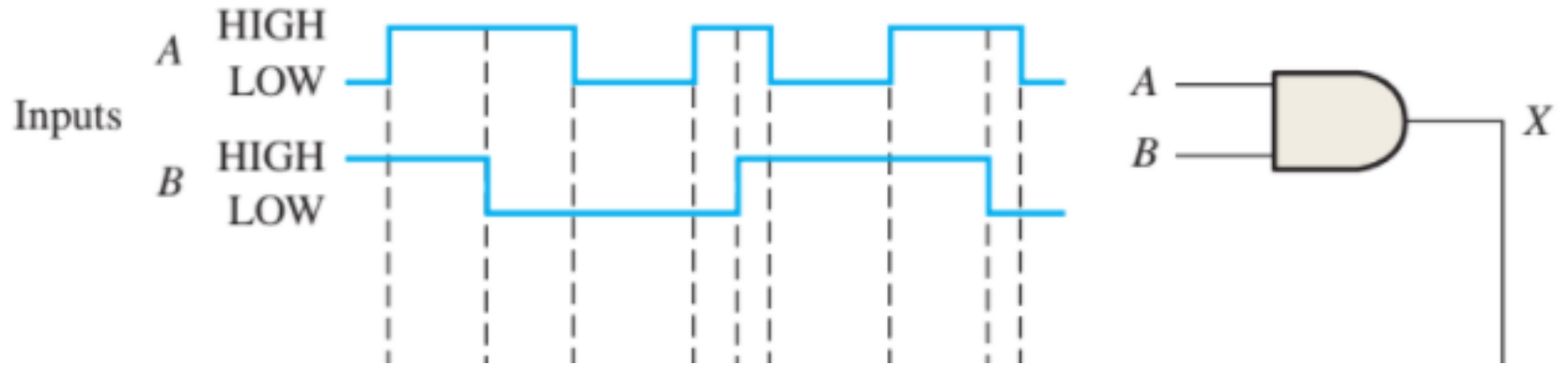


# AND GATE TIMING DIAGRAM

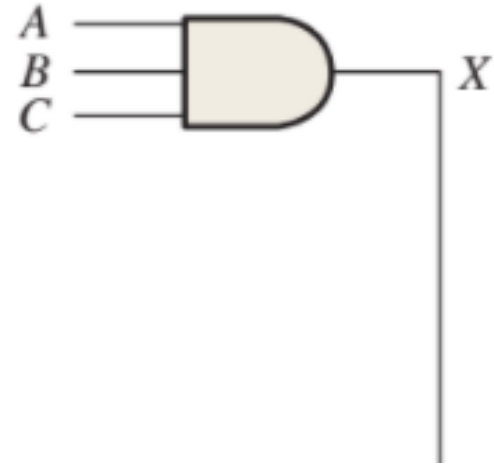
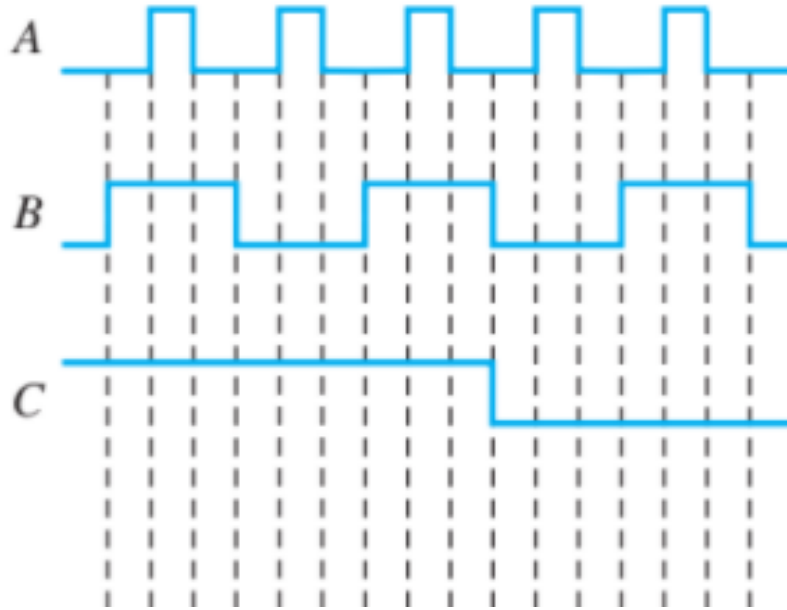




# AND GATE TIMING DIAGRAM

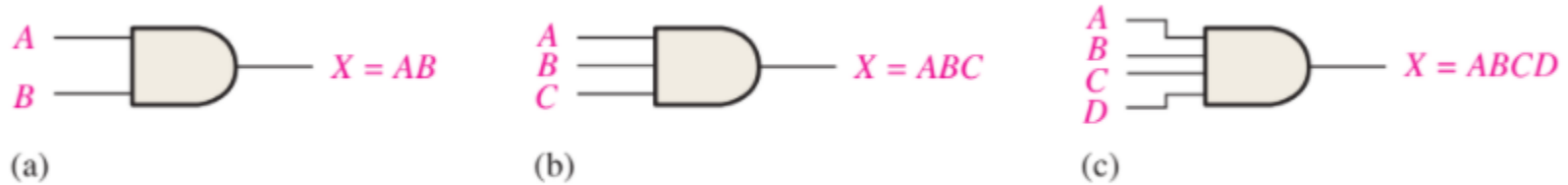


# AND GATE TIMING DIAGRAM



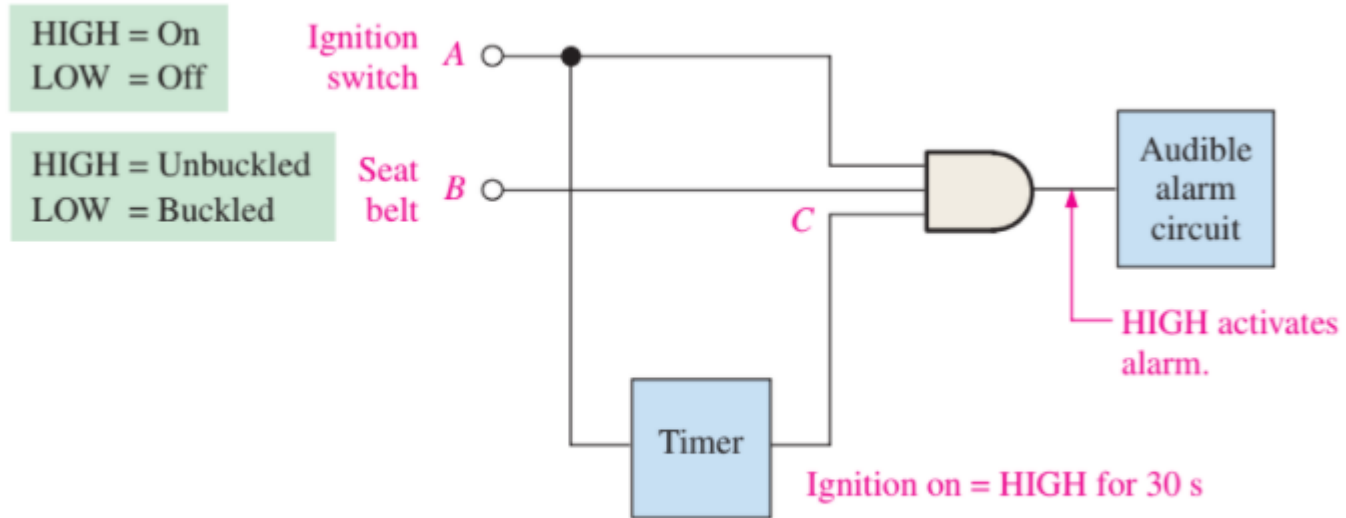
# AND GATE

Boolean multiplication is the same as the AND function.



**FIGURE 3-15** Boolean expressions for AND gates with two, three, and four inputs.

# AND GATE APPLICATION



**FIGURE 3-17** A simple seat belt alarm circuit using an AND gate.

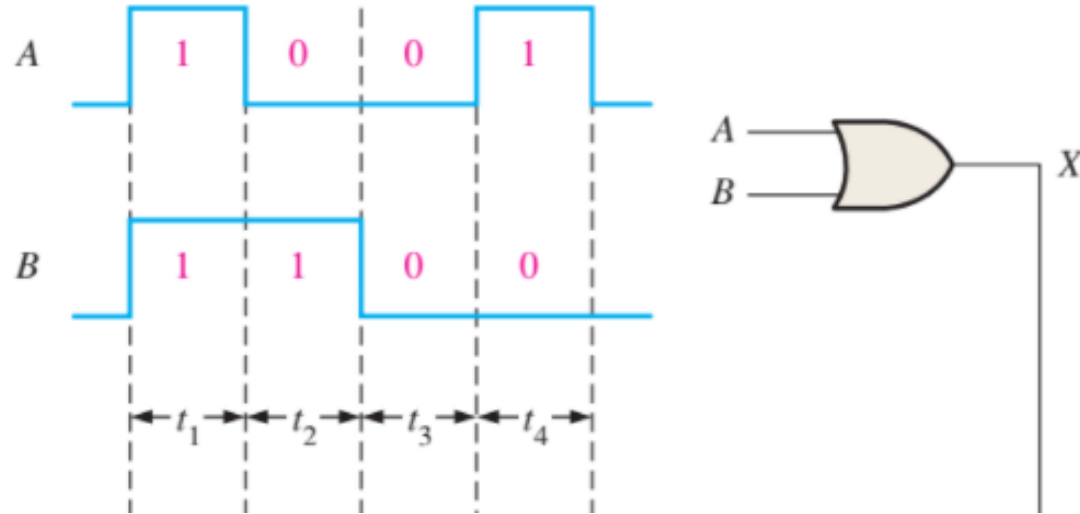
# OR GATE

OR Gate = Boolean Addition

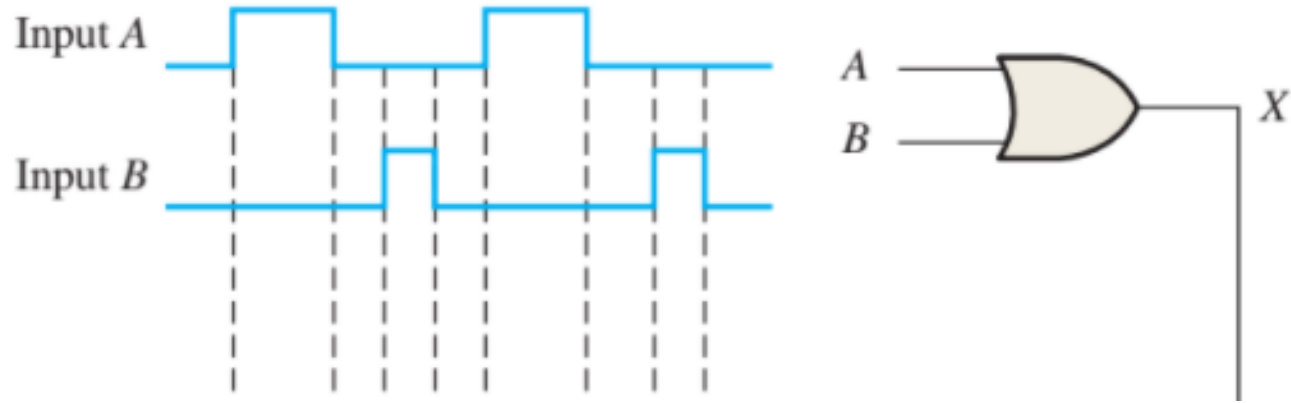
INPUT		OUTPUT
A	B	
0	0	0
1	0	1
0	1	1
1	1	1



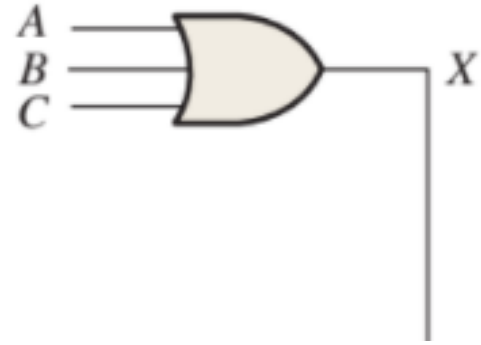
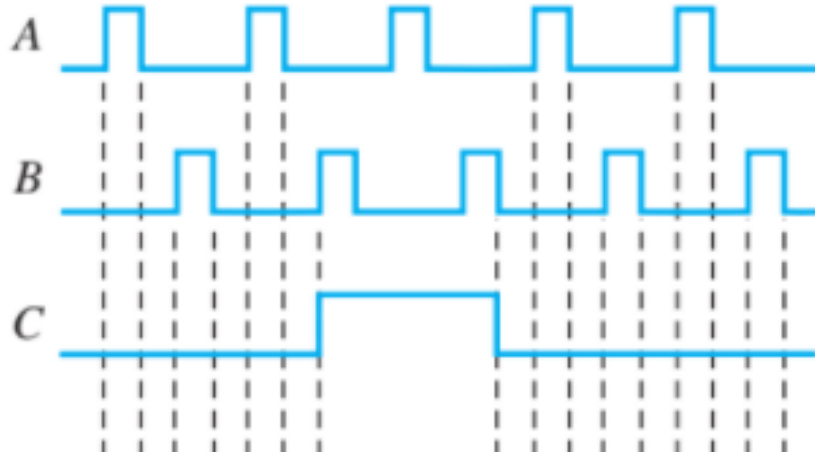
# OR GATE TIMING DIAGRAM



# OR GATE TIMING DIAGRAM



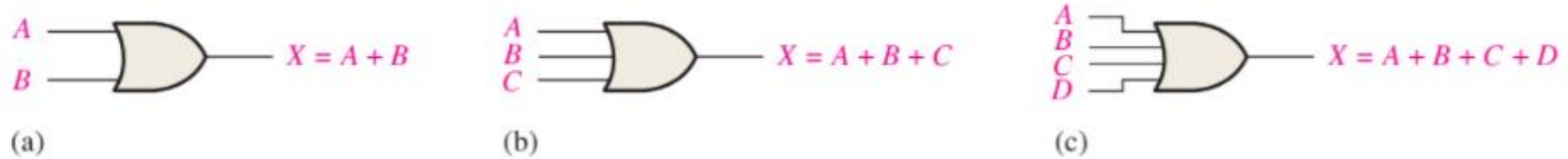
# OR GATE TIMING DIAGRAM





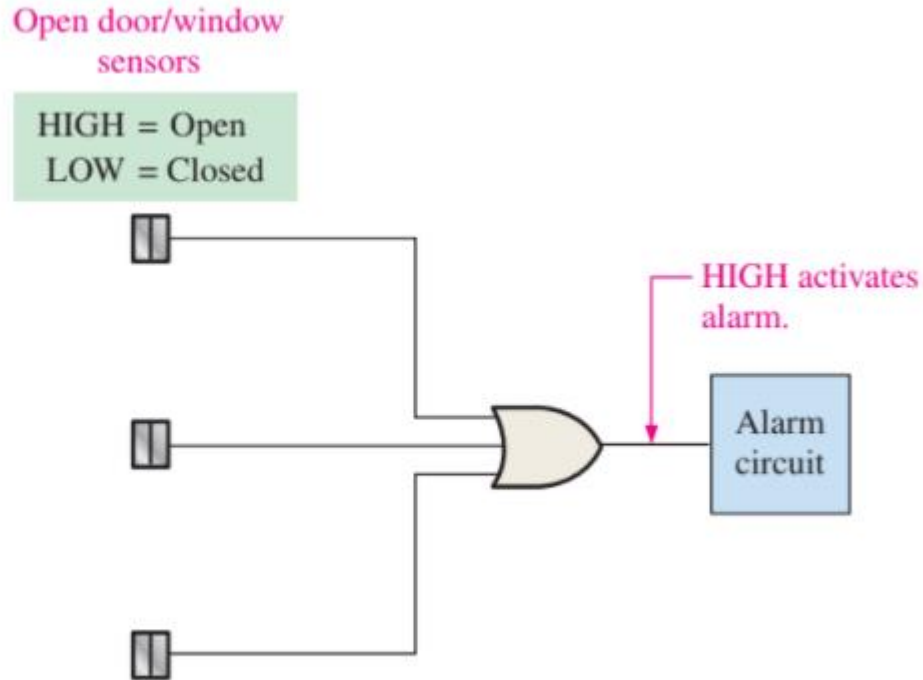
# OR GATE

Boolean addition is the same as the OR function.



**FIGURE 3-24** Boolean expressions for OR gates with two, three, and four inputs.

# OR GATE APPLICATION

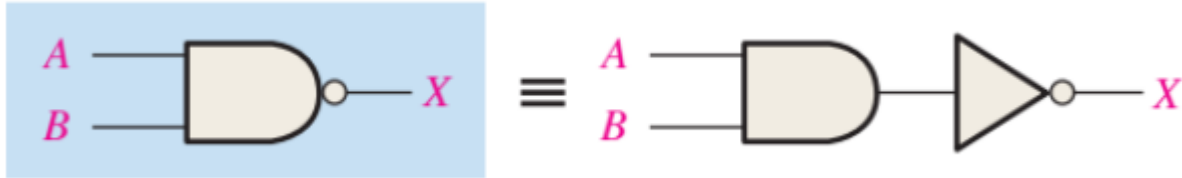


**FIGURE 3-25** A simplified intrusion detection system using an OR gate.

# NAND GATE

NAND = Not AND

Also known as Universal Gate

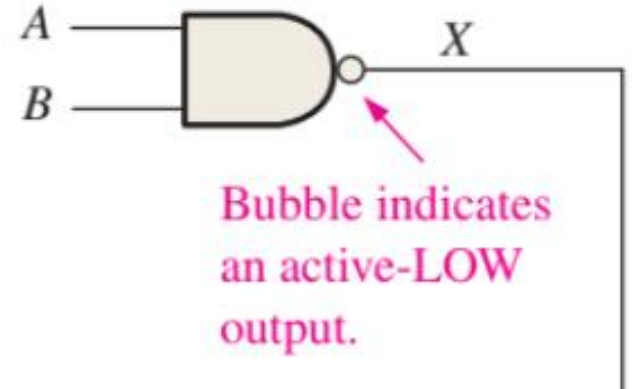
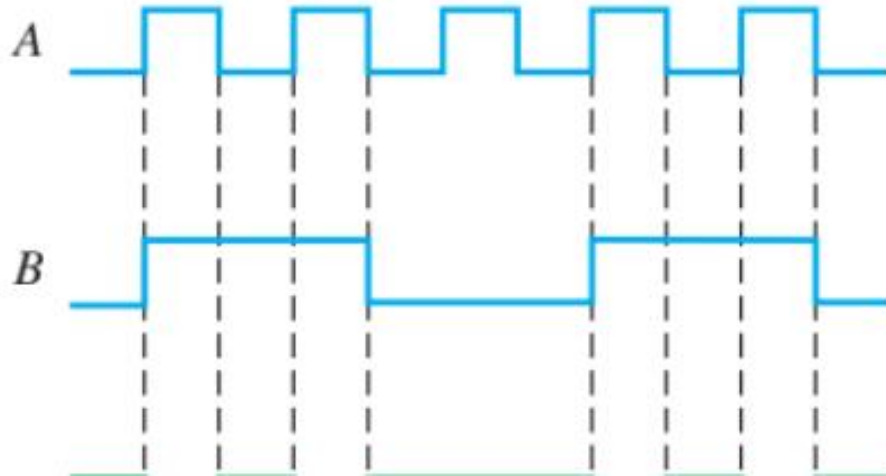


**TABLE 3-7**

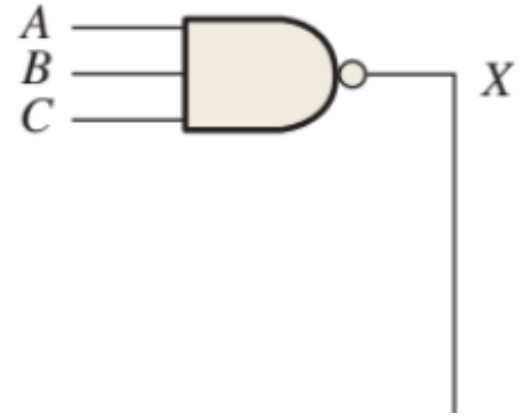
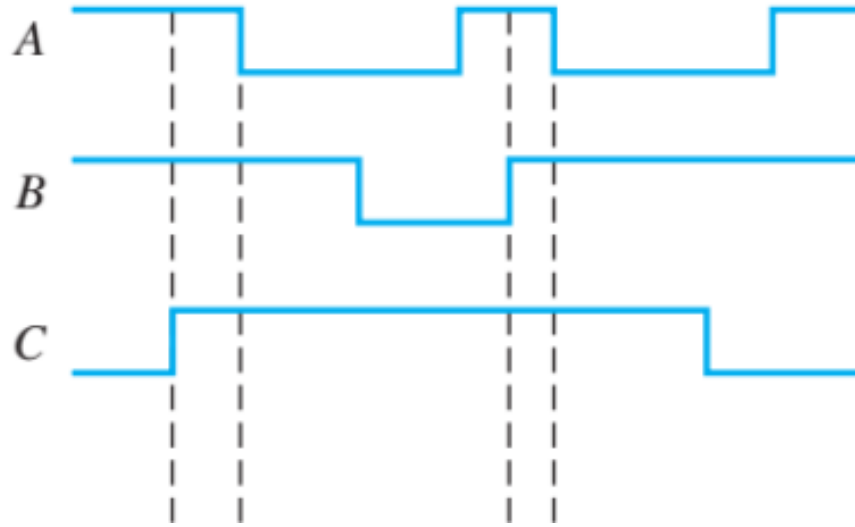
Truth table for a 2-input NAND gate.

Inputs		Output
<i>A</i>	<i>B</i>	<i>X</i>
0	0	1
0	1	1
1	0	1
1	1	0

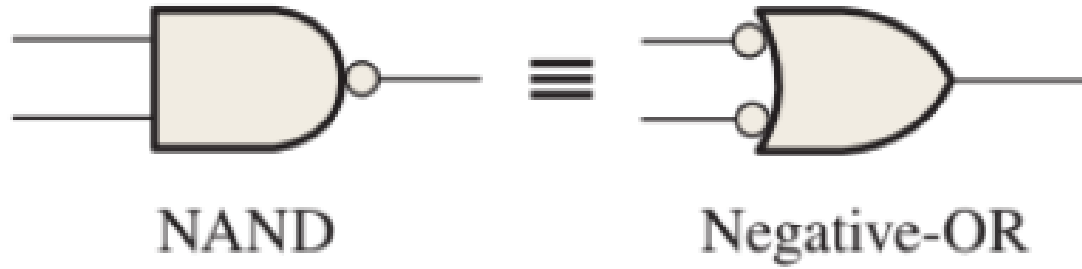
# NAND GATE TIMING DIAGRAM



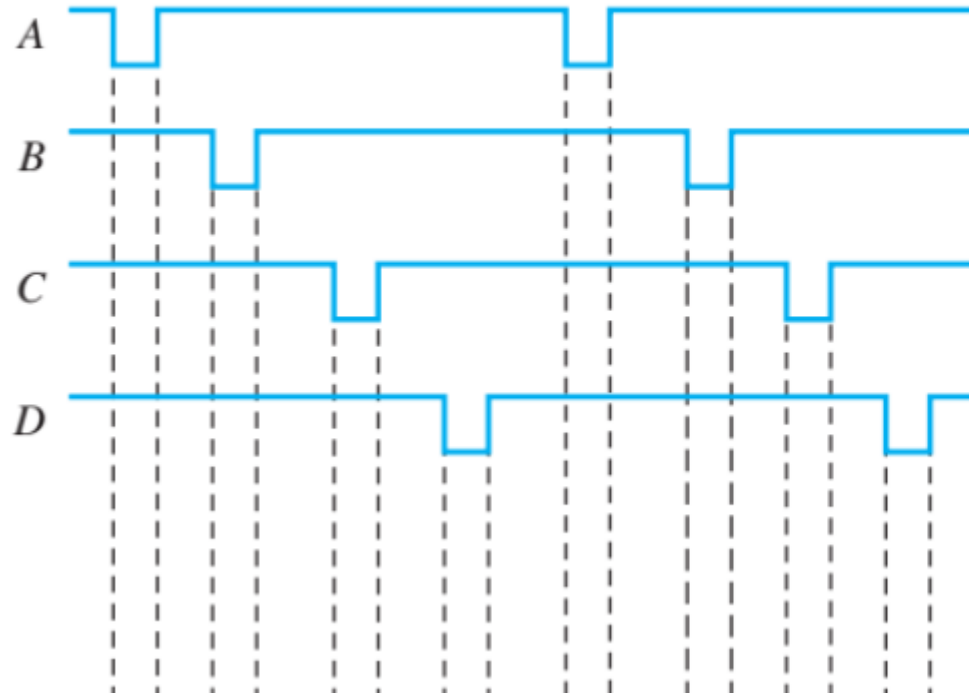
# NAND GATE TIMING DIAGRAM



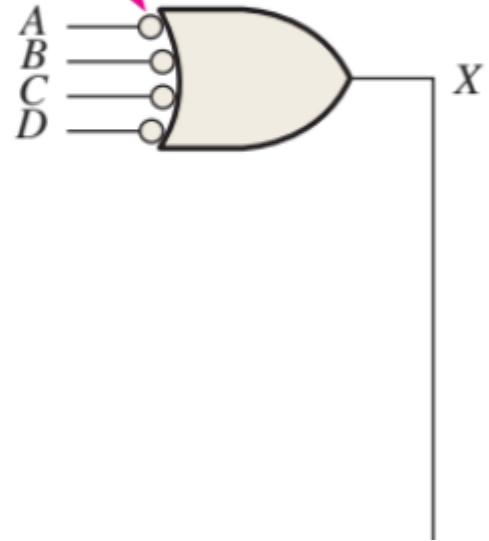
# NAND GATE



# NAND GATE



Bubbles indicate active-LOW inputs.



# NAND GATE

$$X = \overline{AB}$$

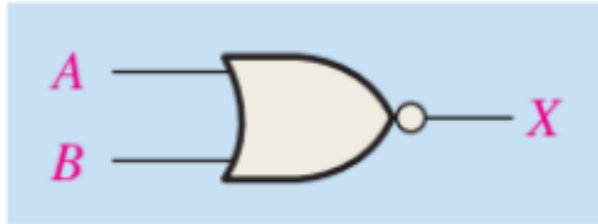
**TABLE 3-8**

<i>A</i>	<i>B</i>	$\overline{AB} = X$
0	0	$\overline{0 \cdot 0} = \overline{0} = 1$
0	1	$\overline{0 \cdot 1} = \overline{0} = 1$
1	0	$\overline{1 \cdot 0} = \overline{0} = 1$
1	1	$\overline{1 \cdot 1} = \overline{1} = 0$



# NOR GATE

NOR = Not OR



≡

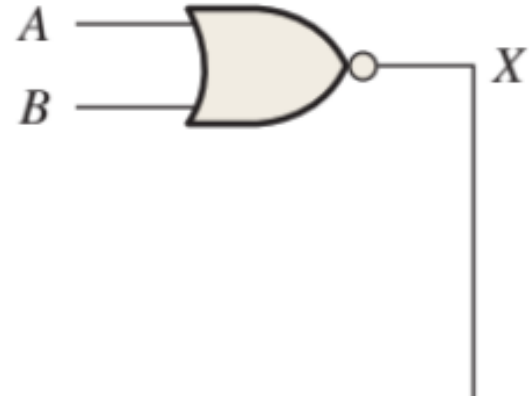
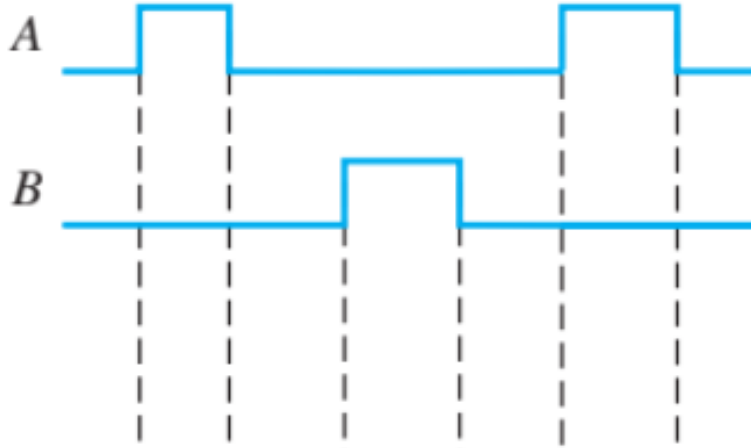


**TABLE 3-9**

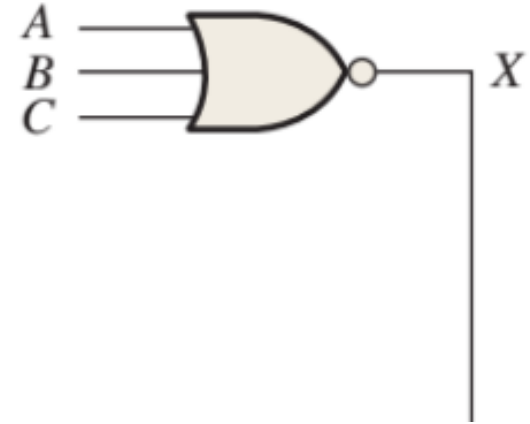
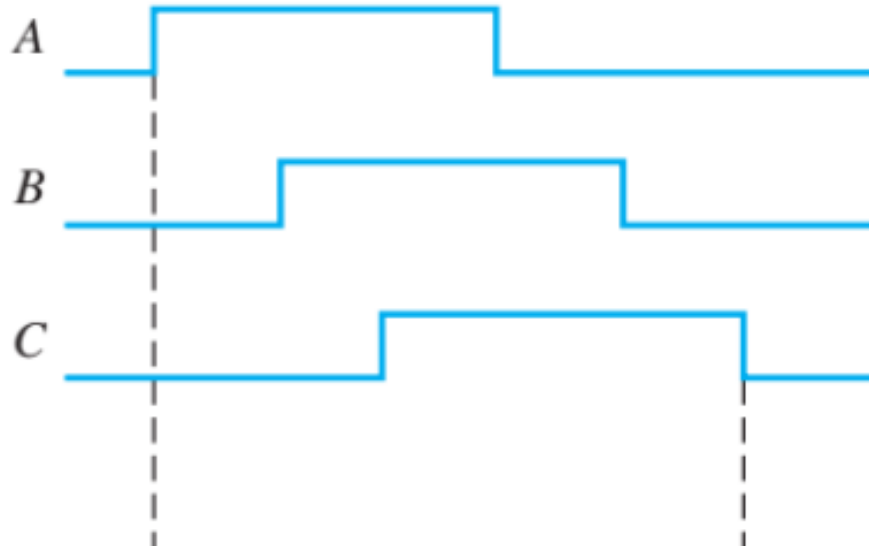
Truth table for a 2-input NOR gate.

Inputs		Output
<i>A</i>	<i>B</i>	<i>X</i>
0	0	1
0	1	0
1	0	0
1	1	0

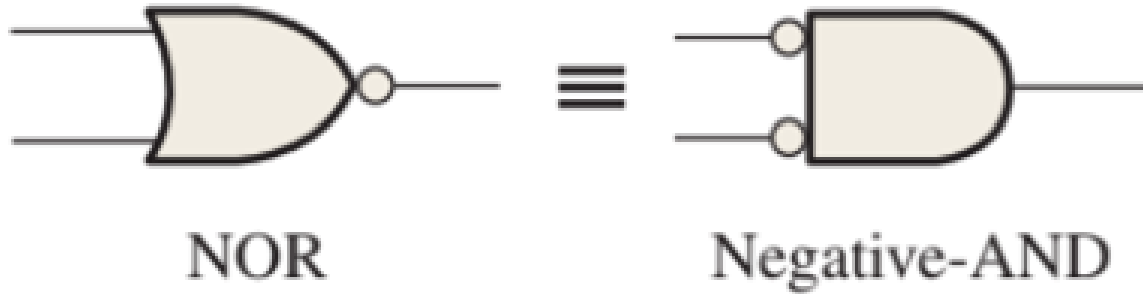
# NOR GATE TIMING DIAGRAM



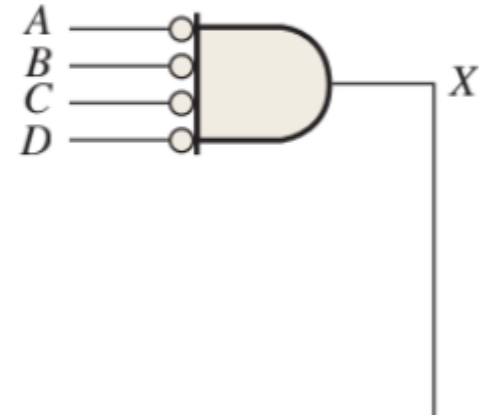
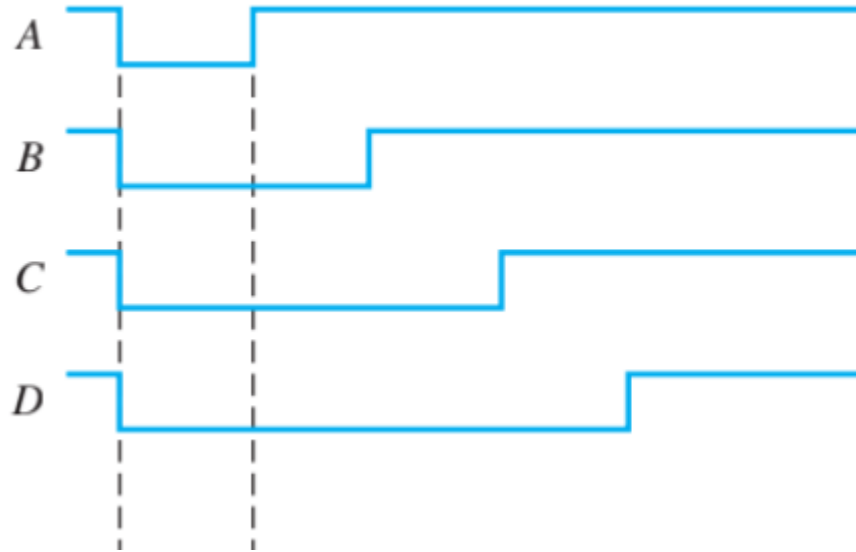
# NOR GATE TIMING DIAGRAM



# NOR GATE



# NOR GATE TIMING DIAGRAM



# NOR GATE

$$X = \overline{A + B}$$

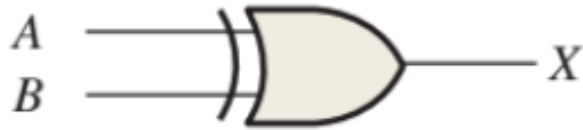
**TABLE 3-10**

<i>A</i>	<i>B</i>	$\overline{A + B} = X$
0	0	$\overline{0 + 0} = \overline{0} = 1$
0	1	$\overline{0 + 1} = \overline{1} = 0$
1	0	$\overline{1 + 0} = \overline{1} = 0$
1	1	$\overline{1 + 1} = \overline{1} = 0$

# EXCLUSIVE OR GATE

Exclusive or XOR Gate

Performs modulo-2 addition

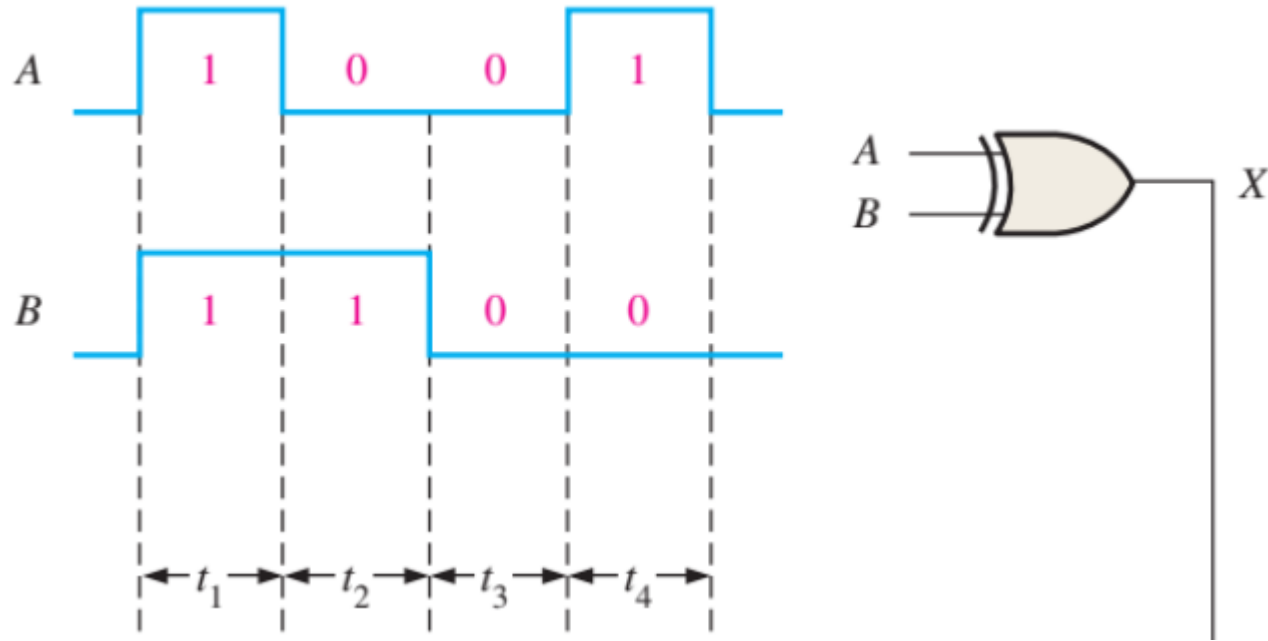


**TABLE 3-11**

Truth table for an exclusive-OR gate.

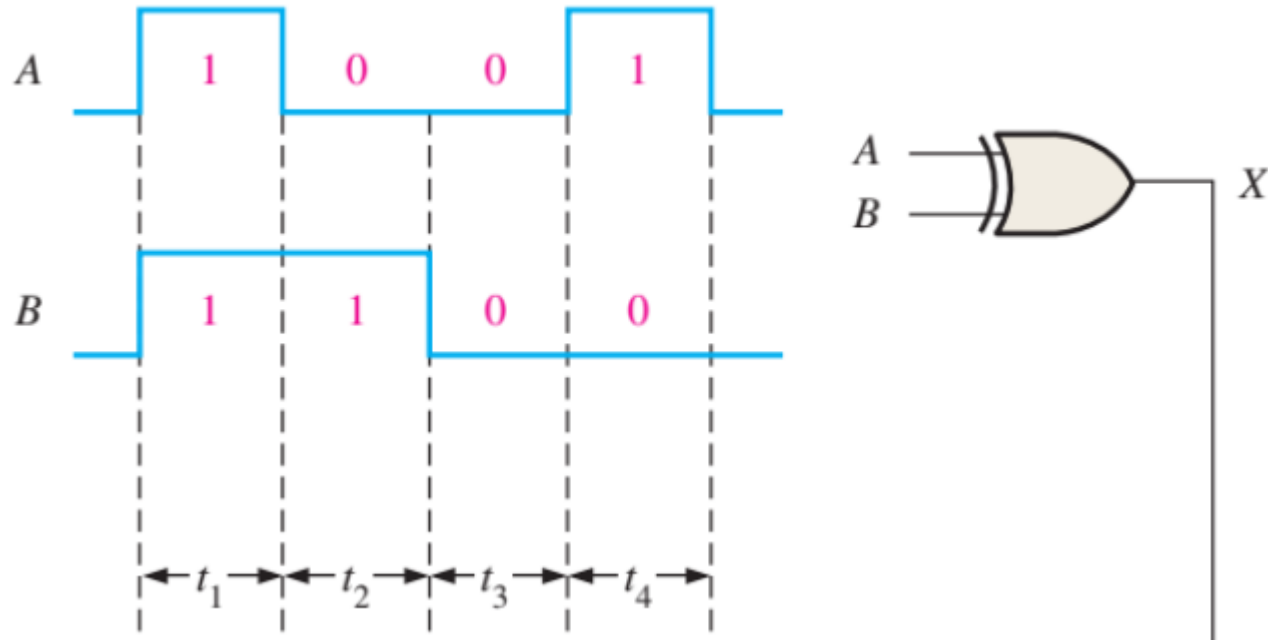
Inputs		Output
<i>A</i>	<i>B</i>	<i>X</i>
0	0	0
0	1	1
1	0	1
1	1	0

# EXCLUSIVE OR GATE TIMING DIAGRAM





# EXCLUSIVE OR GATE TIMING DIAGRAM

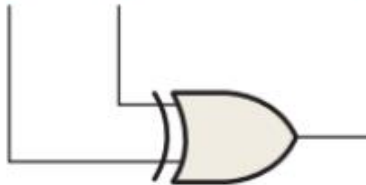


# XOR APPLICATION

**TABLE 3-13**

An XOR gate used to add two bits.

Input Bits		Output (Sum)
<i>A</i>	<i>B</i>	$\Sigma$
0	0	0
0	1	1
1	0	1
1	1	0 (without the 1 carry bit)



# EXCLUSIVE NOR GATE

Exclusive NOT OR or XNOR Gate

Performs modulo-2 addition

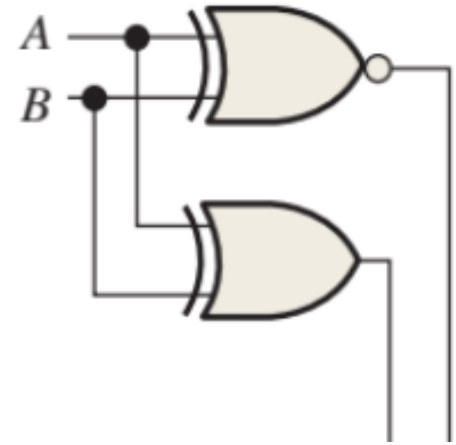
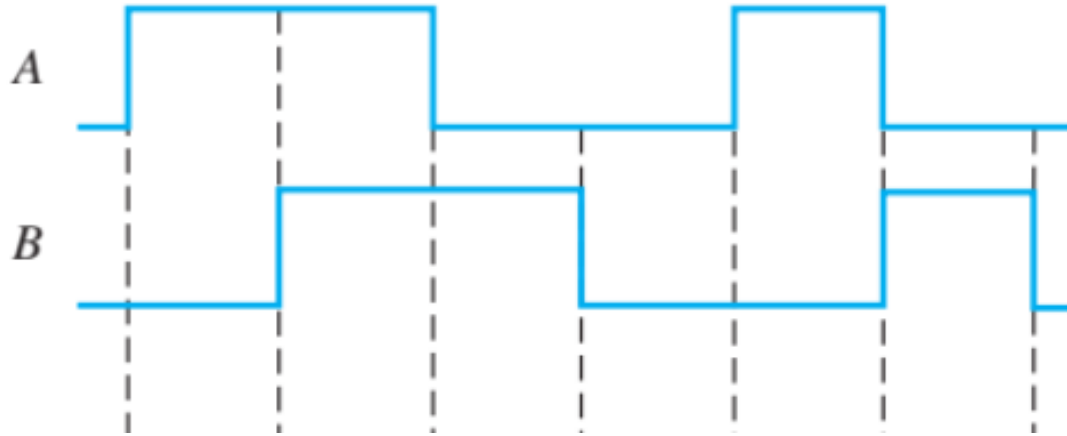


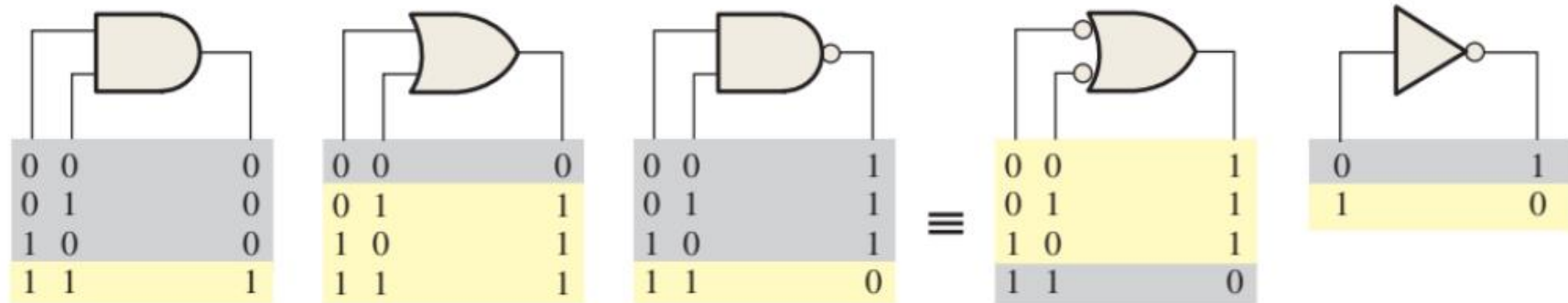
**TABLE 3-12**

Truth table for an exclusive-NOR gate.

Inputs		Output
<i>A</i>	<i>B</i>	<i>X</i>
0	0	1
0	1	0
1	0	0
1	1	1

# XNOR GATE TIMING DIAGRAM





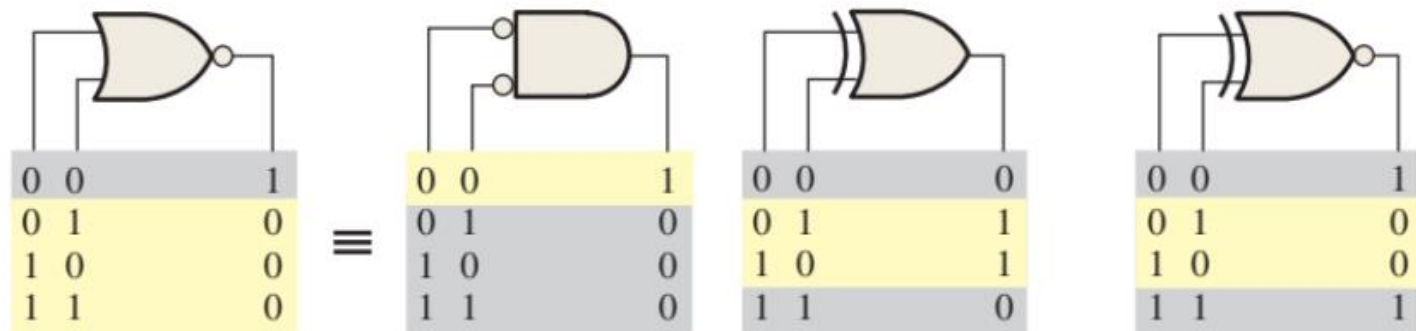
AND

OR

NAND

Negative-OR

Inverter



NOR

Negative-AND

Exclusive-OR

Exclusive-NOR

Note: Active states are shown in yellow.

**FIGURE 3-75**