Multi-Partner Project: Architectures and Design Methodologies to Accelerate AI Workloads. The ICSC Flagship 2 Project

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***Abstract*—Recent pre-exascale and exascale supercomputers have driven the development of increasingly sophisticated AI models for diverse applications, including image recognition and classification, natural language processing, and generative AI. These applications require specialized hardware accelerators, to handle the heavy computational demands of AI algorithms in an energy-efficient manner. Today, AI accelerators are deployed across various systems, from low-power edge devices to large-scale servers, high-performance computing (HPC) infrastructures, and data centers. The primary objective of the ICSC Flagship 2 project, discussed in this paper, is to develop heterogeneous hardware platforms optimized to accelerate HPC and big data applications. Specifically, this paper provides an overview of the key challenges addressed and the achievements realized at the current intermediate stage of the ICSC Flagship 2 project focused on architectures, technologies, and design methodologies to design efficient hardware accelerators for AI workloads, such as deep learning (DL) and transformer models.**

***Index Terms*—High-Performance Computing, Heterogeneous Architectures, AI Accelerators, RISC-V Architecture, Emerging Memory Technologies.**

I. Introduction

The ICSC Italian National Research Center for High-Performance Computing, Big Data, and Quantum Computing is a central hub for supercomputing infrastructure, supported by ten specialized research spokes, each concentrating on a specific thematic area. Among these, Spoke 1, focused on Future HPC, stands as the technological cornerstone of ICSC, committed to advancing state-of-the-art hardware and software technologies for next-generation supercomputers. Research within Spoke 1 is structured around five flagship scientific projects, involving collaboration from 15 Italian universities and 9 leading industries.

The primary objective of the Flagship 2 project is to design hardware accelerators for heterogeneous platforms to support AI workloads. This focus is driven by recent disruptive advances in AI, which have amplified the need for efficient hardware accelerators tailored to complex AI models in HPC environments. Developing these accelerators requires a multidisciplinary approach, drawing on expertise from diverse domains, including computer architecture, AI and machine learning algorithms, computational models, compiler technologies, and approximate computing.

In this context, several methodologies and tools have been proposed in recent years to design accelerators for AI, including hardware-software co-design approaches, High-Level Synthesis methods, customized compilers, and methodologies for design space exploration, modeling, and simulation. These methodologies share a common objective: to maximize computational parallelism for optimal performance while ensuring energy efficiency, thereby enabling the acceleration of AI tasks.

After a brief analysis of the state-of-the-art hardware accelerators for heterogeneous HPC platforms and perspectives on design methodologies for accelerating AI on heterogeneous architectures, this paper provides an overview of the key research challenges addressed and the main achievements reached at the current intermediate stage of the Flagship 2 project. More in detail, the paper is focused on the following research topics:

- Developing a toolchain for design space exploration and High-Level Synthesis (HLS) for AI accelerators;
- Designing efficient In-Memory Computing (IMC) architectures based on emerging technologies;
- Designing FPGA-based accelerators based on approximate computing;
- Exploiting heterogeneous CPU, GPU, ASIC, and FPGA platforms for AI and HPC applications;
- Designing accelerators based on RISC-V open-HW processor architecture.

II. State-Of-The-Art on Architectures and Design Methodologies for AI Accelerators

Stimulated by the recent AI trends that impose the use of hardware accelerators as one of the most viable solutions for several classes of applications, the ICSC Flagship 2 project mainly focused its analysis on state-of-the-art design methodologies suitable to design hardware accelerators and heterogeneous platforms for AI workloads for HPC systems, with special attention to Deep Neural Networks (DNNs) and Transformers.

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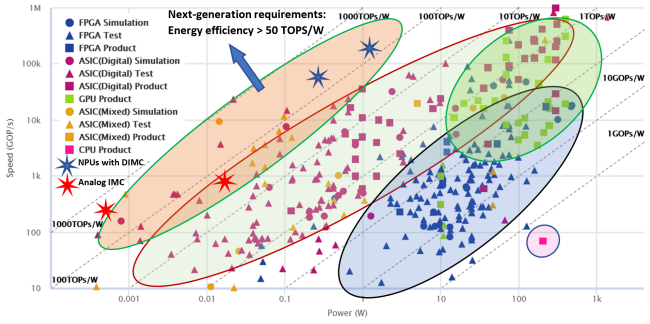


Fig. 1. Trends of state-of-the-art AI accelerators in terms of TOPs/W. Reprinted with permission from [2]. ©2024 IEEE.

One of the first outcomes of the ICSC Flagship 2 project is a survey on hardware architectures designed to accelerate AI workloads and focused on maximizing computational throughput and energy efficiency [1]. Common solutions leverage manycore architectures such as Graphics Processing Units (GPUs), Tensor Processing Units (TPUs), and Neural Processing Units (NPUs). Additional platforms include the RISC-V open-core and reconfigurable cores such as Coarse-Grained Reconfigurable Architectures (CGRAs) and Field-Programmable Gate Arrays (FPGAs). Each of these technologies can be exploited to handle the intensive, parallel nature of AI computations, offering different characteristics in terms of flexibility, cost, throughput, power consumption, and energy efficiency.

Data collected in Fig. 1 provide an overview of state-of-the-art hardware platforms suitable for AI accelerators in terms of computational speed, power consumption, and energy efficiency in TOPs/W (Tera Operations per Second per Watt). CPUs have higher cache sizes and higher on-chip bandwidth than GPUs and reconfigurable architectures but with limited capability to process large amounts of data in parallel. Consequently, CPU-based platforms are quite inefficient compared to their GPU counterparts. In particular, GPUs are extremely efficient in terms of computational speed, as they can use thousands of parallel threads to execute math and graphics tasks. Powerful GPUs represent costly solutions typically preferred for supercomputers and data centers for heavier demanding tasks, such as training complex machine learning models built on large datasets. In contrast, FPGAs are well suited for edge AI applications to accelerate specific inference tasks on resource-constrained devices that favor energy efficiency over processing speeds. ASIC designs require long design times and high design effort, but they provide good performance and energy efficiency. A good trade-off between speed, power consumption, and design effort could be offered by CGRAs, as they exhibit near-ASIC energy efficiency with near-FPGA reconfigurability levels.

Several innovative memory architectures and technologies are emerging to design more efficient hardware accelerators. For example, Fig. 1 also includes data on NPUs combined with near-memory and In-Memory Computing devices based either on analog memory technologies, like resistive RAM (RRAM) and phase change memory (PCM), or on conventional static RAMs (SRAMs). Furthermore, digital IMC represents an effective path toward the next generation of hardware accelerators for data-intensive DNN tasks on the edge.

Designing efficient AI accelerators and heterogeneous architectures requires careful consideration across the hardware and software design phases. Even tailoring accelerators to specific algorithms and computational models, such as DNNs, presents significant challenges due to the extensive design space available to designers. This space encompasses crucial architectural choices, including the number of processing units, memory hierarchy, buffer sizes, and interconnection networks. Beyond hardware architecture design, effective dataflow management, scheduling, and mapping are critical to optimize performance. A coherent link between the algorithmic model and the design constraints — such as the target performance, resource utilization, and energy efficiency —is essential for a successful design. Introducing High-Level Synthesis (HLS) enables designers to operate at a higher level of abstraction and quickly evaluate alternative accelerator designs to meet the hardware-specific constraints. Finally, approximate computing emerged as a powerful methodology for designing efficient AI accelerators limiting power consumption and resource utilization. Such an efficient approach guarantees adequate computational complexity as well as a good trade-off between speed, energy efficiency, and cost.

III. Toolchain for Design Space Exploration and High-Level Synthesis for AI Accelerators

One of the main goals of the ICSC Flagship 2 project consists of developing a Design Space Exploration (DSE) and High-Level Synthesis (HLS) toolchain to enable designers to generate efficient reconfigurable accelerators for AI with minimal manual effort. In particular, the proposed toolchain will allow designers to explore automatically the wide space of the architectural parameters, adopt optimization strategies at a high level of abstraction through performance and resource estimations, and subsequently translate the desired design configuration into an efficient FPGA accelerator by the HLS phase.

Two HLS tools have been evaluated: the commercial tool Vitis HLS from AMD/Xilinx and the open-source tool Bambu [3]. Both tools support a set of optimization directives and standard accelerator interfaces; however, Bambu has some additional features that can result in a significant advantage when targeting AI applications. Bambu does not only support inputs written as C/C++ specifications, but also compiler intermediate representations (IRs) generated from AI frameworks [4], allowing a seamless integration between the design and training of the algorithm and its synthesis. Moreover, Bambu can target FPGAs from vendors other than AMD/Xilinx, and even ASICs through integration with the OpenROAD framework. Finally, having complete visibility of the HLS flow by using an open-source tool allows finer control of the optimization techniques applied during the process and opens up a wide range of possibilities for research into novel HLS design methodologies.

One such novel research developed within the ICSC Flagship 2 project is SPARTA [5], a methodology for the automated Synthesis of PARallel multi-Threaded Accelerators. SPARTA is integrated within Bambu, and it is triggered when the input

design contains OpenMP directives to parallelize part of the application. In this specialized HLS flow, parallel regions are first translated into calls to OpenMP runtime primitives by the front-end Clang compiler, and then implemented through corresponding low-level hardware components in the synthesis backend. Accelerators generated with SPARTA are based on a custom architecture that can exploit spatial parallelism and hide the latency of external memory accesses through context switching. Moreover, SPARTA includes a custom Network-on-Chip connecting multiple external memory channels to each accelerator, memory-side caching, and on-chip private memories for each accelerator. SPARTA has primarily been tested on graph processing kernels, to demonstrate its ability to generate efficient accelerators for irregular applications, suggesting that Graph Neural Networks could benefit from the acceleration of those kernels. However, SPARTA can be applied successfully more in general for AI applications, since many high-level design frameworks for AI provide the possibility to compile the trained model into an OpenMP application.

IV. In-Memory Computing Architectures

In-memory computing (IMC) is an emerging computing paradigm where data processing is largely executed within the memory array, thus minimizing the data movement and the associated latency and energy consumption [6]. IMC is particularly efficient for data-intensive workloads, such as training and inference of AI models. Both volatile memories, such as static random access memories (SRAMs), and emerging nonvolatile memories (NVMs), such as phase change memories (PCMs) and resistive switching memories (RRAMs), have been proposed as computational memory devices supporting IMC [7]. Recently, SRAM-based digital IMC (DIMC) has been proposed with outstanding energy-efficient characteristics [2], [8].

Emerging NVMs (such as the RRAMs and the PCMs) have been recently explored for integration in stand-alone accelerators of deep neural networks (DNNs). NVMs offer the advantage of nonvolatile storage of the computational coefficients, *e.g.*, the weights of the DNNs, and the small area of the individual cell, which is generally in the range of 25 F^2, where F is the lithographic feature of the technology node, for typical one-transistor/one-resistor (1T1R) structure of the memory device [7]. The small area of NVMs allows for a significant cost/density benefit compared to the SRAM technology, characterized by a large-area, low-density structure consisting of six or 8 transistors for a single-bit cell. In addition, multilevel cell (MLC) operation is possible in both PCM and RRAM where the device resistance can be tuned as an analog memory with a virtually continuous distribution of weights [9]. This characteristic enables efficient matrix-vector multiplication (MVM) when RRAM and PCM are arranged in crossbar array structures by leveraging physical laws such as Ohm's law for voltage-conductance multiplication and Kirchhoff's current law (KCL) for summation of memory currents in the same bitline/wordline. The ICSC Flagship 2 project focuses on the development of RRAM-based and PCM-based IMC accelerators that address fundamental design challenges at various levels, including device, circuit, and architecture levels. Nonetheless, SRAM-based DIMC concepts are explored at the circuit and architectural levels.

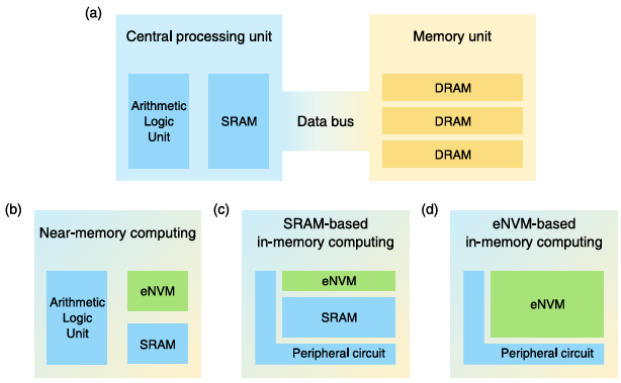


Fig. 2. Processor-memory architectures: (a) Von Neumann architecture, (b) Near-memory computing (c) SRAM-based in-memory computing, and (d) eNVM-based in-memory computing. Reprinted with permission from [7] under Creative Commons License (CC BY 4.0).

On the *device* side, both PCM and RRAM devices are characterized by non-ideal behavior in terms of variability, drift, and noise issues which severely limit the device performance. In the ICSC Flagship 2 project, we developed high-precision program-and-verify algorithms [10] to counter these non-ideal device effects, while avoiding imprecise mapping of coefficients and consequent degradation of the DNN accuracy.

On the *circuit* side, one of the key bottlenecks of NVM IMC-based accelerators is the hybrid analog/digital computation, where the analog computation in the memory enables the maximum level of parallelism. In contrast, digital computation in conventional CMOS designs is needed to perform all other types of operations (such as non-linear activation, max-pooling, and normalization). We investigated new architectures to accelerate AI tasks efficiently by minimizing the required A/D conversions with analog accumulation and neural approximated peripheral circuits [11]. The circuit design should aim at a good tradeoff between the most relevant key performance indicators (KPIs) of AI accelerators, namely performance, energy efficiency, accuracy, and cost. Performance and energy efficiency should be optimized by maximizing the parallelism of the MVM macro via analog input/activation, MLC weights, and minimum operation current. On the other hand, accuracy should be optimized by low operating current, precise MLC states, precise A/D converters, and accurate digital compensation of inaccuracies, such as drift and temperature/voltage dependence. On the other hand, DIMC relieves all the burdens described so far but introduces new challenges such as the design of fast adder trees and multipliers and the design of energy-efficient peripheral circuitry [2].

On the *architecture* side, it is essential to develop a multicore system that can harmonize and synchronize the analog MVM operations in each memory array, the digital activation and error compensation, and the data movement between the Processing Elements. This requires a suitable design of the IMC system architecture, including a proper mapping of the DNN coefficients

```
INPUT: Low-resolution image I with size H×W, filter kernel K with size t×t
OUTPUT: High-resolution image O with size 2H×2W
Initialize up and O to zero
Copy I(i, j) to up(2i, 2j)
for i = 0 to H-1 do
    for j = 0 to W-1 do
        if I(i, j) ∈ foveal region
            for u = 0 to t-1 do
                for v = 0 to t-1 do
                    O(2i, 2j) ← O(2i, 2j) + (K(u, v) × up(2i+u, 2j+v))
                    O(2i+1, 2j) ← O(2i+1, 2j) + (K(u, v) × up(2i+1+u, 2j+v))
                    O(2i, 2j+1) ← O(2i, 2j+1) + (K(u, v) × up(2i+u, 2j+1+v))
                    O(2i+1, 2j+1) ← O(2i+1, 2j+1) + (K(u, v) ×
                                    up(2i+1+u, 2j+1+v))
        else //I(i, j) ∈ peripheral region
            for u = 0 to t-1 do
                for v = 0 to t-1 do
                    O(2i, 2j) ← O(2i, 2j) + (K(u, v) × up(2i+u, 2j+v))
                    O(2i+1,2j) ← (O(2i,2j) + O(2i+2,2j)) / 2
                    O(2i, 2j+1) ← (O(2i,2j) + O(2i,2j+2)) / 2
                    O(2i+1,2j+1) ← (O(2i,2j) + O(2i, 2j+2) +
                                    O(2i+2,2j)+ O(2i+2, 2j+2)) / 4
```

Fig. 3. Pseudo-code of the proposed HTCONV layer. Reprinted with permission from [14] under Creative Commons License (CC BY 4.0).

and operations into the various tiles of the computing system and a proper communication protocol between the multiple cores. In this context, a software compiler is essential to map the DNN layers and weights to the multiple cores to maximize the KPIs.

V. FPGA-based Accelerators for Approximate Computing

In recent years, approximate computing has gained popularity as a powerful methodology to design efficient hardware accelerators with limited power consumption and resource utilization [12], [13]. AI models can take advantage of sophisticated approximation strategies that allow the fine-tuning of the power-delay-accuracy tradeoffs. Our accelerators exploit approximate computing within critical layers typically employed in Deep Learning models, such as convolutions (CONVs), transposed convolutions (TCONVs) ([14], [15], [16], [17]), pooling, fully connected operations, and SoftMax function [18]. To get reasonable flexibility, our accelerators were designed to be integrated as IPs within heterogeneous FPGA-based hardware platforms.

Among the various approximate accelerators developed in the ICSC Flagship 2 project, we focused on the new approximate TCONV layer as one of the most common techniques used in Super Resolution (SR) CNNs to upscale low-resolution images. A TCONV layer has a computational complexity significantly higher than a traditional CONV layer and requires more complex data access policies [14]. Our approach reduces the computational complexity of TCONV layers by exploiting the concept of foveated rendering of the human visual system: it has high visual acuity in a very small region, called the *fovea*, whereas outside this area it has relatively lower visual acuity, color sensitivity, and stereo depth discrimination. Based on this consideration, we developed a hybrid computational scheme (namely, HTCONV) that performs mixed accurate and inaccurate elaborations according to the foveal region.

Fig. 3 shows the pseudo-code of the proposed HTCONV method, whereas Fig. 4 shows its hardware schematic. Tests

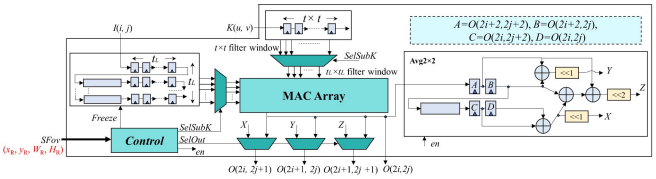


Fig. 4. Hardware architecture of the proposed HTCONV layer. Reprinted with permission from [14] under Creative Commons License (CC BY 4.0).

were performed using the pre-trained FSRCNN(25,5,1) model [19] quantized at 16-bit fixed-point and customized by including our HTCONV layer. Our approximate model was compared to the baseline FSRCNN(56,12,4), in its floating point (FP) and 16-bit quantized configurations [19], and to the 16-bit FSRCNN(25,5,1) model using the conventional TCONV layer. Our approximation strategy saves more than 80% of MACs, with a PSNR reduction lower than 10%. Table I collects some experimental results and shows the advantages offered by the new HTCONV layer over SotA solutions.

VI. Heterogeneous CPU-GPU-ASIC-FPGA platforms for AI and HPC applications

Recent advancements in technology and architecture have led to the integration of an increasing number of high-performance parallel processors and co-processors like graphics processing units (GPUs) and tensor processing units (TPUs) within HPC system nodes. This formidable computing power has accelerated the automatic training phase of AI models and their subsequent inference phases in various application scenarios. Specialized hardware accelerators such as FPGAs are essential to effectively manage the substantial computational requirements of AI algorithms while achieving better energy efficiency [20]. However, the overall performance and energy efficiency of typical AI applications, like the DNN illustrated in Fig.5, are contingent on optimizations applied across the complete software/hardware stack, as well as on the refinement of the end-to-end data flow between the data host and the accelerator. In the ICSC Flagship 2, we conducted a benchmarking campaign on a relevant DL model for medical image segmentation by using the most appropriate profiling tools for CPU, GPU, and FPGA architectures in different stages of the DL pipeline (i.e., mainly during training and inference) to extract the performance characteristics or any other suitable metric to expose the accelerators energy efficiency [21], [22]. The results are a reference point for future optimization and tradeoff analysis. After the performance bottleneck identification, we started improving the end-to-end performance in DL by addressing the I/O path with the adoption of custom solutions such as the one in [23] based on the Computational Storage paradigm and even prospecting the use of advanced memory devices such as Persistent Memory modules or low-latency SSDs. We obtained a training time reduction of up to 10% and inference throughput improvement of up to 10%.

Another application that necessitates HPC computational capabilities is the deoxyribonucleic acid (DNA) based data storage pipeline simulation. DNA is a promising approach

TABLE I
COMPARISON RESULTS TO FPGA-BASED SOTA SOLUTIONS. ADAPTED WITH PERMISSION FROM [14] UNDER CREATIVE COMMONS LICENSE (CC BY 4.0).

Method	In (Out) resolution	Bitwidth (data, weights)	Technology	Fmax (MHz)	Out Thr. (Mpixels/s)	Resources	BRAM (kB)	Power (W)	Energy eff. (Mpixels/s/W)
[15]	1440×640 (2880×1280)	(13, 13)	XC7K410T	130	495.7	171008 LUTs 161792 FFs, 1512 DSPs	922	5.38	92.13
[17]	1920×1080 (3840×2160)	(12, 12)	XC7VX485T	200	762.53	107520 LUTs 125592 FFs, 1558 DSPs	1118	NA	NA
New	1920×1080 (3840×2160)	(16, 16)	XC7K410T	222	753.04	28080 LUTs 81791 FFs, 1750 DSPs	542.25	3.7	203.5

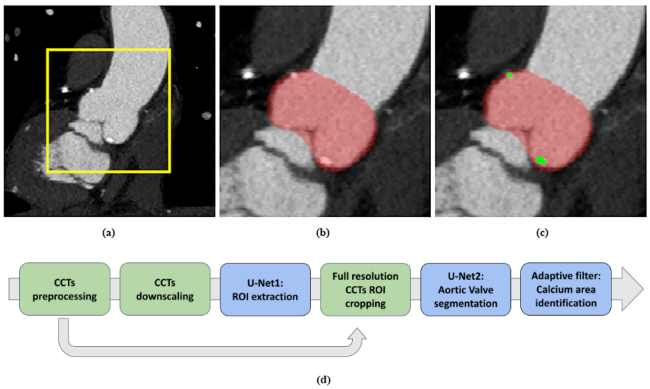


Fig. 5. The processing steps (end-to-end flow) in a typical DNN application for medical image segmentation. Reprinted with permission from [21] under Creative Commons License (CC BY 4.0).

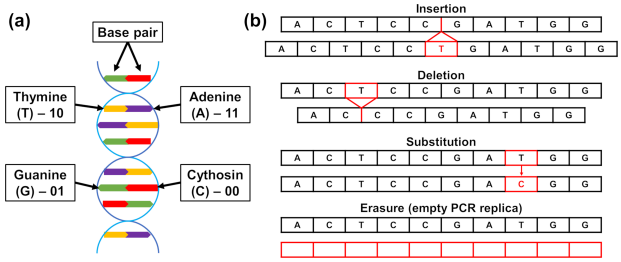


Fig. 6. (a) The double helix structure of the DNA with the base pairs evidenced along with the digital encoding of the bases. (b) Typical channel of a DNA-based data storage application. Adapted with permission from [26] under Creative Commons License (CC BY 4.0).

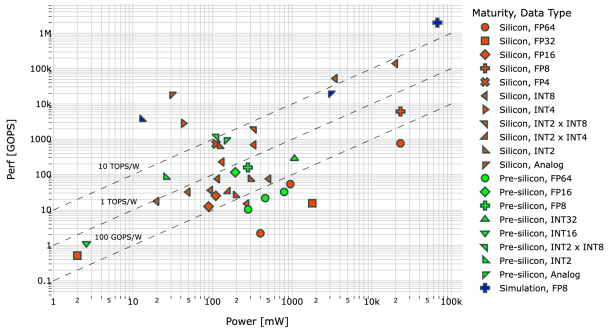


Fig. 7. RISC-V acceleration State-of-the-Art (data from [1]).

to lowering the total cost of ownership (TCO) for storage, addressing challenges in the cloud archival tier, and future AI applications [24]. This method allows encoding the digital information—composed of '1's and '0's—in a synthetic molecule made up of two polymer chains that contain a sequential arrangement of nucleotide monomers (bases) (refer to Fig. 6). Data stored in DNA can endure for thousands of years with minimal power consumption to enhance retention and achieve a density of approximately 100 PB per gram [25]. The DNA storage process encompasses several stages typically modeled by a software framework [26] designed to capture the unique aspects of encoding and decoding information. The most crucial element of the model involves the DNA channel noise characteristics and the decoding phase of the information. A distinctive feature of the DNA channel is that the input consists of numerous strings of similar lengths that share a certain degree of similarity, characterized by a specific distance. The similarity index is determined using the edit distance, also known as the Levenshtein distance [27]. Since the computations are in the context of bitwise operations without the need for floating-point or fast tensor operations, there is a surge of interest in FPGA accelerators for edit distance [28]. GPUs [29] and ASIC accelerators such as the Intel Xeon Phi [30] have provided relevant performance, although their architectures are unsuitable for energy-efficient designs. In literature, previous works demonstrated the feasibility of FPGA designs [26], [28], [31]. However, most results do not meet the requirements dictated by the fast decoding process used in DNA-based storage applications [32]. Alternative solutions are based on approximated distance techniques between strings [33], [34], although struggling in terms of edit/s figure of merit. In the ICSC Flagship 2 project, we developed a custom FPGA accelerator based on the AMD-Xilinx Alveo U50 Data Center Accelerator Card [35]. Our solution uses nearly 90% of FPGA basic-block hardware resources, achieving about 90% computing efficiency while delivering a maximum throughput of 16.8 TCUPS and an energy efficiency of 46 Mpair/Joule, enabling the use of FPGAs as a new class of accelerators for High-Performance Computing in DNA applications.

VII. ACCELERATORS BASED ON RISC-V ARCHITECTURE

AI applications are expected to drive the next generation of HPC applications, as outlined by AMD CEO Lisa Su in the Plenary Session of ISSCC'23 [36]. AI will be used as a companion to conventional HPC applications to speed up and boost their energy efficiency, for example by providing approximate but widely usable first solutions using low-bit-precision (e.g., FP16, FP8, or even FP4) to be refined by con-

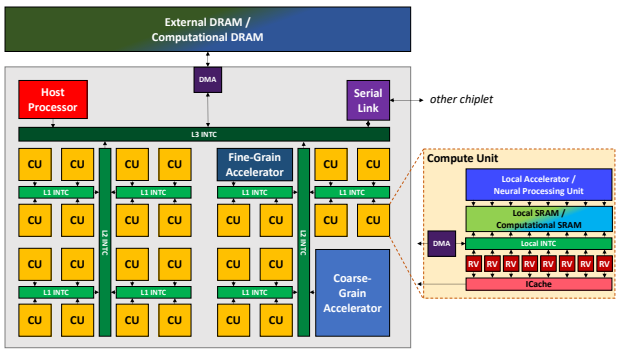
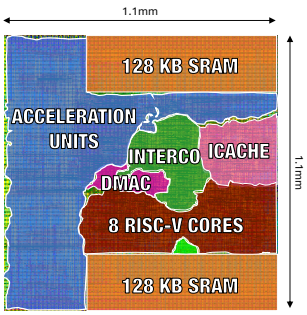


Fig. 8. *Scalable Compute Fabric* architecture template.



Technology	GlobalFoundries 12nm
Maturity	Post-layout
Area	1.21 mm^2
Frequency	460 MHz @ 0.55V
Performance (BF16)	150 GFLOPS
Efficiency (BF16)	1.5 TFLOPS/W

Fig. 9. A prototype *Compute Unit* for AI acceleration.

ventional high-accuracy algorithms employing highly accurate data representation (FP64 or FP128).

To feed these developments, novel hardware accelerator architectures are required that focus on highly energy-efficient inference and not on training, like current-generation data center GPUs [37], [38]. Most developments in this direction are undergoing in North America or East Asia [39]–[43], with the only notable exception of AxeleraAI's Metis architecture [44]. It is therefore highly desirable to increase Europe's independence and know-how in the specification, design, and fabrication of accelerator systems for this particular niche. The RISC-V open instruction set architecture (ISA) and its vast IP ecosystem, with a strong presence of European academia and industry, offer a solid starting point for this effort.

Fig. 7 shows how current RISC-V-based architectures for Deep Learning and Transformers acceleration, many of which are EU-based, are "clustered", especially in the 100mW-1W power range. The ICSC Flagship 2 project aims to extend this range of interest to architectures in the >1W range for HPC deep learning inference. Therefore, one of the target research topics is the architecture design, simulation framework, and overall validation of the system architecture of a *Scalable Compute Fabric* (SCF) exploiting the RISC-V open processor.

Fig. 8 shows the target template of the architecture of the SCF. The template includes, on a single silicon chip/chiplet, a heterogeneous acceleration system with a host/controller Linux capable processor (e.g., based on the CVA6 design) and an acceleration fabric composed of a collection of *Compute Units* (CUs) and accelerators of various granularity, connected using a scalable interconnect, such as a hierarchical AXI [45], [46] or a Network-on-Chip [47]. CUs are based on (not necessarily identical) clusters of one or more RISC-V cores oriented on computation, such as Snitch[1] or CV32E40P[2], sharing a local L1 SRAM to enable coordinated computation. Each CU can further be augmented with special purpose units, such as vector processing units tightly-coupled to the cores [48]; local neural processing units (NPUs) [49]; tensor cores [50]; digital in-memory-computing augmented SRAM [8].

Figure 9 shows a prototype *Compute Unit* developed within the ICSC Flagship 2 for the acceleration of DNN and Transformer units. The CU, laid out in GlobalFoundries 12nm technology, occupies $\sim$1.21mm^2, which is comparable to the size of a cluster in an already-fabricated precursor to the SCF architecture, Occamy [46]. Thanks to accelerators using the BFloat16 precision for all major Transformer blocks, the CU achieves up to 150 GFLOPS and 1.5 TFLOPS/W at 460 MHz, 0.55 V. The next steps of the Flagship 2 activities include using this and other similar CUs to build a scaled-up SCF.

VIII. Conclusions

This paper describes an overview of the main research challenges and related intermediate outcomes realized at the current stage of the ICSC Flagship 2 project focused on design methodologies for energy-efficient hardware accelerators for AI and HPC workloads.

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