Multi-Partner Project: Twinning for Excellence in Reliable Electronics (TWIN-RELECT)

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***Abstract*—Reliable electronics plays a major role in shaping our daily lives, being a key enabler for critical applications, such as space missions, avionics, automotive, medicine, banking, automated industry, wireless communication networks, etc. However, design of highly reliable electronic systems remains a challenge with the advances in semiconductor technology and increase in integrated circuit (IC) complexity. In this work, we introduce the Horizon Europe Twinning project TWIN-RELECT, aimed at strengthening the scientific expertise in designing reliable integrated circuits. The paper presents the general project concept and objectives, and main directions of the joint research activities. The primary scientific goal is to contribute to the development of novel, more efficient, European Electronic Design Automation (EDA) tool-chain for design of reliable chips.**

Keywords—Reliable integrated circuits, EDA tools, transient faults, permanent faults

I. Introduction

High-reliability electronic systems are essential in safety- and mission-critical applications, where any malfunction or failure may cause catastrophic consequences, such as loss of lives or unrecoverable damage. These systems must meet stringent performance and durability standards to ensure continuous, fault-free operation under all exploitation conditions. Typical applications of reliable electronics are in critical sectors like space, avionics, automotive systems, and banking. Reliable electronic systems are also used in radiology and radiotherapy, where precision and dependability directly impact patients' heath. Furthermore, reliable electronics is employed in high-energy physics research experiments, nuclear power plants, wireless communication networks, and automated industrial environments, where any failure could disrupt operations or lead to costly downtimes.

Modern semiconductor technologies enable to develop highly complex integrated circuits (ICs) that combine digital and analog resources with diverse functionalities. However, reliability challenges for ICs increase with every new technology generation. Many applications require reliable operation during a period of 15-30 years, and in some cases (e.g., space missions and deep-sea exploration) maintenance is difficult or impossible. Technological advancements impose the need for novel design solutions for reliable ICs. In addition, there is an increasing need for efficient Electronic Design Automation (EDA) or Computer-Aided Design (CAD) tools and methodologies for reliable electronic systems.

According to the European Chips Act [1], Europe's independence and sovereignty in advanced semiconductor technologies is the key driver for the economic development of Europe in the forthcoming decades. In that regard, there is a need for advanced design technologies to address the challenges of modeling and simulation of reliability, degradation effects and process variability. Achieving the highest possible reliability and a long lifetime for autonomous systems will be key for economic success, keeping a balance between cost and performance. To meet the needs of emerging applications, future connectivity systems need to offer extremely high capacity, extreme coverage, extremely low latency and high reliability, all at low energy and low cost. To achieve these goals, it is important to increase European competences in the design of reliable electronic systems.

The global market of reliable electronics exhibits a steady growth over the past years, and a similar trend is projected for the following decade. According to Transparency Market Research [2], the high-reliability semiconductor market was valued to USD 6.4 billion in 2021, with the projected rise to USD 10.1 billion by the end of 2031. A significant part of the reliability market is shared by radiation hardened electronics. The global radiation hardened electronics market was valued at USD 1.5 billion in 2022, and is projected to reach USD 2.1 billion by 2031. Rise in the usage of satellites in telecommuni-

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cations, broadcasting, and data communications is anticipated to increase the radiation hardened market size in the next few years. An important part of reliability electronics market are the EDA tools. The top EDA companies spend more than USD 1 billion annually on R&D cost. At the moment, US companies control over 70% of the global EDA tools market. This presents an opportunity to join forces within the European EDA community and collaborate on supporting European growth in a sector where Europe has very weak presence.

In this work, we introduce the concept of a novel tool-chain for design of reliable ICs. The proposed concept is explored in the EU-funded multi-partner project TWIN-RELECT. The rest of the paper is organized as follows. Section II introduces the scientific background and major limitations of the state-of-the-art solutions for design of reliable ICs. Section III presents the TWIN-RELECT project. The research part of the project is elaborated in Section IV.

II. Scientific Background: Design Methodologies and Tools for Reliable Integrated Circuits

With the scaling of CMOS technologies, ICs are becoming increasingly susceptible to transient and permanent faults, and that trend is not evident only for ICs used in safety- and mission-critical applications, but also for those employed in mainstream electronics. For example, "In 2020, AMD publicshed a report with evidence that, at that time, the most advanced chips were about 5.5 times less reliable than the previous generation of a similar product" [3]. Similarly, "In 2021, researchers at both Facebook and Google published studies describing computer hardware failures whose causes have not been easy to identify. The problem, they argued, was not in the software - it was somewhere in the computer hardware made by various companies" [3].

One of the most critical reliability threats for modern ICs are soft errors, also known as Single Event Upsets (SEUs). Soft errors represent bit-flips in storage elements (registers and memories). They may be caused when high-energy particles (heavy ions, protons, neutrons) strike directly storage elements, or when these particles hit a combinational circuit and cause voltage glitches, known as Single Event Transients (SETs), which may then propagate through the circuit and be captured by storage elements. Soft errors may also be caused by Electromagnetic Interference (EMI) and crosstalk. In space applications, over 80% of all radiation-induced errors in electronic systems have been related to soft errors [4]. On the other hand, permanent degradation of circuit's performance occurs due to gradual transistor aging, caused by Hot Carrier Injection (HCI) and Bias and Temperature Instability (BTI) effects, or by the radiation-induced Total Ionizing Dose (TID) effect. Due to transistor scaling and increase in electrical field strength, aging due to HCI and BTI effects has become a serious reliability concern in sub-45 nm technologies [5]. Other sources of permanent faults include manufacturing defects and electromigration. In a real application, an electronic system may be subjected to a simultaneous impact of multiple fault sources [6], and the system's response to faults depends on a wide range of design, technology, and operating parameters.

Complex ICs may incorporate a wide variety of functional units, such as general-purpose processors, digital signal processors, memory blocks, artificial intelligence (AI) accelerators,

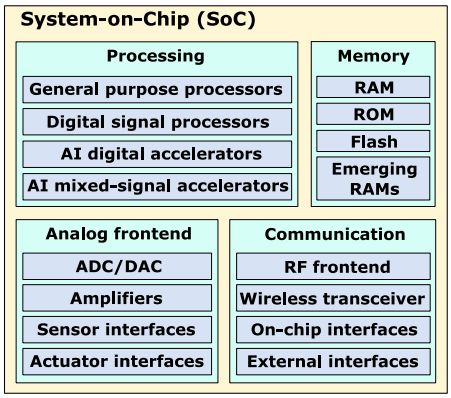

Figure 1: General architecture of an intelligent SoC

communication modules, peripheral units, *etc*. Such complex ICs are known as Systems-on-Chip (SoCs). A typical conceptual design of a SoC is illustrated in Figure 1. The fault effects in SoCs may differ significantly depending on the functional unit where they occur. Therefore, design of reliable SoCs requires a comprehensive methodology for assessment of fault mechanisms and effects across multiple levels of abstraction, *i.e.* from the device level up to the system level, applicable to different hardware architectures.

Reliability should be considered from the beginning of IC design process. Analysis of reliability effects during the design phase is performed with computer-aided simulation flows. Simulation-based analysis may be conducted at all levels of abstraction, provided accurate models of reliability effects are available. Several commercial software tools for simulation of reliability effects exist. In addition, a lot of research work on modeling and characterization of reliability effects has been done, and numerous solutions have been published. However, both commercial and research solutions have limitations.

The cross-layer methodologies for analysis of combined impact of multiple fault effects are scarce. As fault injection simulations are very time-consuming for complex designs, various analytical methods and models have been proposed to simplify and speed up the analysis process [7 - 13]. However, the reported reliability analysis flows have several critical limitations. First, most published approaches do not address the combined impact of multiple fault types. Second, there is no solution for design of large-scale reliable practical circuits, *i.e.* with sizes ranging between 500k transistors to many millions of transistors. In addition, existing solutions lack the support for both gate and interconnect delays in the aforementioned analysis. It is well-known that the impact of interconnection becomes more critical with technology scaling. Semi-custom EDA flows, commercial or open-source, use various modeling techniques to consider interconnect delays, but not from a fault propagation perspective. Last, but not least, the fourth key issue which is lacking in the state of the art, is combining the last two innovations, *i.e.* implementing a semi-custom, standard-cell and interconnect aware tool flow and methodology, which incorporates the capability to improve circuit fault tolerance, by performing both structural and physical changes, and assessing the measure of improvements.

In the past years, the use of artificial intelligence (AI)-based methods for circuit reliability analysis has been investigated

extensively. It has been demonstrated that AI models trained on datasets obtained from simulations can provide fast and very accurate predictions of aging and soft error effects in individual devices as well as in complex circuits [14 - 19]. While the AI-based reliability analysis methods have shown very promising results, they have not provided solutions for the aforementioned limitations of the state-of-the-art approaches. Furthermore, the use of AI models requires very large datasets for training, which imposes the need to conduct exhaustive fault injection simulations on a large set of test designs.

Although several commercial tools for reliability assessment exist, their functionality is limited. The Incisive Functional Safety Simulator (IFSS) of Cadence Inc. [20] supports transient and permanent fault analysis, but does not consider real physical mechanisms and cannot take into account key parameters such as supply voltage or temperature. The SoCFIT tool of IROC Inc. [21] does provide detailed analysis including physical effects, but it is applicable only for radiation-induced soft errors. There exists currently no commercial tool or reported research result which supports both reliability analysis and design for reliability. In addition, there is a lack of EDA tools for analysis of the reliability of AI-based systems, which have gained increased popularity in the last years.

III. TWIN-RELECT Project: General Concept

TWIN-RELECT is the Horizon Europe Twinning project, running from October 2024 to September 2027. The main goal of Twinning projects is to increase the scientific and innovation capacities of a Widening partner (a research institution from a developing European country) through collaboration with at least two advanced partners, where the Widening partner serves as the project coordinator. The TWIN-RELECT project coordinator is the University of Thessaly from Greece, and the advanced partners are IHP from Germany, CNRS from France, University of Montpellier from France (affiliated to CNRS), and University of Manchester from the UK.

The main topic of the project is *Design of Reliable Electronic Systems*. The project methodology combines the knowledge and best practices of the advanced partners IHP, CNRS, University of Montpellier and University of Manchester to enhance the scientific and research management capacities of the University of Thessaly. To this end, the overall methodology is based on five pillars: (i) a joint exploratory research project, (ii) enhancement of scientific capacity, (iii) enhancement of research management and administration capacity, (iv) enhancement of networking capacity, and (v) establishment of a framework for sustainable and long-term collaboration. Each pillar consists of a set of actions that will be implemented in the form of a dedicated work package. The work plan is organized into seven work packages (WPs), as illustrated in Figure 2. Five WPs (WP1 - WP5) address the five pillars of the proposed methodology. WP6 deals with dissemination, exploitation and communication, while WP7 is related to project management.

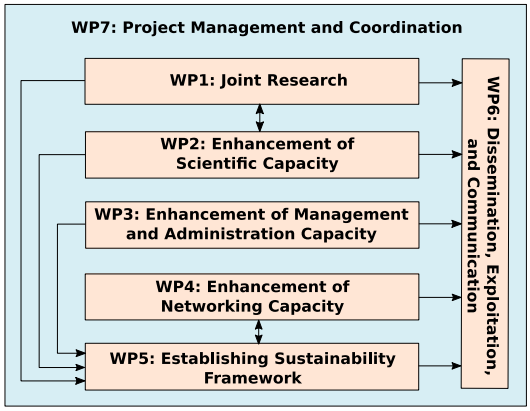

Figure 2: Relation between TWIN-RELECT WPs

The scientific strategy will address the limitations of the state-of-the-art presented in Section II through three topics relevant for the design of reliable ICs: (i) reliability analysis and modeling, (ii) design techniques for reliable systems, and (iii) reliability testing and qualification. The scientific strategy is illustrated in Figure 3. In each topic we will address all relevant aspects from technology level up to system level. Advanced partners will contribute to all three main topics by providing complementary know-how. The expertise of advanced partners will significantly widen the competences of the University of Thessaly in multiple aspects related to reliable electronics, thus establishing the foundation for transforming the University of Thessaly into a Center of Excellence for Reliable Electronic Systems.

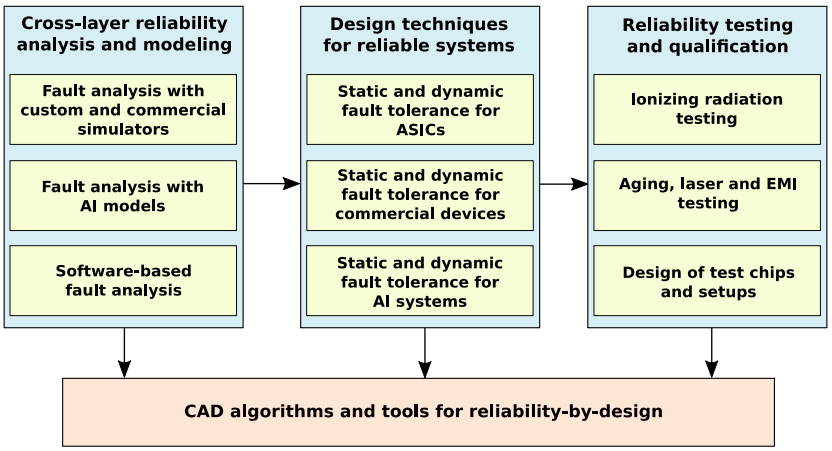

Figure 3: TWIN-RELECT scientific concept

IV. Joint Research: Towards a Comprehensive Tool-Flow for Design of Reliable Integrated Circuits

Given the limitations of the current state-of-the-art, market status and European strategic policies outlined in the previous sections, there is an urgent need for accurate reliability models and EDA tools capable for time-efficient analysis and complex reliable electronic systems design. In that regard, a significant goal of the TWIN-RELECT project is to perform joint research towards a new cross-layer flow for efficient analysis and design of reliable integrated circuits. The joint research aims to exploit the strong expertise of the University of Thessaly in the field of EDA algorithms, tools and methodologies, and the proven expertise of advanced partners in design of reliable electronic systems.

Figure 4 illustrates the concept of the proposed tool-flow for the simulation of reliability effects in integrated circuits and the design of reliable integrated circuits. The proposed tool-flow is based on an EDA timing engine operating on the principles of Static Timing Analysis (STA), developed by the University of Thessaly. Recent joint publication of University of Thessaly and IHP has demonstrated the runtime benefits of STA-based SET analysis [22]. In addition, the University of Thessaly has already developed several technologies to support the design of reliable circuits and systems by applying placement-aware algorithms. However, the current STA-based analysis approach explored at the University of Thessaly lacks support for realistic physical models of transient and permanent faults. In addition, it currently does not support the iterative circuit reliability optimization. Thus, in this research project, the University of Thessaly will collaborate with advanced partners to enhance the capabilities of the STA-based flow. Advanced partners will assist in modeling of fault effects and characterization of fault tolerance techniques, as well as in definition of reliability evaluation metrics, all of which will serve as key inputs for the STA-based tool flow.

The research project will be supported by the partners' ongoing projects related to the proposed research topic. Our research methodology will be based on the combination of cross-layer simulation of fault effects, from device up to system level, and experimental analysis with radiation tests. The methodology is aimed at studying a wide range of technologies, both those above 100 nm, which are still very relevant for some applications like space or automotive, as well as advanced scaled technologies. The research will be composed of six main tasks whose outcomes will constitute the basis of the tool-flow illustrated in Figure 4:

a) Definition of specifications for the tool, and selection of test designs and technologies,
b) Characterization of fault mechanisms in devices, circuits and systems, and definition of fault models for different processes and different types of logic structures,
c) Analysis of fault-tolerance techniques and definition of metrics for evaluation of the fault tolerance,
d) Establishment of STA-based simulation engine for joint analysis of transient and permanent faults,
e) Establishment of STA-based optimization engine for reliability improvement through iterative application of fault tolerance techniques,
f) Integration of all techniques into a single tool-flow and testing of the tool with selected benchmark circuits.

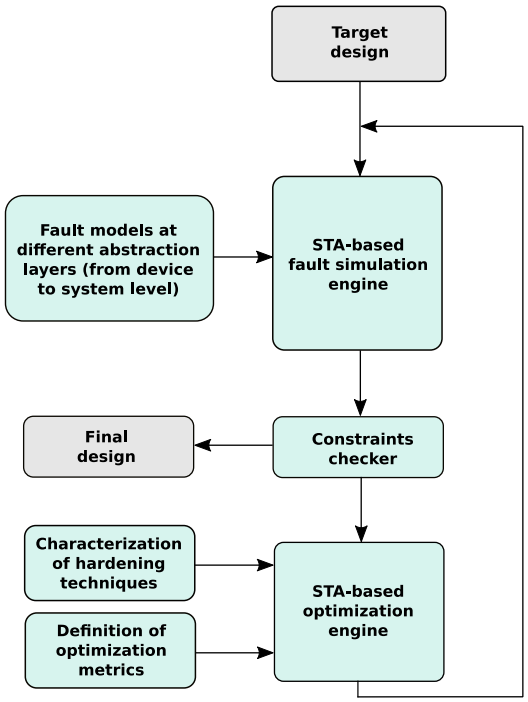

Figure 4: TWIN-RELECT tool-flow for design of reliable integrated circuits

A. Definition of Tool Specifications and Selection of Test Designs and Technologies

As a first step, general specifications for the tool-flow and a set of benchmark circuits for tool validation will be defined. The specifications will include the definition of input and output data for the EDA tool and the format for this data. In general, input parameters will include (i) a circuit specification in device, transistor, netlist (VHDL/Verilog) level, or even Verilog RTL level, (ii) circuit operating conditions (input logic vectors or state probability, supply voltage, temperature, *etc.*), and (iii) a set of fault models and reliability scenarios extracted from simulations and reliability experiments. The tool-flow outputs will include: (i) assessment of the robustness of the test circuit, (ii) identification of the most sensitive logic elements in the test circuit, (iii) radiation-hardened variant of the test circuit obtained by modifying the circuit with appropriate hardware redundancy techniques. Analysis metrics will be obtained considering different radiation scenarios.

For testing the tool-flow, a set of benchmark circuits of various complexities will be selected. We aim to use the circuits from real designs. The following types of test circuits will be considered: (i) AI-based hardware units, such as deep learning accelerators and spiking neural network accelerators, (ii) processing architectures, *e.g.* based on RISC-V, including multi-core processing platforms, (iii) custom microcontroller for space applications, (iv) wireless communication modules such as baseband processors.

The test designs will be implemented in various technologies, with the aim to assess also the impact technology on the overall fault-tolerance. In that regard, as baseline technologies we will use IHP's 130 and 250 nm technologies, whereby the Process Design Kit (PDK) for 130 nm technology is available as open source PDK [23]. In addition, we will analyze scaled technologies below 30 nm.

B. Characterization and Modeling of Fault Effects Across Multiple Abstraction Layers

A major prerequisite for accurate fault tolerance analysis is to have accurate fault models. To this end, we aim to develop accurate fault models considering different technology nodes. This task will be divided into three sub-tasks.

Characterization and modeling of fault effects through device (TCAD) simulations

Since all faults originate from a single device (transistor), it is important, as a first step, to analyze the fault effects on device level. The characterization will cover SEUs, SETs and TID effects. For this purpose, we will rely on irradiation tests and custom device-level simulations with ECORCE [24]. ECORCE is a TCAD-like simulation tool developed by CNRS and the University of Montpellier.

The characterization will start with assessment of device sensitivity through simulations. The simulations will be done for individual transistors in a particular technology, as well as for standard logic cells. TCAD models for transistors and logic cells will be developed. Afterwards, irradiation test campaigns will be conducted. The experimental results will be used to improve the prediction and simulation tools with actual data in terms of sensitivity and fault mechanisms. The outputs of this task will be essential inputs for the gate- and cell-level analysis, including the information such as transient current, deposited and collected charge, critical charge, *etc*.

Characterization and modeling of fault effects through electrical simulations

The soft error and aging effects in standard cells will be studied using commercial SPICE simulator and PredicSEE tool [25] developed by CNRS and the University of Montpellier. PredicSEE is a Monte Carlo simulation tool for calculating the cross-section of standard logic cells and small circuits, for various technologies and radiation types. SPICE simulations will be used to determine the sensitivity of each gate in terms of critical charge (for SET and SEU), SET pulse width, and delay variation due to aging. As inputs for SPICE simulations, the TCAD simulation results obtained in previous task will be used. Extensive SPICE simulations will be conducted to assess the sensitivity of each gate under soft error and aging effects, as well as the combined impact of soft errors and aging, considering the impact of design and operating parameters (transistor size, temperature, supply voltage, *etc*.).

Characterization and modeling of fault effects in application-specific and custom-designed cells

Complex digital ICs may not be composed only of standard cells, but may also consist of some special-purpose or custom-designed cells. For example, such cells may be required for special-purpose hardware modules such as AI accelerators targeting the accelerated inference of both artificial and spiking neural networks. In that regard, we will assess the robustness of asynchronous arbiters for clockless networks-on-chip by means of novel methodologies and tool flows capable of consistent SET/SEU generation and propagation at different abstraction layers, especially electrical and gate-level simulations, so that the scope of the analysis can be extended from the individual arbiter components to the effects at architectural building blocks which include them.

C. Characterization of Fault-Tolerance Techniques and Definition of Evaluation Metrics

In this task, standard fault tolerance mechanisms will be characterized in terms of their sensitivity to faults and their impact on fault sensitivity reduction when applied to a given circuit. In addition, appropriate metrics for assessing the fault tolerance of a circuit will be defined.

Characterization of fault tolerance techniques

Various SET, SEU and aging mitigation techniques, both at gate and circuit levels, will be studied through electrical and logic simulations. Previous studies have shown that there is no a single technique that can provide optimal fault tolerance, but the solution is in the combination of multiple techniques. Fault mitigation techniques may differ significantly in terms of their impact on circuit fault tolerance and overall area, delay and power overhead. Therefore, the characterization of individual mitigation techniques would ease the selection of an optimal fault tolerance scheme for a given design.

Definition of reliability metrics

To identify the most fault-sensitive elements (gates or sub-circuits) of a given design, it is necessary to use appropriate evaluation metrics. A wide range of metrics already exist, such as soft error rate, cross-section, failures in time (FIT), mean time to failure (MTTF), *etc.* However, these metrics do not consider the specificity of different designs and fault types, and they do not take into consideration fault-tolerance techniques. We aim to investigate three classes of metrics: (i) metrics which define the fault sensitivity for each gate in a circuit, (ii) metrics which define the sensitivity of the whole design, and (iii) cost metrics which evaluate the effect of fault tolerance techniques (ratio between improvement in fault tolerance and overhead in terms of area, delay and power).

D. STA-based Fault Tolerance Analysis

The analysis of the fault tolerance of a target circuit will be composed of two phases: (i) analysis of fault generation effects within individual cells in the circuit, and (ii) analysis of fault propagation through the circuit.

For the analysis of fault generation, three approaches will be considered: (i) storage of simulation data in look-up tables, (ii) derivation of analytical models from simulation data, and (iii) use of simulation data to train AI-based models for fault generation prediction. We will assess the benefits and limitations of each approach.

For the analysis of fault propagation, the existing STA simulation engine from the University of Thessaly will be extended in order to enable the simulation of both transient (SET and SEU) faults and permanent (aging) faults. STA is an industry-adopted alternative to SPICE simulation, allowing for a fast reliability analysis with acceptable loss of accuracy. The existing tool is capable of supporting Very Large-Scale Integration (VLSI) circuits, and it follows EDA industry standards, supporting file formats like Library Exchange Format (LEF), Liberty Format (LIB), Gate-level Netlist, Design Exchange Format (DEF) and more. The algorithms for both probabilistic vectorless and a targeted vector-based fault sensitivity analysis will be developed. The first step will be to extend the tool for SET analysis, by considering both the SET

generation phase and the SET propagation phase. Afterwards, the tool will be updated to support the analysis of SEU and aging affects. For SET and SEU analysis, realistic radiation profiles will be employed.

E. STA-based Design Optimization

Based on the performed fault analysis with the STA simulation engine, the design may be optimized to increase its robustness to transient and permanent faults, while considering the circuit performance, power and area constraints. The STA-based optimization algorithm will be applied to modify the design netlist by inserting appropriate fault tolerance mechanisms. Based on the analysis of different fault tolerance techniques, a set of the most suitable techniques will be integrated into the SET optimization flow. The optimization algorithm will insert the fault tolerance solutions in the design and compute the change in circuit's sensitivity to faults. If the required fault tolerance is not achieved, the optimization will be performed until the required threshold is reached.

F. Flow Integration and Validation

The final phase will be to integrate the developed models and analysis flows into a comprehensive EDA tool chain for reliable electronics design, and to test the flow on selected benchmark circuits. For integrating all solutions, we will develop custom scripts, which will allow automating the entire analysis and optimization process. All benchmark designs will be evaluated based on defined metrics. The performance will be assessed in terms of the analysis runtime, and the result of analysis will be compared with experimental results obtained from other projects where the target circuits have been used. We will also compare the runtime of the developed EDA tool with the commercial tools, such as IFSS tool.

V. Conclusion

In this paper, the EU-funded Horizon Europe Twinning project TWIN-RELECT is presented. The key aim of TWIN-RELECT is to advance the scientific know-how in relation to design of reliable integrated circuits, and particularly the EDA tools for design of reliable integrated circuits. The paper introduces main scientific topics be explored in the project, and presents the general concept of the joint research.

Besides enhancing the know-how of the coordinating institution and advanced partners, the project also aims to enhance the overall capacity of EU in chip design, based on the strategy set out in the European Chips Act. To this end, a version of developed tool with limited functionalities may be released for free use for academic purposes.

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