Cool3D: Cost-Optimized and Efficient Liquid Cooling for 3D Integrated Circuits

Jing Li[1,3], Bingrui Zhang[1], Yuquan Sun[1], Wei Xing[4] and Yuanqing Cheng[2,3]
[1]School of Mathematical Sciences, Beihang University, Beijing, China 100083
[2]School of Integrated Circuit Science and Engineering, Beihang University, Beijing, China 100191
[3]Shenzhen Institute of Beihang University, Shenzhen, China 518000
[4]School of Mathematical and Physical Sciences, University of Sheffield, S3 7RH, UK
{sy2309109@buaa.edu.cn, yuanqing@buaa.edu.cn}

***Abstract*—CMOS scaling faces challenges due to lithography and device physics issues, leading to increased costs and difficulties in expanding chip footprint. 3D integration technology offers increased integration density without increasing footprint, but elevated power density makes heat dissipation a significant challenge. Microchannel cooling effectively removes heat inside 3D chips. Traditional microchannel optimizations typically focus only on minimizing pump power within a limited parameter design space, leading to suboptimal cooling efficiency. Moreover, existing research rarely considers manufacturing costs, limiting practical application. To address these issues, we propose a high-dimensional non-uniform microchannel design scheme based on Segmented Sampling Bayesian Optimization (SSBO). This multi-parameter collaborative optimization framework comprehensively optimizes microchannel design. Our method reduces pump power by 70% compared to limited parameter design spaces. Additionally, we introduce a cost model for microchannel design, formulating a multi-objective optimization problem that considers both manufacturing cost and pump power consumption. By solving the multi-objective optimization problem by searching for the Pareto front, we demonstrate a balanced design between microchannel manufacturing cost and pump power and provide guidelines for key design parameters.**

***Index Terms*—Power Optimization, Cost Model, Microchannel Cooling, Bayesian Optimization**

I. Introduction

With the prevalence of AI computing and big data processing, high-performance processors demand escalating integration density and memory bandwidth. 3D-IC is a promising integration technology that supports die stacking with disparate process technologies through Through-Silicon Vias (TSVs). It offers significant advantages over 2D counterparts, including smaller footprint, lower interconnect power, and higher performance [1]. However, die stacking results in high power density and severe thermal issues. Traditional air cooling by heatsinks is no longer sufficient to meet the thermal budgets of 3D-ICs. An effective strategy is to integrate microchannels within 3D-ICs, utilizing liquid flow to efficiently remove heat generated inside [2].

Microchannels are typically parallel straight channels with rectangular or circular cross-sections, etched in each die layer and evenly distributed across the chip. The small channel diameter demands high pump power, leading to significant energy consumption and potential leakage issues from pressure drops, affecting chip reliability. Thus, optimizing microchannel design is crucial to improving cooling efficiency, reducing pump power, and enhancing system reliability.

Microchannel cooling has been extensively studied as a solution to thermal management in 3D-ICs. Previous studies focused on microchannel optimizing design parameters such as channel width, depth, and coolant flow rate [3], [4], but these works often use uniformly distributed microchannels across the entire chip, without considering TSV restrictions or potential over-cooling in some areas. Advancements in design methodologies led to more sophisticated approaches such as microchannels with various cross-sectional shapes and structures [5], [6]; Oevelen *et al.* [7] applied topology optimization to microchannel design, allowing for more complex geometries; Chen *et al.* [8] proposed tree-shaped microchannel networks, significantly reducing pump power. However, current etching technology limitations and manufacturing costs restrict their applications.

Regarding optimal liquid cooling efficiency by tuning microchannel dimension, Shi *et al.* recently proposed a non-uniform microchannel design [9], [10] using a heuristic for microchannel placement(HMP) to determine placement while optimizing width and pressure drop to reduce pumping power. However, their algorithm requires predetermined potential microchannel locations, potentially limiting the optimization design space. Furthermore, microchannel dimensions, layout, and fluid flow rate are closely related and should be considered together to approach the global optimum, which was not addressed in their work.

In recent years, machine learning approaches have shown promise in addressing complex optimization problems in circuit design and physical layout. Among these, Bayesian optimization (BO) has emerged as a particularly effective technique for solving black-box function optimization problems. BO is especially

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useful in scenarios where analytical solutions are impossible or computationally prohibitive, making it well-suited for the microchannel design optimization problem.

However, standard BO approaches may still struggle with the high-dimensionality and multi-scale nature of the microchannel design problem. To address these challenges, we propose a novel Segmented Sampling Bayesian Optimization (SSBO) framework for non-uniform microchannel design. Our approach incorporates both manufacturing cost and pumping power into a comprehensive cost model, allowing for more realistic and practical optimization of microchannel designs in 3D-ICs. The main contributions of this paper are as follows:

- We introduce a microchannel cost model that simultaneously considers manufacturing costs and pump power, enabling a more holistic approach to microchannel design optimization.
- We develop a multi-parameter collaborative SSBO framework tailored for high-dimensional design spaces. This framework employs an anisotropic kernel to handle parameters with different scales and utilizes a segmented optimization strategy to efficiently tackle multi-scale problems in complex, high-dimensional parameter spaces.
- We generate Pareto front curves for pump power and microchannel cost by varying the proportional parameter (PP). For our test cases, we identify recommended PP intervals within specific slope ranges, providing practical guidance for designers.
- We implement a segmented uniform method for microchannel placement that comprehensively considers design parameters including width, height, liquid flow rate, and spacing of uniformly segmented placement. Our method can also account for TSV obstacles during microchannel placement.

The rest of this paper is organized as follows: Section II provides background on Bayesian optimization and formulates the multi-objective optimization problem. Section III details our proposed cost modeling approach and presents the SSBO framework. Section IV discusses our experimental results and analysis. Finally, Section V concludes the paper and suggests directions for future work.

II. Preliminaries and Problem Formulation

A. Bayesian Optimization

Bayesian Optimization (BO) is a powerful technique for optimizing black-box functions, particularly when evaluations are expensive or time-consuming [11]. BO's strength lies in its ability to make efficient use of limited function evaluations by building a probabilistic model of the objective function. The core components of BO are: (1) A surrogate model, typically a Gaussian Process (GP), which approximates the objective function and quantifies uncertainty. and (2) An acquisition function that guides the selection of the next evaluation point by balancing exploration of uncertain regions with exploitation of promising areas. The BO process iteratively updates the surrogate model with new observations and selects the next evaluation point using the acquisition function. This approach is particularly well-suited for microchannel design optimization, where each evaluation may involve computationally expensive thermal simulations.

B. Problem Formulation

To address the non-uniform heat distribution in 3D-ICs, we propose a flexible microchannel placement strategy. This approach allows for denser microchannel placement in hotspot areas while maintaining adequate cooling in less thermally stressed regions. Our placement strategy divides the chip into m sections along the x-axis, based on the power density distribution. Within each section, microchannels are placed uniformly, but the spacing between channels can vary across sections. This is defined by the microchannel spacing parameters $l_1, ..., l_m$ for each section. Formally, given a chip of length L, we define: $N_i = \lfloor \frac{L_i}{l_i} \rfloor$ as the number of microchannels in section i; and $N(l_1, ..., l_m) = \sum_{i=1}^{m} N_i$ as the total number of microchannels.

To account for TSVs, we implement a post-processing step that removes any microchannels conflicting with TSV locations. This ensures our design is compatible with the 3D-IC structure while maintaining cooling performance.

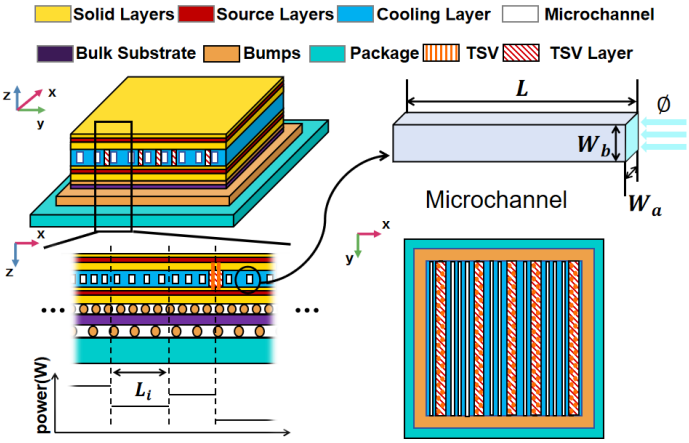

Figure 1: 3D-IC structure and microchannel layout

Our optimization problem aims to find the optimal microchannel design that balances cooling performance, pump power consumption, and manufacturing costs. We formulate this as a multi-objective optimization problem:

$$\begin{aligned} \text{argmin}_{\mathbf{x}\in X} \; & f(\mathbf{x}) = \lambda P(\mathbf{x}) + (1-\lambda) cost_{channel}(\mathbf{x}) \\ \text{subject to:} \quad & l_{min} < l_i < l_{max}, \quad i = 1, ..., m \\ & w_{amin} < w_a < w_{amax} \\ & w_{bmin} < w_b < w_{bmax} \\ & \phi_{min} < \phi < \phi_{max} \\ & T_{max} < T^*_{max} \\ & a_j \notin Range_{TSV}, \quad j = 1, ..., N \end{aligned} \tag{1}$$

where $\mathbf{x}$ represents the vector $[l_1, ..., l_m, \phi, w_a, w_b]$,and $X = [l_{min}, l_{max}] \times ... \times [w_{amin}, w_{amax}] \times [w_{bmin}, w_{bmax}] \times [\phi_{min}, \phi_{max}]$ represents the design space for the microchannel spacing l, width w_a, depth w_b, and liquid flow rate ϕ, T_{max} represents the peak temperature of the chip, which is

used to measure the cooling effect of the microchannel, and $T_{max}*$ represents the corresponding temperature limit. a_j is the location of each microchannel, which is a function of $l_1, ..., l_m$, $a_j = a_j(l_1, ..., l_m)$. Considering that the proportion of pumping power and manufacturing cost in the cost function varies in different scenarios, designers can adjust λ based on their application scenarios, where λ is the weight between pump power and manufacturing cost, and $\lambda \in (0, 1]$. Since P and $cost_{channel}$ have different dimensions, the variables in Eq. (1) have already been made dimensionless as discussed in the following section.

III. Proposed Methodologies

To achieve a comprehensive optimization of microchannel design, we develop a cost model that incorporates both operational costs (pump power consumption) and manufacturing costs. This holistic approach allows for more realistic and practical designs that balance performance with economic considerations.

A. Pumping Power Modeling

The pump power is a critical factor in the operational cost of microchannel cooling systems. It represents the power required to circulate coolant through the microchannels at a rate sufficient to maintain the chip temperature below the specified limit. For a system with N identical microchannels, the total pump power P can be expressed as:

$$P = N\phi\Delta p, \tag{2}$$

where ϕ is the volumetric flow rate in each microchannel and Δp is the pressure drop across the microchannel length. Assuming fully developed laminar flow, the pressure drop can be modeled as:

$$\Delta p = \frac{2r\mu Lv}{D_h^2}, \tag{3}$$

where r is a shape factor related to the aspect ratio of the microchannel, μ is the dynamic viscosity of the coolant, L is the length of the microchannel, v is the coolant velocity, and D_h is the hydraulic diameter of the microchannel. The volumetric flow rate ϕ is related to the velocity by:

$$\phi = \frac{v}{w_a w_b}, \tag{4}$$

where w_a and w_b are the width and depth of the microchannel, respectively. Combining these equations, we can express the pump power as:

$$P = \frac{2Nr\mu L\phi^2 w_a w_b}{D_h^2}. \tag{5}$$

This formulation shows the pump power depends on the number of microchannels, their dimensions, and the flow rate. These parameters are key variables in our optimization process.

B. Manufacturing Cost Modeling

We attempt to incorporate manufacturing cost as an optimization objective into the model. We assume that all microchannels are manufactured using the most mature and commercialized Deep Reactive Ion Etching (DRIE) technology process [12], with the cost primarily including the material cost $cost_{material}$ and the technology cost $cost_{technology}$. Additionally, the manufacturing cost of the microchannels is influenced by the yield $Y_{channel}$ of the microchannels [13]. We propose a cost model that considers both material and fabrication technology factors:

$$cost_{channel} = \frac{cost_{material} + cost_{technology}}{Y_{channel}} \tag{6}$$

$$= \frac{\alpha_1 N w_a w_b L + \alpha_2 \frac{1}{w_a} + \alpha_3 w_b}{(e^{-\beta \frac{w_b}{w_a}})^N} \tag{7}$$

where α_1, α_2, and α_3 are proportional parameters, representing the proportion of each part in the manufacturing cost, with $\alpha_1 + \alpha_2 + \alpha_3 = 1$. N, w_a, w_b, and L represent the number, width, depth, and length of the microchannels, respectively.β is the coefficient related to yield.

Material Cost: The material cost $cost_{material}$ refers to the cost of the Sulfur hexafluoride and Carbon tetrafluoride materials required for microchannel etching, which is related to the volume of the microchannels:

$$cost_{material} = \alpha_1 N w_a w_b L \tag{8}$$

The amount of chemical material used is proportional to the volume of the channel. The larger the volume, the more time it takes to etch the microchannel and the manufacturing cost is higher.

Technology Cost: The technology cost $cost_{technology}$ primarily refers to the cost associated with the technical and environmental requirements of the equipment during the etching process. The microchannel manufacturing process is the TSV etching process, both of which use Deep Reactive Ion Etching (DRIE) technology in the silicon layer. This technology makes the etching cost strongly related to the dimensions of the microchannels [14]. Then, the technology cost of the microchannel cost can be written as follows:

$$cost_{technology} = \alpha_2 \frac{1}{w_a} + \alpha_3 w_b \tag{9}$$

Since the dimensions of each channel are the same, the narrower the channel width, the taller the channel depth, or the deeper the etching depth, the higher the manufacturing cost.

Microchannel Yield: The microchannel yield is derived similar to the Yield of dies [15], and $Y_{channel}$ can be expressed as:

$$Y_{channel} = (e^{-\beta \frac{w_b}{w_a}})^N \tag{10}$$

Eq. (10) indicates that as the number of microchannels increases, or the depth of the microchannels increases, or the channel width narrows, the yield of the microchannels decreases.

Due to the different dimensions of the various components of the cost, we apply the min-max normalization method to

normalize the three parts Nw_aw_bL, $\frac{1}{w_a}$, and w_b in Eq. (7). The normalization formula is as follows:

$$b_i = \frac{a_i - \min\limits_{1\le j\le n}\{a_j\}}{\max\limits_{1\le j\le n}\{a_j\} - \min\limits_{1\le j\le n}\{a_j\}} \tag{11}$$

where we can transform the dimensional physical quantities $[a_1, ..., a_n]$ into dimensionless physical quantities $[b_1, ..., b_n]$, with $b_i \in [0, 1]$.

C. Optimization Framework for Microchannel Design

To address the challenges of high-dimensional optimization in microchannel design, we propose a novel Segmented Sampling Bayesian Optimization (SSBO) framework. This approach combines the efficiency of Bayesian optimization with a segmented sampling strategy tailored to the specific characteristics of the microchannel design problem.

SSBO (Algorithm1) uses a single surrogate model GP and multiple sampling spaces during the optimization process. Before the algorithm iteration begins, the search space X is divided into M smaller spaces $\{S_i\}_{i=1}^{M}$ based on prior knowledge and power traces. Initialize the GP model using the initial dataset $D = \{(\mathbf{x_i}, y_i)\}_{i=1}^{N_0}$ with N_0 prior points, and the current optimum $(\mathbf{x_0^*}, y_0^*)$ is identified. Each $\mathbf{x_i} \in X$ is a vector comprising multiple parameters, including l_i, w_{ai}, w_{bi}, ϕ_i, and the placement position.

Algorithm 1: Segmented Sampling BO

1: **Input:**The initial dataset $D = \{(\mathbf{x_i}, y_i)\}_{i=1}^{N}$, where $\mathbf{x_i} \in X$ denotes microchannel design parameters, and $y_i = f(\mathbf{x_i})$ as per Eq. (1)
2: **Output:** The best point $(\mathbf{x}^*, y^*)$ in dataset D
3: Divide search space X into $\{S_i\}_{i=1}^{M}$,where $S_i \subseteq X$
4: Select the best point $(\mathbf{x_0^*}, y_0^*)$ as per Eq. (13)
5: // SSBO(Segmented Sampling BO) model
6: **while** not converged or max iterations not reached **do**
7: Retrain the GP model as a surrogate model
8: Select n new points $\{\mathbf{x_i^*}\}_{i=1}^{n}$ from $\{S_i\}_{i=1}^{M}$ using the acquisition function PI
9: Evaluate $\{T(\mathbf{x_i^*})\}_{i=1}^{n}$ using thermal simulation software
10: Evaluate new sample points $\{(\mathbf{x_i^*}, y_i^*)\}_{i=1}^{n}$ using Eq. (1)
11: **if** $T(\mathbf{x_i^*}) < T_{max}$ **then**
12: Update dataset $D = D \cup \{(\mathbf{x_i^*}, y_i^*)\}_{i=1}^{n'}$
13: Update newest optimum $(\mathbf{x_{i+1}^*}, y_{i+1}^*)$ from P
14: **end if**
15: **end while**
16: **return** The best point $(\mathbf{x}^*, y^*)$

We use the Probability of Improvement (PI) as our acquisition function. For sampling, we aim to maximize $\Phi(\frac{\mu(\mathbf{x})-(-y^*)-\epsilon}{\sigma(\mathbf{x})})$, where Φ is the cumulative distribution function of the standard normal distribution, y^* is the current best observed value, $\mu(\mathbf{x})$ and $\sigma(\mathbf{x})$ are the mean and standard deviation predictions from the GP model, and ϵ is a parameter that balances exploration and exploitation. This framework allows us to efficiently navigate the complex, high-dimensional design space of microchannel cooling systems, considering both performance and cost factors.

During each iteration of the algorithm, the trained GP model from the previous iteration is used as a surrogate model to approximate the objective function, and the acquisition function PI is applied for independent sampling in the spaces $\{S_i\}_{i=1}^{M}$. The new sample points $\{(\mathbf{x_i^*}, y_i^*)\}_{i=1}^{n}$ are evaluated using the thermal simulator, e.g., COMSOL, to calculate the chip temperature. When all constraints are satisfied, the new sampling points $\{(\mathbf{x_i^*}, y_i^*)\}_{i=1}^{n'}$ are added to D, and the new optimum $(\mathbf{x_{i+1}^*}, y_{i+1}^*)$ is selected. To accelerate convergence, in practice, $n = 15$ optimal points are selected at once using the acquisition function PI to determine the new $(\mathbf{x_{i+1}^*}, y_{i+1}^*)$ in each round. After the iteration converges or the maximum number of iterations is reached, the final selected $(\mathbf{x}^*, y^*)$ will be the optimal design.

Under the temperature constraints, the calculation process for the new design points and the best design point is shown as follows:

$$\mathbf{x} \overset{comsol}{\rightarrow} T_{max}(\mathbf{x}) \rightarrow y, \tag{12}$$

$$y^* = f(\mathbf{x}^*) = min(y_1, y_2, ..., y_n). \tag{13}$$

In Eq. (12), $T_{max}(\mathbf{x})$ represents the maximum temperature of the chip when the microchannel parameters are $\mathbf{x}$. In fact, T_{max} is a complex function of $\mathbf{x}$. y^* is the current optimal value, and $\mathbf{x}^*$ is the design parameters of microchannels corresponding to the optimal value.

IV. Experimental Results

A. Experiment Setup

Model Settings: We chose ICCAD 2015 contest benchmarks as our test cases [16], which provided 3D-IC configurations. The chip dimensions were set as $10.1mm \times 10.1mm$, with $50um \times 50um$ TSVs distributed across the chip area. In our thermal simulations, we set the inlet temperature T_{in} to $293.15K$ and imposed a maximum temperature constraint T_{max^*} of $358.15K$. Table I outlines the parameter ranges employed in our optimization process. These ranges were carefully selected based on practical manufacturing constraints and previous studies in microchannel design.

Table I: Parameter Settings in Our Thermal Simulations.

Test Case and Parameters	Values
ICCAD15 Case1 Die Power	$42W$
ICCAD15 Case2 Die Power	$148W$
Each simulation of T_{max}	$< 358.15K$
Length of Channel L	10.1 mm
Case-1 Volumetric Flow Rate ϕ	$0.2 \sim 0.6\ ml/min$
Case-2 Volumetric Flow Rate ϕ	$1.2 \sim 2\ ml/min$
Microchannel Depth w_b	$150 \sim 300\ \mu m$
Microchannel Width w_a	$70 \sim 100\ \mu m$
Substrate Thickness l	$100 \sim 500\ \mu m$

Bayesian Optimization Setup: In our SSBO implementation, we set the learning rate of the GP model as 0.03 and the number of iterations as 300 to ensure convergence. The search space X was evenly divided into two subspaces, which, combined with the original space, resulted in three distinct search regions $\{S_i\}_{i=1}^{3}$. This segmentation strategy allowed for more efficient exploration of the high-dimensional parameter space. The range of λ is set from 0.5 to 1, mainly due to design space constraints. When the value of λ is less than 0.5, all the microchannel design parameters approach their limits, and it is meaningless to reduce the value further.

Running Environment: All experiments were performed on a high-performance workstation equipped with a dual-core Intel Xeon CPU @2.40GHz, an NVIDIA A100 PCIe 40GB GPU, and 128GB of DDR-4 memory.

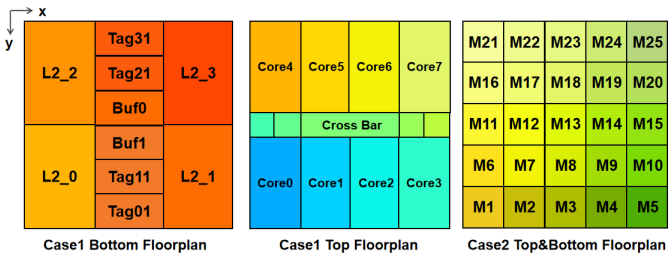

Figure 2: Floorplan of three 3D chips examined in our work

B. Comparison with the SOTA Work

To validate the effectiveness of our approach, we first compared our SSBO method with the heuristic algorithm for microchannel placement (HMP) [10], which represents the current state-of-the-art in this field. For this comparison, we focused solely on optimizing the microchannel layout to minimize pump power, setting $\lambda = 1$ in Eq. (1).

Table II: Performance of Microchannel Optimization

Case	[a]Fixed DP			Method	N	P	T_{max}
	ϕ ml/min	w_a um	w_b um			KW	K
case1	0.4	80	200	SSBO	**26**	**9.41**	355.59
				HMP [10]	**25**	**8.88**	358.09
case2	1.6	80	200	SSBO	**24**	**149.35**	357.43
				HMP	**24**	**149.93**	358.11

[a] DP is short for design parameter.

The results in Table II demonstrate that our SSBO method achieves comparable or slightly better performance than the HMP algorithm in terms of minimizing pump power. For case1, SSBO achieved a pump power of 9.41 KW compared to HMP's 8.88 KW, while maintaining a lower maximum temperature. In case2, SSBO slightly outperformed HMP with a pump power of 149.35 KW versus 149.93 KW, again with a lower maximum temperature. These results validate the effectiveness of our SSBO approach in optimizing microchannel layouts, even when considering only pump power minimization. The slight differences in performance can be attributed to the more comprehensive search capabilities of our method, which can explore a wider range of potential designs.

C. Pump Power Optimizations

Building upon the initial comparison, we expanded our optimization to include all design parameters: microchannel width, depth, liquid flow rate, and layout. This comprehensive optimization aims to minimize both pump power and manufacturing costs, as formulated in Eq. (1).

As the width and depth of the microchannels are now variables within a certain range, the potential combinations of width and depth increase significantly, causing a significant expansion of the design space. So, a greedy algorithm cannot efficiently solve this problem. Moreover, although no prior work has explored this multi-parameter optimization problem, our algorithm remains effective, capable of efficiently searching the vast high-dimensional parameter space, demonstrating its unique advantages in multi-parameter optimization problems.

Table III: Minimum Pump Power the Expanded Parameter Space

Case	[a]DP				P	T_{max}	Save%
	ϕ ml/min	w_a um	w_b um	N	KW	K	
case1	0.40	80	200	26	9.41	355.59	\
	0.29	94	200	36	4.55	354.34	51.65
	0.35	99	291	32	3.16	355.60	66.47
case2	1.60	80	200	24	149.35	357.43	\
	1.20	99	200	33	67.71	353.58	54.66
	1.27	99	284	31	43.65	356.76	70.78

[a] Parameters in gray are fixed given values, while parameters in green are adjustable variables during the optimization process.

The results in Table III demonstrate the significant improvements achieved through comprehensive optimization. For case1, when optimizing microchannel width and liquid flow rate, we reduced pump power by 51.65% compared to the baseline. Further optimization of microchannel depth yielded an additional 14.82% reduction in pump power. Similar improvements were observed for case2, with pump power reductions of 54.66% and 16.12% respectively. These results highlight the importance of considering all design parameters in microchannel optimization. The substantial reductions in pump power demonstrate the potential for significant energy savings in 3D-IC cooling systems.

D. Cost-aware Design and Pareto Front Analysis

To evaluate the impact of our cost model and the trade-offs between pump power and manufacturing costs, we conducted a series of optimizations with varying weights λ between these two objectives.

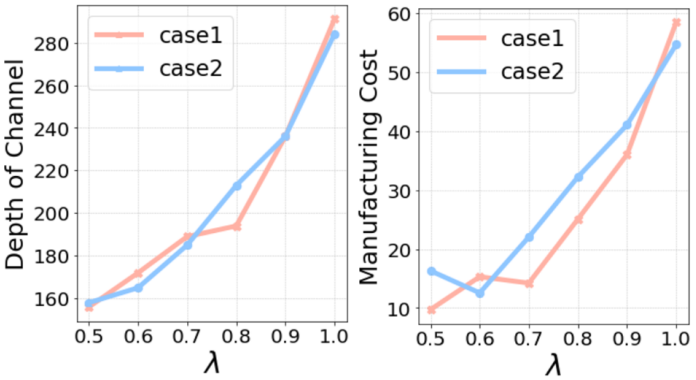

Figure 3: Design parameter variations with different values of λ: (a):variation of depth; (b):variation of manufacturing cost

When manufacturing cost is one of the minimization objectives, the optimal microchannel design trades an increase in pump power for a reduction in manufacturing cost. As shown in Table IV, when proportional parameter λ decreases, the manufacturing cost decreases and the pump power increases. In addition, the number and depth of microchannels also vary significantly after accounting for manufacturing costs. From the Table IV, when $\lambda = 0.5$, the number of microchannels is reduced from 32 to 24 for case1, from 31 to 27 for case2, the depth is reduced from 291 um to 156 um for case 1, and from 284 um to 158 um for case2. The reduction in the number and depth of microchannels helps to reduce manufacturing costs.The trend of depth and manufacturing cost shown in the Fig. 3.

Table IV: Impact of Varying Weights λ Between Pump Power and Manufacturing Cost on Microchannel Design Parameters

Case	[a]PP		DP				Objectives	
	[c]α	[b]λ	ϕ ml/min	w_a um	w_b um	N	P KW	[d]$cost$
case1	4:3:3	1.0	0.35	99	291	32	3.16	58.46
		0.9	0.37	99	236	29	4.14	36.03
		0.8	0.33	99	194	33	5.05	25.09
		0.7	0.51	99	189	19	6.67	14.23
		0.6	0.36	99	172	29	6.23	15.31
		0.5	0.47	96	156	24	11.47	9.75
case2	4:3:3	1.0	1.27	99	284	31	43.65	54.70
		0.9	1.22	94	236	31	58.11	41.07
		0.8	1.2	98	213	33	63.25	32.23
		0.7	1.2	99	185	33	76.07	22.05
		0.6	1.64	99	165	28	154.31	12.56
		0.5	1.60	90	158	27	185.91	16.31

[a] PP is short for proportional parameters.
[b] λ is the weight pump power and manufacturing cost in Eq. (1).
[c] $\alpha = \alpha_1 : \alpha_2 : \alpha_3$ in Eq. (7).
[d] $cost$ is short for the manufacturing cost $cost_{channel}$.

By adjusting the proportional parameter α_1, α_2, and α_3 in Eq. (7), the optimal design of the microchannel shows significant changes in width and depth. As shown in the Table V, when $\alpha_1 : \alpha_2 : \alpha_3 = 3 : 1 : 6$, The depth of the optimized microchannel has been notably reduced, primarily owing to the substantial proportion of depth-related technical costs in the overall manufacturing expenses. When the weight of α_1 increases to $\alpha_1 : \alpha_2 : \alpha_3 = 1 : 0 : 0$, material cost becomes the only factor that affects the manufacturing cost, and the optimization result shows that the width of the microchannel is noticeably reduced, with the number of channels correspondingly decreasing. This indicates that when the manufacturing cost of the microchannel is included in the optimization objective, different proportional factors have a significant impact on the design parameters e.g. channel width.

Pareto Front is an auxiliary curve used in multi-objective optimization, helping decision-makers to intuitively understand the trade-offs between different objectives and select the most suitable solution. Fig. 4 shows the Pareto front between $cost_{channel}$ and P in Table IV. Different colors represent the design sets under different scaling factors, and the blue triangles represent the optimal designs from Table IV. Between the two optimization objectives, the trade-off between pump power and manufacturing cost is illustrated. The closer the solution points are to the Pareto front, the nearer they are to the optimal solution under different requirements. Our optimization algorithm yields solutions that are very close to the Pareto front, indicating strong optimization performance.

Table V: Optimal Microchannel Designs under Different Proportional Parameters of Manufacturing Cost

Case	PP		DP				Objectives	
	λ	α	ϕ ml/min	w_a um	w_b um	N	P KW	$cost$
case1	0.8	4:3:3	0.33	99	194	33	5.05	25.09
		3:1:6	0.45	86	157	23	12.45	9.92
		1:0:0	0.45	76	204	23	11.68	1.37
case2	0.8	4:3:3	1.2	98	213	33	63.25	32.23
		3:1:6	1.34	97	158	30	117.27	10.7
		1:0:0	1.44	78	272	29	109.31	3.70

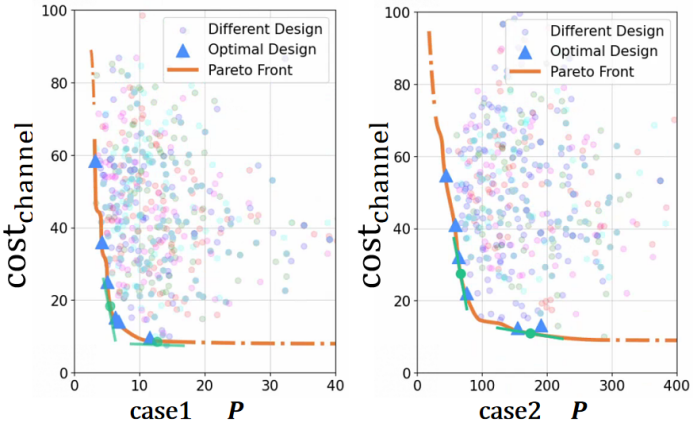

Figure 4: Pareto front analysis of pump power P and $cost_{channel}$ in Table IV

Based on the Pareto front, we recommend the optimal microchannel design in the slope range of -0.06 to -9.35 and -0.03 to -1, which not only meets the cooling requirements, but also meets the cost requirements. When the slope goes to 0, it will be accompanied by extremely high manufacturing costs, which are uneconomical in practical applications. When the slope approaches negative infinity, the pump power is too high, which may lead to unstable operation of the system. Therefore, the proportional parameters setting should be carefully configured considering both pump power and manufacturing cost.

V. Conclusion

This work introduces a novel approach to microchannel design optimization for 3D-IC cooling, addressing both thermal management and manufacturing cost challenges. Our key contributions include a comprehensive cost model, a Segmented Sampling Bayesian Optimization (SSBO) framework for efficient high-dimensional design space exploration, and significant pump power reductions of up to 70%. Through Pareto front analysis, we provide clear trade-offs between pump power and manufacturing costs, offering recommended design candidates for balanced performance and cost. This approach paves the way for more efficient and economically viable thermal management solutions in 3D integrated circuits, with potential for future exploration in dynamic power profiles and adaptive cooling strategies.

References

[1] S. Borkar, "3D integration for energy efficient system design," in *Proceedings of the 48th Design Automation Conference*, pp. 214–219, 2011.

[2] E. G. Colgan, B. Furman, M. Gaynes, W. S. Graham, N. C. LaBianca, J. H. Magerlein, R. J. Polastre, M. B. Rothwell, R. Bezama, R. Choudhary *et al,* "A practical implementation of silicon microchannel coolers for high power chips," *IEEE Transactions on Components and Packaging Technologies*, vol. 30, no. 2, pp. 218–225, 2007.

[3] D. Song, G. Dong, Y. Yao, Z. Zhu, and Y. Yang, "Optimization and analysis of microchannels under complex power distribution in 3-D ICs," *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol. 12, no. 3, pp. 537–543, 2022.

[4] H. Qian, C.-H. Chang, and H. Yu, "An efficient channel clustering and flow rate allocation algorithm for non-uniform microfluidic cooling of 3D integrated circuits," *Integration*, vol. 46, no. 1, pp. 57–68, 2013.

[5] G. Xia, D. Ma, W. Wang, and Y. Zhai, "Effects of different structures and allocations on fluid flow and heat transfer performance in 3D-IC integrated micro-channel interlayer cooling," *International Journal of Heat and Mass Transfer*, vol. 91, pp. 1167–1175, 2015.

[6] A. Chauhan, B. Sammakia, K. Ghose, G. Ahmed, and D. Agonafer, "Hot spot mitigation using single-phase microchannel cooling for microprocessors," *IEEE Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems*, pp. 1–11, 2010.

[7] T. Van Oevelen and M. Baelmans, "Numerical topology optimization of heat sinks," in *International Heat Transfer Conference Digital Library*, 2014.

[8] G. Chen, J. Kuang, Z. Zeng, H. Zhang, E. F. Young, and B. Yu, "Minimizing thermal gradient and pumping power in 3D IC liquid cooling network design," in *Proceedings of the 54th annual design automation conference 2017*, pp. 1–6, 2017.

[9] B. Shi, A. Srivastava, Ankur and P. Wang, "Non-uniform micro-channel design for stacked 3D-ICs," in *Proceedings of the 48th Design Automation Conference*, pp. 658–663, 2011.

[10] B. Shi and A. Srivastava, "Optimized micro-channel design for stacked 3-D-ICs," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 33, no. 1, pp. 90–100, 2013.

[11] P. I. Frazier, "A tutorial on Bayesian optimization," *arXiv preprint arXiv:1807.02811*, 2018.

[12] E. G. Colgan, B. Furman, M. Gaynes, W. S. Graham, N. C. LaBianca, J. H. Magerlein, R. J. Polastre, M. B. Rothwell, R. Bezama, R. Choudhary, *et al.*, "A practical implementation of silicon microchannel coolers for high power chips," *IEEE Transactions on Components and Packaging Technologies*, vol. 30, no. 2, pp. 218–225, 2007.

[13] A. Gruenewald, M. Wahl, and R. Brueck, "Cost modeling and analysis for the design, manufacturing and test of 3D-ICs," in *Proceedings of the 2015 International 3D Systems Integration Conference (3DIC)*, pp. TS8–32, 2015.

[14] J. H. Lau, "TSV manufacturing yield and hidden costs for 3D IC integration," in *Proceedings of the 2010 60th Electronic Components and Technology Conference (ECTC)*, pp. 1031–1042, 2010.

[15] C. C. Chan, Y. T. Yu, I. H. R. Jiang, "3DICE: 3D IC cost evaluation based on fast tier number estimation," in *Proceedings of the 2011 12th International Symposium on Quality Electronic Design*, pp. 1–6, 2011.

[16] A. Sridhar, M. M. Sabry, and D. Atienza, "ICCAD 2015 contest in 3D interlayer cooling optimized network," in *Proceedings of the 2015 IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, pp. 912–915, 2015.