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A 10ps-Order Flexible Resolution Time-to-Digital Converter With Linearity Calibration and Legacy FPGA

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***Abstract*—This paper presents a 10ps-order flexible resolution time-to-digital converter (TDC) consisting of only Lookup Tables and Flip-Flops that can be applied to legacy FPGAs, which is industry friendly. The proposed TDC is a Vernier delay-line based TDC. By using MUX chains as the delay adjustable buffers, it realizes flexible and high resolution 10ps-order TDC. By controlling the control values of each MUX chain independently, the nonlinearity of TDC is compensated. In the evaluation using the AMD Artix-7 FPGA, the DNL and INL were [-0.26 LSB, 0.91 LSB] and [-0.84 LSB, 2.27 LSB], respectively, at a resolution of 8.92 ps.**

Keywords—Vernier time-to-digital converter, MUX chain, linearity calibration, legacy FPGA

I. Introduction

A Time-to-Digital Converter (TDC) is a circuit that converts a time interval into a digital value. It has various applications such as Time-of-Flight (ToF) systems, light detection and imaging, position emission tomography, ultrasonic measurement, and diffuse optical tomography [1].

In recent years, in addition to the miniaturization of the manufacturing process, the implementation of TDC using FPGAs (FPGA TDC) has been widely considered due to its advantages such as reconfigurability, shorter time to market, and lower development cost.

Delay-line based FPGA TDC is well-known and widely used. Various delay-line based FPGA TDCs have been proposed so far. Most of them are tapped delay-line TDC (TDL TDC) which uses dedicated fast carry lines [2],[3]. Only high-end FPGAs with fast carry lines can realize high-resolution TDL TDCs.

This paper presents 10ps-order flexible resolution Vernier delay-line based TDC (VDL TDC) for every FPGAs composed of only Lookup Tables (LUTs) and Flip-Flops (FFs) that are common resources of all FPGAs. By using MUX chains as the delay adjustable buffers, it realizes flexible and high resolution of 10ps-order. By controlling the control values of each MUX chain independently, the nonlinearity of TDC is compensated.

II. Preliminaries

A. VDL TDC

Fig. 1 shows a typical N-stage VDL TDC [4]. The rising transitions TR_U input from the Start input of the upper delay line and TR_B input from the Stop input of the bottom delay line proceed with τ_1 and τ_2 delays, respectively. In this case, the relative delay $\Delta\tau = \tau_1 - \tau_2$ is the resolution of this TDC. The condition under which TDC works is $\Delta\tau > 0$, that is, $\tau_1 > \tau_2$. Normally, the different unit delays τ_1 and τ_2 of the upper and bottom stages are implemented by buffers.

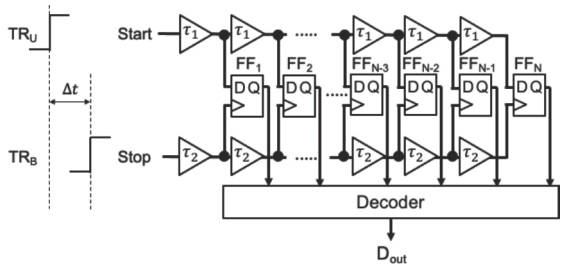

Fig. 1. N-stage VDL TDC.

B. Linearity Calibration with Histogram Method

When VDL TDC is implemented in a fine process, the buffer delays τ_1 and τ_2 of each stage vary. The variation causes nonlinearity and variation of the resolution of the TDC.

This nonlinearity can be compensated with linearity calibration by the histogram method [5]. In the histogram method, random delay intervals following a uniform distribution are continuously input to TDC. The delay intervals are sampled sequentially and a histogram is constructed from the output values. Let $\Delta\tau_i$ be τ_1 minus τ_2 of the *i*-th stage. Let bin_i be the bin length of the *i*-th stage of the constructed histogram. If $\Delta\tau_i > 0$ in all the stages, $\Delta\tau_i$ is in proportion to bin_{i-1} that is the bin length of the left-side stage. As a result, $\Delta\tau_i$ is expressed as following formula.

$$\Delta\tau_i = \frac{\Delta T}{N_{SMP}} \cdot bin_{i-1}, \quad (1)$$

where the maximum time interval is ΔT and the number of sampled time intervals is N_{SMP}.

III. Proposed TDC

A. Basic Idea

In the proposed VDL TDC, each buffer is replaced with delay adjustable buffer. We compensate for resolution and linearity by adjusting $\Delta\tau_i$ by adjusting the delay of each buffer of each stage. Fig. 2 (a) depicts the 4-stage proposed VDL TDC. The buffers MC_1 and MC_2 are delay adjustable buffers for the upper and bottom delay lines, respectively. The delay of *i*-th stage MC_1 and MC_2 are controlled by the control values S_{Ui} and S_{Bi}, respectively. Fig. 2 (b) shows the delay distribution before compensation. Each $\Delta\tau_i$ has an error with

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target resolution $\Delta\tau_t$. In the compensation, S_{Ui} and S_{Bi} are adjusted for $\Delta\tau_i$ to converge to $\Delta\tau_t$ in each stage. Each delay adjustable buffer is implemented with 2-input multiplexer chain (MUX chain: MC). Fig. 2 (a) depicts the gate-level description of MC_1 of the 4th stage. In this example, the MC_1 is implemented with the 4-stage MUX chain. As shown in this figure, wire delay of the chain is intentionally varied for the fine delay adjustment. Changing $S_1S_2S_3S_4$ = 1011, 0010, 1110 realizes delay adjustment in 50 ps steps with the 500ps order MUXs. Fig. 3 shows the architecture of the proposed N-stage TDC.

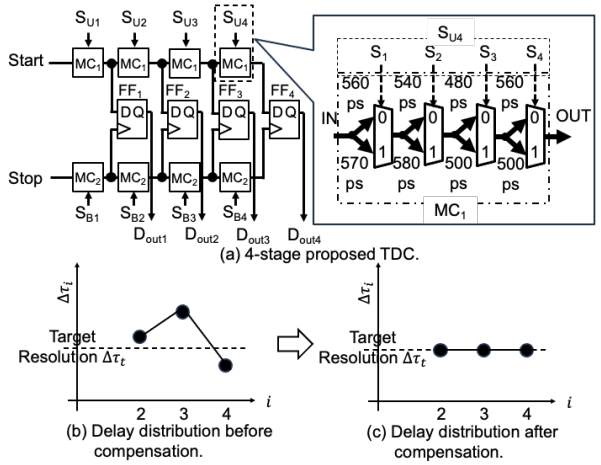

Fig. 2. Basics of proposed TDC.

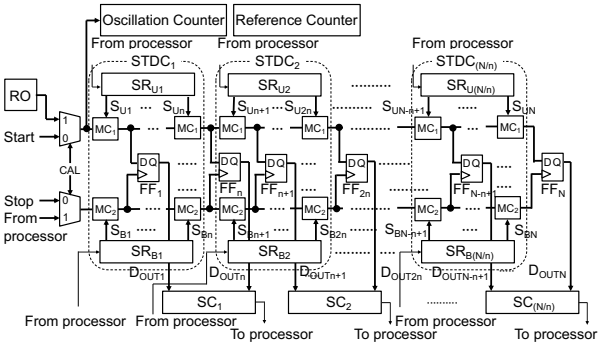

Fig. 3. Architecture of proposed TDC. SR: Shift Register, SC: Scan Chain.

B. Compensation of Resolution and Linearity

The compensation of the proposed TDC consists of two stages. In the first stage, coarse compensation is performed by adjusting the control values S_{Bi} of the bottom MUX chains, and in the second stage, fine compensation is performed by adjusting the control values S_{Ui} of the upper MUX chains.

IV. Experimental Results

The proposed TDC is implemented on AMD Artix-7 (XC7A35T) with Vitis 2023.1. In this evaluation, the number of stages of TDC is 32 and that of MC_1 and MC_2 is common 13. Fig. 4 shows the delay distributions of TDC_0 which is a proposed TDC with $\Delta\tau_t$ set to 9.43 ps and with compensation, and TDC_0' which is another TDC implemented with $\Delta\tau_t$ set to 10 ps and without compensation. Each S_{Ui} and S_{Bi} of TDC_0' is set with the delay simulation. The horizontal axis is stage i. The vertical axis is $\Delta\tau_i$. The linearity of TDC_0' is lower and its resolution is in the order of hundreds ps. On the other hand, the linearity of TDC_0 is higher and its resolution is in the order of 10 ps.

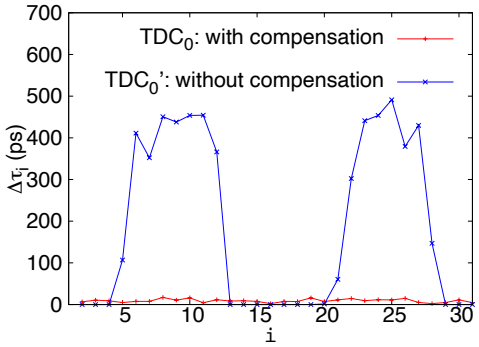

Fig. 4. Delay distribution of proposed TDCs with and without compensation.

Next, we evaluate the resolution and linearity of the proposed TDC quantitatively. In this evaluation, we use TDC_1 which is the proposed TDC implemented on another chip of the same model, too. Table 1 shows the result. The 3rd, 4th, and 5th columns are the resolution $\Delta\tau$, DNL, and INL, respectively. The absolute error of $\Delta\tau$ from $\Delta\tau_t$ of TDC_0 is less than 1 ps. That of TDC_1 is about 7 ps. DNL and INL of the proposed TDCs are in the same order of those of the conventional ones [6],[7].

TABLE I. Comparison with recent FPGA TDCs.

	$\Delta\tau_t$ (ps)	$\Delta\tau$ (ps)	DNL (LSB)	INL (LSB)
Proposed (TDC_0)	9.43	8.92	[-0.26, 0.91]	[-0.84, 2.27]
	18.86	18.57	[-0.50, 0.46]	[-0.69, 0.60]
Proposed (TDC_1)	9.29	17.30	[-0.74, 2.01]	[-1.75, 1.41]
	18.59	24.66	[-0.50, 0.64]	[0.00, 2.24]
[6]		-	10.54	[-0.95, 1.77]	[-2.54, 2.61]
[7]		-	51.28	[-0.31, 0.21]	[-0.32, 0.00]

V. Conclusion

We have presented a 10ps-order flexible fine resolution FPGA TDC consisting only of LUTs and FFs without any dedicated hardware such as carry line. Future work is the extension of the TDC measurement range.

Acknowledgement

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