A Soft Error Tolerant Flip-Flop for eFPGA Configuration Hardening in 22nm FinFET Process

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***Abstract*—We propose a soft error tolerant flip-flop (FF) design to protect configuration storage cells in standard cell-based embedded FPGA fabrics used in SoC designs. Traditional rad-hard FFs such as DICE and Triple Modular Redundant (TMR) use additional redundant storage nodes for soft error tolerance and hence incur high area overheads. Since the eFPGA configuration storage is static, the master latch of the FF is transparent and unused, except when a configuration is loaded. The proposed dual-storage-mode (DSM) FF reuses the master and slave latches as redundant storage along with a C-element for error correction. The DSM FF was fabricated on a 22nm FinFET process along with standard D-FF, pulse DICE FF, and TMR FF designs to evaluate soft error tolerance. The radiation test results show that the DSM FF can reduce the error cross section by more than three orders of magnitude (3735X) compared to the standard D-FF and two orders of magnitude (455X) compared to the pulse DICE FF with a comparable area. Furthermore, the DSM FF is 42% smaller than the TMR FF with a similar error cross section.**

***Index Terms*—Rad-hard, DICE, TMR, Dual-storage mode, FPGA**

I. Introduction

A soft error upset (SEU) is a temporary change in the state of an integrated circuit caused by energetic particles, such as protons, neutrons, or heavy ions, when they interact with the semiconductor. Circuits used in upper atmosphere and outer space applications are usually vulnerable to such SEUs (Fig 1(a)). SEUs are particularly problematic in FPGAs when they occur in configuration memory. An SEU in the configuration memory can permanently alter the circuit implemented on the FPGA fabric until the FPGA is reconfigured to fix the SEU (Fig 1(b)). Previous studies have shown that more than 86% of SEUs occur in configuration storage elements [1]. When Block RAMs are protected with ECC, configuration SEUs represent more than 95% of the SEUs in an FPGA. Therefore, it is essential to protect the configuration memory from SEUs to reduce application failure rates in an FPGA fabric.

To reduce the application failure rate on FPGA fabrics, techniques such as application-level dual modular redundancy (DMR) and triple modular redundancy (TMR) are used with configuration scrubbing to prevent failures due to SEUs in configuration memory. However, these methods incur 2-4X additional area overhead and reduced performance due to the additional logic and routing. While commercial discrete FPGAs use semi-custom layout techniques and SRAM for configuration storage, embedded FPGA (eFPGA) fabrics are built out of standard cells and use flip-flops (FF) for configuration storage.

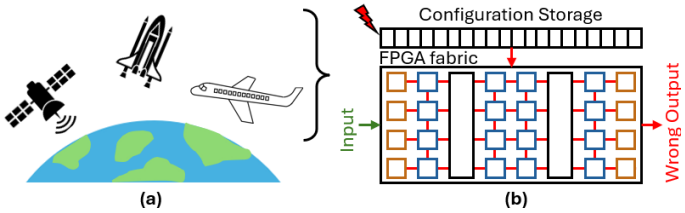

Fig. 1. (a) FPGAs are used in several space and upper atmosphere applications, which makes them prone to radiation-related upsets, (b) Configuration storage upsets account for more than 86% of SEUs in FPGAs.

Hardening of configuration FFs can significantly reduce area and delay overhead compared to costly application-level DMR or TMR-based solutions. Since configuration storage accounts for about 30% of the eFPGA area [2], an area-efficient rad-hard FF with low CS is necessary for efficient hardening of the configuration memory.

Various rad-hard FFs such as TMR, DICE [3] [4], BISER [5] and BCDMR [6] [7] have been proposed in the literature with different area, delay, and cross section (CS) trade-offs. The Master-Slave DICE FF, pulse DICE FF and TMR FF schematics are shown in Fig. 2. The master and slave latches in a Master-Slave DICE FF use additional redundant storage nodes with an interlocked structure that can correct the value when one of the storage nodes is affected by a radiation strike. However, a simultaneous upset on two storage nodes leads to an SEU in the DICE FF. Therefore, the spacing between redundant nodes in the DICE FF is crucial in determining its resilience to SEUs. To reduce the area and delay overheads introduced by redundant nodes in the DICE FF, a pulse FF structure with a single DICE latch is often used in many designs [4] [8]. TMR FF uses a majority voter in the output to prevent SEUs when one of the redundant FFs experiences an SEU. When two redundant FFs are corrupted by SEUs, the TMR FF experiences an SEU. This paper presents an alternate design approach for an SEU resilient FF that avoids adding new storage nodes, as seen in DICE and TMR FFs, by reusing the master and slave latches in a standard D-FF as redundant storage nodes.

II. Design of Dual-Storage-Mode (DSM) FF

The dual-storage-mode FF design reuses existing storage elements (master and slave latches) in a D-FF as redundant storage nodes to increase tolerance to SEUs. The schematic of a DSM FF is shown in Fig. 2 (a). In a standard D-FF, one of

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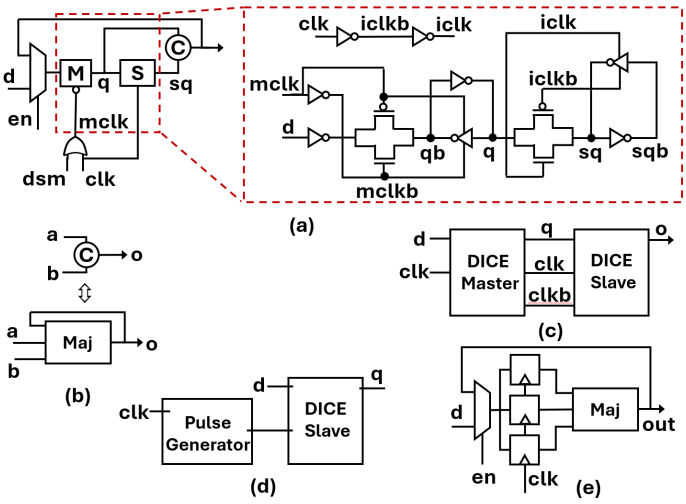

Fig. 2. Schematic of (a) DSM FF, (b) C-element, (c) Master-Slave Dice FF (d) Pulse DICE FF and (e) TMR FF. The schematic of the DSM FF is enlarged to show the master and slave latches separately with their clock signals.

the master or slave latches is always transparent. For a positive edge-triggered FF the master is transparent when CLK = 0, and the slave is transparent when CLK = 1. We introduce an additional dual-storage-mode (DSM) signal to the FF that can force the master latch from transparent mode to storage mode. Now, redundant master and slave latches can be used to increase the SEU resilience of the DSM FF by adding an error correction element before the output. A Muller C-element inserted before the output of the DSM FF can be used to correct an error in one of the storage nodes. A C-element, as shown in Fig. 2 (b), can be implemented by feeding back the output of a majority gate to one of its inputs. When one of the storage nodes experiences an upset, the feedback path helps retain the correct output value. The majority gate performs the same function as the carry cell (AB + BC + CA), and the carry cells in the std-cell library are already well-optimized for reducing delay. Therefore, using a carry cell to construct the C-element can significantly reduce its delay. When replacing the output inverter in a D-FF with a delay-optimized C element, the impact on the CLK-Q delay can be negligible.

A. Self-refresh for DSM and TMR cells

Radiation-tolerant FFs using redundant storage cells can experience an SEU due to three different scenarios. First, a multi-bit upset (MBU) can cause two redundant storage nodes to flip simultaneously (Fig. 3(a)). It is not possible to correct this error using a C-element or a majority voter, but its impact can be reduced by increasing the node spacing between the redundant storage nodes. The second scenario, shown in Fig. 3(b) is caused by an accumulation of errors in which the two storage nodes are independently flipped at two different points in time. SEUs due to error accumulation can be avoided if the first storage node experiencing an SEU is restored to the correct value using a refresh mechanism before the second storage node is upset. The third scenario, shown in Fig. 3(c), is caused due to a single event transient (SET) on the clock inverters when

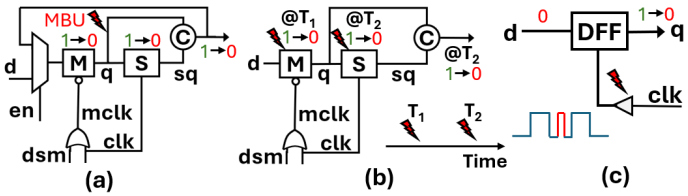

Fig. 3. Illustration of different SEU scenarios in rad-hard Flip-Flops (a) Multi-bit upset (MBU) simultaneously affecting two redundant storage nodes, (b) error accumulation on redundant storage nodes, and (c) clock SET on the clock buffers in designs without self-refresh mux.

the input data and the stored data are different. Like the error accumulation scenario, SEUs caused by clock SETs can also be mitigated with a refresh mechanism. This refresh mechanism can be performed externally using configuration scrubbing or locally at the cell level. The external configuration scrubbing is typically a slow process, as the entire configuration has to be read from an external device or memory and written into the FPGA configuration cells. Therefore, we implement a local self-refresh by adding a mux to recirculate the corrected output from the majority gate in TMR and C-element in DSM FFs and refresh the storage nodes periodically. Evaluating the cells under radiation with and without refresh can reveal the predominant upset mechanism in each cell.

B. Layout of DSM cells

To study the effect of different SEU scenarios in the DSM cell, we implemented two versions, DSM-small and DSM-large, with minimal and increased spacing between redundant storage nodes the latches. The increased storage node spacing in the DSM-large cell reduces the probability of experiencing multi-bit upsets compared to the DSM-small cell. The layout of the DSM-small cell shown in Fig. 4 (b) closely mirrors the layout of the standard D-FF that is optimized for area. The master and slave latches are placed close to each other, and the spacing between the master and slave storage nodes (q, sq) is just one poly pitch. In the layout of the DSM-large cell shown in Fig. 4 (b), the spacing between master and slave storage nodes (q, sqb) is increased from one poly pitch to eleven poly pitches by placing the clock inverters between them and inserting a tri-state buffer in place of the transmission gate. The output inverter of both DSM FFs is replaced with the C-element, as shown in Fig. 4 (c). The addition Evaluating the cells under radiation with and without refresh can reveal the predominant upset mechanism (MBU or error accumulation) in each cell.

III. Test Chip

A 4mm x 4mm test chip was fabricated on a 22nm commercial FinFET process including the DSM FF cells and other reference FFs. Fig. 6 (a) shows the packaged test die. Fig. 6 (b) shows the test chip layout with the radtest block. The block diagram of the *radtest* block containing the scan chains of different FF cells is shown in Fig. 5. Each chain comprises 8K FF cells, and there are a total of 64K cells of each FF type. The chains can be clocked by an external clock or an internal RO-based clock if high refresh rates become necessary

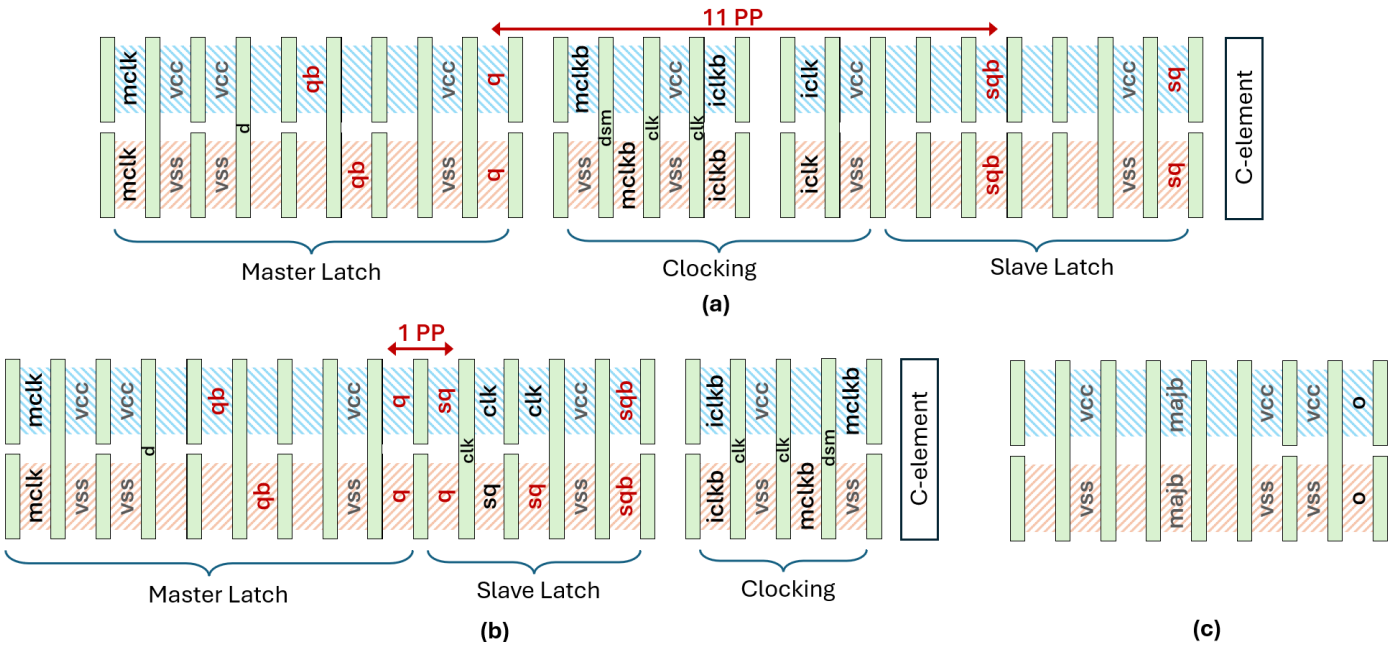

Fig. 4. (a) Layout of the DSM-large FF showing storage nodes (q, sqb) on the redundant latches spaced out by 11 poly pitches (PP). (b) layout of the DSM-small FF with one PP spacing between storage nodes of the redundant latches, and (c) layout of the static C-element constructed using the majority gate cell.

for error correction. The test block also contains a pop-count circuit to keep track of errors during the radiation test. The error count from the pop-count data can be correlated with the data read out of the chains after radiation exposure to ensure correct operation.

The DSM and DICE FFs that require custom layouts are designed as single-height cells for inclusion into the foundry-provided high-density 6-track standard cell library with five tracks available for internal routing. Although the metal-1 layer was sufficient to route the standard DFF cell, the interlocked DICE structure significantly increased the routing complexity and required the use of two thirds of the metal-2 tracks available in the cell. The DSM cells also required additional metal 2 routing but used just one third of the available metal-2 tracks. The custom FF cells were extracted and characterized using the Synopsys SiliconSmart ADV Library Characterization tool and the characterization flow provided by the foundry. The characterization flow was validated by re-characterizing standard DFF and comparing the resulting composite current source (CCS) timing library files with the default standard cell timing library provided by the foundry. We characterized the custom cells (DSM and DICE) for all PVT corners in the standard cell library and used the resulting liberty files for physical design. During placement and routing, cell spacing constraints were added to the TMR FFs to ensure a radial spacing of 0.54 µm between the three redundant copies of the TMR FF. This constraint will ensure storage node separation between the redundant FFs, one of the main causes of uncorrectable multi-bit upsets. The TMR cell spacing constraint increases the robustness of the TMR solution and can serve as a hardened

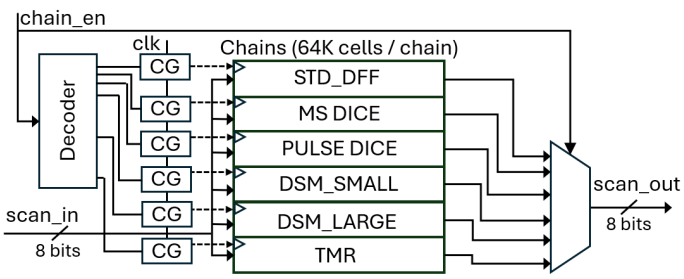

Fig. 5. A simplified block diagram of the radtest block showing the scan chains containing the FF cells used in the experiment.

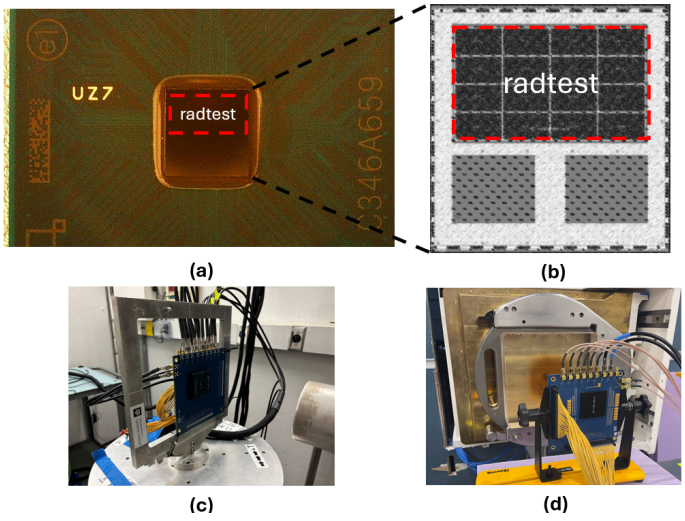

Fig. 6. (a) Packaged test chip, (b) layout of the chip showing the radtest block which has the test structures, (c) test setup for heavy-ion testing, and (d) test setup for proton beam testing.

reference design to compare the different FF designs [9].

IV. Radiation Test Results

The test die was packaged as a flip chip ball grid array (BGA) and mounted on the test PCB using a BGA socket to allow exposure of the die backside to the radiation beam. A Xilinx ZCU104 FPGA board was used to control the scan chains on the test chip. During radiation testing, a test program running on the Xilinx FPGA continuously monitors the errors accumulated in the different FF chains by reading the output of the pop-count circuit on the test chip. Proton testing was conducted using 200 MeV proton beam at the Thompson Proton Center in Knoxville, USA. We collected test data for different supply voltages and data patterns, including the static all-0/1 pattern and an alternating 01 pattern at room temperature with both refresh on and refresh off settings. The fluence of each experiment was in the range of 1 x 10^{12} to 4 x 10^{12} $protons/cm^2$, with high fluence for runs without self-refresh (no refresh) to provide more time for error accumulation.

A. Proton Test Results

The soft error cross section (CS) of the different FF cells, normalized to the CS of standard D-FF, with and without refresh for the static (All-0/1) and alternating (01) data patterns, are shown in Fig. 7. The TMR FF performed the best (>1235X CS reduction) and did not experience any upsets. The DSM large FF showed 329X CS reduction and experienced very few upsets, resulting in high error uncertainty. One notable observation is that the CS for the D-FF and DICE designs shows a significant difference between the static and alternating data patterns. The CS increases by 8X and 10X for the D-FF and DICE designs, respectively. This increase in CS with an alternating data pattern indicates that D-FF and pulse DICE FFs are susceptible to single event transient (SET) pulses on the clock inverters in the FF. When a particle strike causes a SET pulse in the internal clock nodes, the data at the input of the FF can flow through and corrupt the data stored in the slave latch. The clock SET pulses affect the pulse DICE FF more than the D-FF due to the additional strike footprint of the delay buffers used in the pulse generator. The CS of DSM and TMR FFs are not affected by the alternating data pattern and show high resilience to clock SETs due to the presence of the refresh mux that recirculates the output back to the input.

To study the effect of supply voltage dependence, we measured the cross section of FFs at multiple supply voltages with and without refresh and the results are shown in Fig. 8. The increase in error cross section of DSM FFs by (2-5X) at lower voltages with refresh indicates an increase in MBU contribution even with increased node spacing in the DSM-large cell. At 0.95V, refresh did not affect the cross section of DSM FFs, indicating that almost all errors were due to MBUs. However, the accumulation of errors might take longer due to the reduced SEU rates at higher voltages, and higher fluences are required to draw more definitive conclusions. The cross section of TMR FF remained relatively similar across voltages with and without refresh, indicating that TMR FFs are unaffected by MBUs even at lower voltages due to the physical separation of the redundant FFs enforced during physical design.

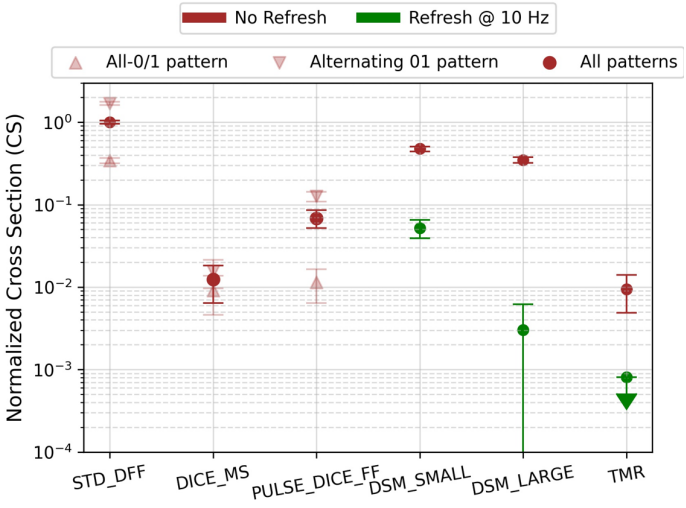

Fig. 7. Normalized Cross Section (CS) of different FF cells under 200MeV proton radiation at 0.85V. DSM-small and DSM-large cells show more than one (19x) and two orders of magnitude (329x) improvement in CS with refresh enabled @ 10 Hz.

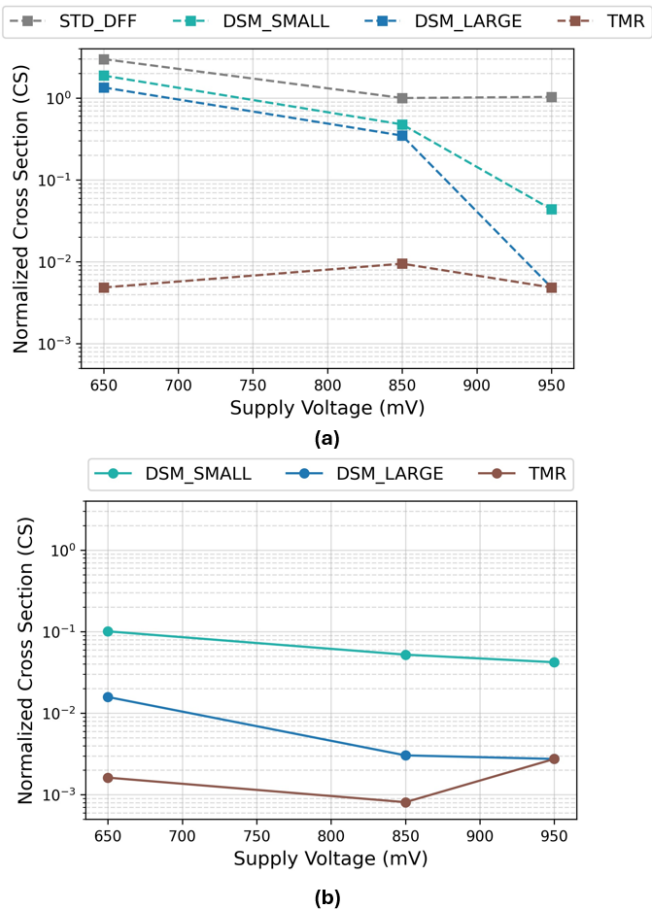

Fig. 8. Voltage dependence of soft error cross section of different FF designs (a) without refresh and (b) with refresh

TABLE I
AREA, DELAY, POWER, AND CROSS SECTION IMPROVEMENT OF VARIOUS FF DESIGNS

Cell Type	Area	Delay	Static Power	Dynamic Power	Cross section Improvement	
					Heavy Ion	Proton
STD DFF	1	1	1	1	1	1
MS DICE	2.79	1.29	1.23	1.79	340	78
PULSE DICE	2.21	1.10	1.28	3.1	8	15
DSM_SMALL	2.05	1.00	1.91	1.26	9	19
DSM_LARGE	2.26	1.26	2.03	1.55	3735	329
TMR	3.89	2.56	3.80	3.55	3237	>1235

B. *Heavy-ion Test Results*

Heavy-ion testing was performed at the Cyclotron Institute at Texas A&M University. The heavy-ion flux was 1 x 10^6 $ions/cm^2/s$ and the fluence for each experiment was in the range of 1 x 10^7 to 10^8 $ions/cm^2$ for a range of LETs from 3 to 52 $MeV-cm^2/mg$. We tested the different FF designs with and without self-refresh to differentiate between error accumulation and multi-bit upset scenarios, as discussed in II-A. Fig. 9 shows the soft error cross section for different FF designs, normalized to standard D-FF at a LET of 22 $MeV-cm^2/mg$. Both the DSM-large and physically separated TMR FF designs reduced cross section by more than 3000X when refresh was enabled. Both DSM and TMR FF designs did not show a significant reduction in cross section without refresh, as seen in Fig. 9 (b), highlighting the need to prevent error accumulation using self-refresh. Furthermore, the DSM-small design showed just 9X reduction in cross section even when refresh is enabled indicating the dominance of uncorrectable MBUs. The master-slave and pulse DICE FF, which use the same DICE latch, show 329X and 8X cross section reduction respectively indicating the pulse DICE FF was highly susceptible to clock SETs.

Turning self-refresh on and off during radiation tests can help us distinguish SEUs caused by error accumulation and multi-bit upset scenarios. Fig. 9 shows that DSM FF designs do not significantly reduce cross section when refresh is turned off (brown). But when the cells are refreshed at a frequency of 10 Hz, the cross section of the DSM-small and DSM-large FFs improved by about 6x and 1200x, respectively. The lower cross section reduction shows that the DSM-small FF, with a storage node spacing of one poly pitch, is ∼200X more susceptible to uncorrectable multi-bit upsets under heavy ion beam. We can also infer that while error accumulation contributes to most

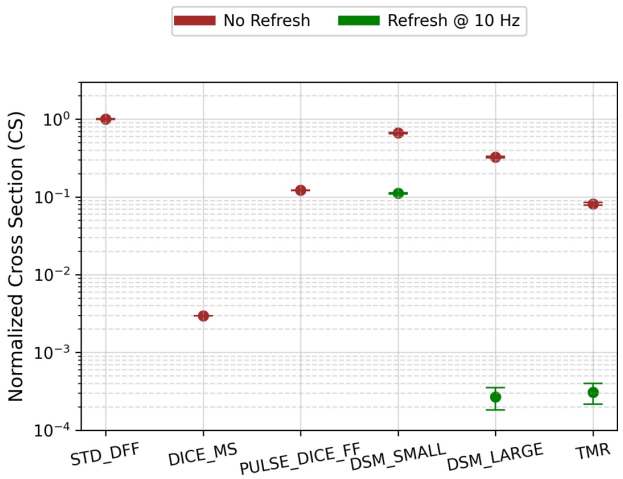

Fig. 9. Normalized error cross section of different FF cells with and without refresh under heavy-ion beam with an LET of 22 $MeV-cm^2/mg$

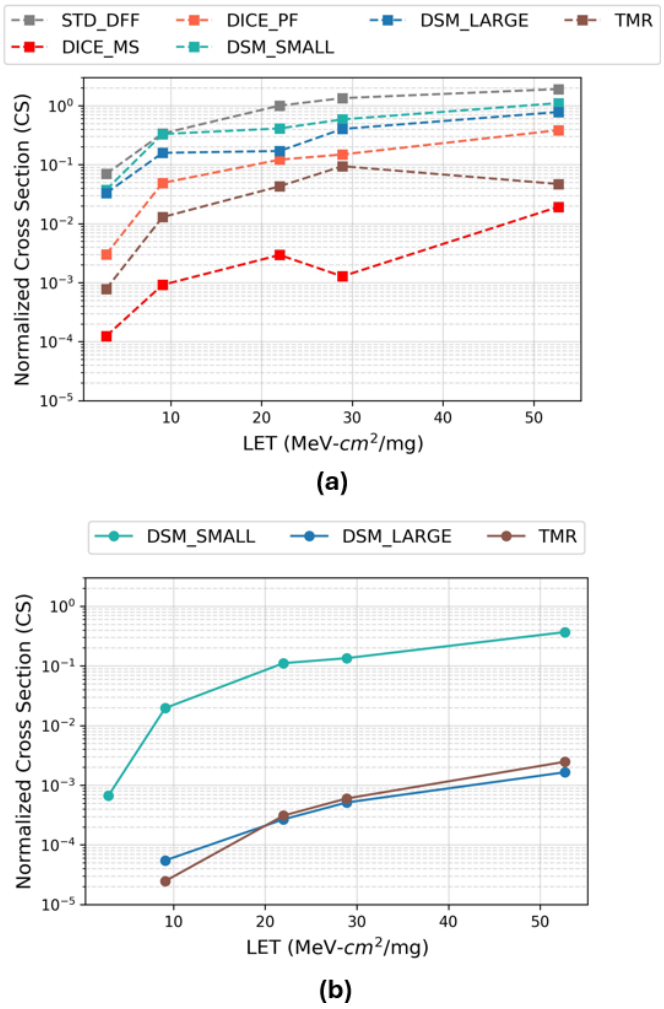

Fig. 10. Normalized heavy ion cross section at different LETs (a) without refresh and (b) with refresh.

TABLE II
COMPARISON OF DSM FF WITH RELATED WORK

	Cell Type	Technology	Patterns Tested	Area*	Delay*	CS Improvement*
IRPS '17 [7]	BCDMR	16nm	All-0	4.48	-	∼100
TNS '13 [10]	LEAP DICE	28nm	All-0/1	2.8	1.2	∼500
ISSCC '08 [8]	PULSE DICE	65nm	-	1.34	0.96	∼100
TCAS-I '21 [11]	TMR	130nm	All-0/1, 0, 1	7.9	1.8	>2000
This work	**DSM**	**22nm**	**All-0/1, 0, 1**	**2.26**	**1.26**	**∼3735**

* Results are normalized to the area, delay, and CS of standard D-FF for the respective technology node

upsets, a small but significant fraction of the errors are caused by multi-bit upsets, especially for the DSM-small FF cells. Fig. 10 (a) and (b) show the cross section of different FF designs across a range of heavy-ion LETs with and without refresh respectively. The cross section of the DSM-large FF tracks the TMR FF across different heavy-ion LETs.

Table I shows the normalized area, delay, power, and CS improvement of the different FF cells under heavy ion and proton beam tests. The DSM-small cell is found to be susceptible to MBUs and only provides modest (<19X) CS improvement compared to the standard DFF while being ∼2X larger in area. The area of the DSM-large cell, including the refresh mux is comparable to that of the pulse DICE FF but provides more than 10X cross section reduction for protons and more than 400X cross section reduction for heavy ions. Although DSM FF requires periodic refreshing, a low refresh rate of 10Hz was sufficient to provide significant CS improvements in accelerated beam testing. At low refresh rates, the additional dynamic power consumption due to refresh is negligible, as the energy required to refresh a DSM FF cell is less than 10 fJ. Moreover, the DSM signal is not timing critical and incurs minimal area and routing overheads for distribution, comparable to typical reset signals used in FF designs. Table II compares the performance of the newly proposed DSM FF with other state-of-the-art radiation-hardened FF designs. DSM large FF shows the best CS, comparable to the TMR designs, which is more than three orders of magnitude (∼3236X) lower than the standard D-FF in the same technology node. The DSM FF is also ∼42% smaller than the TMR FF, making it an excellent candidate for area-efficient configuration hardening of standard cell-based embedded FPGA fabrics.

V. CONCLUSION

An area-efficient soft error upset-tolerant dual storage mode (DSM) flip-flop was proposed to harden the configuration storage cells in FPGA fabrics. The proposed DSM FF improves area-efficiency by reusing the master and slave latches for redundant storage and a C-element for error correction. The DSM FF was fabricated on a 22nm FinFET process along with standard D-FF, Master-Slave DICE FF, pulse DICE FF, and TMR FF cells to evaluate soft error tolerance. Heavy-ion radiation tests show that DSM FF design performs similar to the highly resilient TMR design reducing cross section by >3000X compared to standard D-FF while being ∼42% smaller in area.

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REFERENCES

[1] E. Trumann, G. B. Thieu, J. Schmechel, K. Weide-Zaage, K. Schmidt, D. Hagenah, and G. Payá Vayá, "Radiation tolerant reconfigurable hardware architecture design methodology," in *International Symposium on Applied Reconfigurable Computing*. Springer, 2023, pp. 357–360.

[2] P. Mohan, O. Atli, O. O. Kibar, and K. Mai, "A top-down design methodology for synthesizing fpga fabrics using standard asic flow," in *Proceedings of the 2020 ACM/SIGDA International Symposium on Field-Programmable Gate Arrays*, ser. FPGA '20, New York, NY, USA, 2020.

[3] T. Calin, M. Nicolaidis, and R. Velazco, "Upset hardened memory design for submicron cmos technology," *IEEE Transactions on Nuclear Science*, vol. 43, no. 6, pp. 2874–2878, 1996.

[4] B. Narasimham, K. Chandrasekharan, J. K. Wang, and B. L. Bhuva, "Soft error performance of high-speed pulsed-dice-latch design in 16 nm and 7 nm finfet processes," in *2019 IEEE International Reliability Physics Symposium (IRPS)*, 2019, pp. 1–4.

[5] M. Zhang, S. Mitra, T. M. Mak, N. Seifert, N. J. Wang, Q. Shi, K. S. Kim, N. R. Shanbhag, and S. J. Patel, "Sequential element design with built-in soft error resilience," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 14, no. 12, pp. 1368–1378, 2006.

[6] J. Furuta, C. Hamanaka, K. Kobayashi, and H. Onodera, "A 65nm bistable cross-coupled dual modular redundancy flip-flop capable of protecting soft errors on the c-element," in *2010 Symposium on VLSI Circuits*, 2010.

[7] K. Kobayashi, J. Furuta, H. Maruoka, M. Hifumi, S. Kumashiro, T. Kato, and S. Kohri, "A 16 nm finfet radiation-hardened flip-flop, bistable cross-coupled dual-modular-redundancy ff for terrestrial and outer-space highly-reliable systems," in *2017 IEEE International Reliability Physics Symposium (IRPS)*, 2017, pp. SE–2.1–SE–2.3.

[8] D. Krueger, E. Francom, and J. Langsdorf, "Circuit design for voltage scaling and ser immunity on a quad-core itanium® processor," in *2008 IEEE International Solid-State Circuits Conference - Digest of Technical Papers*, 2008, pp. 94–95.

[9] V. Petrovic and M. Krstic, "Design flow for radhard tmr flip-flops," in *2015 IEEE 18th International Symposium on Design and Diagnostics of Electronic Circuits & Systems*, 2015, pp. 203–208.

[10] N. Gaspard, S. Jagannathan, Z. Diggins, M. King, S.-J. Wen, R. Wong, D. Loveless, K. Lilja, M. Bounasser, T. Reece, A. Witulski, W. Holman, B. Bhuva, and L. Massengill, "Technology scaling comparison of flip-flop heavy-ion single-event upset cross sections," *Nuclear Science, IEEE Transactions on*, vol. 60, pp. 4368–4373, 12 2013.

[11] O. Schrape, M. Andjelković, A. Breitenreiter, S. Zeidler, A. Balashov, and M. Krstic, "Design and evaluation of radiation-hardened standard cell flip-flops," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. PP, pp. 1–14, 09 2021.