Low-Latency Digital Feedback for Stochastic Quantum Calibration Using Cryogenic CMOS

Nathan Eli Miller*, Laith A. Shamieh and Saibal Mukhopadhyay
School of Electrical and Computer Engineering
Georgia Institute of Technology
Atlanta, GA, USA
*nathan.miller@gatech.edu

***Abstract*—In order to develop quantum computing systems towards practically useful applications, their physical quantum bits (qubits) must be able to operate with minimal error. Recent work has demonstrated stochastic gate calibration protocols for quantum systems which are meant to track drifting control parameters and tune gate operations to high fidelity. These protocols critically rely on low-latency feedback between the quantum system and its classical control hardware, which is impossible without on-board classical compute from FPGAs or ASICs. In this work, we analyze the performance of a single-shot stochastic calibration protocol for indefinite outcome quantum circuits under various latency conditions based on timing considerations from experimental quantum systems. We also demonstrate the benefits that can be achieved with ASIC implementation of the protocol by synthesizing the classical control logic in a 28 nm CMOS design node, with simulations extended to 14 nm FinFET and at both room and cryogenic temperatures. We show that these classes of quantum calibration protocols can be easily implemented within contemporary control system architectures for low-latency performance without significant power or resource utilization, allowing for the rapid tuning and drift control of any gate-model quantum system towards fault-tolerant computation.**

***Index Terms*—quantum control, cryogenic CMOS, quantum calibration, quantum computing**

I. Introduction

In order to implement practically useful algorithms and applications on quantum computers with provable advantage over their classical counterparts, the quantum computing systems in use today still require significant scaling in their number of qubits and reduction of their error rates (whether for single- and two-qubit gates, state-preparation or readout). One projection shows that even with surface code error correction, quantum systems with nanosecond-scale unitary gate operations and 10^{-6} error rates (a far cry from state-of-the-art quantum systems) would require weeks of operation time and millions of physical qubits to perform a quantum chemistry algorithm with advantage over classical systems [1]. To achieve these performance benchmarks, there is a rich landscape of research that is being done to reduce error rates in quantum hardware through both fabrication advancements and the calibration of noisy qubits.

The development of quantum computers from qubits requires highly complex and precise control systems to address many qubits, perform single- and multi-qubit gate operations, measure qubits and reset them to their ground state, perform error correction, and maintain coherence. In many research groups, the control systems in use rely on arbitrary waveform generators (AWGs) or other analog control systems for the control of a small number of qubits. These AWGs involve long compilation times and often require significant latency from software or human-user input if a parameter in the designed control pulse needs to be changed between quantum circuit executions. Several groups are now designing FPGA-based control systems, including the open source QubiC [2], [3] and QICK [4], [5] systems, the Sinara and ArtiQ hardware and software ecosystem [6], and more closed systems like the Octet pulse compiler [7]. These FPGA-based systems allow for reconfigurability of the control designs, customizable gate control, and fast feedback between the quantum hardware and its classical control system. To further improve performance for specific quantum hardware designs, companies such as Google and Intel are developing their own cryogenic ASICs for certain limited control functionalities [8], [9]. Placing control hardware at lower temperatures closer to the quantum hardware can aid in the reduction of both latency and signal attenuation, as compared to placing the control system at room temperature and routing its signals through the cryogenic layers to the qubits. Additionally, since there are many different types of physical qubit modalities being explored such as superconducting transmons, trapped ions, silicon spin qubits, and neutral atoms, the control hardware stacks which address these systems will each have different needs and different control parameter spaces. This results in bespoke control implementations across different quantum hardware modalities, and across academic and industry groups, as creating a generalized and hardware-agnostic control system becomes complex.

In large part, the calibration of quantum hardware has not fully taken advantage of the low-latency feedback which is enabled by advanced control systems. Many calibration protocols use a large number of circuits and measurements to characterize a quantum system, tweak parameters to address observed errors, and iterate over this process until some minimum target error rates are achieved [10]–[13]. A recent work presented stochastic calibration protocols designed to correct for gate errors by tuning control parameters without fully characterizing the system [14], seeking to take advantage of low-latency control hardware. This novel approach allows for

*Present Address: MIT Lincoln Laboratory, Lexington, MA 02421

978-3-9826741-0-0/DATE25/© 2025 EDAA

rapid calibration and tracking of drifting control parameters by relying on low-latency feedback with a classical control system to modify specific parameters of a gate control pulse between each circuit shot. Protocols such as this could significantly speed up the bring-up and maintenance of quantum devices to well-calibrated operating conditions.

In this work, we assess the on-line, low-latency classical compute requirements necessary for stochastic quantum gate calibration as in Magann et al. [14] and present FPGA and ASIC designs implementing it. This work contributes:

1) An assessment of the sources of latency present in single-shot stochastic calibration based on state-of-the-art quantum hardware.
2) A demonstration of the impacts of update latency on the fidelity of calibrated gates and their noise spectrum.
3) An FPGA-implemented design for stochastic calibration with nanosecond-scale parameter update times.
4) An ASIC synthesis of the stochastic calibration design with considerations for room temperature and cryogenic operation, demonstrating the benefits of cryogenic control for low power and high speed calibration.

With these contributions, we demonstrate the need for low-latency control hardware design and its usefulness for the rapid calibration of quantum gates. In particular, our implementation of stochastic quantum calibration in FPGA and ASIC is ready for implementation in present-day quantum systems towards the high-fidelity gate operations necessary to push quantum computing systems towards fault tolerance.

II. Background: Single-Shot Stochastic Quantum Calibration

In a single-shot calibration protocol described by Magann et al. [14], a single indefinite outcome quantum circuit is prepared, a single measurement shot is taken, and a small update is made to a given control parameter following the equation:

$$\eta_t = \eta_{t-1} + z_{t-1}\frac{k}{s} \tag{1}$$

where η_t is the value of a drifting control parameter at time t, z_{t-1} is a single measurement outcome of ± 1 (corresponding to $|0\rangle$ or $|1\rangle$), k is a tunable gain, and $s = \frac{\partial \delta\eta}{\partial \eta}$ is the sensitivity of the circuit's measurement to small changes in η. The control parameter η represents any tunable physical parameter which causes a coherent over- or under-rotation to occur in a noisy indefinite outcome circuit, such as a $G_x(\pi/2)$ gate acting on $|0\rangle$. Then, $s \propto r$ with r the number of times the circuit being calibrated is repeated to amplify the coherent error.

The hyperparameters k and r can be tuned over time following heuristic methods such as:

1) Start with a high gain value and a single $G_x(\pi/2)$ gate for each shot of the calibration.
2) Keep a measurement history FIFO of length h and calculate the autocorrelation of the measurement history as $a = \sum_{t=1}^{h-1} z_t * z_{t-1}$. Based on the result:
   a) If a is greater than an upper bound b_u, increase the gain k and reset the FIFO.
   b) Else, if a is less than a lower bound b_l, reduce the gain k and reset the FIFO.
   c) Else, if $a = 0$, increase the circuit repetitions r.
   d) Else, continue storing measurements in the FIFO up to its maximum length.

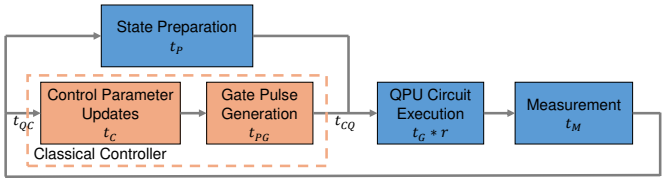

Fig. 1. Mapping the timing and feedback loop involved in our stochastic calibration protocols, including quantum (blue) and classical (orange) hardware steps and the communication latency between them.

In Magann et al. [14], the hyperparameter values used when tracking a stochastically drifting η in simulation are $h = 100$, $b_u = 30$, $b_l = -30$, and r follows the sequence $r = \{1, 5, 13, 25, 41, 61\}$ with $r = 61$ the maximum. We use the same values in this work for consistent comparison.

III. The Importance of Rapid Classical Feedback

The shot-to-shot updates the stochastic calibration algorithm requires utilize rapid feedback capabilities which are only recently becoming a realistic possibility in quantum control hardware. In each update step, the single-shot stochastic calibration algorithm encounters several sources of latency as mapped out in Fig. 1. The total time between updates, t_U, is the sum of the delays which occur when communicating from the classical system to the quantum system, t_{CQ}; performing the quantum circuit (or single gate) for r repetitions of execution time t_G; measuring the outcome, t_M; communicating these measurement results to the classical system, t_{QC}; updating our control parameters, t_C; generating gate control pulses from those parameters, t_{PG}; and preparing the initial state to be run again (typically through active or passive reset), t_P. In some initial implementations of the stochastic calibration protocol, we observe that we can parallelize the state preparation in the quantum system with the classical update steps. Thus, our total delay equation becomes:

$$t_U = t_G r + t_M + max(t_P, t_{QC} + t_C + t_{PG} + t_{CQ}) \tag{2}$$

In quantum systems which use cryogenic environments for their qubits, the delays between the quantum and classical hardware are impacted by the latency and signal attenuation involved in communicating across temperature gradients, often from a 0.15 mK temperature range for the qubits, to a 4 K range for a cryogenic control chip or out to room temperature for most FPGA-based control systems. This latency is typically on the order of 10 ns [15] depending on wire lengths. The worse scenario occurs where human users are programming AWGs between quantum circuit trials, where the rapid feedback required for the stochastic calibration algorithm is impossible.

Through a review of modern quantum technologies, we can get an estimate of how long t_U may be in certain platforms. In Table I we calculate the total quantum processing unit

TABLE I

ESTIMATES OF QUANTUM DEVICE TIME SCALES. EXAMPLES OF SINGLE-QUBIT GATE, MEASUREMENT AND RESET TIMES FROM LITERATURE PROJECT THE QPU PROCESSING TIME BETWEEN CALIBRATION STEPS.

Device Architecture	Single Qubit Gate Time	Measurement Time	Reset Time	Total QPU Time ($r = 50$ Gates)
Transmons [16]–[20]	20 ns	500 ns	500 ns	2 us
Trapped Ions [21], [22]	10 us	300 us	1 ms	1.8 ms
SiMOS [22], [23]	0.5 us	100 us	100 us	225 us

(QPU) time as $t_{QPU} = t_G r + t_M + t_P$. If we assume $t_P \geq t_{QC} + t_C + t_{PG} + t_{CQ}$, then $t_U = t_{QPU}$. Observing t_P, we see the upper timing bound that our classical systems (including communication to and from the QPU) must beat to not be the limiting factor to feedback. The quantum systems which will require the most stringent timing conditions for the classical update steps are those based on transmons, as their gate, measurement, and reset times are significantly faster than for other devices such as trapped ions. We note that some state-of-the-art systems will beat the times demonstrated in Table I, but we aim to give an estimate of QPU times on average to observe that t_{QPU} is generally on the order of micro- or milliseconds, being most dependent on measurement and reset times if r is kept small. Additionally, as the stochastic calibration protocol may be used either on boot-up of the quantum hardware or interleaved between useful circuits to maintain calibration [14], one may also consider the time spent running other circuits as a contributing factor to total latency. Detailed analysis of this is out of the scope of this work.

We simulate (using PyGSTi [24]) how these different t_U may affect the performance of the single-shot stochastic calibration algorithm, as it relies heavily on rapid feedback to respond to drifting control parameters. In Fig. 2, we introduce random walk noise at a 1 ns time scale in η and track the gate infidelity of a $G_x(\pi/2)$ gate when tuning for 10 ms at various lengths of t_U. The drift described by this model follows:

$$\eta_{opt,t} = \eta_{opt,t-1} + q\ell \tag{3}$$

where $\eta_{opt,t}$ is the optimal value of η at time t which drifts by a random walk of length $\ell = 0.0001$ every 1 ns, and q is a random choice of ± 1, as in the random walk noise model used in [14]. We calculate the gate infidelity $\mathcal{I} = 1 - f_{G_x}$, where $f_{G_x} = Tr\left(\sqrt{\sqrt{J(a)} * J(b) * \sqrt{J(a)}}\right)^2$ where $J(.)$ is the Jamiolkowski isomorphism map that maps a operation matrix to it's corresponding Choi Matrix, with a and b the noisy and target $G_x(\pi/2)$ gates [24]. We begin with $k = 0.01$ and $r = 1$ and follow the scheduling heuristic described previously, given an initial $\Delta\eta = \eta - \eta_{opt}$ condition of 0.2.

Looking at a moving average over 100000 shots to smooth out the data (where a shot is taken every nanosecond), it becomes clear that faster feedback times between calibration steps are vital for the usefulness of the stochastic calibration protocol in improving gate fidelities. Reducing the calibration update time t_U significantly improves both the convergence rate and the lower bound on the gate infidelity which can be achieved, though even with relatively slow t_U the algorithm is still able to move η closer to η_{opt} over time.

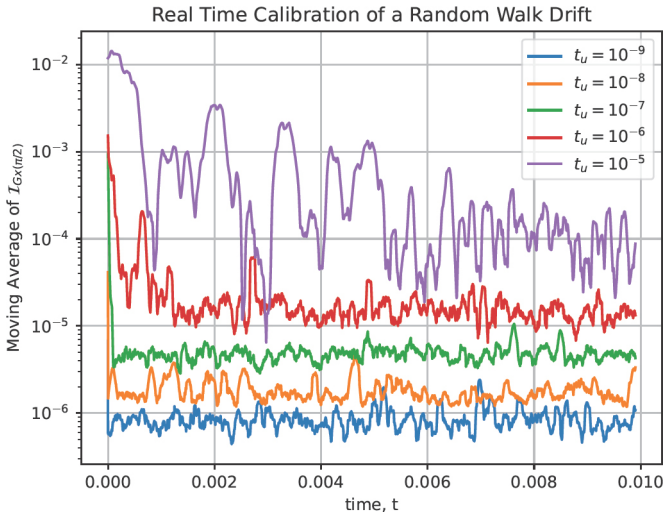

Fig. 2. Simulating the evolution of a $G_x(\pi/2)$ gate with a random walk parameter drift of magnitude 0.0001 which occurs every nanosecond. The gate is calibrated to low infidelity with a delay between updates of t_U, with a moving average over 100000 shots to smooth the curve.

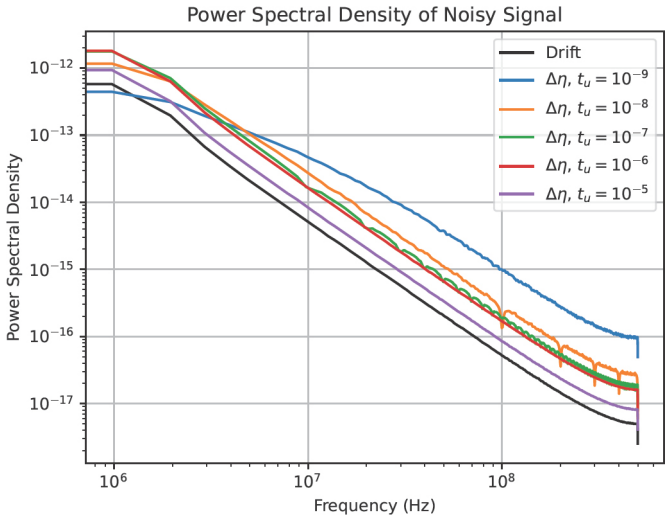

Fig. 3. Simulating the stochastic calibration protocol for a $G_x(\pi/2)$ gate with random walk drift indicates that a faster t_U helps to reduce the low frequency components of the noise in the system at the cost of some high frequency noise.

Furthermore, in Fig. 3 we observe that the calibration protocol works to reduce the low-frequency components of the noisy $\Delta\eta$. Introducing the calibration protocol adds noise across the measured frequency spectrum due to updating the parameter at each shot, but if the parameters update fast enough, the low frequency noise is reduced as η is tuned at the cost of high frequency noise. We expect to see even more stark trends with a longer-term simulation, where the noise spectrum would be reduced closer to white noise with ideal update steps.

By comparing the results of Figs. 2 and 3 with the approximate t_{QPU} shown in Table I, we can see clear motivations for reducing the operating times of quantum computing hardware

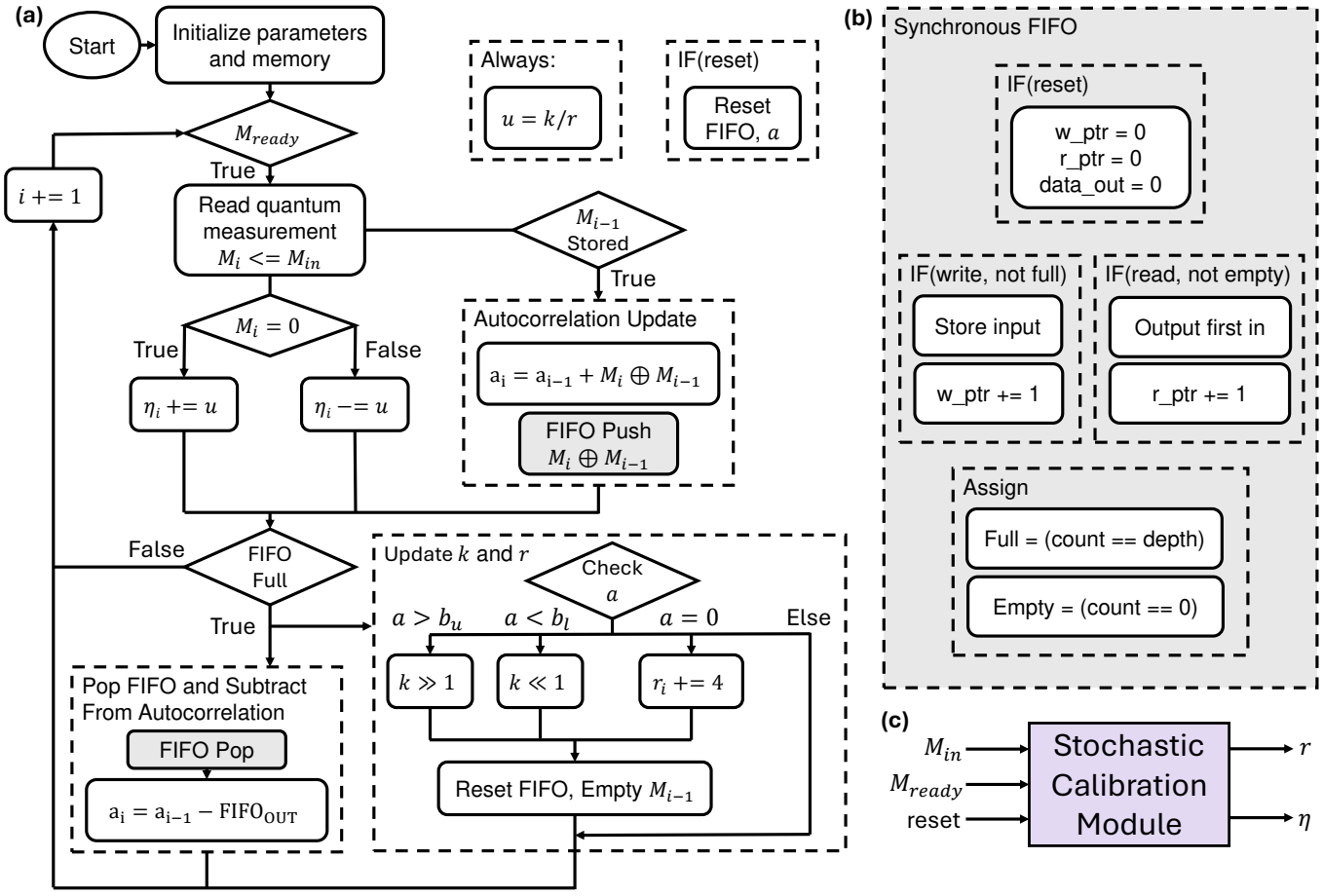

Fig. 4. Implementing the single-shot calibration algorithm in digital hardware, initially in FPGA and then synthesized in ASIC. The state machine in (a) shown as a module in (c) takes streaming inputs of single-shot measurements M_{in} and a signal M_{ready} indicating the measurement result is ready from the quantum readout system, outputting the control parameter η and the number of gate repetitions r to run on the next algorithm iteration.

to improve low-latency calibration. As shown in works like [1], improvements in the fidelities of basic unitary operations in a quantum computer can drastically reduce the physical qubit overhead required to implement advantageous quantum algorithms due to the lower error-correcting surface code distance required to create fault-tolerant logical qubits.

IV. An FPGA Implementation of the Single-Shot Calibration Protocol

As quantum gate, measurement and reset operations improve in their speed, we are also left with the question of how rapidly the classical hardware can perform the calibration updates and generate the next gate pulse in the sequence. To explore this question, we first developed an FPGA-based implementation of the stochastic calibration protocol. We take advantage of slight modifications to the hyperparameter scheduling heuristic and a signed 32-bit encoding of the parameters for simple digital logic. First, we set the k modification steps of the scheduling heuristic to increase or decrease k by multiplying or dividing by 2, allowing simple bit shift logic to modify k. Additionally, we modify our FIFO measurement history buffer to length $h = 128$ for use of binary overflow when tracking the FIFO pointers. Taking advantage of parallelization and a simple state machine, we emulate a single calibration trajectory from simulated PyGSTi gate measurement data to prove that our digital implementation of the calibration protocol performs accurately and on the time scale of only 8 clock cycles per update step. With a sufficiently fast clock, this allows us to reduce t_C to the order of a few nanoseconds, well within the time scale shown by Table I.

Figure 4 demonstrates the calibration state machine as well as the I/O structure of the stochastic calibration module. Figure 5 demonstrates the calibration outputs for an example trajectory using this algorithm, where the calibration protocol using a Python-based implementation (parameter η_t) is nearly perfectly matched by the FPGA-based implementation (parameter η_v) with only minor errors from the bit precision of the data encoding. In a realistic quantum system, this module will take inputs from a processor performing measurement discrimination, which determines whether a $|0\rangle$ or $|1\rangle$ measurement has been received. The module then outputs the number of repetitions to be run and the η value to registers in a pulse control module in order to queue the next circuit for QPU execution. This represents $t_M + t_C + t_{PG}$, and additional t_{QC} must be accounted for to include the time communicating the measurement result to classical system. A recent work [16] has demonstrated a

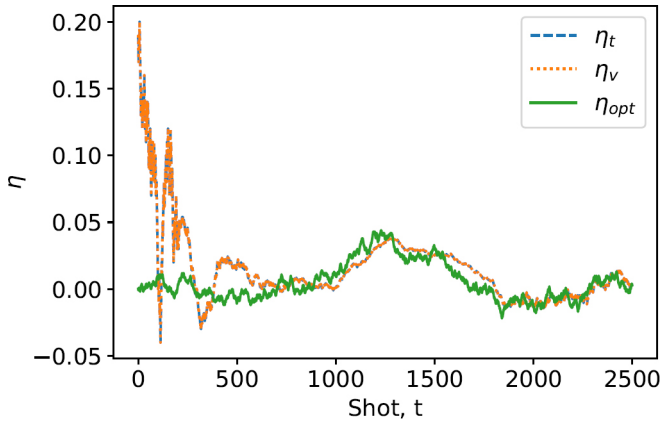

Fig. 5. Implementing the single-shot calibration protocol for a $G_x(\pi/2)$ gate with random walk drift and an initial error of $\Delta\eta = 0.2$ in Python-based software yields the tuned value of η over time, η_t, which is nearly perfectly matched by output from the Verilog-based implementation of the algorithm η_v. Both are able to closely track the drifting η_{opt}.

machine-learning enabled measurement state discriminator on FPGAs, which cites a 54 ns state discrimination time for a 500 ns measurement readout length. Other works such as Intel's Horse Ridge II quantum control processor [8] cite on-chip control pulse generation with precision down to pulse widths of 10 ns. Thus, our calibration module with time t_C in the nanosecond range would be well suited to be inserted between these cells on an FPGA or cryogenic CMOS system with the primary timing bottleneck being the QPU circuit execution and readout. Additionally, the pulse compilation unit can be a significant source of classical compute latency (t_{PG}), which is an area of active research [7].

V. Cryogenic and Room Temperature CMOS ASIC Implementations

We continue our analysis by synthesizing the design in Fig. 4 in several CMOS technology nodes. Table II provides a comparison of timing, dynamic power and leakage power across 28 nm and 14 nm process nodes under room temperature and cryogenic temperature operating conditions. We test at 77 K for our cryogenic systems and expect further performance improvements could be gained when scaling down to the 4 K temperatures of most cryogenic quantum control ASICs [8].

To achieve these results, the following steps were taken:

1) **Stochastic Calibration Module Synthesis:** The stochastic calibration module was synthesized for the TSMC 28 nm planar CMOS node using both low-voltage threshold (LVT) and standard-voltage threshold (SVT) models at room temperature (300 K). The timing, leakage, and dynamic power for these models were recorded.
2) **Scaling to 14 nm Node:** The power and timing numbers for the 14 nm node were scaled using the 28 nm SVT model numbers. Scaling was done by comparing standard cell designs, including delay, leakage, and static current, between the 28 nm and 14 nm nodes at room temperature.
3) **Cryogenic Analysis:** Scaling to cryogenic temperature was done using the scaled values from the 14 nm RT (Room Temperature) data and a comparison of a few standard cells and a ring oscillator operating at approximately 100 MHz [25]. The analysis included comparisons of the 14 nm models under different conditions: Room Temperature at 1 V, Cryogenic Temperature at 1 V, and Cryogenic Temperature at 0.6 V.

Figure 6 shows the HSpice simulations for TSMC 28 nm NMOS and PMOS, along with 14 nm nFinFET and pFinFET models at room (300 K) and cryogenic (77 K) temperatures. The current-voltage (I_{DS} vs. V_{GS}) plots show that lower temperatures decrease leakage currents (I_{OFF}) and improve ON currents (I_{ON}) for both 0.6 V and 1 V power supplies. The cryogenic FinFET models are adjusted by reducing the threshold voltage (V_{th}), lowering the gate-source voltages (V_{GS}) to reduce leakage due to Gate Induced Drain Leakage (GIDL).

Based on the timing and power performance of this algorithm, we see the ability for our stochastic calibration module to be implemented in modern control platforms. For example, the Intel Horse Ridge II chip uses power at 4 K in the mW per qubit range for qubit pulsing and readout, whereas our calibration module only requires roughly 25 μW of power even at 77 K, which would be reduced further at lower temperatures. This places our calibration protocol well within the power budget of commercial quantum control ASIC platforms and within the ability of a dilution fridge to cool [26], whether the module would be placed at the 4 K layer or in higher-temperature regions of the fridge. Additionally, the timing and slack measurements indicate that we can run the stochastic calibration protocol at very high frequencies for rapid calibration. In the fastest case, which is the 14 nm 1 V design at 77 K, we can run the calibration at up to nearly 450 MHz, leading to a total time for the calibration step of less than 18 ns.

VI. Future Outlook

We have demonstrated a very promising implementation of a single-shot, stochastic calibration algorithm for tuning and drift control of quantum processors using FPGA and CMOS control hardware. Successfully calibrating quantum systems using this algorithm requires low-latency control hardware, as faster update times allow for tuning to higher gate fidelities.

The algorithm's dependence on this rapid timing and single-shot feedback motivates the need for low-latency feedback between quantum and classical systems. We designed FPGA and ASIC synthesis of the calibration algorithm and demonstrated the ease with which it can be added to modern quantum control systems to perform on-line calibration of quantum gates in rapid time scales. This is one example algorithm in a class of algorithms that rely on fast feedback and have extensions to many different scenarios for tuning quantum systems, including multi-parameter and multi-qubit gate calibration [14]. The power and timing constraints of our implementation show promise for these extensions. Calibrating multiple qubits or parameters could be done either serially or in parallel, depending on the addressability of qubits in the system and constraints

TABLE II

SYNTHESIZED AND SIMULATED POWER AND TIMING RESULTS FOR CRYOGENIC AND ROOM TEMPERATURE IMPLEMENTATIONS OF STOCHASTIC CALIBRATION. WE OBSERVE VERY LOW POWER AND EXCELLENT TIMING PERFORMANCE WHEN SCALING OUR DESIGN TO LOW VOLTAGE CRYOGENIC NODES. TAKING THE INVERSE OF THE TOTAL TIME MEASUREMENTS ALSO INDICATES HOW FAST THIS PROTOCOL COULD BE RUN IN EACH PLATFORM, UP TO APPROXIMATELY 448 MHZ IN THE BEST TIMING CASE OF 14 NM, 300K OPERATION AT 1 V.

Metric	**28 nm (LVT) at 1 V**	**28 nm (SVT) at 1 V**	**14 nm at 1 V**	**14 nm at 1 V**	**14 nm at 0.6 V**
Temperature	300 K	300 K	300 K	77 K	77 K
Slack (Total Time) at 100 MHz	1.01 ns (8.98)	2.54 ns (7.43)	5.54 ns (4.46)	7.77 ns (2.23)	6.88 ns (3.12) (**1.24x higher**)
Dynamic Power	83.1 uW	77.5 uW	34.49 uW	48.29 uW	20.78 uW (**1.66x lower**)
Leakage Power	0.244 mW	19.1 uW	22 uW	19.5 uW	4.2 uW (**5.2x lower**)
Total Power	0.3272 mW	96.65 uW	56.49 uW	67.79 uW	24.98 uW (**2.26x lower**)

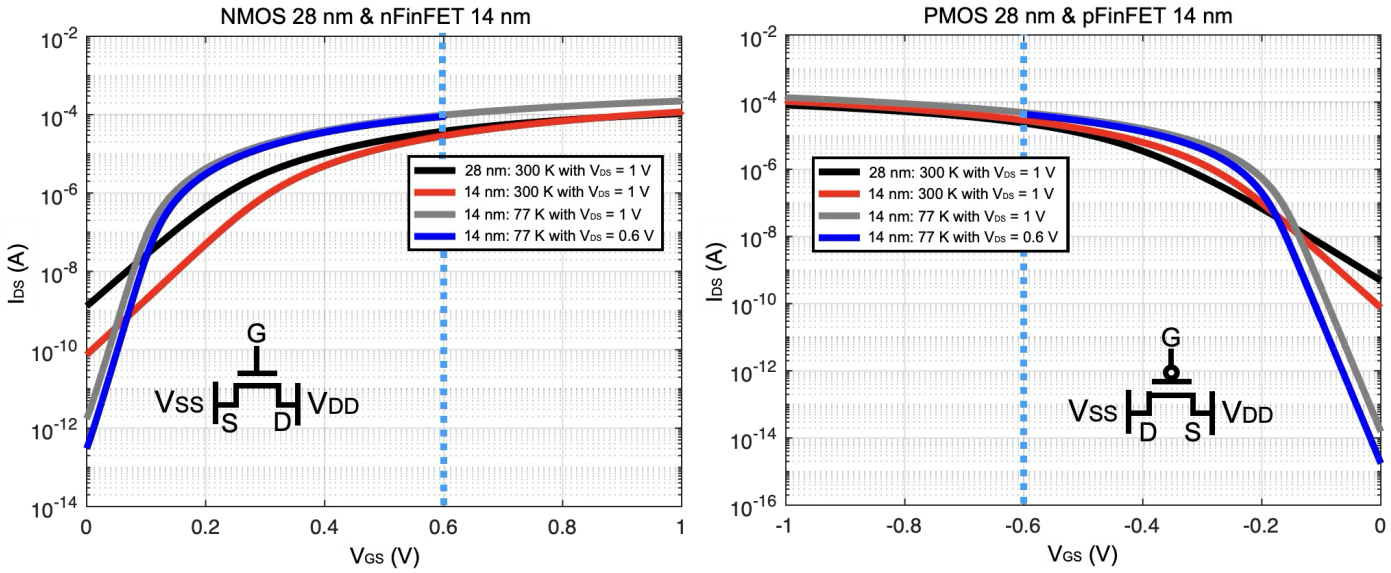

Fig. 6. The I_{DS} vs. V_{GS} curves for the various device technologies used in our ASIC synthesis show the improved switching performance gained at cryogenic temperatures.

from qubit crosstalk. The very low power consumption of our single-parameter, single-qubit gate example shows promise that power will not be a major limiter for small numbers of qubits being calibrated in parallel, but could become an issue in large systems where serial calibration may be needed.

While the custom digital hardware used in our design can quickly scale, a limiter shown in Table I is QPU execution time, particularly for slower qubit modalities such as trapped ion and silicon spin qubits. Different qubit modalities also involve different control parameters, some of which may impose additional constraints on the way η is tuned (for example, the power applied to a voltage source will have upper and lower limits). Additionally, the specific topology of the quantum hardware under calibration will impose constraints on the input and output chain between the quantum and classical hardware.

We envision our calibration module being a piece of a larger classical control stack, including other important functionality like FPGA- or ASIC-based quantum characterization protocols [27] or decoding for error correction [28], [29], in a future where quantum and classical hardware sit in close proximity for rapid feedback and adaptive control. The development of further designs for low-power control, characterization, calibration and error-correction in cryogenic CMOS ASICs will be especially important for the future of quantum computing. The modular, low-power and high-speed nature of our calibration logic design will aid in this endeavor, and shows a promising start towards on-line calibration implemented within the classical control hardware of quantum systems.

ACKNOWLEDGMENT

N. E. Miller is a 2021 Fellow of the DOD National Defense Science and Engineering Graduate (NDSEG) Fellowship program and acknowledges the funding of the Air Force Office of Scientific Research as his sponsoring agency. N. E. Miller acknowledges insightful conversations with Luke Burkhart and Daniel Lobser.

REFERENCES

[1] M. E. Beverland, P. Murali, M. Troyer, K. M. Svore, T. Hoefler, V. Kliuchnikov, G. H. Low, M. Soeken, A. Sundaram, and A. Vaschillo, "Assessing requirements to scale to practical quantum advantage," 2022.

[2] Y. Xu, G. Huang, J. Balewski, R. Naik, A. Morvan, B. Mitchell, K. Nowrouzi, D. I. Santiago, and I. Siddiqi, "Qubic: An open-source fpga-based control and measurement system for superconducting quantum information processors," *IEEE Transactions on Quantum Engineering*, vol. 2, pp. 1–11, 2021.

[3] Y. Xu, G. Huang, N. Fruitwala, A. Rajagopala, R. K. Naik, K. Nowrouzi, D. I. Santiago, and I. Siddiqi, "Qubic 2.0: An extensible open-source qubit control system capable of mid-circuit measurement and feed-forward," 2023.

[4] L. Stefanazzi, K. Treptow, N. Wilcer, C. Stoughton, C. Bradford, S. Uemura, S. Zorzetti, S. Montella, G. Cancelo, S. Sussman, A. Houck, S. Saxena, H. Arnaldi, A. Agrawal, H. Zhang, C. Ding, and D. I. Schuster, "The qick (quantum instrumentation control kit): Readout and control for qubits and detectors," *Review of Scientific Instruments*, vol. 93, p. 044709, 04 2022.

[5] C. Ding, M. Di Federico, M. Hatridge, A. Houck, S. Leger, J. Martinez, C. Miao, D. S. I, L. Stefanazzi, C. Stoughton, S. Sussman, K. Treptow, S. Uemura, N. Wilcer, H. Zhang, C. Zhou, and G. Cancelo, "Experimental advances with the qick (quantum instrumentation control kit) for superconducting quantum hardware," *Phys. Rev. Res.*, vol. 6, p. 013305, Mar 2024.

[6] G. Kasprowicz, P. Kulik, M. Gaska, T. Przywozki, K. Pozniak, J. Jarosinski, J. W. Britton, T. Harty, C. Balance, W. Zhang, D. Nadlinger, D. Slichter, D. Allcock, S. Bourdeauducq, R. Jördens, and K. Pozniak, "Artiq and sinara: Open software and hardware stacks for quantum physics," in *OSA Quantum 2.0 Conference*, p. QTu8B.14, Optica Publishing Group, 2020.

[7] D. S. Lobser, J. W. Van Der Wall, and J. D. Goldberg, "Performant coherent control: bridging the gap between high- and low-level operations on hardware," in *2022 IEEE International Conference on Quantum Computing and Engineering (QCE)*, pp. 320–330, 2022.

[8] S. Pellerano, S. Subramanian, J.-S. Park, B. Patra, T. Mladenov, X. Xue, L. M. K. Vandersypen, M. Babaie, E. Charbon, and F. Sebastiano, "Cryogenic cmos for qubit control and readout," in *2022 IEEE Custom Integrated Circuits Conference (CICC)*, pp. 01–08, 2022.

[9] J. C. Bardin, E. Jeffrey, E. Lucero, T. Huang, S. Das, D. T. Sank, O. Naaman, A. E. Megrant, R. Barends, T. White, M. Giustina, K. J. Satzinger, K. Arya, P. Roushan, B. Chiaro, J. Kelly, Z. Chen, B. Burkett, Y. Chen, A. Dunsworth, A. Fowler, B. Foxen, C. Gidney, R. Graff, P. Klimov, J. Mutus, M. J. McEwen, M. Neeley, C. J. Neill, C. Quintana, A. Vainsencher, H. Neven, and J. Martinis, "Design and characterization of a 28-nm bulk-cmos cryogenic quantum controller dissipating less than 2 mw at 3 k," *IEEE Journal of Solid-State Circuits*, vol. 54, no. 11, pp. 3043–3060, 2019.

[10] J. Kelly, R. Barends, B. Campbell, Y. Chen, Z. Chen, B. Chiaro, A. Dunsworth, A. G. Fowler, I.-C. Hoi, E. Jeffrey, A. Megrant, J. Mutus, C. Neill, P. J. J. O'Malley, C. Quintana, P. Roushan, D. Sank, A. Vainsencher, J. Wenner, T. C. White, A. N. Cleland, and J. M. Martinis, "Optimal quantum control using randomized benchmarking," *Phys. Rev. Lett.*, vol. 112, p. 240504, Jun 2014.

[11] D. Egger and F. Wilhelm, "Adaptive hybrid optimal quantum control for imprecisely characterized systems," *Physical Review Letters*, vol. 112, June 2014.

[12] C. Ferrie and O. Moussa, "Robust and efficient in situ quantum control," *Phys. Rev. A*, vol. 91, p. 052306, May 2015.

[13] E. Abbasgholinejad, H. Deng, J. Gamble, J. N. Kutz, E. Nielsen, N. Pisenti, and N. Xie, "Extremum seeking control of quantum gates," 2023.

[14] A. B. Magann, N. E. Miller, R. Blume-Kohout, and K. C. Young, "Single- and few-shot protocols for quantum device calibration and drift mitigation," *In Preparation*, 2025.

[15] L. Burkhart. personal communication.

[16] N. R. Vora, Y. Xu, A. Hashim, N. Fruitwala, H. N. Nguyen, H. Liao, J. Balewski, A. Rajagopala, K. Nowrouzi, Q. Ji, K. B. Whaley, I. Siddiqi, P. Nguyen, and G. Huang, "Ml-powered fpga-based real-time quantum state discrimination enabling mid-circuit measurements," 2024.

[17] M. McEwen, D. Kafri, Z. Chen, J. Atalaya, K. J. Satzinger, C. Quintana, P. V. Klimov, D. Sank, C. Gidney, A. G. Fowler, F. Arute, K. Arya, B. Buckley, B. Burkett, N. Bushnell, B. Chiaro, R. Collins, S. Demura, A. Dunsworth, C. Erickson, B. Foxen, M. Giustina, T. Huang, S. Hong, E. Jeffrey, S. Kim, K. Kechedzhi, F. Kostritsa, P. Laptev, A. Megrant, X. Mi, J. Mutus, O. Naaman, M. Neeley, C. Neill, M. Niu, A. Paler, N. Redd, P. Roushan, T. C. White, J. Yao, P. Yeh, A. Zalcman, Y. Chen, V. N. Smelyanskiy, J. M. Martinis, H. Neven, J. Kelly, A. N. Korotkov, A. G. Petukhov, and R. Barends, "Removing leakage-induced correlated errors in superconducting quantum error correction," *Nature Communications*, vol. 12, p. 1761, Mar 2021.

[18] F. Swiadek, R. Shillito, P. Magnard, A. Remm, C. Hellings, N. Lacroix, Q. Ficheux, D. C. Zanuz, G. J. Norris, A. Blais, S. Krinner, and A. Wallraff, "Enhancing dispersive readout of superconducting qubits through dynamic control of the dispersive shift: Experiment and theory," 2023.

[19] E. Hyyppä, A. Vepsäläinen, M. Papič, C. F. Chan, S. Inel, A. Landra, W. Liu, J. Luus, F. Marxer, C. Ockeloen-Korppi, S. Orbell, B. Tarasinski, and J. Heinsoo, "Reducing leakage of single-qubit gates for superconducting quantum processors using analytical control pulse envelopes," *PRX Quantum*, vol. 5, p. 030353, Sep 2024.

[20] N. Ofek, A. Petrenko, R. Heeres, P. Reinhold, Z. Leghtas, B. Vlastakis, Y. Liu, L. Frunzio, S. M. Girvin, L. Jiang, M. Mirrahimi, M. H. Devoret, and R. J. Schoelkopf, "Extending the lifetime of a quantum bit with error correction in superconducting circuits," *Nature*, vol. 536, pp. 441–445, Aug 2016.

[21] S. M. Clark, D. Lobser, M. C. Revelle, C. G. Yale, D. Bossert, A. D. Burch, M. N. Chow, C. W. Hogle, M. Ivory, J. Pehr, B. Salzbrenner, D. Stick, W. Sweatt, J. M. Wilson, E. Winrow, and P. Maunz, "Engineering the quantum scientific computing open user testbed," *IEEE Transactions on Quantum Engineering*, vol. 2, pp. 1–32, 2021.

[22] K. M. Rudinger, C. I. Ostrove, S. K. Seritan, M. D. Grace, E. Nielsen, R. J. Blume-Kohout, and K. C. Young, "Two-qubit gate set tomography with fewer circuits," 2023.

[23] S. Neyens, O. K. Zietz, F. Watson, Thomas F.and Luthi, A. Nethwewala, H. C. George, E. Henry, M. Islam, A. J. Wagner, F. Borjans, E. J. Connors, J. Corrigan, M. J. Curry, D. Keith, R. Kotlyar, L. F. Lampert, M. T. Madzik, K. Millard, F. A. Mohiyaddin, S. Pellerano, R. Pillarisetty, M. Ramsey, R. Savytskyy, S. Schaal, G. Zheng, J. Ziegler, N. C. Bishop, S. Bojarski, J. Roberts, and J. S. Clarke, "Probing single electrons across 300-mm spin qubit wafers," *Nature*, vol. 629, pp. 80–85, May 2024.

[24] E. Nielsen, K. Rudinger, T. Proctor, A. Russo, K. Young, and R. Blume-Kohout, "Probing quantum processor performance with pygsti," *Quantum Science and Technology*, vol. 5, p. 044002, jul 2020.

[25] A. D. Gaidhane, R. Saligram, W. Chakraborty, S. Datta, A. Raychowdhury, and Y. Cao, "Design exploration of 14 nm finfet for energy-efficient cryogenic computing," *IEEE Journal on Exploratory Solid-State Computational Devices and Circuits*, vol. 9, no. 2, pp. 108–115, 2023.

[26] D. J. Reilly, "Challenges in scaling-up the control interface of a quantum computer," in *2019 IEEE International Electron Devices Meeting (IEDM)*, pp. 31.7.1–31.7.6, 2019.

[27] N. E. Miller, B. Chakraborty, and S. Mukhopadhyay, "A reconfigurable quantum state tomography solver in fpga," in *2023 IEEE International Conference on Quantum Computing and Engineering (QCE)*, vol. 01, pp. 1412–1421, 2023.

[28] K. M. Barnes, T. Bialas, O. Buğdayci, E. T. Campbell, N. I. Gillespie, K. Johar, R. Rajan, A. W. Richardson, L. Skoric, C. Topal, M. L. Turner, and A. B. Ziad, "A highly efficient qec decoder implemented on fpga and asic," in *2023 IEEE International Conference on Quantum Computing and Engineering (QCE)*, vol. 02, pp. 375–376, 2023.

[29] B. Barber, K. M. Barnes, T. Bialas, O. Buğdaycı, E. T. Campbell, N. I. Gillespie, K. Johar, R. Rajan, A. W. Richardson, L. Skoric, C. Topal, M. L. Turner, and A. B. Ziad, "A real-time, scalable, fast and resource-efficient decoder for a quantum computer," *Nature Electronics*, Jan 2025.