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Enabling a Portable Brain Computer Interface for Rehabilitation of Spinal Cord Injuries

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***Abstract*—In clinical trials, brain signal decoders combined with spinal stimulation have shown to be a promising means to restore mobility to paraplegic and tetraplegic patients. To make this technology available for home use, the complex brain signal decoding must be performed using a low-power, portable battery operated system. This case study shows how the decoding algorithm for a Brain-Computer Interface (BCI) system was ported to an embedded platform, resulting in an over $25\times$ power reduction, compared to the previous implementation, while respecting real-time and accuracy constraints.**

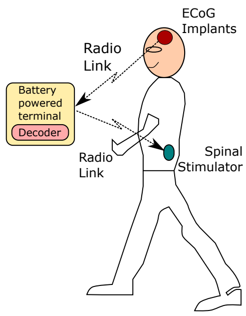
***Index Terms*—Brain-computer interfaces (BCIs), Decoder, Feature extraction, Embedded systems.**

I. Introduction

Recent advances in BCI make it possible to extract meaningful information from brain signals. Electrocorticography (ECoG) is a minimally invasive technique for detecting brain signals, where an array of electrodes is implanted on the surface of the brain and each electrode measures a signal that is averaged over thousands of neurons. The decoded information can be used in a closed-loop system to control an exoskeleton or to generate stimulation patterns for patients suffering spinal cord injury [1], [2], [3]. This approach can be used to restore mobility to paralyzed patients, by detecting the patient's movement intention, and then inducing controlled movements in the lower-limbs through spinal cord stimulation [1], [4], as shown in Fig. 1a. The system consists of the ECoG implants, a radio link to relay the brain signals to a battery-powered terminal where decoding is performed, a radio link to the stimulator, and the spinal stimulator (Fig. 1b).

One of the technical hurdles is the compute intensive signal processing required to decode the brain signals in real-time with low power consumption. We summarize the work done to take an early system prototype where the signal decoding algorithm was performed on a notebook computer running Matlab and consuming ≈50W, and to port it to a low power embedded platform consuming $\approx 1.85W$, resulting in $25\times$ power reduction. This smaller system could be worn by the patient on a belt and used in daily life.

(a) Patient Walking Using BCI System [1]



(b) High Level System View

Fig. 1: Restoring Mobility using BCI and Spinal Stimulation

II. Decoding Algorithm

Brain signal decoding systems typically work using a two step process. First, *features* are extracted from the raw signals and then these *features* are applied to a classifier to decode actions. In this system, the algorithm is executed every 100 msec and the flow [5] is shown in Fig. 2. The raw input signals from the electrodes are first processed to remove artifacts from possible errors in the Analog to Digital Converter (ADC) or the radio link. Then, a set of frequency band power features are extracted using a Continuous Wavelet Transform (CWT), for a fixed number of frequency bands in the range of 10 Hz to 200 Hz. The resulting features are decoded by first applying a pre-calculated linear model, and then using a soft-max function and a Hidden Markov Model (HMM) for decisions

The features are extracted by a convolution of the input signal with a Morlet Wavelet [6]. A "mother" wavelet is scaled for the different frequency bands and convolved with a 200-msec window of the input signal. This convolution is performed using the Fast Fourier Transform (FFT) algorithm. A FFT is performed on each window of the signal, the result is multiplied by the pre-computed FFT of the scaled wavelets, then an inverse Fast Fourier Transform (iFFT) is performed, as shown in Fig. 3.

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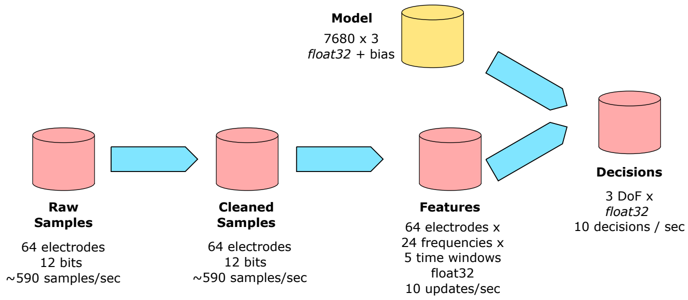

Fig. 2: BCI Decoding Flow for Scenario with 7680 Features

Although the system can be used for different applications including walking, 6D continuous movement of an upper limb, and others, the experimental results presented here are for a walking application which requires 64 electrodes, 24 frequency bands and 5 time windows, resulting in 7 680 features.

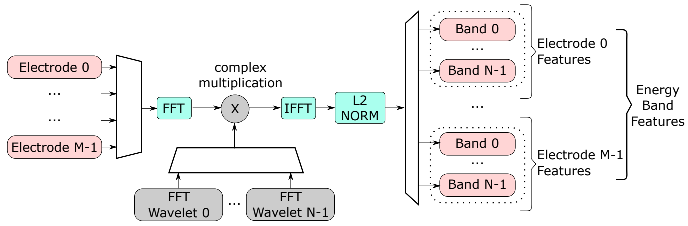

Fig. 3: Use of FFT for Wavelet Convolutions

The FFT results in a complex, frequency domain signal (stored in single-precision *FP32*). Each complex multiplication between a wavelet value and this signal requires four multiplications and two additions. Initial benchmarking of the algorithm running in C++ on an x86 host showed that these multiplications took close to half of the overall CPU time for the (see column 'No Optimization' in Fig. 4). Looking at the FFT of the wavelet we observe that the majority of the values are zero, or extremely close to zero. Multiplying by these near zero values is unnecessary. Using a threshold of 10^{-11}, we were able to remove 80% of the multiplications, resulting in a 25% reduction in the execution time (see column 'Wavelet Sparsity' in Fig. 4). This change barely impacted the decoding accuracy, resulting in a single mis-prediction in 2000 predictions, an acceptable error rate.

The ECoG signal is sampled at 590 $Samples/s$, and the decoding algorithm is performed every 100 msec, after every 59 new samples. To avoid boundary effects and improve detection of low frequency components, the most recent time window is concatenated with the two previous ones to give a signal with 177 samples. The original implementation used a 512-point FFT, however a 256-point FFT (power of 2 above 177) is sufficient. Reducing the FFT size from 512 to 256 yielded close to a 50% reduction in compute time for this step (see column 'FFT256' in Fig. 4). Combined, both optimizations, resulted in a reduction of the total execution time by 50%.

The code was then ported to an embedded platform based on a BCM2711 SoC integrating a quad core ARM™ A72 processor, using the FFTW library which exploits Neon™ extensions for computing the FFTs. On this platform, the complete decoding algorithm executed in 18 msec, well within target required for real-time operation. The power consumption of the platform was measured to be $\approx 1.85\ W$ while the decoding was executing, resulting in a $\approx 25\times$ reduction compared to the original implementation on a laptop computer.

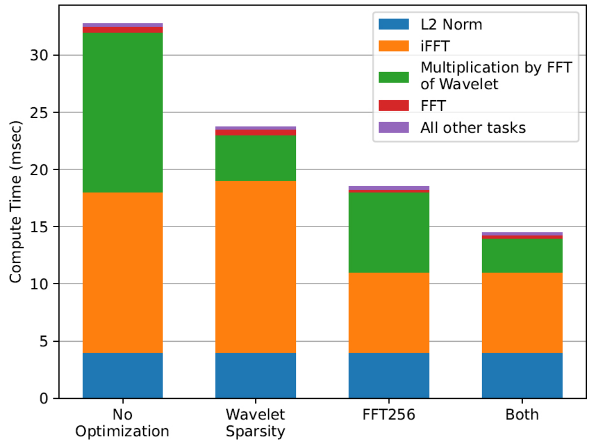

Fig. 4: Compute Time for Decoding (x86 Host)

III. Conclusions

Patients require that the BCI systems for motor rehabilitation be portable and low-power to provide autonomy for home use. Our case study showed how, with simple algorithmic optimizations, the signal decoding could be performed on an off-the-shelf embedded platform. The next stage of this research is the design of a dedicated integrated circuit, enabling the decoding to be performed directly in the implant.

Acknowledgments

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