

# Older and Wiser: The Marriage of Device Aging and Intellectual Property Protection of Deep Neural Networks

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## ABSTRACT

Deep neural networks (DNNs), such as the widely-used GPT-3 with billions of parameters, are often kept secret due to high training costs and privacy concerns surrounding the data used to train them. Previous approaches to securing DNNs typically require expensive circuit redesign, resulting in additional overheads such as increased area, energy consumption, and latency. To address these issues, we propose a novel hardware-software co-design approach for DNN intellectual property (IP) protection that capitalizes on the inherent aging characteristics of circuits and a novel differential orientation fine-tuning (DOFT) to ensure effective protection.

Hardware-wise, we employ random aging to produce authorized chips. This process circumvents the need for chip redesign, thereby eliminating any additional hardware overhead during the inference procedure of DNNs. Moreover, the authorized chips demonstrate a considerable disparity in DNN inference performance when compared to unauthorized chips. Software-wise, we propose a novel DOFT, which allows pre-trained DNNs to maintain their original accuracy on authorized chips with minimal fine-tuning, while the model's performance on unauthorized chips is reduced to random guessing. Extensive experiments on various models, including MLP, VGG, ResNet, Mixer, and SwinTransformer, with lightweight binary and practical multi-bit weights demonstrate that the proposed method achieves effective IP protection, with only 10% accuracy on unauthorized chips, while preserving nearly the original accuracy on authorized ones.

## CCS CONCEPTS

• Security and privacy → Embedded systems security.

## KEYWORDS

Deep Neural Networks; Intellectual Property Protection; Process-in-Memory; Device Aging.

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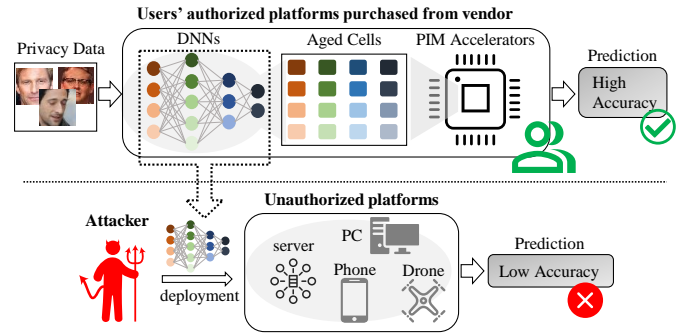


Figure 1: IP protection overview.

## 1 INTRODUCTION

In recent years, foundation models like GPT-3 [2], have driven the advancement of artificial intelligence to unprecedented levels. However, the security concerns associated with these models are garnering increasing attention. This is primarily due to the fact that well-trained deep neural networks (DNNs) represent valuable intellectual property (IP) assets, as they necessitate significant investments in extensive datasets, cutting-edge hardware, and skilled professionals to design the architecture and optimize hyperparameters. While these factors contribute to the commercial profitability of DNNs, they also introduce security vulnerabilities. For instance, the leakage of confidential parameters, such as weights, could enable attackers to develop Trojan horses or adversarial examples, thereby jeopardizing the proper functioning of DNNs.

Existing protection methods can be classified into three categories: watermarking, encryption and circuit obfuscation. However, these methods either provide only a verification capability or incur additional performance overhead during the inference phase.

Watermarking-based protection, encompassing both white-box and black-box techniques (e.g., [6, 20, 23]), primarily operates at the software level. As an example of a typical black-box method, during the training phase, owners introduce distinct marks and labels to a minor subset of the training dataset [6]. In the inference stage, the DNN output on alternative platforms is authenticated by incorporating a specific mark into the input data. If the DNN's output aligns with the expected result, the validator establishes ownership. Although its additional hardware overhead is almost negligible, watermarking cannot prevent model stealers from normally using DNNs for free.

Encryption protection involves using particular encryption algorithms to encrypt the weights of DNNs. For instance, Zuo *et al.* [29] propose a smart encryption scheme that stores AES-encrypted weights of DNNs in the main memory and decrypts them when they are transferred to the processing units. Nevertheless, the mathematically complex AES-based encryption methods tend to consume a significant amount of area overhead and power consumption. To make protection lightweight, Huang *et al.* [10] implemented XOR

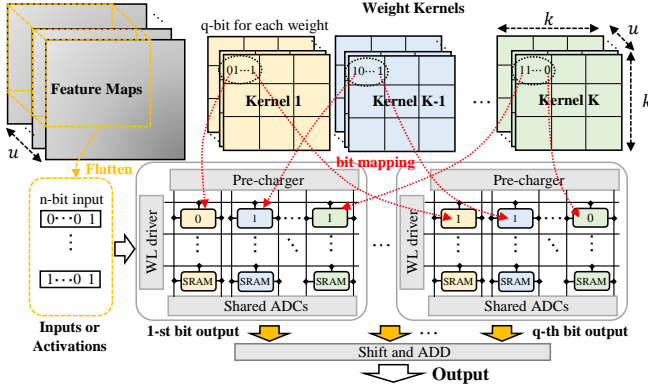


Figure 2: Principle of SRAM-based PIM accelerators.

encryption by modifying the 6T-SRAM cell with dual wordlines and corresponding peripheral circuits to protect DNNs running on SRAM-based accelerators. Cai *et al.* [3] proposed a sparse fast gradient encryption to protect DNNs running on RRAM-based accelerators by encrypting a small proportion of weights.

Circuit obfuscation protection requires modifying the circuit structure according to specific operational logic to achieve normal computation. Chakraborty *et al.* [4] proposed a simple neuron locking scheme by modifying the multiply and accumulate units of TPU-like accelerators, which combines a hardware root-of-trust (i.e., secret key embedded on-chip) to protect DNNs. Zhao *et al.* [27] used a stochastic computing-based scheme and custom hardware accelerator architecture to protect the weights of DNNs running on RRAM crossbars.

This raises the question of whether it is possible to secure DNN workloads without changing the physical architecture of the accelerators. Aging is commonly observed on almost all circuits, which typically been seen as a drawback on hardware's performance. However, when protecting the intellectual property of DNNs, this flaw can be turned into an advantage as shown in Fig. 1. We introduce several innovations to achieve this.

- We propose a novel hardware-software co-design to protect the IP of DNNs without any circuit modification, resulting in zero additional latency, power, and area overheads during the inference phase of DNNs.
- Hardware-wise, we leverage the inherent aging mechanism of transistors to create authorized chips with distinct operational mechanisms compared to unauthorized hardware platforms. Our approach enhances the security of the model by randomly selecting the aging configurations.
- Software-wise, we introduce a differential orientation fine-tuning method that enables DNNs to achieve high accuracy on authorized chips and low accuracy on unauthorized chips with only few fine-tuning procedures.
- Various models, comprising MLP, VGG, ResNet, Mixer, and SwinTransformer, have effectively substantiated the efficacy of our method. Furthermore, the utility and security have also been rigorously appraised.

## 2 PRELIMINARIES AND MOTIVATION

### 2.1 SRAM-based DNN Accelerators

In the last decade, a large number of hardware DNN accelerators have been developed to improve both throughput and energy efficiency. Traditional von Neumann architecture accelerators (e.g., [12]) suffer from large energy and time overheads due to data shuttling between the main memory and computing components. Process-in-memory

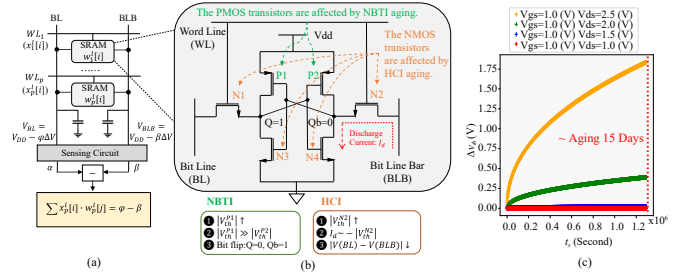


Figure 3: Dot-product computation (a) and aging mechanism in a 6T-SRAM cell (b). Threshold voltage changes due to the HCI-induced Aging (c).

(PIM) accelerators that feature collocation of memory and processing units have been proposed to mitigate the von Neumann bottleneck. Representative PIM-based accelerators include RRAM- and SRAM-based DNN accelerators. In this paper, we choose SRAM-based accelerators for faster programming speed and mature technology and proven reliability.

Fig. 2 depicts the basic principle of SRAM-based DNN accelerators [16], which are mainly composed of a set of SRAM arrays. Well-trained weights are stored in the SRAM cells. Each sliding window on the input feature maps is flattened into a vector, which is converted into word line (WL) voltages using the WL driver. The SRAM arrays perform matrix-vector multiplications between the weights stored in the arrays and the input vectors.  $q$ -bit weights require  $q$  SRAM arrays to store different bits of weights. A  $q$ -bit weight  $w^l(q)$  in layer  $l$  can be represented by

$$w^l(q) = 2^{q-1}w^l[q] + \dots + 2^1w^l[2] + 2^0w^l[1], \quad (1)$$

where  $w^l[i]$  is a binary weight bit and  $i$  is the bit index ( $i \in \{1, 2, \dots, q\}$ ), and the  $i$ -th SRAM array stores the  $i$ -th bits of weights of different kernels in the  $l$ -th layer of DNNs. An  $n$ -bit input can also be expressed in a similar way to Eq. (1). These input vectors are streamed in through a bit-serial manner, and the same index bits of inputs are supplied at the same time.

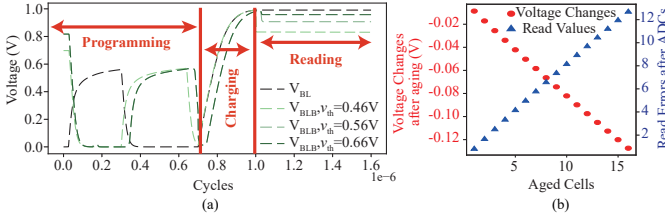
Fig. 3 (a) illustrates the in-memory computation principle of an SRAM column, which computes an inner product between an input bit vector  $[x_1^l[i], x_2^l[i], \dots, x_p^l[i]]$  ( $p = k \times k \times u$ ) and the stored weight bit vector  $[w_1^l[j], w_2^l[j], \dots, w_p^l[j]]$ , where  $i$  and  $j$  are the bit indexes of inputs and weights, respectively. Though the involved input bits and weight bits are both digital, the inner product is computed in the analog domain. The inner product of the two vectors is manifested by the voltage difference between BL and BLB of the column, which is proportional to  $\sum_p x_p^l[i] \cdot w_p^l[j]$ . The voltage difference between the bit line (BL) and bit line bar (BLB), which is called *read voltage difference* in this work, is sensed and digitized by an analog-to-digital converter (ADC).

### 2.2 Device Aging

Hot Carrier Injection (HCI) and Negative Bias Temperature Instability (NBTI) are two primary factors contributing to the aging of NMOS and PMOS transistors, respectively [5, 18, 24, 25]. HCI and NBTI both cause an increase in the threshold voltage ( $v_{th}$ ) of transistors, which can result in the malfunctioning of SRAM cells,

$$\Delta v_{th} \propto \zeta \cdot t_s^\chi, \quad (2)$$

where  $t_s$  is the stress time,  $\zeta$  is a coefficient that depends on the aging type and working environment of the circuit, and  $\chi$  is a positive exponent which differs from the aging type. The detailed formulas of



**Figure 4: Voltage changes of 6T-SRAM cells (a) and read errors after ADC (b).**

NBTI- and HCI-induced aging can be found in [5, 18, 24, 25]. Fig. 3 (c) illustrates the trend of threshold voltage growth with stress time at different supply voltages (i.e.,  $V_{ds}$ ) for HCI-induced aging under the 45nm technology node. The increase in  $v_{th}$  is faster with a higher supply voltage applied to an NMOS transistor. When  $V_{ds} = 2.0V$  is applied to the NMOS transistor for about 15 days,  $v_{th}$  increases by about 0.5V. With the power supply voltage  $V_{ds} = 2.5V$ ,  $v_{th}$  increases by about 2.3V. Therefore, changing the working conditions can rapidly age the chip. Even though both types of aging can increase the threshold voltage, they result in different behaviors of aged SRAM devices.

**NBTI can cause read bit flip.** Fig. 3 (b) illustrates the NBTI aging impact on a 6T-SRAM cell. If the SRAM has been configured to  $Q=1$  and  $Qb=0$  for a sufficiently long time, the threshold voltage of the P1 transistor ( $v_{th}^{P1}$ ) will experience a clear increase due to the influence of NBTI. When  $|v_{th}^{P1}| \gg |v_{th}^{P2}|$ , bit flip may occur, that is,  $Q=0$  and  $Qb=1$ . Under this circumstance, the read result of the SRAM will flip as well.

**HCI can change the SRAM read voltage.** As illustrated in Fig. 3 (b), when the WL is at logic high, the NMOS transistors N1 and N2 discharge BL and BLB, respectively. While transistor N4 is on and transistor N3 is off, the charge on the BL remains constant and the BLB discharges. However, if the discharge current flowing through N2 is reduced due to HCI-induced aging, the threshold voltage of N2 increases. As a result, the read voltage difference (i.e.,  $\Delta V_{read}$ ) of the SRAM cell decreases, which can lead to changes in the layer outputs of DNNs, and associated accuracy degradation.

### 2.3 Motivation

NBTI in SRAMs can cause bit flip, which causes “digital” errors and can easily be detected as defective chips. On the contrary, HCI impacts SRAMs in an “analog” way and cannot be detected through the I/O interface of chips. Indeed, it is reasonable to assume that only the I/O interface can be accessed when chips are sold. Thus, HCI-induced aging is more concealed that can prevent attackers from obtaining specific aging information of SRAM-based DNN accelerators through I/O interface. From this point of view, we utilize HCI-induced aging to protect the security of DNNs’ weights.

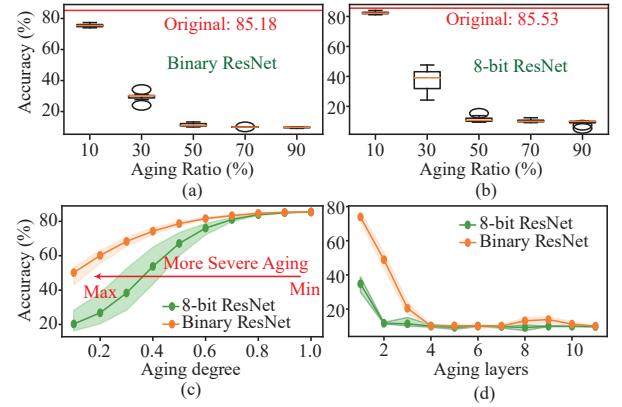
## 3 MARRIAGE OF AGING AND IP PROTECTION

### 3.1 Threat Models

Once the attacker obtains the weights of DNNs, (s)he could potentially clone the DNNs to another chip. As a result, attackers may gain financial interests by reselling high performance DNNs without authorization from the DNN providers.

**Attacker’s Capabilities.** End users may require a new DNN when facing with new tasks, so the DNN vendor needs to transmit it through the internet, which provides the possibility for attackers to steal these DNNs by the man-in-the-middle attacks. DNNs running on accelerators may also be stolen by attackers via side-channel attacks [9].

**Attacker’s Limitations.** Consistent with literatures (e.g., [7, 15]), we assume attackers do not have the private data to retrain the stolen



**Figure 5: Aging ratio impact on binary (a) and 8-bit ResNet (b). Aging degree impact (c) and layer impact (d). Results are obtained after 100 trials.**

parameters of DNNs, as these data are usually private and precious. Also, data protection laws and commercial values protect these data from being made public.

### 3.2 HCI Aging Impact

We first analyze how HCI impacts the accuracy of DNNs running on SRAM-based PIM accelerators. We utilize LTspice to simulate the BL (BLB) voltage comparison of a  $16 \times 1$  SRAM array with different HCI-induced aged cells under 45nm technology node in Fig. 4 (a). When the SRAM stores ‘1’ (where  $Q=1$  and  $Qb=0$ ) and the read voltage signal is at high level, NMOS transistors N2 and N4 are turned on, forming a discharge path of BLB as shown in Fig. 3 (b). At this point, the voltage of  $V_{BLB}$  is  $V_{BLB} = V_{pre} - \Delta$ . Conversely, since transistor N3 is turned off, the voltage of BL remains unchanged as  $V_{BL} = V_{pre}$ . As the SRAM cell ages, the voltage drop of BLB changes accordingly.

Specifically, when no aging has occurred (i.e.,  $v_{th} = 0.46V$ ), the read voltage of BLB (see  $V_{BLB}$  in Fig. 4 (a)) is approximately 0.83V. When HCI aging occurs, the read voltage of BLB is about 0.9V when  $v_{th} = 0.56V$ . As the threshold voltage increases to 0.66V, the read voltage of BLB also increases to 0.95V. Thus, the change in threshold voltage  $v_{th}$  causes a corresponding change in the BLB voltage, which in turn results in read errors. Fig. 4 (b) shows that as the number of aged SRAM cells in a population increases, the read voltage of the aged circuit becomes smaller than that of the unaged case. This introduces read errors after digitization by ADCs. For instance, if 15 SRAM cells that all store ‘1’ connected to the same BL and BLB are aged, although the voltage difference after aging ( $v_{th} = 0.66V$ ) is reduced by about only 0.12V, a read error value of ‘12’ will be generated after ADCs with 0.01V read voltage interval. Hence, we can utilize the HCI aging mechanism to develop unique DNN accelerators. This approach is fundamentally distinct from traditional accelerator protection. Investigating the impact of aged chips on DNNs’ accuracy becomes a critical issue, which will be explored in the following contents.

**• Aging Ratio.** Assuming that the aged SRAM cells are distributed in a two-dimensional aging matrix  $M_{aging}$ , consisting of aged element  $m_{aging}$  and normal element  $m$ , then the aging ratio  $\sigma$  can be expressed as

$$\sigma = \frac{\text{Number}(m_{aging})}{\text{Number}(m_{aging}) + \text{Number}(m)} \times 100\%. \quad (3)$$

To investigate the impact of aging ratio, we evaluate the accuracy of ResNet on CIFAR10 under different aging ratios, as shown in Fig. 5 (a) and (b). The aging degree is 0.24 (aging degree is defined in the

following sub-section). Obviously, the accuracy decreases as the aging ratio increases. For instance, the accuracy of the binary (8-bit) ResNet decreases by an average of 50% (40%) on aged SRAM accelerators when the aging ratio is 30%. As the aging ratio increases to 50%, the accuracy drops to about 10%.

**⊗ Aging Degree.** Aging degree refers to the read voltage difference ratio between the aged read voltage difference  $\Delta V_{BL,BLB}^{Aged}$  and the unaged read voltage difference  $\Delta V_{BL,BLB}^{Unaged}$  of an SRAM cell, which is defined as

$$\alpha = \Delta V_{BL,BLB}^{Aged} / \Delta V_{BL,BLB}^{Unaged}, \quad (4)$$

where  $0 < \alpha \leq 1$ . Here  $\alpha = 1$  indicates that no aging has occurred. The lower the aging degree  $\alpha$ , the more severe the aging is. As the aging degree  $\alpha$  decreases, the read voltage of the aged device also decreases, which leads to a drop in DNN accuracy. Fig. 5 (c) shows the accuracy of binary and 8-bit ResNet under different aging degrees with aging ratio  $\sigma$  equals to 30%. The accuracy drops by approximately 8% (12%) when the aging degree is 0.6, and it sharply drops to about 61% (27%) for the binary (8-bit) ResNet when the aging degree decreases to 0.2.

**⊗ Aging Layers Impact.** Fig. 5 (d) shows that as the number of aging layers (where aging ratio and aging degree equal to 90% and 0.24, respectively) increases, the accuracy drops dramatically. For example, when randomly choosing four layers are aged in a binary ResNet, its accuracy drops close to 10%, and only two layers need to be aged for an 8-bit ResNet to completely lose its classification ability. Therefore, the inference accuracy on aged chips can dramatically differ from that of unaged chips, which motivates the development of DNNs that perform well on aged chips but poorly on unaged chips.

### 3.3 HCI-Based Authorized Accelerators

**Step-I: Randomly Aging Generation.** For each layer  $l \in \{1, 2, \dots, L\}$  of a DNN, we first randomly generates  $q$  aging matrices,  $\mathbf{M}^l[i]$  for each weight bit index  $i (i \in \{1, 2, \dots, q\})$ , with the same size as the weight bit matrix  $\mathbf{W}^l[i]$  in the  $l$ -th layer mapped on one or multiple SRAM arrays according their capacity limitation.

Assume that for a single SRAM cell, the read voltage differences corresponding to '+1' and '-1' are  $\Delta V$  and  $-\Delta V$ , respectively. After aging with a degree of  $\alpha$  (where  $0 < \alpha \leq 1$ , see Eq. (4)), the corresponding read voltage differences become  $\alpha\Delta V$  and  $-\alpha\Delta V$ , respectively. The aging matrix  $\mathbf{M}^l[i]$  consists of the following values:  $m^l[i]$  for unaged cells and  $m_{aging}^l[i]$  for aged cells, mathematically

$$m^l[i] = \Delta V, m_{aging}^l[i] = \alpha m^l[i]. \quad (5)$$

The positions of the aged cells, aging ratio and aging degree in the aging matrices are randomly generated.

State-of-the-art DNNs typically have a large number of layers, and thus, SRAM computing resources may not be sufficient to hold all layers on different SRAM arrays. In this case, the same SRAM arrays may be reused, and different layers will share the same aging matrices. We use the layer with the most number of weights to generate a prototype aging mask  $\mathbf{M}^{pro}[i]$  for each bit index, and the other layers use subsets of it, which is mathematically

$$\mathbf{M}^l[i] \subseteq \mathbf{M}^{pro}[i]. \quad (6)$$

**Step-II: Differential Orientation Fine-tuning (DOFT).** After obtaining the aging matrices by reading the real SRAM-based PIM chip, the fine-tuning procedure is performed on independent hardware (e.g., GPU/TPU servers) rather than on the actually aged chips due to the challenges involved in developing additional hardware and software drivers to shuttle inference results and updated weights

between servers and deliberate-aged chips. Moreover, the procedure of programming updated weights into SRAM cells during training incurs significant latency overhead. Therefore, to overcome these challenges, an aged chip simulation is developed to reflect the aging situation during fine-tuning.

**Authorized Chip Simulation.** Authorized chips mean the chips with deliberate aging. For weights represented by  $q$  bits (each weight bit is either '+1' or '-1' to match the electrical properties of 6T SRAMs), the matrix-vector multiplication of weights and inputs  $A^{l-1}$  of layer  $l$  can be expressed as

$$O^l = (2^{q-1} \times \mathbf{M}^l[q] \odot \mathbf{W}^l[q] + \dots + 2^1 \times \mathbf{M}^l[2] \odot \mathbf{W}^l[2] + 2^0 \times \mathbf{M}^l[1] \odot \mathbf{W}^l[1]) \times A^{l-1}, \quad (7)$$

where  $\odot$  is the Hadamard Product operation, and  $\mathbf{W}^l[i]$  and  $\mathbf{M}^l[i]$  are the weight matrix and the corresponding aging matrix of bit index  $i (i \in \{1, 2, \dots, q\})$ , respectively. Then the output of layer  $l$  on after ADCs can be represented by

$$A^l \leftarrow h \left( \left\lfloor O^l / \Delta V^{inter} \right\rfloor \right), \quad (8)$$

where  $\Delta V^{inter}$  is the read voltage interval of ADCs. Eq. (8) simulates the function of nonlinear module and ADCs in SRAM-based PIM DNN accelerators.  $h(\cdot)$  is the nonlinear activation function (e.g., relu or sigmoid), which is realized by digital modules in the peripheral circuits.

**Unauthorized Chip Simulation.** The term "unauthorized" is used to describe chips that have not undergone the deliberate aging treatment. In practice, commonly used GPUs/TPUs, general-purpose CPUs, and DNN accelerators without deliberate aging can be considered as unauthorized chips. Eqs. (7) and (8) remain valid in this case, but the elements in the aging matrices are simply composed of  $\Delta V$  and  $-\Delta V$ , corresponding to the '+1' and '-1' values, respectively.

To distinguish between authorized and unauthorized chips, we introduce a penalty term in the loss function to reflect the accuracy gap through the objective loss function of the DOFT method, which is defined as

$$\begin{aligned} \min \mathcal{L}_{DOFT} &= \min_X \mathbb{E} \mathcal{L}(Y^a, Y^t) + \lambda \times \max_X \mathbb{E} \mathcal{L}(Y^u, Y^t) \\ &\approx \min_X (\mathbb{E} \mathcal{L}(Y^a, Y^t) - \lambda \times \mathbb{E} \mathcal{L}(Y^u, Y^t)), \end{aligned} \quad (9)$$

where  $X$  and  $Y^t$  represent the inputs and ground-truth labels of the entire dataset, respectively.  $Y^a$  and  $Y^u$  are the outputs on authorized and unauthorized chips, respectively.  $\mathcal{L}$  denotes the loss function, which can be either cross-entropy loss or mean squared error loss.  $\mathbb{E}$  is the operation of mathematical expectation.  $\lambda$  is a hyper-parameter that controls the importance of the accuracy loss between authorized and unauthorized chips. Thus, this loss function aims to achieve two objectives. The first is to improve accuracy on authorized chips, and the second is to reduce accuracy on unauthorized chips.

To achieve the objectives, we employ the gradient backpropagation method to update the weights of DNNs during fine-tuning. Specifically, each weight bit  $w^l[i] (i \in \{1, 2, \dots, q\})$  in each weight bit matrix  $\mathbf{W}^l[i]$  is updated by

$$w_{fp}^l[i] \leftarrow w_{fp}^l[i] - \eta \times \frac{\partial \mathcal{L}_{DOFT}}{\partial a^l} \times \frac{\partial a^l}{\partial o^l} \times \frac{\partial o^l}{\partial w_{fp}^l[i]}, \quad (10)$$

$$w^l[i] \leftarrow \text{Binary}(w_{fp}^l[i]), \quad (11)$$

where  $\eta$  is the learning rate, and  $a^l$  and  $o^l$  are elements in the output matrix  $A^l$  and multiplication matrix  $O^l$ , respectively.  $w_{fp}^l[i]$  is full-precision intermediate weight in layer  $l$  for bit index  $i$  (each  $w^l[i]$ ,



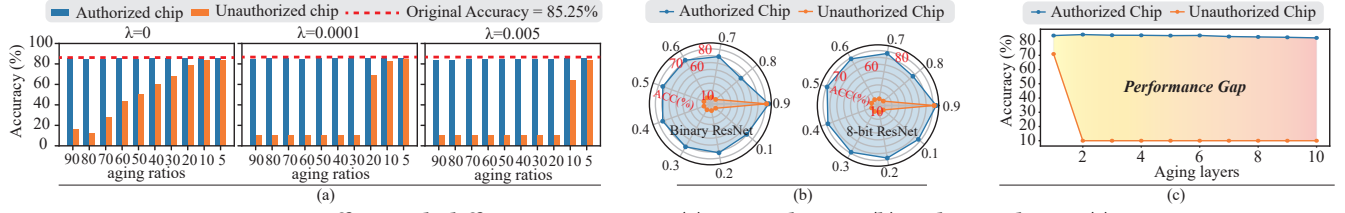


Figure 6: IP Protect effect with different aging ratios (a), aging degrees (b) and aging layers (c) on ResNet.

$i \in \{1, 2, \dots, q\}$ , has an associated full-precision intermediate weight  $w_{fp}^l[i]$ . The third gradient term in Eq. (11) involves the derivative binary quantization (where  $\text{Binary}(\cdot)$  function in Eq. (11) quantizing  $w_{fp}^l[i]$  to ‘+1’ or ‘-1’), which is non-differentiable. To address this issue, the straight-through estimator (STE) [1] is utilized to approximate its gradient by

$$\partial o^l / \partial w_{fp}^l[i] \approx \partial o^l / \partial w^l[i]. \quad (12)$$

After few epochs of fine-tuning, once the loss function  $\mathcal{L}_{DOFT}$  has reached a plateau and is no longer decreasing, the well-trained weight bit matrices  $\mathbf{W}^l[i]$  ( $i \in \{1, 2, \dots, q\}$ ) can be deployed onto deliberate-aged authorized chips.

## 4 EVALUATION

### 4.1 Experimental Setup

**Benchmarks.** The evaluation was carried out using an MLP consisting of two fully-connected layers on the MNIST dataset [14], as well as VGG [21], ResNet [8], Mixer [22], and Swin Transformer [17] on the CIFAR-10 dataset [13]. To evaluate the versatility of the method on both edge and server-side applications, the model’s weights are quantized into single-bit (binary) and multi-bit (8-bit) representations. All aged models successfully completed the proposed differential orientation fine-tuning procedure within few epochs.

**Accelerators.** To simulate SRAM-based accelerators [16], we used LTSpice and derived the parameters of NMOS and PMOS transistors from the 45nm models for low-power applications in the Predictive Technology Model [28]. The SRAM array size is fixed at  $64 \times 64$ , the ADC resolution is set to 7 bits, which generates a read voltage interval ( $\Delta V^{inter}$ ) of 0.01V and covers output values ranging from ‘-64’ to ‘+64’ from the SRAM array without affecting the accuracy of the well-trained DNNs. We developed a PyTorch based toolchain to evaluate accuracy of various DNNs running on (un)aged SRAM-based DNN accelerators according to prior architecture [16]. Unless otherwise specified, the aging degree  $\alpha=0.24$ , and aging ratio  $\sigma=90\%$ . The number of aged layers encompasses all layers of the model.

### 4.2 IP Protection Effect

**Sensitivity Analysis.** Fig. 6 illustrates that our proposed method achieves significantly higher accuracy on authorized chips than on unauthorized chips with different aging ratios, aging degrees and aging layers on ResNet. As depicted in Fig. 6 (a), the fine-tuned ResNet can achieve a significant performance difference between authorized and unauthorized chips across the majority of aging ratios. For instance, when  $\lambda = 0.05$  and the aging ratio is higher than 20%, the accuracy on unauthorized chips is equivalent to random guessing, while the accuracy on authorized chips remains consistent with that of original model. Moreover, the regularization term  $\lambda$  is essential for performance disparity. Specifically, when  $\lambda$  is set to 0, there is minimal performance difference between authorized and unauthorized chips under low aging rates. In contrast, when  $\lambda$  is assigned values of 0.0001

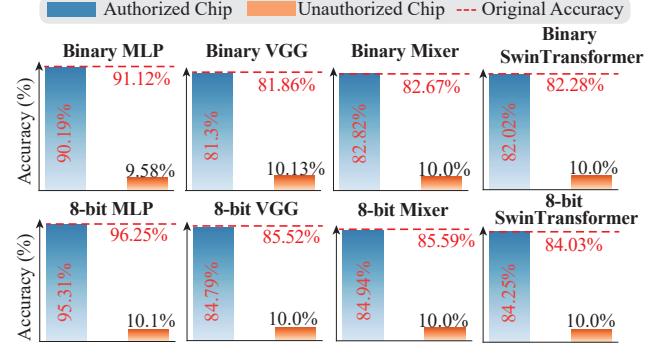


Figure 7: Generalization across various DNNs.

or 0.005, the model can generate significant performance disparities across most aging ratios.

We also performed a sensitivity analysis on the aging degree in Fig. 6 (b). The results demonstrate that for binary or 8-bit weight model, when the aging degree is smaller than 0.7, the accuracy running on the attacker’s chip is close to random guessing, while the accuracy on our chip is guaranteed to be higher. Fig. 6 (c) demonstrates that as the number of aged layers increases, the model displays a distinct difference in accuracy between authorized and unauthorized chips. Notably, when the number of aged layers exceeds 2, the model exhibits higher accuracy for authorized chips, while the accuracy for unauthorized chips approaches that of random guessing.

**Generalization Capability.** Fig. 7 demonstrates the effectiveness of the proposed method across various models, including lightweight MLPs, large-scale VGGs, complex Mixer structures, and Swin Transformers with attention mechanisms. The method consistently enables these models to achieve high accuracy on authorized chips, closely resembling the original model’s accuracy. Simultaneously, the method ensures that the model’s performance on unauthorized chip platforms is nearly equivalent to random guessing.

### 4.3 Utility & Security

**Array Reuse.** For DNNs with a large number of layers or PIM accelerators with limited SRAM computing resources, it may not be possible to map all layers to the available arrays. Instead, we may need to reuse a single SRAM array for multiple layers. In such cases, the aging matrices are also shared by different layers. We can still employ the proposed DOFT method, with the only difference being that the aging matrices are shared among layers, as illustrated in Eq. (6). We examine the protective effects of a total of two (binary MLP) and sixteen (8-bit MLP) binary weight matrices on a single SRAM array in Fig. 8 (a). For example, an aging ratio of 10% demonstrates adequate protection. The accuracy of binary and 8-bit MLP on unauthorized attackers is approximately 20% and 10%, respectively. Thus, these results confirm that our method remains effective in array reuse scenarios.

**Process Variation.** There is a concern that the actual aging chip may deviate from the intended one due to process variation (PV) when the chip is deliberately aged. To evaluate the robustness, we assume that an aging ratio of  $\sigma=90\%$ , but the aging degree  $\alpha$  in the actual

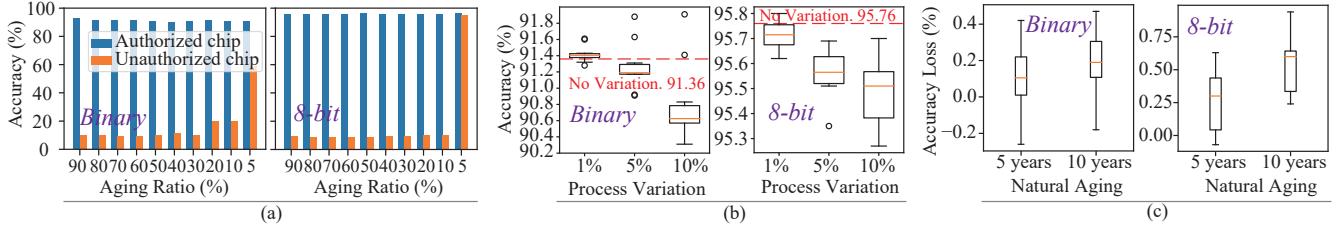


Figure 8: (a) SRAM array reuse and (b) process variation analysis on MLP. (c) Natural aging evaluation on ResNet.

aging mask is a Gaussian random variable with a mean of 0.24 and standard deviation of 1%, 5%, or 10%. Fig. 8 (b) shows the evaluation results on binary and 8-bit MLP models with 100 trials. Our findings demonstrate that even when subjected to PV effect ranging from 1% to 10%, the accuracy drops by no more than 1% point. These results suggest that the proposed method can achieve high fidelity, even when the aging matrix deviates from its intended values due to PV noise.

**Natural Aging.** The chip undergoes natural aging as it is used. A natural question is whether the deliberate aging scheme can still function. We analyze it in Fig. 8 (c) with 100 trials. The natural aging of chips is extremely slow under normal use, as the working voltage  $V_{ds}$  of SRAM-based DNN accelerators is usually small, about 0.6 to 1.2V (e.g., [11, 26]). From the  $v_{th}$  change curve shown in Fig. 3 (c), it can be concluded that the smaller the  $V_{ds}$ , the slower the aging speed. Under the condition of  $V_{ds}=1.2V$  and 323.15K working temperature, the threshold voltage of NMOS transistor with  $v_{th}=0.46893V$  increased by only about 0.0083V(0.0114V) after 5(10) years of continuous stressing. That is to say, compared with the original unaged voltage, the threshold voltage only increases by 1.78% to 2.43% after five to ten years of continuous use. We performed 5-year and 10-year aging accuracy loss validation on ResNet as shown in Fig. 8 (c). All layers of ResNet are aged and the aging ratio is set to 90%. Experimental results confirm that the accuracy loss in natural usage is indeed very small. In the case of 5-year or 10-year aging of the binary ResNet, the accuracy loss does not exceed 0.5%. For the 8-bit model, the maximum accuracy loss does not exceed 1%.

**Security Analysis.** According to Kerckhoff's Principle and Shannon's Maxim [19], attackers can comprehend the protection method except for the secret keys. In our HCI-based DNN weight protection method, the aging status of the cells in SRAM arrays can be regarded as the secret key. For hardware manufacturers, it is reasonable to assume that they only open the I/O interface of accelerators after they are manufactured and tested. As HCI-induced aging does not cause bit flips, attackers cannot determine the aging status of each cell through the I/O interface. Therefore, the only attack method is the exhaustive search to find which cells are aged and how much the aging degree is. Obviously, the crack complexity is at least  $O(2^{|SRAM|} \times |D|)$ , where  $|SRAM|$  is the total number of SRAM cells in the accelerator and  $|D|$  is the number of possible aging degree values. For any existing computer, executing the attack is impossible. If an accelerator has 1Mb SRAM cells, and even if we assume that attackers know the aging degree, namely,  $|D| = 1$ , the attack needs  $2^{1048576}$  attempts to find out the aging status, which is clearly an astronomical number.

## 5 CONCLUSION

Aged chips were once seen as a drawback, but when used with DNNs fine-tuned through the proposed DOFT method, they can achieve remarkable accuracy. This paper skillfully employs HCI to create a hardware-software co-design for DNN weight protection, introducing no additional hardware overhead during DNN inference procedure. We believe this research will inspire the scientific community to

concentrate on low-cost model protection, which has greater potential for practical application.

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