A Comprehensive Inductance-Aware Modeling Approach to Power Distribution Network in Heterogeneous 3D Integrated Circuits

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***Abstract*—Heterogeneous 3D integration technology is a cost-effective and high-performance alternative to planar integrated circuits (ICs). In this paper, we propose an on-chip power distribution network (PDN) modeling technique for heterogeneous 3D-ICs (H3D-ICs), which explicitly takes the effects of on-chip inductance into account. The proposed model facilitates efficient transient and AC simulations with integrated inductive effects, enabling accurate noise characterization at high frequencies and facilitating the exploration of early-stage PDN design. The model is validated via HSPICE simulations, demonstrating a maximum error below 1% and achieving average speedups of 1.5x in transient and 8.5x in AC simulations.**

***Index Terms*—power distribution network, 3D heterogeneous integration, modeling and analysis.**

I. Introduction

Heterogeneous 3D integration is a promising approach to sustain Moore's Law, offering advantages in cost efficiency and high integration density [1]. Unlike homogeneous 3D-ICs, where each tier uses the same process technology, heterogeneous 3D-ICs (H3D-ICs) integrate dies with different process technologies [2]. The scaling of supply voltage and clock frequency, along with increasing power density and variations in interconnect parasitics, complicates PDN design for H3D-ICs significantly. Developing an efficient and accurate PDN model is crucial for "what-if" scenarios and resource allocation, especially in the early stage of 3D IC design.

Various approaches have been proposed to model PDN and evaluate power supply noise (PSN) in 3D-ICs. However, existing methods either rely on commercial tools with high computational demand and long runtime [3], or neglect on-chip inductance effects, overlooking the complexities of heterogeneous 3D integration. Thus, a PDN model specifically for H3D-ICs is needed, which incorporates on-chip inductance and tier heterogeneity, while supporting both time-domain noise simulation and frequency-domain impedance analysis for efficient design exploration at high frequencies.

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In this work, we present a PDN model for H3D-ICs that incorporates on-chip inductance and heterogeneity. HSPICE simulations validate the model with less than 1% error, achieving 1.5x faster transient and 8.5x faster AC simulations.

II. Proposed Method

A. Separation of Power and Ground Networks

The PDN architecture of H3D-ICs, as shown in Fig. 1, comprises power and ground wires, TSVs and bumps. For clarity, TSV and metal layer process variations are not depicted.

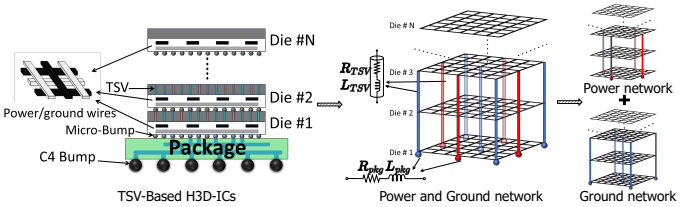

Fig. 1: Separation of power and ground networks in TSV-based H3D-ICs.

Based on the principles of symmetry [4], the power and ground networks are divided into two distinct isolated systems, as illustrated in Fig. 1. This symmetry can be leveraged to simplify the PDN model, thereby effectively reducing its complexity by half. Subsequently, TSVs and bumps are modeled as resistance and inductance, respectively.

B. Consideration of On-Chip Inductance in PDN Modeling

Most studies on H3D-ICs PDN focus on package and TSV inductance, overlooking on-chip interconnect inductance, which becomes more important at higher switching frequencies due to technology scaling. To accurately predict on-chip PSN in the high-frequency domain, it's essential to include the inductive properties of on-chip interconnects. We use the grid sheet inductance formula from [5] to calculate on-chip inductance.

$$L_{\square} = 0.4P\left(\ln\frac{P}{T+W}+\frac{3}{2}\right)\frac{\mu H}{\square} \tag{1}$$

where W, T, and P are the width, thickness, and pitch of the power grid wires, respectively. The unit of $L_{\square}$ is Henrys per square (H/sq).

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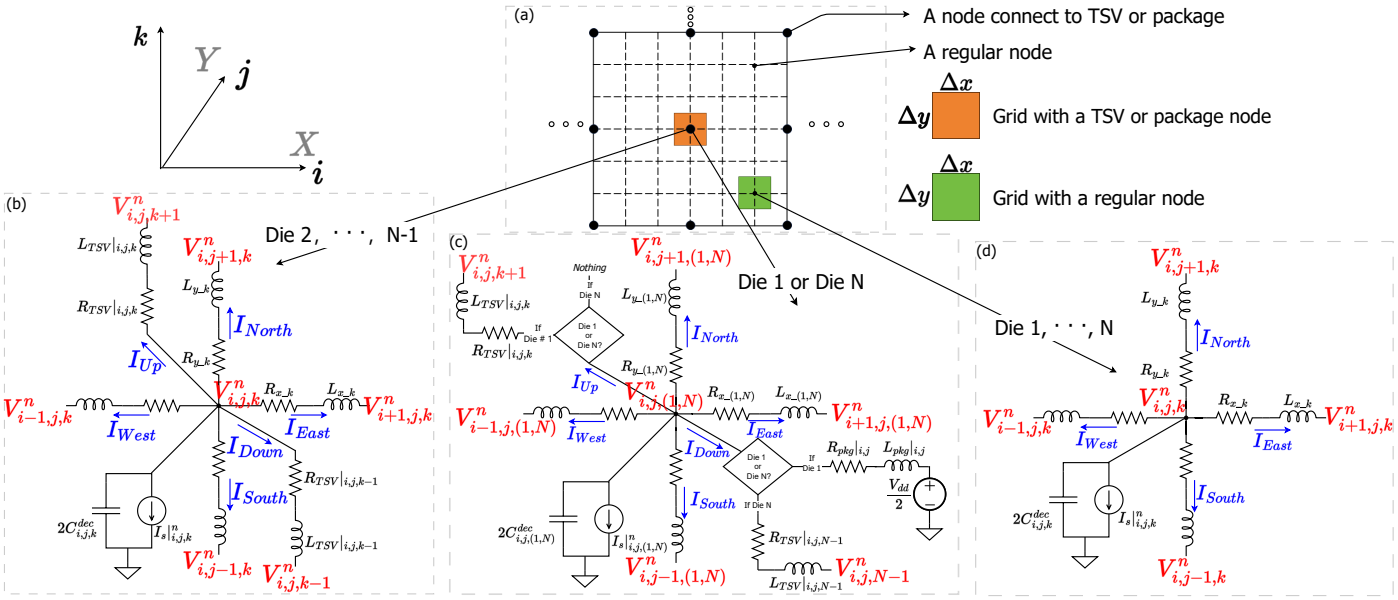

Fig. 2: (a) Top view of PDN grids. Circuit model: (b) Node connected to TSV in Die $1, \ldots, N$. (c) Node connected to TSV in Die 1 or Die N. (d) Regular node in Die $1, \ldots, N$.

C. Equivalent Circuit Models and Simulation Methods

Fig. 2(a) shows the top view of the power distribution grid in H3D-ICs, while Fig. 2(b)–(d) illustrate three different kinds of grid nodes. Die k refers to the die at the k-th layer. R_{x_k}, L_{x_k}, R_{y_k} and L_{y_k} are the segment resistance and inductance of Die k in the x and y directions, respectively. $I_s|_{i,j,k}$ denotes the current source simulating switching circuits, and $C^{dec}_{i,j,k}$ is the decoupling capacitor, both connected to node (i, j, k).

For the transient simulation, Kirchhoff's laws can be applied to derive the KCL equations for each node and the KVL equations for each branch. The time-differentiated terms can then be discretized using the trapezoidal rule (TR) scheme. The AC simulation results can be derived by applying the Laplace transform to the transient simulation.

III. EXPERIMENTAL RESULTS

We implemented the proposed model on a Linux server and compared the simulation results with HSPICE. The chip's initial power density and PDN parameters are based on [6], [7], with additional layers to assess simulation runtime differences.

Fig. 3(a)-(c) show that the discrepancy between our model and HSPICE is below 1%, while Fig. 3(d) illustrates the speedup ratio, with an average speedup of 1.5x for transient simulations and 8.5x for AC simulations.

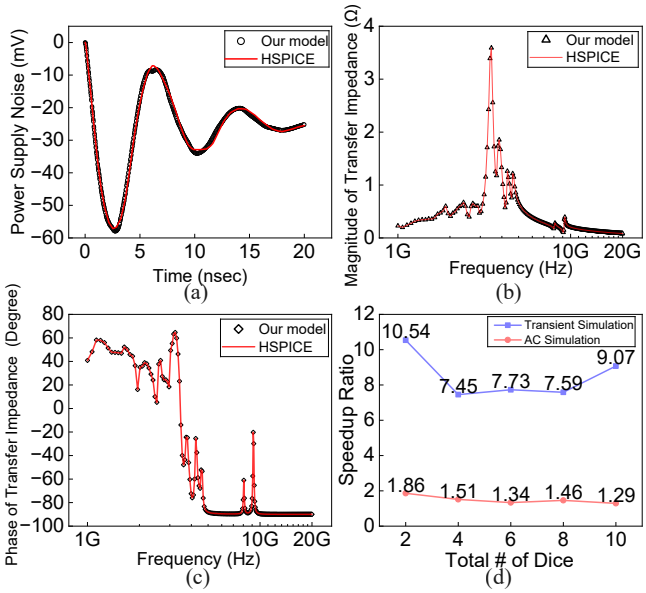

Fig. 3: Comparisons of our model and HSPICE simulation results. (a) Transient simulation results. (b) Magnitude of transfer impedance. (c) Phase of transfer impedance. (d) Speedup ratio.

REFERENCES

[1] K. K. Samanta, "3D/multilayer heterogeneous integration and packaging for next generation applications in millimeter-wave and beyond," in *2017 IEEE MTT-S International Microwave and RF Conference (IMaRC)*, pp. 294–297, 2017.

[2] G. Murali and S. K. Lim, "Heterogeneous 3D ICs: Current status and future directions for physical design technologies," in *2021 Design, Automation & Test in Europe Conference & Exhibition (DATE)*, pp. 146–151, 2021.

[3] Z. Xu, Q. Wu, H. He, and J. J.-Q. Lu, "Electromagnetic-simulation program with integrated circuit emphasis modeling, analysis, and design of 3-D power delivery," *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol. 3, no. 4, pp. 641–652, 2013.

[4] I. P. Vaisband, R. Jakushokas, M. Popovich, A. V. Mezhiba, S. Köse, and E. G. Friedman, *On-chip power delivery and management*. Springer, 2016.

[5] K. Xu and E. G. Friedman, "Grid-based redistribution layers within 3-D power networks," *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol. 11, no. 4, pp. 672–682, 2021.

[6] Y. Zhang and M. S. Bakir, "Integrated thermal and power delivery network co-simulation framework for single-die and multi-die assemblies," *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol. 7, no. 3, pp. 434–443, 2017.

[7] L. Zheng, Y. Zhang, and M. S. Bakir, "Full-chip power supply noise time-domain numerical modeling and analysis for single and stacked ics," *IEEE Transactions on Electron Devices*, vol. 63, no. 3, pp. 1225–1231, 2016.