Transistor Aging and Circuit Reliability at Cryogenic Temperatures

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***Abstract*— The increasing interest in cryogenic circuits is driven by their transformative potential across high-performance computing, medical devices, space exploration, and quantum technologies. Operating transistors at cryogenic temperatures, such as 77 K and below, yields substantial improvements, including increased ON current, reduced OFF current, and enhanced sub-threshold slope. While recent studies have explored device-level reliability at cryogenic temperatures, circuit-level reliability—particularly under bias temperature instability (BTI)—remains underexamined, leaving critical aging mechanisms at these temperatures not well understood. To bridge this gap, we designed and fabricated a customized chip in a commercial HKMG 28 nm technology. The chip integrates several ring oscillator (RO) circuits for precise characterization of accelerated aging effects, enabling evaluation of their impact on performance at cryogenic temperatures. Finally, we project technology degradation in a 10-year future comparing, the achieved wear out between room temperature (298 K) and at 77 K when operating circuits at the nominal voltage, revealing the significant mitigation of BTI aging when operating at affordable cryogenic temperatures.**

1. Introduction

Novel chip applications in cutting-edge markets, like quantum computing, where commercial CMOS chips are used as control or readout interfaces, or the data center industry, focused on high performance applications, are demanding reliable and dependable chips that can operate effectively without performance reduction for prolonged times [1-2]. In this scenario, operating chips at cryogenic temperatures, is not just appealing but transformative, offering substantial increases in ON current, dramatic reductions in OFF current, and significant improvements in sub-threshold slope [3-5]. Moreover, operating at cryogenic temperatures, promise a major reduction of unwanted reliability effects caused by the two major degradation phenomena: bias temperature instability (BTI) [6] and hot carrier degradation (HCD) [7].

The unavoidable degradation of CMOS devices and circuits due to BTI an HCD, can lead to performance deviations, system failures, and compromised data integrity if not thoroughly understood. While transistor-level reliability at cryogenic temperatures has been recently studied [8-10], circuit-level reliability under BTI and HCD remains insufficiently explored, leaving these critical aging mechanisms at cryogenic temperatures poorly understood [11]. To address this gap, a fully customized chip was designed and fabricated using a commercial 28 nm HKMG technology, incorporating several NAND-controlled RO circuits. The versatile design of the chip enabled, for the first time, the accurate evaluation of BTI and HCD accelerated aging in RO circuits, providing a quantitative assessment of CMOS aging effects at cryogenic temperatures.

In this paper, we leverage our RO-array chip, wire bonded to a custom PCB board as shown in Figure 1a, to quantify the impact of voltage-accelerated BTI aging phenomenon in our RO circuits at the cryogenic temperature of 77 K. Moreover, an extensive data set of accelerated BTI aging at room temperature (298 K) is also exploited to compare aging impact from room temperature down to 77 K. To achieve this, various fabricated RO-based arrays were extensively characterized under a wide range of stress voltage conditions at the two temperatures by means of a modified Lakeshore CPX-LVT cryostat shown in Figure 1b. The resulting RO degradations were carefully analyzed and adjusted so unwanted performance deviations due to low stress levels and noise do not obscure the total achieved degradation. The results reveal how cryogenic temperatures significantly suppress the effects of BTI in our RO fabricated circuits.

2. Experimental Setup

All the tests conducted in this work have been gathered using our latest RO-array designed in a 1 × 1 mm chip manufactured in a commercial 28 nm planar technology. The main building blocks of the IC are described hereinbelow.

A. Chip biulding blocks

The developed array occupies an area of 1mm × 160 µm that allows full digital selection to a total of 112 ROs designed with standard threshold voltage (SVT) core devices with fanout 0, distributed over 4 rows and 28 columns.

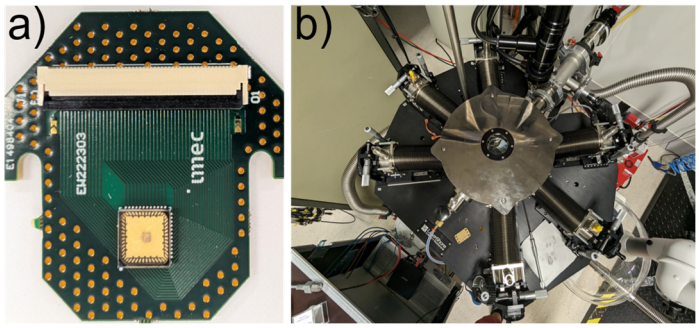

Figure 1. (a) The RO-array chip wire bonded and soldered to a custom PCB and connected to a 48-line break-out box on a modified (b) Lakeshore CPX-LVT cryostat. This setup allows us to program and easily measure our chips, change the sample temperature enabling semi-automated measurements.

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The layout of an RO-array submodule includes replicated unit cells interconnected in a mosaic pattern as shown in Figure 2a. Unit cell selection is facilitated by means of a row and column selection circuitry designed with two-layer shift registers constructed with type D flip-flops. These selection circuitry permits individual or multiple unit cell activation for operation controlled by a 32-bit selection word, i.e., 4-bit for row and 28-bit for column selection, allowing for single or parallel testing. Furthermore, the connection of the unit cell ROs to the biasing paths is achieved through three operation modes which establish a physical connection between the ROs' VDD and the biasing paths via IO transmission gates.

The array is also equipped with individual on-chip Force-and-Sense (F&S) internal paths utilized to mitigate on-chip voltage drop, which are connected to all unit cells of the array for individual stress and measurement biasing [12-13]. Thanks to the versatility of the array to select single or multiple unit cells, different operations can occur simultaneously. For instance, when a unit cell is selected for stress, where the RO is connected to the stress paths, at the same time, another unit cell can be selected for measurement by connecting it to the measure path. Also, parallel stress tests on several ROs can be conducted simultaneously to significantly reduce the total aging test time.

B. *RO unit cell circuitry.*

Each designed RO embedded in its individually controlled unit cell harbors the necessary digital and analog circuitry to set the RO biasing conditions in three different modes: stress (ST) voltages from 0.9 V to 2.5 V, measurement (ME), applied voltage of 0.9 V or standby (SB), applied voltage of 0 V.

As depicted in Figure 2b, each unit cell contains a digital control circuitry unit that can store a 3-bit defined operation mode, i.e., ST, ME or SB for RO operation. Moreover, 4 full transmission gates have been also incorporated for accurate RO bias during aging tests depending on the selected operation mode. In this regard, the voltage applied to the ROs is provided by means of F&S biasing paths that minimize voltage drops. As depicted in Figure 2b, "VST_F" and "VST_S" stands for F&S path of the stress lines while "VME_F" and "VME_S" for the measurement lines of the chip. Finally, the standby voltage of 0 V can be established by means of the VSB pass gate.

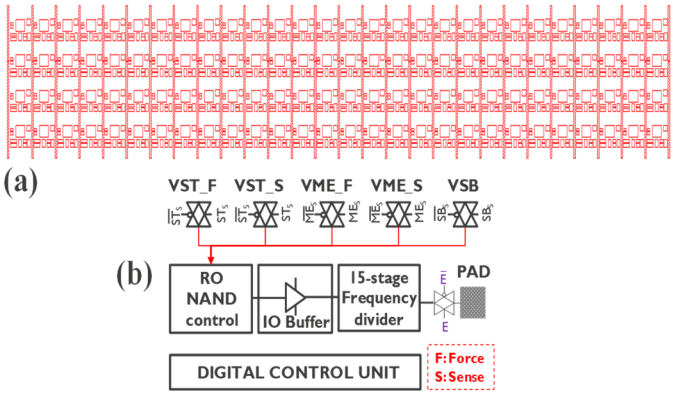

Figure 2. (a) GDS illustration of the RO-array chip including 112 ROs showing the vertical on-chip heater stripes for on-chip temperature aging tests. (b) RO unit cell high level circuit block including the NAND controlled RO an IO buffer to prevent unwanted degradation of the 15-stage frequency divider.

The core of the unit cell contains a single 51-stage RO with its feedback loop operated by a NAND gate that enables toggling the RO oscillation on and off, allowing for both dynamic (closed-loop) and static (open-loop) tests.

Additionally, the RO output is connected to a 15-stage frequency divider, which provides on-chip frequency down-division up to 2^15 or 32,768 times frequency division. To protect the frequency divider from degradation during over-nominal RO voltage stress, a VDDH-to-VDD thick oxide buffer is included between the RO and the frequency divider. As illustrated in Fig. 2b, the output of the frequency divider is routed to external pads for off-chip frequency measurements. Finally, the on-chip F&S paths, as well as the pass gates, have been designed to withstand RO biasing voltages up to 3 V and DC currents up to 3 mA.

C. *Cryogenic evaluation mehtod.*

Our RO-array chip was wire-bonded to a custom PCB designed at imec that grants access to the 24 pads of the chip for both analog and digital operation. For the cryogenic measurements, we employed a modified Lakeshore CPX-LVT cryostat that utilizes liquid helium to achieve the cryogenic temperatures down to 4 K, but also permits establishing room temperature (298 K). With this setup, and together with a custom-made switching matrix, two 2 SMUs from a Keithley 2B2020 system and a Tektronix FCA3103 frequency meter, several RO-array chips were tested with accurate timing precision.

All RO aging tests were conducted using the well-known measurement-stress-measurement (MSM) accelerated aging technique depicted in Figure 3. In this regard, before executing the SM pairs, a fresh RO frequency readout is gathered and will serve as unique RO-frequency reference to later compute frequency shifts (Δfreq.) after stress. After the nominal test, the SM pairs are executed utilizing stress times increased exponentially but maintaining fixed recovery times of 100 s. Finally, a controlled time gap of 100 µs happens between the stress and the measurement phases in our aging experiments. This timing control permits to always have precise control of the MSM sequence which is critical during the study of aging effect CMOS technologies and further modelling of BTI aging phenomenon in our RO circuits [6][13].

In our Stress-Measurement experiments the stress times are increased exponentially starting from 60 ms until 1 ks of accumulated stress time, while keeping constant measurement, a.k.a. recovery, times of 100 s using a sampling rate of 100 µs.

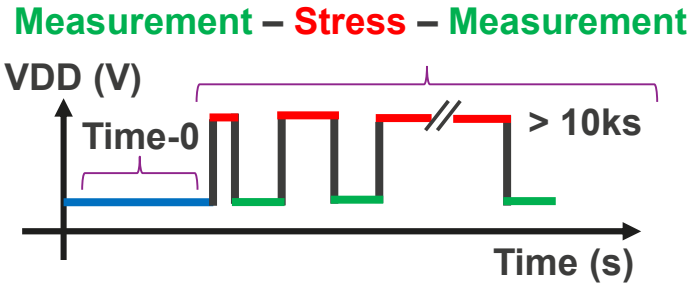

Figure 3. MSM test sequence utilized to stress all ROs: an initial time-zero measurement (M), followed by stress (S) phase, and a subsequent measurement (a.k.a. recovery) test pairs. In the stress phases, the stress times are increased exponentially starting from 60 ms until 1 ks of accumulated stress time, while keeping constant recovery times of 100 s using a sampling rate of 100 µs.

Moreover, the stress voltages chosen for this study are [1.4, 1.6, 1.8, 2.0, 2.2 and 2.4] V tested at room temperature and at the cryogenic temperature of 77 K. This approach allowed us to systematically age the ROs and observe degradation dynamics over a wide range of voltage and temperature stress conditions, ensuring accurate assessment of aging effects in RO circuits.

3. Aging Characterizacion at Cryogenic Temperautres.

The present section will cover the experiments and findings obtained from the reliability tests conducted at room temperature and 77 K in our RO-array chips.

The first step before conducting overvoltage stress tests is to obtain the non-degraded RO oscillation frequencies. Each RO exhibits a unique oscillation frequency due to process variability and device mismatch. This variability arises from the stochastic nature of BTI aging combined with the initial process variability [6]. After the T0 characterization of all the ROs, voltage-accelerated BTI aging tests were conducted with voltages ranging from 1.4 V to 2.4 V at 298 K and 77 K. In this context, Figure 4 shows the ΔFreq (%) of the RO degradation data collected at 77 K during static stress, i.e., when the RO feedback loop is open and BTI aging dominates the circuit degradation.

The aging data shown in Figure 4 correspond to the relative ΔFreq (%) as a function of the accumulated stress time where each ΔFreq symbol corresponds to the very first data point collected 100 µs after removing the stress conditions. This results in a relatively short experimental stress window; however, the collected degradation data prove to be sufficiently accurate, following a power-law dependency with time, i.e., $\Delta Freq\ (\%) = A \times t^n$, as expected in RO aging experiments [12-13].

As clearly shown in Figure 5, at a stress voltage of 1.4 V (blue circles), the accumulated degradation falls below ~0.2%, accompanied by significant noise in the measurements. Due to this low degradation at mid-stress voltage levels and below, it is impossible to obtain meaningful degradation data at the nominal

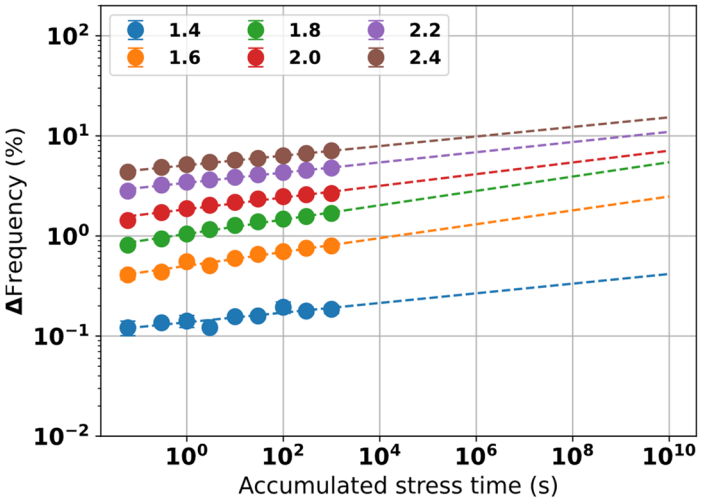

Figure 4. Accelerated frequency degradation of stressed ROs was conducted at a temperature of 77 K. The voltage stress range begins at 1.4 V due to the significantly low degradation observed at lower voltages. Furthermore, power-law extrapolations for each voltage dataset are shown and extended over several decades. Each extrapolation intersects with the three vertical lines, which represent stress durations of 1 month in blue, 1 year in red, and 10 years in black.

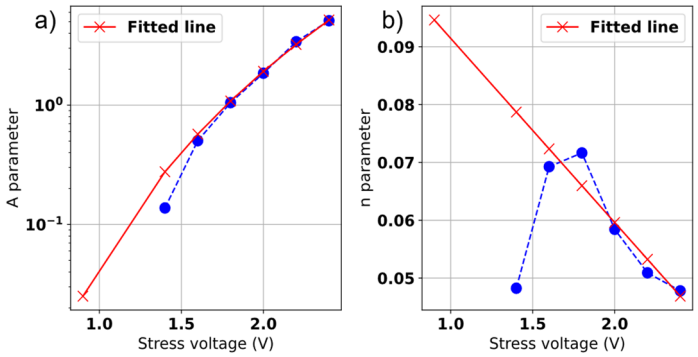

Figure 5. Power-law "A" and "n" parameter fittings for later extrapolation to 0.9 V operating conditions. Due to the significantly low degradation observed at low stress voltages, the A and n parameters are obtained via fitting. As clearly shown in both figures, low degradation and measurement noise prevent direct extraction at the nominal voltage. Therefore, these parameters must be extrapolated, as shown in both figures, using power-law models.

voltage of the technology, i.e., 0.9 V. To address this issue, the scale factor "A" and the time acceleration factor "n" of the power laws obtained in Figure 4, are fitted with power laws as a function of voltage, as shown in Figure 5, to obtain these two parameters for the 0.9 V regular operation voltage.

Figure 5 illustrates how noise and low-level degradation affect the parameter values, while the fittings allow us to retrieve accurate power law parameters extrapolating to the operation voltage of 0.9 V, i.e., A = 0.025 and n = 0.095. Finally, the new power law parameters for all stress voltages are obtained, allowing the degradation achieved at all stress voltages, including nominal, to be reconstructed and projected for accumulated stress times exceeding 30 years, far beyond the 1 ks achieved in our tests. In this regard, Figure 6 shows the reconstructed degradation at the different stress voltages, where the blue crosses reveal the accumulated degradation of 0.13 % when operating at the nominal voltage due to pure BTI projected to happen in 10+ years. Finally, we conducted the same BTI aging experiments at room temperature (298 K) using the same mid-to-high stress voltages.

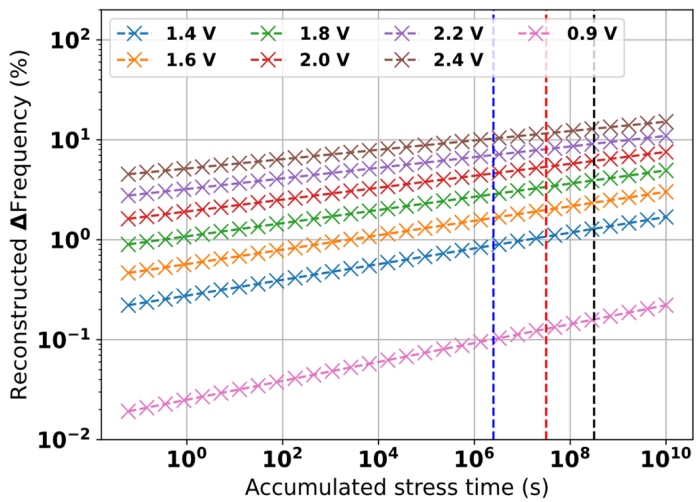

Figure 6. Reconstructed RO degradation data at 77 K using the fitted A and n parameters obtained from the fittings in Figure 5 for all stress voltages including the nominal voltage of 0.9 V. This enables all degradation curves to be extrapolated to more than 10 years of stress time and reveals that after 10 years at 0.9 V, only 0.15% of circuit degradation will occur due to BTI aging.

Additionally, the achievable degradation for stress voltages below 1.4 V was negligible. Therefore, the same power law fitting procedure shown in Figure 5 was utilized to determine the power law parameters A and n for a complete set of data collected at room temperature (298 K). In this context, Figure 7 presents the degradation projections for both temperatures: 298 K (blue crosses) and 77 K (orange crosses). The projection starts at a stress time of 60 ms and extends to an accumulated stress time of more than 10 years.

These degradation projections reveal that, by simply operating the RO circuits at room temperature, the RO degradation due to the BTI aging phenomenon can result in approximately 1% frequency shift, as clearly shown by the blue RO degradation line crossing the red vertical horizon line at 1 year. Figure 6 also demonstrates that operating the circuit at 77 K using, for instance, liquid nitrogen, reduces the accumulated degradation after 1 year of use by one order of magnitude, i.e., from 1% down to 0.1% frequency shift. This result clearly shows that cooling down to affordable cryogenic temperatures, such as 77 K, can achieve a very significant reduction in accumulated degradation, thereby drastically increasing the intended lifetime of circuits and ICs in critical application like quantum computing or high-performance computing.

4. Conclusions

In this work, we present our latest RO-array chip, fabricated using a commercially available 28 nm HKMG planar technology. The array consists of 112-unit cells, each one containing an identically designed Ring-Oscillator circuit with NAND-gate feedback loop control for static and dynamic accelerated aging. The chips were wire-bonded and measured at 298 K and 77 K using a modified Lakeshore cryostat under voltage-accelerated BTI aging conditions. Results from the reliability experiments and degradation projections down to the nominal voltage of the technology, obtained with our proposed method, revealed a significant reduction of one order of magnitude in BTI degradation by operating the circuit at 77 K, such as with liquid nitrogen.

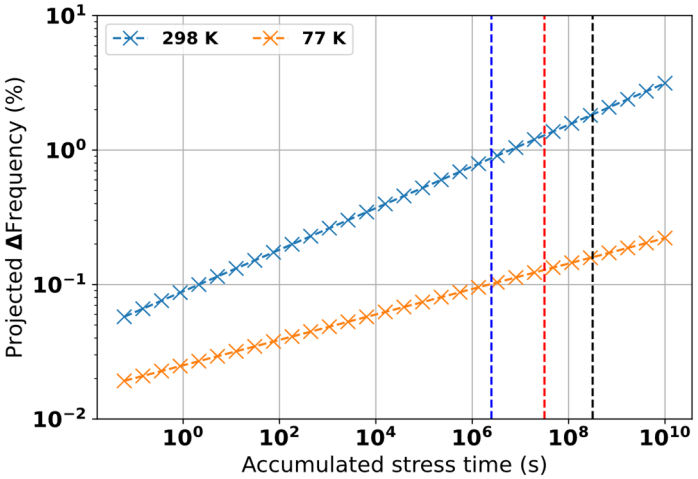

Figure 7. Projected RO frequency shift subjected to BTI aging phenomenon operated at the nominal voltage of 0.9 V at the operation temperature of 298 K and 77 K. The fitted A and n parameters for both temperatures have been obtained from the power law extrapolations. Vertical lines define horizon times of 1 month in blue, 1 year in red and 10 years in black revealing that approximately the degradation relaxes up to one decade simply by cooling at the temperature of 77 k cooling with liquid nitrogen.

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