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Runtime Security Analysis of Monolithic 3D Embedded DRAM with Oxide-Channel Transistor

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***Abstract*—We present the first security and disturbance study of monolithic 3D (M3D) embedded DRAM (eDRAM) with 2T gain cell using oxide-channel transistors. We explore the Rowhammer/Rowpress vulnerabilities on amorphous indium tungsten oxide (IWO) transistors for eDRAM with standalone 2D integration and memory-on-memory M3D integration. In addition, We examine M3D-specific electrical disturbances from memory-on-logic M3D integration. We evaluate IWO eDRAM's susceptibility to these vulnerabilities/disturbances and discuss the potential impact on M3D integration. We examine physical design and architecture strategies for M3D integration of IWO eDRAM. We provide systematic recommendations to inform security strategies for M3D integration and security of IWO eDRAM. Our results show that limiting the minimum vertical interlayer distance to 300 nm reduces vertical disturbances in memory-on-memory M3D integration. In addition, for memory-on-logic M3D integration, we observed that IWO eDRAM's read bitline is sensitive to crosstalk from high-speed switching logic circuits. In conjunction, we show that IWO eDRAM standalone 2D integration is $30\times$ more resilient to Rowhammer than current state-of-the-art memory because the IWO transistor's I_{ON}/I_{OFF} ratio is roughly three orders of magnitude greater than standard memory access transistors.**

I. Introduction & Motivation

Rowhammer is a memory vulnerability that impacts system-level security across a range of memory technologies [1]–[15]. This vulnerability occurs when a malicious actor accesses the same row frequently. These frequent accesses result in memory disturbances (i.e., bit flips) in physically adjacent rows (victim rows). The frequently accessed row(s) are known as aggressor row(s). The minimum number of aggressor accesses to cause bit flips is called "hammer count first" or HC_{first}. The HC_{first} threshold has been decreasing since Rowhammer was first reported (i.e., 139K in 2014, 4.8K in 2020, and 3.2K in 2022) [1], [4], [16]. It is projected that HC_{first} will continue to decrease due to technology scaling. The rowhammer vulnerability has been extensively characterized in DRAM [6]–[15], [17]–[22]. However, Rowmmer disturbances have been shown in other commodity and emerging memory types, e.g., SRAM, flash memory, hard drives, STT-RAM, FeFET, and ReRAM [2], [23]–[27]. However, no prior work has examined the rowhammer disturbance on monolithic 3D (M3D) amorphous indium tungsten oxide (IWO) eDRAM, sequentially integrated on the back-end-of-line (BEOL).

We select the IWO eDRAM cell architecture as our next-generation memory of choice as it offers the best tradeoffs between leakage and access time latency [28]–[30]. This paper provides the first Rowhammer vulnerability analysis of IWO eDRAM for M3D integration. The paper also includes other integration scenarios, i.e., 2D integration. Rowhammer typically flip bits within a 2D integrated memory bank (i.e., layered horizontally). However, 3D integration increases memory density through vertical memory integration [21], [31], [32]. This is enabled by monolithic-interconnect-vias (MIVs).

The IWO eDRAM and IWO transistor have been experimentally demonstrated [30]. A compact model for the IWO transistor has been calibrated using experimental data [28], [30]. This compact model is used to simulate IWO eDRAM. We simulate the Rowhammer vulnerability of monolithic IWO eDRAM in various integration scenarios. As packaging density increases, we show that vertical crosstalk in M3D IWO eDRAM leads to a vertical Rowhammer vulnerability, i.e., Rowhammer across memory layers. We simulate IWO eDRAM memory operations through HSPICE with the OPEN-ROAD ASAP7 PDK (7 nm technology) [33] and IWO transistor compact model [28]. Our simulations consider interconnect parasitics (from ASAP7), and 3D integration for M3D IWO eDRAM [29], [30]. Our results show that a minimum vertical interlayer distance of 300 nm reduces vertical disturbances in memory-on-memory M3D integration. For memory-on-logic M3D integration, we observed that the read bitline is sensitive to crosstalk from high-speed switching logic circuits. In addition, we show that IWO eDRAM standalone 2D integration is 30× more resilient to Rowhammer than current state-of-the-art memory. The contributions are as follows: (1) We present the first Rowhammer and Rowpress vulnerability analysis for M3D IWO eDRAM. (2) We show how integration scenarios contribute to vulnerabilities and disturbances in these memories. (3) We provide systematic recommendations to mitigate disturbances in M3D IWO eDRAM.

The rest of the paper is organized as follows. Section II provides background material. Section III provides our simulation setup and methodology. Section IV presents the results and analysis. Section V presents the conclusion.

II. Background

A. Memory Disturbances & Rowhammer

Memory disturbances have been widely studied in commodity and emerging memory types such as SRAM, flash memory,

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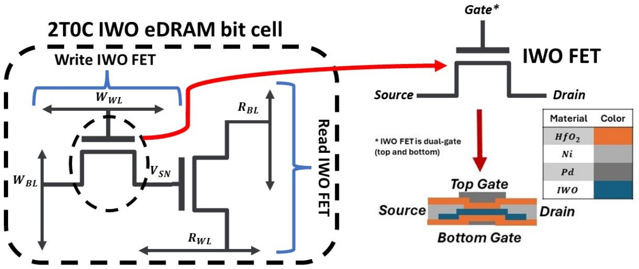

Fig. 1. Example of monolithic IWO eDRAM cell and IWO FET device breakdown [30].

hard drives, STT-RAM, ReRAM, and DRAM [2], [23]–[25]. SRAM has faced scalability issues due to soft errors [34]. In flash memory, frequent read and write operations have shown data integrity loss [35] and hard errors [36], respectively. Hard drives face periodic disturbance issues impacting long-term data stability [37]. STT-RAM are vulnerable at high memory densities [26]. In ReRAM and FeFET memory, area-efficient cell architecture types are sensitive to voltage and temperature — leading to data integrity loss [24], [25], [38], [39]. However, the DRAM memory disturbance (Rowhammer) has more severe implications such as system-level security breaches and privacy loss [1]–[4].

Rowhammer has been widely studied due to its severity on real systems. [19] shows that the underlying parasitic enables charge recombination (sub-threshold leakage) at victim cells due to neighboring aggressor cells and corresponding bitlines. Thus, longer precharging periods leads to a greater impact on victim cells. Furthermore, Rowhammer increases by up to 36% when the aggressor WL stays active longer or when the precharge occurs for a longer period [17]. In conjuction, [17], [18], [20] show that an increase in temperature can induce more carrier movement to the victim cells and victim interconnects (i.e., victim WL) and thus decrease HC_{first}. Hence, higher temperatures and longer aggressor WL activation periods may increase Rowhammer vulnerability, as corroborated in a chip study [17], [40]. This insight has been published as a Rowhammer variant — Rowpress [40]. In Rowpress [40], one memory row access with an extraneous WL activation duration can flip bits in commodity DRAM. We consider the Rowhammer and Rowpress vulnerabilities for M3D IWO eDRAM memory.

TABLE I
OXIDE FET COMPARISON.

Oxide FET [30]	$I_{ON}@\Delta V_{GS} = 1.8V(\frac{\mu A}{\mu m})$
IWO	1.2×10^2
ITO	0.5×10^2
IGZO	3×10^1

TABLE II
IWO EDRAM PROPERTIES.

Property [28]–[30]	Attribute
Access Time (ns)	10
Destructive Read	No
Density ($\frac{Mb}{mm^2}$)	180
Fabrication Process	BEOL

B. Indium Tungsten-doped Oxide eDRAM

The IWO eDRAM cells consist of two Indium Tungsten-doped Oxide (IWO) FETs to establish a “two transistor, zero capacitor” memory bit cell (e.g., 2T0C). An example is described in Figure 1. Compared with other next-generation devices for monolithic memory (e.g., IGZO FET, MoS_2 MOSFET, ITO FET), IWO FETs have superior performance [30]; see Table II-A. IWO eDRAM is significant as an emerging technology due to the properties listed in Table II. In conjunction, IWO FETs for 2T0C eDRAM have competitive retention and access time when compared with state-of-the-art volatile memory [30]. Unlike its 1T1C DRAM counterpart, IWO eDRAM cells do not destroy its memory content during a read operation [1], [17], [30]. IWO eDRAM provides faster access times compared to traditional DRAM [21], [30], making it suitable for processors and high-performance computing systems as an L3 cache candidate instead of SRAM [41]. In addition, IWO eDRAM is fabricated with a sole back-end-of-the-line (BEOL) process [30]. Hence, IWO eDRAM can embed more memory on a chip monolithically, reducing the need for external memory, improving overall system performance, and reducing latency. These attributes make IWO eDRAM suitable for compute-intensive applications.

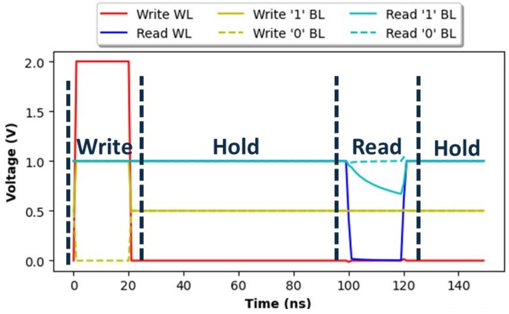

Fig. 2. Example waveform for IWO eDRAM memory operation.

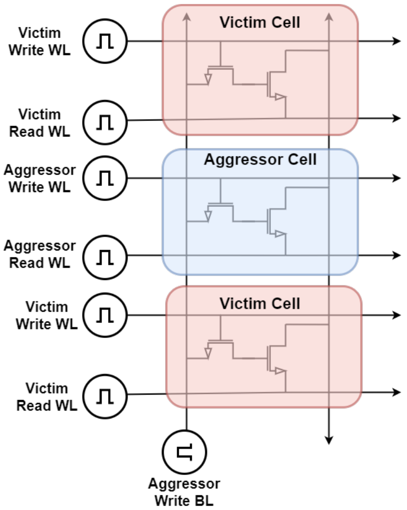

Fig. 3. SPICE schematic of the horizontal Rowhammer vulnerability analysis.

III. SIMULATION SETUP & METHODOLOGY

A. General Setup

We use IWO eDRAM derived from experimental data and calibrated TCAD simulations [29], [30]. The read, write, and hold operations are driven by peripheral circuits (pass gates, sense amplifiers, and row decoders). A typical read, write, and hold waveform is shown in Figure 2. We use the timing characteristics of commodity memory to inform the pulse width of memory operations in this study [42].

Note that we use voltage pulses to represent control signals for the pass gates and to act as driving pulses for the read

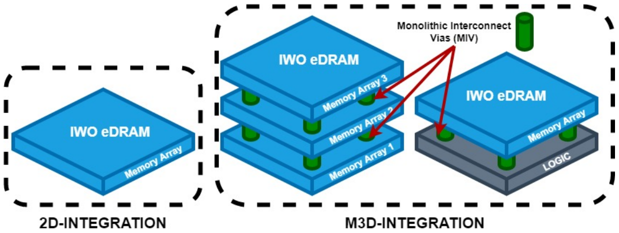

Fig. 4. Two integration methods for IWO eDRAM.

TABLE III
INTERCONNECT GEOMETRY FOR OPENROAD ASAP7 PDK [33]. MEASUREMENTS ARE IN nm. ASPECT RATIO IS 2:1.

Layer	Via	Width	Layer Pitch	Via Pitch
M1-M3	VIA0-VIA3	18	36	25
M4-5	VIA4-VIA5	24	48	34
M6-M7	VIA6-VIA7	32	64	45
M8-M9	VIA8	40	80	57

and write operations (i.e., W_{WL}, W_{BL}, R_{WL}). The schematic of our HSPICE setup is described in Figure 3. Note that we use the ASAP7 PDK for the pass gate and its interconnect geometry at an advanced node (7 nm) [33]. We utilize the transistors that offer lower subthreshold leakage for our pass gate design (i.e., *nmos_sram*) [33]. In memory design, a small capacitance is added to the bitline (BL) for stability, noise reduction, and functional correctness [43]. A $5fF$ capacitor is attached to the read bitline (R_{BL}) for functionally correct read operations and faster pre-charging operations [28], [43].

B. Device and Interconnect Parasitics

We insert parasitics into our simulation to represent coupling capacitance (crosstalk) and wire resistance [43]. The parasitics are lumped Π models based on the stated interconnect geometry [33], [43]. Equation (1) represents capacitive crosstalk as discussed in prior Rowhammer studies [18], [20]. Equation (2) represents the fringe capacitance crosstalk. Parameter d in Equation (1)/(2) represents interconnect distance. Parameters T and L in Equation (2) represent interconnect thickness and length. Parameter A in Equation (1)/(3) represents the area of the two-facing metal interconnects/cross-section of the metal interconnect. In Equation (1), ϵ_{SiO_2} is the permittivity of silicon dioxide ($3.9\epsilon_0$) [44]. In Equation (3), ρ_{Cu} is the resistivity of Cu ($1.7 * 10^{-8}\Omega m$) [44].

$$C_{coupling} = \epsilon_{SiO_2} \frac{A_{facing}}{d} \tag{1}$$

$$C_{fringe} = \epsilon_{SiO_2} \ln{(1 + \frac{T}{d})} \times L \tag{2}$$

$$R_{wire} = \rho_{Cu} \frac{l}{A_{cross-section}} \tag{3}$$

By computing and inserting the resistance (R) and capacitance (C) values, we can incorporate the relative parasitic mechanisms that induce Rowhammer in our SPICE framework. We assume that SiO_2 is used as the insulator [44]. In addition, we presume Cu metal for the wordline and bitline interconnects, as specified by the ASAP7 PDK [33]. We utilize the interconnect geometry as defined by ASAP7 PDK (Table III) [33]. Note that the fin width and pitch are 7nm and 27 nm [33]. The gate width and pitch are 20 nm and 54 nm [33].

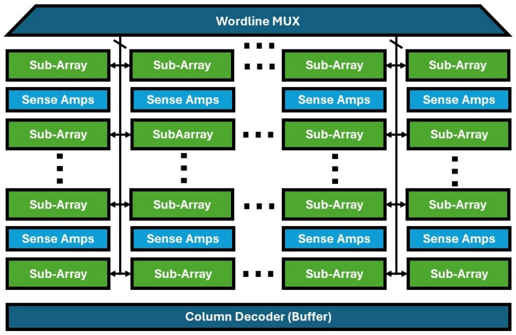

Fig. 5. General memory layout with bitline and wordline partitions.

To simulate IWO eDRAM and the vertical parasitics for vertical Rowhammer [45], [46], we consider memory placement and packaging density, i.e., vertical interlayer pitch. We consider stand-alone memory (2D integration), M3D memory-on-memory, and M3D memory-on-logic. An example is shown in Figure 4. We use recent analysis of MIVs to inform the vertical interlayer distance for M3D IWO eDRAM simulation [46]. Vertical Rowhammer for M3D integration considers vertical crosstalk and fringe capacitance coupling from relative interconnects [33], [43], [46].

C. Optimization Techniques

To model practical memory architectures, we consider the layout and architectural performance optimizations described in [47], [48]. These performance optimizations make use of interconnect partitioning to reduce power and memory access time. They introduce sub-array/sub-bank level parallelism for memory accesses [47]. This is done by using more peripheral circuits (i.e., sense amplifiers) that divide the bitline into smaller interconnects. Power optimizations are also considered; the wordline is partitioned to lower activation energy [48]. By reducing wordline length, memory architects can increase power efficiency [47], [48]. We consider subarray/sub-bank partitioning to achieve shorter interconnects between memory cells. Hence, without loss of generality, we consider an IWO eDRAM sub-array of size 128x128. Figure 5 illustrates the overall memory architecture.

D. IWO eDRAM Power, Performance, Area

We follow the voltage characteristics in [28], [29] for IWO eDRAM memory operations. Note that the write-to-read device sizing ratio impacts the power, performance, and area. We perform a write, hold, and read operation following the waveform in Figure 2. We sweep the write-to-read device sizing to determine the resulting IWO eDRAM cell area, write/read performance, and write/read energy. The results are shown in Figure 6. In addition, we consider the IWO eDRAM voltage level and R_{BL} swing. We select a write device width of 0.018 µm with a write-to-read size ratio of 1:10. The sense amplifier is fully custom to detect a voltage swing of 100 mV to distinguish between logic ‘1’ and logic ‘0’. From our selected configuration, we sweep the IWO eDRAM bit cell

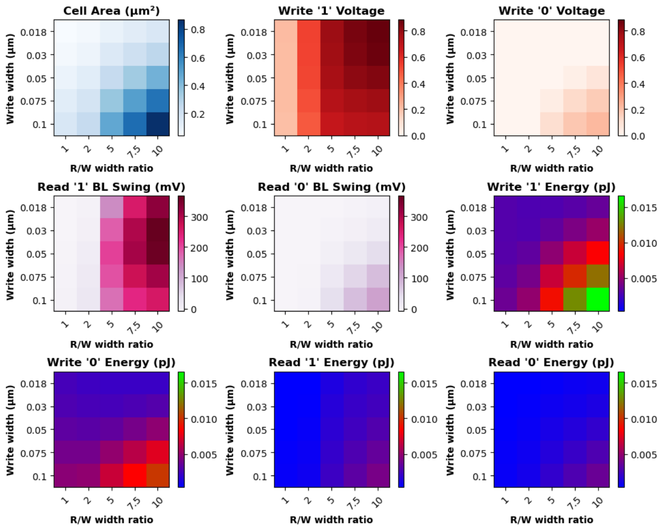

Fig. 6. IWO eDRAM cell area under various device parameters.

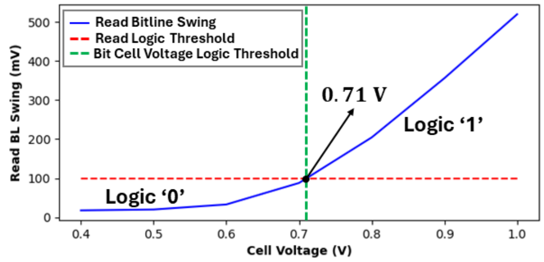

Fig. 7. R_{BL} swing from IWO eDRAM cell voltage. In this study, the IWO eDRAM logic threshold is 0.71 V to distinguish between logic '1' and '0', i.e., cell voltage above (below) 0.71 V will indicate logic '1' ('0').

voltage level during a read operation and capture the R_{BL} swing. Figure 7 presents the results. The cell voltage threshold to distinguish between logic '1' and logic '0' is 0.71 V.

E. Vulnerabilities

We consider the memory-specific disturbances Rowhammer and Rowpress. Each disturbance is based on the orientation of memory integration, i.e., horizontal Rowhammer/Rowpress for 2D integration, and vertical Rowhammer/Rowpress for M3D integration. A Rowhammer attack may be executed in different ways based on memory access frequency, timing, distribution, randomness, and location [21]. For example, a single-sided Rowhammer attack is carried out by accessing the same location in memory frequently HC_{first} times to achieve bit flips. A double-sided Rowhammer and other Rowhammer frameworks (TRRespass, BLACKSMITH) require interlacing single-sided Rowhammer attacks to achieve bit flips. Half-double requires a low and high-frequency aggressor to achieve bit flips from further away [21]. Feinting utilizes high-frequency memory accesses at certain periods to achieve its attack [21]. Essentially, Rowhammer attack methods require frequent access to the same aggressor row to achieve bit flips [21]. Thus, we use a single-sided Rowhammer aggressor to act as the Rowhammer base case.

TABLE IV
AGGRESSOR AND VICTIM CELL INITIAL STATES. EACH CASE FOR ALL SCENARIOS IS DENOTED BY THE COLOR DEPICTED IN THE TABLE.

Aggressor State	Victim State	Color	Case
1	0	🔴	1
1	1	⚫	2
0	0	🔵	3
0	1	🟢	4

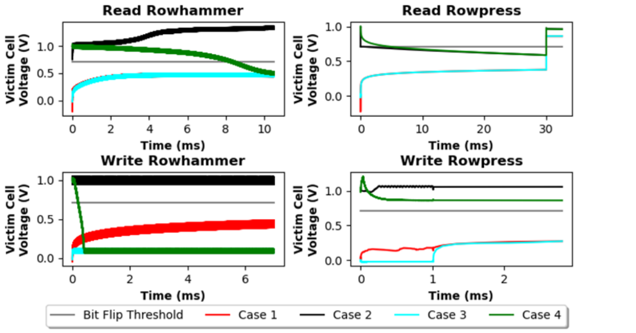

Fig. 8. Disturbances for IWO eDRAM in 2D integration. Results for horizontal Rowhammer and Rowpress are shown. Read and write versions of each disturbance are considered.

Note that Rowpress is fundamentally different from the original concept of "frequently accessed row". Rowpress occurs when memory requests continually access the same row to force longer wordline activation. The continuously-on wordline stores the requested data in a row buffer to enable fast memory access. However, this enables the underlying Rowhammer mechanisms to flip bits during extended wordline access periods. It has been shown that Rowpress can flip bits in one access with enough time, i.e., 30 ms. Hence, evaluating IWO eDRAM for Rowpress will inform system-level architecture decisions for M3D-integrated systems. Note that we sweep various disturbance scenarios from the aggressor type (1/0) against the victim type (1/0). The specific disturbance type is color-coded as seen in Table IV. In addition, we consider memory-on-logic M3D integration. In this integration scenario, we consider how vertical crosstalk from high-speed logic circuits may cause data corruption at ultra-dense vertical integration, i.e., sub-300 nm interlayer distance.

IV. RESULTS & ANALYSIS

A. Standalone 2D-Integrated Memory

In this first case study, we consider standalone IWO eDRAM banks, similar to that of DRAM DIMMs. To fully characterize horizontal Rowhammer and Rowpress, we consider read and write versions of each disturbance. For example, frequent read/write operations will lead to read/write specific Rowhammer disturbances. In addition, an extended read/write operation will lead to a read/write Rowpress disturbance.

We execute 150K operations to characterize the horizontal Rowhammer/Rowpress vulnerability and show the resultant change in victim cell voltage in Figure 8. For read-based (write-based) Rowhammer, the HC_{first} of IWO eDRAM is 130K (1.37K) for flipping bits $1 \rightarrow 0$. We were unable to flip bits from $0 \rightarrow 1$ as the increased victim voltage saturated with the leakage voltage. However, the HC_{first} of write-based Rowhammer is directly related to the hold duration following a write operation. As more hold latency is introduced, the write operation suffers from slowdown. However, the attack effort

TABLE V
THE IMPACT OF ADDITIONAL HOLD LATENCY BETWEEN WRITES ON HORIZONTAL WRITE-BASED ROWHAMMER (BIT FLIP 1 → 0).

Write slowdown	HC_{first}	Vic. Volt. after 10K hammers
1.0×	1.37K	81.5 mV
2.44×	1.44K	600.8 mV
3.33×	144K	836.4 mV

TABLE VI
HORIZONTAL READ-BASED ROWHAMMER HC_{first} OF IWO EDRAM COMPARED TO STATE OF ART DRAM MEMORY.

Memory Type	HC_{first}
DDR4 [4]	10.0K
LPDDR4 [4]	4.8K
DDR5 [16]	3.2K
OPENROAD 1T1C DRAM [21]	4.1K
IWO eDRAM	130K

to flip bits increases drastically as seen in Table V. When compared with state-of-the-art 2D-integrated memory, i.e., DRAM, IWO eDRAM is more resilient against Rowhammer. In recent studies, the HC_{first} of DDR4, LPDDR4, DDR5, and an OPENROAD version of 1T1C DRAM are 10K, 4.8K, 3.2K, and 4.1K, respectively [4], [21]. However, for 2D-integrated IWO eDRAM — the HC_{first} is shown to be 130K which is roughly 30× greater than state-of-the-art in-market memory. Note that current in-market DRAM uses saddle-fin FETs as the memory access device [49]. We compare the I_{ON}/I_{OFF} ratio of OPENROAD memory finFETs, and saddle finFETs with IWO FETs in Table VII. IWO FETs I_{ON}/I_{OFF} ratio is almost 3 (5) orders of magnitude greater than saddle (OPENROAD memory) finFETs. We believe the I_{ON}/I_{OFF} ratio difference is what makes IWO eDRAM so resilient to Rowhammer.

We also consider the Rowpress disturbance in our characterization. Note that a 30 ms for the Rowpress disturbance is the longest press time achievable. The results are presented in Figure 8. The write Rowpress was not able to flip bits during its attack. Note that write-based Rowpress attacks lead to an initial victim cell voltage change in the first millisecond of the vulnerability. After this initial 1 ms press, extending the press duration did not lead to further victim voltage cell changes. However, the read Rowpress was successfully able to flip bits from 0 → 1 in one access. While the read Rowpress was not able to flip bits 1 → 0, the read Rowpress was able to force a logic inversion during the read operation. In total, Rowpress-type disturbances in IWO eDRAM can occur due to extended wordline accesses, which are made possible by the row buffer through continuous memory access. The row buffer is used to further extend a wordline access to ensure quick memory access. While the row buffer can enhance performance, it introduces the risk of disturbances. To prevent Rowpress in this emerging technology, we recommend that designers either avoid using this technique or integrate the row buffer in a way that does not excessively extend memory wordline activation.

B. Memory-on-Memory: M3D Integration

In our second case study, we consider IWO eDRAM banks as M3D-integrated memory, i.e., memory-on-memory.

TABLE VII
I_{ON}/I_{OFF} RATIO OF IWO FET COMPARED TO STATE-OF-THE-ART MEMORY ACCESS DEVICES.

Memory-Access Device (Memory Type)	I_{ON}/I_{OFF}
Saddle-FinFET (1T1C DRAM) [49]	1.6×10^9
OPENROAD Memory FinFET (1T1C DRAM) [33]	2.8×10^7
IWO FET (2T0C IWO eDRAM) [30]	1×10^{12}

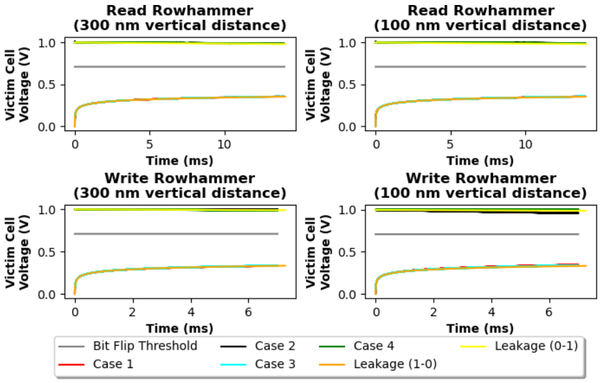

Fig. 9. 3D Monolithic Memory-on-Memory integration. Vertical Rowhammer Read and Write disturbances.

Note that current 3D memory (HBM) is layered memory-on-memory based on through-silicon-vias (TSVs). As IWO eDRAM is fabricated with a BEOL fabrication process based on monolithic inter-layer vias (MIVs). We consider MIV-based integration of memory layers in a single monolithic package (i.e., metal layer 1 holds IWO eDRAM bank 0, metal layer 2 holds IWO eDRAM bank 1, etc.). We consider the vertical versions of Rowhammer and Rowpress. To fully characterize these vertical disturbances, we consider various vertical distances between aggressor and victim. For conciseness, we focus our vertical disturbances at ultra-dense vertical integration, i.e., sub-300 nm. In addition, we consider read and write versions of Rowhammer/Rowpress.

We execute 200K operations to characterize the vertical Rowhammer vulnerability and show the resultant change in victim cell voltage in Figure 9. To verify the victim cell voltage loss over time, we directly compare our results with IWO eDRAM bit cell leakage. We discovered that only very small vertical distances (100 nm) resulted in successful outpacing of inherent bit cell leakage for the Rowhammer vulnerability (write, for bit flips 1 → 0 only). For M3D-DRAM, the estimated HC_{first} for vertical Rowhammer is 250K for vertical interlayer distances of 1795 nm [21]. For IWO eDRAM, the vertical Rowhammer estimated HC_{first} is 700K for a vertical interlayer distance of 100 nm. Therefore, IWO eDRAM offers 2.8× more resilience against vertical Rowhammer than state-of-the-art M3D-integrated DRAM at 17.95× higher memory density. Note that as the vertical distance increases (e.g., to 300 nm), the disturbance is not seen and the victim cell voltage change is similar to that of inherent bit cell leakage.

We also consider the vertical Rowpress. We execute a 30 ms press as the longest press time achievable [40]. The results are shown in Figure 10. We compare the victim voltage change to the voltage change caused by leakage to ensure that vertical Rowpress is successful. While it was successfully able to flip

TABLE VIII
VERTICAL WRITE-BASED ROWHAMMER ESTIMATED HC_{first} OF IWO eDRAM COMPARED WITH STATE-OF-THE-ART M3D DRAM STUDIES.

Memory Type	HC_{first}	Ver. distance
OPENROAD 1T1C M3D DRAM [21]	250K	1795 nm
2T0C IWO eDRAM	700K	100 nm

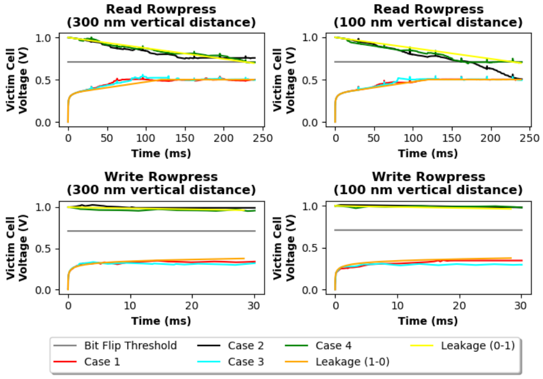

Fig. 10. 3D Monolithic Memory-on-Memory integration. Vertical RowPress Read and Write disturbances.

bits 1 → 0 at tighter interlayer distances (100 nm), these pressed bit flips only occurred after five read Rowpresses at maximum duration (i.e., 30 ms per press).

Volatile memory cell lifespan has been standardized through JEDEC's refresh window of 64/32 ms for DDR4/DDR5 [16], [21]. Note that if IWO eDRAM adopts a similar refresh specification, then vertical Rowpress would be infeasible. However, if IWO eDRAM attempts to enable a longer cell lifespan, then vertical Rowpress is feasible (30& reduction to cell lifespan). Once again, the row buffer is used to further extend a wordline access for quick memory access. The technique can enhance performance, but introduces the risk of disturbances as shown. To prevent Rowpress, we advise designers either avoid using this technique or integrate the the row buffer to prevent extended wordline activations in memory.

C. Memory-on-Logic: M3D Integration

In our third case study, we consider IWO eDRAM banks as M3D integrated memory on top of logic, i.e., memory-on-logic. The electrical disturbance we characterize is crosstalk from logic onto memory interconnects. We utilized a 500 MHz switching circuit, i.e., a ring oscillator with trigger logic, to cause crosstalk to the IWO eDRAM interconnects. A small time duration of crosstalk (almost 100 ns) is compared with an extended period of crosstalk (more than 1 ms). The results are shown in Figure 11. The noise from logic impacts the victim cell. In the left subplot of Figure 11, We do not observe victim cell changes for short burst of switching (within ns). In the right subplot of Figure 11, we extend switching periods to several milliseconds of consistent switching at 500 MHz and observe bit flips from 1 → 0. We sweep the crosstalk on each impacted IWO eDRAM interconnect, i.e., $W_{WL}, W_{BL}, R_{WL}, R_{BL}$, to observe which interconnect is vulnerable to extended crosstalk from logic. We denote the maximum peak-to-peak noise observed on each memory interconnect in Table IX. When vertical logic crosstalk is introduced to memory interconnects W_{WL}, W_{BL}, and R_{WL}, we do not observe any changes to the victim cell state and the relative peak-2-peak noise remains small. However, R_{BL} is found to oscillate and capture more noise from the crosstalk. We conclude that this disturbance is derived from the R_{BL} capacitance which is used for functional correctness and faster pre-charging. Enabling capacitance on the bitlines is a normal part of memory design [43]. In the case of M3D memory-on-logic, this bitline capacitance can lead to disturbances due to crosstalk. Hence, we propose in future work that vertical guard rings may be explored to protect sensitive parts of IWO eDRAM memory operations for monolithic integration.

TABLE IX
PEAK-TO-PEAK NOISE ON MEMORY INTERCONNECT FROM VERTICAL LOGIC CROSSTALK.

Impacted Interconnect	Crosstalk Source	
	W_{WLBL}, W_{BL}, R_{WL}	R_{BL}
W_{WL}	300 nV	4 mV
W_{BL}	200 nV	4 mV
R_{WL}	10 nV	10 mV
R_{BL}	4 μV	250 mV
Bit Flip?	No	Yes

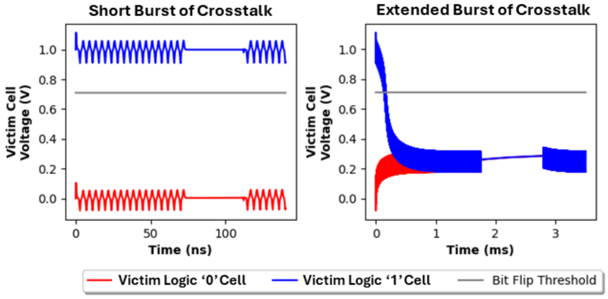

Fig. 11. 3D Monolithic Memory-on-Logic integration, and crosstalk from high-frequency switching logic interconnects to memory interconnect. The impact of crosstalk to victim cell voltage is shown for a short period of time (left subplot) versus an extended period of time (right subplot).

V. CONCLUSION

As memory technologies evolve, emerging monolithic-3D (M3D) memory types, such as IWO eDRAM, face the challenge of disturbances and vulnerabilities. We have presented the first security and disturbance study of monolithic 3D (M3D) embedded DRAM (eDRAM) with 2T gain cells using oxide-channel transistors. This paper explores the Rowhammer and Rowpress vulnerabilties on IWO eDRAM with standalone 2D integration and memory-on-memory M3D integration. In conjuction, we have examined the impact of crosstalk from memory-on-logic M3D integration. Our results show that limiting monolithic interlayer distance to ≥ 300 nm reduces the observed Rowhammer and Rowpress vulnerabilties in memory-on-memory M3D integration and that the read bitline is senstive to crosstalk noise for memory-on-logic M3D integration. In addition, we have demonstrated that IWO eDRAM with standalone 2D-integration is 30× more resilient to Rowhammer than current state-of-the-art memory because the I_{ON}/I_{OFF} ratio is three orders of magnitude greater than standard memory access devices.

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