Voronoi Diagram-based Multiple Power/Ground Plane Generation on Redistribution Layers in 3D ICs

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ABSTRACT

In three-dimensional integrated circuits, the interconnection design among chiplets on redistribution layers (RDLs) is crucial for achieving high-performance computing systems. To optimize the inter-chip connections, most of the previous works focused on automatic signal net routing and pin assignment. The power/ground plane generation, is still a manual and time-consuming task, especially when generating the power planes of more than ten power supplies on a limited number of RDLs. This paper proposes a novel Voronoi diagram-based multiple power/ground plane generation methodology that simultaneously optimizes the power/ground planes of all power/ground nets by utilizing the white space of given RDLs, while considering the signal routing blockages, power integrity, and complex design rules. Experimental results show that the proposed approach can achieve not only optimal area utilization but also the best cross-layer power integrity in terms of the total number of redundant vias.

KEYWORDS

3D-IC, RDL, redistribution layer, routing, power plane, power integrity, redundant via

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1 INTRODUCTION

In advanced packing technologies, or heterogeneous integration of three-dimensional integrated circuits (3D ICs), the interposer, which consists of several redistribution layers (RDLs), is the medium to deliver massive power supplies and a large number of signals among different chiplets. Compared with traditional printed circuit boards (PCBs), RDLs offer higher I/O density, shorter interconnections, and better electronic characteristics, resulting in high-performance computation [1, 2].

As the number of power supplies may be much more than the number of RDLs in modern 3D ICs, multiple power/ground nets usually share common RDLs together with other signal nets. Different from the mesh [3], tree [4], stripe [5], and strap [6] structures of the intra-chip power delivery network, the inter-chip power nets in 3D ICs usually form irregular areas, or power planes, on each RDL. When generating the power planes of each power net on different RDLs, it is essential to enlarge the power plane area and the number of redundant vias for reducing IR-drop, mitigating electromigration, and enhancing power integrity.

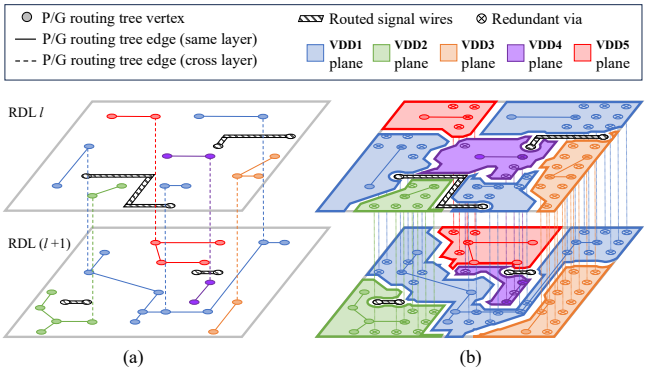

Figure 1: Simultaneous power and signal routing on RDLs and power plane generation. (a) An RDL routing instance, including the routing trees of five power nets, VDD1, VDD2, VDD3, VDD4, and VDD5, and routed signal wires, on two adjacent RDLs. (b) The optimal power planes of each power net resulting from the power routing trees.

Fig. 1 illustrates a 3D-IC RDL routing instance containing both power and signal nets. First of all, the global routing for both power and signal nets must be simultaneously performed in order to ensure the routability of not only signal nets but also power nets. After obtaining the global routing trees, the detailed routing for all signal nets is then executed, followed by power plane generation for the rest power nets. Fig. 1(a) shows the global routing trees of all power nets resulting from simultaneous global routing for both power and signal nets. The routed wires and vias after detailed routing for all signal nets are also highlighted in Fig. 1(a). Based on the global routing trees of all power nets and the obstacles of signal wires and vias, Fig. 1(b) further demonstrates the optimal power planes, which maximizes both the space utilization of each RDL and the number of redundant vias between the power planes of the same power net on adjacent RDLs, leading to better power integrity.

1.1 Related Works

Although the RDL routing and pin assignment problems has been extensively studied in the literature [7–10], all these works only focused on interconnection optimization for signal nets. None of them discussed about power delivery issues with an increasing number of power supplies and power domains in modern 3D ICs. Consequently, creating power planes on RDLs is still a manual and time-consuming task, and the automatic power

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plane generation and optimization for multiple power nets on RDLs in 3D ICs remains an open problem.

Other recent works [11, 12] focused on PCB power network layout synthesis. Bairamkulov *et al.* [11] presented a power routing tool based on a graph-search algorithm. They further apply the simulated annealing (SA) algorithm to reduce the impedance of the power network by dilation and erosion operations. Instead of applying the graph-search algoirthm and SA, Liao *et al.* [12] proposed to use the genetic optimizer and multi-layer perception (GOMLP) for power plane generation on PCBs. Their objective is to minimize the total number of power plane islands in order to ensure the connectivity of each power net.

We observe some disadvantages of the previous works.

- Most of the problem formulations in the previous works routes power nets and signal nets separately. Such formulation may cause routability issues of either power nets or signal nets. Although some signal routing methods could be applied to power net routing, the routing styles are quite different.
- Power integrity is crucial for each power distribution network. The previous works mainly focus on reducing the resistance or impedance of each power plane on one single layer. They do not consider cross-layer power integrity optimization among the power planes of each power net on any two adjacent layers.
- Last but not least, different from PCB design, the sources (fan-in pads/bumps) and sinks (fan-out pads/bumps) of each power net in a 3D IC are usually on the opposite sides of the interposer. The power planes of a power net may be distributed on all RDLs, and different power nets may compete for the routing resources on each RDL. Consequently, the problem of power plane generation on RDLs in 3D ICs is even more difficult than that on PCBs.

1.2 Our Contributions

The significant contributions of this paper can be summarized in the following:

- To the best of our knowledge, this is the *first* work in the literature that addresses the power plane generation problem in modern 3D ICs, which is even more sophisticated than that in conventional PCBs, considering the routing resource competition among different power nets on each RDL and cross-layer power integrity of each power net.
- Different from the previous works which only focused on routing either signal nets or power nets, we present the *first* problem formulation in the literature for multiple power plane generation in 3D ICs that guarantees the routability of both signal nets and power nets.
- Based on the presented problem formulation, we introduce the *first* Voronoi diagram-based power plane generation method to achieve balanced power plane distribution on each RDL according to the global routing trees of all power nets, while maximizing space utilization under design rule constraints.
- We further refine the power planes on each RDL resulting from the Voronoi diagram by considering signal wires and vias as obstacles, and optimize the cross-layer power planes with more redundant vias for better power integrity.
- Based on the industry benchmarks with up to fifteen power nets on four RDLs in 3D ICs, our experimental results show that the power planes generated by the proposed method can achieve significant improvement on cross-layer power integrity in terms of the total number of redundant vias, compared with the manual approach and the latest work for PCBs.

The rest of this paper is organized as follows: Section 2 presents the problem formulation. Sections 3–6 detail the proposed flow and algorithms.

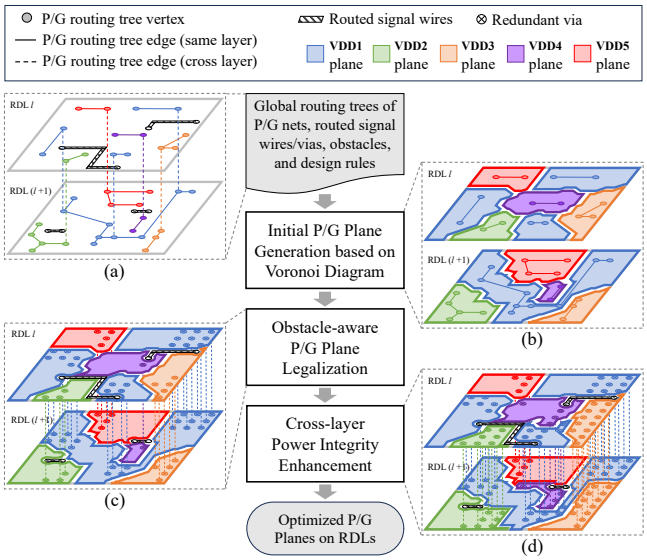

Figure 2: The proposed algorithm flow, and the corresponding examples at each stage. (a) The problem input, including the power routing trees and the obstacles. (b) The initial power planes of different power nets resulting from the power routing trees while ignoring obstacles. (c) The refined power planes with the consideration of obstacles, where the number of redundant vias is not optimal. (d) The optimal power planes which maximizes cross-layer redundant vias for power integrity enhancement.

Section 7 reports the experimental results, and finally section 8 concludes this work.

2 PROBLEM FORMULATION

The *obstacle-avoiding multiple redistribution layer routing problem* has been well formulated and solved in [8]: Given a set of RDLs, a set of I/O pads, a set of bump pads, a set of obstacles, a set of unified-assignment netlists, and RDL design rules, connect all the netlists such that the routability is maximized, the total wirelength is minimized, and all design rules are satisfied. Although such formulation can also simultaneously route the power nets in addition to the signal nets, it does not generate power planes for the routed power nets on RDLs. Therefore, we shall further define the RDL power plane generation problem as follows:

Problem 1. ***Obstacle-Avoiding Multiple Redistribution Layer Power Plane Generation****: Given a set of RDLs, a set of obstacles including routed signal wires and vias, RDL design rules, and a set of global routing trees of all power nets, create all the power/ground planes such that the area utilization is maximized, the cross-layer power integrity (i.e. total via numbers) is maximized, and all design rules are satisfied.*

Based on the problem definition and formulation, Fig. 1(a) gives an example of the problem input, while Fig. 1(b) shows the expected result.

3 ALGORITHM OVERVIEW

In order to solve Problem 1, which is the first time defined in the literature, we propose a novel algorithm flow, as demonstrated in Fig. 2. Our algorithm flow consists of three major stages:

- **Initial Power/Ground Plane Generation based on Voronoi Diagram** constructs a Voronoi diagram for each RDL according to the global routing tree vertices and edges of the power nets on the same RDL. Based on the Voronoi diagram, each RDL can be dissected into different power planes corresponding to the global routing trees of

those power nets, as shown in Fig. 2(b), while achieving the highest area utilization.

- **Obstacle-aware Power/Ground Plane Legalization** realizes power planes by considering design rules and trims off the areas of the routed signal wires/vias and other obstacles from the initial power planes based on the Boolean operations. It further refines the power planes by identifying and reconnecting the floating planes while maintaining the area utilization, as shown in Fig. 2(c).
- **Cross-layer Power Integrity Enhancement** further enlarges the overlapped power plane areas on adjacent RDLs belonging to the same power net by converting some fractions of power planes into different power nets for more redundant via insertion, as shown in Fig. 2(d). Consequently, both area utilization and cross-layer power integrity are maximized.

The following sections will further explain the algorithms of each stage in greater detail.

4 INITIAL POWER PLANE GENERATION

Instead of directly solving Problem 1, we ignore all obstacles at the beginning to reduce the complexity of the problem. We define the simplified initial power plane generation problem as follows:

Problem 2. ***Initial Power Plane Generation****: Given a set of RDLs, design rules, and the global routing trees of all power nets, create all the power/ground planes such that the area utilization is maximized, while all design rules are satisfied.*

We employ the idea of constructing the Voronoi diagram to solve Problem 2 because of its advantages of geometric properties and efficiency. Given a set of *seeds* which are randomly distributed on a two-dimensional (2D) surface, a Voronoi diagram partitions the 2D surface into a set of connected convex polygons, or *Voronoi cells*, where each Voronoi cell, c_i, contains a seed, s_i, and all points in c_i are closer to s_i than any other seeds. All Voronoi cells form a tessellation which completely covers the 2D surface with full area utilization. By applying the Fortune's algorithm [13], it takes only $O(n \lg n)$ to construct a Voronoi diagram, where n denotes the number of seeds.

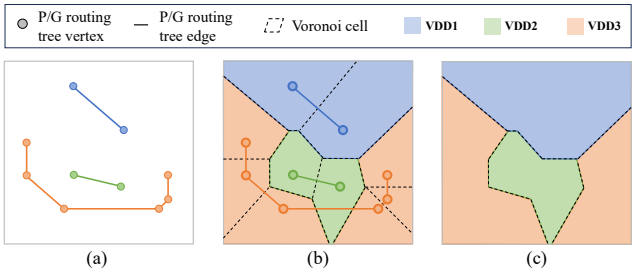

Figure 3: An example of constructing power planes on an RDL based on the power routing trees and Voronoi diagram. (a) The global routing trees of three power nets on the RDL. (b) The Voronoi diagram with the seeds corresponding to the global routing tree vertices in (a). (c) The resulting power planes of the three power nets on the RDL, where VDD3 has disconnected power plane violation.

We are the first in the literature which propose to generate the power planes on RDLs by taking the aforementioned advantages of the Voronoi diagram. We construct the Voronoi diagram on each RDL by considering at least the global routing tree vertices of all power nets on that RDL as the initial seeds, which is demonstrated Fig. 3. Fig. 3(b) shows the resulting Voronoi diagram with the seeds corresponding to the global routing tree vertices in Fig. 3(a). Each Voronoi cell in Fig. 3(b) represents a power plane of the corresponding power net. If two adjacent Voronoi cells belong to the same power net, the power planes can be merged, as shown in Fig. 3(c). In this example, both VDD1 and VDD2 result in a single connected power plane after merging their Voronoi cells, respectively. However, VDD3 in Fig. 3(c) results in two separate power planes, which violates the original power routing tree of VDD3 in Fig. 3(a).

Definition 1. ***Disconnected Power Plane Violation****: Given a globally routed power net on an RDL with the power routing tree, the power plane resulting from the power routing tree must be connected. Otherwise, the disconnected power plane violation occurs.*

To avoid the disconnected power plane violation when generating power planes based on the Voronoi diagram, all Voronoi cells belonging to the same power net must be connected. In order to ensure a Voronoi diagram without any disconnected power plane violation, we have the following lemma and theorem while omitting the proofs due to the page limit.

Lemma 1. *When constructing a Voronoi diagram with the seeds corresponding to the power routing tree vertices, the disconnected power plane violation occurs if any circumscribed circle, which is formed by a power routing tree edge of the power net, n_i, as its circumdiameter, contains any power routing tree vertex of the other power net, n_j.*

Theorem 1. *The power planes of each RDL resulting from the Voronoi diagram are valid without any disconnected power plane violation if the smallest circumscribed circle of each power routing tree edge does not contain any other vertex.*

Based on Lemma 1 and Theorem 1, we shall insert extra vertices/seeds to separate those power routing edges whose smallest circumscribed circle contains other vertices. Once those long power routing edges are separated into shorter ones whose smallest circumscribed circles do not contain any other vertex, the power planes resulting from the Voronoi diagram with seeds based on both the original power routing tree vertices and the inserted vertices are valid without any disconnected power plane violation.

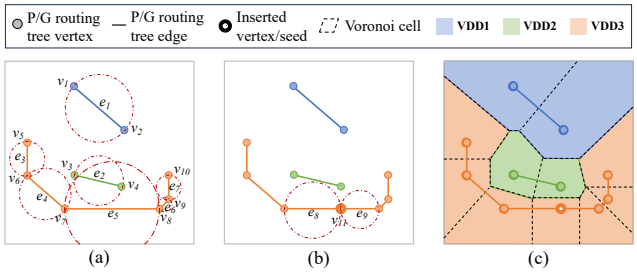

Figure 4: Vertex/Seed insertion to avoid disconnected power plane violation. (a) The smallest circumscribed circles of all power routing tree edges. (b) The newly inserted vertex/seed, v_{11}, which avoids disconnected power plane violation. (c) The resulting Voronoi diagram and the power planes of all power nets without disconnected power plane violation.

Fig. 4 gives an example of vertex/seed insertion to avoid disconnected power plane violation. Fig. 4(a) highlights the smallest circumscribed circles of the power routing tree edges, e_1, e_2, ..., e_7. The smallest circumscribed circle means that the circumdiameter of each circle is the corresponding edge length. It should be noted the circumscribed circle of e_5 contains the vertex, v_4. Therefore, we shall insert an extra vertex/seed, v_{11}, by projecting v_4 to e_5. After inserting v_{11}, e_5 is separated into two shorter edges e_8 and e_9, as shown in Fig. 4(b). We shall further verify whether the newly inserted vertex is contained by any other circumscribed circle and whether the smallest circumscribed circles of the new edges contain other vertices. The vertex/seed insertion will stop until no circumscribed circle

contains other vertices. Fig. 4(c) shows the resulting Voronoi diagram and the power planes of all power nets without disconnected power plane violation after vertex/seed insertion.

5 OBSTACLE-AWARE POWER PLANE LEGALIZATION

After generating the initial power/ground planes based on the Voronoi diagram, we shall realize the power/ground planes according to the design rules while considering the routed signal wires/vias and other obstacles. The design rules include both the angle rule and the spacing rule. For the angle rule, the boundary lines of power planes are restricted to 0, 45, 90, and 135 degrees. To convert any angle boundary lines into the restricted degrees of angles, we rotate each boundary line with the axis at its center point to the closest satisfied degree. To satisfy the spacing rule, we apply the Boolean operations on polygons. We first upsize the polygon of each power plane based on the spacing rule and then remove the overlap area. Fig. 5(a) shows the initial power planes of the three power nets resulting from the Voronoi diagram in Fig. 4(c), and Fig. 5(b) realizes the power planes according to the angle and spacing rules. Other design rules, such as the acute angle, will be handled at the post-processing stage, which is beyond the scope of this work.

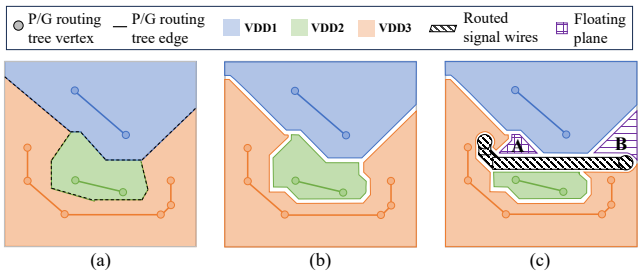

Figure 5: Plane realization and obstacle consideration. (a) The power planes resulting from the Voronoi diagram. (b) Power plane realization according to design rules. (c) Power plane realization considering obstacles, which may lead to floating planes.

Once the power planes are realized, we shall further consider the routed signal wires/vias and other obstacles. We apply the Boolean operator, *NOT*, to trim off the up-sized signal wires/vias and obstacles due to the spacing rule from the realized power planes, as shown in Fig. 5(c). It should be noted that such a Boolean operation may lead to some floating planes.

Definition 2. ***Floating Plane****: a floating plane is a dangled plane that does not associate with any global routing tree vertex of a power net after trimming off the obstacles from the initial power planes.*

In Fig. 5(c), the regions, *A* and *B*, become floating planes after trimming off the area of signal wires/vias because they are dangled and do not associate with the power net, VDD3, anymore.

Instead of removing the floating planes, we shall reconnect the floating planes to their adjacent power planes of different power nets to achieve even better area utilization.

Problem 3. ***Floating Plane Reconnection****: Given a set of power planes and a set of floating planes, reconnect each floating plane to one of its adjacent power planes such that the area utilization is maximized.*

Different from the previous works [14–18] which reconnect different polygons of the same net by searching for the shortest path, Problem 3 reconnect the polygon of each floating plane to any power net by search for the longest common borders between the floating plane and its adjacent power planes in order to maximize the area utilization. The common borders can be found by upsizing the floating planes and the neighboring non-floating power planes.

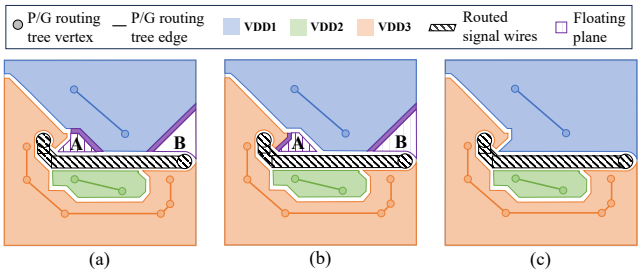

Figure 6: Floating plane reconnection. (a) Both floating planes, *A* and *B*, can be reconnected to the power plane of VDD1. (b) The floating planes, *A* and *B*, can be reconnected to the power planes of VDD3 and VDD1, respectively. (c) The refined power planes after floating plane reconnection.

Fig. 6 gives an example of floating plane reconnection. When sizing up the floating planes, *A* and *B*, and their neighboring non-floating power planes, the floating plane, *B*, has only one common border with the power plane of VDD1, and the floating plane, *A*, has common borders with the power planes of both VDD1 and VDD3. Since the border between *A* and VDD1 is longer than that between *A* and VDD3, reconnecting *A* to VDD1 results in higher area utilization.

6 CROSS-LAYER POWER INTEGRITY ENHANCEMENT

After solving Problems 2 and 3, the result is already a legal solution, which maximizes power plane area utilization while satisfying the design rule constraints with the consideration of all obstacles. However, Problems 2 and 3 only focus on every single RDL without considering cross-layer power plane co-optimization. The cross-layer power integrity is essential especially when the fan-in pad and fan-out bumps of a power net are on different sides of the interposer. We shall further maximize the number of vias between the power planes on adjacent RDLs by enlarging the overlapping area. As the RDLs have been fully occupied by power planes resulting from the former stages, all we can do is trade some fractions of power planes among different power nets. Fig. 7 illustrates the improvement of the power plane via numbers after cross-layer power integrity enhancement between two adjacent RDLs.

Problem 4. ***Power Plane Trading for Cross-Layer Power Integrity Enhancement****: Given the legalized non-floating power planes on different RDLs with maximized utilization, trade some fractions of power planes among different power nets such that the overlapping ratio of the power planes of the same power net on adjacent RDLs and the total number of power plane vias are maximized without sacrificing power plane area utilization.*

Before solving Problem 4, we give the following definitions:

Definition 3. ***Stacked Plane****: A power plane is a stacked plane if it overlaps with two or more planes belonging to the same net on consecutive adjacent RDLs.*

Definition 4. ***Hard Plane****: A power plane is a hard plane if it is not a stacked plane, while overlaps with another power plane belonging to the same net on the adjacent RDL.*

Definition 5. ***Soft Plane****: A power plane is a soft plane if it is neither a stacked plane nor a hard plane.*

Definition 6. ***Tradeable Plane Set****: A set of two overlapped power planes on adjacent RDLs is tradeable if one of them is a soft plane, and the other is either a soft plane or a stacked plane.*

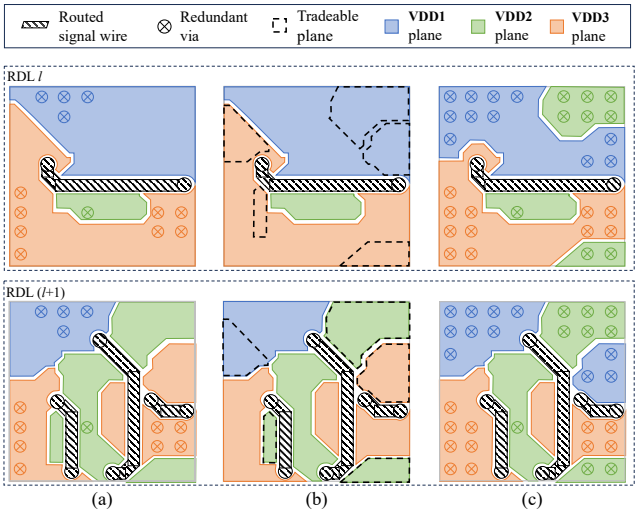

Figure 7: Cross-layer power integrity enhancement between two adjacent RDLs. (a) The power planes resulting from Section 5 with only a few power plane vias between RDL_l and RDL_{l+1}. (b) The tradeable power plane fractions for enhancing power integrity. (c) The resulting power planes with much more power plane vias after power plane trading.

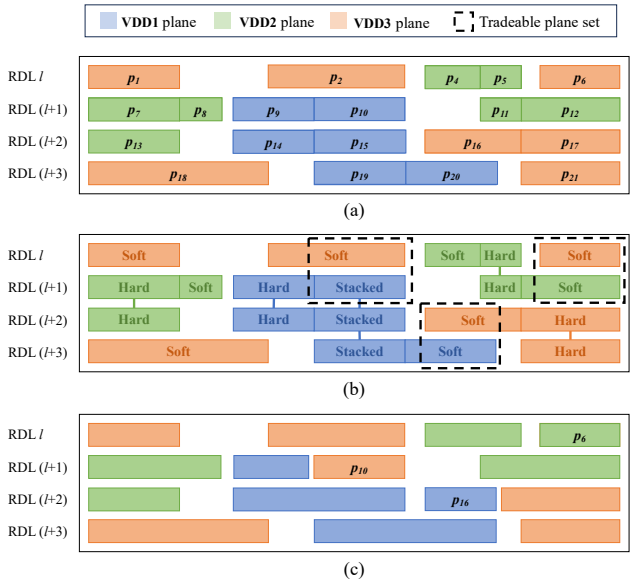

Figure 8: The cross-section view of power plane trading for cross-layer power integrity enhancement. (a) The fragmented power planes on four RDLs before power plane trading. (b) The tradeable plane set. (c) The resulting power planes after power plane trading, where VDD1 trades p_{16} from VDD3, VDD2 trades p_4 from VDD3, and VDD3 trade p_{10} from VDD1.

To solve Problem 4, first of all, we shall fragment the power planes on each RDL according to the power plane boundaries on the adjacent RDL. Once the power planes are fragmented into smaller pieces, we label each fragmented power plane with either a stacked plane, a hard plane, or a soft plane. With the label of each plane, we shall collect all tradeable plane sets, according to Definition 6 between any two adjacent RDLs. For the overlapped power planes, p_i and p_j, in each tradeable plane set, they must belong to different power nets, n_a and n_b, respectively. We can either trade p_i from n_a to n_b, or trade p_j from n_b to n_a. The objective of the trading is to maximize the overlap ratio of all power planes belonging to the same power net on adjacent RDLs, which can be calculated by Equation (1), where A_{P_l} is total area of the power planes on the RDL_l.

$$Overlap\ Ratio = \frac{A_{P_l} \bigcap A_{P_{l+1}}}{A_{P_l} \bigcup A_{P_{l+1}}} \tag{1}$$

A larger overlap ratio between the power planes on adjacent RDL belonging to the same power net indicates that more redundant vias can be inserted leading to higher power integrity. We apply the greedy algorithm to achieve the optimal power plane trading for all tradeable plane sets.

Fig. 8 demonstrates an example of power plane trading for cross-layer power integrity enhancement with a cross-section view. In Fig. 8(a), the power planes are fragmented into smaller pieces according to the power plane boundaries on the adjacent RDL. Fig. 8(b) shows the label of each fragmented power plane, as well as the tradeable plane sets. After applying the greedy algorithm to maximize the total overlap ratio of power planes belonging the the same net on adjacent RDLs, the optimal power plane result is shown in Fig. 8(c).

7 EXPERIMENTAL RESULTS

We implemented the proposed power plane generation algorithm in the C++ programming language with Boost Geometry 1.8.0 for the polygon computation. Our algorithm was executed on an Intel i9 3.4GHz Linux workstation with 64GB memory, and tested based on the industry benchmarks, as shown in Table 1. The benchmarks include five cases with the number of power nets ranging from 3 to 14 and the number of signal nets ranging from 27 to 250. Each power net is globally routed (not physically routed yet) with a 3D routing tree on four RDLs connecting a large number of fan-in pads and fan-out bumps with hundreds of tree vertices. Each benchmark also has a globally routed (not physically routed yet) ground net connecting even more fan-in pads and fan-out bumps. All signal nets in each benchmark had been physically routed wires and vias, which are obstacles during power plane generation.

To demonstrate the effectiveness and efficiency of our algorithm, we experimentally compared our algorithm with the most recent power plane generation method [12], namely GOMLP, and the manual approach from the industry. Tables 2 and 3 show the experimental results. Compared with GOMLP [12], our approach results in similar power plane area utilization, but achieves 2.5X via number between cross-layer power planes, 16% more ground plane area, and 29% more ground plane vias. Compared with the manual approach from the industry, although our approach results in 28% less ground plane area and 40% less ground plane vias, our approach leads to 9X power plane area and 100X via number between cross-layer power planes. Most importantly, the runtime based on our approach can be significantly reduced from hours or even days to less than one minute according to Table 3.

It should also be noted that, according to Table 1, the total routing tree wirelength of the power nets in Cases 0–2 is much longer than the routing tree wirelength of the ground net. Consequently, the percentages of power plane area and ground plane area resulting from GOMLP [12] and our approach are more balanced than those resulting from the manual design.

In summary, the reasons why our proposed Voronoi diagram-based multiple power plane generation algorithm can achieve better performance in power plane area utilization, cross-layer power plane vias, and runtime are analyzed as follows:

- We construct the Voronoi diagram based on the global routing trees of both power and ground nets on each RDL, which not only maximizes the power plane area utilization but also balances the power plane area across all RDLs according to the distributions of the power routing trees.

Table 1: Benchmarks statistics including the number of layers ($|L|$), the number of power nets ($|N_P|$), the number of power fan-in pads ($|Q_P|$), the number of power fan-out bumps ($|B_P|$), the number of power routing tree vertices ($|V_P|$), the total wirelength of power routing trees ($|WL_P|$), the number of ground nets ($|N_G|$), the number of ground fan-in pads ($|Q_G|$), the number of ground fan-out bumps ($|B_G|$), the number of ground routing tree vertices ($|V_G|$), the total wirelength of ground routing trees ($|WL_G|$), and the number of signal nets (N_S).

Benchmarks	$\|L\|$	$\|N_P\|$	$\|Q_P\|$	$\|B_P\|$	$\|V_P\|$	$\|WL_P\|(\mu m)$	$\|N_G\|$	$\|Q_G\|$	$\|B_G\|$	$\|V_G\|$	$\|WL_G\|(\mu m)$	$\|N_S\|$
Case 0	4	3	42	48	301	8467.46	1	113	81	704	2090.80	27
Case 1	4	7	507	94	580	55184.64	1	557	142	1364	13827.32	62
Case 2	4	6	207	77	412	35130.22	1	565	142	1388	14075.32	62
Case 3	4	13	28	13	105	11216.81	1	1846	445	3260	41482.05	250
Case 4	4	14	48	14	136	21609.04	1	1846	445	3260	41482.05	250

Table 2: Comparisons of the percentage of total power plane area ($|A_P|$), the number of vias in the power planes ($|I_P|$), the percentage of total ground plane area ($|A_G|$), the number of vias in the ground planes ($|I_G|$) for GOMLP [12], the manual approach from industry, and Ours.

Benchmarks	GOMLP[12]				Manual				Ours w/o Cross-Layer PI Opt.				Ours w/ Cross-Layer PI Opt.			
	$\|A_P\|$	$\|I_P\|$	$\|A_G\|$	$\|I_G\|$	$\|A_P\|$	$\|I_P\|$	$\|A_G\|$	$\|I_G\|$	$\|A_P\|$	$\|I_P\|$	$\|A_G\|$	$\|I_G\|$	$\|A_P\|$	$\|I_P\|$	$\|A_G\|$	$\|I_G\|$
Case 0	30.71%	6482	67.25%	30703	2.39%	175	97.18%	60868	33.34%	11150	66.66%	33200	38.52%	17274	61.48%	32241
Case 1	40.92%	6905	46.62%	16751	8.10%	211	91.60%	43416	33.54%	7985	66.47%	27704	36.82%	10935	63.21%	26381
Case 2	22.10%	3863	63.74%	26493	5.73%	146	94.26%	48019	21.17%	4998	78.84%	37183	24.51%	8030	75.51%	36109
Case 3	5.99%	1583	79.07%	102070	0.05%	40	99.75%	150899	4.04%	3023	95.76%	145470	4.34%	3840	95.46%	145322
Case 4	7.84%	861	60.17%	71817	0.07%	58	99.73%	149964	6.74%	5916	92.91%	137977	7.87%	8747	91.78%	137119
Comp.	1.04	0.40	0.84	0.71	0.11	0.01	1.28	1.40	0.89	0.69	1.04	1.02	1.00	1.00	1.00	1.00

- We maximize the overlapping ratio of power plane areas on adjacent RDLs that belong to the same power net for more redundant vias, which helps ensure cross-layer power integrity.
- Our power plane generation and optimization algorithms can be done in polynomial time, which is extremely efficient compared to both manual and non-deterministic approaches.

Table 3: Comparisons of runtime for GOMLP [12], the manual approach from industry, and Ours.

Benchmarks	GOMLP [12]	Manual	Ours w/o Cross-Layer PI Opt.	Ours w/ Cross-Layer PI Opt.
Case 0			0.59 s	6.15 s
Case 1	minutes	hours	3.99 s	12.92 s
Case 2	to	to	2.87 s	10.19 s
Case 3	hours	days	18.18 s	32.68 s
Case 4			13.18 s	35.18 s

8 CONCLUSIONS

In this paper, we have presented the new problem formulation for multiple power plane generation on RDLs in 3D ICs that guarantees the routability of both signal nets and power nets. We have proposed to generate the initial power planes of all power nets based on the Voronoi diagram and their global routing trees while maximizing routing space utilization under design rule constraints. We have further proposed to refine the power planes by considering routed signal wires and vias as obstacles. We have finally enhanced the cross-layer power integrity. Our experimental results have shown that the power planes generated by our method can achieve significant improvement in cross-layer power integrity, compared with the manual approach and the recent work.

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