

Post-Layout Automated Optimization for Capacitor Array in Digital-To-Time Converter

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Abstract—The integral non-linearity (INL) of Digital-to-Time Converter (DTC) in fractional-N phase-locked loops introduces fractional spurs, especially at near-integer channels, resulting in increased jitter. To meet the strict jitter and spur performance requirements of high-performance wireless transceivers, minimizing the INL in DTC designs is crucial. This work presents a computer-aided, automated optimization methodology that focuses on addressing issues stemming from the uniform capacitor unit structure within the capacitor array in Variable-Slope DTC. These issues include parasitic resistance and capacitance, which distort the charging and discharging behavior of the capacitors, contributing to INL. By systematically optimizing the capacitor layout and mitigating parasitic effects, the methodology allows precise tuning of each capacitor unit in capacitor array to reduce INL, enhancing the overall performance of the DTC.

Index Terms—capacitor arrays, digital to time converter, design automation, layout automation.

I. INTRODUCTION

In the design of frequency synthesizers for high-performance wireless transceivers, achieving ultra-low jitter and high spectral purity is paramount. Digital-to-Time Converter (DTC) have proven effective in precision timing systems, particularly within fractional-N PLLs, where they are utilized to cancel quantization errors arising from divider modulation, thus achieving lower jitter [1], [2]. However, the integral non-linearity (INL) of DTC introduces fractional spurs, particularly in near-integer channel, leading to increased jitter.

Several methods have been explored to mitigate the INL of DTC, as summarized in Table I. These include digital pre-distortion (DPD) [3], constant-slope (CS-DTC) [4] reduce non-linearity by charging a capacitor at a consistent ramp rate, and inverse constant-slope DTC (ICS-DTC) [5] improves linearity by adjusting pre-charging times to eliminate voltage dependencies. Variable-slope DTC (VS-DTC) have been improved by adding parallel fixed capacitors to switched-capacitor banks to reduce INL, though this requires a trade-off between power consumption and linearity [6], [7]. To overcome this, a topology of DTC which Reverse-Concavity Variable-Slope DTC(RCVS-DTC) was recently introduced [8].

Despite these advancements, the design of DTC remains complex and resource-intensive, often involving intricate struc-

TABLE I: Comparison of related work

Source	Structure	Approach to reduce INL
[3]	DTC with pre-distortion	DPD modifies $\Delta\Sigma M$ code
[4]	Constant-Slope DTC	Charging capacitors at a constant ramp rate
[5]	Inverse Constant-Slope DTC	Initial voltage generation based on VCO-period pre-charging time
[8]	Reverse-Concavity Variable-Slope	Adding a resistor to the unit capacitor
This work	Variable-Slope DTC	Automatically refines layout with post-layout simulations

tures and iterative adjustments to meet strict performance criteria. Existing methods primarily focus on reducing INL at the circuit level, our approach introduces a design methodology that uses computer-aided tools and automatic simulation scripts to directly adjust each capacitor and perform simulations, which would be challenging and time-consuming to achieve manually. For instance, adjusting a 10-bit capacitor array with 1,024 units manually and performing post-layout simulations would be highly labor-intensive, repetitive, and prone to errors. This methodology replaces the need for such manual efforts, accelerates the design cycle, simplifies circuit design, and optimizes device parameters across a wide range of capacitor array schemes.

In this work, we address the INL reduction challenges of Variable-Slope DTC, which circuit structure is simple but complicates in INL reduction due to the use of repeated identical capacitor units. Our approach specifically addresses the challenges posed by parasitic resistance and capacitance, which introduce variations in capacitor charging and discharging times. Such effects are difficult to predict and analyze due to complex interactions between parasitic and the physical layout in RC network and leading to non-uniform delay time step.

To mitigate these effects, our methodology employs iterative post-layout simulations. By automating the schematic, layout, and post-layout simulation processes, this approach enables

precise adjustments of the capacitor values within the layout, thereby minimizing INL while maintaining a simple circuit structure with efficient power consumption. This work presents an automated-optimized 10-bit variable-slope DTC. This DTC achieves a resolution of 260 fs and a peak INL of 224 fs, implemented using a 40nm CMOS process.

This paper is organized as follows. Section II presents the proposed circuit structure. The post-layout optimization method of capacitor array is discussed in Section III. Finally, measurement results are presented in Section IV, followed by a conclusion in Section V.

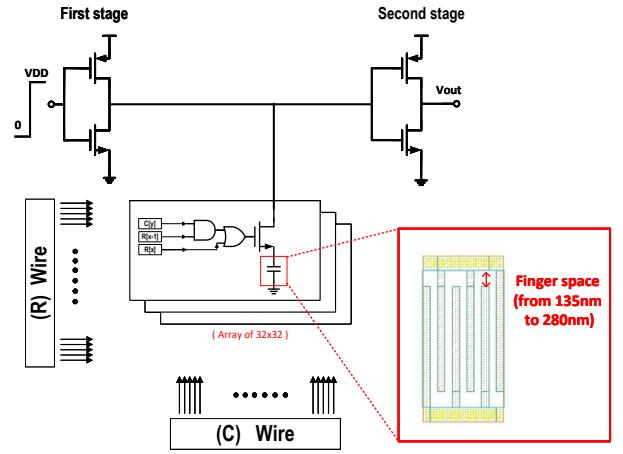
II. PROPOSED ARCHITECTURE

In conventional capacitor array structures, a common approach for step-size adjustment involves one functional capacitor array for normal operation and a calibration DAC for fine adjustments [9], [10]. This method requires precise coordination between the operational capacitor and the calibration DAC to achieve the desired tuning resolution. However, the combination of an operational capacitor and a calibration DAC increases area and power consumption, which can negatively impact overall efficiency and performance. To overcome these challenges, our approach opts for a single, highly optimized fine-tuning array consisting of 1023 individual units. Each unit is capable of minute adjustments, enabling linearity across the entire range. By consolidating the tuning functionality into a single array, our design simplifies the circuit architecture and ensures consistent performance. This approach eliminates the need for complex coordination between separate arrays, thereby reducing the risk of errors and enhancing the overall accuracy and efficiency of the tuning process.

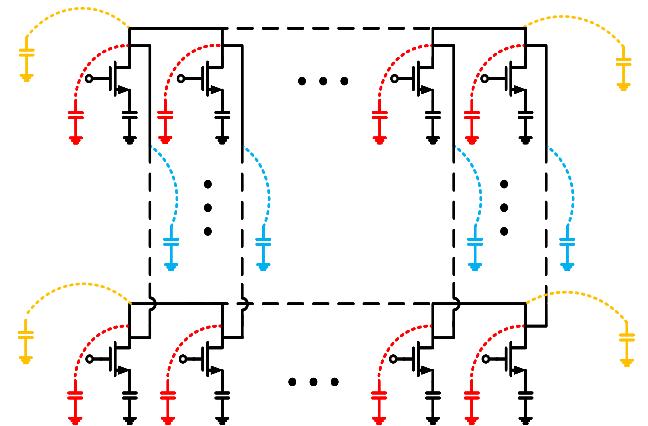
The initial stage of the DTC links to a 1023 capacitor cell (32x32-1) switchable array (Fig. 1(a)), utilizing minimum-sized capacitors to attain a fine resolution of 0.26 ps. The 5-bit decode to control 32 rows through R [31:0] in the R-wires, and 32 columns through C [31:0] in the C-wires. For sequential switching of each unit in the capacitor bank, the C[y], R[x], and R[x-1] signals control an AND-OR gate, which in turn manages the connection of capacitors in the DTC. The MOM capacitor in each unit of capacitor array is the minimum size ($W=0.07 \mu m$, $S=0.07 \mu m$) specified by the process design kit (PDK) to achieve precise resolution.

Various types of parasitic in the capacitor network arise after routing, and the schematic of the MOM capacitor array is shown in Fig. 1(b). This parasitic capacitance may have serious impact on charging and discharging times of the capacitors within the DTC, leading to degraded INL performance. Moreover, these parasitic capacitors are highly dependent on the routing and placement of the layout. To address this issue, the spacing between the metal finger and the bus strip (Finger-space) of capacitor in each cell (Fig. 1(a) red square) which ranges from 135 nm to 280 nm with step of 5nm. results in variations in the capacitor value from 1.46fF to 1.53fF to mitigate the effects of parasitic.

Manufacturing process mismatches can cause variations in capacitor values, stemming from inconsistencies in the fabrication process. These mismatches result in slight deviations



(a) DTC Architecture.



(b): Capacitor Array (32x32-sized) Parasitic Capacitors

Fig. 1: (a) DTC Architecture. (b) Parasitic Capacitors in the Net of DTC Capacitor Array (32x32-sized)

from the intended capacitor values, which can impact overall performance.

In the case of a 10-bit DTC capacitor array, the value of each unit capacitor can be modeled as a Gaussian random distribution, with the process variation ratio $\Delta C/C$ following $N(0, \sigma^2)$ during fabrication [11]. The standard deviation σ , which can be characterized in the CMOS process, quantifies the mismatch between unit capacitors. By using Monte Carlo simulations, the relative mismatch distribution has a standard deviation of $\sigma C = 0.82\%$, which is consistent with results in [12]. For the minimum unit capacitor in the DTC ($C = 1.46 \text{ fF}$), the relative mismatch distribution between them $\Delta C/C$ also satisfies Gaussian random distribution, as analyzed using the method in [13]. The result shows that the mismatch of MOM capacitors with $\sigma C = 0.82\%$ results in an INL variation within 1 LSB for the 10-bit DTC. Given the memory limitations encountered during detailed Monte Carlo post-simulation for INL analysis, this mismatch analysis relies on approximate calculations.

III. POST-LAYOUT OPTIMIZATION

The complete implementation workflow for generating and simulating the circuit's schematic and layout, as well as the automated adjustments, is shown in Fig. 2(a).

At the start of this process, the schematic and layout of the capacitor bank are generated within a single cell using Python-skill language bridge (green square in Fig. 2(a)), beginning with an initial fingertip spacing value. Each capacitor unit is placed in a fixed location with built-in redundancy, ensuring that any adjustments to the capacitor's fingertip spacing will still meet Design Rule Check (DRC) requirements during the routing of the entire DTC layout. This approach helps to minimize DRC issues during the optimization process. Following this, a post-layout simulation is performed to obtain the initial INL of the DTC. The testbench for this simulation is pre-built and reused in each iteration of the optimization loop to assess the DTC INL. After completing the initial post-layout simulation, the process moves into the optimization loop (green square). In the first iteration, the fingertip spacing is adjusted based on the initial INL results from the simulation. The automatic optimization process flow chart of the DTC shows in Fig. 2(b).

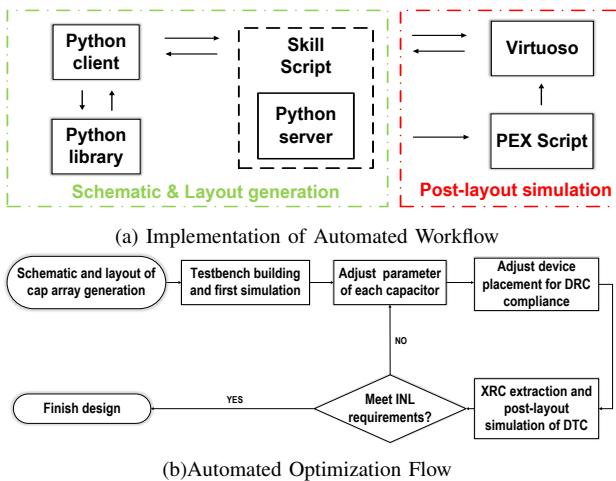


Fig. 2: (a) Implementation Method of Automated Workflow for Schematic, Layout Generation and Iterative Optimization. (b) Automated Optimization Flow

To keep simulation time within an acceptable range, the capacitor adjustments are made in groups of 32 capacitors. Each iteration takes approximately 30 minutes, including regenerating the schematic and layout of the capacitor array, extracting parasitic, and running post-extraction simulations. The process was conducted in a Linux environment using an Intel® Xeon® Gold 6248R CPU running at 3.00 GHz.

Fig. 3 illustrates the initial INL and DNL measurements prior to any modifications and with iterative adjustment process applied to the 1023 capacitor cells, refining the INL and DNL values toward the desired targets. The parameter adjustments for each capacitor are guided by the results of the most recent INL simulation of the DTC. The method involves comparing each DNL to the initial average DNL

obtained from the first simulation. If a step's DNL exceeds the average, the corresponding capacitor is reduced by increasing its finger spacing; if the DNL is lower, the capacitor is increased by decreasing the finger spacing. To accelerate the iterative process, the initial iterations involve adjusting groups of 32 cells which is one row in capacitor array at a time. Fine-tuning is then performed where the INL is closest to linear. This iterative approach ensures continuous refinement of capacitor parameters to achieve optimal performance. The INL and DNL of the final iteration in the optimization loop are represented by the blue line in Fig. 3.

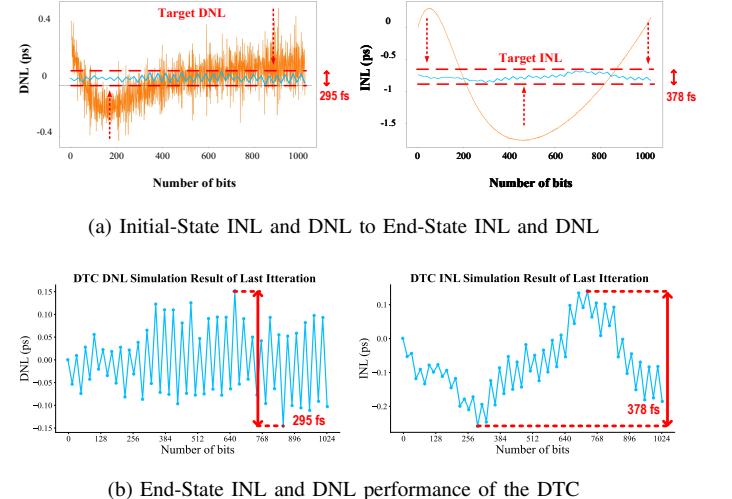


Fig. 3: (a) Simulation result of Initial INL and DNL to final INL and DNL. (b) End-State INL and DNL performance of the DTC

IV. MEASUREMENT RESULT

The proposed DTC, developed using automated parameterized simulation and layout scripts, was fabricated using a 40nm CMOS process, occupying a compact area of 0.012 mm².

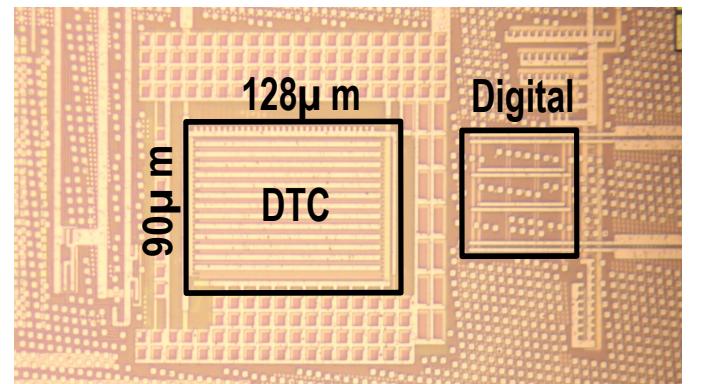


Fig. 4: Die Photo of DTC

The die micrograph of the fabricated chip is presented in Fig. 4. To mitigate the adverse effects of uncontrollable parasitic, fixed-position dummy metal structures were strategically placed near the DTC during layout.



Fig. 5: Measured INL and DNL Performance of the Proposed DTC Across Two Chips at 1.00V(top), 1.05V(middle), and 1.10V(bottom) Supply Voltages

The DTC was characterized through a phase modulation measurement technique as described in [14], achieving a resolution of 10-bit and a full-scale delay range of 260 ps. The reference clock frequency was set to 50 MHz for these measurements. The INL and DNL performance of the DTC across varying supply voltages are depicted in Fig. 5, which presents results for three voltage levels: 1.00V, 1.05V, and 1.10V (Fig. 5 top, middle, and bottom). Each plot includes four curves representing the performance of three tested chips compared with simulation result. The DNL results demonstrate consistent trend across different chips, validating the effectiveness of the design methodology. While the DNL curves show similar behavior, the subtle differences between them lead to variations in the accumulation of INL, as INL is the cumulative result of DNL. These differences in INL are primarily caused by process mismatches during fabrication runs, along with variations in the input and output drivers, which are sensitive to voltage fluctuations and can lead to variations in INL and DNL at different voltage operating points. Additionally, variations in the testing environment, such as temperature or power supply fluctuations, can further impact the INL and DNL measurements. Under the same test conditions, environmental noise for the same chip measured between -20 fs and +20 fs, which has a minimal impact compared to the process-induced variations. Fig.6 shows the setup of the testing environment.

At a supply voltage of 1.05V, the DTC of three chips achieve peak INL of 224 fs, 282 fs and 211 fs, peak DNL of 181 fs,

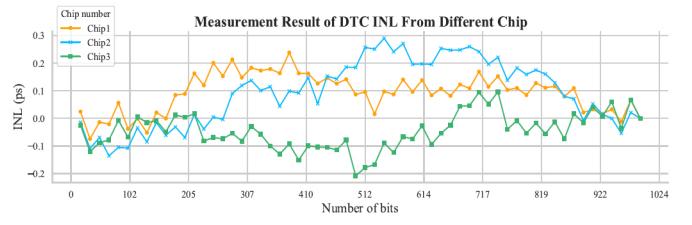


Fig. 6: Setup of the DTC Test Environment

174 fs and 215 fs, illustrating the precision and stability of the design across multiple chips, despite the inherent process mismatch in manufacturing and testing environment. The overall consistency between the three chips further confirms the reliability of the DTC.

Table II presents a comparison of the proposed DTC with several state-of-the-art designs. The proposed DTC, fabricated in a 40nm CMOS process, achieves a resolution of 260 fs and a peak INL of 224 fs, with a power consumption of 0.17 mW. These results demonstrate the effectiveness of the proposed design, providing a balance between power efficiency,

precision, and linearity.

TABLE II: COMPARISON TO STATE-OF-THE-ART DTCs

Source	This Work	ISSCC'24 [15]	ISSCC'18 [16]	JSSC'19 [17]
Method	Variable slope	Multi Pseudo-Diff	Constant slope	Constant slope
Process	40nm CMOS	65nm CMOS	65nm CMOS	28nm CMOS
Supply(V)	1.1	1	1	1
Number of bits	10	3+6+6	10	9
Resolution(fs)	260	60	580	148
Delay Range(ps)	263	280	593	76
INL (fs)	224 (0.08%)	580 (0.21%)	870 (0.15%)	159 (0.21%)
Power (mw)	0.17	1.75	0.14	0.031

V. CONCLUSION

In this work, we presented a design methodology for reducing the integral non-linearity of Digital-to-Time Converter within fractional-N PLL systems. Leveraging an automated, computer-aided design flow, we achieved precise capacitor adjustments and minimized the impact of parasitic effects, which are traditionally challenging to mitigate in manual designs. Our methodology enables accurate post-layout simulations and iterative refinements, leading to a DTC that achieves superior INL performance while maintaining a simple circuit structure and efficient power consumption. It is important to note that while mismatch effects are negligible for the work present in this paper, this approach may encounter limitations in higher resolution designs, where mismatches become more pronounced and could impact performance. Additionally, this methodology heavily relies on the accuracy of the simulation settings.

The proposed 10-bit variable-slope DTC was fabricated using a 40nm CMOS process and demonstrated excellent performance with a 260-fs resolution and a peak INL of 224 fs. The measurement results demonstrated consistent behavior across different chips, validating the effectiveness of the design methodology in mitigating variations introduced by process mismatches. By addressing the optimization of capacitor arrays in DTCs, reduces manual effort and simplifies circuit design while addressing issues caused by system or parasitic elements. It can be applied to improve the performance of device arrays in other circuit designs, facilitating broader applications.

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