On the Impact of Warpage on BEOL Geometry and Path Delays in Fan-out Wafer-Level Packaging*

Dhruv Thapar[1], Arjun Chaudhuri[1], Christopher Bailey[1], Ravi Mahajan[2] and Krishnendu Chakrabarty[1]
[1]School of Electrical, Computer and Energy Engineering, Arizona State University (ASU), AZ
[1]ASU Center for Semiconductor Microelectronics [2]Intel Corporation

***Abstract*—Warpage is a major concern in fan-out wafer-level packaging (FOWLP) due to the complex thermal processing steps involved in manufacturing. These steps include curing, electroplating, and deposition, which induce residual stresses through differential thermal expansion and contraction of materials. This effect is further amplified by mismatches in the coefficients of thermal expansion (CTE) between different materials. In particular, high-density interconnects in the back-end of line (BEOL), redistribution layers (RDLs), and through-mold vias (TMVs) are susceptible to warpage-induced stress, strain, and deformation. This work conducts structural simulations to analyze warpage in the BEOL stack induced by FOWLP. Our results indicate that the impact of warpage is non-uniform across the entire BEOL geometry of a die, hence it impacts different metal layers differently, and different coordinates within one metal layer differently. We leverage this warpage analysis to calculate parasitics and evaluate the resulting changes in path delays.**

I. Introduction

Manufacturing processes, particularly those involving high temperatures, such as curing, electroplating, or deposition, can induce warpage due to the thermal expansion and contraction of materials [1]. Differential thermal expansion between various layers or materials in a structure causes residual stresses that lead to warpage [2]. Additionally, the mismatch in the coefficients of thermal expansion (CTE) between different materials can exacerbate this effect, resulting in uneven deformations that impact the structural integrity and functionality of the device. Process-induced warpage, resulting from high-density interconnects in the back-end of line (BEOL) also significantly impact the performance [3]. This warpage, driven by temperature variations during BEOL processing, differentially affects the metal layers within the BEOL stack.

Warpage is a critical concern in advanced packaging technologies, such as fan-out wafer-level packaging (FOWLP) [2]. In these packages, redistribution layers (RDLs) and through-mold vias (TMVs) are particularly susceptible to warpage-induced stress due to their intricate geometries and material properties [4]. The non-uniform expansion and contraction during thermal processing and cure shrinkage of the polymer materials can lead to misalignment and deformation in the BEOL interconnects and Cu traces in the RDL, affecting the electrical performance and reliability of the interconnections. These mechanical deformations can significantly impact the parasitic characteristics of the interconnects, leading to small delay variations in the design.

In this paper, we perform structural analysis of FOWLP in `Ansys` to compute warpage on a die placed at given coordinates on the wafer to account for the warpage-induced deformations in the BEOL interconnects. We utilize this analysis in our design flow to perform warpage-aware path-delay computation. Our goal is to analyze the impact of warpage-induced deformation in BEOL interconnects on variation in path delays. Our results show that warpage exhibits a non-uniform impact across the BEOL geometry, leading to varying effects on different design paths. This variation leads to reordering of critical paths, thereby necessitating the re-generation of test patterns to detect small delay defects effectively.

II. Structural simulations

In this section, we describe our structural simulation setup in `Ansys` to perform elastic analysis for chip-first die face-up FOWLP. To conduct warpage simulations, we constructed the structure of a die of area 5 mm $\times$ 5 mm in `Ansys` workbench. The BEOL of the die consists of metal layers M1 to M7. The thickness for metal and via layers is obtained from the ASAP7 pdk [5]. In our die face-up configuration, M1 (M7) is the metal layer closest (farthest) to the wafer. The metal and via layers are deposited on top of a 10 µm silicon layer. As the BEOL layers primarily consist of copper and SiO_2, we use equivalent material concept to model these layers [3], [6], [7]. We use the volume percentage method [7] to compute the material properties for the equivalent material.

The values of Cu density used to create equivalent material in our simulations are 0.5 and 0.2 for metal and via layers, respectively [8]. The die is surrounded with a 700 µm thick layer of epoxy mold compound (EMC). For the EMC process, EMC compression molding (125°C) is followed by post-mold cure (PMC) (150°C) [2]. After PMC, we allow the package to cool down to room temperature. We perform transient structural simulations in `Ansys` workbench to compute the deformation across the BEOL stack after the room temperature is achieved. The die is mounted on a square shaped glass carrier wafer which is 700 µm thick and have two of its side faces being constrained to any normal displacement to mark the symmetric axis of the wafer. Also, the edges at the intersection of these faces with the bottom face are fixed supports. The 115 mm $\times$ 115 mm wafer represents a single quadrant of the entire wafer. The edge where the two displacement-restricted side-faces intersect represents the center of the entire wafer. The distance

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of the die from this center is 140 mm which is representative of the dies placed closer to the edge of a 300 mm wafer. Note that dies further from the center experience higher deformation [2].

Table I shows the values of minimum and maximum directional deformation for metal layers M1 to M7. The directional deformation takes both positive and negative values. Note that here, minimum corresponds to the most negative (or least positive) value it achieves, not necessarily the smallest in magnitude. The deformation along Z-direction contributes the most towards total deformation.

TABLE I: Directional deformation for metal layers M1 to M7.

Metal Layer	Deformation along X(nm)		Deformation along Y(nm)		Deformation along Z(nm)	
	Max	Min	Max	Min	Max	Min
M1	0.57	−0.95	0.77	−0.30	3.30	0.89
M2	0.11	−0.49	0.50	−0.21	2.99	0.90
M3	0.07	−0.34	0.35	−0.08	2.70	0.90
M4	0.04	−0.25	0.24	−0.03	2.54	0.90
M5	0.00	−0.15	0.16	−0.01	2.35	0.90
M6	0.00	−0.09	0.09	0.00	2.19	0.90
M7	0.10	−0.10	0.06	−0.11	2.02	0.77

III. Warpage-aware Timing Analysis

We next describe our methodology to compute warpage-aware path delays. The deformed structure from `Ansys` simulations provide us deformation values at all coordinates in different metal layers present in the geometry. We extract these values from the simulations and use them to update the design exchange format (DEF) file created post placement and routing. After synthesis using `Synopsys DC Compiler` and place and route using `Cadence Innovus`, we obtain the DEF file for the design. The DEF file consists of all the polygons created in the BEOL metal routing. Non-uniform deformation adds a non-uniform shift to different sections of the interconnect, which results in the change in the dimension of the interconnect along its length. The total change in length of the interconnect due to deformation is approximated by creating a linear segment based on the deformation values obtained at the center and the endpoints of the interconnect as illustrated in Figure 1. We create a modified DEF file based on the updated dimensions and extract the modified parasitics in the standard parasitic exchange format (SPEF) file. The modified SPEF file is used for static timing analysis.

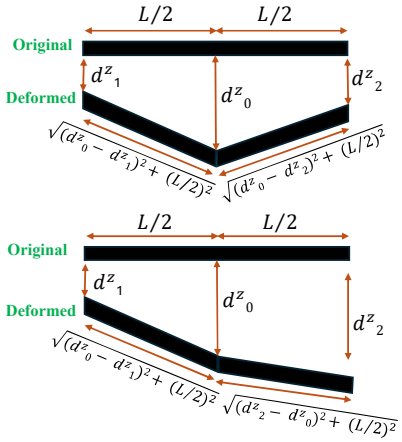

Fig. 1: Change in interconnect length due to non-uniform deformation in Z-direction for two possible deformed geometries.

A. Impact on Path Delay

We applied the warpage-aware analysis to different designs from ISPD and Opencore benchmarks. We compute the top N critical paths for the benchmark designs. Without loss of generality, we set N = 2000 for ac97, DMA_fast, and oc8051_top. The number of paths reported by `PrimeTime` for mc_top and usbf are 1278 and 333, respectively; therefore, N takes the tool-reported value for these designs. We extract these N paths with the warpage-unaware model and compute delays again with the warpage-aware model to determine the longest paths under warpage. To depict the reordering of critical paths, we compute two metrics, N_1 and ΔR_{avg}, for each benchmark. Note that N_1 denotes the number of paths for which the rank in the critical path order changed with warpage-aware modeling. In addition, ΔR_{avg} depicts the average change in path-rank across all these N paths. Table II shows the values for these metrics. The high values of N_1 and ΔR_{avg} across all benchmarks clearly show that long paths are reordered due to warpage.

TABLE II: Metrics and results for different benchmark designs.

Design	Number of critical paths considered (N)	N_1	ΔR_{avg}
ac97	2000	1983	137
mc_top	1278	1254	70
DMA_fast	2000	1972	143
usbf	333	319	24
oc8051	2000	1989	179

IV. Conclusion

We have evaluated the impact of process-induced warpage on the path delay in BEOL interconnects. We performed structural analysis of the package with dies in `Ansys` and incorporated the warpage analysis to compute the change in path delays. Based on our analysis, we conclude that warpage has a non-uniform impact on the interconnect dimensions in the BEOL geometry. Therefore, path delays need to be carefully analyzed to recompute critical paths. This information is critical for test generation for small delay defects.

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