

# Automatic Routing for Photonic Integrated Circuits Under Delay Matching Constraints

Yuchao Wu  
HKUST(GZ)

Weilong Guan  
HKUST(GZ)

Yeyu Tong  
HKUST(GZ)

Yuzhe Ma  
HKUST(GZ)

**Abstract**—Optical interconnects have emerged as a promising solution for rack-, board-scale, and even in-package communications, thanks to their high available optical bandwidth and minimal latency. However, the optical waveguides are intrinsically different from traditional metal wires, especially the phase matching constraints, which impose new challenges for routing in the photonic integrated circuits design. In this paper, we propose a comprehensive and efficient optical routing framework that introduces a diffuse-based length-matching method and bend modification methods to ensure phase-matching constraints. Furthermore, we present a congestion-based A\* formulation with a negotiated congestion-based rip-up and reroute strategy on new rectangular grids with an aspect ratio of  $1 : \sqrt{3}$  to reduce insertion loss. Experimental results based on real photonic integrated designs show that our optical routing flow can reduce total insertion loss by 11% and maximum insertion loss by 108%, while effectively satisfying matching constraints, compared to manual results.

## I. INTRODUCTION

The growing demand for reduced power consumption and minimized interconnection delays in VLSI circuits has exposed the limitations of conventional metal interconnections. Optical interconnects, with their superior bandwidth, lower power consumption, and reduced delay, present a compelling alternative.

However, optical routing presents distinct challenges when compared to conventional electrical routing. In photonic circuits, minimizing transmission loss takes precedence over propagation length, waveguides must follow smooth paths with minimal bend radii to avoid signal attenuation, and routing is restricted to a single dielectric layer with permissible waveguide crossings. Furthermore, applications such as optical neural networks impose stringent phase-matching requirements. Consequently, traditional electrical routing algorithms can not be directly applied to photonic circuits, and new methodologies are needed to tackle the unique optical routing challenges that minimize transmission loss while satisfying phase-matching constraints.

Series research of automated optical router has emerged for the past few years [1]–[3]. Notwithstanding the abundant studies, most existing studies only focus on external requirements like transmission loss and power while ignoring the internal limitations of matching constraints. The few works that do consider matching constraints, such as [3], impose overly stringent requirements that all matched light paths be symmetrical or consistent. Furthermore, nearly all studies rely on integer-linear programming (ILP) methods, which can achieve the global optimum by concurrently routing all the nets. However, this reliance on ILP-based approaches significantly limits scalability, as solving time grows exponentially with problem size.

To tackle with the aforementioned problem, we propose a

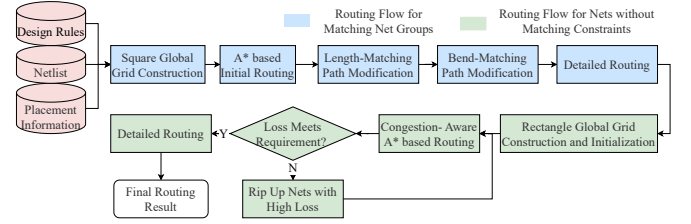


Fig. 1 The overview of our proposed routing flow.

comprehensive and fast framework, focusing on minimizing insertion loss while satisfying phase-matching constraints.

Our contributions are summarized as follows:

- We propose a comprehensive and fast optical routing framework that minimizes insertion loss while adhering to matching constraints.
- We introduce a diffuse-based iterative length-matching method that incorporates a spiral detour pattern, effectively reducing the number of bends introduced during detouring and thereby minimizing total insertion loss.
- We present a congestion-based A\* formulation with a negotiated congestion-based rip-up and reroute strategy on new rectangular grids to reduce insertion loss.
- Experimental results based on a real photonic integrated design show that our optical routing flow decrease 11% total insertion and 108% of max insertion loss while effectively satisfying matching constraints compared to manual results.

## II. PROPOSED METHOD

Fig. 1 summarizes our routing flow, which is divided into two main parts: (1) routing for matching net groups and (2) routing for other general nets without matching constraints. Each part is further subdivided into two stages, which are global routing and detailed routing.

For matching net groups, the global routing stage begins with square global grid construction based on the routing area and the positions of placed devices. An A\*-based method is then applied to establish preliminary paths. To match the accumulated phase delay in optical waveguides, we propose a diffusion-based method that incorporates a spiral detour pattern. By iteratively allocating enough area, spiral detour patterns are applied to unmatched nets, ensuring matching with minimal bends introduced during detouring, thereby minimizing total insertion loss. Additionally, several bend modification techniques are employed to reduce bend discrepancies among nets. In the detailed routing stage, refinement to the positions of pins and turning points while

TABLE I Comparison of the total and max insertion loss (TL, ML), max length difference (MLD), max bends difference (MBD) and the runtime for our full optical routing flow.

Benchmark	Manual				BSG-route [4]				Runtime (s)	Ours				
	TL (dB)	ML (dB)	MLD ( $\mu m$ )	# MBD*	TL (dB)	ML (dB)	MLD ( $\mu m$ )	# MBD		TL (dB)	ML (dB)	MLD ( $\mu m$ )	# MBD	Runtime (s)
OS	3.612	0.669	0	0	5.538	0.838	0	20	4.88	<b>2.760</b>	<b>0.345</b>	<b>0</b>	<b>0</b>	<b>4.06</b>
OM1	5.772	0.879	0	0	13.512	2.319	0	62	188.45	<b>5.592</b>	<b>0.699</b>	<b>0</b>	<b>0</b>	<b>53.97</b>
OM2	<b>22.118</b>	4.377	1001.075	16	41.148	4.045	0	91	118.65	22.488	<b>1.435</b>	<b>0</b>	<b>2</b>	<b>42.15</b>
<b>Norm.</b>	1.11	2.08	-	-	2.08	2.85	-	-	2.50	1.00	1.00	-	-	1.00

\* MBD\* represents the maximum difference between the bend differences of the inputs of MMIs.

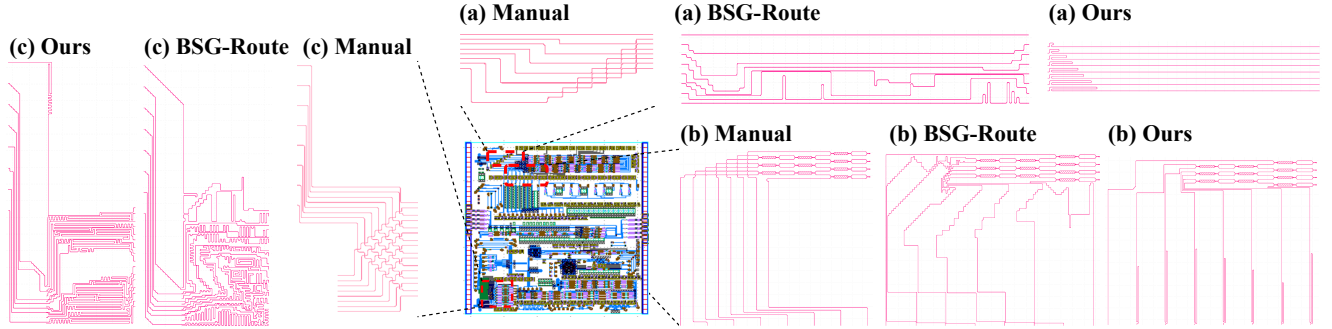


Fig. 2 Comparison of our algorithmic results with manual results. (a), (b) and (c) are zoom-in views of the three regions that need to be matched in the chip: (a) OS, (b) OM1, and (c) OM2.

considering matching constraints is made to obtain the actual physical interconnections.

Similarly, for nets without matching constraints, the global routing stage starts with the rectangular global grid construction and initialization to set up the routing grid. To address insertion loss globally, instead of using the square grid, we use a new rectangular routing grid with an aspect ratio of  $1 : \sqrt{3}$  according to the experimental results of [5], based on which a congestion-aware A\* formulation is investigated to reduce the potential crossing loss in the subsequent detail routing stage while ensuring low current loss. Additionally, a negotiated congestion-based rip-up and reroute strategy [6] is applied to nets with high loss to dynamically manage and further reduce overall insertion loss. During the detailed routing stage, an enhanced A\* search algorithm is employed to navigate the finer grids, enabling precise optimization of the routing paths.

### III. EXPERIMENTAL RESULTS

We implement the proposed optical routing framework in C++ and export the final result into GDS file in Python with *Nazca* library. To evaluate the effectiveness and scalability of our optical routing framework, we select a real photonic integrated design and choose the three most challenging regions for routing, comparing the performance metrics of the resulting circuit layouts with those produced by the BSG-route [4] and experienced photonic integrated circuit designers.

As shown in the TABLE I, our results achieve an 11% and 108% reduction in total loss, as well as a 108% and 185% reduction in maximum loss, compared to manual designs and BSG-Route, respectively. Moreover, despite the moderate scale of the problem, our method demonstrates a 150% reduction in computation time, highlighting its efficiency. As shown in the last column of TABLE I, our approach can complete the routing in seconds, whereas manual routing would take hours. This dramatic reduction in time significantly shortens the design cycle

and facilitates design closure. The resulting layout is shown in Fig. 2. The (a), (b), and (c) are amplifications of three parts that need to be matched with different topologies. The results demonstrate that regardless of how the pins of the matching net groups are arranged, our flow can generate good routing results with minimized insertion loss while adhering to matching constraints.

### IV. CONCLUSION

This paper proposes a comprehensive optical routing framework. Experimental results demonstrate that our routing flow significantly reduce insertion loss while effectively satisfying matching constraints compared to manual results and completing the routing in seconds.

### ACKNOWLEDGMENT

This work is supported by the Natural Science Foundation of Guangdong Province (No.2024A1515012438), Nansha District Key Area S&T Scheme (No. 2024ZD007), CCITA Funding (20240105), and Guangzhou Municipal Science and Technology Project (Guangzhou EDA Key Laboratory, No.2023A03J0013).

### REFERENCES

- [1] D. Ding *et al.*, "Glow: A global router for low-power thermal-reliable interconnect synthesis using photonic wavelength multiplexing," in *17th Asia and South Pacific Design Automation Conference*, 2012.
- [2] D. Liu *et al.*, "Operon: optical-electrical power-efficient route synthesis for on-chip signals," in *Proceedings of the 55th Annual Design Automation Conference*, 2018.
- [3] F.-Y. Chuang and Y.-W. Chang, "On-chip optical routing with waveguide matching constraints," in *2021 IEEE/ACM International Conference on Computer Aided Design (ICCAD)*, 2021.
- [4] T. Yan and M. D. Wong, "Bsg-route: A length-matching router for general topology," in *2008 IEEE/ACM International Conference on Computer-Aided Design*, 2008.
- [5] P. Sanchis *et al.*, "Low-crosstalk in silicon-on-insulator waveguide crossings with optimized-angle," *IEEE Photonics Technology Letters*, 2007.
- [6] L. McMurchie and C. Ebeling, "Pathfinder: A negotiation-based performance-driven router for fpgas," in *Proceedings of the 1995 ACM third international symposium on Field-programmable gate arrays*, 1995.