NVSRLO: A FeFET-Based Non-Volatile and SEU-Recoverable Latch Design with Optimized Overhead

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***Abstract*—This paper presents a FeFET-based non-volatile and single-event upset (SEU) recoverable latch, namely NVSRLO, which does not require any extra control signals. Simulation results show that the proposed latch provides non-volatility and SEU-recovery with optimized overhead. Compared with existing non-volatile latches, NVSRLO significantly reduces delay, power, and delay-power-area product at the cost of area.**

***Index Terms*—FeFET, non-volatility, single-event upset, error-recovery, latch design.**

I. Introduction

Nowadays, Internet of Things (IoTs) have shown great potential in many applications. They are often designed with no battery or limited capacity of battery, so that energy harvesting becomes indispensable. Non-volatile memory (NVM) retains values in normal operations and it reloads the retained values when power is restored. Currently, many emerging NVMs, such as ferroelectric field effect transistors (FeFETs) based ones, are being developed. Moreover, for the advanced CMOS technologies combined with FeFETs, it is common for them to suffer from the hit of radiative particles causing soft errors [1-3]. There have been many important advances in FeFET-based NVMs and/or radiation-hardened latches [4-9]; however, they still have many drawbacks. In this paper, a FeFET-based non-volatile and SEU-recoverable latch is proposed without the requirement for extra control signals for backup and restart operations. It provides not only non-volatility but also SEU-recovery. It also performs better than many designs in terms of latency and energy overhead.

II. Proposed NVSRLO Design

Figure 1 shows the proposed NVSRLO latch. It comprises two CLK-marked switches, i.e., transmission gates (TGs), a 2-input C-element (CE), a clock-gated (CG) 2-input CE, and two inverters with FeFETs. CLK is the system clock, and NCK is the negative system clock, respectively. When CLK = 1, it works in transparent mode and the TGs are on. When input D = 1, MP1 is turned off and MN1 is turned on. The gate voltage of FeFET1 is high, and the source electrode is discharged to GND through MN1. Thus, the gate-source voltage (V_{GS}) of FeFET1 can reach the positive threshold, so that FeFET1's state becomes LRS, i.e., "1", and N4 becomes 0. Then, MP2 is turned on, MN2 is turned off, so that N1 = 1. Thus, N2 = 0 through CE. Then, the V_{GS} of FeFET2 can reach the negative threshold, so that FeFET2's state becomes HRS, i.e., "0". When CLK = 0, it works in hold mode. The TGs are off and the CG-CE is turned on. The value of input D can no longer pass to N1 and N3. The voltage of N1 is fed by the inverter with FeFET2, and the voltage of N3 is fed by the CG-CE to form feedback loops to retain values. Therefore, the latch can work correctly in normal operations.

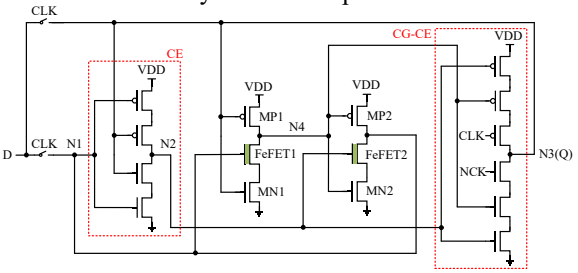

Fig. 1. Schematic of the proposed NVSRLO latch.

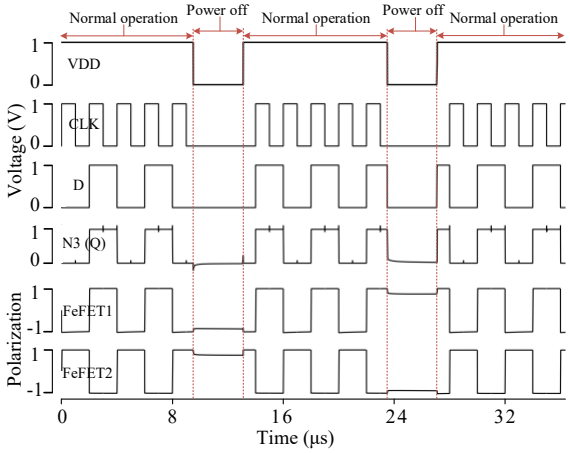

Fig. 2. Simulation waveform of the proposed latch in case of power failures.

The latch has two non-volatile modes, i.e., backup and restore. The states of FeFET change with the input, thus completing the backup operation; when power is restored from a power-down state, the states of FeFETs can write back to determine the recovered state of NVSRLO. When the supply voltage (i.e., VDD) is off, all transistors are turned off and all nodes are back to 0. When VDD is on, the latch enters into restore mode. If N1 = N3 = 1 before power off, FeFET1 is in LRS and FeFET2 is in HRS. In restore operation, when VDD just starts to provide, all nodes are initially at 0, and thus all PMOS are on. Then, the voltages at N1, N2, N3 and N4 also rise. However, since FeFET1 is in LRS, the rising voltage of N3 can turn on MN1, thus preventing the voltage rise of N4. Since FeFET2 is in HRS, it prevents MN2 from affecting N1, so that the voltage at N1 continues rising. Then, N1 and N3 prevent the voltage rise of N2 by CE, which further causes the voltage rise of N3. Eventually, the voltage of N1 and N3 becomes 1, and the voltage of N2 and N4 becomes 0, and all nodes return to the correct states. Note that, if N1 = N3 = 0

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before power off, we can observe similar results. Therefore, the proposed latch can work correctly in non-volatile modes. Figure 2 shows the simulation results of the latch in case of power failures. It can be seen that the latch can work correctly.

A.SEU-Recovery

Clearly, NVSRLO has four nodes (N1 to N4). Due to page limitation, two key cases of SEUs are discussed. **Case S1**: Assuming that an SEU affects N1, its value changes from 0 to 1. CE can block the error at N1 to maintain the correct value of N2. Through feedback loops, N1 restores to its correct value "0". **Case S2**: Assuming that an SEU affects N2, its value changes from 0 to 1. CE-CG can block the error at N2 to maintain the correct value of N3. Through feedback loops, N2 restores to its correct value "0". For the other cases, we can observe similar results. In summary, the latch can provide SEU-recovery. Figure 3 shows the simulation results of SEU-injections for NVSRLO. Clearly, the latch can recover from the injected key SEUs.

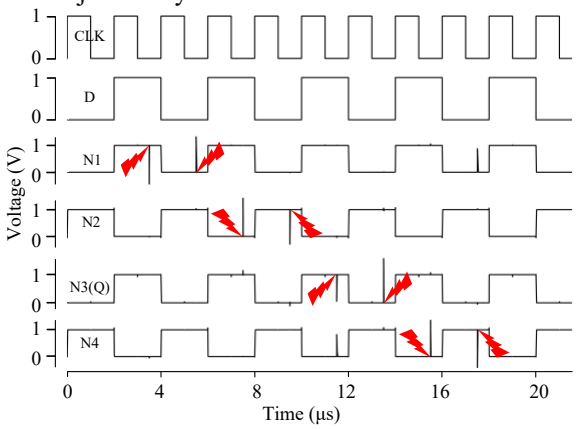

Fig. 3. Simulation waveform with SEU injections for the proposed latch.

III. Comparisons

NVSRLO was designed using a 65 nm CMOS bulk library combined with a FeFET model [9]. VDD = 1V and the operating temperature was 27 ℃. For a fair comparison, we used the same conditions to extract all comparative data. Table I presents the comparison results of latches in terms of whether SEU recoverable (Rec.), non-volatile (NV), and whether no additional control signals (No Ad. Ctrl.) are required. It can be seen that, although the NV-SEU-Latch [8] can provide non-volatility and SEU-recovery, it requires extra transistors/devices as compared to the proposed latch. Clearly, the proposed latch can simultaneously provide SEU recovery and non-volatility with no additional control signals.

Table II presents the overhead comparison of latches in terms of D to Q delay (Delay), average power considering dynamic and static (Power), measured silicon area (Area) and delay-power-area product (DPAP) that is measured by multiplying delay, power and area. Note that, since a FeFET is made with embedding ferroelectric materials in the gate stack of the transistor, its area can be considered as quite similar to a CMOS transistor and can be defined as a standard area. It can be seen from Table II that NVSRLO has the lowest delay due to the fact that the high-speed transmission path from D to Q in the transparent mode is used. As for power, since the proposed latch uses CG without extra control operations, it can reduce the power of the design. However, to provide more features, the proposed latch uses extra devices that cannot reduce power in the lowest level. As a result, the proposed latch has low or moderate power, delay, and DPAP compared to the other latches. Therefore, the proposed latch has even low or balanced overhead with more extra features.

TABLE I
COMPARISON OF ALTERNATIVE LATCHES

Designs	SEU Rec.	NV	No Ad. Ctrl.	Number of Transistors/Devices
FeFET-in-NVFF [4]	×	√	×	11 CMOS +1 FeFET
FeFET-out-NVFF [4]	×	√	×	12 CMOS +1 FeFET
FeFET-in-NVFF [5]	×	√	×	12 CMOS +1 FeFET
Low-area-Latch [6]	×	√	×	12 CMOS +2 FeFET
P-FeFET NV [7]	×	√	√	10 CMOS +2 FeFET
NV-SEU-Latch [8]	√	√	√	26 CMOS +2 FeFET
NVSRL (Proposed)	√	√	√	18 CMOS +2 FeFET

TABLE II
OVERHEAD COMPARISON OF NON-VOLATILE LATCHES

Designs	Delay (ps)	Power (µW)	Area (μm^2)	DPAP
FeFET-in-NVFF [4]	31.70	0.30	0.14	1.33
FeFET-out-NVFF [4]	31.83	0.33	0.15	1.58
FeFET-in-NVFF [5]	32.48	0.43	0.15	2.12
Low-area-Latch [6]	33.83	0.42	0.15	2.13
P-FeFET NV [7]	29.57	0.39	0.14	1.61
NV-SEU-Latch [8]	7.41	1.04	0.32	2.47
NVSRL (Proposed)	7.08	0.33	0.23	0.54

IV. Conclusions

In this paper, we have proposed a FeFET-based non-volatile and SEU-recovery latch without extra control signals with balanced overhead. Simulation results have shown that the latch not only has multiple features but also has optimized overhead. The latch is therefore suitable for applications where energy harvesting and radiation hardening are required.

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