Ferroelectric-Superconducting Synergy for Future Computing

Shamiul Alam and Ahmedullah Aziz
Department of Electrical Engineering and Computer Science, University of Tennessee, Knoxville, TN 37996, USA
Email: salam10@vols.utk.edu and aziz@utk.edu

***Abstract*—Ferroelectric Superconducting Quantum Interference Devices (Fe-SQUIDs) have recently gained attention as a transformative technology for superconducting computing, offering voltage-controlled switching that is essential for large-scale digital circuits. This unique technology has the potential to drive advancements in cryogenic computing by enabling scalable memory systems and voltage-controlled logic circuits. These innovations are critical for the realization of large-scale quantum computers and hold significant promise for high-performance computing and space exploration. In this article, we explore how Fe-SQUIDs, integrated with heater cryotrons (hTrons), can be harnessed to develop key components of computing systems. These include non-volatile memory, voltage-controlled logic circuits, in-memory matrix-vector multiplication systems, and ternary content-addressable memory. We also examine how changes in the key characteristics of Fe-SQUIDs and hTrons influence the performance of these applications, providing insights into the design and optimization of next-generation superconducting hardware.**

Keywords—cryogenic, computing, ferroelectric SQUID, heater cryotron, in-memory computing, logic, memory, superconducting.

I. Introduction

Cryogenic computing systems, operating at or below 4K temperature, have recently earned significant attention with the rapid progress of quantum computing [1]. Suitable cryogenic control processor and memory system can facilitate the scaling of quantum computers up to millions of qubits, which is challenging to achieve with the existing architectures reliant on room temperature (RT) components [2], [3]. The use of RT controller and memory system requires a substantial amount of wires and interconnects to interface with qubits placed at milli-Kelvin temperature [4]. Moreover, this introduces a high temperature gradient between the qubits and the RT components which can lead to significant heat dissipation and can possibly destruct the sensitive qubit states. A suitable cryogenic computing system offers the use of lossless superconducting (SC) wires and interconnects and reduces the thermal gradient to a negligible level.

In addition to quantum computing, cryogenic computing holds great promise for high-performance computing (HPC), addressing the high energy requirement of existing technologies [5]. SC devices and circuits provide fast operation with a speed of hundreds of gigahertz and extremely low energy requirement (sub-attojoule switching energy) [6]. Furthermore, cryogenic computing systems are naturally suited for the exploration of deep space, where ambient temperatures align with the operational condition of SC devices and circuits.

Various technologies have been explored for cryogenic computing, including SC, non-SC, and hybrid approaches [3]. However, all of these suffer from their own challenges. For example, non-SC technologies suffer from high power consumption, low speed, and other challenges resulting from cryogenic temperatures. On the other hand, SC technologies are compatible with the energy budget of cryogenic environment but suffer from poor scalability due to the need for inductors, and limited fanout and cascadability. Hybrid systems attempt to combine the advantages of non-SC and Sc technologies but lack a suitable interface circuit between SC and non-SC circuits.

Recently, the interplay between non-SC ferroelectric materials and SC devices has been utilized to overcome these limitations [7]. Ferroelectric materials introduce the voltage control over the SC to non-SC switching of SC devices, opening up new possibilities in the circuit and system-level. While the non-volatile feature of ferroelectric materials is used to develop a scalable memory system [8], the voltage-controlled superconductivity solves the limited fanout and cascadability issues inherent in current-controlled SC logic circuits [9].

This article presents how this unique Fe-SQUID technology, integrated with another SC device called heater cryotron (hTron) [10], is harnessed to develop key components for cryogenic computing. Specifically, we discuss the designs of a voltage-controlled CMOS-like Boolean logic family [9], [11], a non-volatile memory system [8], a ternary content addressable memory (TCAM) [12], and an in-memory computing system [13]. The contributions of this paper are as follows-

- We provide a comprehensive overview of how the integration of ferroelectric materials with SC devices enables scalable and efficient solutions for cryogenic computing.
- We explore the impacts of different device characteristics of Fe-SQUIDs and hTrons on the performance of different cryogenic circuits.

The rest of the paper is organized as follows: section II provides an overview of two unique technologies, Fe-SQUID and hTron. Section III discusses how these two devices are used to design key components of cryogenic computing. Section IV explores the impact of device properties of Fe-SQUIDs and hTrons on these cryogenic computing components.

II. Device Characteistics of Fe-SQUID and hTron

A. Ferroelectric SQUID

SC devices, such as Josephson junctions (JJs) and SQUIDs, have been widely used in cryogenic applications [14]. However, their reliance on current bias and two-terminal configuration leads to several circuit-level challenges [15]. Therefore, introducing a convenient gating mechanism to achieve voltage-control over superconductivity has been a long pursuit. The recent integration of ferroelectric materials with SQUIDs (Fe-SQUID) addresses this need of voltage-controlled Sc devices [7]. Fig. 1(a) shows the device structure of a Fe-SQUID, where a planar SQUID built with two parallel weak links using 15 nm thick $\alpha Mo_{80}Si_{20}$ SC materials was fabricated on top of a 70 nm thick $PbZr_{0.2}Ti_{0.8}O_3$ (PZT) ferroelectric material. Ferroelectric materials show voltage-controlled non-volatile polarization states, as shown in Fig.

978-3-9826741-0-0/DATE25/© 2025 EDAA

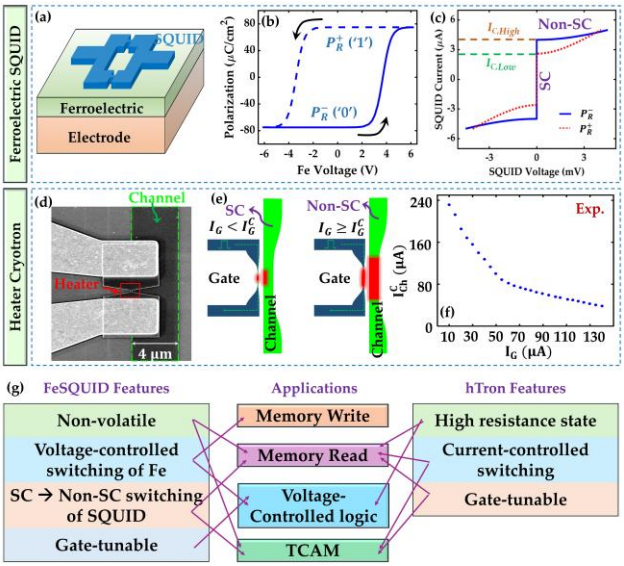

Fig. 1: (a) Device structure, **(b)** polarization vs. voltage characteristics, and (c) I-V characteristics of a Fe-SQUID. **(d)** False-colored SEM image of device structure, **(e)** illustration of gate current-controlled channel switching, and **(f)** gate current-controlled suppressing of channel critical current of a hTron. **(g)** Leveraging different features of Fe-SQUID and hTron to develop key components of cryogenic computing.

1(b), commonly utilized in RT ferroelectric memories [16]. On the other hand, SQUID switches between their SC and resistive states depending on the applied current and its critical current (I_C), illustrated in Fig. 1(c).

Now, when a SQUID is integrated with a ferroelectric material, the polarization state of the ferroelectric affects the surface charge density at the interface. This change in the surface charge density impacts the critical temperature (T_C) and SC energy gap (Δ) of SQUID, governed by Bardeen–Cooper–Schrieffer (BCS) theory [17], [18]-

$$\Delta(T) = 1.763 k_B T_C \tanh\left(2.2\sqrt{\frac{T_C}{T} - 1}\right) \quad (1)$$

where T is the temperature and k_B is the Boltzmann constant. According to Ambegaokar–Baratoff (AB) theory [19], this variation in $\Delta(T)$ affects I_C-

$$I_C(T) = \frac{\pi\Delta(T)}{2q_e R_N}\tanh\left(\frac{\Delta(T)}{2k_B T}\right) \quad (2)$$

where q_e is the electron charge and R_N is the normal state resistance of SQUID. As a result, the two polarization states (negative, P_R^- and positive, P_R^+) lead to two different I_C ($I_{C,high}$ and $I_{C,low}$, respectively), as shown in Fig. 1(c). Now, depending on the applied current, the SQUID shows either SC (zero resistance and zero voltage drop) or resistive (nonzero resistance and nonzero voltage drop) behaviors in its I-V characteristics.

B. Heater Cryotron (hTron)

hTron is a three-terminal SC device which has a gate and a channel formed by two SC nanowires. Gate and channel are separated by a dielectric material. Device structure of a hTron is shown in Fig. 1(d), where WSi and SiO_2 are used as the SC nanowire and dielectric material, respectively. Initially, both gate and channel remain in their SC state, allowing channel current (I_{Ch}) to flows completely through the channel (Fig. 1(e)). However, the gate and channel can be switched to their resistive state by applying high enough currents. To trigger the switching, the applied currents must be greater than the gate and channel critical currents (I_G^C and I_{Ch}^C, respectively).

In this device, the gate acts as the heater for the channel. When a high gate current (I_G) exceeding I_G^C is applied, the gate switches to its resistive state, generating thermal phonons (Fig. 1(e)). These thermal phonons propagate to the channel through the dielectric spacer. This increases the temperature of the channel and reduces the critical current. Therefore, as we keep increasing I_G, more thermal phonons are generated which keep suppressing the superconductivity of the channel. As seen in Fig. 1(f), I_{Ch}^C keeps decreasing with the increase in I_G. Now, for a specific gate current, the decrease in I_{Ch}^C will be sufficient to bring that below the applied channel current and as a result, the channel will switch to its resistive state, driving most of I_{Ch} through the external circuitry.

III. Cryogenic Computing with Fe-SQUID and hTron

Fe-SQUID and hTron provide several unique features compared to JJs and SQUIDs, which can be leveraged to design different key components of cryogenic computing (Fig. 1(g)). For example, the voltage-controlled and gate-tunable superconductivity in Fe-SQUID along with the high resistance state of hTron devices enable the design of a voltage-controlled Boolean logic family. Additionally, the non-volatile nature of ferroelectric materials and energy-efficient switching of SQUID make FeSQUIDs suitable for developing a scalable and energy-efficient memory system. This memory system can further be extended to perform in-memory computing and develop a TCAM. This section discusses the design methodology and working principles of these circuit and system-level implementations.

A. Voltage-controlled Boolean Logic Family [9]

In this logic family, logic states ('0' and '1') are represented with negative (-6 V) and positive (6 V) voltages, respectively. This choice of input voltages avoids the hysteresis region of the ferroelectric material and shows either negative or positive polarization, respectively. Now, if a suitable bias current (in between the two critical current states) is applied to SQUID, we will either get SC or resistive behavior. In the SC state, the applied current flows entirely through the SQUID, while the resistive state of SQUID drives major share of the applied current through the external circuitry. However, the voltages dropped across the load resistor differ from the input voltage levels. Therefore, to ensure seamless integration of multiple logic gates in the cascade fashion, hTron is used. The high resistance state of hTron makes it suitable for this purpose. Using Fe-SQUID and hTron devices, all the basic Boolean logic gates (NOT, AND, and OR) have been designed.

Fig. 2(a) shows the schematic of the designed NOT gate where the gate of hTron is connected in series with the Fe-SQUID. The input voltage is applied to the ferroelectric material of Fe-SQUID which determines its polarization state and the device state of SQUID. For example, when a logic '0' input is applied, it results in the negative polarization of ferroelectric and SC behavior in the SQUID. As a result, the applied current flows through the SQUID and the gate of hTron. This high enough current to the gate of hTron switches its channel to the resistive state, producing a logic '1' at the output. Similarly, for the logic '1' input, the ferroelectric material shows positive polarization and SQUID shows its resistive behavior, driving all the currents through the load resistor. Therefore, the gate of hTron does not get sufficient

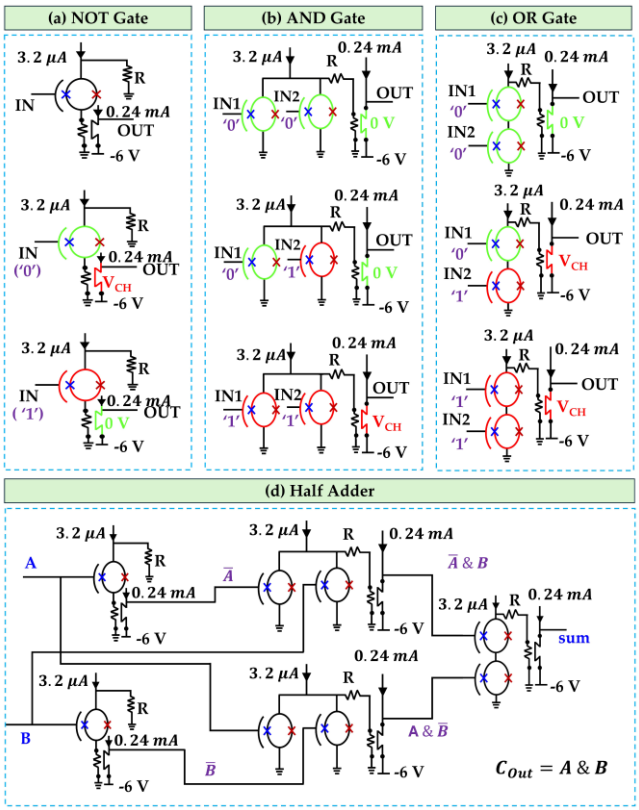

Fig. 2: Circuit schematics and operating principles of Fe-SQUID-based voltage-controlled Boolean **(a)** NOT, **(b)** AND, and **(c)** OR gates [9]. **(d)** Circuit schematic of a half adder using the basic logic gates.

current and the channel remains in its SC state, maintaining a logic '0' at the output.

Figs. 2(b) and (c) show the two-inputs AND and OR gates, respectively where two Fe-SQUIDs are connected in parallel and series, respectively. The gate of hTron is connected in series with the load resistor in these gates. Now, for the AND gate, since two Fe-SQUIDs are connected in parallel, only logic '11' input condition results in the resistive behavior in both Fe-SQUIDs. This drives sufficient current to the gate of hTron to switch its channel to the resistive state (logic '1' output). For all the other input conditions ('00', '01', and '10'), at least one of the Fe-SQUIDs remains in its SC state and takes all the applied current through it. As a result, the gate of hTron does not get enough current and the channel remains in its SC state (logic '0' output). On the other hand, for the OR gate, since two Fe-SQUIDs are connected in series, the resistive behavior of at least one drives the applied current to the load resistor and the hTron gate. Therefore, for '01, '10', and '11' input conditions, the hTron gate gets sufficient current to switch its channel to the resistive state (logic '1' output). Only for '00' input condition, both the Fe-SQUIDs remain superconducting and take the current trough them, keeping the hTron channel in its SC state (logic '0' output).

These voltage-controlled Boolean logic gates solve the single fanout and limited cascadability issues of existing current-controlled SC logic circuits. To demonstrate the fanout capability of these logic gates, a half adder is designed using the basic logic gates, as shown in Fig. 2(d). Fig. 2(e) shows the functional verification of the half adder through experiment-calibrated simulation results where Fe-SQUID and hTron were simulated using developed compact models in previous works.

B. Non-volatile Memory [8]

The non-volatile polarization states of a ferroelectric material are used for data storage in Fe-SQUID-based cryogenic memory, analogous to RT ferroelectric memories. Negative and positive polarization states of the ferroelectric material represent two memory states ('0' and '1', respectively), as shown in Fig. 1(b).

Fig. 3(a) shows the schematic of the memory cell where Fe-SQUID stores the data and a hTron is used as the access device. For write operation in this memory cell, a suitable write voltage, V_{WRITE} (-6 V and +6 V for write '0' and '1', respectively) needs to be applied across the ferroelectric material of the accessed Fe-SQUID. Here, V/2 biasing scheme [20] is used to ensure the successful write operation of the accessed cell only. Table in Fig. 3(b) shows the biasing scheme to write into one specific cell in the memory array by applying different levels of voltage to the write word lines (WWL) and source lines (SL). Due to the choice of V/2 biasing scheme, only the accessed cell gets V_{WRITE} across its ferroelectric, while the half-accessed cells (cells in the same row or column with the accessed cell) get $\frac{V_{WRITE}}{2}$ and the unaccessed cells (other cells in the array) get 0 V. Therefore, this biasing scheme allows writing into the accessed cell only, keeping all the other cells in the array undisturbed.

For the read operation, the SQUID portion of Fe-SQUID is used which is current-controlled. Therefore, hTron is used as the access device to control the direction of the read current. Here, the read current needs to be chosen carefully so that it falls in between the two levels of critical current that we obtain for two polarization states. This choice of read current leads to binary decisions (zero and nonzero voltage) for the two memory states ('0' and '1', respectively). The biasing scheme for the read operation is shown in Fig. 3(b). Here, all the WWLs and SLs are kept at 0 V. Then, suitable currents are applied to the read bit lines (RBL) in a way such that the hTron of the accessed cell remains SC and all the other hTrons become resistive. Then, when the read current is applied to the accessed read word line (RWL), that flows through the accessed cell only. Therefore, based on the memory state stored in the accessed cell, we get either 0 V or some nonzero voltage drop across the cell.

C. Ternary Content Addressable Memory (TCAM) [12]

The Fe-SQUID-based memory cell shown in Fig. 3(a) is further modified to design a TCAM cell. The schematic of the TCAM cell is shown in Fig. 3(c). While one Fe-SQUID is connected in series with one hTron to build a memory cell, two of these memory cells are connected in parallel for performing the TCAM operation. Here, storing data inside the TCAM cells follows the same mechanism of the memory write operation. After storing the data, the TCAM allows to search any combinations of data which are applied with the help of two RBL currents.

This TCAM supports both exact search and hamming distance (HD) calculations, which are selected by choosing a suitable RWL current (3.2 μA and 5 μA per TCAM cell, respectively), as shown in Fig. 3(d). For the exact search mode, the RWL current is chosen in a way so that the Fe-SQUID shows either SC or resistive behavior for logic '0' or '1', respectively. Parallel connection of all the TCAMs in a row ensures that the match line (ML) voltage will be zero if only one Fe-SQUID in that row becomes SC. This provides binary decision- zero voltage for any amount of mismatch or some non-zero voltage for complete match.

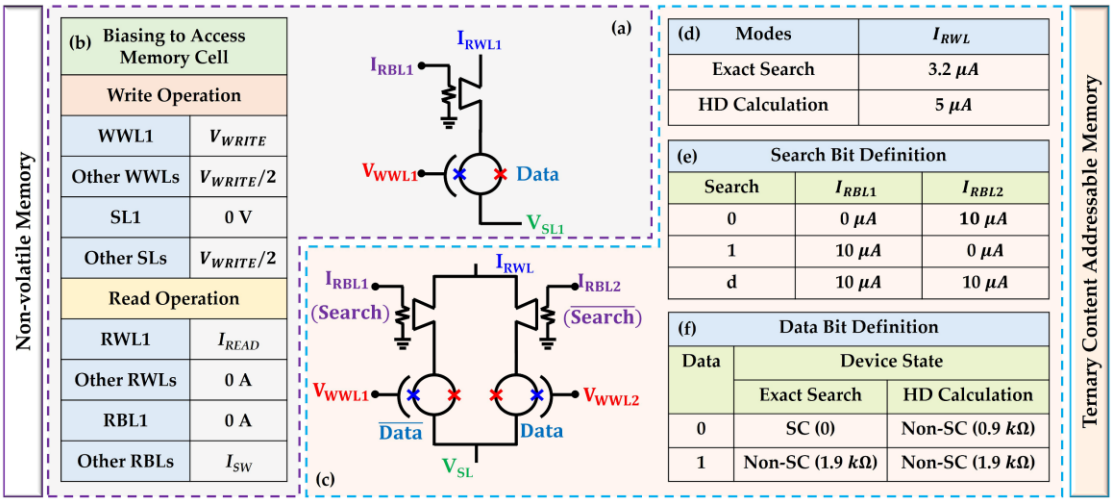

Fig. 3: (a) Circuit schematic of a Fe-SQUID-based memory cell and **(b)** biasing scheme to write into and read from a specific cell in the memory array [8]. **(c)** Circuit schematic and **(d)** operating modes of a TCAM cell. Definitions of **(e)** search and **(f)** data bits [12].

Now, for HD calculation, we want different levels of ML voltage for different amounts of mismatch instead of binary decisions. Therefore, the RWL current needs to be chosen in a way so that no Fe-SQUID shows Sc behavior. In this regard, FeSQUIDs become extremely useful because FeSQUIDs have the capability to show both SC/resistive states and only resistive state with two different resistance values for two states. In the HD calculation mode, the resistive behavior with two resistance values are leveraged and different amounts of mismatch between the search and stored data represent different levels of ML voltage. Figs. 3(e) and (f) show the definitions of search and data bits, respectively.

The search operation in the Fe-SQUID-based TCAM depends on the switching of the SQUID portion of Fe-SQUIDs which provides excellent energy-efficiency. Fe-SQUID-based TCAM consumes an average energy of 1.36 aJ and 26.5 aJ for 1-bit binary and ternary search, respectively. Compared with the cryogenic 5 nm FinFET SRAM-based TCAM [21], Fe-SQUID-based TCAM needs over one order of magnitude lower energy to perform hyperdimensional computing-based language recognition task.

D. In-memory Matrix-Vector-Multiplication [13]

In-memory computing provides better performance in terms of energy efficiency and latency compared to traditional *von Neumann* architectures with physically separate memory and processing units [22]. A suitable in-memory computing system at cryogenic environment can be useful for more efficient implementations of machine learning algorithms, which have proven to be useful for control [23] and quantum error correction [24] of qubits. Moreover, the amount of coolant (determining factor of cooling cost) required to maintain a cryogenic temperature increases exponentially with the power consumption of the cooled system [25]. A suitable cryogenic in-memory computing system can reduce the power consumption and hence, can help reduce the cooling cost. Fe-SQUID-based memory system has been modified to perform in-memory matrix-vector-multiplication (MVM), the most frequently performed operation in machine learning algorithms.

Fig. 4(a) shows the Fe-SQUID-based memory system incorporating modified peripheral circuitry to perform MVM. Here, the input matrix ($[I_1\ I_2\ I_3\ \dots\ I_n]$) is represented by

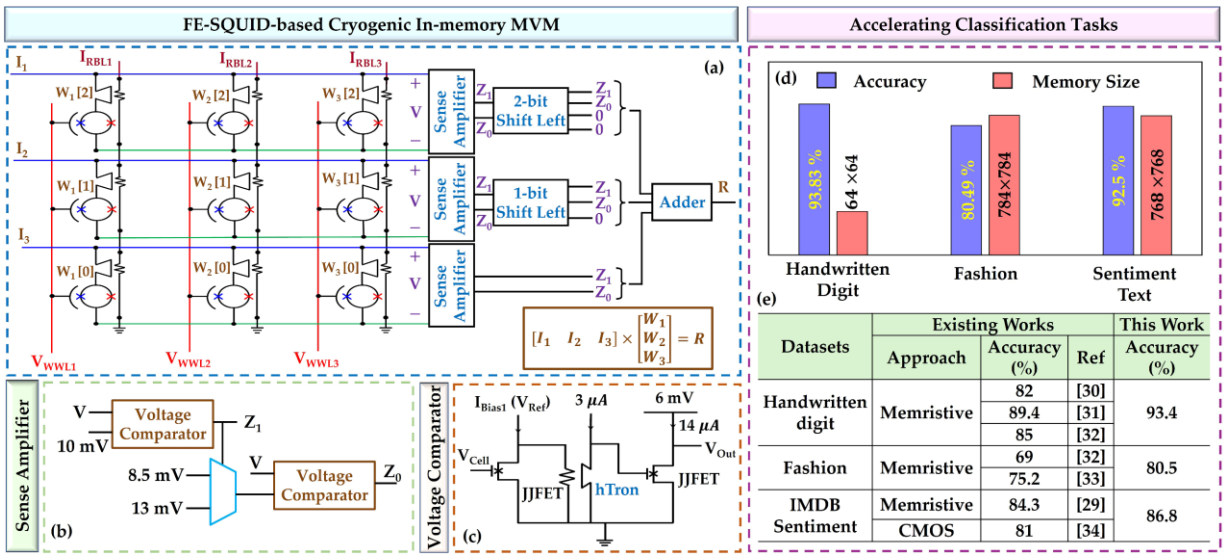

Fig. 4: Schematics of **(a)** Fe-SQUID-based in-memory MVM system [13], (b) a sense amplifier, and (c) a voltage comparator. (d) Accuracy achieved for the three classification tasks. (e) Comparison of Fe-SQUID-based system with existing CMOS and memristor-based approaches.

read currents applied to the RWLs, while the weight matrix corresponds to data stored in the memory cells. Each weight matrix element is mapped to a single column, with the most significant bit (MSB) stored in the first row and the least significant bit (LSB) in the last row of the column. When read currents are applied, the interaction between these currents and the stored data generates distinct voltage levels across each row, which are then processed by sense amplifiers. In a 3×3 memory array, the sense amplifier for each row produces a two-bit output. Fig. 4(b) shows the sense amplifier design, comprising two voltage comparators with appropriate reference voltages and a 2:1 multiplexer for selecting the reference voltage for the second comparator. Fig. 4(c) shows the schematic of the Josephson junction FET-based voltage comparator [26] used in the system. Finally, two left shifters are used for the first and second rows, and the outputs of all the rows are added to compute the MVM output.

This in-memory MVM system is then used to perform different classification tasks utilizing hardware-software co-design approach. The tasks include classifying the MNIST handwritten digit dataset [27], MNIST fashion dataset [28], and IMDB sentiment text dataset [29]. For each task, the Fe-SQUID-based in-memory MVM system demonstrates reasonable accuracy with a realistic memory size, as shown in Fig. 4(d). Additionally, the system's performance is compared against RT CMOS and memristor-based approaches. As shown in Fig. 4(e), the Fe-SQUID-based system outperformed all existing approaches [29]–[34], achieving better accuracy in all the classification tasks.

IV. Impacts of Device Characteristics on Applications

This section examines how changes in different device characteristics of Fe-SQUID and hTron impact the performance of different cryogenic computing applications. Table I provides a qualitative summary showing the effects of major device properties on the performance of voltage-controlled logic, memory, TCAM, and in-memory MVM systems.

Table I: Impact of Device Characteristics on performance of different applications

Device	Characteristics	Desired for applications			
		Memory	Logic	In-memory MVM	TCAM
Fe-SQUID	Fe coercive voltage	High	Low	High	High
	Fe polarization	High	High	High	High
	SQUID critical current	Low	Low	Low	Low
	SQUID resistance	High	High	High	High
hTron	Channel resistance	No effect	High	No effect	High
	Gate critical current	Low	No effect	Low	Low
	Channel critical current	Low	Low	Low	Low

Higher coercive voltage of the ferroelectric material improves the reliability and robustness of memory, TCAM, and in-memory computing systems. However, this requires larger input voltage levels for logic circuits which increases the switching energy. On the other hand, higher polarization value of the ferroelectric improves the performance of all the applications since this strengthens the differentiation between two logic states. For the SQUID portion of Fe-SQUID, higher critical current levels necessitate larger bias currents for all the applications which lead to higher power and energy consumption. In contrast, increased SQUID resistance benefits all the applications by enhancing the distinguishability of voltage levels corresponding to two logic states for the memory and in-memory applications. It also improves the fanout and cascadability of the logic circuits.

Regarding hTron, higher channel resistance does not have any impact on the memory and in-memory computing system because these operations rely on switching between superconducting (SC) and resistive states rather than absolute resistance levels. However, increased channel resistance improves the performance of logic circuits and TCAM by enabling the use of lower channel currents. In addition, the gate and channel critical currents of hTron influence the choice of bias currents. Higher critical currents necessitate the use of higher bias currents which lead to increased power and energy consumption.

V. Conclusion

This article presented an overview of how the integration of non-SC ferroelectric materials with SC devices can be harnessed to design key components for cryogenic computing. Fe-SQUID-based cryogenic computing systems not only offer superior performance but also address critical challenges faced by current cryogenic technologies. Consequently, these innovative technologies pave the way for scalable and efficient cryogenic processing and memory systems, making them highly applicable for quantum computing, high-performance computing, deep space exploration, and other advanced cryogenic applications. Additionally, we analyzed how changes in device characteristics impact the performance of both circuit-level and system-level implementations.

References

[1] G. Wendin and V. S. Shumeiko, "Quantum bits with Josephson junctions (Review Article)," *Low Temperature Physics*. 2007, doi: 10.1063/1.2780165.

[2] J. M. Hornibrook, J. I. Colless, I. D. C. Lamb, S. J. Pauka, H. Lu, A. C. Gossard, J. D. Watson, G. C. Gardner, S. Fallahi, M. J. Manfra, and D. J. Reilly, "Cryogenic Control Architecture for Large-Scale Quantum Computing," 2015, doi: 10.1103/PhysRevApplied.3.024010.

[3] S. Alam, M. S. Hossain, S. R. Srinivasa, and A. Aziz, "Cryogenic memory technologies," *Nat. Electron. 2023 63*, vol. 6, no. 3, pp. 185–198, Mar. 2023, doi: 10.1038/s41928-023-00930-2.

[4] P. R. Genssler, F. Klemme, S. S. Parihar, S. Brandhofer, G. Pahwa, I. Polian, Y. S. Chauhan, and H. Amrouch, "Cryogenic Embedded System to Support Quantum Computing: From 5-nm FinFET to Full Processor," *IEEE Trans. Quantum Eng.*, vol. 4, 2023, doi: 10.1109/TQE.2023.3300833.

[5] R. N. Das, V. Bolkhovsky, S. K. Tolpygo, P. Gouker, L. M. Johnson, E. A. Dauler, and M. A. Gouker, "Large Scale Cryogenic Integration Approach for Superconducting High-Performance Computing," *Proc. - Electron. Components Technol. Conf.*, pp. 675–683, Aug. 2017, doi: 10.1109/ECTC.2017.54.

[6] G. Krylov and E. G. Friedman, *Single Flux Quantum Integrated Circuit Design*. 2022.

[7] M. Suleiman, M. F. Sarott, M. Trassin, M. Badarne, and Y. Ivry, "Nonvolatile voltage-tunable ferroelectric-superconducting quantum interference memory devices," *Appl. Phys. Lett.*, vol. 119, no. 11, p. 112601, Sep. 2021, doi: 10.1063/5.0061160.

[8] S. Alam, M. M. Islam, M. S. Hossain, K. Ni, V. Narayanan, and A. Aziz, "Cryogenic Memory Array based on Ferroelectric SQUID and Heater Cryotron," *2022 Device Res. Conf.*, pp. 1–2, Jun. 2022, doi: 10.1109/DRC55272.2022.9855813.

[9] S. Alam, M. S. Hossain, K. Ni, V. Narayanan, and A. Aziz, "Voltage-controlled cryogenic Boolean logic gates based on

ferroelectric SQUID and heater cryotron," *J. Appl. Phys.*, vol. 135, no. 1, p. 14903, Jan. 2024, doi: 10.1063/5.0172531/2932581.

[10] A. N. McCaughan and K. K. Berggren, "A superconducting-nanowire three-terminal electrothermal device," *Nano Lett.*, 2014, doi: 10.1021/nl502629x.

[11] S. Singh Parihar, F. Klemme, S. Alam, A. Aziz, Y. S. Chauhan, H. Amrouch, G. Student Member, S. Member, and Y. Singh Chauhan, "Modeling and Evaluating Superconducting Ferroelectric SQUID Circuits," *Authorea Prepr.*, Sep. 2024, doi: 10.36227/TECHRXIV.172651772.28145900/V1.

[12] S. Alam, S. Thomann, S. S. Parihar, Y. S. Chauhan, K. Ni, H. Amrouch, and A. Aziz, "Energy-Efficient Cryogenic Ternary Content Addressable Memory using Ferroelectric SQUID," *ArXiV Prepr.*, Oct. 2024, doi: 10.48550/arXiv.2410.11091.

[13] S. Alam, J. Hutchins, M. S. Hossain, K. Ni, V. Narayanan, and A. Aziz, "Cryogenic In-Memory Matrix-Vector Multiplication using Ferroelectric Superconducting Quantum Interference Device (FE-SQUID)," in *2023 60th ACM/IEEE Design Automation Conference (DAC)*, 2023, pp. 1–6, doi: 10.1109/DAC56929.2023.10247669.

[14] K. K. Likharev, "Superconductor digital electronics," *Phys. C Supercond. its Appl.*, 2012, doi: 10.1016/j.physc.2012.05.016.

[15] S. Alam, D. S. Rampini, B. G. Oripov, A. N. McCaughan, and A. Aziz, "Cryogenic reconfigurable logic with superconducting heater cryotron: Enhancing area efficiency and enabling camouflaged processors," *Appl. Phys. Lett.*, vol. 123, no. 15, Oct. 2023, doi: 10.1063/5.0170187.

[16] J. Vaidya, R. S. S. Kanthi, S. Alam, N. Amin, A. Aziz, and N. Shukla, "A three-terminal non-volatile ferroelectric switch with an insulator–metal transition channel," *Sci. Reports 2022 121*, vol. 12, no. 1, pp. 1–7, Feb. 2022, doi: 10.1038/s41598-021-03560-w.

[17] J. Bardeen, L. N. Cooper, and J. R. Schrieffer, "Theory of superconductivity," *Phys. Rev.*, 1957, doi: 10.1103/PhysRev.108.1175.

[18] S. Alam, M. A. Jahangir, and A. Aziz, "A Compact Model for Superconductor- Insulator-Superconductor (SIS) Josephson Junctions," *IEEE Electron Device Lett.*, vol. 41, no. 8, pp. 1249–1252, 2020, doi: 10.1109/LED.2020.3002448.

[19] V. Ambegaokar and A. Baratoff, "Tunneling between superconductors," *Phys. Rev. Lett.*, 1963, doi: 10.1103/PhysRevLett.11.104.

[20] S. Alam, M. S. Hossain, and A. Aziz, "A non-volatile cryogenic random-access memory based on the quantum anomalous Hall effect," *Sci. Rep.*, vol. 11, no. 1, pp. 1–9, 2021, doi: 10.1038/s41598-021-87056-7.

[21] S. S. Parihar, S. Thomann, G. Pahwa, Y. S. Chauhan, and H. Amrouch, "5nm FinFET Cryogenic SRAM Evaluation for Quantum Computing," *Device Res. Conf. - Conf. Dig. DRC*, vol. 2023-June, 2023, doi: 10.1109/DRC58590.2023.10186959.

[22] T. Soliman, F. Muller, T. Kirchner, T. Hoffmann, H. Ganem, E. Karimov, T. Ali, M. Lederer, C. Sudarshan, T. Kampfe, A. Guntoro, and N. Wehn, "Ultra-low power flexible precision FeFET based analog in-memory computing," *Tech. Dig. - Int. Electron Devices Meet. IEDM*, vol. 2020-December, pp. 29.2.1-29.2.4, Dec. 2020, doi: 10.1109/IEDM13553.2020.9372124.

[23] X. M. Zhang, Z. Wei, R. Asad, X. C. Yang, and X. Wang, "When does reinforcement learning stand out in quantum control? A comparative study on state preparation," *npj Quantum Inf. 2019 51*, vol. 5, no. 1, pp. 1–7, Oct. 2019, doi: 10.1038/s41534-019-0201-8.

[24] P. Wang, X. Peng, W. Chakraborty, A. I. Khan, S. Datta, and S. Yu, "Cryogenic benchmarks of embedded memory technologies for recurrent neural network based quantum error correction," *Tech. Dig. - Int. Electron Devices Meet. IEDM*, vol. 2020-December, pp. 38.5.1-38.5.4, Dec. 2020, doi: 10.1109/IEDM13553.2020.9371912.

[25] A. Nordlund, M. Harrison, and J. Gess, "Viability of Cryogenic Cooling to Reduce Processor Power Consumption," *J. Electron. Packag.*, vol. 143, no. 4, Dec. 2021, doi: 10.1115/1.4051752/1114542.

[26] S. Alam, M. M. Islam, M. S. Hossain, and A. Aziz, "Superconducting Josephson Junction FET-based Cryogenic Voltage Sense Amplifier," *2022 Device Res. Conf.*, pp. 1–2, Jun. 2022, doi: 10.1109/DRC55272.2022.9855654.

[27] L. Deng, "The MNIST database of handwritten digit images for machine learning research," *IEEE Signal Process. Mag.*, vol. 29, no. 6, pp. 141–142, 2012, doi: 10.1109/MSP.2012.2211477.

[28] H. Xiao, K. Rasul, and R. Vollgraf, "Fashion-MNIST: a Novel Image Dataset for Benchmarking Machine Learning Algorithms," *ArXiV Prepr.*, Aug. 2017, doi: 10.48550/arxiv.1708.07747.

[29] S. Wen, H. Wei, Y. Yang, Z. Guo, Z. Zeng, T. Huang, and Y. Chen, "Memristive LSTM Network for Sentiment Analysis," *IEEE Trans. Syst. Man, Cybern. Syst.*, vol. 51, no. 3, pp. 1794–1804, Mar. 2021, doi: 10.1109/TSMC.2019.2906098.

[30] F. Liu, C. Liu, and F. Bi, "A Memristor based Unsupervised Neuromorphic System Towards Fast and Energy-Efficient GAN," May 2018, doi: 10.48550/arxiv.1806.01775.

[31] M. Shahsavari, P. Falez, and P. Boulet, "Combining a volatile and nonvolatile memristor in artificial synapse to improve learning in Spiking Neural Networks," *Proc. 2016 IEEE/ACM Int. Symp. Nanoscale Archit. NANOARCH 2016*, pp. 67–72, Sep. 2016, doi: 10.1145/2950067.2950090.

[32] Y. Wei, Q. Duan, R. Yuan, X. Yan, and Y. Yang, "Dropout neuronal unit with tunable probability based on NbOx stochastic memristor for efficient suppression of overfitting," *Microelectron. Eng.*, vol. 259, p. 111778, Apr. 2022, doi: 10.1016/J.MEE.2022.111778.

[33] P. Zhou, J. K. Eshraghian, D.-U. Choi, and S.-M. Kang, "SPICEprop: Backpropagating Errors Through Memristive Spiking Neural Networks," Mar. 2022, doi: 10.48550/arxiv.2203.01426.

[34] C. Chen, H. Ding, H. Peng, H. Zhu, Y. Wang, and C. J. R. Shi, "OCEAN: An On-Chip Incremental-Learning Enhanced Artificial Neural Network Processor with Multiple Gated-Recurrent-Unit Accelerators," *IEEE J. Emerg. Sel. Top. Circuits Syst.*, vol. 8, no. 3, pp. 519–530, Sep. 2018, doi: 10.1109/JETCAS.2018.2852780.