

Analysis and Design of Novel Three Phase Modified Impedance Source Inverters for Renewable Energy Resources

A report submitted in partial fulfilment of the requirements for the award of the degree of

B. Tech in Electrical Engineering

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Spring, 2020-2021

Declaration by the Students

We hereby declare that the project work presented in this report entitled "**Analysis and Design of Novel Three Phase modified Impedance Source Inverters for Renewable Energy Resources**", submitted in partial fulfilment for the award of the degree of Bachelor of Technology in Electrical Engineering, Tezpur University during the period from January 2021 to June 2021, has been carried out by us and that it has not been submitted in part or whole elsewhere for the award of any other degree or diploma.

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This is to certify that the report entitled "**Analysis and Design of Novel Three Phase modified Impedance Source Inverters for Renewable Energy Resources**", submitted to the Department of Electrical Engineering, Tezpur University in partial fulfilment for the award of the degree of Bachelor of Technology in Electrical Engineering, is a record of project work carried out by

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under my supervision during the period from January 2021 to June 2021. All support received by them from various sources have been duly acknowledged. No part of this report has been submitted elsewhere for the award of any other degree or diploma to the best of my knowledge.

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and submitted in partial fulfilment for the award of the degree of Bachelor of Technology in Electrical Engineering, Tezpur University during the period from January 2021 to June 2021. They have carried out their project work under the supervision of **Dr. Anish Ahmad, Assistant Professor, Department of Electrical Engineering, Tezpur University, Assam.**

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Acknowledgement

It is our privilege to express our sincerest regards to our project supervisor in-charge, Dr. Anish Ahmad for his valuable inputs, able guidance, encouragement, whole-hearted cooperation and constructive criticism throughout the duration of our project.

We deeply express our sincere thanks to our Head of Department Prof. Soumik Roy for encouraging and allowing us to present the project on the topic "**Analysis and Design of Novel Three Phase modified Impedance Source Inverters for Renewable Energy Resources**" at our department premises for the partial fulfillment of the requirements leading to the award of B-Tech degree.

Our thanks and appreciations go to the project partners in developing the project and people who have willingly helped us out with their abilities. We take this opportunity to thank all our lecturers who have directly or indirectly helped throughout our project.

Last but not the least we express our thanks to our friends for their cooperation and support.

Abstract

The project highlights the importance of conventional inverters like the VSI and CSI. It also depicts the disadvantages it holds. Due to the disadvantages, a new type of inverter was made known as the Impedance source inverter (Z-Source Inverter or ZSI). It employs a unique impedance network to couple the converter main circuit to the power source, load or another converter, for providing unique features that cannot be observed in traditional inverters. The main advantage it held was that it has a single power conversion stage. However, it too has its disadvantages.

With the improvement of technology, the disadvantages of Impedance Source Inverters were also minimized and hence the inverter called Quasi Z Source Inverter came into existence. This inverter gives us the freedom of using different values for inductors and capacitors, unlike ZSI. It also has a lower capacitor voltage stress and high efficiency. However, the boost capability is still low and renewable energy resources need to operate on a higher duty cycle to achieve the voltage requirements.

To overcome these drawbacks, a modified switched boost is very effective to achieve high voltage gain as compared to the conventional qZSIs. In the project, a novel modified switched boost family of ZSIs are presented for renewable energy resource applications. The proposed ZSIs uses the same philosophy as in a modified switched-Z Source Inverter, but each of them has got its own advantages regarding the continuous input current or discontinuous input current, voltage and current stresses and efficiency. The passive components and numbers of switched are also the same.

In this project, detailed analysis of proposed ZSIs is analyzed. The detailed steady-state analysis, comparative analysis, simulation, PCB design using Eagle software (fee version) are carried out. Moreover, the digital control is being used to generate the PWM signals using the help of a DSP kit TMS320F28335 from Texas Instruments. It has been coded using the Code Composer Studio.

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CHAPTER 1 – INTRODUCTION

Power Electronics refers to an interdisciplinary subject within electrical engineering that deals with the design, control and conversion of power in its electric form. A system that converts electric energy to an electric load through a control circuit known as a Power Electronic System. Power electronics is an essential part of many devices and systems in one or more of their phases. It deals with conversion of electrical energy of one type into another with different characteristics and used to drive any device that requires an input of electric power other than that supplied by the primary power source [1].

However, that is just the technical explanation of engineering power electronics. As COVID-19 continues to spread throughout the world, we have worked on the topic Inverters in our final year B. Tech studies.

The main motive of doing research on Inverters is because it is a useful electronic device that changes direct supply voltage (DC) to Alternating supply voltage (AC). Since we have mainly focused on three phase inverters, which are generally used for high power applications. The three-phase square wave inverter can be used to generate balanced three phase ac voltages with desired frequency. However harmonic voltages of 3rd, 5th and other non-triplet odd multiples of fundamental frequency distorts the output voltages. These distortions are very difficult to remove. We design different filters to remove these distortions but it is very tedious task. There are some other kinds of inverters such as pulse width modulated (PWM) inverters, which can provide a higher quality of output voltage [1].

A three-phase inverter working principle is, it includes three inverter switches with single-phase where each switch can be connected to load terminal. For the basic control system, the three switches operation can be synchronized so that single switch works at every 60 degrees of basic output waveform to create a line-to-line output waveform including six steps. This waveform includes a zero-voltage stage among the two sections like positive and negative of the square-wave. Once PWM techniques based on the carrier are applied to these waveforms, then the basic shape of the waveform can be taken so that the third harmonic including its multiples will be canceled [2]. In a 3 phase, the power can be transmitted across the network with the help of three different currents, which are out of phase with each other, whereas in single-phase inverter, the power can transmit through a single phase.

CHAPTER 2 - INVERTER TOPOLOGY

Inverters are classified into two main categories –

- **Voltage Source Inverter** VSI – The voltage source inverter has stiff DC source voltage that is the DC voltage has limited or zero impedance at the inverter input terminals.
- **Current Source Inverter** CSICSI – A current source inverter is supplied with a variable current from a DC source that has high impedance. The load does not influence the resulting current waves.

2.1 VOLTAGE SOURCE INVERTER

The figure shows the traditional single-phase voltage source converter (abbreviated as V source converter) structure. A dc voltage source supported by a relatively large capacitor feeds the main converter circuit, a single-phase bridge. The dc voltage source can be a battery, fuel stack, diode rectifier, and/or capacitor. Four switches are used in the main circuit; each is traditionally composed of a power transistor and an anti-parallel (or freewheeling) diode to provide bidirectional current flow and unidirectional voltage blocking capability.

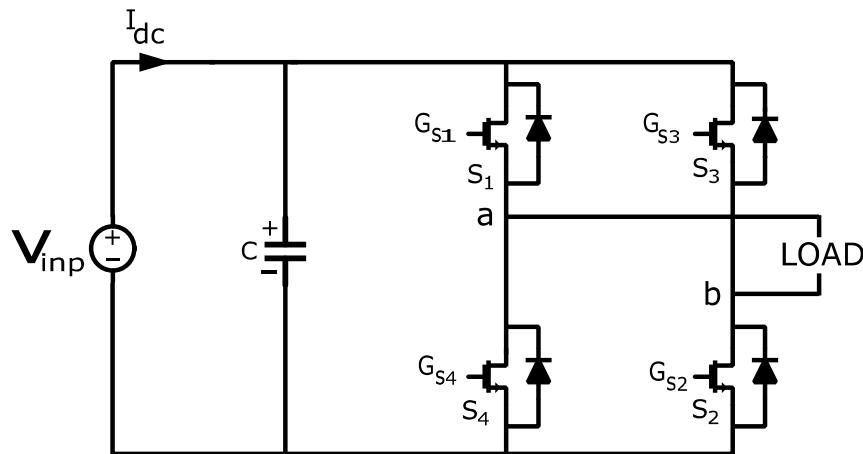


Figure 2.1: Traditional Voltage Source Inverter

The V-Source converter is widely used. It, however, has the following conceptual and theoretical barriers and limitations. [3]. Fig 2.1 shows a traditional voltage source inverter.

- The ac output voltage is limited below and cannot exceed the dc-rail voltage or the dc-rail voltage has to be greater than the ac input voltage. Therefore, the voltage source inverter is a buck (step-down) inverter for dc-to-ac power conversion, and the voltage source converter is a boost (step-up) rectifier (or boost converter) for ac-to-dc power conversion. For applications where overdrive is desirable and the available dc voltage is limited, an additional dc-dc boost converter is needed to obtain the desired ac output. The additional power converter stage increases system cost and lowers efficiency.

- The upper and lower devices of each phase leg cannot be gated simultaneously either by purpose or by EMI noise. Otherwise, a shoot-through would occur and destroy the device. Dead time to block both upper and lower devices has to be provided in the voltage source converter, which causes waveform distortion, etc.
- An output LC filter is needed for providing a sinusoidal voltage compared with the current source inverter which causes additional power loss and control complexity.

2.2 CURRENT SOURCE INVERTER

The figure shows the traditional single-phase current source converter (abbreviated as I-source converter) structure. A DC source feeds the main converter circuit, a single-phase bridge. The DC source can be a relatively large dc inductor fed by a voltage source such as a battery, fuel-cell stack, diode rectifier, or thyristors converter. Four switches are used in the main circuit; each is traditionally composed of a semiconductor-switching device with reverse block capabilities such as a gate-turn-off thyristor (GTO) and silicon controlled rectifier (SCR) or a power transistor with a series diode to provide unidirectional current flow and bidirectional voltage blocking.

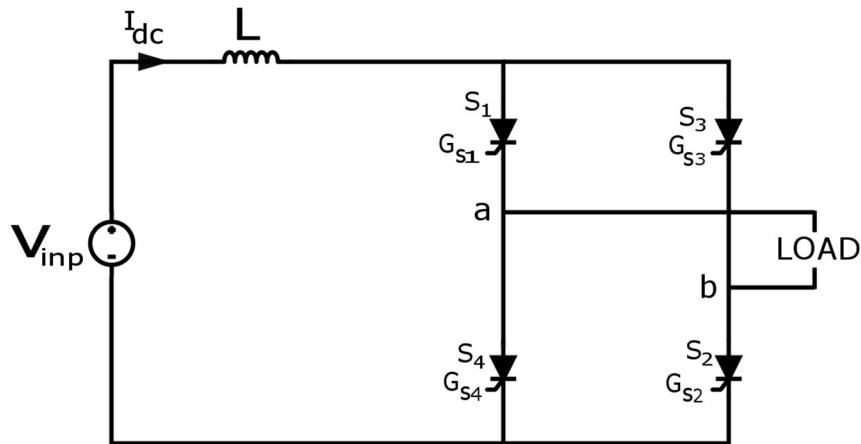


Figure 2.2: Traditional Current Source Inverter

However, the current source converter has the following conceptual and theoretical barriers and limitations. [3].

- The ac output voltage has to be greater than the original dc voltage that feeds the dc inductor or the dc voltage produced is always smaller than the ac input voltage. Therefore, the current source inverter is a boost inverter for dc-to-ac power conversion, and the current source converter is a buck rectifier (or buck converter) for ac-to-dc power conversion. For applications where a wide voltage range is desirable, an additional dc-dc buck (or boost) converter is needed. The additional power conversion stage increases system cost and lowers efficiency.

- The main switches of the current source converter have to block reverse voltage that requires a series of the diode to be used in combination with high-speed and high-performance transistors such as insulated gate bipolar transistors (IGBTs). This prevents the direct use of low-cost and high-performance IGBT modules and intelligent power modules (IPMs).

Table 2.1 gives us the comparative study between VSI and CSI.

Table 2.1: Comparison between VSI and CSI [4]

VSI	CSI
VSI is fed from a DC voltage source having small or negligible impedance.	CSI is fed with adjustable current from a DC voltage source of high impedance
Input voltage is maintained constant	The input current is constant but adjustable.
Output voltage does not dependent on the load	The amplitude of output current is independent of the load.
The waveform of the load current as well as its magnitude depends upon the nature of load impedance.	The magnitude of output voltage and its waveform depends upon the nature of the load impedance
VSI requires feedback diodes	The CSI does not require any feedback diodes.
The commutation circuit is complicated	Commutation circuit is simple as it contains only capacitors.
Power BJT, Power MOSFET, IGBT, and GTO with self-commutation can be used in the circuit.	They cannot be used, as these devices have to withstand reverse voltage.

2.3 PWM INVERTER

Pulse Width Modulated inverters (PWM inverter) replaced the older versions of inverters and has a wide range of applications. Practically these are used in the power electronics circuits. The inverters based on the PWM technology possess MOSFETs in the switching stage of the output. Most of the inverters available nowadays possess this PWM technology and are capable of producing ac voltage for varying magnitudes and frequencies available in [5]. There are multiple protection and control circuits in these types of inverters. The implementation of PWM technology in the inverters makes it suitable and ideal for the distinct loads connected.

There are two well-known switching schemes for the standard H-bridge inverter: Bipolar voltage switching and unipolar voltage switching.

Bipolar switching: is a two-level switching technique that is based on sending two polarity voltage carriers. By closing, one switch with its diagonal counterpart in an inverter the current will flow to the load. By using this method, the output voltage of each leg sends half of the input voltage.

Unipolar switching: is a multi-level switching technique that has a third switching stage where the V_{tri} is compared with the V_{ref} and $-V_{ref}$ simultaneously. This allows the top switches or the two lower switches to be closed at the same time, which will set the output voltage to zero. This method will yield a softer transition between the output peaks, thanks to the zero stage. The switching frequency can then be increased to the double compared with the bipolar switching frequency and decrease the harmonic distortions

All the traditional pulse-width-modulation (PWM) schemes can be used to control the Z-source inverter and their theoretical input-output relationships still hold. To operate the ZSI we can use a traditional PWM switching sequence based on the triangular carrier method. In every switching cycle, the two non-shoots through zero states are used along with two adjacent active states to synthesize the desired voltage. When the dc voltage is high enough to generate the desired ac voltage, the traditional PWM is used. While the dc voltage is not enough to directly generate the desired output ac voltage, a modified PWM with shoot-through zero states will be used to boost voltage.

Fig 2.3 and 2.4 shows the waveforms of Bipolar and Unipolar modulation schemes.

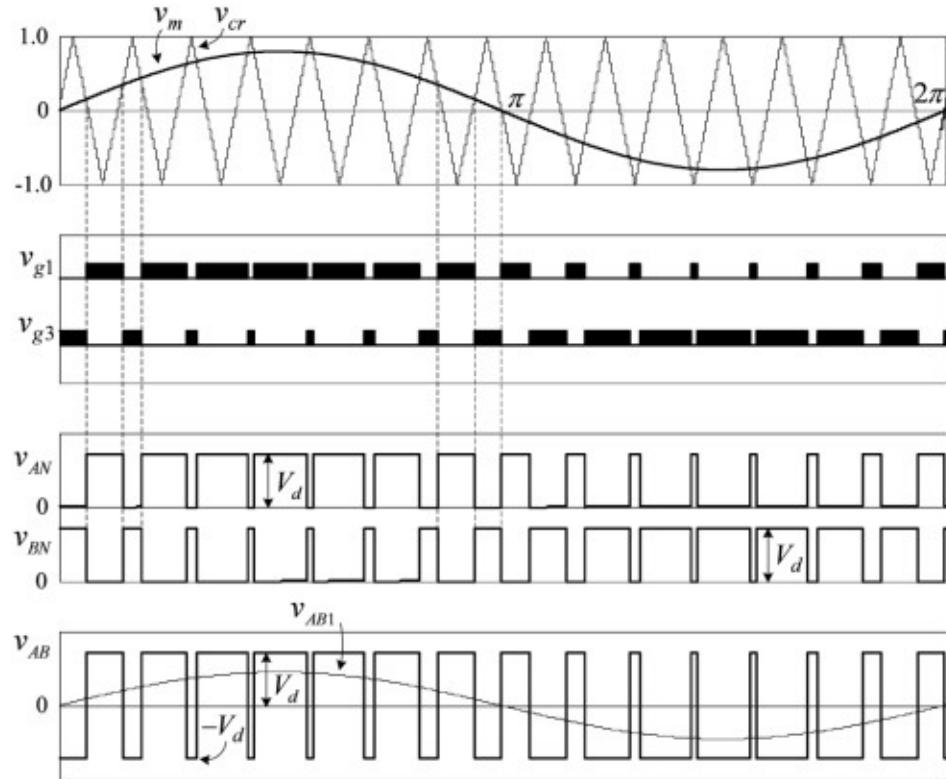


Figure 2.3: Waveform of Bipolar Modulation Scheme [6]

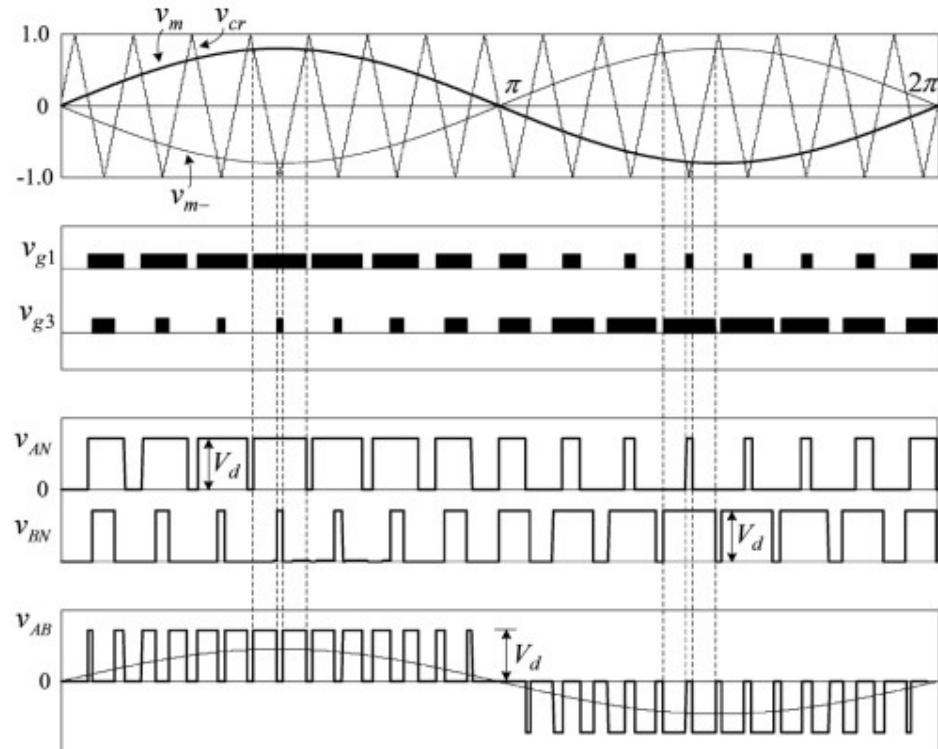


Figure 2.4: Waveform of Unipolar Modulation Scheme [6]

2.4 DRAWBACKS OF CONVENTIONAL TOPOLOGIES

Both the voltage source converter and the current source converter have the following common problems.

- They are either a boost or a buck converter and cannot be a buck-boost converter. That is, their obtainable output voltage range is limited to either greater or smaller than the input voltage.
- The VSI is a buck (down) inverter where AC output voltage cannot exceed DC input voltage. CSI is a boost (up) inverter where the AC output voltage is always greater than the DC voltage feeding the inductor. For applications exceeding the available voltage range an additional boost (or buck), DC/DC converter is needed. This increases system cost and decreases efficiency.
- Their main circuits cannot be interchangeable. In other words, the voltage source converter main circuit can be used neither for the current source converter or vice versa.
- For a VSI, the upper and lower switches cannot be on simultaneously, which may cause a short circuit. On the other hand, for a CSI one of the upper switches and one of the lower switches have to be on to provide a path for the continuous input current. The VSI(CSI) requires dead time (overlap time) to provide safe commutation, which causes waveform distortion.
- In a CSI, switch implementation requires diodes in series with the switches. This prevents the use of low-cost switches that come with anti-parallel diodes implementation, as is usually manufactured.

CHAPTER 3 - INVERTER TOPOLOGIES LITERATURE REVIEW

A new type of converter in power conversion, Z source converter (ZSC) was introduced in 2002, which has unique features that can overcome the limitations of VSI and CSI. This chapter introduces Z-source Inverter and its other modified versions along with the Continuous Current Quasi Z Source Inverter or impedance source power converter and its control method for implementing dc-to-ac power conversion. It employs a unique impedance network (or circuit) to couple the converter main circuit to the power source, load, or another converter, for providing unique features that cannot be observed in the traditional V- and I-source converters where a capacitor and inductor are used, respectively. Figure 3.1 shows the general configuration of a Z- source converter.

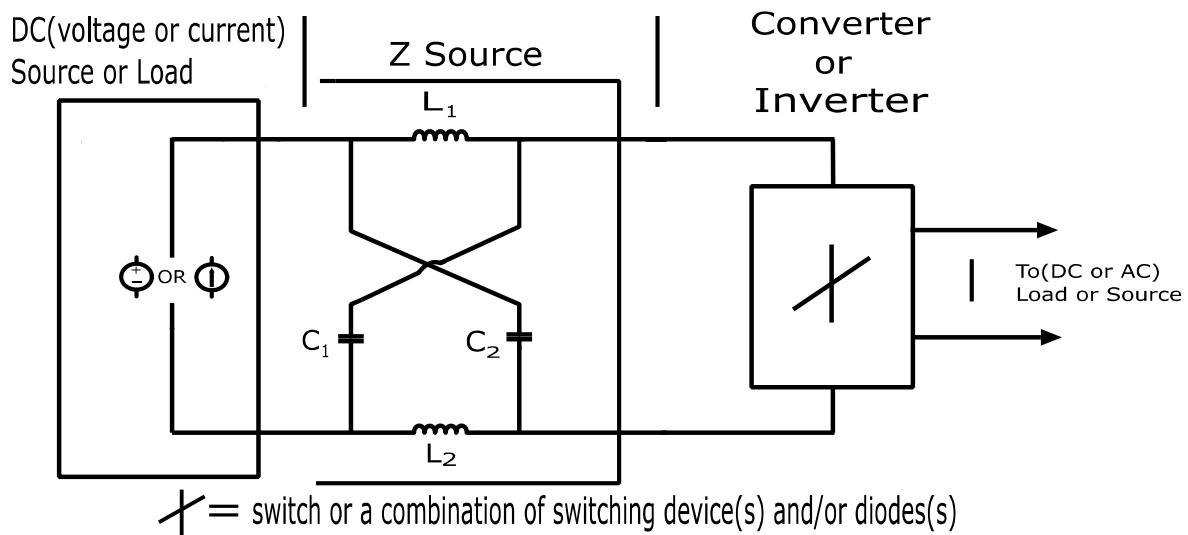


Figure 3. 1: General configuration of a Z Source Converter

Unlike a conventional VSI, the shoot-through state is not harmful and has been utilized in ZSI. The analysis shows how the shoot-through state over the non-shoot through state controls the buck-boost factor of the system. Through the boost factor in combination with modulation index M of VSI, the DC-AC buck-boost factor can be obtained. The Z-source inverter (ZSI) is shown in Fig 3.2.

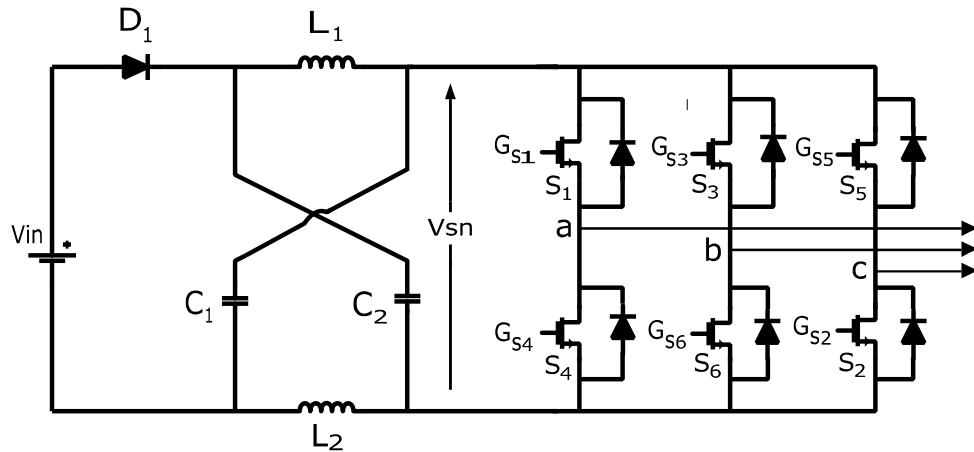


Figure 3. 2: Z-source converter structure using the anti-parallel combination of switching device and diode.

Advantages of Z-source Inverter:

- The step-up transformer is not needed to boost the voltage. By introducing shoot through operation mode in ZSI, the output voltage can be increased.
- The ZSI provides a cheaper, simpler, and single-stage power conversion by combining dc-dc booster and dc/ac inverter.
- The ac output voltage waveform distortion is reduced because the shoot-through is allowed and the dead time in the PWM signals is absent in ZSI.
- The Total Harmonic Distortion (THD) of the output voltage waveform is less.

The unique feature of the Z-source inverter is that the output ac voltage can be any value between zero and infinity regardless of the fuel-cell voltage. That is, the Z-source inverter is a buck-boost inverter that has a wide range of obtainable voltage. The traditional V- and I-source inverters cannot provide such a feature.

Classical ZSI consists of two capacitors and two inductors of symmetrical values. Switched boost inverter (SBI) is derived from inverse Watkins–Johnson topology [7] has similar characteristics as ZSI. The SBI has less number of components count over classical ZSI but has less voltage gain compared to ZSI. Both ZSI and SBI utilize shoot-through duty cycle in the inverter leg to improve reliability against EMI but both have discontinuous input current profile.

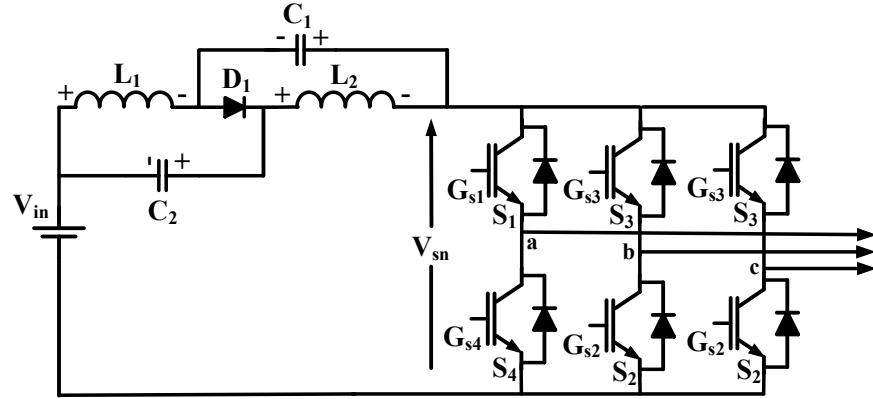


Figure 3. 3: Traditional quasi-ZSIs (qZSIs): discontinuous continuous input current qZSI

The disadvantages of discontinuous input current profile of ZSI are overcome by the continuous input current qZSI with same gain factor and have reduced capacitor voltage stress. The traditional discontinuous input current based qZSI is shown in Fig. 3.3. Different variants of quasi-Z- source inverter (qZSI) is presented in [8]. Continuous input current based qZSI are shown in Figs. 3.4. The difference between embedded qSBI and continuous input current type qZSI is that the embedded qSBI save one extra capacitor and inductor but at the cost of one additional active switch and one diode compared to qZSI. The current rating required for switches and diodes in qSBI is low and has higher efficiency as compared to qZSI [9].

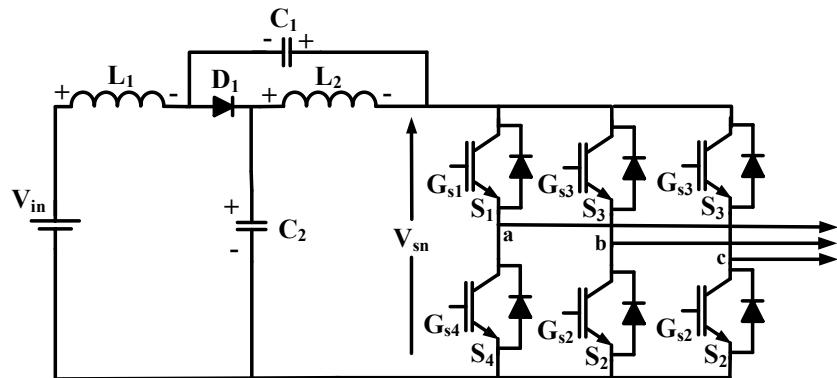


Figure 3. 4 Traditional quasi-ZSIs (qZSIs): continuous input current qZSI.

The ZSI, qZSI, and qSBI are having same boost factor and if D is shoot-through duty cycle, the boost factor of these inverters is $B = 1/(1 - 2D)$. Further, ac output voltage depends on modulation index (M), B and peak ac voltage $V_o = M \cdot B \cdot V_{in}$. It may be noted that ac output voltage is restricted by M and there is a constraint on D and M that $M + D \leq 1$ [10]. For high boost factor, inverter needs to be operated with higher values of duty cycle. However, higher values of D is restricted because of components voltage stresses and poor power quality of

output. Moreover, operating at higher values of duty cycle, the effect of parasitic components become more dominant which results into reduction in voltage gain significantly.

Improved voltage gain in inverters can be achieved by cascading of different topologies [11], switched-inductor topologies [12]-[15], switched-capacitor topologies [16] and coupled inductor topologies [17],[18]. For increasing output voltage using switched-inductor and switched-capacitors, number of passive components increases which eventually increases the converter weight, volume, and size. Further, the leakage inductance of the coupled inductors increases power losses and thus deteriorates the efficiency. [19]

The modified ZSI is shown in Fig 3.5. The advantage of this ZSI is that it has same passive components only addition is additional switch and diode as compared to conventional qZSI. However, still this ZSI has problem with floating ground. Moreover, to improve this ZSI we have done various modification on it and keeping all the parameters and states into consideration. The proposed family of ZSI has many advantages including common ground to the input without using any additional components

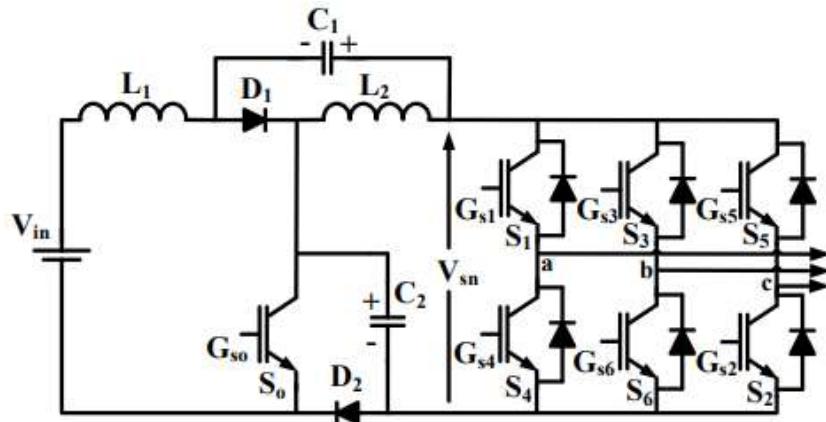


Figure 3.5: Conventional modified switched boost inverter

In this report proposed family of ZSIs are proposed. The proposed ZSIs are first analyzed with steady state analysis. Detailed comparative analysis among the ZSIs are discussed. The analysis is carried with the analysis, simulation, PCB design, Digital control, comparative analysis and verifications.

CHAPTER 4 - PROPOSED MODIFIED SWITCHED BOOST FAMILIES

The family of proposed Switched Boost inverter (SBI) has been modified into three different members. In each of the members, the positioning of the input voltage source has been shifter and then analyzed. All the procedures have been similar to that of the conventional switched boost inverter. The Fig. 4.1 shows the proposed modified switched boost inverter (MSBI) family. The proposed family of ZSIs are input voltage assisted modified switched boost inverter, switched inductor-switched capacitor SBI and common ground based modified SBI. Fig. 4.1 (a) shows the input voltage assisted modified switched boost inverter (VM-MSBI), Fig 4.1 (b) is shows the proposed switched inductor-switched capacitor SBI (SLC-MSBI) and Fig. 4.1(c) shows the proposed common ground based modified SBI (CG-MSBI).

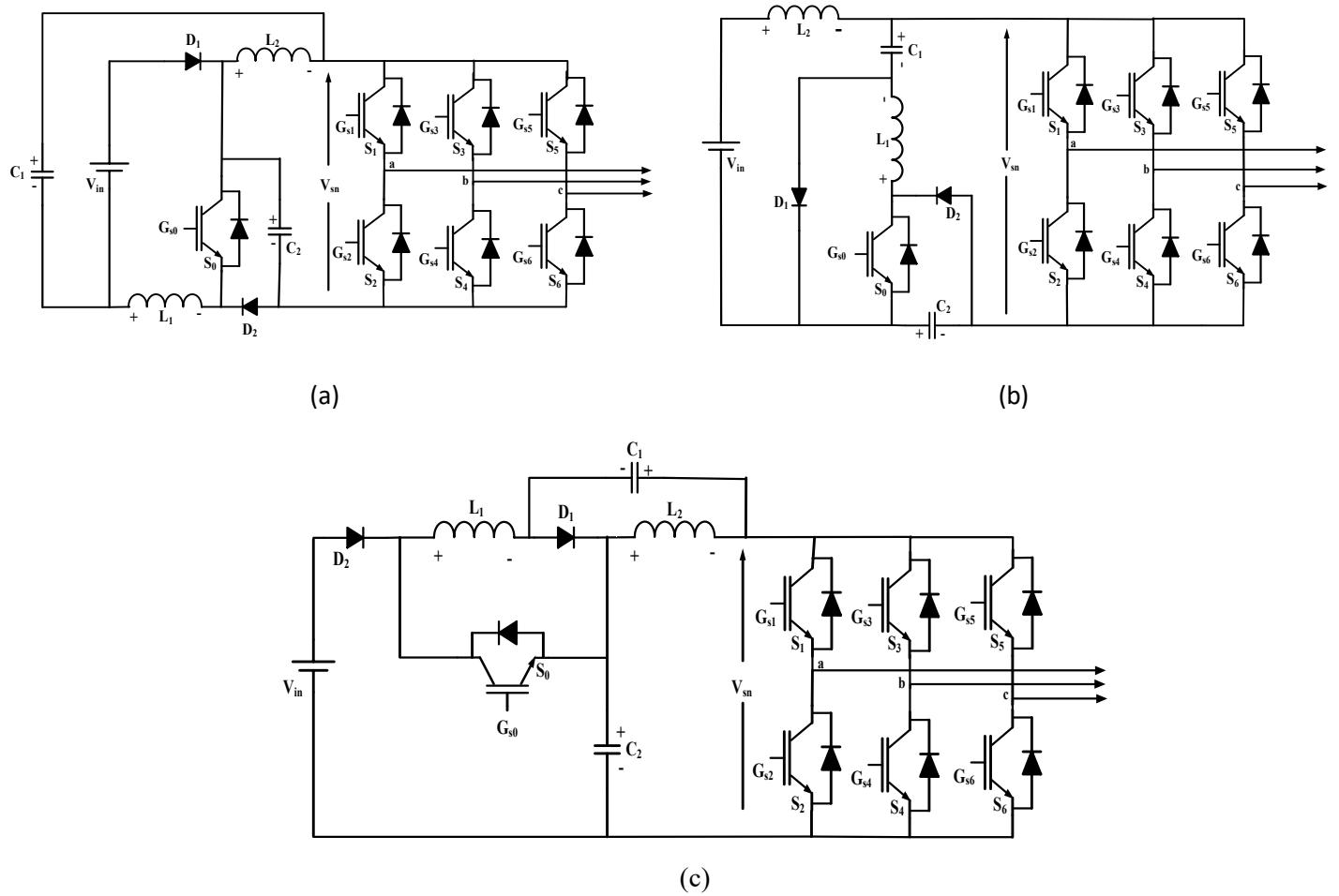


Figure 4.1: Proposed Family of SBI (a) VMSBI (b) SLC-MSBI (c) CG-MSBI

4.1 OPERATING PRINCIPLE OF THE PROPOSED VMSBI

The proposed VMSBI equivalent circuits for shoot-through and non-shoot-through states are shown below in the Fig. 4.2 and Fig. 4.3 respectively. The voltages across the inductors are V_{L1} , V_{L2} and the currents through inductors are I_{L1} and I_{L2} . The current through the capacitors are I_{C1} , I_{C2} and the voltage across the capacitors are V_{C1} and V_{C2} .

1) Shoot through interval

The diodes D₁ and D₂ are reverse biased and switch So conduct. In this interval, one of the inverter legs is also conducted. The input current is discontinuous as traditional ZSI. The voltage across the inductors and current through the capacitors in the shoot-through interval can be written as:

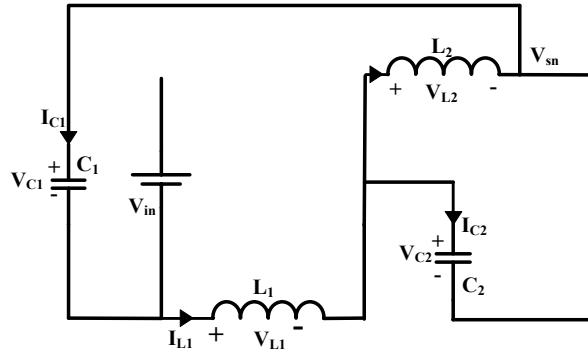


Figure 4. 2: Equivalent circuit in Shoot through interval

$$L_i \frac{di}{dt} = V_{C1} + V_{C2} \quad (1)$$

$$L_2 \frac{di_2}{dt} = V_{C2} \quad (2)$$

$$C_1 \frac{dv_1}{dt} = -I_{L1} \quad (3)$$

$$C_2 \frac{dv_2}{dt} = -I_{L1} - I_{L2} \quad (4)$$

2) Non shoot through interval

During the non-shoot-through behavior of proposed VMSBI switches, switch So is turned-OFF and inverter bridge is in power interval. In this case, both the diodes are in conduction mode. The voltage across the inductors and current through the capacitors in non-shoot-through interval are obtained as follows:

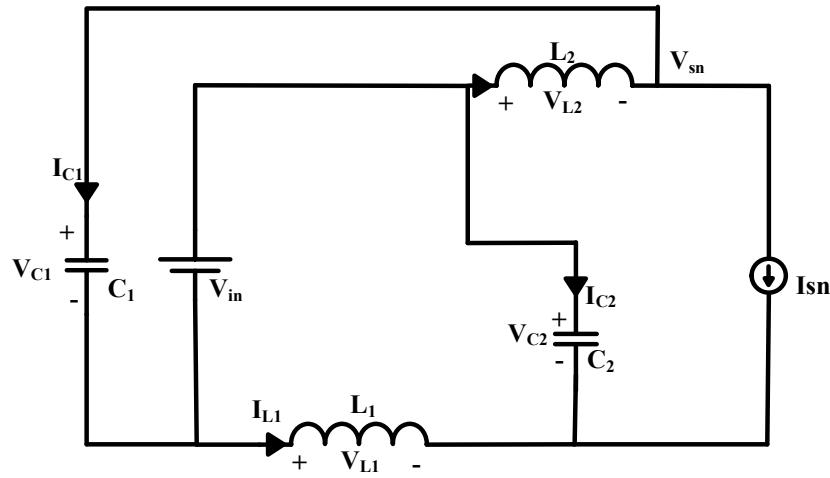


Figure 4.3: Equivalent Circuit in Non-shoot through interval

$$L_1 \frac{di}{dt} = V_{in} - V_{c2} \quad (5)$$

$$L_2 \frac{di_2}{dt} = V_{in} - V_{c2} \quad (6)$$

$$C_1 \frac{dv}{dt} = I_{L2} - I_{sn} \quad (7)$$

$$C_2 \frac{dv}{dt} = I_{L1} - I_{sn} \quad (8)$$

Applying volt-sec balance principle to L_1 and L_2 over one switching period.

$$V_{c1} = \frac{(1-D)^2}{(1-3D+D^2)} V_{in} \quad (9)$$

$$V_{c2} = \frac{(1-D)}{D^2-3D+1} V_{in} \quad (10)$$

By applying charge-seconds balance principle to C_1 and C_2 over one switching period.

$$I_{L1} = \frac{(1-D)}{D^2-3D+1} Isn \quad (11)$$

$$I_{L2} = \frac{(1-D)^2}{D^2-3D+1} Isn \quad (12)$$

The switched node voltage across the inverter bridge can be written as:

$$\begin{aligned} V_{sn} &= V_{C1} + V_{C2} - V_{in} \\ &= \frac{V_{in}}{D^2 - 3D + 1} \end{aligned} \quad (13)$$

The Boost Factor is given as:

$$B = \frac{1}{D^2 - 3D + 1} \quad (14)$$

4.2 OPERATING PRINCIPLE OF THE PROPOSED SLC-MSBI

The proposed SLC-MSBI equivalent circuits for shoot-through and non-shoot-through states are shown below in the Fig 4.4 and Fig 4.5 respectively. The voltages across the inductors are V_{L1} , V_{L2} and the currents through inductors are I_{L1} and I_{L2} . The current through the capacitors are I_{C1} , I_{C2} and the voltage across the capacitors are V_{C1} and V_{C2} .

1) Shoot through interval

The diodes D₁ and D₂ are reverse biased and switch So conduct. In this interval, one of the inverter legs is also conducted. The input current is discontinuous as traditional ZSI. The voltage across the inductors and current through the capacitors in the shoot-through interval can be written as:

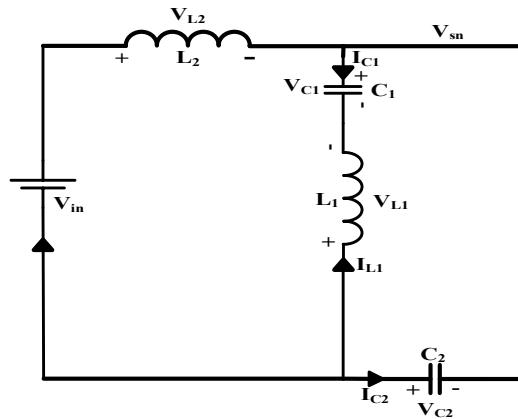


Figure 4. 4: Equivalent circuit in Shoot through interval

$$V_{L1} = V_{C1} + V_{C2} \quad (15)$$

$$V_{L2} = V_{in} + V_{C2} \quad (16)$$

$$I_{C1} = -I_{L1} \quad (17)$$

$$I_{C2} = -I_{L1} - I_{L2} \quad (18)$$

2) Non shoot through interval

During the non-shoot-through behavior of proposed SLC-MSBI switches, switch So is turned-OFF and inverter bridge is in power interval. In this case, both the diodes are in conduction mode. The voltage across the inductors and current through the capacitors in non-shoot-through interval are obtained as follows:

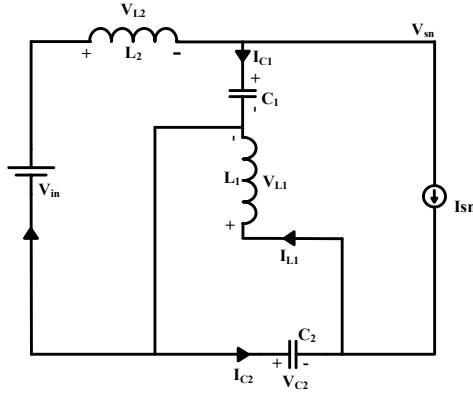


Figure 4.5: Equivalent Circuit in Non-shoot through interval

$$V_{L1} = V_{C2} \quad (19)$$

$$V_{L2} = V_{in} - V_{C1} \quad (20)$$

$$I_{C1} = I_{L2} - I_{sn} \quad (21)$$

$$I_{C2} = I_{L1} - I_{sn} \quad (22)$$

Applying volt-sec balance principle to L_1 and L_2 over one switching period.

$$V_{C1} = \frac{1 - 2D}{D^2 - 3D + 1} V_{in} \quad (23)$$

$$V_{C2} = \frac{1}{D^2 - 3D + 1} V_{in} \quad (24)$$

By applying charge-seconds balance principle to $C1$ and $C2$ over one switching period.

$$I_{L1} = \frac{2D^2 - 3D + 1}{D^2 - 3D + 1} I_{sn} \quad (25)$$

$$I_{L2} = \frac{(1 - D)^2}{D^2 - 3D + 1} I_{sn} \quad (26)$$

From Figs. and the switched node voltage across the inverter bridge can be written as

$$V_{sn} = V_{c1} + V_{c2} = \frac{(1 - D)}{D^2 - 3D + 1} V_{in} \quad (27)$$

The Boost Factor is given as:

$$B = \frac{V_{sn}}{V_{in}} = \frac{(1 - D)}{D^2 - 3D + 1} \quad (28)$$

4.3 OPERATING PRINCIPLE OF THE PROPOSED CG-MSBI

The proposed CG-MSBI equivalent circuits for shoot-through and non-shoot-through states are shown below in the Fig. 4.6 and Fig. 4.7 respectively. The voltages across the inductors are V_{L1} , V_{L2} and the currents through inductors are I_{L1} and I_{L2} . The current through the capacitors are I_{c1} , I_{c2} and the voltage across the capacitors are V_{c1} and V_{c2} .

1) Shoot-through interval:

In this mode of operation, the diodes D_1 and D_2 are reverse biased. The inductor currents I_{L1} and I_{L2} built-up-to maximum value through the capacitor C_1 and C_2 . The inductor voltages and capacitor currents are given as follows:

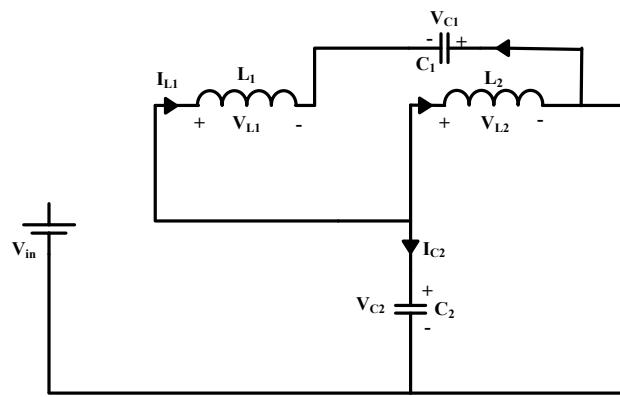


Figure 4.6: Equivalent circuit in Shoot through interval

$$L_1 \frac{di}{dt} = V_{c1} + V_{c2} \quad (29)$$

$$L_2 \frac{di}{dt} = V_{c2} \quad (30)$$

$$C_1 \frac{dv}{dt} = -I_{L1} \quad (31)$$

$$C_2 \frac{dv}{dt} = -I_{L1} - I_{L2} \quad (32)$$

2) Non-shoot through Interval

In this mode of operation, the switch S_0 is reverse biased, and the inverter bridge operates in power mode. The inductor voltages and capacitor currents in the non-shoot-through interval are given as follows:

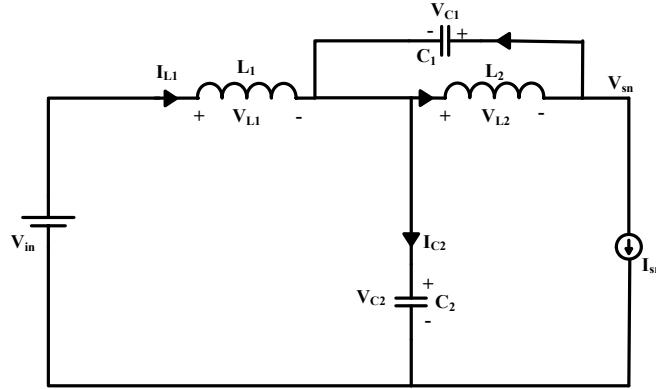


Figure 4.7: Equivalent circuit in Shoot through interval

$$L_1 \frac{di}{dt} = V_{in} - V_{C2} \quad (33)$$

$$L_2 \frac{di}{dt} = -V_{C1} \quad (34)$$

$$C_1 \frac{dv}{dt} = I_{L2} - I_{sn} \quad (35)$$

$$C_2 \frac{dv}{dt} = I_{L1} - I_{sn} \quad (36)$$

Applying the volt-second balance principle to L_1 and L_2 over one switching period,

$$V_{C1} = \frac{(1-D)D}{(1-2D)(1-D) - D^2} V_{in} \quad (37)$$

$$V_{C2} = \frac{(1-D)^2}{(1-2D)(1-D) - D^2} V_{in} \quad (38)$$

Applying the charge-seconds balance principle to C_1 and C_2 over one switching period, we get

$$I_{L1} = \frac{(1 - D)}{(1 - 3D + D^2)} I_{sn} \quad (39)$$

$$I_{L2} = \frac{(1 - D)^2}{(1 - 3D + D^2)} I_{sn} \quad (40)$$

The switched-mode voltage across the inverter bridge is given by:

$$V_{sn} = V_{C1} + V_{C2} = \frac{(1 - D)}{D^2 - 3D + 1} V_{in} \quad (41)$$

The Boost factor (B) is defined as:

$$B = \frac{V_{sn}}{V_{in}} = \frac{(1 - D)}{D^2 - 3D + 1} \quad (41)$$

4.4 PASSIVE COMPONENT DESIGN

In three-phase ZSI/qZSI, the capacitors and inductors are designed to limit the ripple voltage and switching frequency current ripple. Thus, for the proposed three-phase CC-qZSI, the inductors and capacitors are obtained as follows:

$$L_i = \frac{D_S V_{Li}}{\Delta i_{Li} \% I_{Li} f_s K_{sht}} \quad (42)$$

$$C_i = \frac{D_S I_{Ci}}{\Delta V_{Ci} \% V_{Ci} f_s K_{sht}} \quad (43)$$

Where $i = 1$ and 2 . V_{L1} and V_{L2} are the voltages across inductors L_1 and L_2 , I_{L1} and I_{L2} are the current flowing through L_1 and L_2 , Δi_{L1} and Δi_{L2} represent percentage ripple currents in L_1 and L_2 during shoot-through interval D_s . V_{C1} and V_{C2} are the voltages across the capacitors C_1 and C_2 , I_{c1} and I_{c2} are the currents flowing through C_1 and C_2 . ΔV_{C1} and ΔV_{C2} represent percentage ripple voltages in C_1 and C_2 during D_s . f_s is the switching frequency and K_{sht} is the coefficient factor, which is equal to the number of shoots through interval in one switching cycle.

CHAPTER 5 - PCB DESIGNING

5.1 INTRODUCTION

When it comes to printed circuit board (PCB) there are variety we can choose according to our requirement from single sided board to multi-layer or even flexible board each of these circuit boards has different kinds of layers that contribute to their functionality making them the right choice for different task with a multitude of options at our fingerprint. Fig. 5.1 shows the different layers of a PCB.

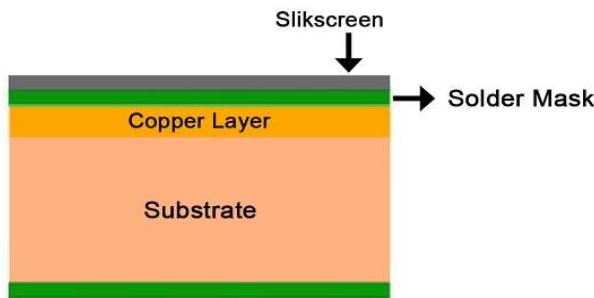


Figure 5. 1: Different Layers of a PCB

Substrate Layer

Substrate layer of any PCB is usually made from fiberglass which gives the board its rigid form generally speaking the majority of the board will have this material for their substrate with the exception of flexible PCB which are built on flexible plastic such as captain substrate PCB layer can also be made with other material such as epoxies however they lack the durability.

Copper layer

Next is a thin layer of copper foil, which is laminated to the board using heat when we are speaking of different layer PCB we are referring to numbers of copper layers. If we are creating a single, sided PCB the circuit board has one layer of conducting material on one side of the board and the other side is used for incorporating different electronic components.

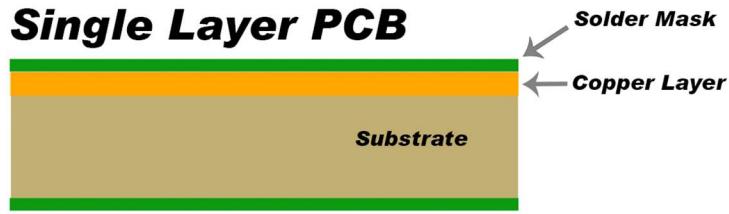


Figure 5. 2: Single layer PCB

where is double sided PCB can Mount the conductive copper and the component on both side of the board this double-sided board allow for closer routing dresses as they can alternate between the top and the bottom layer using vias.

Double Layer PCB



Figure 5. 3: Double Layer PCB

This can be very useful in many electronic products as the circuits on one side of the board can be connected to the other with the help of holes drilled into it.

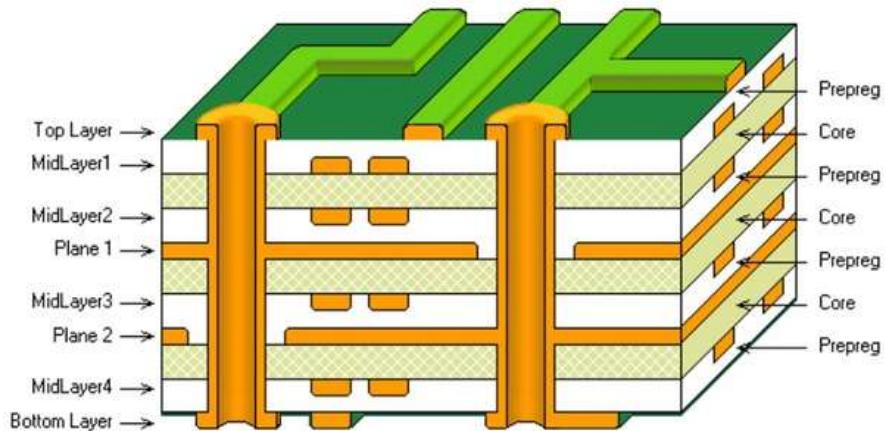


Figure 5. 4: Multi-layer PCB

The thickness of the copper layer on our PCB will depend on the power the PCB need to withstand PCB that need to handle very high power throughout may have thicker copper layer than those that do not.

Solder mask layer

Once the copper layer has been applied the solder mask layer is placed on top this gives the PCB its screen color and is used to insulate the copper layer to avoid any contact with any other metal or element of the board that could damage the copper traces. This layer is also important for the manufacturing process where the components are soldered onto the board as it helps the user to solder to the correct places.

Silkscreen layer

This silkscreen is mainly for the purpose of us humans to help us better understand the board and the functionality of different pins or leads by adding letter number and symbol to the board. The above layers are all present in different forms of PCBs and are crucial to the functionality of any board.

Depending on the complexity of the electronics device it is decided whether to use single layer PCB, double layer PCB or Multi-layer PCB. Most PCBs for easy electronics are simple and composed of only one layer.

Today PCBs are used in almost every electronics device irrespective of their size and shape, though PCBs are mostly associated with computers, but they can be found in many other electronics devices, like TVs, Radios, Digital cameras and Cell phones.

In addition to their use in consumer electronics and computers, differing types of PCBs are utilized in a spread of other fields, including:

- **Medical devices**: - Electronics products are now denser and consume less power than previous generations, making it possible to ascertain new and exciting medical technology. Most medical devices use a high-density PCB, which is employed to make the littlest and densest design possible. PCBs have found their way into everything from small devices, like pacemakers, to much larger devices like X-ray equipment or scan machines.
- **Industrial machinery**: - PCBs are commonly used in high-powered industrial machinery. Situations where thicker copper PCBs would be beneficial include motor controllers, high-current battery chargers and industrial load testers.
- **Lighting**: - As LED-based lighting solutions catch on in popularity due to their low power consumption and high levels of efficiency, so too does aluminum-backed PCB which is employed to form them.

- **Automotive and aerospace industries:** - Both the automotive and aerospace industries make use of flexible PCB, which is meant to face up to the high-vibration environments that are common in both fields. Depending on specifications and style, they will even be very lightweight, which may be a necessity when manufacturing parts for transportation industries.

There are several differing kinds of circuit boards, each with its own particular manufacturing specifications, material types, and usages:

Single-layer PCB

A single-layer or single-sided PCB is one that's made out of one layer of base material. One side of the bottom material is coated with a skinny layer of metal. Copper is that the commonest coating thanks to how well it functions as an electrical conductor. Once the copper base plating is applied, a protective solder mask is usually applied, followed by the last silk-screen to mark off all of the weather on the board.

Since single-layer/single-sided PCBs only have their various circuits and components soldered onto one side, they're easy to style and manufacture. This popularity means they will be purchased at a low-cost, especially for high-volume orders. The low-cost, high volume model means they're commonly used for a spread of applications, including calculators, cameras, radio, stereo equipment, solid state drives, printers and power supplies.

Double-layer PCB

Double-layer or double-sided PCBs have a base material with a thin layer of conductive metal, like copper, applied to every side of the board. Holes drilled through the board allow circuits on one side of the board to attach to circuits on the opposite.

The circuits and components of a double-layer PCB board are usually connected in one among two ways: either utilizing a through-hole or with the utilization of a surface-mount. A through-hole connection means small wires, referred to as leads, are fed through the holes, with each end of the leads then soldered to the proper component.

Surface mount PCBs don't utilize wires as connectors. Instead, many small leads are soldered on to the board, meaning that the board itself is employed as a wiring surface for the various components. This allows circuits to be completed using less space, freeing up space to permit the board to finish more functions, usually at higher speeds and a lighter weight than a through-hole board would allow.

Double-sided PCBs are typically utilized in applications which require an intermediate level of circuit complexity, like industrial controls, power supplies, instrumentation, HVAC systems, LED lighting, automotive dashboards, amplifiers and vending machines.

Multi-layer PCB

Multi-layer PCBs contains a series of three or more double-layered PCBs. These boards are then secured alongside a specialized glue and sandwiched between pieces of insulation to make sure that excess heat doesn't melt any of the components. Multi-layer PCBs are available a spread of sizes, going as small as four layers or as large as ten or twelve.

The largest multi-layer PCB ever built was 50 layers thick.

With many layers of computer circuit boards, designers can make very thick, complex designs which are suitable for a broad range of complicated electrical tasks. Applications where multi-layer PCBs would be beneficial include File servers, Data storage, GPS technology, Satellite systems, Weather analysis and medical equipment.

5.2 METHODS

To get started with our Project and Schematic

At first, we need to Download EAGLE for free from the official website of Eagle Autodesk. Every project is organized into a project folder, with schematics, PCB layouts, and other files all nestled together in one location. This makes it easy to keep things organized.

1. First of all, we need to open Autodesk EAGLE, and we will be greeted with the Control Panel. The panel will contain all of our libraries, projects, scripts, and many more.
2. From the Control Panel, we need to select File » New » Project and give our new project folder a name.
3. Next, we must right-click on our project folder and select New » Schematic to add a new schematic sheet to our project.
4. This will open a blank schematic document. Before we do anything else, save your schematic by selecting File » Save As and give it a name.

Now we have our project folder set up with our first schematic. If we go back to our Control Panel, we'll be able to see all of our project files organized together

To open a previous project, we must select open and select the particular project.

After we created a new project folder, we must start with schematic circuit diagram.

On the extreme left-hand side, we can see that we get many options such as the move, mirror, rotate copy, paste, delete, change, add-part, net etc.

Creating the Schematic diagram

Creating a Schematic Is a Multi-Step Process

The process that it takes to complete a schematic for a PCB. Selecting and placing your symbols is just one step.

To give an idea of what it takes to consider a schematic fully complete, here are all the steps:

- First, we need to find, place and orient all of your symbols on a blank schematic sheet
The very 1st steps are to identify all the components that are required in the circuit.
After we successfully identify all the components required, we must place them on the blank schematic workspace
Once all the component are placed on the sheet they must be placed accordingly as given in the circuit diagram for proper arrangement of the components.
- Next, we need to provide some electrical connectivity between each part with nets and assign values and names to our parts
After the component are placed properly and arranging the orientation of the symbols, we need to connect the connect the components with each other as given in the circuit diagram. To connect the components with each other we must select the net option which is given in the left-hand side of the screen.
To connect the components, we must select one terminal and connect it with the terminal of the other component as per the circuit diagram.
Likewise, we must complete the entire netting(wiring) of the entire circuit.
- And lastly, we need to make sure everything is connected as the circuit needs to be completed
We must check once whether all the terminals are connected properly with correct symbolic orientation.

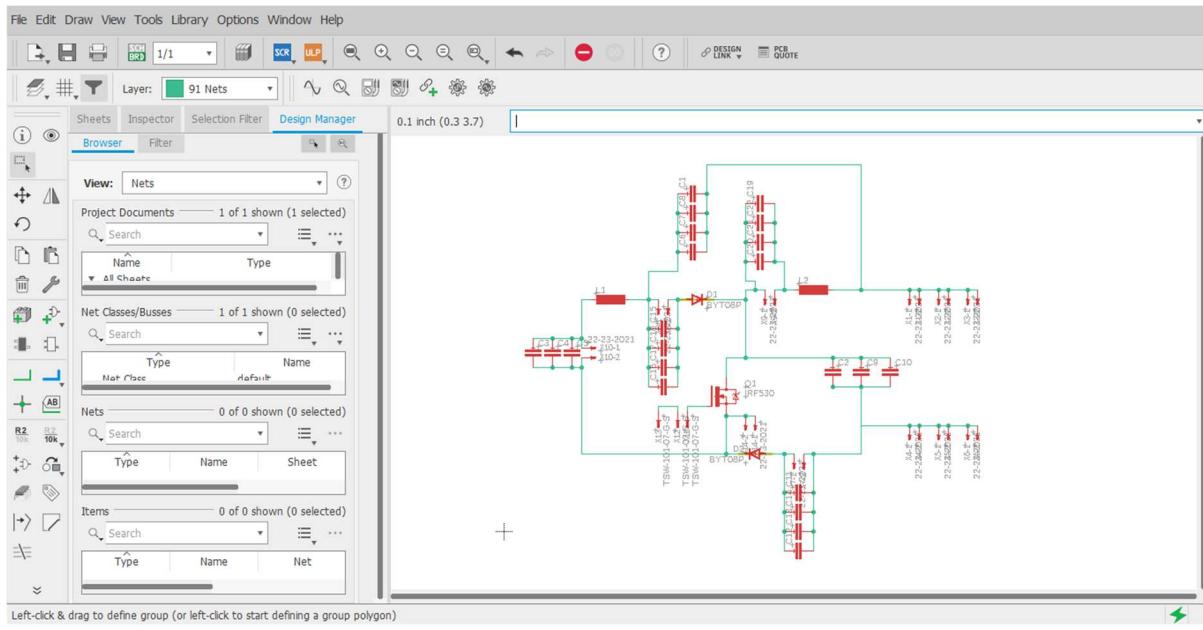


Figure 5. 5: Schematic Diagram of the circuit

After the schematic diagram is completed, we have converted the schematic diagram to board diagram in the eagle software. This can be done by selecting the (sch/brd) option present on the top of the interface. Fig. 5.5 shows the schematic diagram of the circuit.

On selecting the (sch/brd) option a new interface is opened. After converting the schematic diagram to board diagram, the components in the board diagram it looks like this.

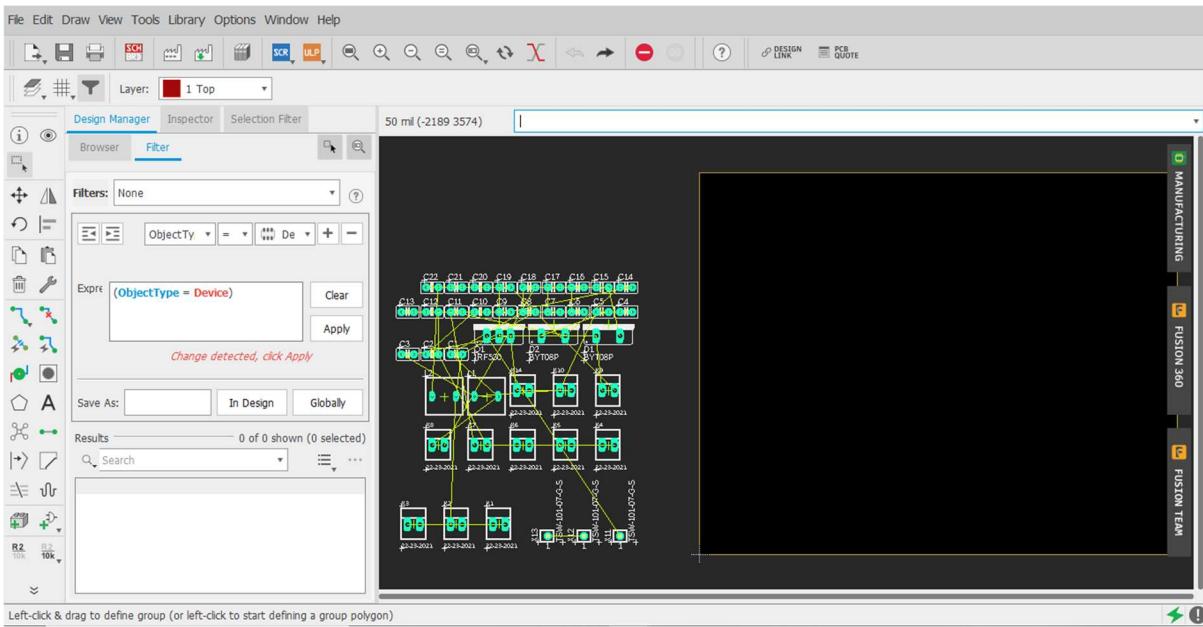


Figure 5. 6: Unarranged Components (outside the allowed area)

Now we need to re-arranged the components by moving all the components inside the area allowed

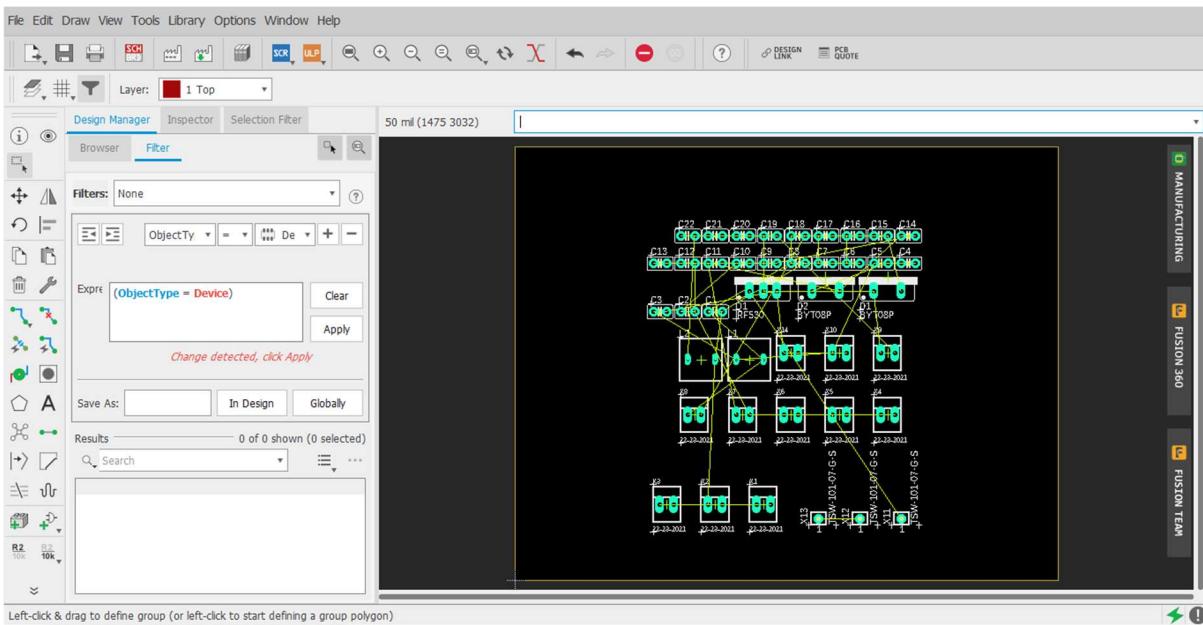


Figure 5. 7: Unarranged Components (inside the allowed area)

After moving the components, the arrangement is done in such a way so that the wires of the component do not cross the wire of another components, it is because we have to made a single layer PCB and the wires connecting two components cannot overlap or cross the wires of another component.

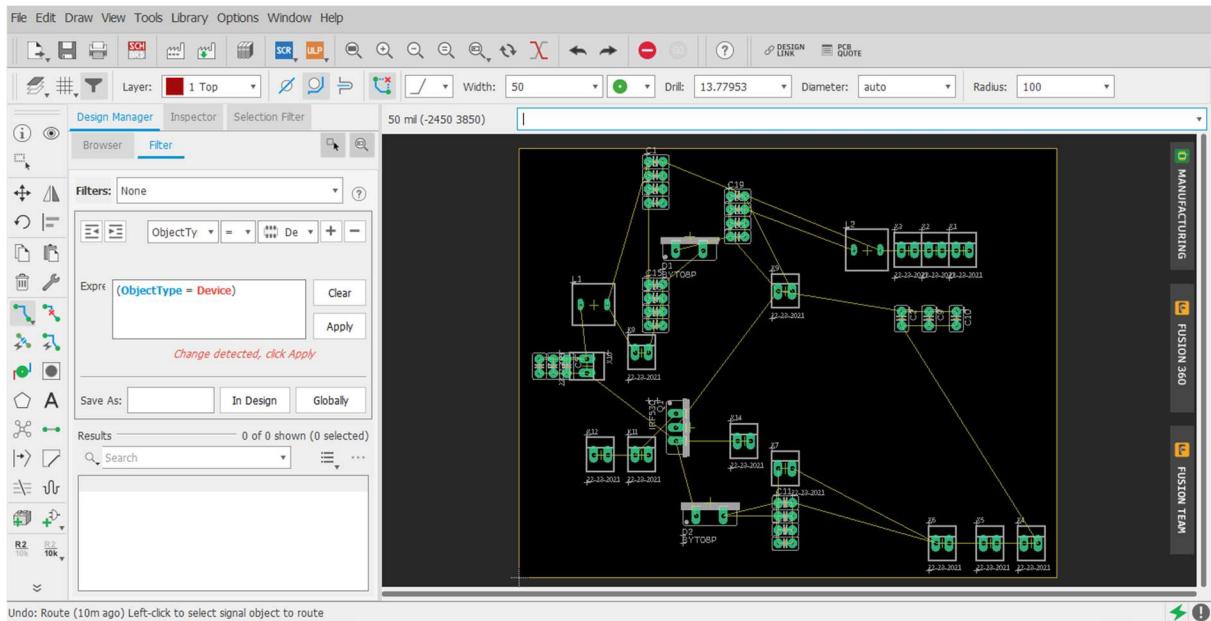


Figure 5. 8: Intermediate state of Board design

Then the board diagram circuit is designed in such way that maximum area can be covered for the conventional use of the PCB, as the PCB is designed in such a way so that it can be conventionally used for various purposes and the voltage source can be taken in various ways such for this reason the PCB is designed in a conventional way as so that it can be used by just opening and short-circuiting various end points.

If the arrangement is done in a proper way, then we can select the auto routing located on the left side of the interface. On selecting the auto routing the routing part are done automatically but for precision we must try to do it manually.

To route manually we must select the router located on the left side of the interface and route them accordingly.

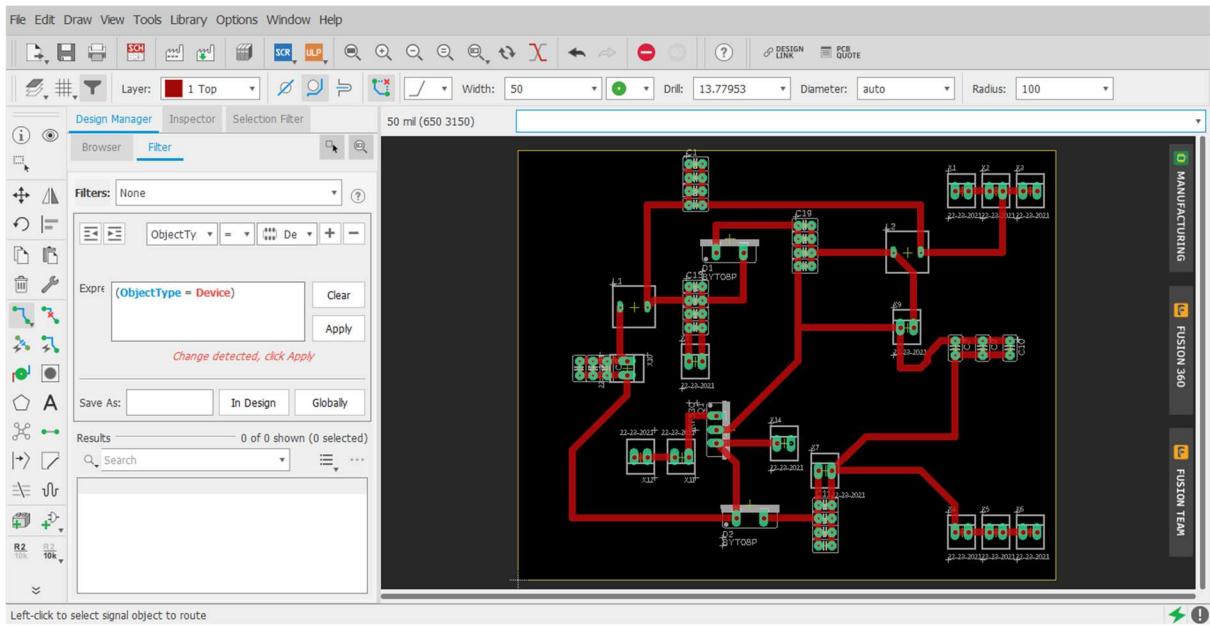


Figure 5.9: Routing of the Board wires

While designing the PCB we have kept in mind various factors that is the current flowing through the part, the circulation current, the thickness of the copper layer over the copper sheet, size of the copper sheet and various other factors.

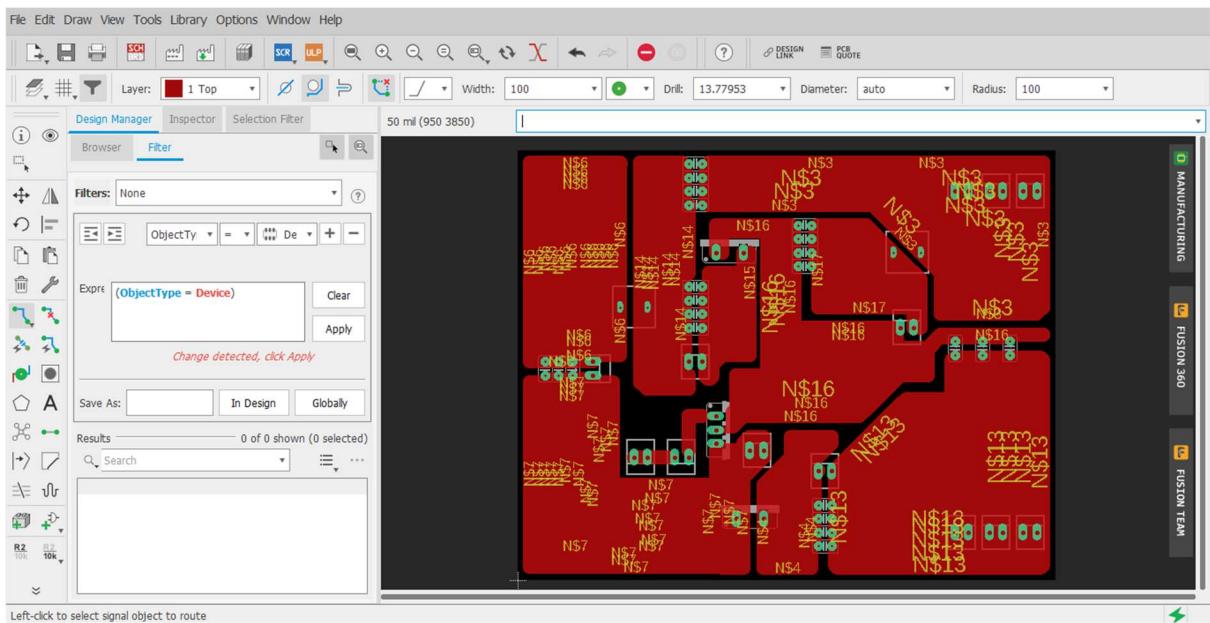


Figure 5. 10: Board Diagram of the PCB

Once we are done with the designing of the PCB in the eagle software then we have to print out the mirror image of the circuit in a photo paper. Here mirror image is taken because when we will paste the layout over copper sheet, we must get the correct orientation of the circuit.

We then carried out the further process by pasting the circuit diagram image over the copper layer sheet and by ironing it so that the laser printed circuit of the photo paper get pasted over the copper sheet so that we get the circuit's copy on the copper sheet.

Once the circuit is printed over the copper sheet by ironing it for continuous 1 hours, we have carried out the etching process.

The etching process is carried out but reacting the copper sheet with diluted HCL acid and hydrogen peroxide. This reaction is carried out for around 2 hours for the etching process.

5.3 DESIGN LAYOUT

Different PCB Gerber file are given for different stages from Fig. 5.11 to 5.18. Fig. 5.17 and 5.18 are the final products of the PCB. This PCB are used for the prototyping of the ZSIs. The components are placed and soldered accordingly.

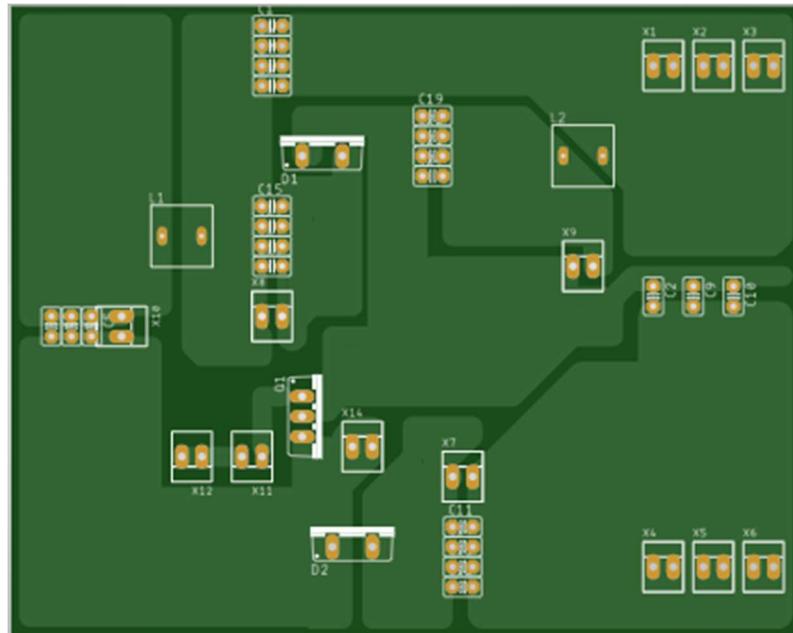


Figure 5. 11: Top view of PCB

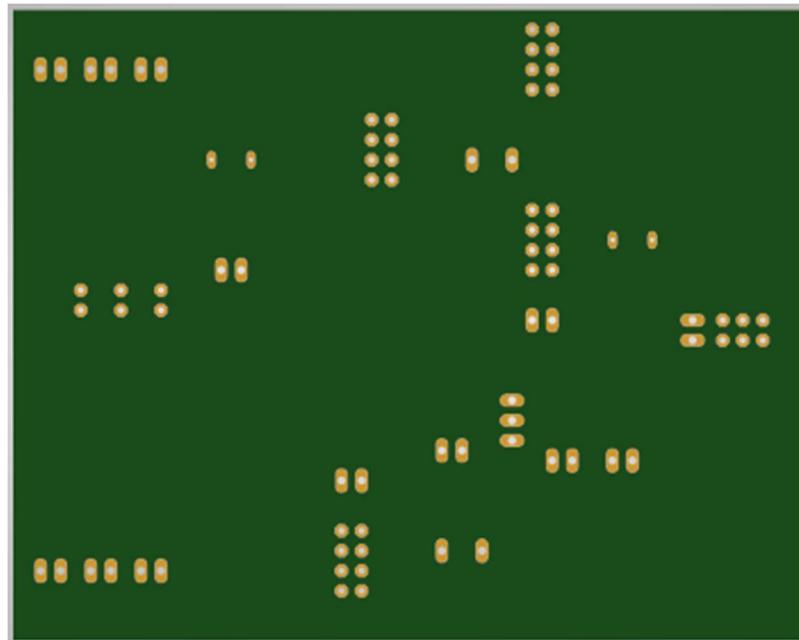


Figure 5. 12: Bottom layer of PCB

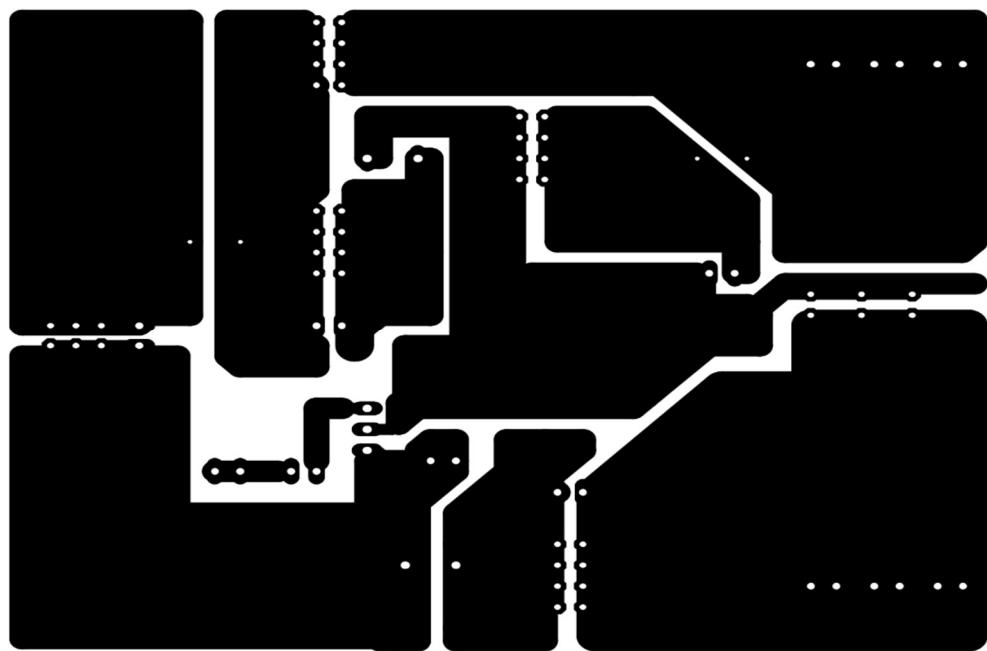


Figure 5. 13: Paper print of Booster part

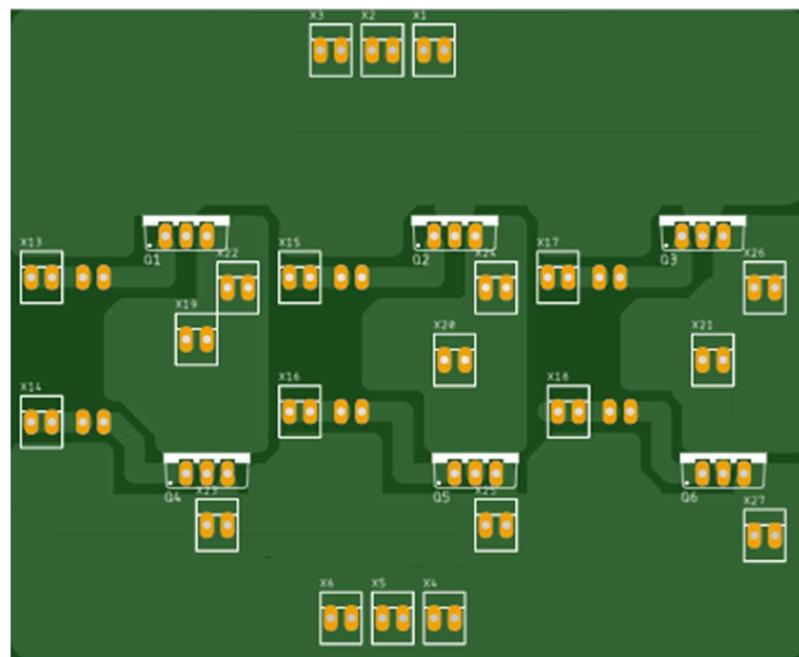


Figure 5. 14: Top View of the PCB

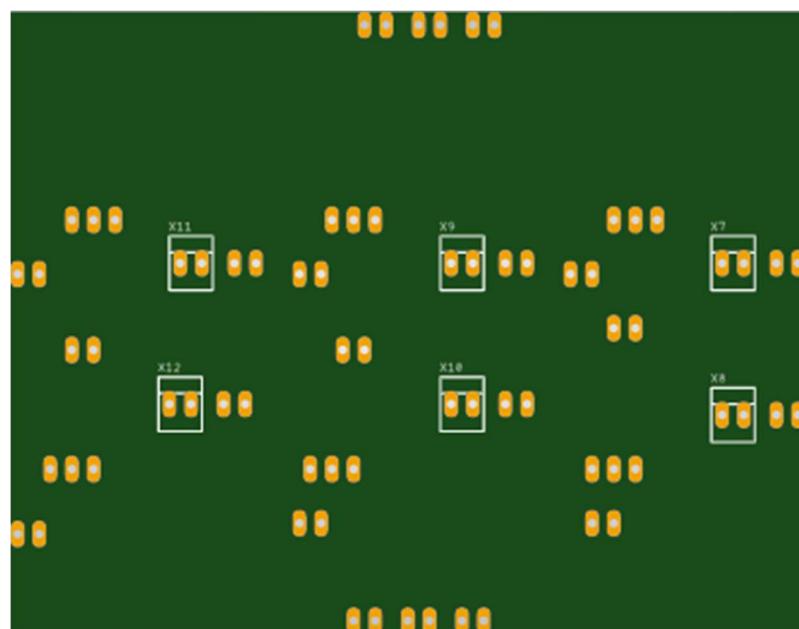


Figure 5.15: Bottom layer of PCB

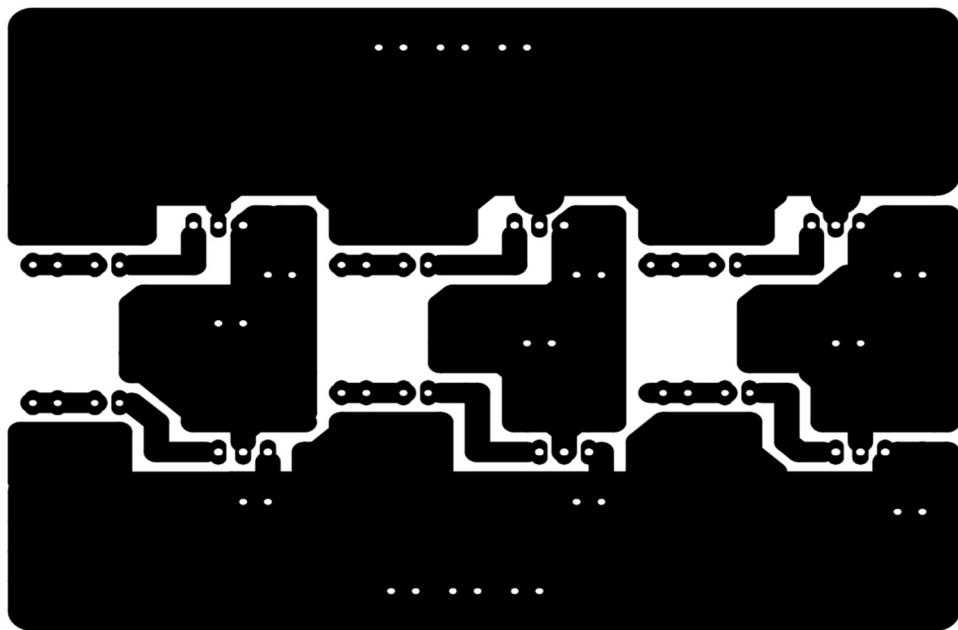


Figure 5. 16: Paper print of inverter part

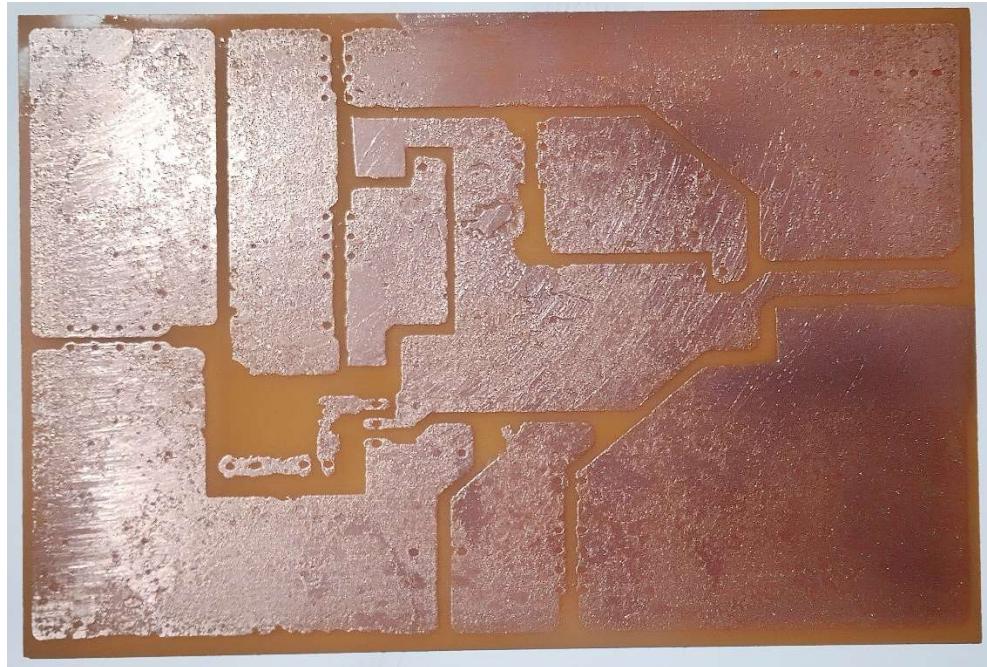


Figure 5. 17: PCB layout (Copper, solder-mask, silkscreen) layer (1)

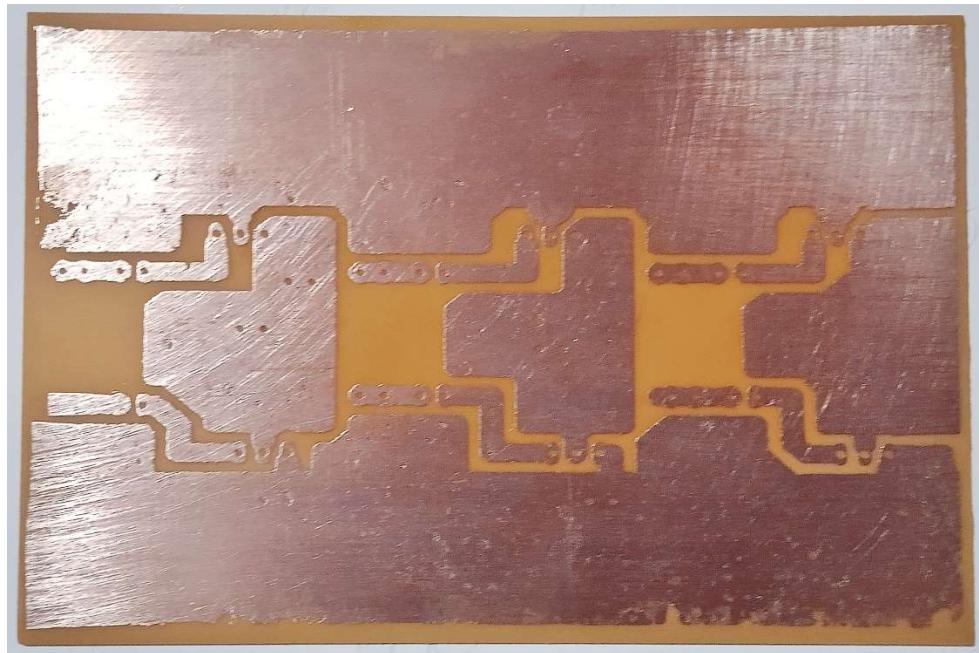


Figure 5. 18: PCB layout (Copper, solder-mask, silkscreen) layers (2)

Fig. 5.17 and 5.18 shows the PCB layouts for the circuit.

CHAPTER 6 - DIGITAL CONTROL USING DSP

6.1 ANALOG AND DIGITAL CONTROL

Analog control system deals, processes and outputs continuous values between a certain range (theoretically infinite, but practically all actuators are limited to a certain range) while digital makes use of an intermediary binary language for all sorts of computation before it is converted back to analog using digital to analog converters.

Since manipulating a continuous signal is much harder, and with advent of powerful computers in recent years, most of control system are digital just because they're just a whole lot easier to deal with in so many circumstances with the only real addition being ADC and DAC in the process pipeline between the input and output states.

The digital control systems have their own advantages over the analog control systems. They are as follows:

1. Digital signals are very resistant to noise since most communication in the pipeline is done in 1's and 0's. Noise interference with these signals hardly causes any distortion in the original signal. In addition, noise filters during the computation process can usually take care of any noise, if induced
2. Since analog signals needs to inevitably be quantized to digital signals (quantized, meaning the continuous signal needs to be discretized into small steps), the resolution of the signal is significantly reduced. However, an upside to this is that this reduces a great deal of load for computation and storage purposes. Moreover, these days, computers have become powerful enough to process a signal with extremely small discretization steps, thereby mostly overcoming the aforementioned resolution loss.
3. As a direct result to above point, power efficiency is also dramatically increased
4. Devices that usually process purely in analog tend to degrade or get damaged over time and needs to be constantly checked, or calibrated while in digital control systems, only the input sensor device and actuators usually have to be calibrated, making maintenance much easier

Table 6.1 show the differences between Analog and Digital Control Systems.

Table 6. 1: Comparison between Digital and Analog Control

Sl. No.	Digital Control	Analog Control
1	Digital control systems deal with binary or discrete signals having values 1 or 0.	They deal with continuous signals that can take a wide range of values.
2	Their input-output relationship (also called as transfer function) is represented by difference equation in z-domain.	The transfer function is given by differential equation in s-domain.
3	It uses Fourier Analysis, z-transform, DFT transform techniques.	It use Laplace Transform techniques.
4	Noise, interference and distortion is comparatively less in case of digital control systems.	Noise, interference and distortion is comparatively more.
5	Power efficiency is more.	Power efficiency is comparatively less (because of continuous signals).
6	Storage, analysis and processing of data is easy and convenient.	Storage, analysis and processing of data is a bit complicated.
7	They are widely used, as they are easy to handle and operate.	They are less used.

Actually, most of the control systems used now days are discrete versions of their analog counterparts. They are implemented in Centralized or Distributed manner.

6.2 WHAT WE HAVE USED?

For the project we have tried to do an experimental setup when the PWM signals are generated using the DSP kit TMS320F28335 from Texas Instruments. For interfacing the DSP board, we have generated the code using the Code Composer Studio v10.2.0 [20] and then the code has been dumped to the DSP board.

6.3 DIGITAL SIGNAL CONTROLLERS AND TMS320F28335

The TMS320F28335 belongs to a group of devices that are called Digital Signal Controllers (DSC). In computing, we use words like “Microprocessor”, “Microcomputer” or “Microcontroller” to specify a given sort of electronic device. When it comes to digital signal processing, the preferred name is “Digital Signal Processor” (DSP).

To begin with, let us introduce some terms:

- Microprocessor (μ P)
- Micro Computer
- Microcontroller (μ C)
- Digital Signal Processor (DSP)
- Digital Signal Controller (DSC)

Microprocessors are based on a simple sequential procedural approach: 1) read next machine code instruction from code memory, 2) decode instruction, 3) read optional operands from data memory, 4) execute instruction, and 5) write back result. This series of events runs in an endless manner. To use a μ P one has to add memory and additional external devices to the Microprocessor. The microprocessor consists of two parts “the control unit” and “the central processing unit” (CPU). It operates on input signals, reads operands from data memory, writes results back in data memory, and updates output modules. All computing is based on machine code instructions, which are sequentially stored in code memory. The microprocessor reads these instructions one after another into its control logic.

A Digital Signal Processor is a specific device that is designed around the typical mathematical operations to manipulate digital data that are measured by signal sensors. The objective is to process the data as quickly as possible to be able to generate an output stream of ‘new’ data in real time.

Finally, a Digital Signal Controller (DSC) is a new type of microcontroller, where the processing power is delivered by a DSP - a single chip device combining both the computing power of a Digital Signal Processor and the embedded peripherals of a single chip computing system. For advanced real time control systems with a high amount of mathematical calculations, a DSC is the best choice. Today there are only a few manufacturers offering DSC's. Due to the advantages of DSC's for many projects, a number of silicon manufacturers are developing this type of controller.

TMS320F28335 belongs to a group of devices that are called “Digital Signal Controllers” (DSC). When it comes to Digital Signal Processing, it is called “Digital Signal Processor” (DSP). TMS320F28335 is a 32-bit floating point Digital Signal Controller.

The DSP / DSC - portfolio of Texas instruments is split into three major device families, called Micro-controllers, ARM-based, and DSP.

The C64x branch is the most powerful series of DSP in computing power. There are floating - point as well as fixed - point devices in this family. The application fields are image processing, audio, multimedia server, base stations for wireless communication etc.

The C55x family is focused on mobile systems with very efficient power consumption per MIPS. Its main application area is in cell phone technology.

The C2000 - group is dedicated to Digital Signal Control (DSC), is a very powerful solution for real time control applications. This group is accompanied at the two ends by a 16-bit Microcontroller group (MSP430), and a 32 – bit series of ARM-core based microcontrollers (Cortex M3, Cortex A-8 or ARM9).

Table 6.2 summarizes the main application areas for the 3 Texas Instruments families of DSP:

Table 6. 2: Different families of microcontroller

C2000	C5000	C6000
Lowest Cost	Efficiency	Performance and Ease of use
<ul style="list-style-type: none"> ▪ Motor Control ▪ Storage ▪ Digital Control Systems ▪ Power Supply Control 	<ul style="list-style-type: none"> ▪ Wireless Phones ▪ Internet audio player ▪ Digital Still Cameras. ▪ Modems ▪ Telephony ▪ VoIP 	<ul style="list-style-type: none"> ▪ Communication infrastructure ▪ Wireless Base-Stations ▪ DSL ▪ Imaging ▪ Multi Media servers ▪ Video

C2000™ 32-bit microcontrollers are optimized for processing, sensing, and actuation to improve closed-loop performance in real-time control applications such as industrial motor drives; solar inverters and digital power; electrical vehicles and transportation; motor control; and sensing and signal processing. The C2000 line includes the Delfino™ Premium Performance family and the Piccolo™ Entry Performance family.

TMS320C2000™ 32-bit microcontrollers are optimized for processing, sensing, and actuation to improve closedloop performance in real-time control applications. The C2000™ microcontroller's line includes the Delfino™ Premium Performance microcontroller family and the Piccolo™ Entry Performance microcontroller family.

The TMS320F28335, TMS320F28334, TMS320F28333, TMS320F28332, TMS320F28235, TMS320F28234, and TMS320F28232 devices, members of the TMS320C28x/ Delfino™ DSC/MCU generation, are highly integrated, high-performance solutions for demanding control applications. [21]-[23].

Original Delfino™ series:

TMS320F2833x Delfino™ Microcontrollers

The F2833x series is the original Delfino MCU. It is the first C2000™ MCU that is offered with a floating-point unit (FPU). It has the first-generation ePWM timers that are used throughout the rest of the Delfino and Piccolo™ families. The 12.5-MSPS, 12-bit ADC is still class leading for an integrated analog-to-digital converter. The F2833x has a 150-MHz CPU and up to 512KB of on-chip flash. It is available in a 176-pin QFP or 179-ball BGA package.

TMS320C2834x Delfino™ Microcontrollers

The C2834x series removes the on-chip Flash memory and integrated ADC to enable the fastest available clock speeds of up to 300 MHz. It is available in a 179-ball BGA or 256-ball BGA package.

Newest Delfino™ series:

TMS320F2837xD Delfino™ Microcontrollers

The F2837xD series sets a new standard for performance with dual subsystems. Each subsystem consists of a C28x CPU and a parallel control law accelerator (CLA), each running at 200 MHz. Enhancing performance are TMU and VCU accelerators. New capabilities include multiple 16-bit/12-bit mode ADCs, DAC, Sigma-Delta filters, USB, configurable logic block (CLB), on-chip oscillators, and enhanced versions of all peripherals. The F2837xD is available with up to 1MB of Flash. It is available in a 176-pin QFP or 337-pin BGA package.

TMS320F2837xS Delfino™ Microcontrollers

The F2837xS series is a pin-to-pin compatible version of F2837xD but with only one C28x-CPU-and-CLA subsystem enabled. It is also available in a 100-pin QFP to enable compatibility with the Piccolo™ TMS320F2807x series.

For our project, we have used the Texas Instrument TMS320F28335 Delfino Micro controller. The equipment comes with a TMS320F28335 Control Card and a TMS320F28335 Docking station and a USB Cable A Male to B Male. Together all of them are called TMS320F28335 Experimenter Kit. [24]

Specifications of TMS320F28335:

- Manufactured by Texas Instruments.
- Static Cosmos technology.
- DSP core voltage 1.8v-1.9v with 3.3v i/p-o/p.
- 32 bit floating DSP
- Harvard bus architecture.
- Six channel DMA controller.
- 96 interrupt sources.
- GPIO – 88
- 16 ADC channel each 12 bit.
- Timer Units and Watch Dog module.
- DAC (4 parallel DAC, 8 bit and 12 bit).
- (ADC, MsBSP, ePWM, XINTF and SARAM)
- 16 or 32 bit XINTF.
- On – chip memory 256K x 16 flash memory 34K x 16 SARAM.

Fig. 6.1, 6.2, 6.3, 6.4 shows the control card, the docking station (top view), docking station (angled view), the experimenter kits respectively.



Figure 6. 1: TMS320F28335 Control Card

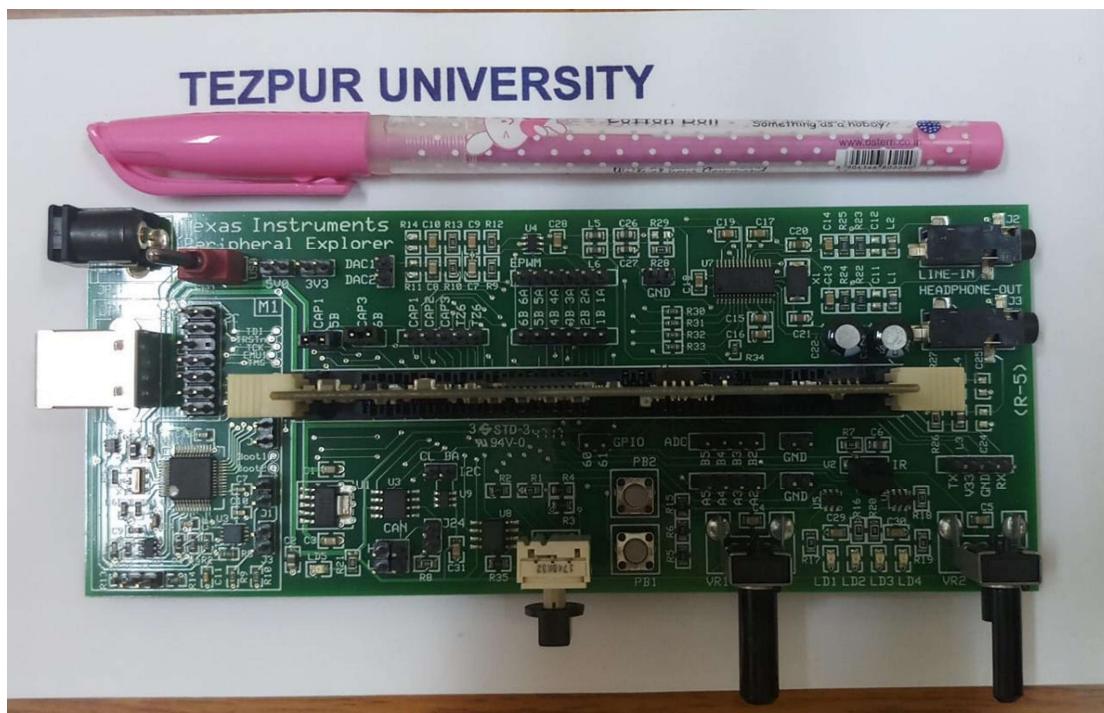


Figure 6. 2: TMS320F28335 Docking Station (top view)



Figure 6. 3: TMS320F28335 Docking Station (Angled view)



Figure 6. 4: TMS320F28335 Experimenter kit

6.4 Enhanced Pulse Width Modulation (ePWM)

Today's electronic systems are described using terms such as "direct digital control", "digital power supply", "digital power converters" and so on. A core feature of all these applications is the ability to generate different series of digital pulse patterns to control power electronic switches based on the results of sophisticated numerical calculations. The F283xx family provides such hardware units; several pulse width modulation (PWM) output signals, along with time measurements units ("Capture Units").

The enhanced pulse width modulator (ePWM) peripheral is a key element in controlling many of the power electronic systems found in both commercial and industrial equipment. These systems include digital motor control, switch mode power supply control, uninterruptible power supplies (UPS), and other forms of power conversion. The ePWM peripheral performs a digital to analog (DAC) function, where the duty cycle is equivalent to a DAC analog value; it is sometimes referred to as a Power DAC.

An effective PWM peripheral must be able to generate complex pulse width waveforms with minimal CPU overhead or intervention. It needs to be highly programmable and very flexible while being easy to understand and use. The ePWM described here addresses these requirements by allocating all needed timing and control resources on a per PWM channel basis. Cross coupling or sharing of resources has been avoided; instead, the ePWM is built up from smaller single channel modules with separate resources that can operate together as required to form a system. This modular approach results in an orthogonal architecture and provides a more transparent view of the peripheral structure, helping users to understand its operation quickly. [27]

In this document the letter x within a signal or module name is used to indicate a generic ePWM instance on a device. For example output signals EPWMxA and EPWMxB refer to the output signals from the ePWMx instance. Thus, EPWM1A and EPWM1B belong to ePWM1 and likewise EPWM4A and EPWM4B belong to ePWM4.

6.4.1 ePWM Phase Synchronization

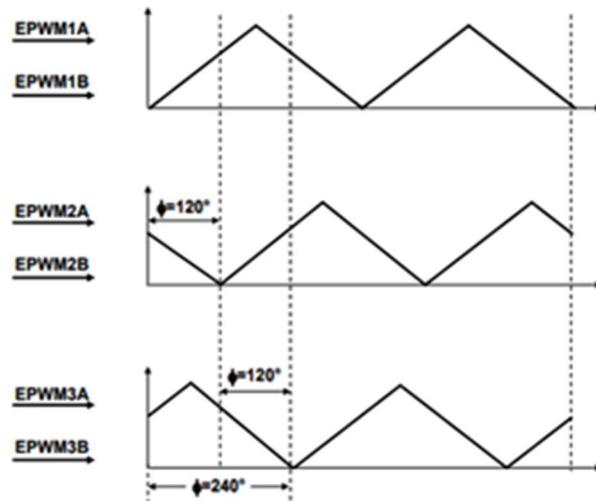


Figure 6.5: ePWM Phase Synchronization [28]

Two hardware signals "SYNCI" (synch in) and "SYNCO" (synch out) can be used to synchronize ePWM units to each other. For example, we could define one ePWM unit as a "master" to generate an output signal "SYNCO" each time the counter equals period. Two more ePWM units could be initialized to recognize this signal as "SYNCI" and start immediately counting, each time they receive this signal. In such way, we have established a synchronous set of 3 ePWM channels. By using another register called "TBPHS" we can introduce a phase shift between master, slave 1 and slave 2, an absolute necessity for three-phase control systems.

The figure shows such an example, where register TBCNT of ePWM2 and ePWM3 are preloaded with a start value that corresponds to 120° and 240° respectively. In this example ePWM1 has been initialized as master to generate SYNCO each time the counter register equals zero. With the enabled phase input feature for ePWM2 and ePWM3 the two channels operate as slave 1 and slave 2 and will load their counter registers TBCNT with numbers stored in the corresponding phase registers TBPHS.

Example:

- ePWM1 counts from 0 to 6000. TBPRD = 6000
- ePWM2 register TBPHS = 2000
- ePWM3 register TBPHS = 4000.

6.4.2 Submodule Overview

The ePWM module represents one complete PWM channel composed of two PWM outputs: EPWMxA and EPWMxB. Multiple ePWM modules are instanced within a device as shown in Figure 3-1. Each ePWM instance is identical with one exception. Some instances include a hardware extension that allows more precise control of the PWM outputs. This extension is the high-resolution pulse width modulator (HRPWM) and is described in the High-Resolution Pulse Width Modulator (HRPWM) chapter. See the datasheet to determine which ePWM instances include this feature. Each ePWM module is indicated by a numerical value starting with 1. For example ePWM1 is the first instance and ePWM3 is the 3rd instance in the system and ePWMx indicates any instance.

The ePWM modules are chained together via a clock synchronization scheme that allows them to operate as a single system when required. Additionally, this synchronization scheme can be extended to the capture peripheral modules (eCAP). The number of modules is device-dependent and based on target application needs. Modules can also operate stand-alone.

Each ePWM module supports the following features:

- Dedicated 16-bit time-base counter with period and frequency control
- Two PWM outputs (EPWMxA and EPWMxB) that can be used in the following configurations:
 - Two independent PWM outputs with single-edge operation
 - Two independent PWM outputs with dual-edge symmetric operation
 - One independent PWM output with dual-edge asymmetric operation
 - Asynchronous override control of PWM signals through software.
- Programmable phase-control support for lag or lead operation relative to other ePWM modules.
- Hardware-locked (synchronized) phase relationship on a cycle-by-cycle basis.
- Dead-band generation with independent rising and falling edge delay control.
- Programmable trip zone allocation of both cycle-by-cycle trip and one-time trip on fault conditions.
- A trip condition can force either high, low, or high-impedance state logic levels at PWM outputs.
- All events can trigger both CPU interrupts and ADC start of conversion (SOC)
- Programmable event prescaling minimizes CPU overhead on interrupts.
- PWM chopping by high-frequency carrier signal, useful for pulse transformer gate drives.

6.4.3 Calculating PWM Period and Frequency

The frequency of PWM events is controlled by the time-base period (TBPRD) register and the mode of the time-base counter. The figure shows the period (T_{pwm}) and frequency (F_{pwm}) relationships for the up-count, down-count, and up-down-count time-base counter modes when the period is set to 4 (TBPRD = 4). The time-base clock (TBCLK) which is a prescaled version of the system clock (SYSCLKOUT) defines the time increment for each step.

The time-base counter has three modes of operation selected by the time-base control register (TBCTL):

- **Up-Down-Count Mode:**

In up-down-count mode, the time-base counter starts from zero and increments until the period (TBPRD) value is reached. When the period value is reached, the time-base counter then decrements until it reaches zero. At this point, the counter repeats the pattern and begins to increment.

- **Up-Count Mode:**

In this mode, the time-base counter starts from zero and increments until it reaches the value in the period register (TBPRD). When the period value is reached, the time-base counter resets to zero and begins to increment once again.

- **Down-Count Mode:**

In down-count mode, the time-base counter starts from the period (TBPRD) value and decrements until it reaches zero. When it reaches zero, the time-base counter is reset to the period value and it begins to decrement once again

Which of the three modes is used is mostly determined by the application. The second two operating modes are called "Asymmetrical" because in of the shape of the counting pattern from 0 to TBPRD (count up) or from TBPRD to 0 (count down). Also, in a three phase system, one could define three different timing events between 0 and TBPRD to switch a phase output signal to "ON" and to use the match between TBCNT and TBPRD to switch "OFF" all three phases simultaneously, thus generating an asymmetrical shape of the switch signals. In "Symmetrical" waveform mode, the register TBCNT starts from zero to count up until it equals TBPRD. Then TBCNT turns direction to count down back to zero to finish a counting period.

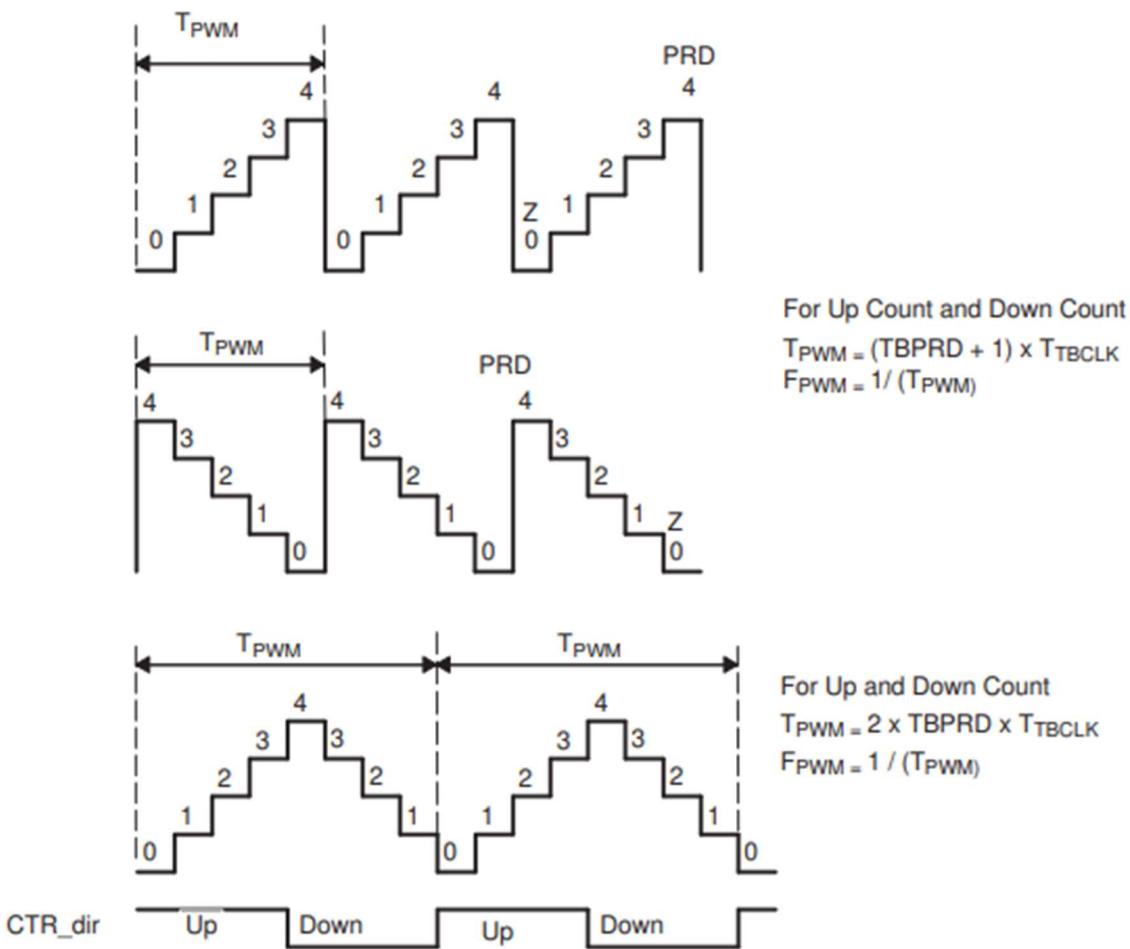


Figure 6.6: Time Base Frequency and Period [28]

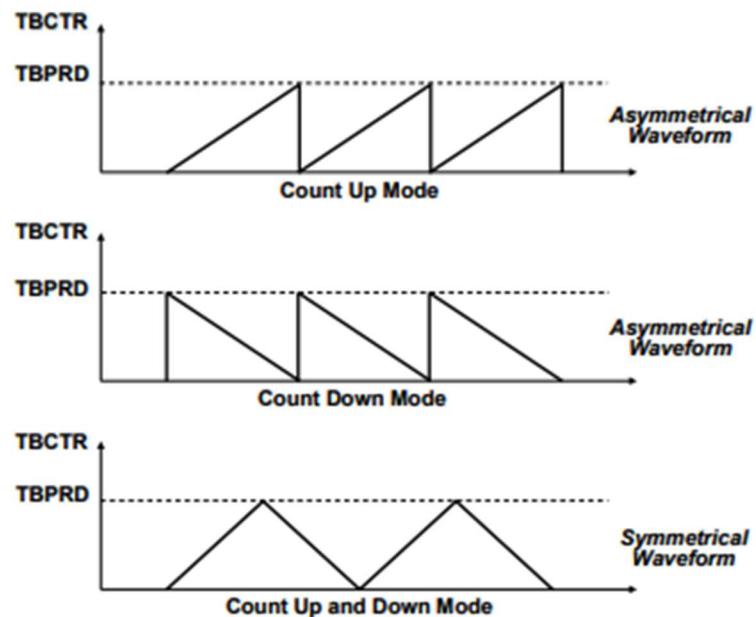


Figure 6.7: ePWM Time Base Count Modes [28]

6.4.4 Waveforms for Common Configurations

The waveforms in the figure shows the ePWMs behavior for a static compare register value. In a running system, the active compare registers (CMPA and CMPB) are typically updated from their respective shadow registers once every period. The user specifies when the update will take place; either when the time-base counter reaches zero or when the time-base counter reaches period. There are some cases when the action based on the new value can be delayed by one period or the action based on the old value can take effect for an extra period. Some PWM configurations avoid this situation. These include, but are not limited to, the following:

Use up-down-count mode to generate a symmetric PWM:

- If you load CMPA/CMPB on zero, then use CMPA/CMPB values greater than or equal to 1.
- If you load CMPA/CMPB on period, then use CMPA/CMPB values less than or equal to TBPRD-1. This means there will always be a pulse of at least one TBCLK cycle in a PWM period which, when very short, tend to be ignored by the system.

Use up-down-count mode to generate an asymmetric PWM:

- To achieve 50%-0% asymmetric PWM use the following configuration: Load CMPA/CMPB on period and use the period action to clear the PWM and a compare-up action to set the PWM. Modulate the compare value from 0 to TBPRD to achieve 50%-0% PWM duty.

When using up-count mode to generate an asymmetric PWM:

- To achieve 0-100% asymmetric PWM use the following configuration: Load CMPA/CMPB on TBPRD.

Use the Zero action to set the PWM and a compare-up action to clear the PWM. Modulate the compare value from 0 to TBPRD+1 to achieve 0-100% PWM duty.

The figure below shows how a symmetric PWM waveform can be generated using the up-down-count mode of the TBCTR. In this mode, 0%-100% DC modulation is achieved by using equal compare matches on the up count and down count portions of the waveform. In the example shown, CMPA is used to make the comparison. When the counter is incrementing, the CMPA match will pull the PWM output high. Likewise, when the counter is decrementing the compare match will pull the PWM signal low. When CMPA = 0, the PWM signal is low for the entire period giving the 0% duty waveform. When CMPA = TBPRD, the PWM signal is high achieving 100% duty. When using this configuration in practice, if you load CMPA/CMPB on zero, then use CMPA/CMPB values greater than or equal to 1. If you load CMPA/CMPB on period, then use CMPA/CMPB values less than or equal to TBPRD-1. This means there will always be a pulse of at least one TBCLK cycle in a PWM period, which,

when very short, tend to be ignored by the system. Fig. 6.8 shows the up-down counter mode symmetrical waveforms.

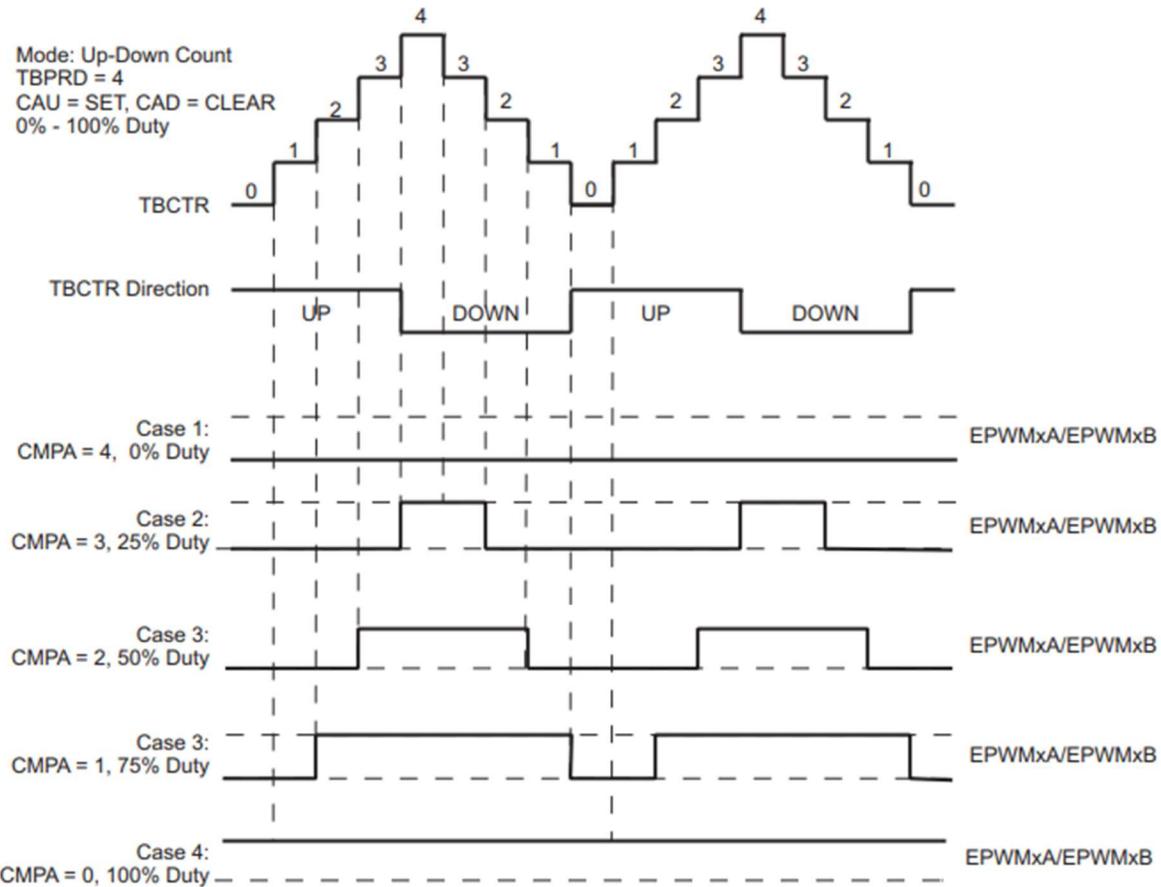


Figure 6.8: Up-Down-Count Mode Symmetrical Waveform [28]

6.5 PROGRAMMING METHOD TO GENERATE EPWM FOR PROPOSED INVERTER

We will be generating a 1 KHz wave signal at ePWM1A with a duty cycle of 50%. The registers that are involved are:

- TBPRD: define signal frequency.
- TBCTL: setup operating mode and time pre-scale.
- AQCTLA: define signal shape for ePWM1A.

The formula to calculate the signal frequency is given under:

$$TBPRD = \frac{1}{2} * \frac{T_{PWM}}{T_{SYSCLKOUT} * CLKDIV * HSPCLKDIV} \quad (44)$$

Procedure:

1. Using Code Composer Studio, we create a new CCS Project in any path that is accessible to us.
2. We then define the size of the C system stack. In the project window, we choose the project name, right click on it, and then select “Properties”. In category “C/C++ Build”, “C2000 Linker”, “Basic Options” and set the C stack size to 0x400.
3. In the C/C++ perspective, we right click at project name and select “**Link Files to Project**”. We then go to folder “C:\tidcs\c28\ dsp2833x\v131\DSP2833x_headers\source” and link:

- **DSP2833x_GlobalVariableDefs.c**

4. We again repeat the “Link Files to Project” step. From C:\tidcs\c28\ dsp2833x\v131\ DSP2833x_common\source we add:

- **DSP2833x_CodeStartBranch.asm**
- **DSP2833x_SysCtrl.c**
- **DSP2833x_ADC_cal.asm**
- **DSP2833x_usDelay.asm**
- **DSP2833x_CpuTimers.c**
- **DSP2833x_PieCtrl.c**
- **DSP2833x_PieVect.c**
- **DSP2833x_DefaultIsr.c**

5. From C:\tidcs\c28\ dsp2833x\v131\DSP2833x_headers\cmd link to project “entitled”:

- **DSP2833x_Headers_nonBIOS.cmd**

6. We also have to extent the search path of the C-Compiler for include files. Right click at project name and select “Properties”. Select “C/C++ Build”, “C2000 Compiler”, “Include Options”. We select the path for header and common files.

C:\tides\c28\ dsp2833x\v131\ DSP2833x_headers\include

C:\tides\c28\ DSP2833x\v131\ DSP2833x_common\include

Build, Test and Load

7. Check the “Rebuild Active Project” button or perform:

Project → Rebuild All (Alt+B)

and watch the tools run in the build window. If you get errors or warnings, debug as necessary.

8. Load the output file in the debugger session:

Target → Debug Active Project

and switch into the “Debug” perspective.

9. Verify that in the debug perspective the window of the source code of the project is high-lighted and that the blue arrow for the current Program Counter position is placed under the line “void main(void)”
10. Perform a real time run.

Target → Run

Modify Source Code

11. In CCS, switch to the “C/C++” perspective. In function "Gpio_select()", set multiplex register line GPIO0 to enable ePWM1A as output signal.
12. In “main()”, just after the call to the function "Gpio_select()", call a new function "Setup_ePWM1A()". Also, add a new function prototype at the beginning of “project.c”:

void Setup_ePWM1A(void);

13. At the end of project.c, add the definition of the new function "Setup_ePWM1A()". We will use this function to initialize ePWM1 to generate a 1 kHz square wave signal. We have to initialize the following registers:

- EPwm1Regs.TBCTL

- EPwm1Regs.TBPRD
- EPwm1Regs.AQCTLA

To setup the registers we can use either the "all"-member of the register union or the individual bit field member "bit". An instruction to "all" would require us to calculate a hexadecimal number for all 16 bits. By using the "bit" - structure we can leave the task to calculate the correct logical and/or -instruction to set or clear individual bit fields with the C-compiler. As an example, an instruction to setup the operating mode to "up/down"-mode would look like this:

- EPwm1Regs.TBCTL.bit.CTRMODE = 2;

Furthermore, we have to calculate the value for register TBPRD. If we use the "up/down" - counting operating mode for ePWM1A, the formula is:

$$TBPRD = \frac{1}{2} * \frac{T_{PWM}}{T_{SYSCLKOUT} * CLKDIV * HSPCLKDIV} \quad (45)$$

The factor 1/2 must be used in "up/down operating mode. TBPRD is a 16- bit register, therefore the maximum number for TBPRD is (2¹⁶ -1) or 65535. Now the objective is to generate a PWM signal of 1 kHz with the F28335ControlCard running at 150 MHz. [29]

In function "Setup_ePWM1A()" initialize:

```
EPwm1Regs.TBCTL.bit.CLKDIV = 0;           // CLKDIV = 1
EPwm1Regs.TBCTL.bit.HSPCLKDIV = 1;         //HSPCLKDIV = 2
EPwm1Regs.TBCTL.bit.CTRMODE = 2;           // up-down mode
EPwm1Regs.TBPRD = 37500;                  // 1Khz Signal = PWM signal
EPwm1Regs.AQCTLA.all = 0x0006;            // zero = set; period = clear
```

CHAPTER 7 - SIMULATION VERIFICATION

The proposed modified inverters are made to operate at different modulation index (M) and Duty Cycle (Ds). We have taken the Modulation index to be 0.7 and the Duty Cycle is 0.3. The simulations are performed using the PSIM software of version 9.1.4. The frequency of the reference sinusoidal signal is 50 Hz and the frequency of the carrier triangular waveform is 20 kHz. The capacitor and inductors parameter are designed accordingly. The % ripple current in the inductor and the % ripple voltage in the capacitor is taken as The simulation analysis for each 30% and 1% respectively.

7.1 INPUT VOLTAGE ASSISTED MODIFIED SWITCHED BOOST INVERTER

For $M = 0.7$, $D_s = 0.3$, the capacitors (C_1, C_2) values are $50.4 \mu\text{F}$ and $60 \mu\text{F}$. The inductors (L_1, L_2) values are 0.9 mH and 0.75 mH . The input from the supply is 24 V. The proposed CC-qZSI gives $V_{c1} = 61.89 \text{ V}$, $V_{c2} = 88.42 \text{ V}$. Line output voltage ($V_{ab} = V_{bc} = V_{ca}$) = 54.3 V (rms); Phase output voltage ($V_{an} = V_{bn} = V_{cn}$) = 13.7 V (rms); Phase output current ($I_{an} = I_{bn} = I_{cn}$) = 0.98 A (rms); The values of the boost factor (B) = 5.26. The resistance taken is 14 ohm.

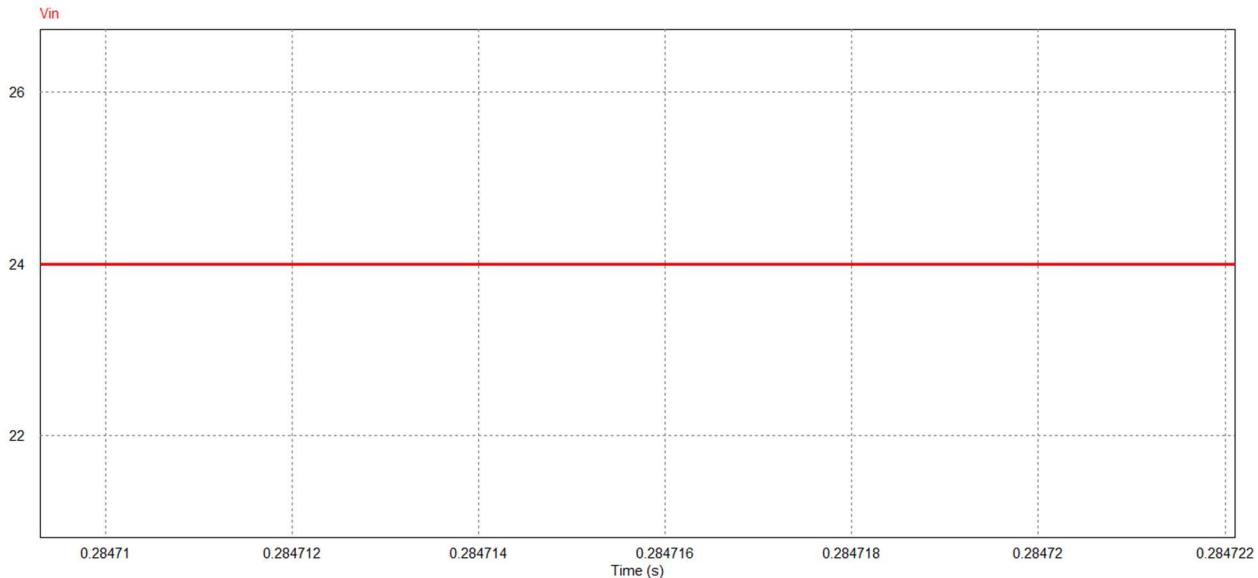


Figure 7. 1: Input Voltage

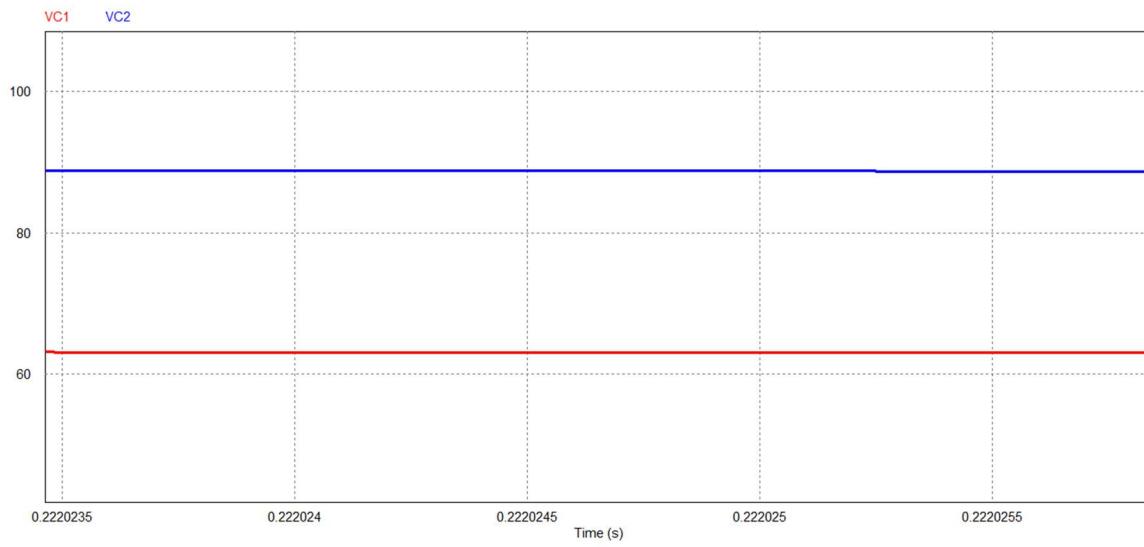


Figure 7.2: Capacitor Voltages

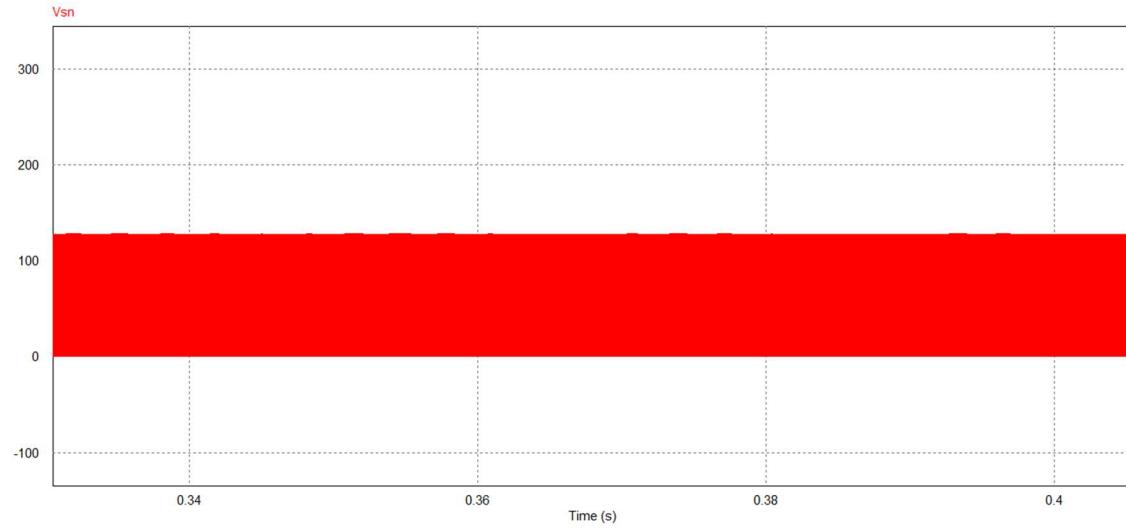


Figure 7.3: Node Voltage

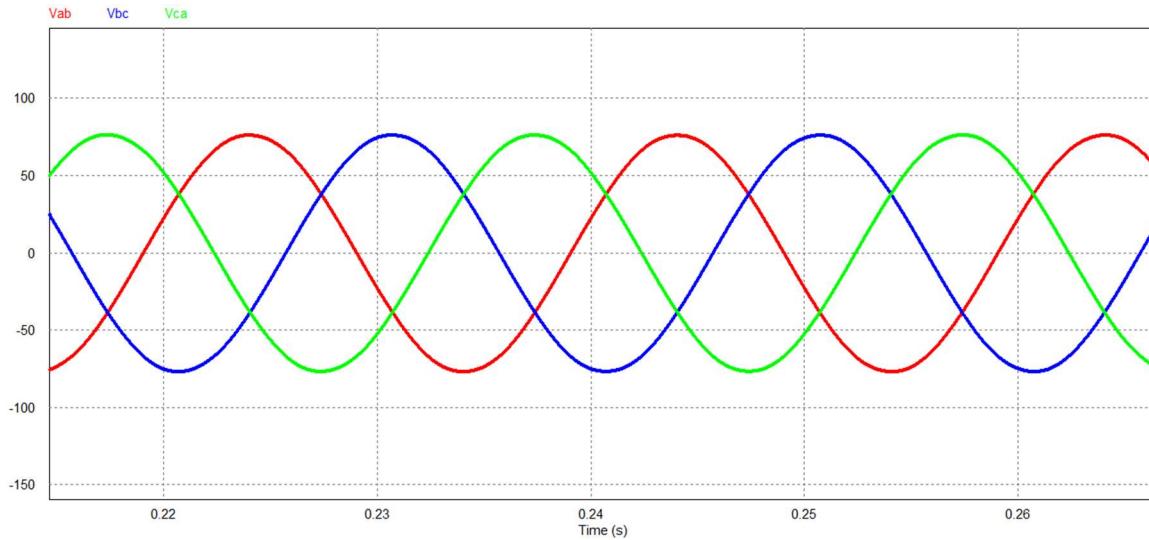


Figure 7.4: Line Voltage

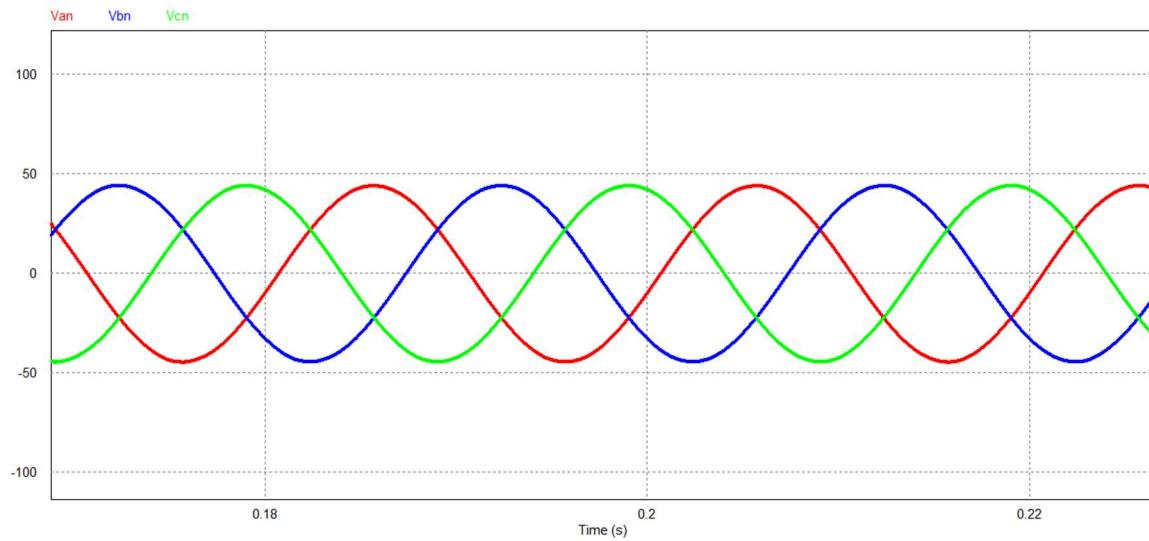


Figure 7.5: Phase Voltage

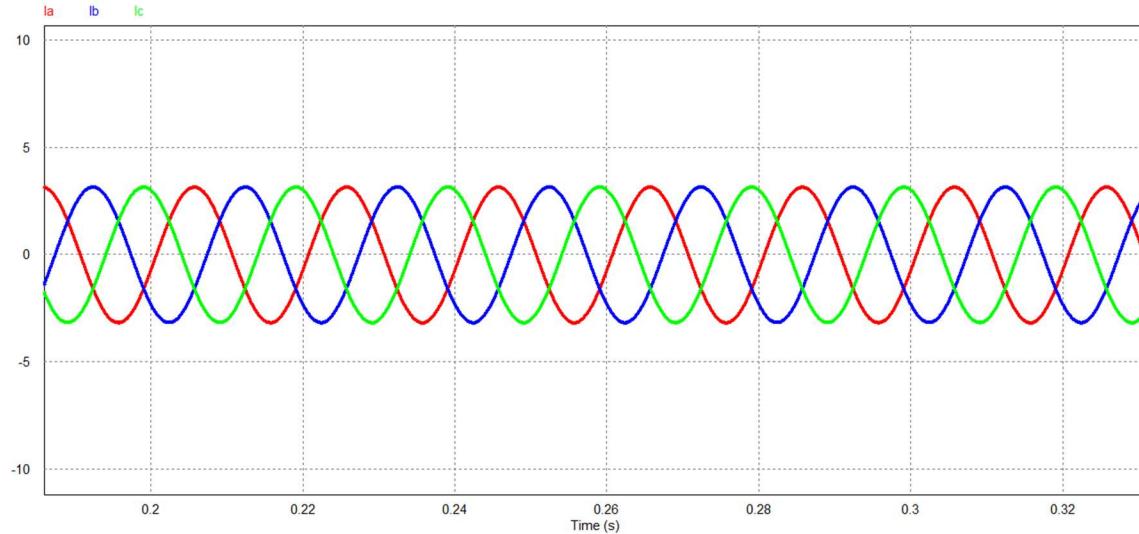


Figure 7.6: Phase current

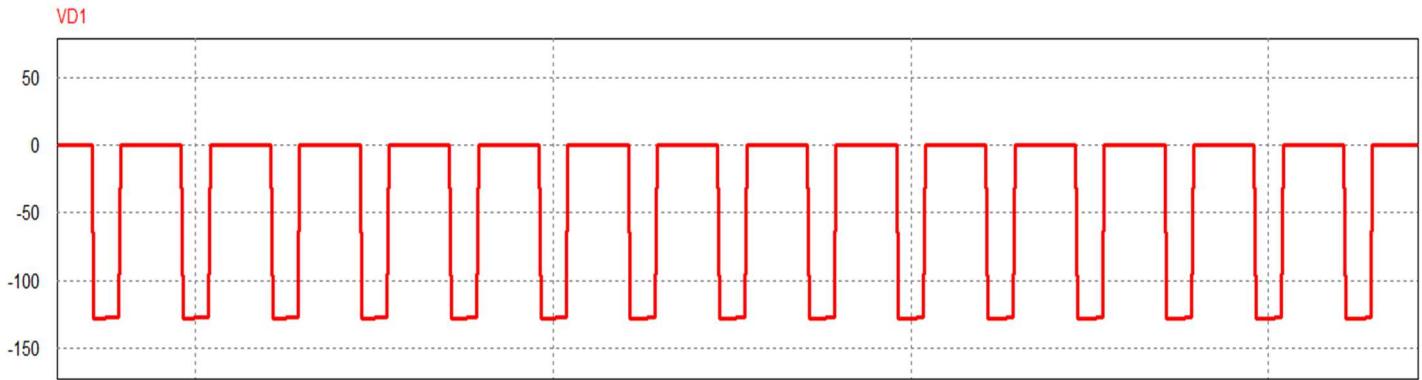


Figure 7.7: Voltage across diode 1

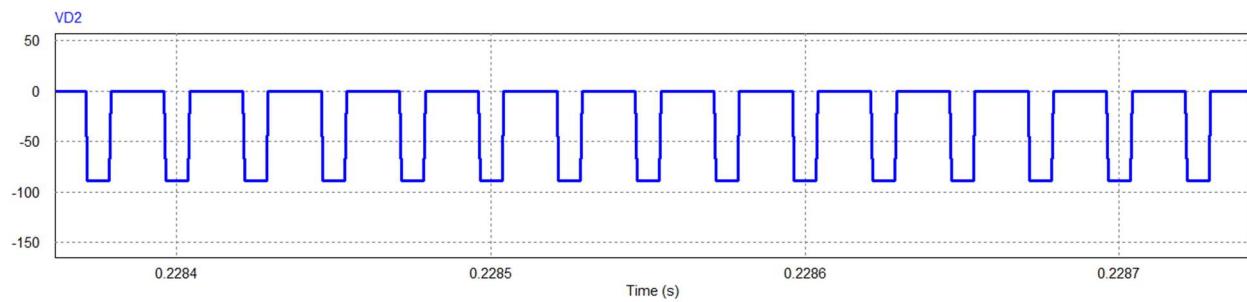
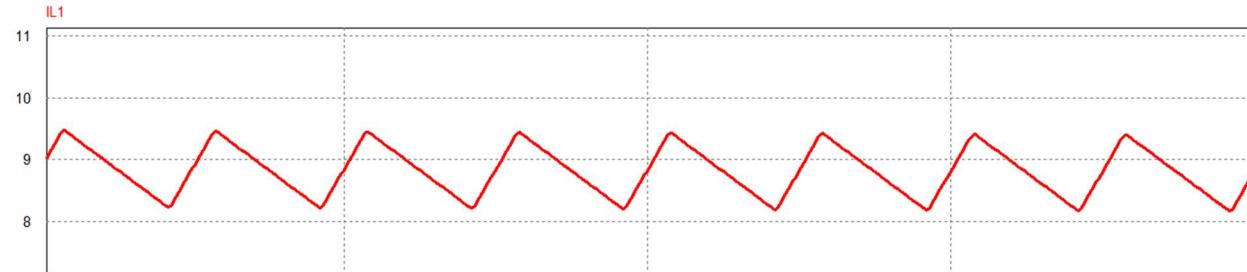


Figure 7.8: Voltage across diode 2



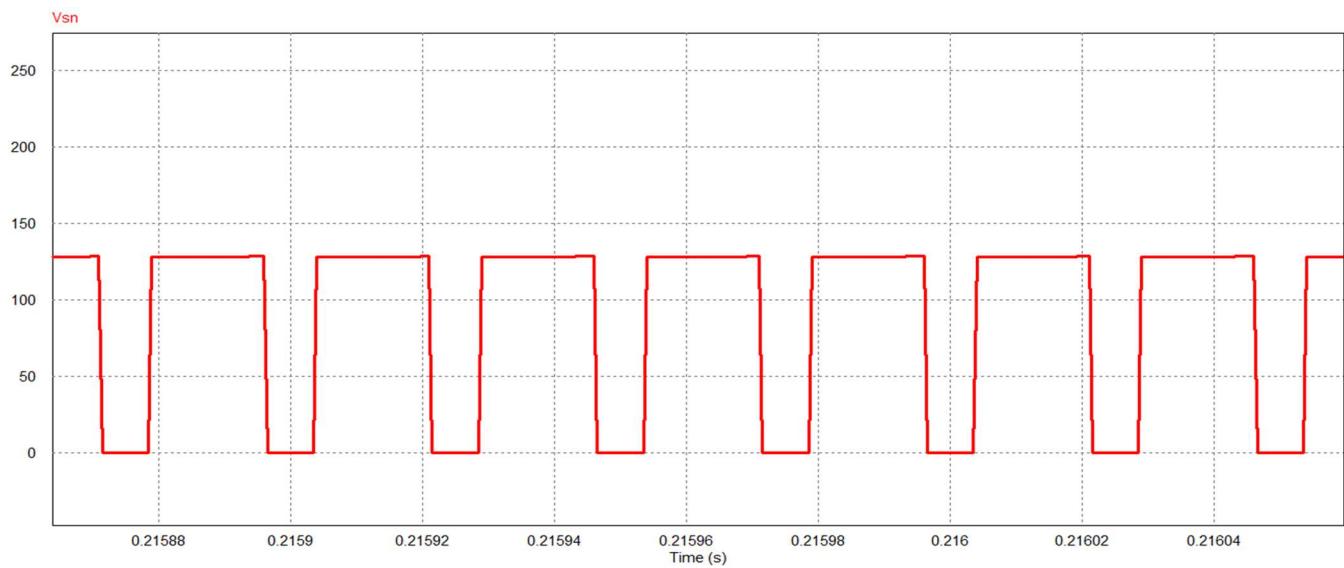


Figure 7.12: Node voltage

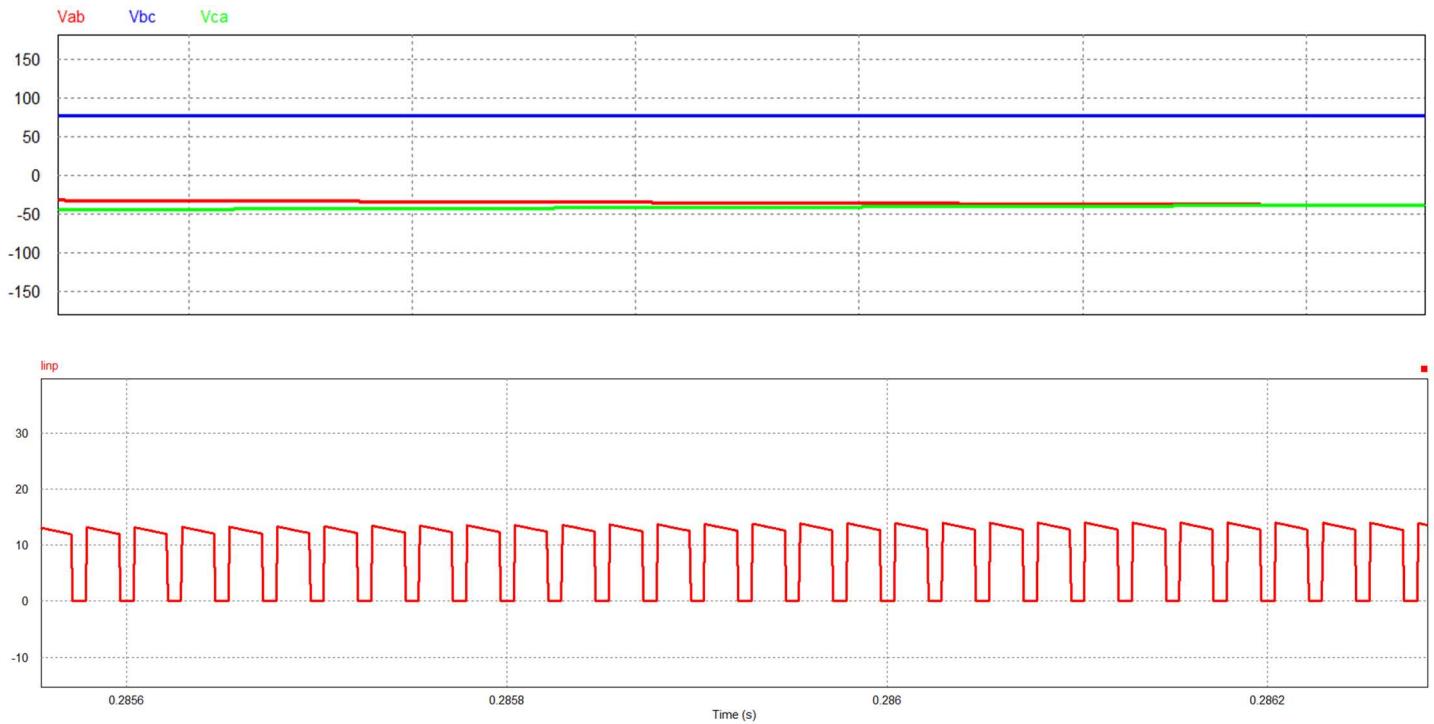


Figure 7.13: Discontinuity in Input Current

Table 7. 1: Comparison between calculated and simulated values for VMSBI

Parameters	Calculated	Simulated
VC1 (V)	61.89	61.2
VC2 (V)	88.42	88.21
IL1 (A)	8.8	8.72
IL2 (A)	6.4	6.24
VD1 (V)	-126.31	-126.1
VD2 (V)	-88.42	-88.16
Vsw (V)	88.42	88.2
B	5.26	5.25
Vsn (V)	126.31	126.07
Vab = Vbc = Vca (rms) (V)	54.3	54.2
Van= Vbn = Vcn (rms) (V)	31.7	31.3
Ian = Ibn = Icn (rms) (A)	2.26	2.21

7.2 SWITCHED INDUCTOR-SWITCHED CAPACITOR SBI

For $M = 0.7$, $D_s = 0.3$, the capacitors (C_1, C_2) values are $61.7 \mu\text{F}$ and $140.1 \mu\text{F}$. The inductors (L_1, L_2) values are 0.53 mH and 0.53 mH . The input from the supply is 24 V . The proposed CC-qZSI gives $V_{c1} = 50.52\text{V}$, $V_{c2} = 37.89 \text{ V}$. Line output voltage ($V_{ab} = V_{bc} = V_{ca}$) = 37.85 V (rms); Phase output voltage ($V_{an} = V_{bn} = V_{cn}$) = 21.85 V (rms); Phase output current ($I_{an} = I_{bn} = I_{cn}$) = 4.37 A (rms); The values of the boost factor (B) = 3.68 . The resistance is 5 ohm .

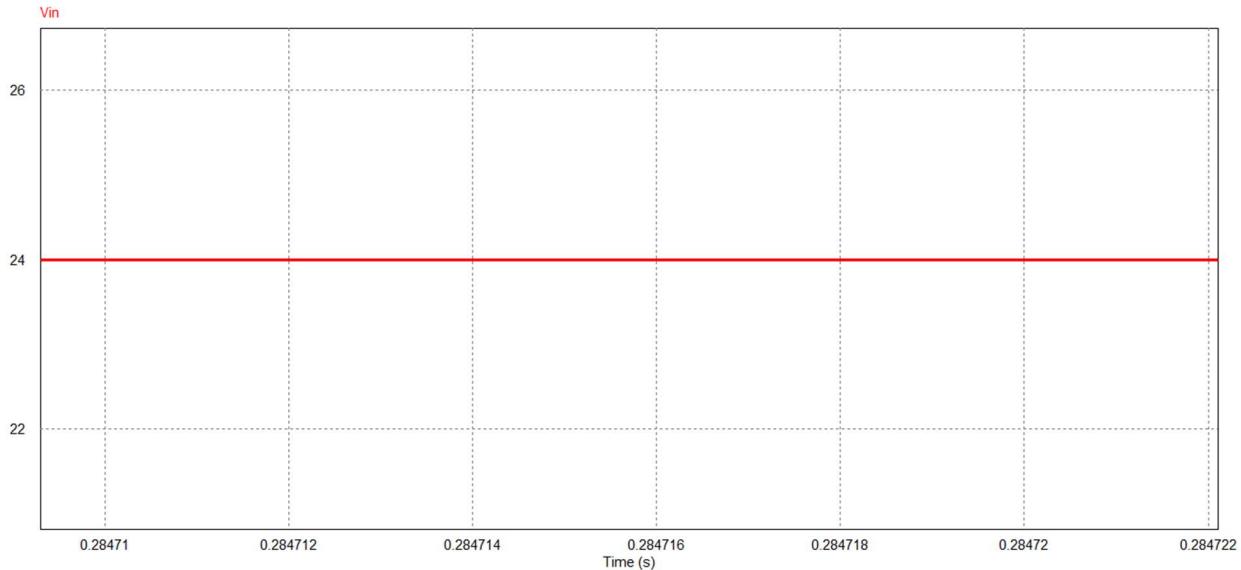


Figure 7. 14: Input Voltage

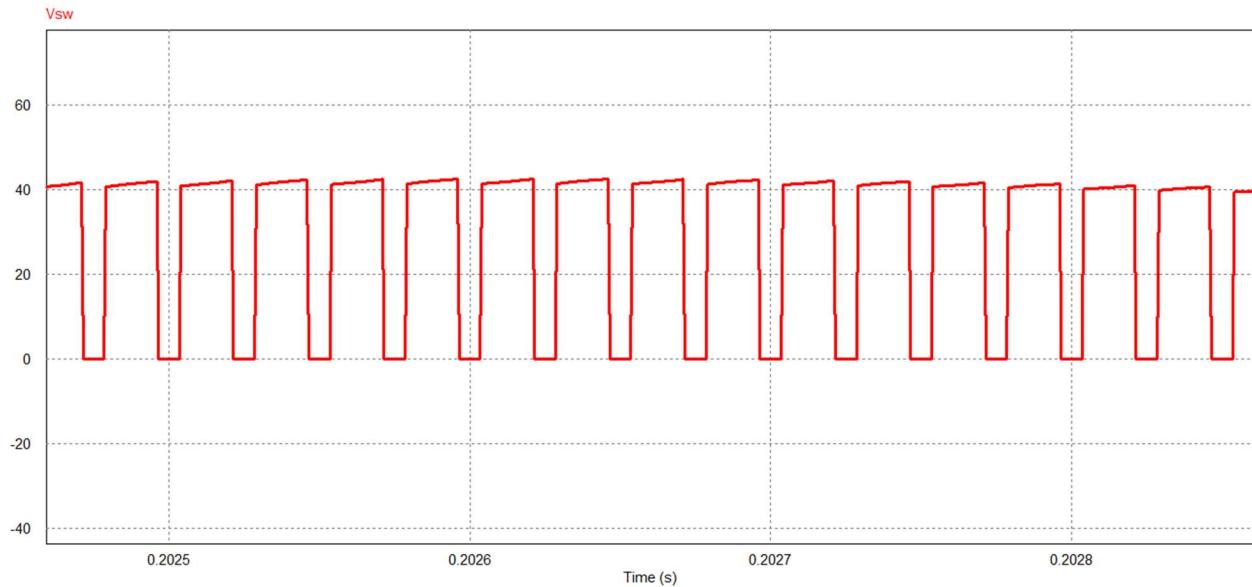


Figure 7. 15: Switch voltage

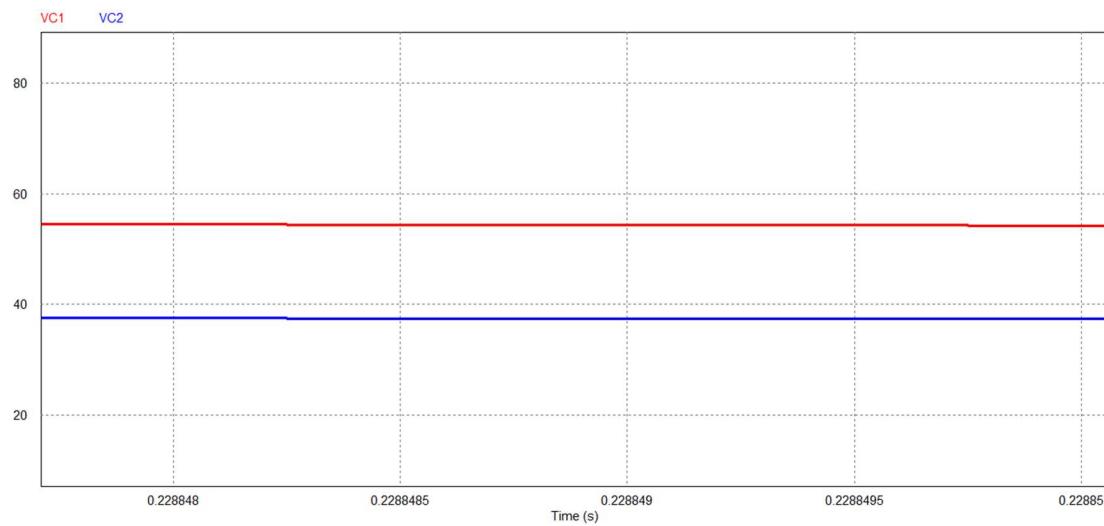


Figure 7.16: Voltage across capacitors

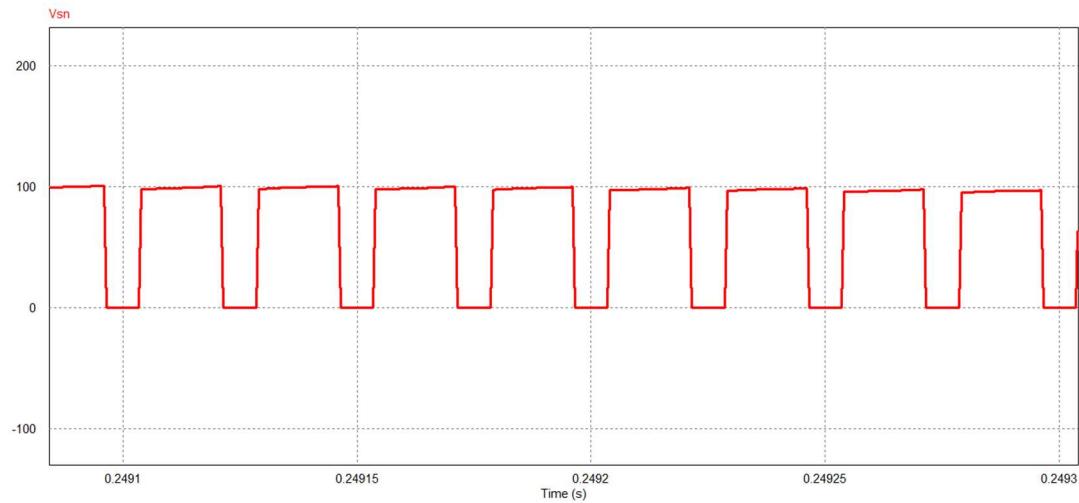


Figure 7.17: Node voltage

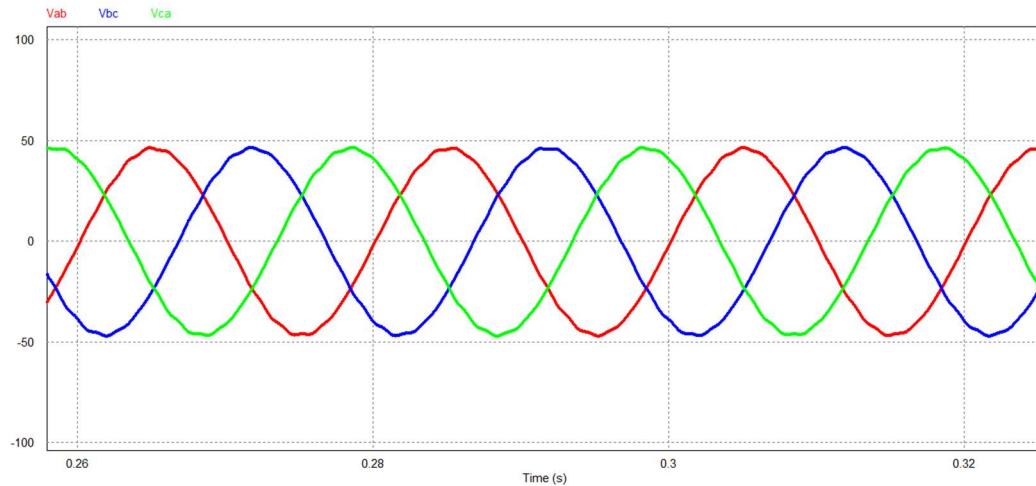


Figure 7.18: Line Voltage

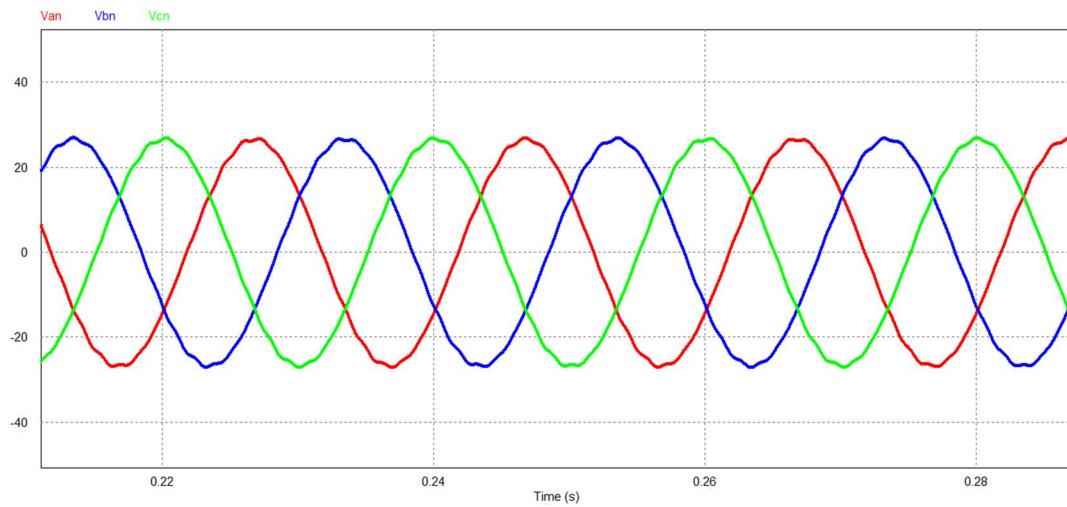


Figure 7.19: Phase voltage

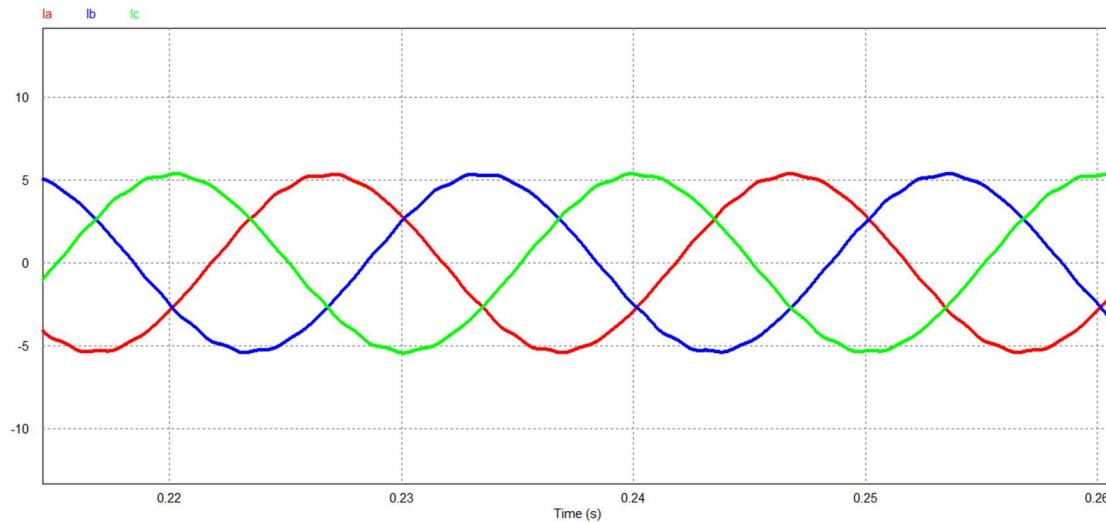
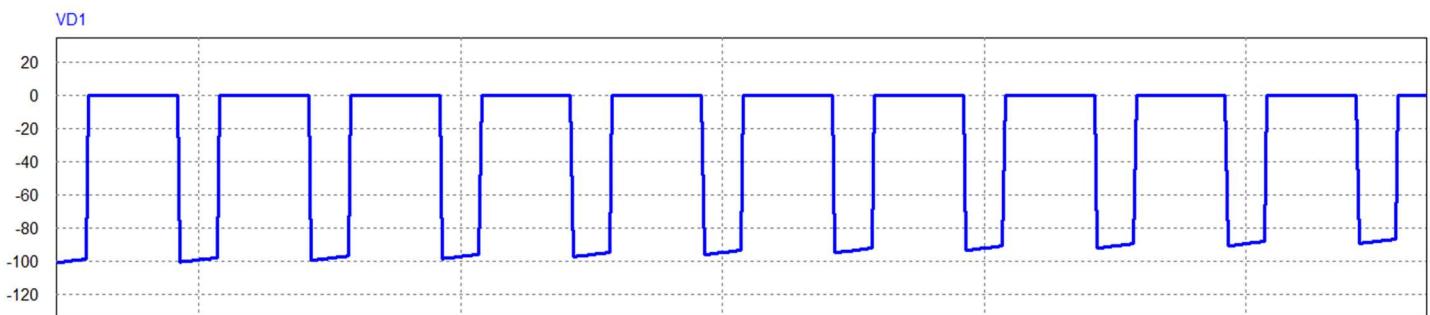


Figure 7.20: Phase Current



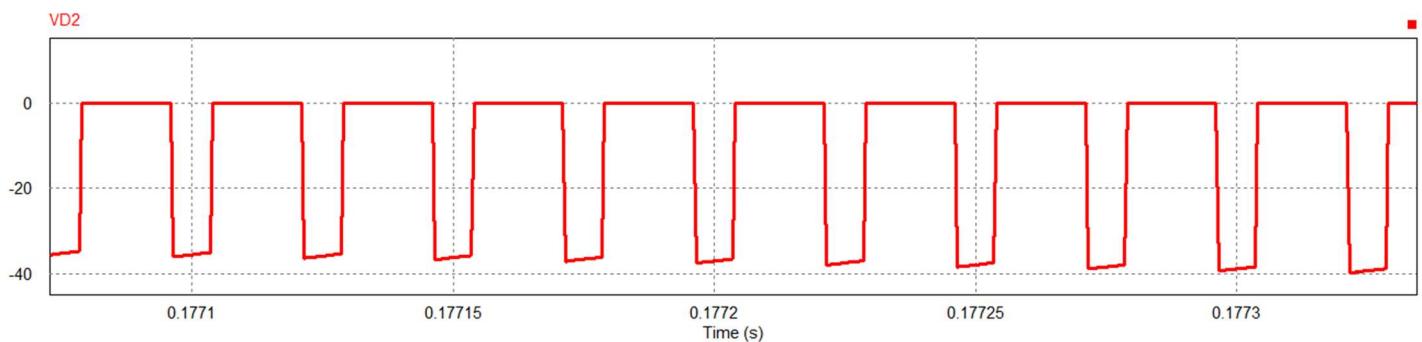


Figure 7.21: Voltage across diodes

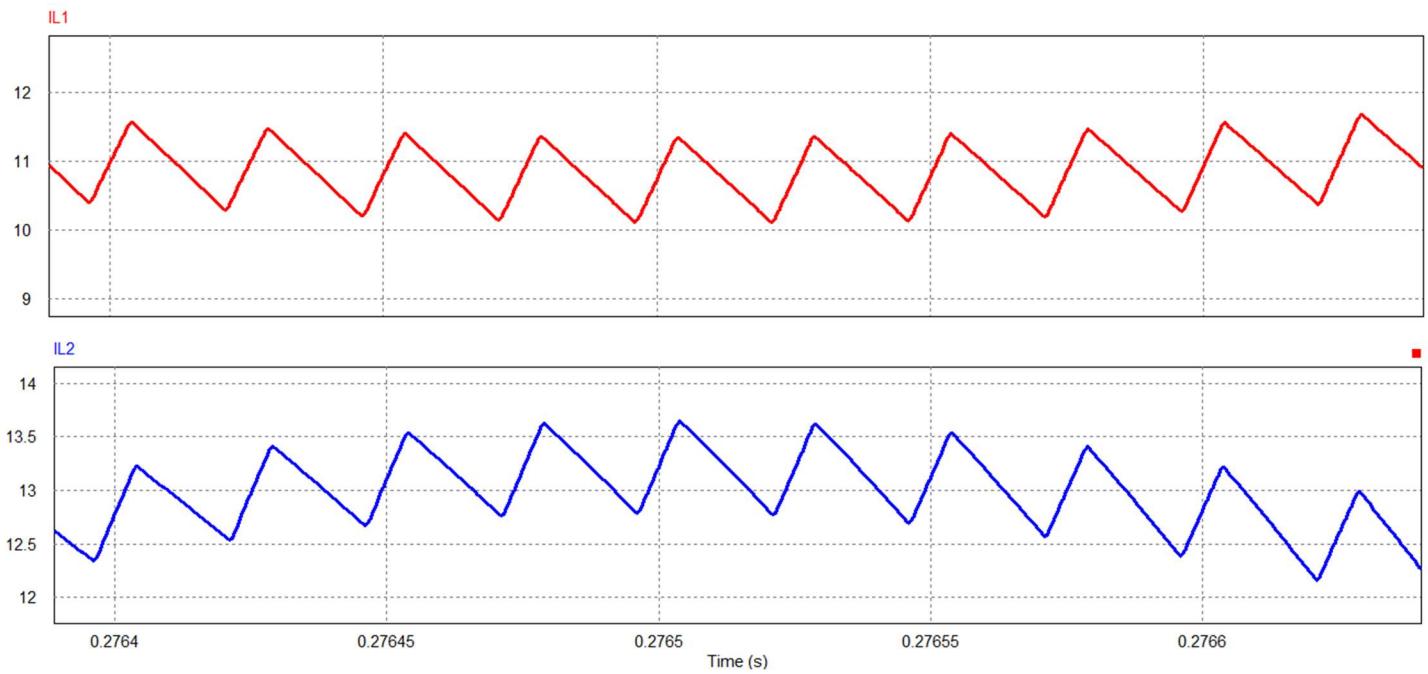


Figure 7.22: Current across inductors

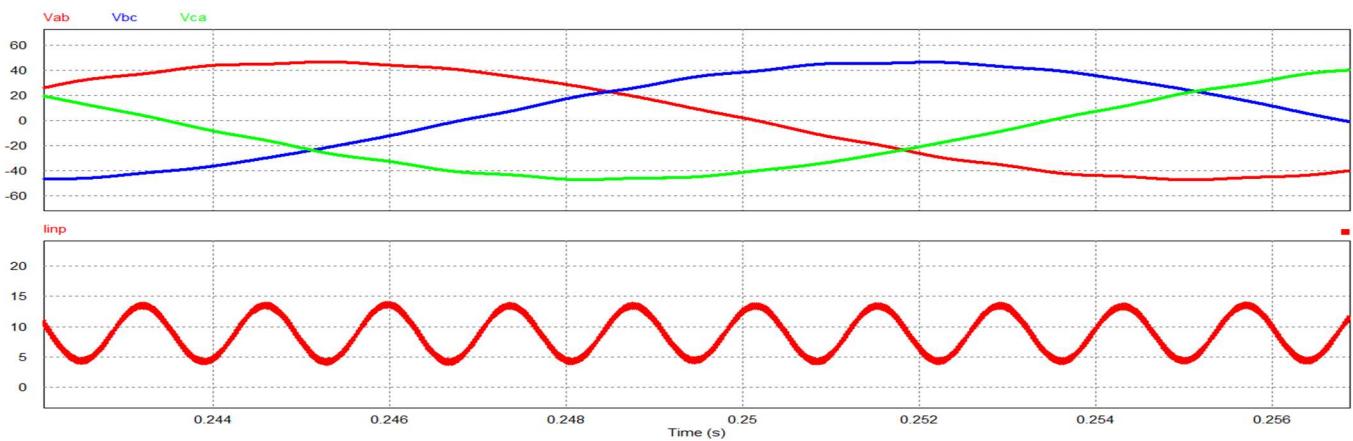


Figure 7.23: Continuity in Input Current

Table 7. 2: Comparison between calculated and simulated values for SLC- MSBI

Parameters	Calculated	Simulated
V _{C1} (V)	50.52	50.1
V _{C2} (V)	37.89	37.1
I _{L1} (A)	8.4	8.1
I _{L2} (A)	6.3	6.1
V _{D1} (V)	-176.8	-176.2
V _{D2} (V)	-126.3	-126.1
V _{sw} (V)	126.3	126.0
B	3.68	3.61
V _{sn} (V)	88.42	88.2
V _{ab} = V _{bc} = V _{ca} (rms) (V)	32.7	32.7
V _{an} = V _{bn} = V _{cn} (rms) (V)	21.85	21.1
I _{an} = I _{bn} = I _{cn} (rms) (A)	4.37	4.1

7.3 COMMON GROUND BASED MODIFIED SBI

For $M = 0.7$, $D_s = 0.3$, the capacitors (C_1, C_2) values are $85.7 \mu\text{F}$ and $117.6 \mu\text{F}$. The inductors (L_1, L_2) values are 0.55 mH and 0.11 mH . The input from the supply is 24 V . The proposed CC-qZSI gives $V_{c1} = 26.52\text{V}$, $V_{c2} = 61.89 \text{ V}$. Line output voltage ($V_{ab} = V_{bc} = V_{ca}$) = 37.85 V (rms); Phase output voltage ($V_{an} = V_{bn} = V_{cn}$) = 21.85 V (rms); Phase output current ($I_{an} = I_{bn} = I_{cn}$) = 4.37 A (rms); The values of the boost factor (B) = 3.68 . The resistance is taken as 5 ohm .

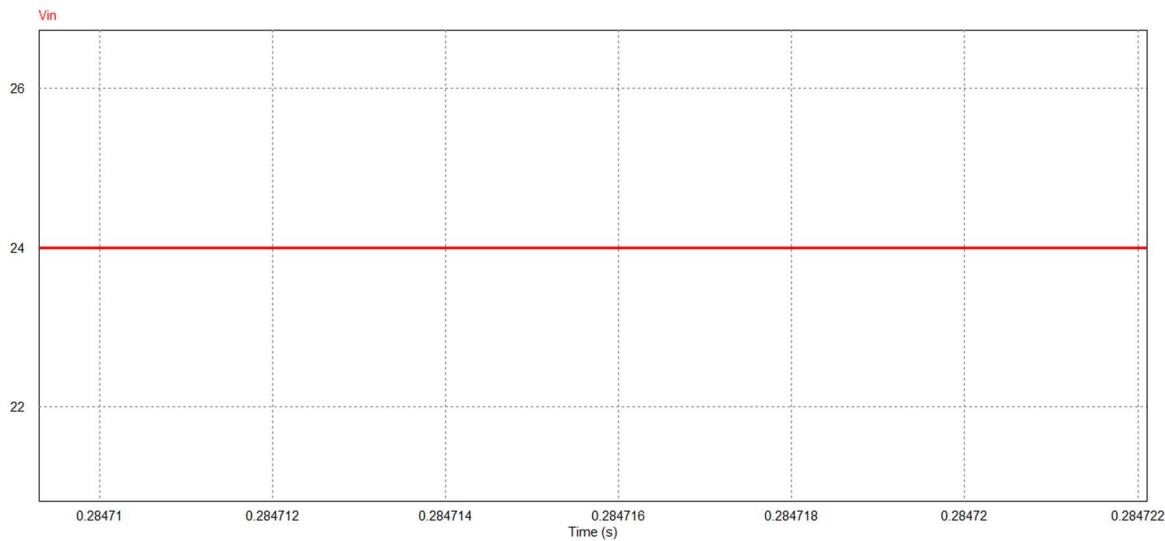


Figure 7. 24: Input Voltage

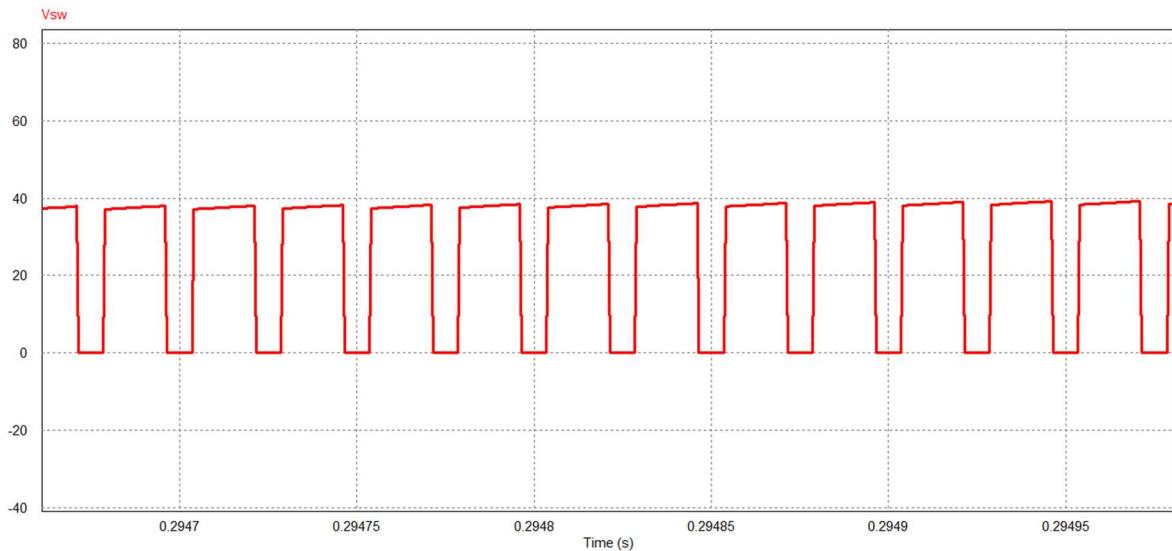


Figure 7. 25: Switch voltage

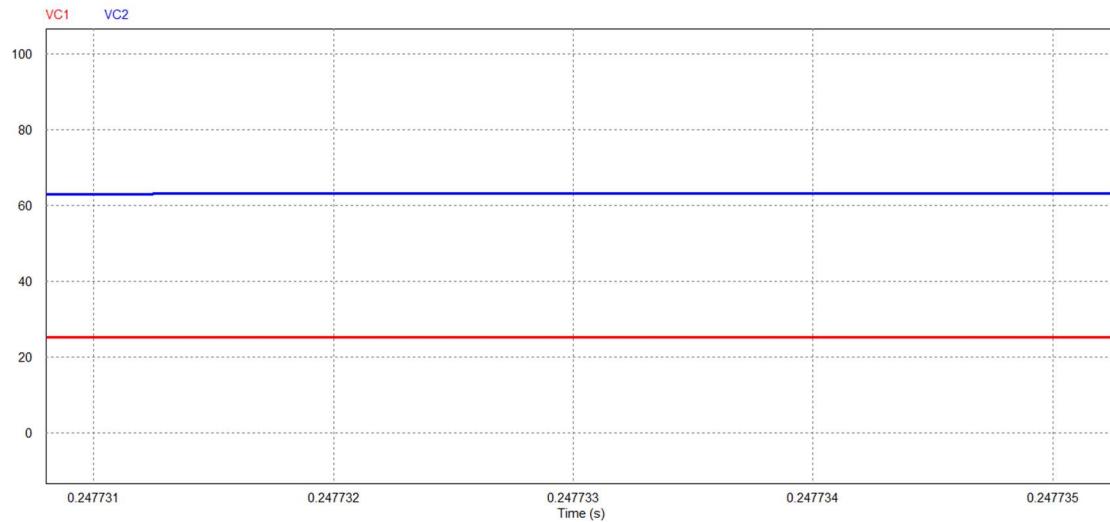


Figure 7.26: Capacitor voltages

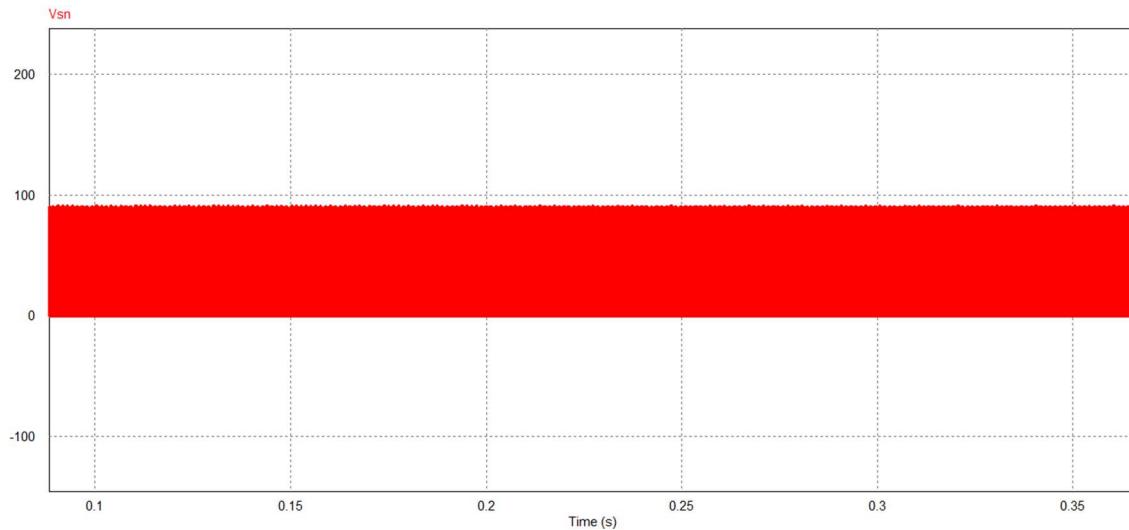


Figure 7.27: Node voltage

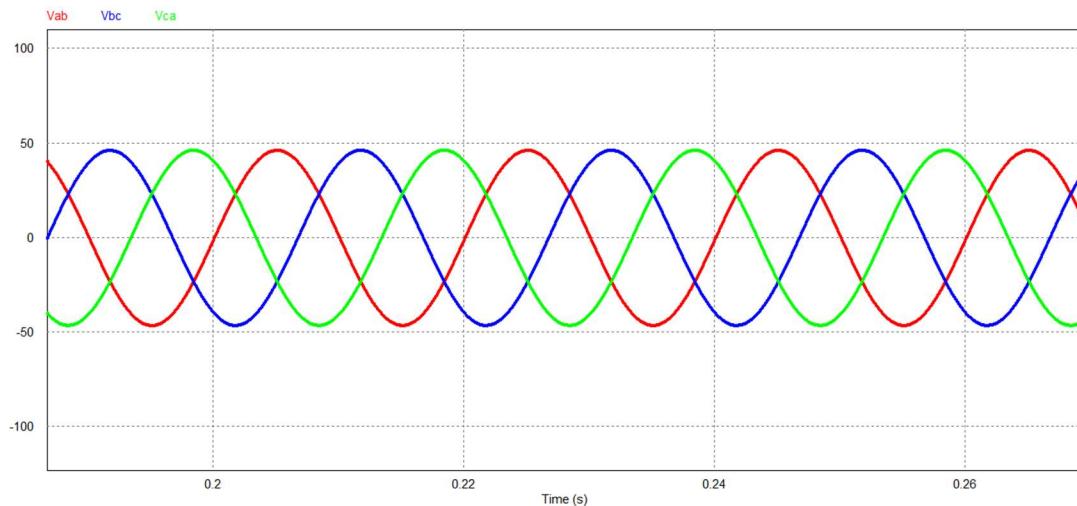


Figure 7.28: Line voltage

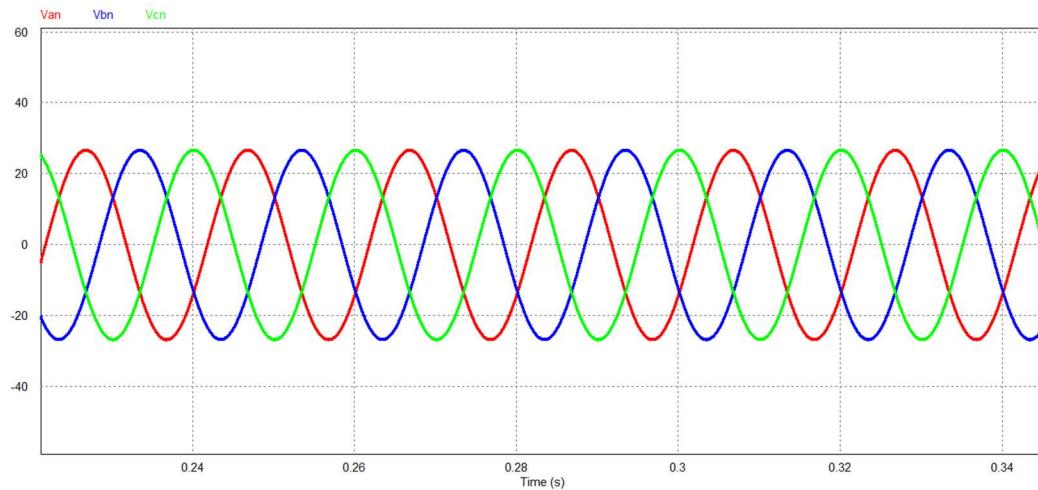


Figure 7.29: Phase voltages

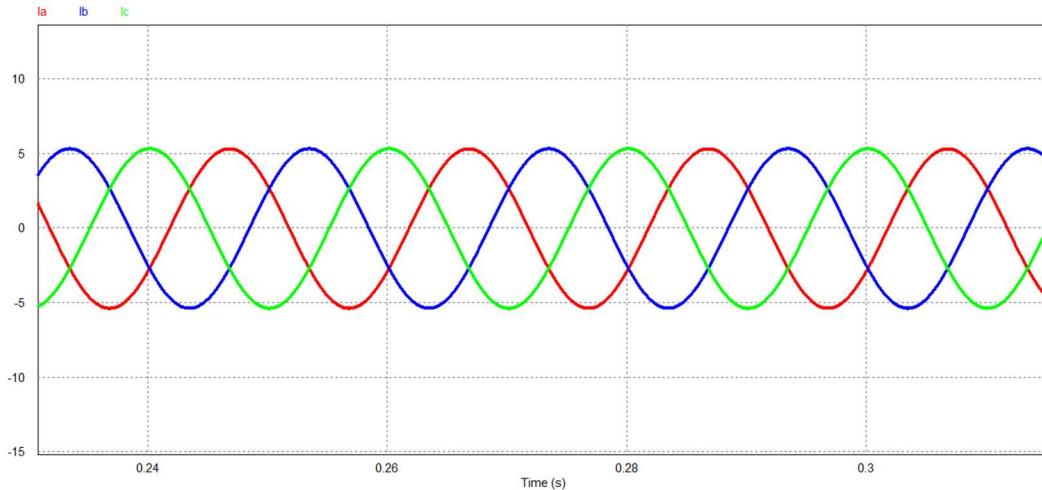


Figure 7.30: Phase currents

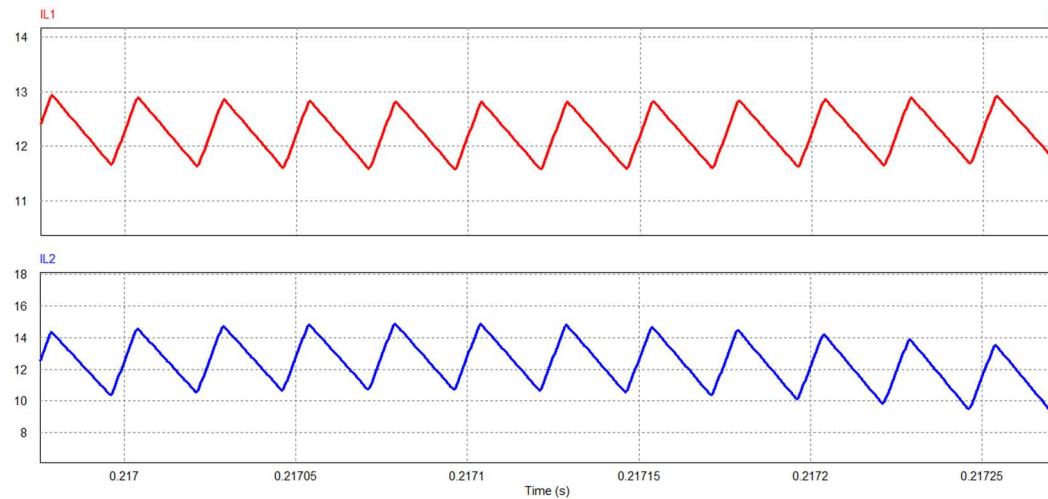


Figure 7.31: Current across inductors

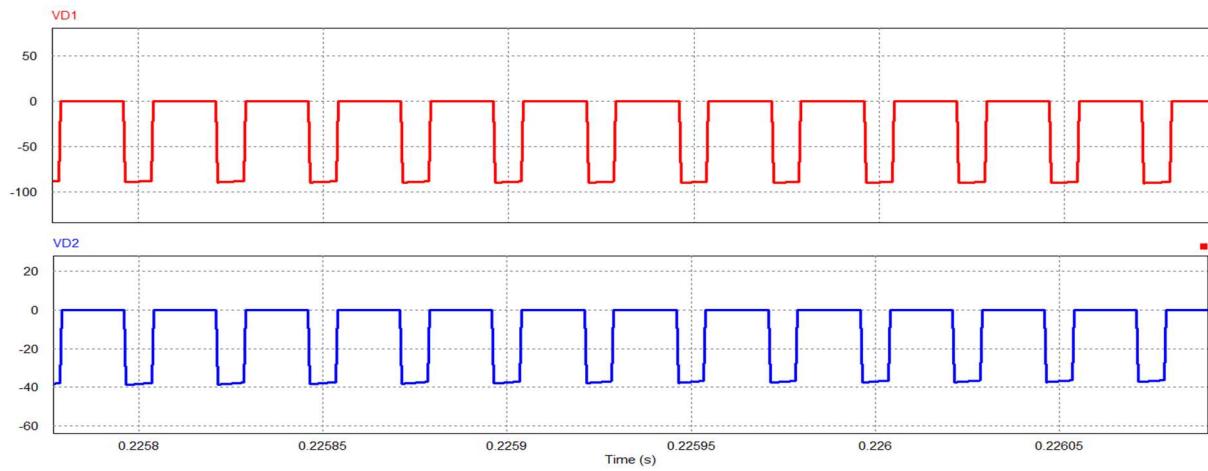


Figure 7.32: Voltage across diodes

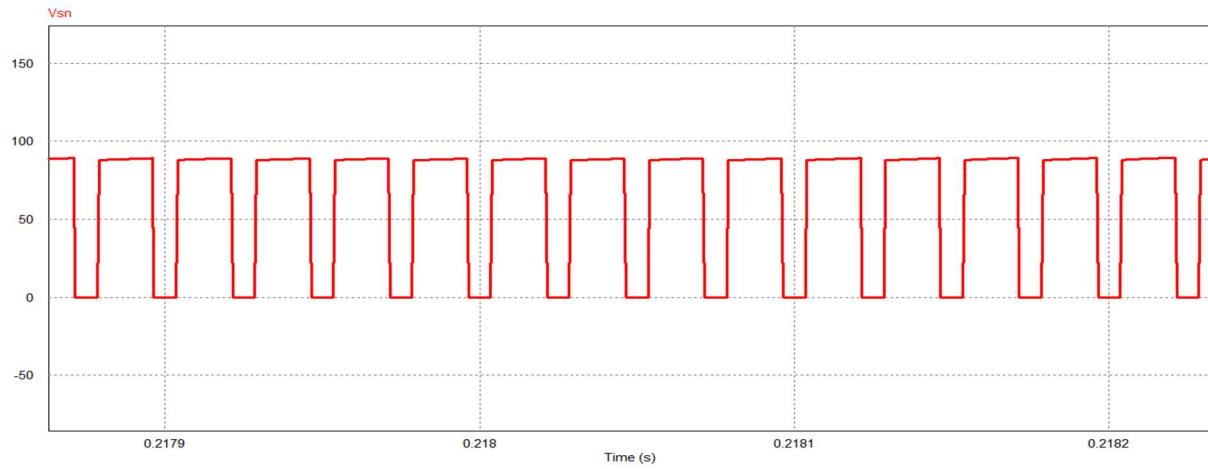


Figure 7.33: Node voltage

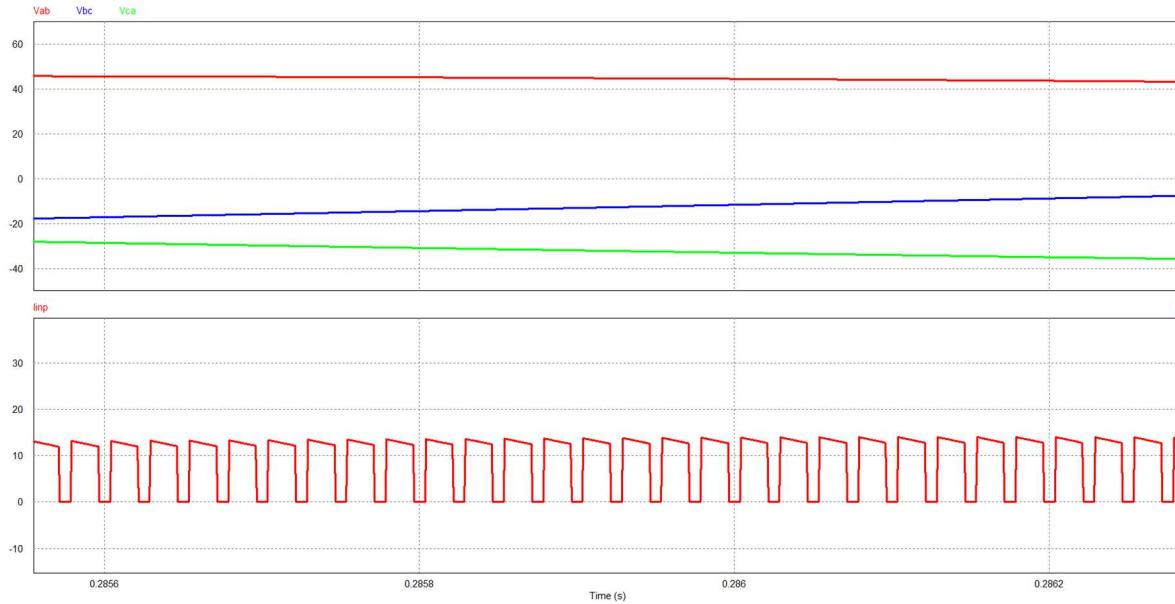


Figure 7.34: Discontinuity in Input Current

Table 7. 3: Comparison between calculated and simulated values for CG-MSBI

Parameters	Calculated	Simulated
V _{C1} (V)	26.52	26.1
V _{C2} (V)	61.89	61.5
I _{L1} (A)	8.4	8.32
I _{L2} (A)	6.1	5.98
V _{D1} (V)	-88.42	-88.1
V _{D2} (V)	-11.36	-11.1
V _{sw} (V)	11.36	11.1
B	3.68	3.61
V _{sn} (V)	88.42	88.2
V _{ab} = V _{bc} = V _{ca} (rms) (V)	37.85	37.1
V _{an} = V _{bn} = V _{cn} (rms) (V)	21.85	21.1
I _{an} = I _{bn} = I _{cn} (rms) (V)	4.37	4.25

CHAPTER 8 - COMPARATIVE ANALYSIS

Table 8. 1: Different attributes for different modifications

ATTRIBUTES	VM-SBI	SLC-MSBI	CG-MSBI	CC-qZSI
V_{C1}	$\frac{(1-D)^2}{1-3D+D^2} V_{in}$	$\frac{(1-2D)}{1-3D+D^2} V_{in}$	$\frac{D(1-2D)}{1-3D+D^2} V_{in}$	$\frac{D_s}{1-3D+D^2} V_{in}$
V_{C2}	$\frac{(1-D)}{1-3D+D^2} V_{in}$	$\frac{D}{1-3D+D^2} V_{in}$	$\frac{1-2D+D^2}{1-3D+D^2} V_{in}$	$\frac{1-D_s}{1-3D+D^2} V_{in}$
V_{L1}	$\frac{2-3D+D^2}{1-3D+D^2} V_{in}$	$\frac{(1-D)}{1-3D+D^2} V_{in}$	$\frac{(1-D)}{1-3D+D^2} V_{in}$	$\frac{3-3D+D^2}{1-3D+D^2} V_{in}$
V_{L2}	$\frac{(1-D)}{1-3D+D^2} V_{in}$	$\frac{1-3D+D^2}{1-3D+D^2} V_{in}$	$\frac{1-2D+D^2}{1-3D+D^2} V_{in}$	$\frac{1-D_s}{1-3D+D^2} V_{in}$
I_{C1}	$-\frac{(1-D)}{1-3D+D^2} I_{sn}$	$-\frac{(1-3D+2D^2)}{1-3D+D^2} I_{sn}$	$-\frac{(1-D)}{1-3D+D^2} I_{sn}$	$-\frac{(1-D)}{1-3D+D^2} I_{sn}$
I_{C2}	$-\frac{2-3D+D^2}{1-3D+D^2} I_{sn}$	$-\frac{(2-5D+3D^2)}{1-3D+D^2} I_{sn}$	$-\frac{(D^2-3D+2)}{1-3D+D^2} I_{sn}$	$-\frac{2-3D+D^2}{1-3D+D^2} I_{sn}$
I_{L1}	$\frac{(1-D)}{1-3D+D^2} I_{sn}$	$\frac{1-3D+2D^2}{1-3D+D^2} I_{sn}$	$\frac{(1-D)}{1-3D+D^2} I_{sn}$	$\frac{1-D_s}{1-3D+D^2} I_{sn}$
I_{L2}	$\frac{(1-D)^2}{1-3D+D^2} I_{sn}$	$\frac{1-2D+D^2}{1-3D+D^2} I_{sn}$	$\frac{(1-D)^2}{1-3D+D^2} I_{sn}$	$\frac{(1-D_s)^2}{1-3D+D^2} I_{sn}$
V_{sn}	$\frac{V_{in}}{1-3D+D^2}$	$\frac{(1-D)}{1-3D+D^2} V_{in}$	$\frac{(1-D)}{1-3D+D^2} V_{in}$	$\frac{V_{in}}{1-3D+D^2}$
B	$\frac{1}{1-3D+D^2}$	$\frac{(1-D)}{1-3D+D^2}$	$\frac{(1-D)}{1-3D+D^2}$	$\frac{1}{1-3D+D^2}$
G	$\frac{1-D}{1-3D+D^2}$	$\frac{(1-D)^2}{1-3D+D^2}$	$\frac{(1-D)^2}{1-3D+D^2}$	$\frac{(1-D)}{1-3D+D^2}$

The characteristics curve between the Duty cycle (Ds) and Boost factor (B) has been plotted for the conventional and the modification of the inverters.

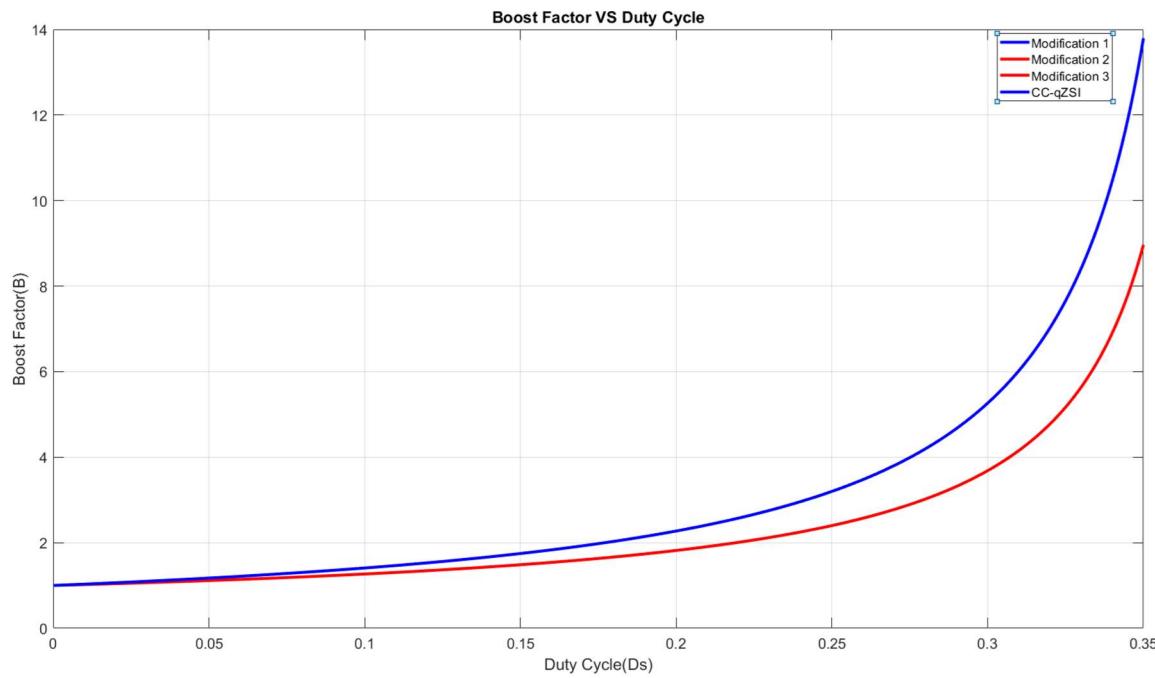


Figure 8.1: Boost factor VS Duty cycle for conventional and modified inverters

The characteristics curve between the Duty cycle (Ds) and Voltage Gain (G) has been plotted for the conventional and the modification of the inverters.

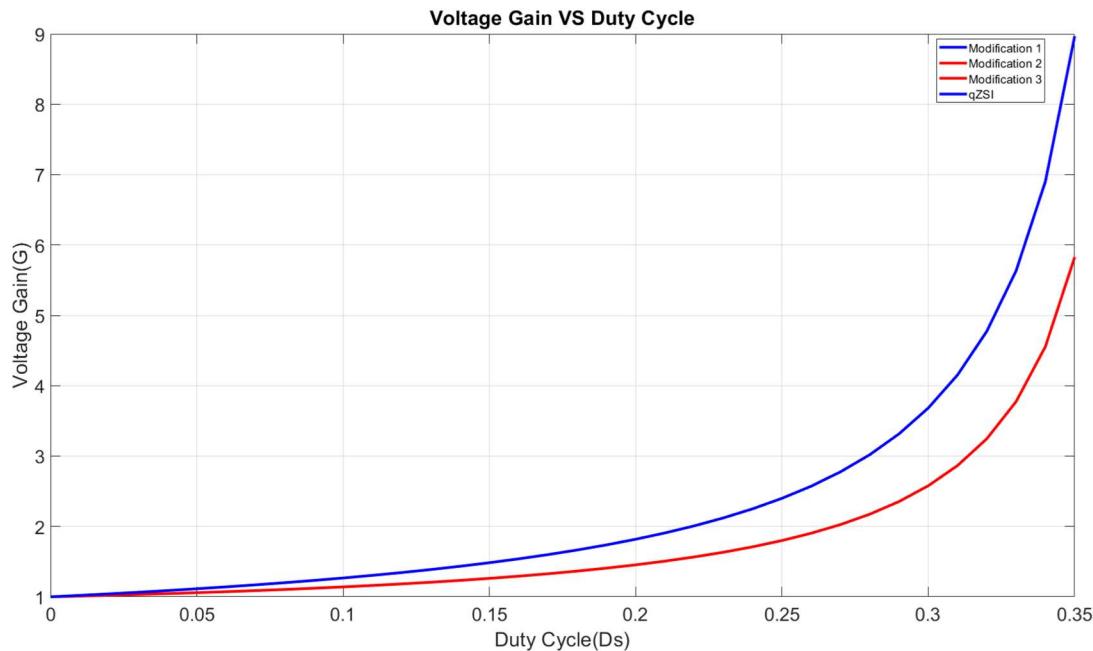


Figure 8.2: Voltage Gain VS Duty cycle for conventional and modified inverters

Table 8. 2: Voltage stresses of the elements in proposed inverters

Attributes	VMSBI	SLC-MSBI	CG-MSBI
C₁	$\frac{(1-D)^2}{D^2 - 3D + 1} V_{in}$	$\frac{1-2D}{D^2 - 3D + 1} V_{in}$	$\frac{(1-D)D}{D^2 - 3D + 1} V_{in}$
C₂	$\frac{(1-D)}{D^2 - 3D + 1} V_{in}$	$\frac{1}{D^2 - 3D + 1} V_{in}$	$\frac{(1-D)^2}{D^2 - 3D + 1} V_{in}$
D₁	$-\frac{1}{D^2 - 3D + 1} V_{in}$	$-\frac{2(1-D)}{D^2 - 3D + 1} V_{in}$	$-\frac{(1-D)}{D^2 - 3D + 1} V_{in}$
D₂	$-\frac{(1-D)}{D^2 - 3D + 1} V_{in}$	$-\frac{1}{D^2 - 3D + 1} V_{in}$	$-\frac{D}{D^2 - 3D + 1} V_{in}$
S_o	$\frac{(1-D)}{D^2 - 3D + 1} V_{in}$	$\frac{1}{D^2 - 3D + 1} V_{in}$	$\frac{D}{D^2 - 3D + 1} V_{in}$

Table 8. 3: Current stresses of the elements in proposed inverters

Attributes	VMSBI	SLC-MSBI	CG-MSBI
L₁	$\frac{(1-D)}{1 - 3D + D^2} I_{sn}$	$\frac{(1-D)}{1 - 3D + D^2} I_{sn}$	$\frac{(1-D)}{1 - 3D + D^2} I_{sn}$
L₂	$\frac{(1-D)^2}{1 - 3D + D^2} I_{sn}$	$\frac{(1-D)^2}{1 - 3D + D^2} I_{sn}$	$\frac{(1-D)^2}{1 - 3D + D^2} I_{sn}$
D₁	$\frac{1}{1 - 3D + D^2} I_{sn}$	$\frac{1}{1 - 3D + D^2} I_{sn}$	$\frac{1}{1 - 3D + D^2} I_{sn}$
D₂	$\frac{(1-D)}{1 - 3D + D^2} I_{sn}$	$\frac{(1-D)}{1 - 3D + D^2} I_{sn}$	$\frac{(1-D)}{1 - 3D + D^2} I_{sn}$
S_o	$\frac{(1-D)}{1 - 3D + D^2} I_{sn}$	$\frac{(1-D)}{1 - 3D + D^2} I_{sn}$	$\frac{(1-D)}{1 - 3D + D^2} I_{sn}$

CHAPTER 9 - VERIFICATION

Parameters	VMSBI			SLC-MSBI			CG-MSBI		
	Th	Sim	%Error	Th	Sim	%Error	Th	Sim	%Error
V _{C1} (V)	61.89	61.2	1.11	50.52	50.1	0.83	26.52	26.1	1.58
V _{C2} (V)	88.42	88.21	0.23	37.89	37.1	2.08	61.89	61.5	0.63
I _{L1} (A)	8.8	8.72	0.9	8.4	8.2	2.3	8.4	8.32	0.95
I _{L2} (A)	6.4	6.24	2.5	6.3	6.21	1.42	6.1	5.98	1.96
V _{D1} (V)	-126.31	-126.1	0.16	-176.8	-176.2	0.33	-88.42	-88.1	0.36
V _{D2} (V)	-88.42	-88.16	0.29	-126.3	-126.1	0.15	-11.36	-11.1	2.22
V _{sw} (V)	88.42	88.03	0.44	126.3	126.0	0.23	11.36	11.1	2.2
B	5.26	5.25	0.19	3.68	3.61	1.9	3.68	3.61	1.9
V _{sn} (V)	126.31	126.07	0.19	88.42	88.2	0.24	88.42	88.2	0.24
V _{ab} = V _{bc} = V _{ca} (rms) (V)	54.3	54.2	0.18	32.7	32.7	0.0	32.7	32.5	0.61
V _{an} = V _{bn} = V _{cn} (rms) (V)	31.7	31.3	1.26	21.85	21.5	1.6	21.85	21.5	1.6
I _{an} = I _{bn} = I _{cn} (rms) (V)	2.26	2.21	2.2	4.37	4.24	2.97	4.37	4.25	2.8

CONCLUSION

The conventional inverters are divided into CSI and VSI. The conventional CSI and VSI has drawback. In order to eliminate the conventional VSI and CSI, new inverter known as ZSI are proposed by F. Z. Feng. However, the conventional ZSI is limited with boost factor, and it is not capable to meet the voltage requirement coming from renewable energy resources. As the renewable energy resources are low voltage generation capability. So, in order to meet the desire voltage level, inverter should have high voltage conversion capability.

In this project three ZSIs are proposed for renewable energy resource applications. The family of ZSIs can be used where common ground is required, low current stress and low capacitor voltage stress are required. The detailed steady-state analysis of all the ZSIs are carried out. Detailed comparative analysis, components design, simulation verification, PCB design, digital control of ZSIs, comparative analysis and verifications are carried out. The steady-state analysis and verification are good match with each other.

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APPENDIX

1. ePWM Submodules

Seven submodules are included in every ePWM peripheral. Each of these submodules performs specific tasks that can be configured by software. The sub module configuration parameters are given below.

Submodule	Configuration Parameter
Time-base (TB)	<ul style="list-style-type: none"> • Scale the time-base clock (TBCLK) relative to the system clock (SYSCLKOUT). • Configure the PWM time-base counter (TBCTR) frequency or period. • Set the mode for the time-base counter: <ul style="list-style-type: none"> – count-up mode: used for asymmetric PWM – count-down mode: used for asymmetric PWM – count-up-and-down mode: used for symmetric PWM • Configure the time-base phase relative to another ePWM module. • Synchronize the time-base counter between modules through hardware or software. • Configure the direction (up or down) of the time-base counter after a synchronization event. • Configure how the time-base counter will behave when an emulator halts the device. • Specify the source for the synchronization output of the ePWM module: <ul style="list-style-type: none"> – Synchronization input signal – Time-base counter equal to zero – Time-base counter equal to counter-compare B (CMPB) – No output synchronization signal generated.
Counter – Compare (CC)	<ul style="list-style-type: none"> • Specify the PWM duty cycle for output EPWMxA and/or output EPWMxB. • Specify the time at which switching events occur on the EPWMxA or EPWMxB output.
Action - qualifier (AQ)	<ul style="list-style-type: none"> • Specify the type of action taken when a time-base or counter-compare submodule event occurs: <ul style="list-style-type: none"> – No action taken – Output EPWMxA and/or EPWMxB switched high – Output EPWMxA and/or EPWMxB switched low – Output EPWMxA and/or EPWMxB toggled
Dead – band (DB)	<ul style="list-style-type: none"> • Control of traditional complementary dead-band relationship between upper and lower switches • Specify the output rising-edge-delay value • Specify the output falling-edge delay value

	<ul style="list-style-type: none"> Bypass the dead-band module entirely. In this case, the PWM waveform is passed through without modification.
PWM – chopper (PC)	<ul style="list-style-type: none"> Create a chopping (carrier) frequency. Pulse width of the first pulse in the chopped pulse train. Duty cycle of the second and subsequent pulses. Bypass the PWM-chopper module entirely. In this case, the PWM waveform is passed through without modification.
Trip – zone (TZ)	<ul style="list-style-type: none"> Configure the ePWM module to react to one, all, or none of the trip-zone pins . Specify the tripping action taken when a fault occurs: <ul style="list-style-type: none"> Force EPWMxA and/or EPWMxB high Force EPWMxA and/or EPWMxB low Force EPWMxA and/or EPWMxB to a high-impedance state Configure EPWMxA and/or EPWMxB to ignore any trip condition. Configure how often the ePWM will react to each trip-zone pins <ul style="list-style-type: none"> One-shot Cycle-by-cycle Enable the trip-zone to initiate an interrupt. Bypass the trip-zone module entirely.
Event – Trigger (ET)	<ul style="list-style-type: none"> Enable the ePWM events that will trigger an interrupt. Enable ePWM events that will trigger an ADC start-of-conversion event. Specify the rate at which events cause triggers (every occurrence or every second or third occurrence) Poll, set, or clear event flags

2. Definitions used in the Code examples.

```

// TBCTL (Time-Base Control)
// =====
// TBCTR MODE bits
#define TB_COUNT_UP          0x0
#define TB_COUNT_DOWN         0x1
#define TB_COUNT_UPDOWN       0x2
#define TB_FREEZE             0x3
// PHSEN bit
#define TB_DISABLE            0x0
#define TB_ENABLE              0x1
// PRDLD bit
#define TB_SHADOW              0x0
#define TB_IMMEDIATE           0x1
// SYNCSEL bits
#define TB_SYNC_IN              0x0
#define TB_CTR_ZERO             0x1
#define TB_CTR_CMPB             0x2
#define TB_SYNC_DISABLE          0x3
// HSPCLKDIV and CLKDIV bits
#define TB_DIV1                0x0
#define TB_DIV2                0x1
#define TB_DIV4                0x2
// PHSDIR bit
#define TB_DOWN                 0x0
#define TB_UP                  0x1
// CMPCTL (Compare Control)
// =====
// LOADAMODE and LOADBMODE bits
#define CC_CTR_ZERO             0x0
#define CC_CTR_PRD               0x1
#define CC_CTR_ZERO_PRD          0x2
#define CC_LD_DISABLE            0x3

```

```
// SHDWAMODE and SHDWBMODE bits  
  
#define CC_SHADOW 0x0  
#define CC_IMMEDIATE 0x1  
  
// AQCTLA and AQCTLB (Action-qualifier Control)  
===== //  
  
// ZRO, PRD, CAU, CAD, CBU, CBD bits  
  
#define AQ_NO_ACTION 0x0  
#define AQ_CLEAR 0x1  
#define AQ_SET 0x2  
#define AQ_TOGGLE 0x3  
  
// DBCTL (Dead-Band Control)  
===== //  
  
// MODE bits  
  
#define DB_DISABLE 0x0  
#define DBA_ENABLE 0x1  
#define DBB_ENABLE 0x2  
#define DB_FULL_ENABLE 0x3  
  
// POLSEL bits  
  
#define DB_ACTV_HI 0x0  
#define DB_ACTV_LOC 0x1  
#define DB_ACTV_HIC 0x2  
#define DB_ACTV_LO 0x3  
  
// PCCTL (chopper control)  
===== //  
  
// CHPEN bit  
  
#define CHP_ENABLE 0x0  
#define CHP_DISABLE 0x1  
  
// CHPFREQ bits  
  
#define CHP_DIV1 0x0  
#define CHP_DIV2 0x1  
#define CHP_DIV3 0x2  
#define CHP_DIV4 0x3  
#define CHP_DIV5 0x4  
#define CHP_DIV6 0x5
```

```
#define CHP_DIV7          0x6
#define CHP_DIV8          0x7
// CHPDUTY bits
#define CHP1_8TH          0x0
#define CHP2_8TH          0x1
#define CHP3_8TH          0x2
#define CHP4_8TH          0x3
#define CHP5_8TH          0x4
#define CHP6_8TH          0x5
#define CHP7_8TH          0x6
// TZSEL (Trip-zone Select)
// =====
// CBCn and OSHTn bits
#define TZ_ENABLE          0x0
#define TZ_DISABLE         0x1
// TZCTL (Trip-zone Control)
// =====
// TZA and TZB bits
#define TZ_HIZ             0x0
#define TZ_FORCE_HI        0x1
#define TZ_FORCE_LO        0x2
#define TZ_DISABLE         0x3
// ETSEL (Event-trigger Select)
// =====
// INTSEL, SOCASEL, SOCBSEL bits
#define ET_CTR_ZERO        0x1
#define ET_CTR_PRD         0x2
#define ET_CTRU_CMPA        0x4
#define ET_CTRD_CMPA        0x5
#define ET_CTRU_CMPPB       0x6
#define ET_CTRD_CMPPB       0x7
```

```
// ETPS (Event-trigger Prescale)  
// =====  
// INTPRD, SOCAPRD, SOCBPRD bits  
  
#define ET_DISABLE          0x0  
#define ET_1ST               0x1  
#define ET_2ND               0x2  
#define ET_3RD               0x3
```
