Measuring small differential-mode voltages with high common-mode voltages and fast transients – Application to gate drivers for wide band-gap switches

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***Abstract*—In power electronics, gate-voltage measurement is used to optimize the design of the gate driver. Therefore a proper measurement technique is vital to ensure the proper operation of the electronic device. Measuring a small signal in a high switching voltage environment is a complicated task especially for high-side switches in a half-bridge configuration with fast semiconductor devices where voltage probes are subject to high common-mode voltages with fast transients. Hence, this article compares experimentally the conventional differential probes with optically isolated probes for measuring a small signal (26V) with a 1200V common-mode voltage and high switching rates created by SiC MOSFET (30kV/μs). The conventional differential probe shows differences of measured voltage amplitude up to 10V compared to optically isolated probe. The experimental results prove that parasitic elements of conventional differential probes change the gate-voltage shape and increase the common-mode current in the experimental set-up up to 6dB.**

***Index Terms*—Common-mode voltage, Wide band-gap semiconductors, Half-bridge, Silicon carbide, SiC MOSFET, Isolated-probe, Differential probe, Gate-driver.**

I. Introduction

Power electronic converters play an important role in energy industry nowadays [1]. Most power converter technologies consist of multiple power semiconductors arranged as a pair of switches in a half-bridge configuration. In the operation of the half-bridge configuration, the high-side and low-side devices are switched complementary with appropriate dead time. The fast switching is a solution to decrease the losses in power converters [2], but it faced challenges due to fast variation of the voltage in the mid-point of the half-bridge [3], [4]. SiC technology involves semiconductor material with a larger band-gap energy compared to Si which allows to build devices which are able to block higher voltages. Moreover, SiC semiconductors are shown with lower on-resistance in conduction mode which allows faster switching [5], [6]. To fully benefit from the mentioned advantages of the half-bridge configuration of semiconductors, the gate driver circuit and layout should be properly designed and optimized which depends directly on proper measurement. The challenge in front of this goal is that the mid-point of half-bridge is varying rapidly between $0V$ to the DC source voltage (in this work $dv/dt = 30kV/\mu s$). Most of the measurement equipment are affected by this big common-mode (CM) voltage. The ability of the measurement equipment to withstand this CM voltage without transferring it into a perturbation for the output signal is called CM rejection ratio (CMRR). The CMRR of measurement equipment is generally degraded at high frequency whereas the increase of switching speeds is a trend in power electronic. Therefore, using maximum switching speed increases the risk of losing important information due to limitation of the measurement equipment. Moreover, the optimized design will be compromised because it will be based on incorrect measurement results. In this work, it is targeted to show the importance of the measurement in the design of the gate driver due to the specificity of the power converter. Considering all the aforementioned importance of measurement, the effect of the measurement technique is targeted to be studied in this work. Measurement challenges in gate-source voltage include: measuring small signals ($26V$)

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in the presence of fast variation of a high CM voltage (here $dv/dt = 30kV/\mu s$), measuring the gate perturbation due to the complementary switching effect and gate signal oscillation due to the parasitic inductance in the layout of the converter [6]. So as, this work is arranged as follows. Section II, introduces the experimental test-bench used to examine the measurement techniques, section III explains differential probes operation to carry out floating measurement, finally the effect of the measurement tools and assessing how they can disturbs the set-up and cause errors in the design of power electronic device will be shown in section IV. The paper will be finished by section V as a conclusion.

II. Experimental setup

Here to illustrate what is happening during switching transition of the half-bridge configuration and gate-source measurement, the half-bridge 1.7kV SiC MOSFET (CAS300M17BM2) has been examined in a synchronous operation with double pulse method (see Fig. 1). The two switches are controlled by half-bridge gate driver (see Fig. 2) respecting proper dead-time (see Fig. 3). During switching transition of the half-bridge, the mid-point current in the inductor can be either in positive or negative direction. In positive direction the low side switch is controlled and the current, during dead-time, flows through the body diode of the high-side switch. In negative direction while the high-side switch is controlled, during dead-time the current is passing through the body diode of the low-side switch. Gate-source voltage of high-side switch has been experimentally evaluated with two different directions of the current in inductor (see Fig. 3). In order to illustrate how much the system is under influence of the measurement devices, it has been tested in different situations : with conventional differential probe, with conventional differential probe and isolated probe and at the end, the conventional probe has been removed and the test has been reproduced only with presence of isolated probe.

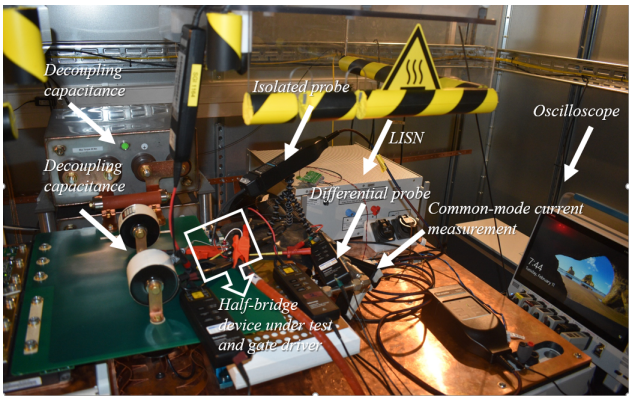

Fig. 1. Experimental setup

III. Theory of operation and problem statement

A. Conventional differential probe

The state of the art of differential measurement technologies for floating signal measurement (both measurement points

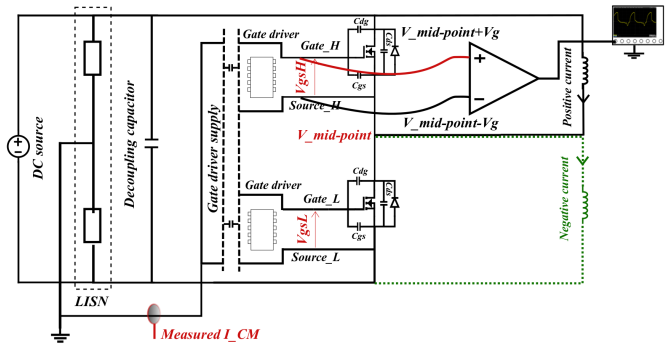

Fig. 2. Synchronous converter, double pulse test schematic.

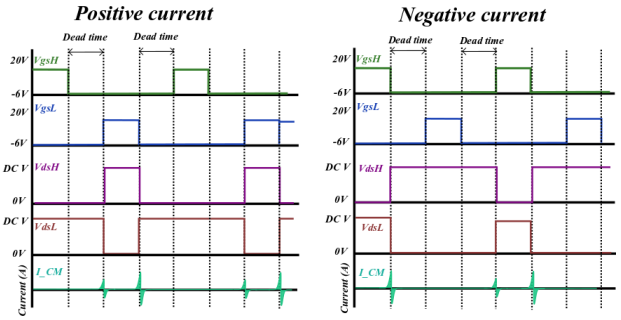

Fig. 3. Operation of a synchronous converter in different current direction.

are without ground reference), like gate-source voltage of the high-side switch in phase-leg, is conventional differential probe. In theory it consists of two well-matched input voltage dividers linked to a differential amplifier to produce output signal as an image of the measured signal. The ground referenced output signal of the differential amplifier as an indicator of the measured signal is the attenuated input signal [7]. With the differential probe technique, both of the differential inputs of the probe are high impedance (high resistance and low capacitance). With the balanced impedance of both probe tips and low capacitance inputs, floating measurement can be done without risk of loading the circuit under test. If the inputs of this amplifier are connected to the same source signal, it is expected to have a zero output. This signal is

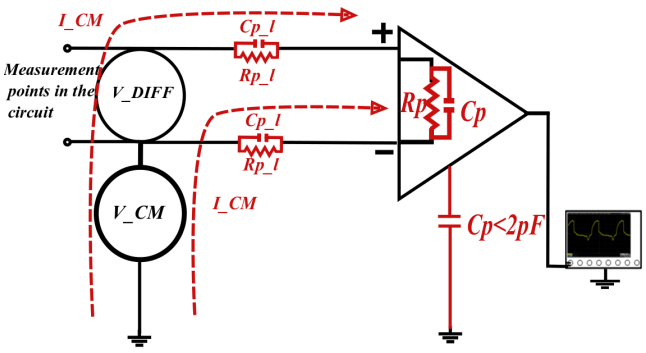

Fig. 4. Conventional differential probe

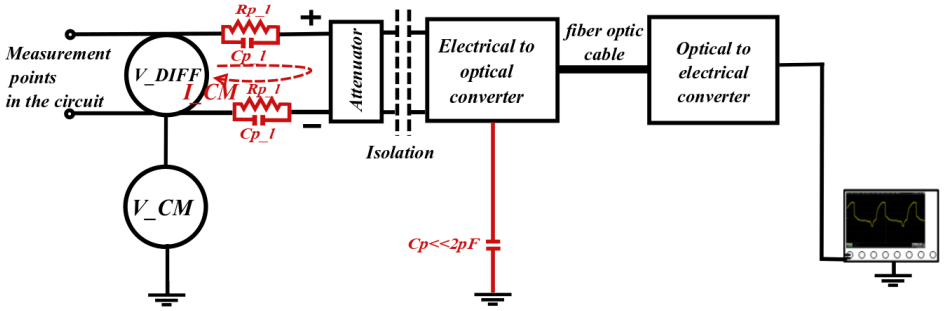

Fig. 5. Isolated differential probe

called CM signal. An ideal differential amplifier would reject 100% of the CM signal that is how the output would be zero. However, in practice it is very difficult to provide these balanced inputs impedances for differential probes and the probe fails to provide a good representation of the actual measured signal [8] in high voltage switching environment. The limitation of the probe is due to the imposed effect of the CM voltage (mid-point voltage in the Fig.2). During gate-source voltage measurements, the differential amplifier of the differential probe is subject to the mid-point voltage in addition of the measured signal. The CMRR of the measurement device is degraded at high frequency. This frequency is related to the maximum rise time of the signal not the switching frequency. So in high switching speed of high voltage semiconductor, the measurement is affected by this factor. Another factor that limits the ability of the differential probe is the effect of the long input leads of the probe. These limitations are more remarkable when testing power devices with fast switching under high voltage and consequently high CM voltage [9].

B. Isolated differential probe

The input stage of isolated probes is a voltage divider (similar to conventional differential probe) with much higher impedance (up to 10^3 times more) in comparison with conventional differential probe (Fig. 5) [10]. Moreover, in order to reach the minimum parasitic capacitance, all the connections of the probe terminals are locally shielded. The sensor head of the device provides an interface to change the measured data (electrical) to optical signal thanks to the electronic to optic converter. In addition, the electrical-to-optic and optic-to-electrical converter provide an optical isolation of the device under test from the oscilloscope. A fibre optic cable carries the information of the measured signal (instead of an electrical cable) which reduces the effect of the lead parasitic of the probe to almost zero. Conceptually, the electric-to-optic converter senses and sends the signal without involving the error of the unbalanced input of differential amplifier. That is how it can remove the effect of the superimposed CM voltage rejection of the differential amplifier [10].

IV. Experimental results

The VgsH (see Fig. 3) with t_{rise} equal to $70ns$ is measured where the mid-point voltage of the half-bridge configuration is changing between from $0V$ to the supply voltage ($1200V$) in maximum switching rate ($30kV/\mu$) of the SiC MOSFET (external gate resistance of gate driver $= 0.2\Omega$). The differential probe [9], isolated probe [10] and an oscilloscope with a maximum 2GHz bandwidth are used to be sure that the bandwidth of the measurement equipments (eq. (1)) are 5 times bigger than the measured signal bandwidth (eq. (2)) [11].

$$BW_{-3dB} = 1/\sqrt{1/BW^2_{-3dB,scope} + 1/BW^2_{-3dB,Probe}} \quad (1)$$

$$BW_{GHz} = 0.35/T_{rise}(nsec) \quad (2)$$

The comparison has been done by measuring the VgsH where the CMRR ability of the probes should be able to reject $1200V$ from $5MHz$ (measured signal frequency bandwidth). The conventional differential probe data sheet provides the information of CMRR between $3.2MHz$ to $100MHz$ equal to $30dB$ and $26dB$ respectively (see Table. I). Thanks to Eq .3, it can be expected to have an error between $20V$ to $37V$. The same calculation can be done for the isolated probe with the ability of the CMRR from $160dB$ at $1MHz$ to $80dB$ at $1GHz$ which concludes to expect an error between $12\mu V$ to $120mV$ (see Table. I). The measurement system needs to accurately resolve the $26V$ differential voltage with CMRR ability of the measurement device. Therefore, the error due to the conventional differential probe is not negligible. Moreover, for gate-source measurement, it is important to minimize the effect of the input capacitance of probes and ground lead length. The small connectors of the isolated probe, could overcome the problem thanks to completely solid metal body of the connectors [10].

$$CMRR = 20 \times log10(V2/V1)(dB) \quad (3)$$

Figures 6 and 7 depict the experimental comparison with both voltage probes. The effect of the low CMRR of the conventional differential probe and the reaction of the lead's parasitic impedance to high CM voltage can be seen through the differences in amplitude (around 10V) and frequency of oscillations.

Following the investigation on the reaction of two different technologies of differential probes, the input CM current of the

TABLE I
DIFFERENTIAL PROBES SPECIFICATION [9], [10].

	TMDP0200	**IsoVu TIVM series**
Bandwidth	200MHz	1GHz
Common Mode Voltage Range	±750 V	60 kV
Rise time	<1.8 ns	<350 ps
Cable length	1.5 m	3 m
Typical CMRR	DC:>-80dB 100kHz:>-60dB 3.2MHz:>-30dB 100MHz:>-26dB	DC-1MHz:>160dB 1MHz-100MHz:120dB 1GHz:80dB

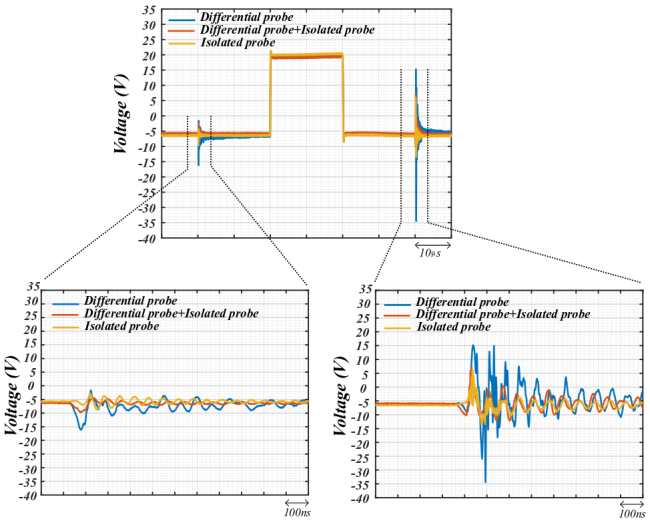

Fig. 6. Experimental comparison of conventional differential probe and isolated probe, VgsH, positive current, in 1200V, 150A double pulse test.

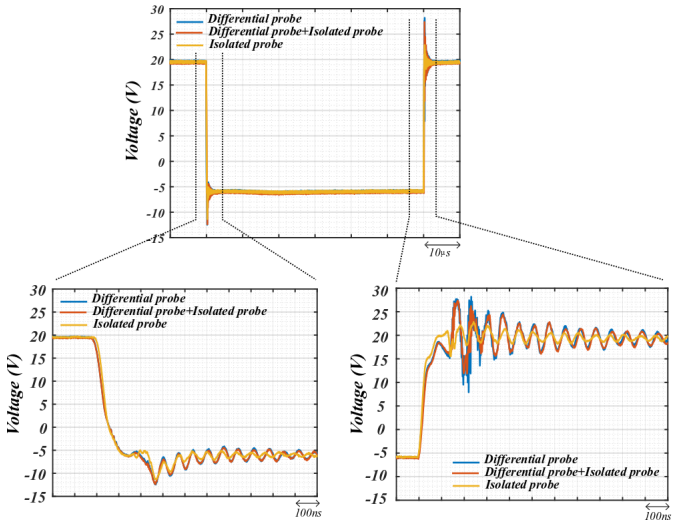

Fig. 7. Experimental comparison of conventional differential probe and isolated probe, VgsH, negative current, in 1200V, 150A double pulse test.

gate driver (measurement point is shown in Fig. 2) has been measured during the voltage variation across the switches. The goal is to show the impact of the different isolation of the two differential probes in producing wrong measurement data and how the parasitic elements of the voltage measurement as a path for the CM current change the measurement results. The new technology of the isolated differential probes increases the impedance of the input lead [10] while the value of the parasitic capacitance is very small compared to conventional one [8]. Moreover, optical isolated supply of the isolated probe prevents offering a path to the CM current into the circuit under test and measurement equipments. The earth connected measurement [7] of the CM current (I_{CM}) of the gate driver power supply has been done for two probes under 1200VDC. Experimental results showed (Fig. 8) how parasitic capacitance provides a path for the CM current, while optical isolation of the isolated probe outperforms the conventional differential probe up to 6dB.

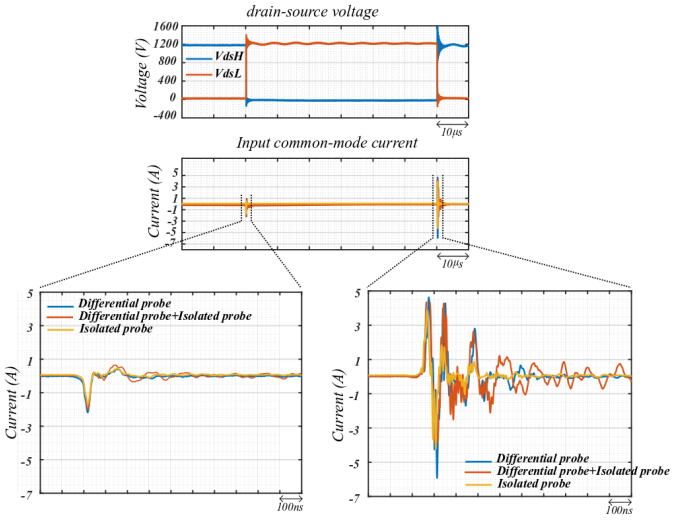

Fig. 8. Experimental comparison conventional differential probe and isolated probe, Common-mode current of gate driver, in 1200V, 150A double pulse test.

V. CONCLUSION

Gate-source voltage of power semiconductor should be measured properly due to its significant effect on converter efficiency and stability. In circuits such as a half-bridge, where large common-mode mode voltages and fast edge rates occur, small amplitude signals such as the gate-source voltage are very difficult to be measured accurately without superior common-mode rejection ratio. Due to the parasitic elements of the conventional differential probe, there is a risk of measurement errors and also unexpected loading of the circuit under test in fast switching power electronic converters. High input impedance and low parasitic capacitance of the isolated probes are important parameters for high voltage phase-leg configuration measurement specification. New technology of differential isolated probe provides this characteristic. Measuring the common-mode current of the gate driver validated

the necessity of using the new optical technology of the differential measurement equipment.

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