॥ सा विद्या या विमुक्तये ॥

भारतीय प्रौद्योगिकी संस्थान धारवाड़

Indian Institute of Technology Dharwad

High Voltage Isolated Differential Probe

EE314: EDL Project

Team Members:

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Project Supervisor

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Project Timeline

A. First Evaluation

1. Study of existing solutions
2. Requirement Building / Spec freeze
3. High-level system Design by 27/Jan 2023

B. Second Evaluation

4. Simulation
5. Prototyping
6. PCB design by 17/Feb 2023

C. Third Evaluation

7. Prototyping and Assembling
8. Integration 17/March 2023

D. Final Evaluation

9. Testing and Calibration
10. Bugs and Fixing
11. Final PoC System Demonstration 10/April 2023

Presentation Outline

- Problem Statement
- Target Objective
- Wish Specifications
- Isolation Techniques
- Market Survey Details
- System Level Block Diagram
- Core Component
- Preliminary Design

Problem statement:

High Voltage Differential Probe

- Tektronix P5200A
- Too high bandwidth & voltage range for UG lab use

  100MHz, 1500V

  Cons:
- Imported
- Only works with MDO Series Tek DSOs (or needs adapters)
- Too expensive **₹4,00,000**

Wish specifications:

- Voltage Range: **0-600V**
- Impedance: **10MΩ**
- Bandwidth: **DC-5Mhz**
- Common Mode Rejection Ratio (CMRR): **> 65dB**
- Signal Noise Ratio (SNR): **> 65dB**
- Isolation Voltage Rating: **1000V**
- Input Connector: **Banana jack type**
- Output Connector: **BNC**
- Operating Temperature: **10°C to 50°C**
- Power Source: **External**

Current Probe:

- Tektronix A622
- Too expensive **₹ 1,50,000**
- Too high bandwidth for lab use **100kHz**
- Imported

Target objective:

- Replacement of P5200A Device at low budget at 35k.

Isolation Techniques

- **RF, fibre optic, isolation mechanisms.**
- **RF Isolation :** It is used to protect your RF components from excessive power reflection.
- **RF Isolator :** An RF isolator is a 2-port device that transmits microwave or radio frequency power in one direction only while blocking the signal in the opposite direction.
- **RF ISOLATION TECHNIQUES:**
  1)grounding techniques:

➢ It is used to have separate supplies for analog and digital sections of the chip to isolate the analog circuits from switching noise .

2)GUARD RINGS:

- current taken from a DC power source is properly isolated from the power source.
- The ring-guard isolation technique usually consists of three components: an insulating ring, a ground conductor, and a guard ring.

Pros:

Provide better isolation at lower frequencies

Cons:

At higher frequencies isolation becomes weak.

3)ON CHIP DECOUPLING:

- It improve signal integrity and reduce unwanted crosstalk between signals.
- The technique involves isolating the circuits or devices on the IC by using a dielectric material such as silicon dioxide (SiO2) or polyimide (PI)..

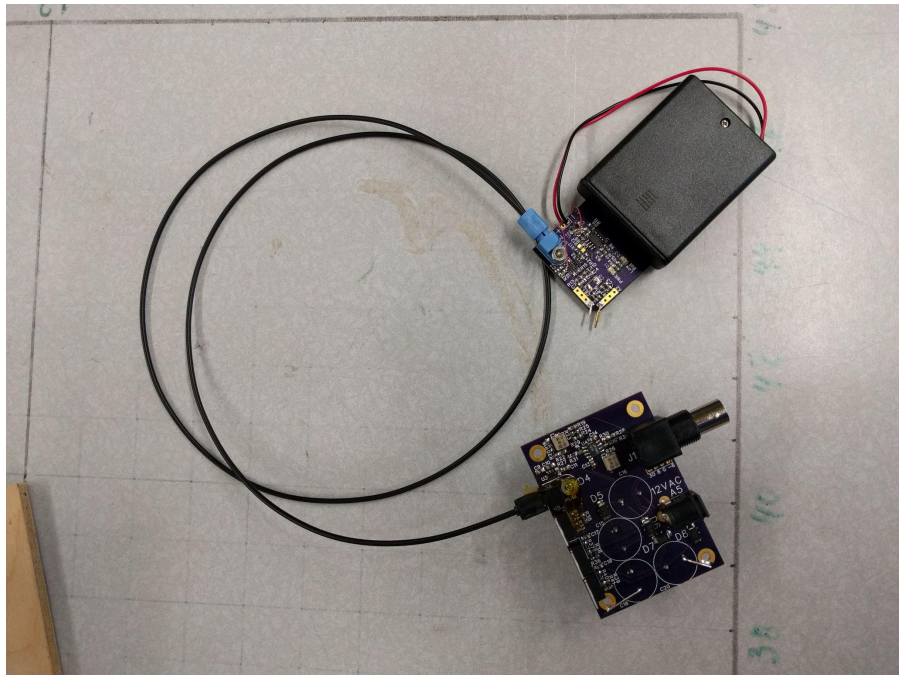
Optical isolation

Principle:

Uses a LED or laser diode as light source,directed into a single mode optical fiber,which travels and then incident on photo detector(photodiode),this generates electrical signal.

Cons:

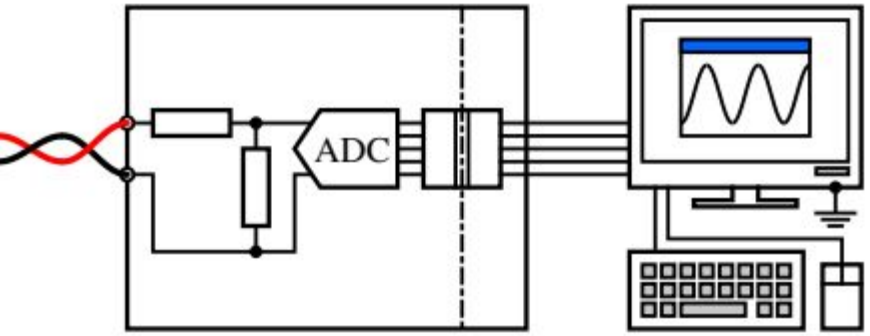
Low bandwidth,more delay,used in less input voltage,etc.



Fiber Optic isolated voltage probe

- 10x attenuation
- +-50V input voltage range
- used battery for power supply
- it is noisy

Market Survey:



(b) Digital isolated high voltage probe

A Digital Isolated High Voltage Probe

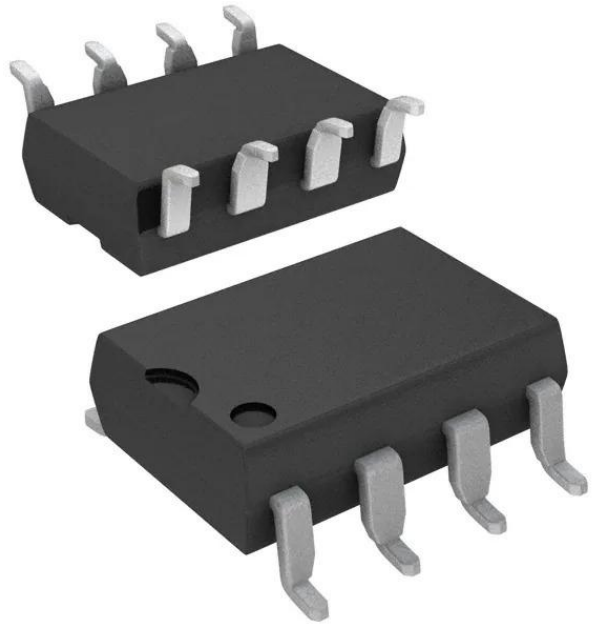
In this probe isolation is provided by converting analog signals to digital using ADC and then isolating the digital dta lines

High Voltage differential probe 25MHz , 400V input , same which we are targeting but not isolated.

Survey on isolated amplifiers

AMC1301QDWVQ1
Isolation Amplifiers Automotive Precision +/-250mV-Input , Reinforced Isolated Amplifier.

Price: ₹966.22



HCPL-7520-300E optoisolator. Which have ADC and DAC all built in, and basically only requires a power supply on each side. Although the bandwidth is only 100kHz.

COST $7

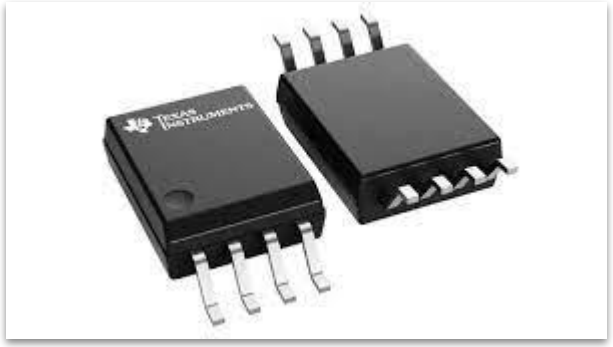
Core Component

(isolation amplifier)

AMC1301-Q1

- **This barrier is certified to provide reinforced galvanic isolation of up to 7 kV peak.**
- **Specs**

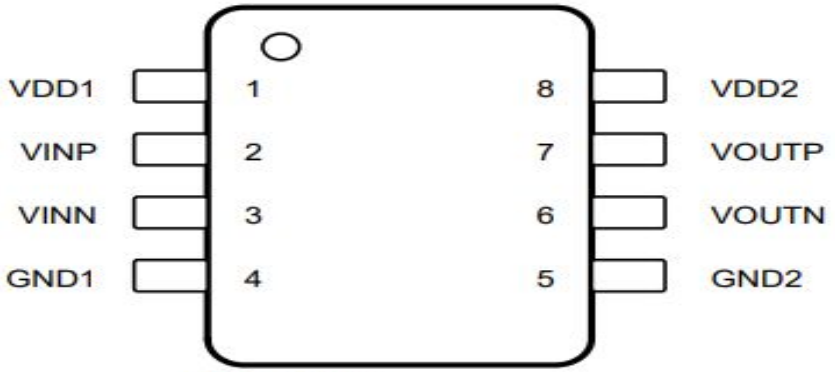
GBWP	—1000 kHz
CMRR	-— 92 dB
Operating Temperature	—(-40 to 125 c)
VDD	— (–0.3 to 7) V
Input Voltage Range	— (GND1 – 6) to (VDD+ 0.5)



AMC1301-Q1

5 Pin Configuration and Functions

DWV Package
8-Pin SOIC
Top View

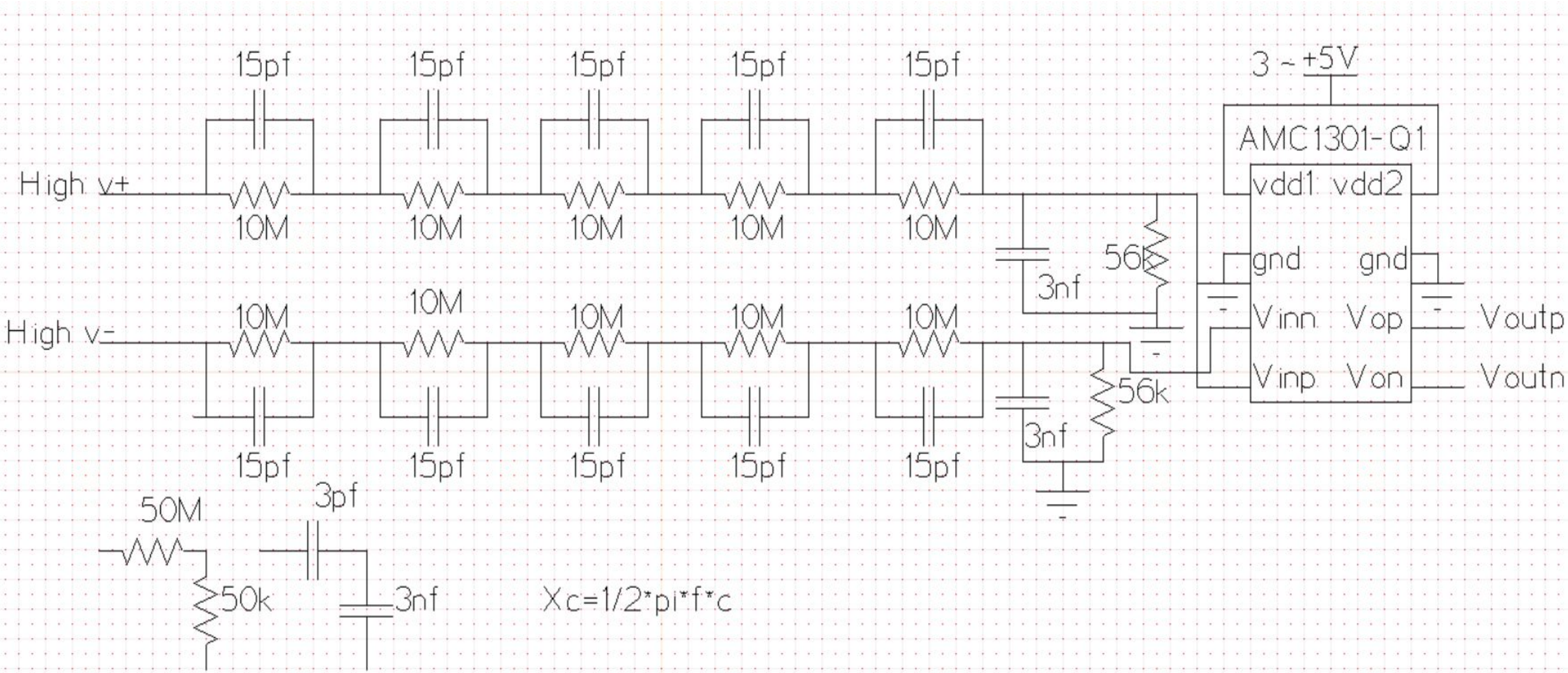


Not to scale

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
GND1	4	—	High-side analog ground
GND2	5	—	Low-side analog ground
VDD1	1	—	High-side power supply, 3.0 V to 5.5 V. See the *Power Supply Recommendations* section for decoupling recommendations.
VDD2	8	—	Low-side power supply, 3.0 V to 5.5 V. See the *Power Supply Recommendations* section for decoupling recommendations.
VINN	3	I	Inverting analog input
VINP	2	I	Noninverting analog input
VOUTN	6	O	Inverting analog output
VOUTP	7	O	Noninverting analog output

- **Rough Schematic of Circuit Diagram**

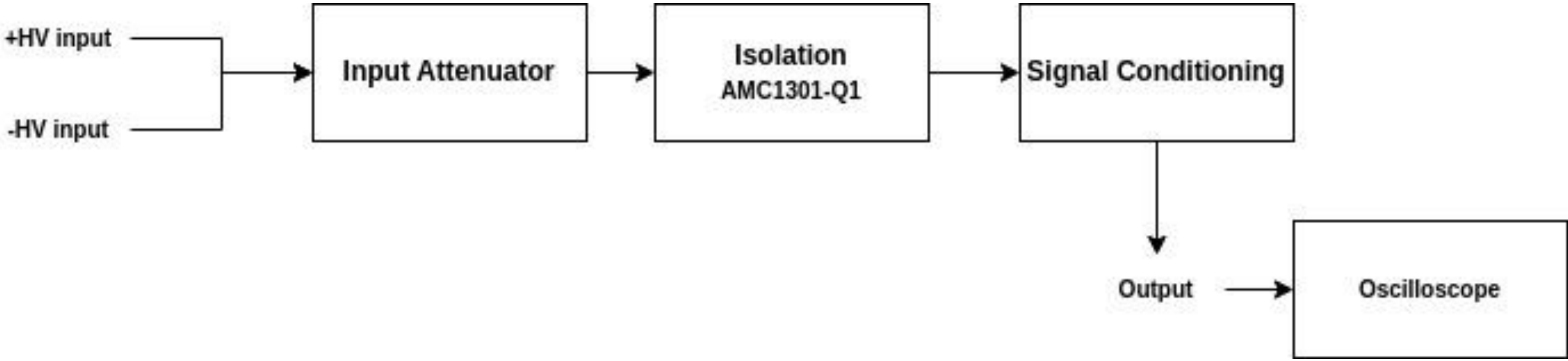


Future Work

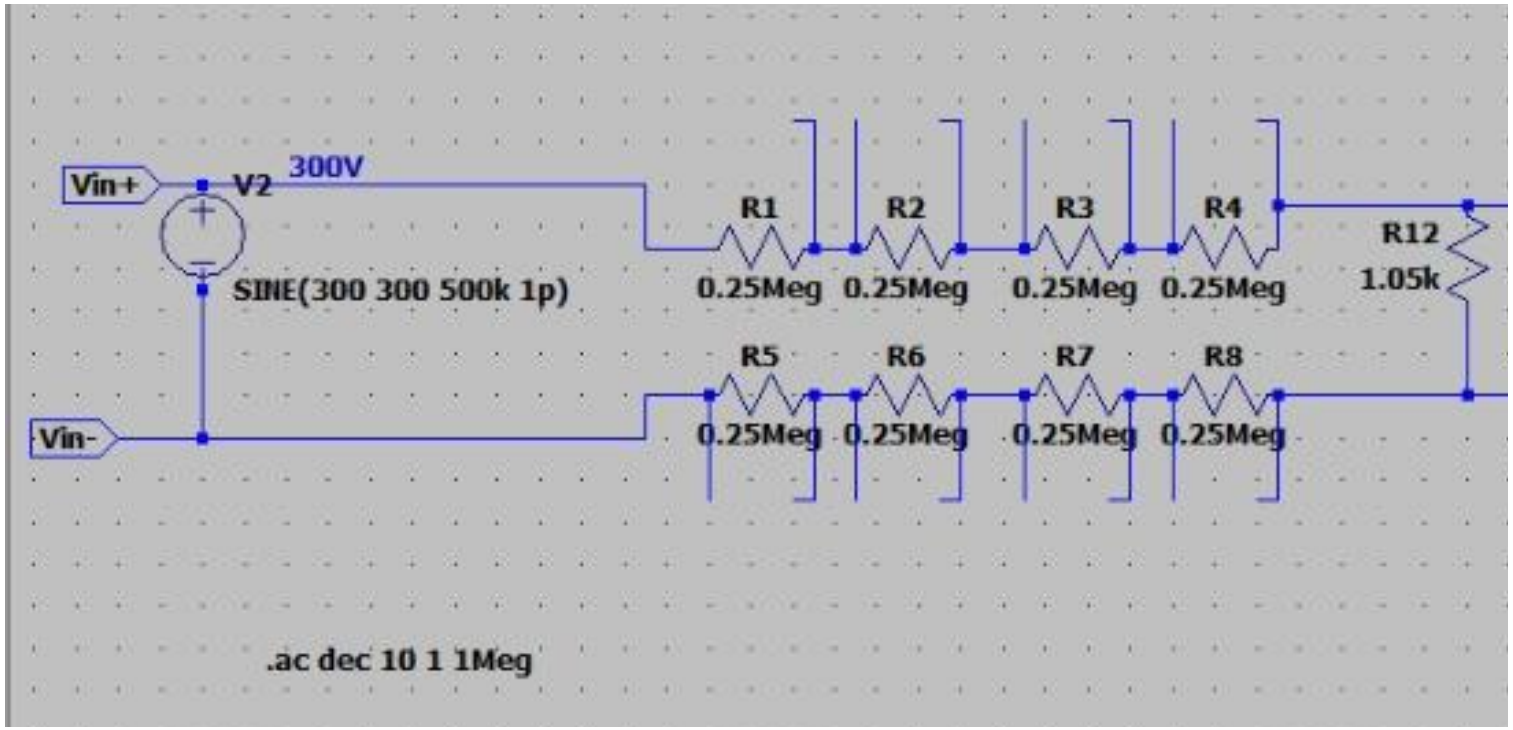
Second Evaluation

1. Simulation
2. Prototyping
3. PCB design by 17/Feb 2023

System Block diagram

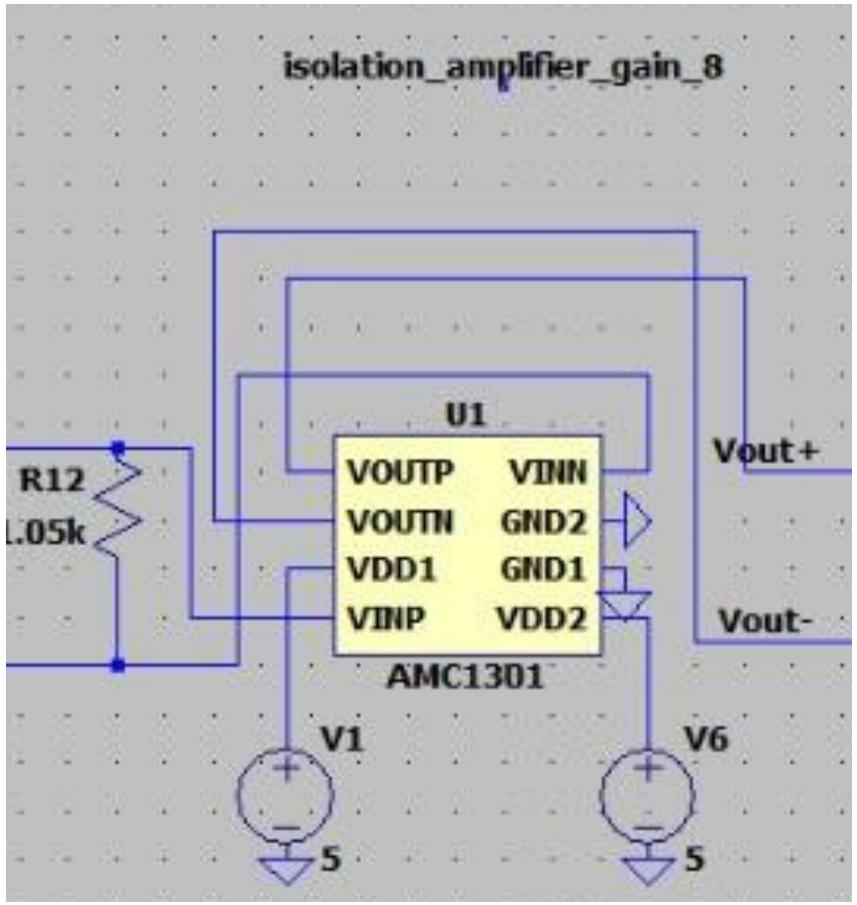


Input Attenuator Stage



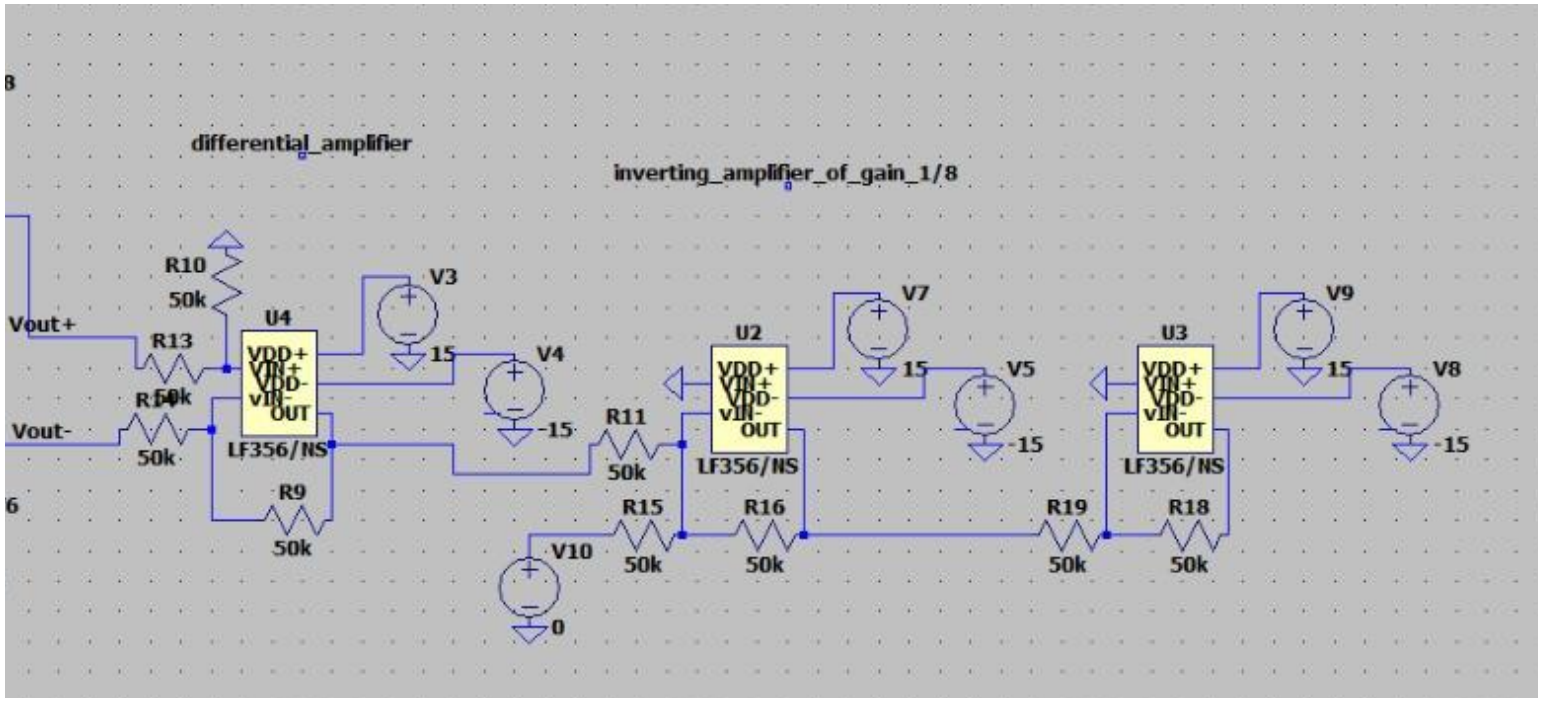
Attenuation: 1/2000

Isolated Amplifier Stage



Bandwidth: 1MHz
gain: 8
Vdd: -0.3 to 7V
Input voltage range : 330mV (calculated by simulations)

Signal Conditioning

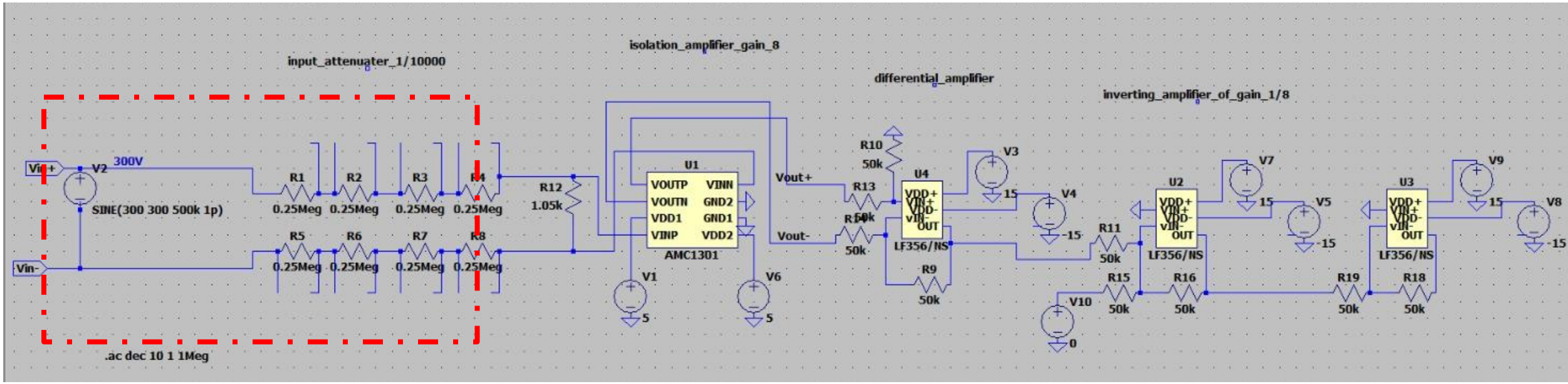


IC (LF356)
Differential amplifier : making output single ended
Inverting amplifier : used for trimming of gain and offset correction

Trimming Values Required for gain and offset correction

Frequency (Hz)	Gain (dB)	Trimming Values (Ohm)
1-10	-48.14	51075.(45892 to 45894)
10-100	-48.14	51075.(
100-1000	-48.14	
1000-10k	-48.14	
10k-100k	-48.15 - -48.71	
100k-1000k	-48.71 - -114.8	

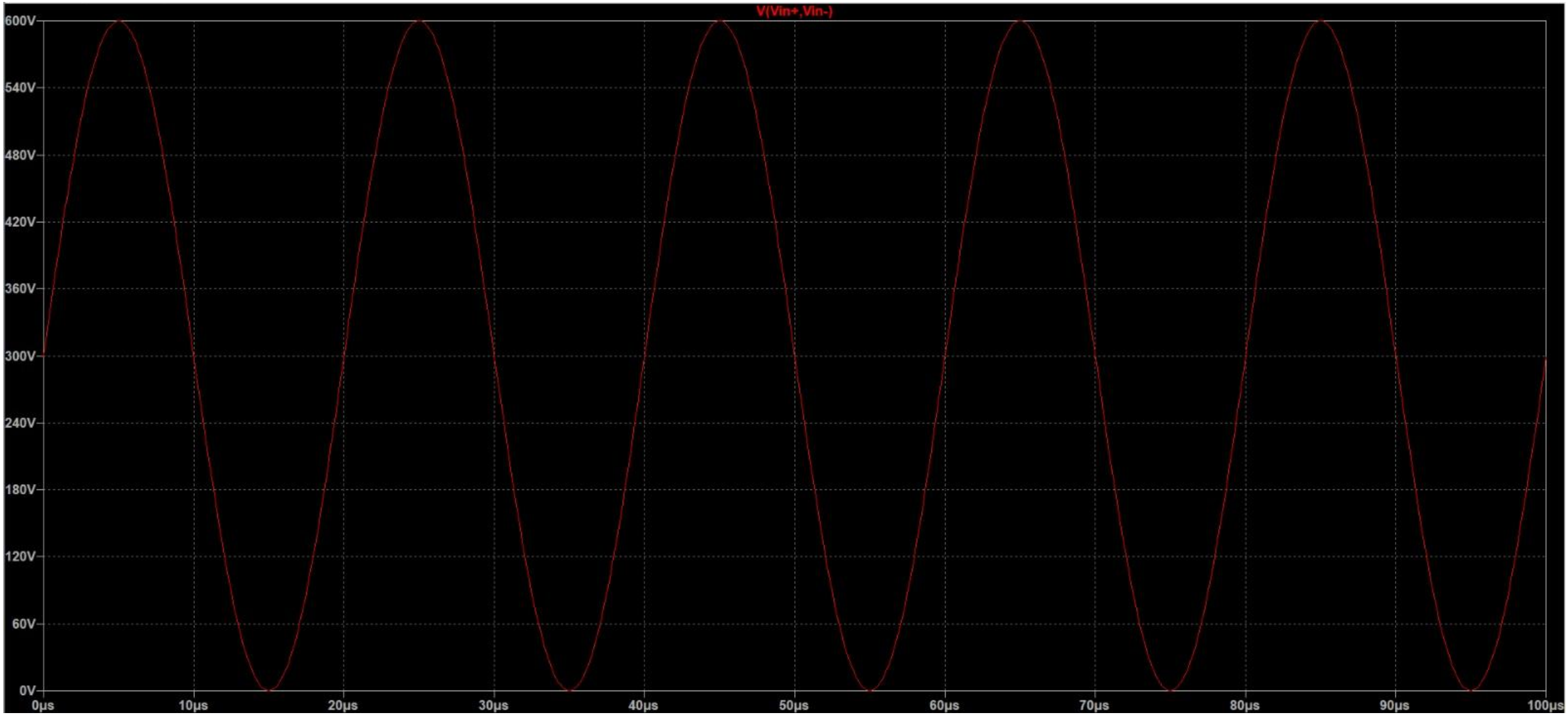
Circuit Schematic



Stages:

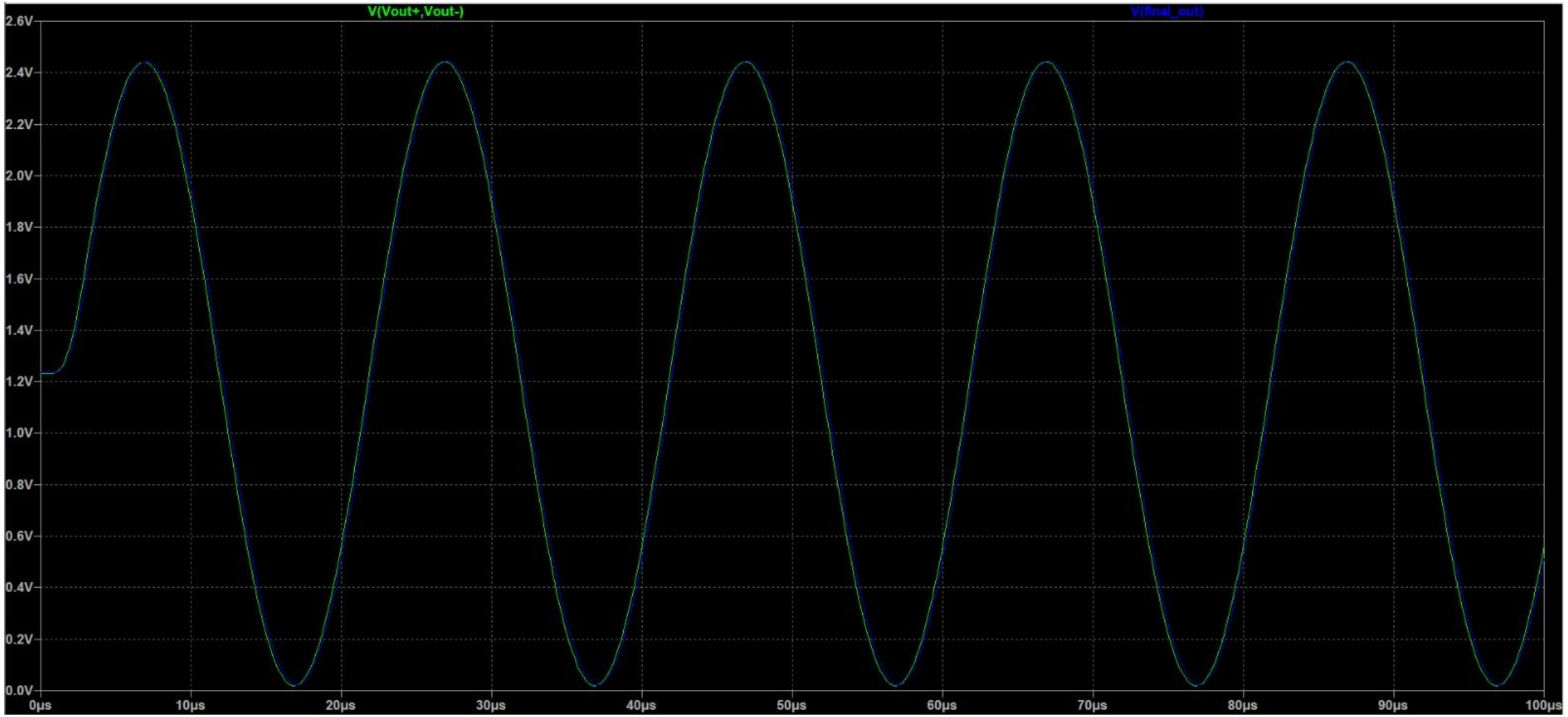
Input attenuator(voltage divider)
isolation amplifier (AMC1301 IC) (bandwidth=1000kHz)
differential amplifier
inverting amplifier (for gain correction)
inverting amplifier (for offset correction)

High Voltage Input plot (± 600V)

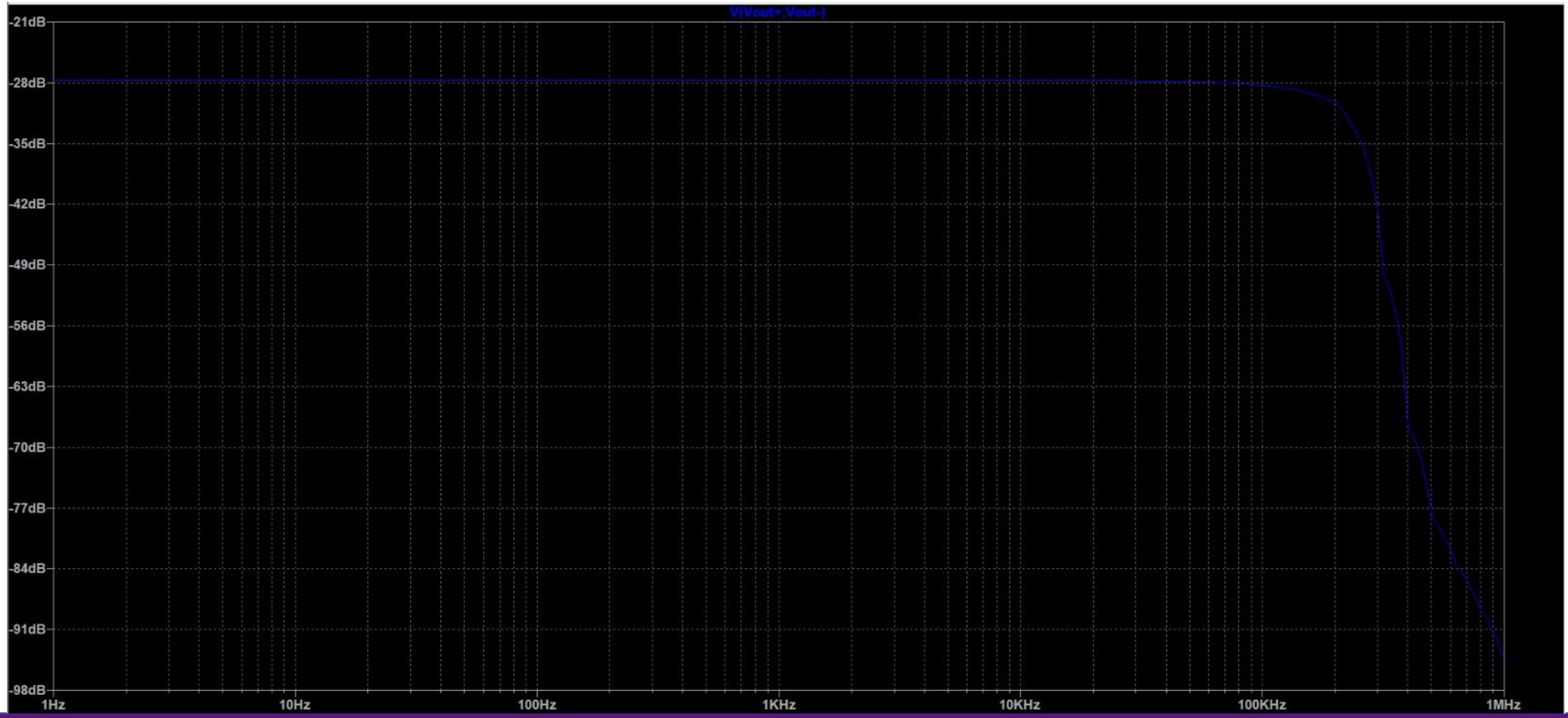


AC analysis Output after Isolated amplifier stage

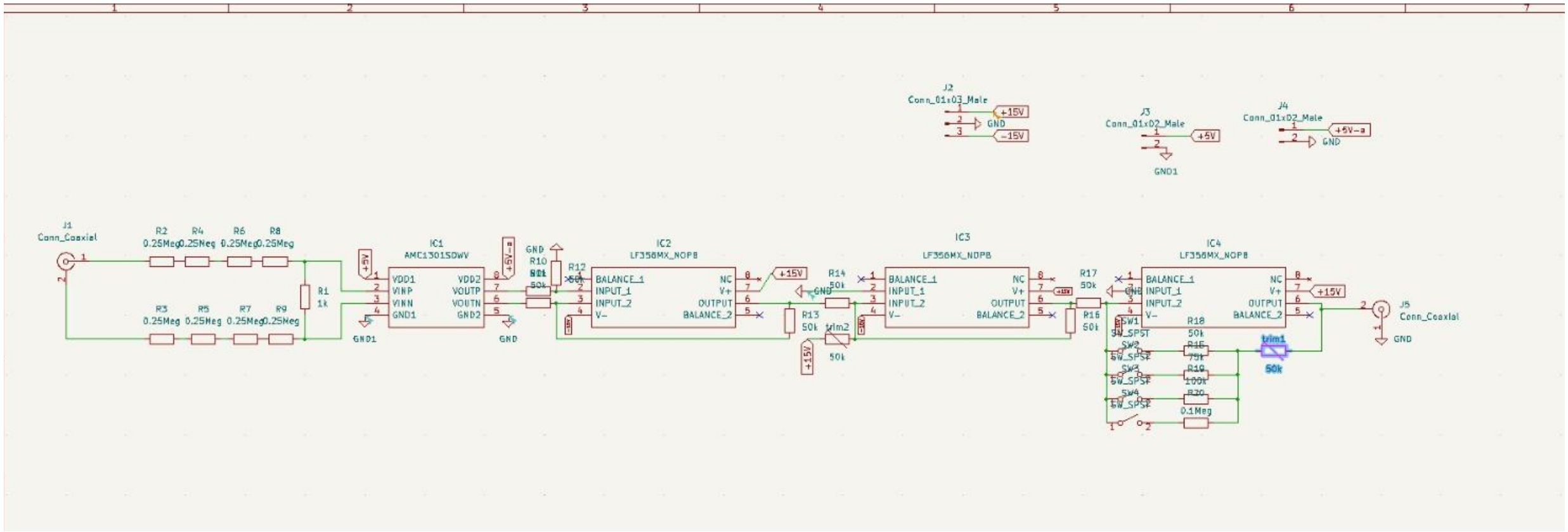
Output after differential amplifier vs output after Isolated amplifier



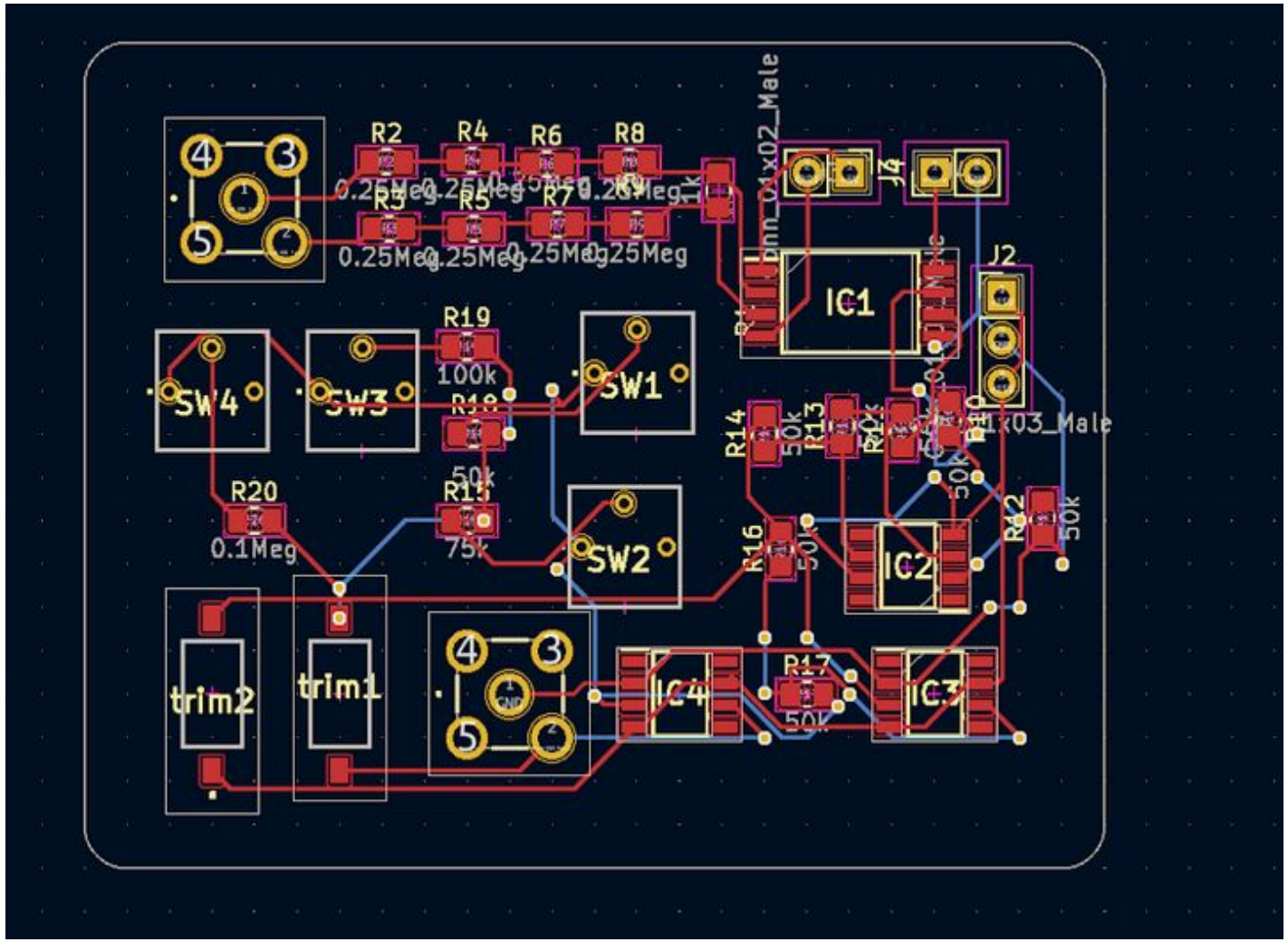
Transient analysis Output after Isolated amplifier stage



PCB schematic diagram



PCB Design


R2
R4
R6
R8
R3
R5
R7
0.25Meg
R19
100k
SW4
SW3
SW1
R18
50k
R20
0.1Meg
R15
75k
SW2
trim2
trim1
IC1
IC2
IC3
IC4
J2
J4
R14
R13
R12
R16
R17
50k

3D model of PCB Design