



॥ सा विद्या या विमुक्तये ॥

भारतीय प्रौद्योगिकी संस्थान धारवाड़

Indian Institute of Technology Dharwad

High Voltage Isolated Differential Probe

EE314: EDL Project Evaluation 3

Team Members:

Shashi prabha	200020043
Mouli Venkata Prakash	200020027
Devi Prasad	200020022

Project Supervisor

Prof. Dr.Abhijit Kshirsagar
Dept. of Electrical Engineering IIT Dharwad

Project Timeline

A. First Evaluation

1. Study of existing solutions
2. Requirement Building / Spec freeze
3. High-level system Design by 27/Jan 2023



B. Second Evaluation

4. Simulation
5. Prototyping
6. PCB design by 17/Feb 2023



C. Third Evaluation

7. Prototyping and Assembling
8. Integration 17/March 2023



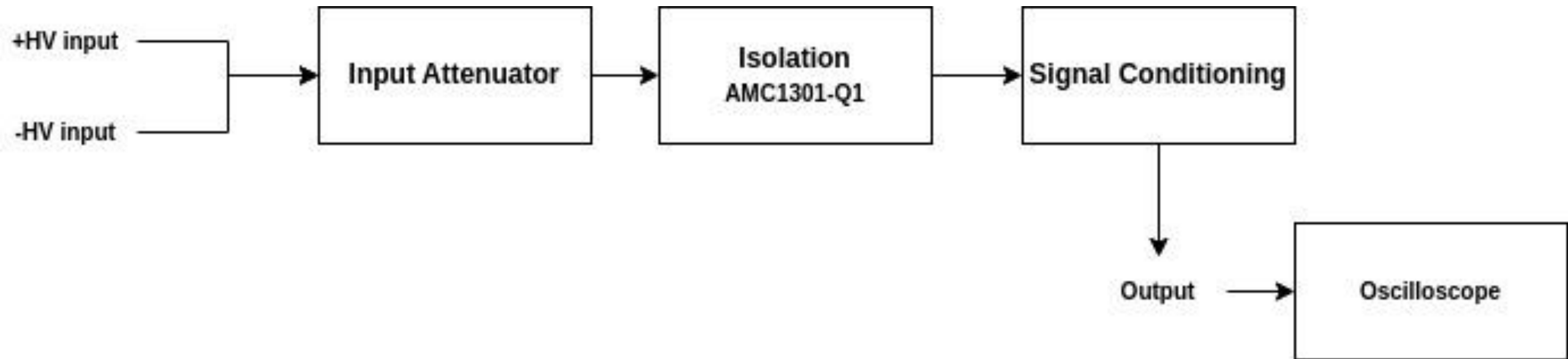
D. Final Evaluation

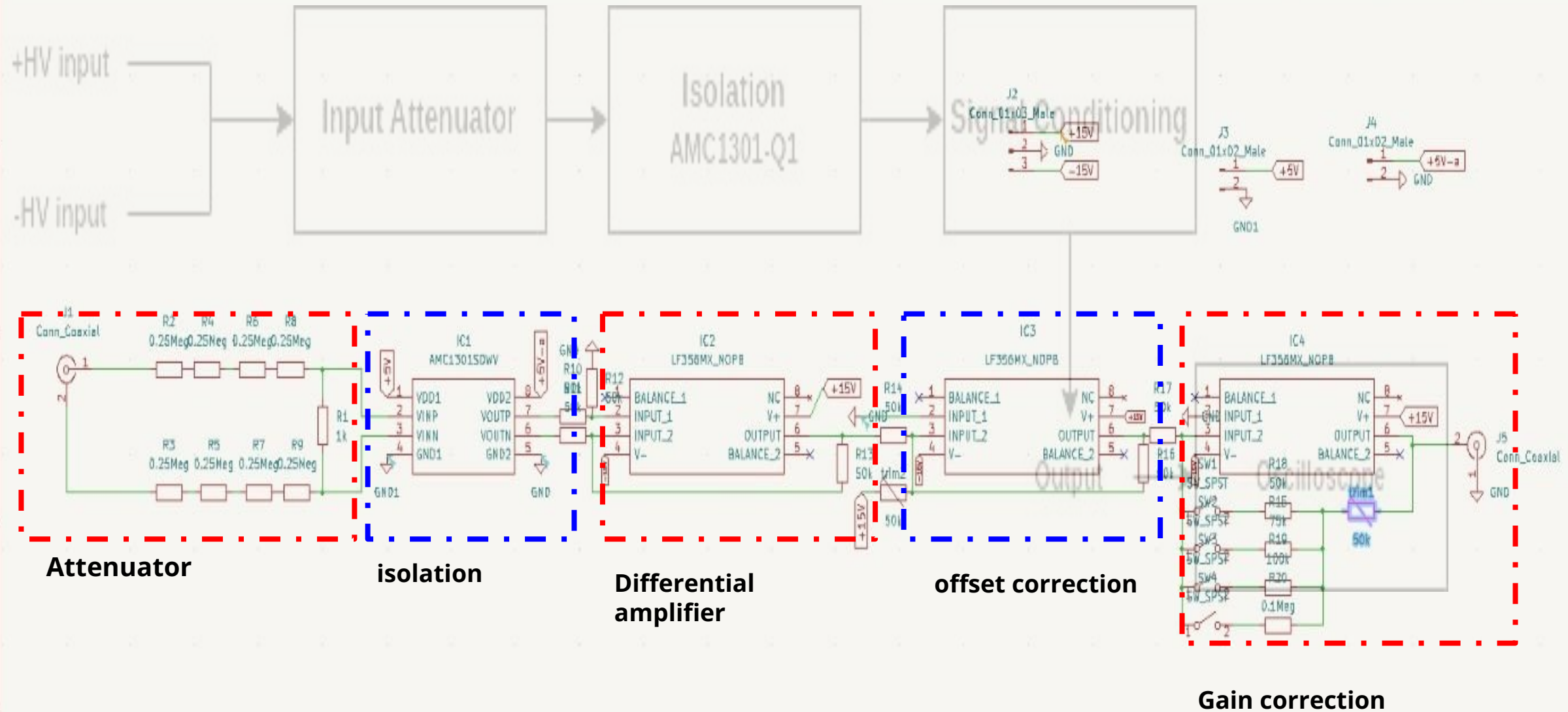
9. Testing and Calibration
10. Bugs and Fixing
11. Final PoC System Demonstration 10/April 2023

Wish specifications:

- Voltage Range: **0-600V**
- Impedance: **10M Ω**
- Bandwidth: **DC-5MHz**
- Common Mode Rejection Ratio (CMRR): **> 65dB**
- Signal Noise Ratio (SNR): **> 65dB**
- Isolation Voltage Rating: **1000V**
- Input Connector: **Banana jack type**
- Output Connector: **BNC**
- Operating Temperature: **10°C to 50°C**
- Power Source: **External**

System Block diagram





Test plan

	A	B	C	D
1		Dc	low frequency (linearity)	high frequency
2	Identify 3 power sources	✓		
3	Checking attenuator stage	✓	✓	✓
4	Checking isolated amplifier (gain,offset)	✓	✓	✓
5	check diffrential amplifier	✓	✓	✓
6	Checking Offset correction	✓		✓
7	at low voltage	✓	✓	✓
8	at moderate voltage	✓	✓	✓
9	at high voltage (60V max applied)	✓	✓	□
10	checking gain correction	✓	✓	✓

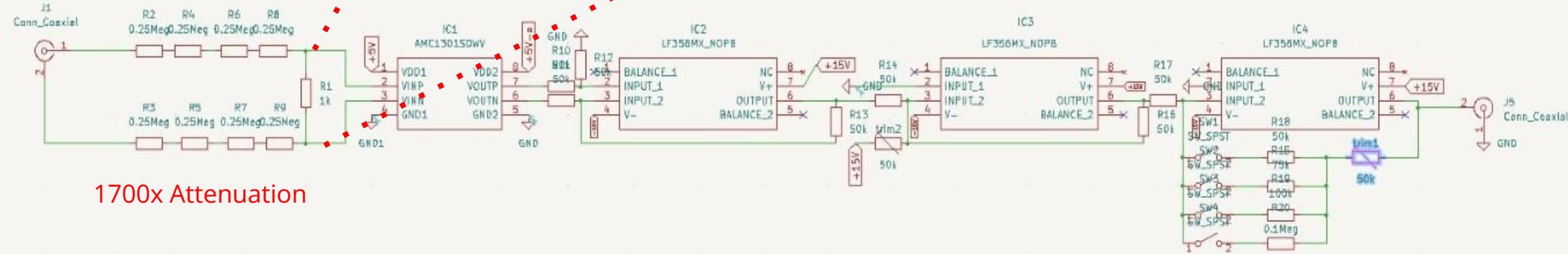
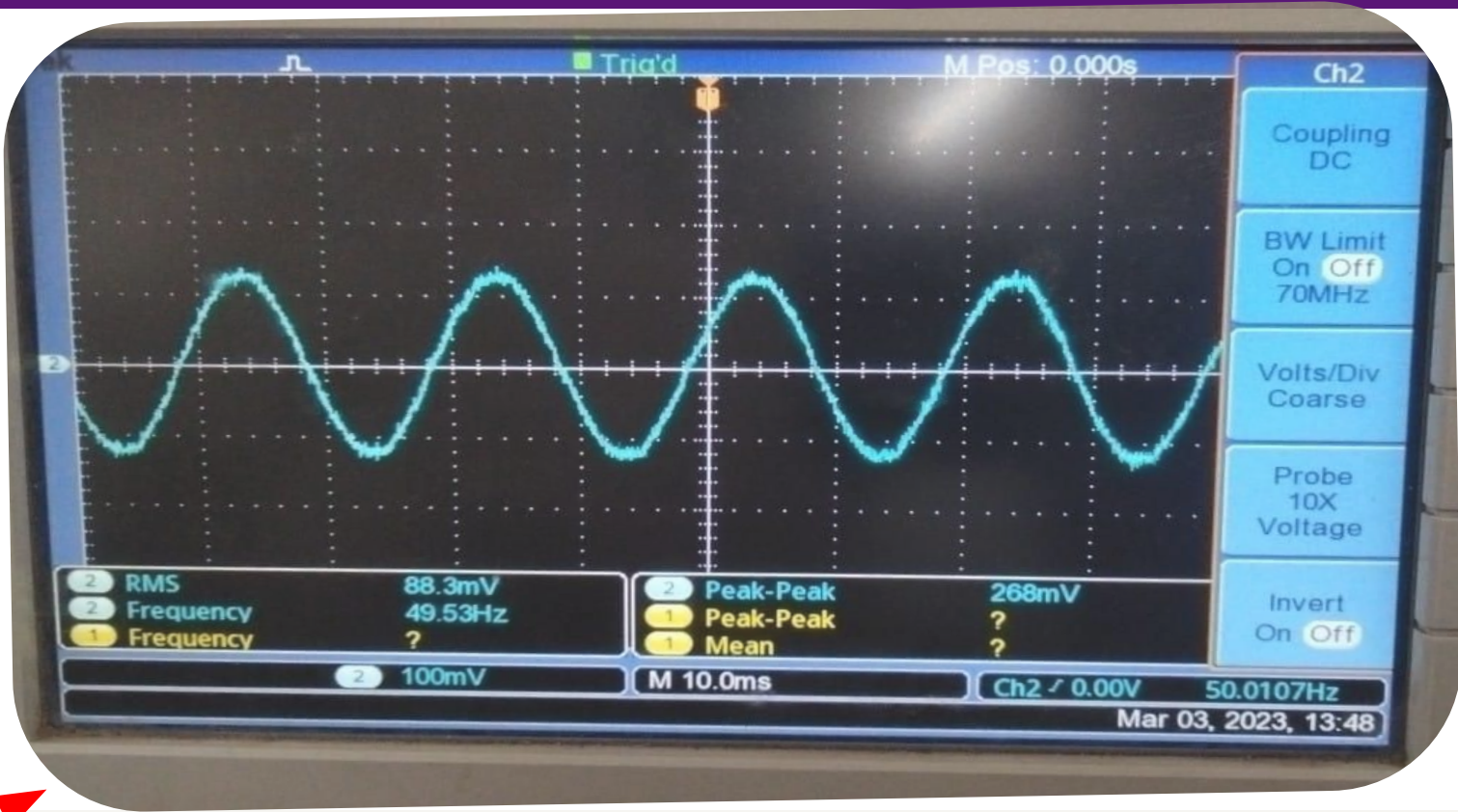
Checking attenuator stage:

since at the starting stage we can't deal with 600V so we start with

- 1) One stage attenuator
- 2) two stage attenuator
- 3)three stage attenuator
- 4) four stage attenuator

At an input of 480V pp

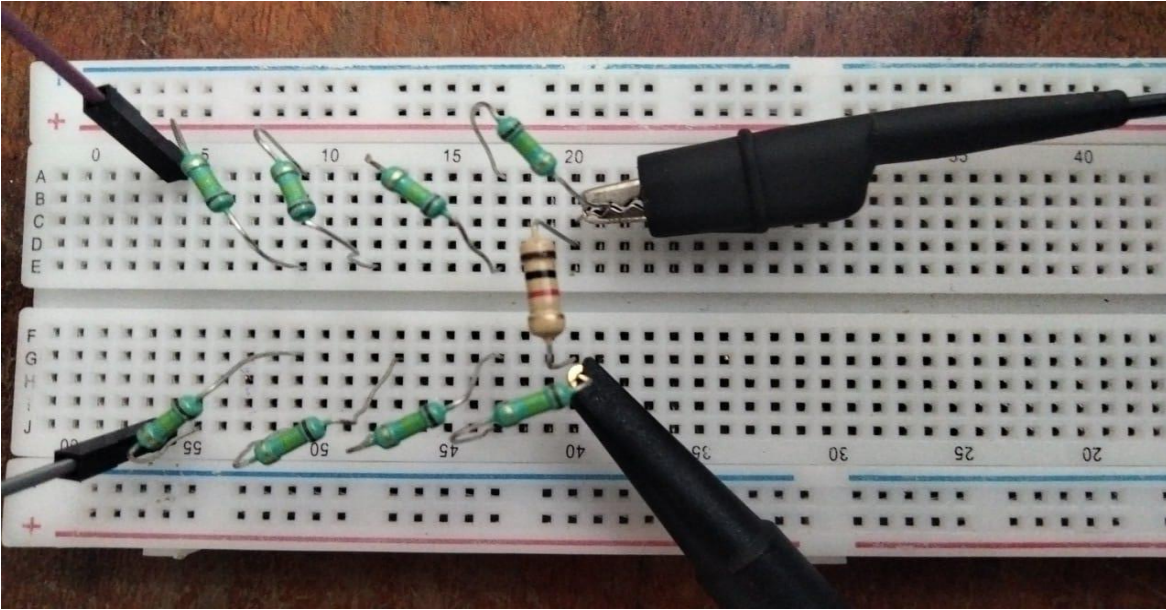
Expected = $480V / 1760 = 272mV$
Obtained = 268mV



1700x Attenuation

Attenuator

60V DC four stage attenuator



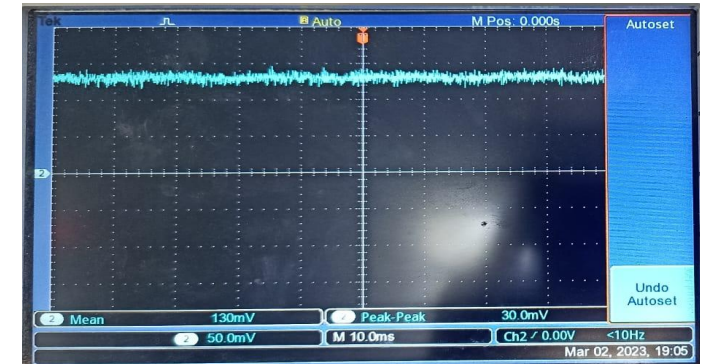
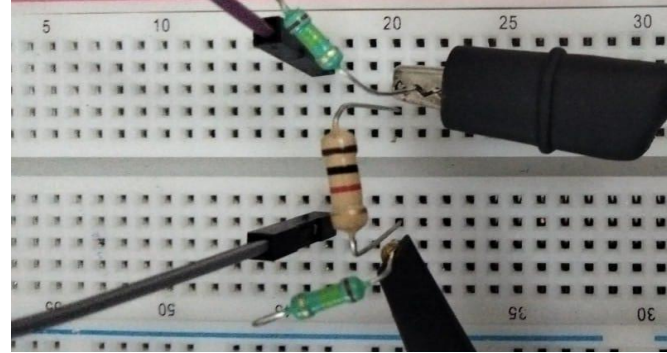
Calculations

Expected = $60V/1760 = 34mV$

Obtained = 42mV

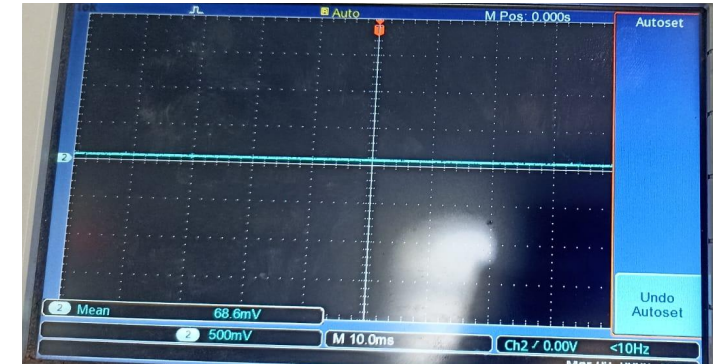
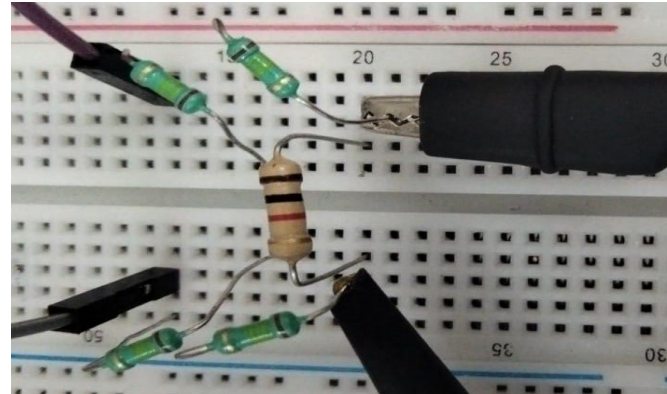
60V DC one stage attenuator

attenuation = $1/440$
expected output = 136mV
obtained = 130 mV



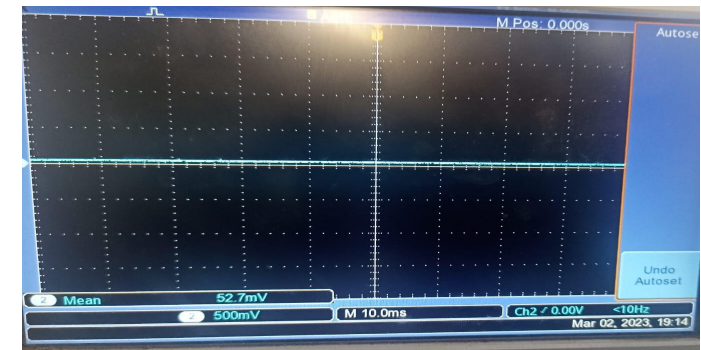
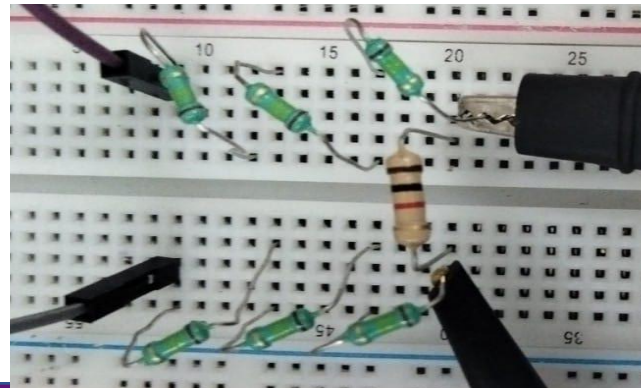
60V DC two stage attenuator

attenuation = $1/880$
expected output = 68.1mV
obtained = 68.5 mV



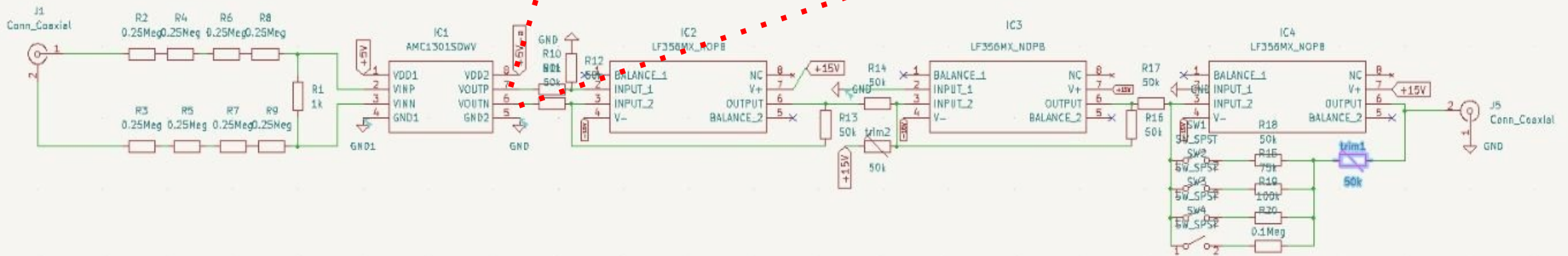
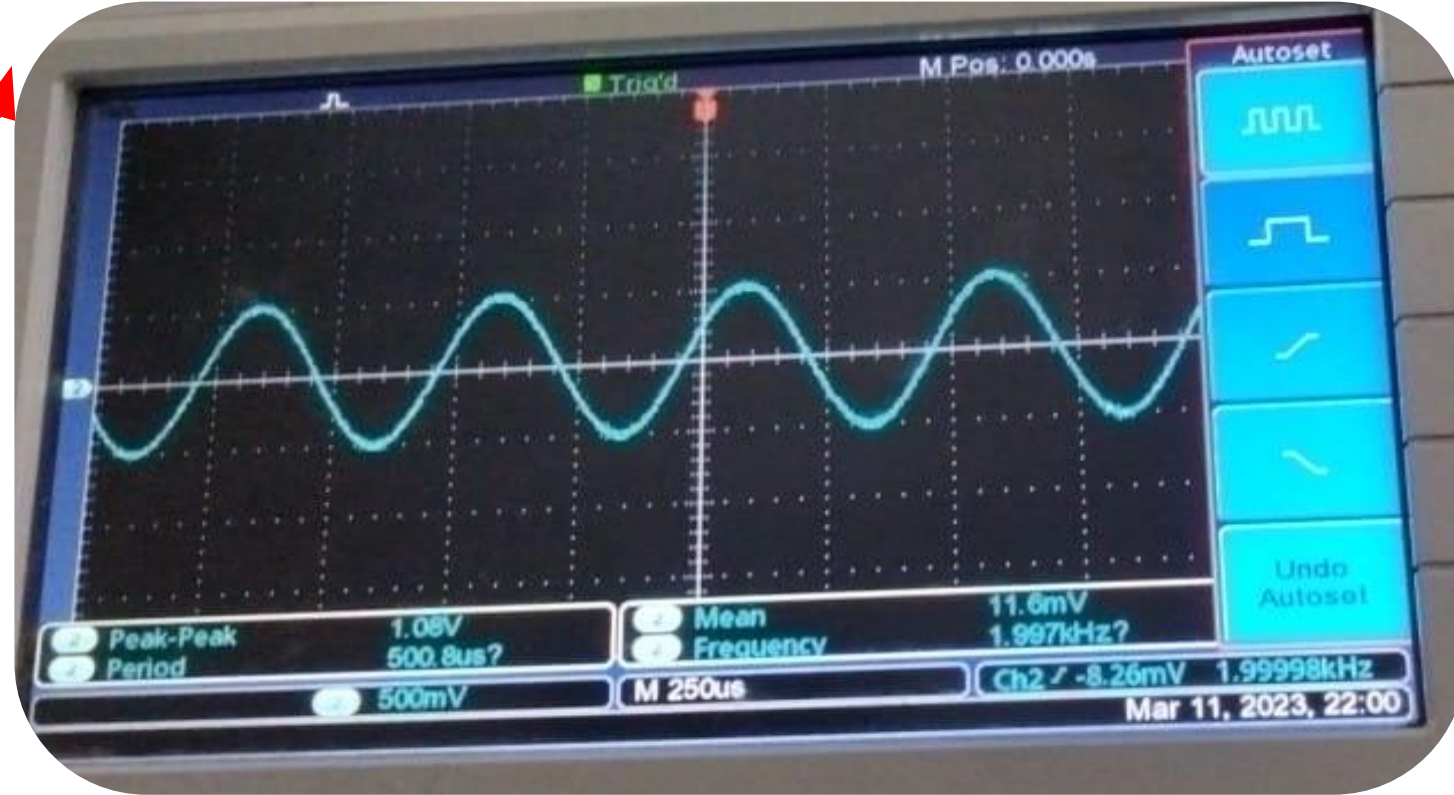
60V DC three stage attenuator

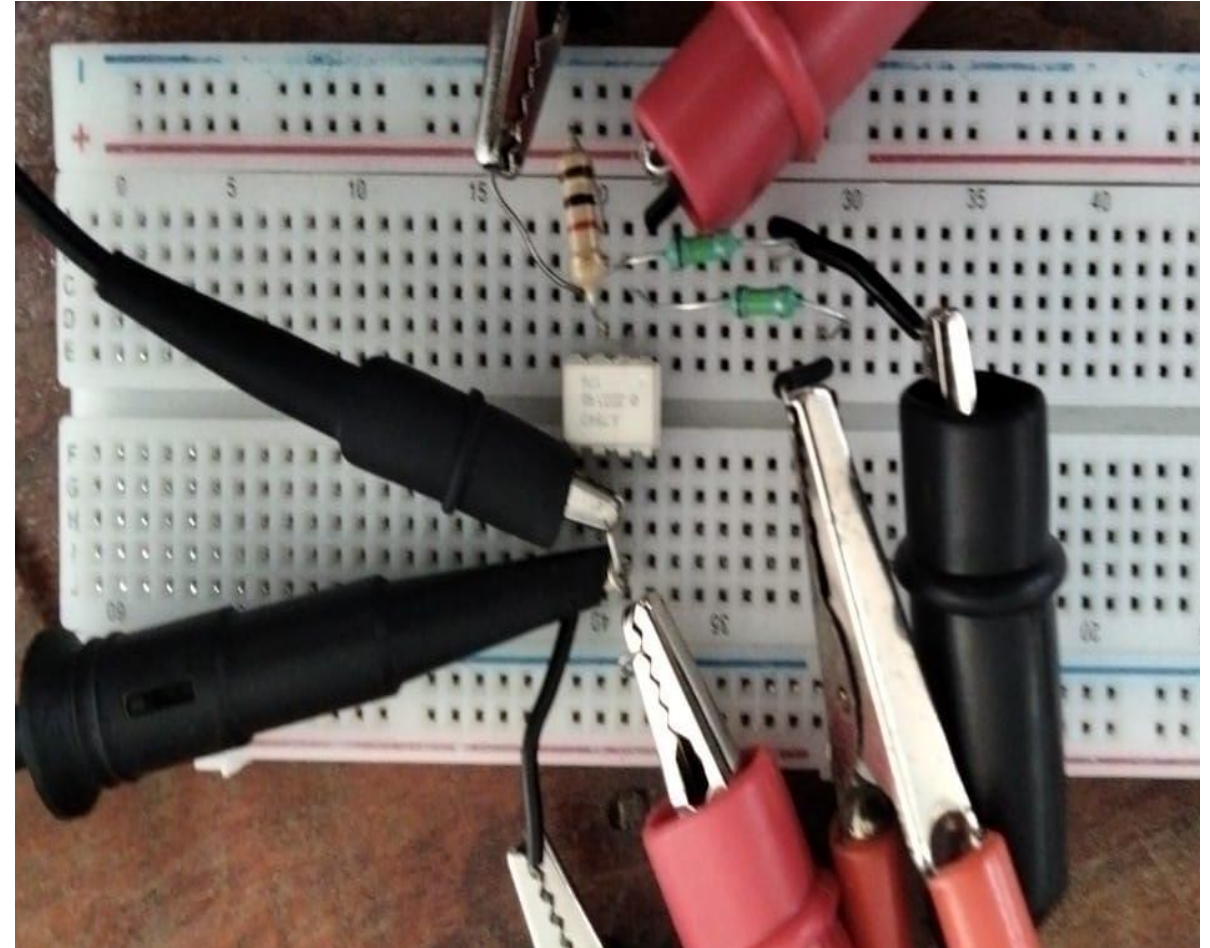
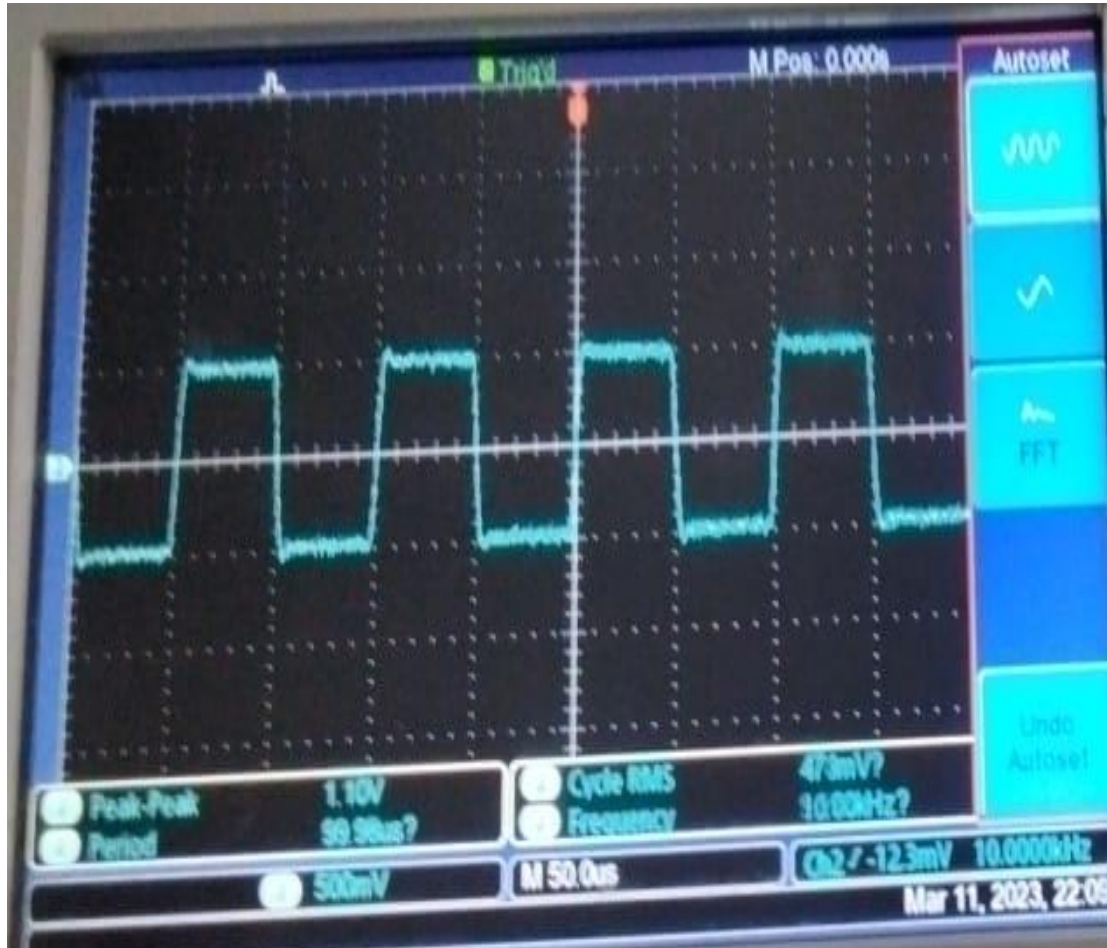
attenuation = $1/1320$
expected output = 45.45mV
obtained = 52.7 mV



At an input of 200 mv pp to isolation amplifier at 2kHz

Expected gain = 8
expected output = 2V
obtained output = 1.08V
obtained gain = around (5-6)

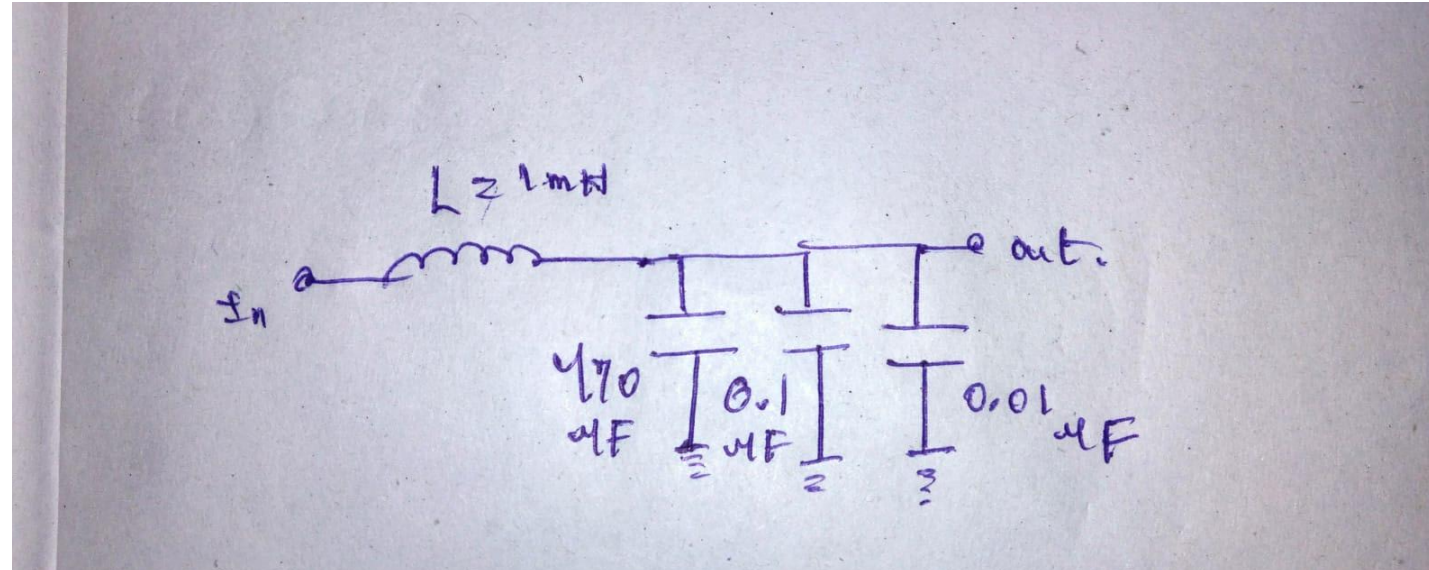
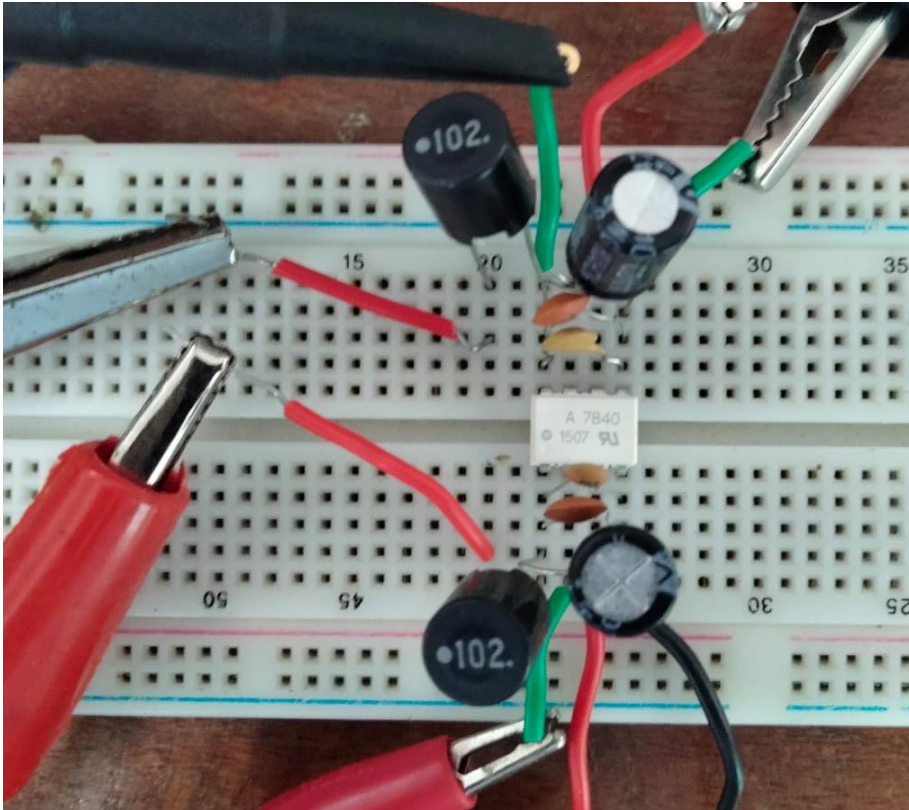




Circuit of isolation amplifier with one stage attenuator

POWER SOURCE for isolation amplifier

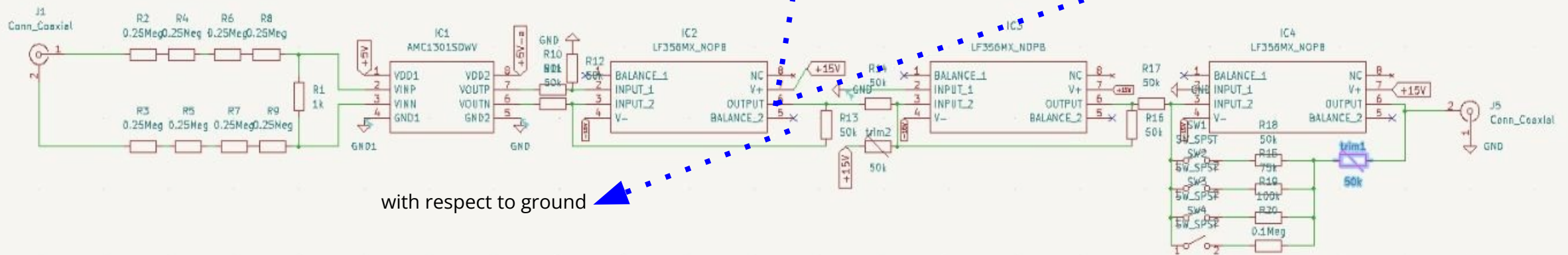
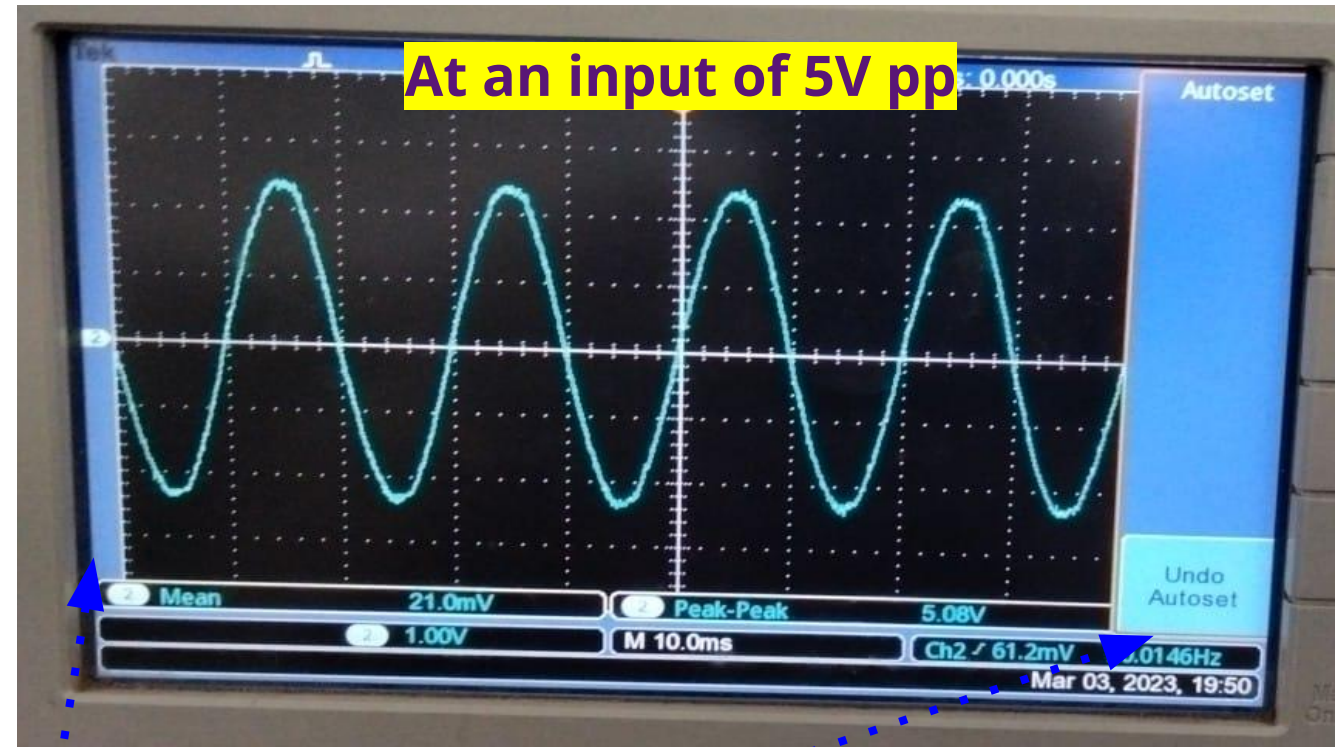
- 1) Input side and output side with RPS
- 2) Both side RPS through isolation transformer
- 3) Input side with battery and output side with RPS
- 4) Input side with RPS and output side with battery
- 5) used LC filter for cancellation of noise
- 6) Input side and output side with battery



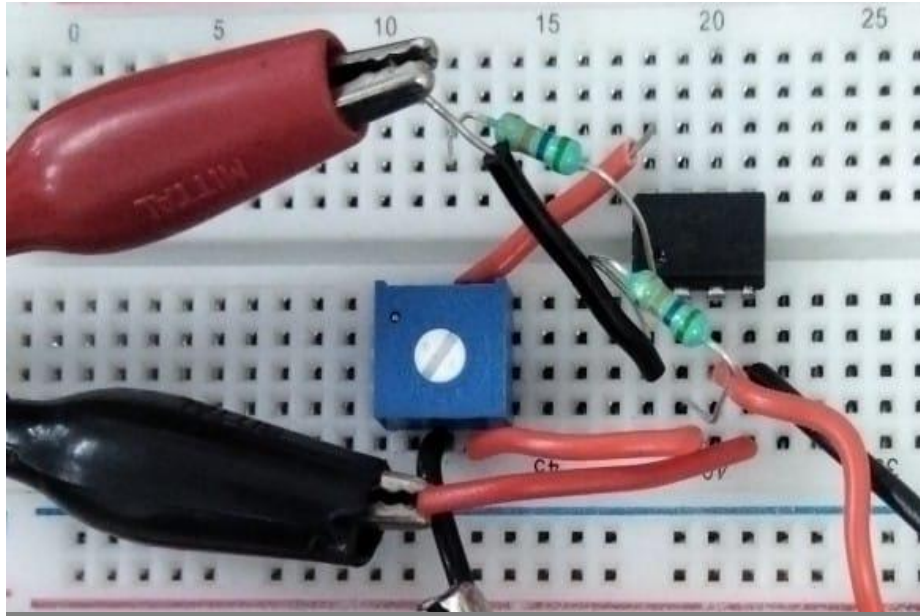
LC Filter Circuit

used for noise correction

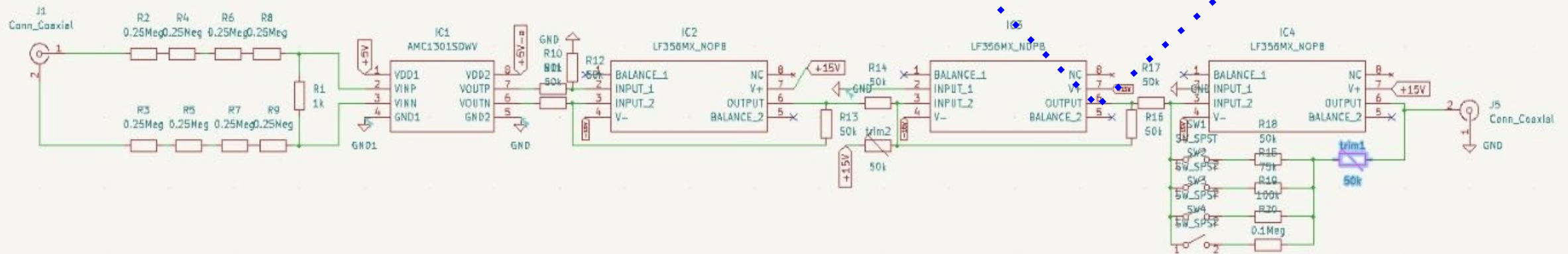
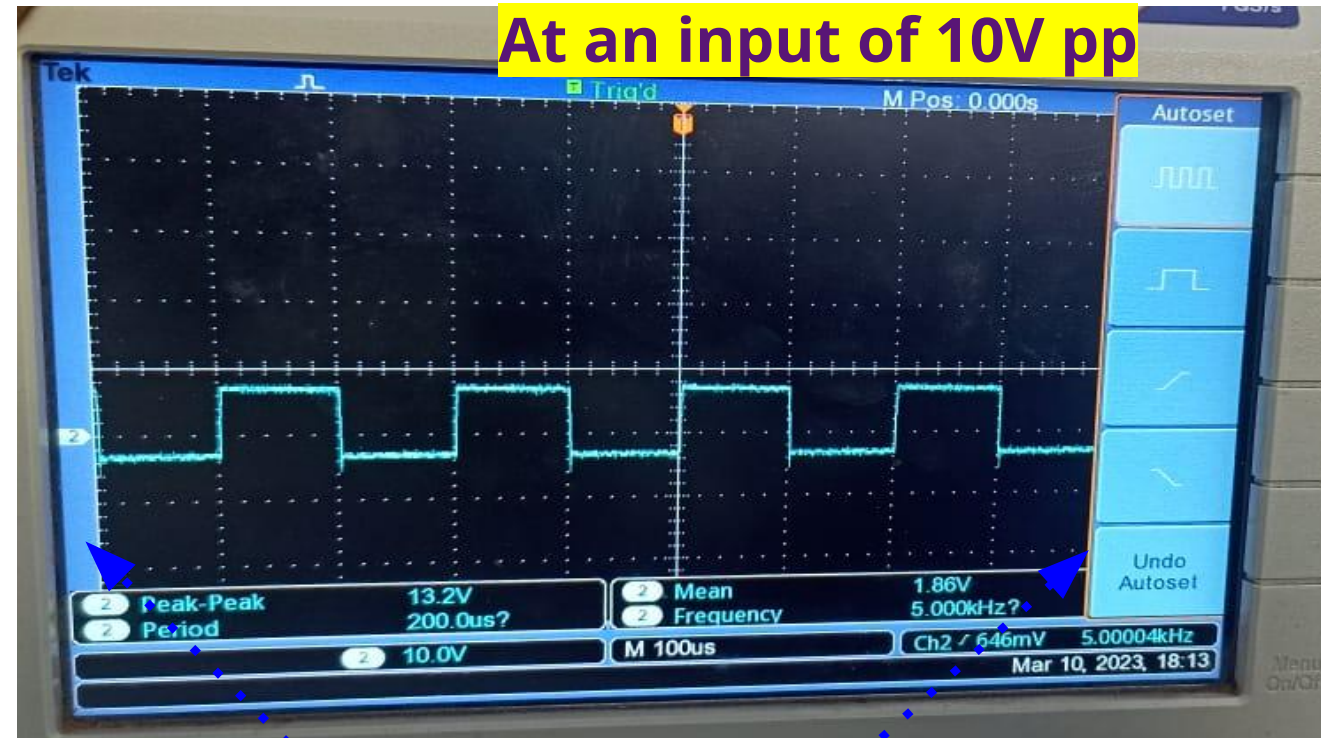
Differential Amplifier



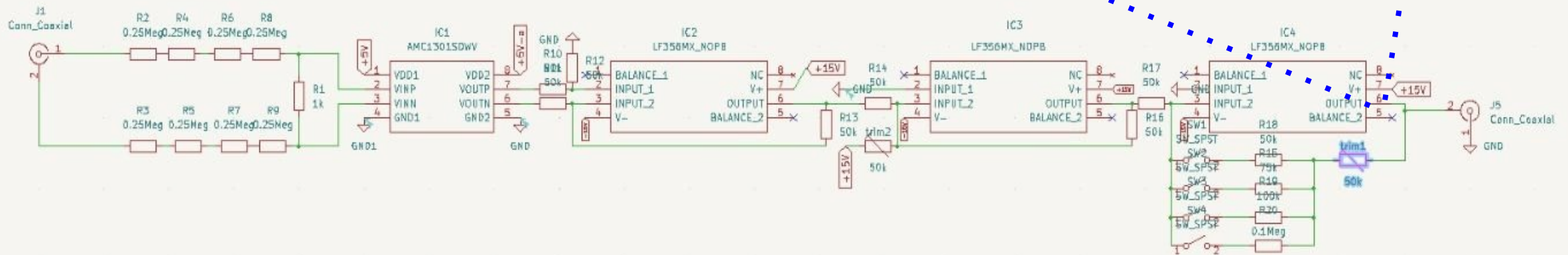
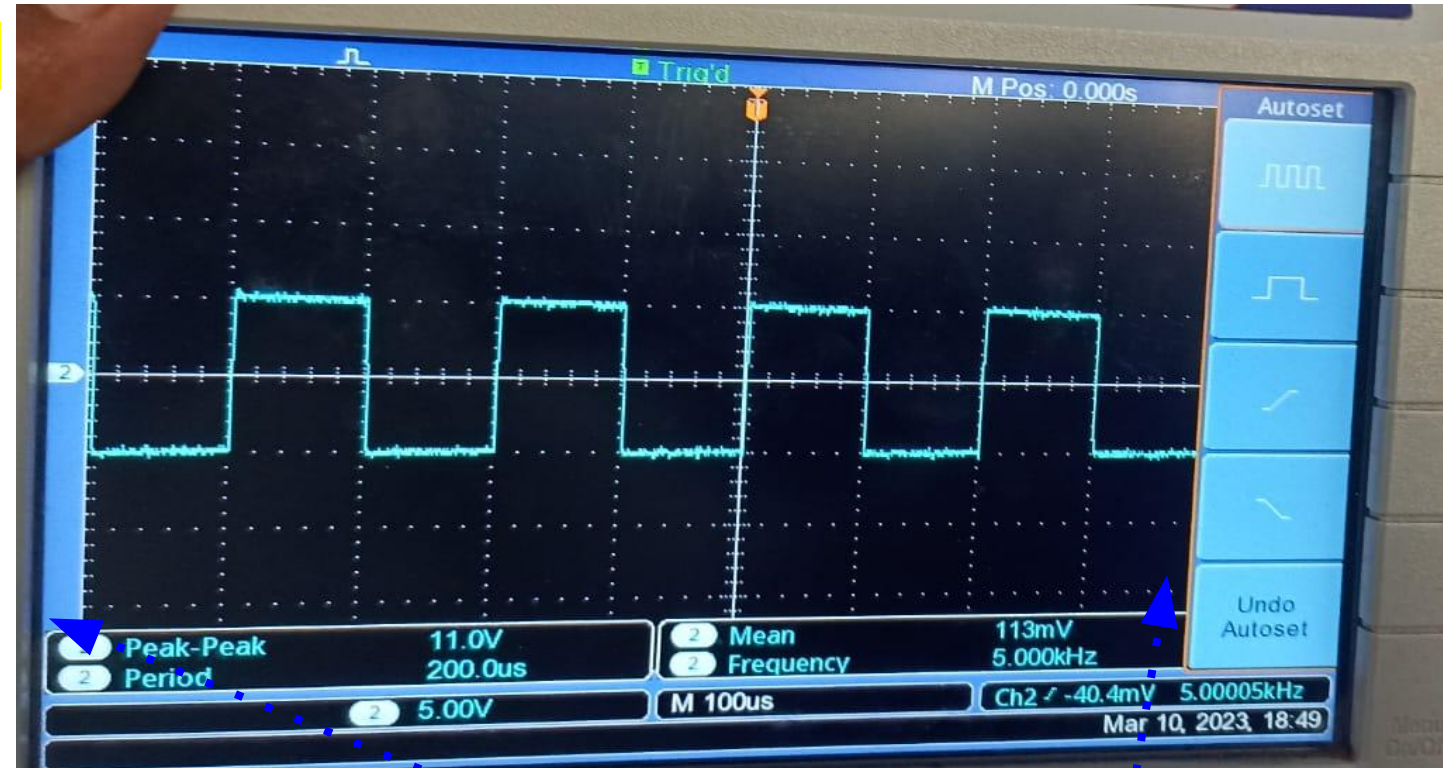
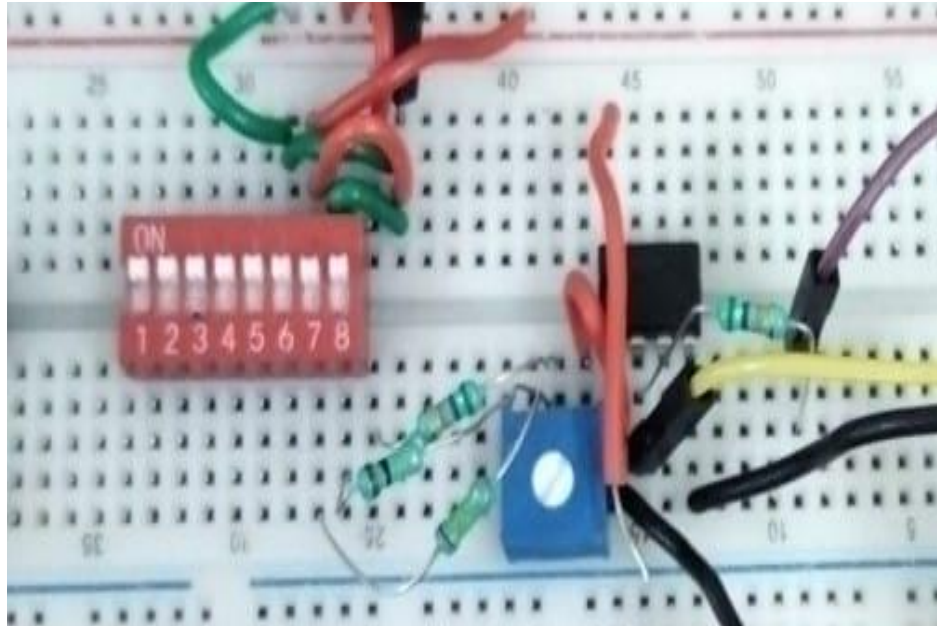
Summing amplifier(offset correction)



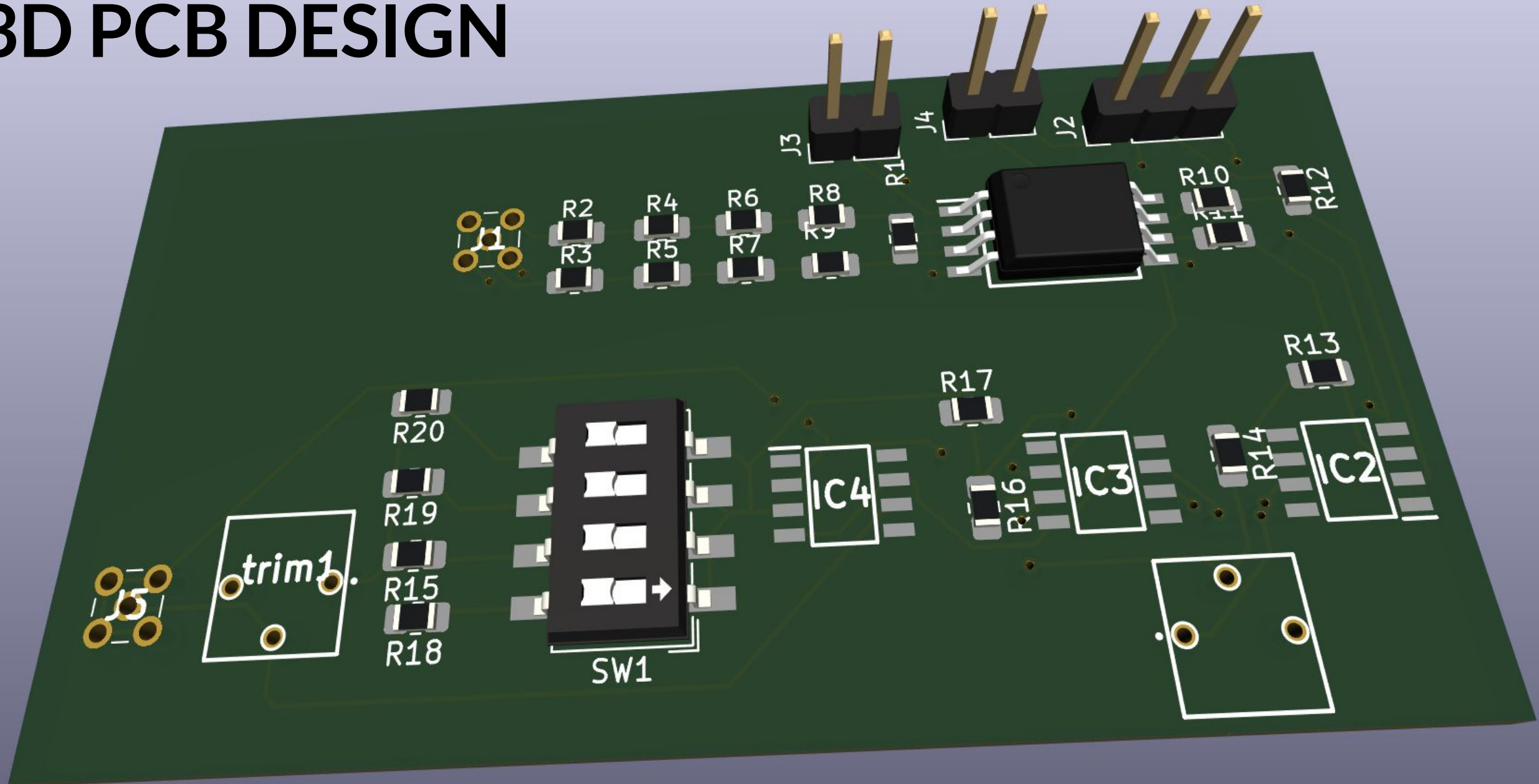
At an input of 10V pp



Inverting amplifier (Gain Correction)



3D PCB DESIGN



Future work / path to completion

Final Evaluation

1. Testing and Calibration
2. Bugs and Fixing
3. Final PoC System Demonstration 10/April 2023

Final demo plan

We will show our working design for 600V DC which will display voltage value in DSO.