Q1.

Ppr 2

Message Passing Interface(MPI) is a programming paradigm used wdiely on parallel computer architecture. Why do we use these interfaces? Briefly discuss MPI communication along with discussion on point to point and collectiove MPI communication methods.

Message Passing Interface (MPI) is a **standardized and portable programming paradigm** designed for **parallel computing** on distributed-memory systems. It allows multiple processes running on different nodes (or processors) to communicate and coordinate their tasks efficiently. MPI is widely used because it provides **high performance, scalability, and flexibility** in parallel applications such as scientific simulations, data analysis, and engineering computations.

Why do we use MPI?

1. **Parallelism**: MPI enables processes to run concurrently across multiple processors, improving performance for large computations.
2. **Portability**: MPI programs can run on different parallel architectures without modification.
3. **Explicit Communication**: Processes can exchange data explicitly, giving programmers control over data flow and synchronization.
4. **Scalability**: MPI supports thousands of processes efficiently, making it suitable for high-performance computing (HPC) systems.
5. **Flexibility**: MPI provides both **point-to-point** and **collective communication** methods for different communication patterns.

MPI Communication

MPI communication is the process by which **data is exchanged between processes**. It is categorized mainly into:

1. Point-to-Point Communication

- **Definition:** Direct communication between **two processes**.
- **Operations:**
  - `MPI_Send`: Sends data from one process to another.
  - `MPI_Recv`: Receives data from a specific process.
- **Characteristics:**
  - One-to-one communication.
  - Can be **blocking** (waits until the operation completes) or **non-blocking** (allows computation to continue while communication occurs).
- **Example:**
  Process 0 sends an array of numbers to Process 1 for further computation.

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2. Collective Communication

- **Definition:** Communication involving **all or a subset of processes** in a communicator.
- **Common Methods:**
  - `MPI_Bcast`: Broadcasts data from one process to all others.
  - `MPI_Reduce`: Combines data from all processes using an operation (like sum, max) and returns the result to one process.
  - `MPI_Allreduce`: Like `MPI_Reduce`, but the result is distributed to all processes.
  - `MPI_Gather`: Collects data from all processes to a single process.
  - `MPI_Scatter`: Distributes distinct data from one process to all processes.
- **Characteristics:**
  - Efficient for synchronized operations across multiple processes.
  - Reduces programming complexity for group communication.

Summary:
MPI is used to enable communication between processes in parallel computing. **Point-to-point communication** is for **direct exchange between two processes**, while **collective communication** involves **coordinated data exchange among multiple processes**. Using these methods, programmers can implement scalable, high-performance parallel applications.

If you want, I can also draw a **diagram showing MPI communication flow** for point-to-point vs collective methods, which makes it easier to visualize. Do you want me to do that?

Q2.

Analyze the role of the mapping schemes in parallel and distributed computing. Briefly describe different schemes(any three) used for load balancing in parallel and distributed computing.

In **parallel and distributed computing**, **mapping schemes** play a crucial role in determining **how tasks or processes are assigned to processors or computing nodes**. Effective mapping is essential to ensure **load balancing, minimize communication overhead, and improve overall system performance**. Poor mapping can lead to idle processors, increased communication costs, and reduced efficiency.

Role of Mapping Schemes

1. **Load Distribution:** Ensures that each processor gets a roughly equal portion of the total work to avoid some processors being idle while others are overloaded.
2. **Communication Minimization:** Assigns tasks to processors in a way that reduces inter-processor communication, improving performance.

3. **Scalability:** Helps the system scale efficiently with the addition of more processors or nodes.
4. **Resource Utilization:** Optimizes the use of available computing resources, memory, and network bandwidth.

Load Balancing Schemes

Load balancing schemes are mapping strategies that **distribute workload evenly across processors**. Some common schemes include:

1. Static Mapping (Static Load Balancing)

- **Description:** Tasks are assigned to processors **before execution**, based on predetermined criteria such as estimated workload.
- **Characteristics:**
  - Simple to implement.
  - Low runtime overhead.
  - Not adaptive to dynamic workload changes.
- **Example:** Dividing a large matrix multiplication task evenly among all processors at the start.

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2. Dynamic Mapping (Dynamic Load Balancing)

- **Description:** Tasks are assigned to processors **during runtime**, based on current load and processor availability.
- **Characteristics:**
  - Adapts to unpredictable workloads.
  - Can achieve better utilization compared to static mapping.
  - Slight overhead due to monitoring and task redistribution.
- **Example:** In a web server cluster, incoming requests are dynamically assigned to the least busy server.

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3. Cyclic Mapping

- **Description:** Tasks are distributed to processors **in a round-robin fashion**, often used for evenly spaced workloads or data patterns.
- **Characteristics:**
  - Useful for workloads with repetitive patterns.
  - Helps avoid load imbalance when tasks have variable execution times.

- **Example:** Assigning iterations of a loop alternately to processors: Process 0 → iteration 0, Process 1 → iteration 1, Process 2 → iteration 2, and so on.

Summary:
Mapping schemes in parallel and distributed systems are essential for **efficient task allocation, load balancing, and performance optimization**. Static, dynamic, and cyclic schemes are commonly used strategies, each with advantages depending on the predictability of workloads and system architecture.

If you want, I can also create a **small diagram comparing static, dynamic, and cyclic mapping** to make it visually easier to understand. Do you want me to do that?

Q3 Enlist different mapping schemes along with its types. Briefly discuss different schemes which are used for static task-process ampping based on data partitioning .

In **parallel and distributed computing**, **mapping schemes** define how **tasks (or processes) are assigned to processors**. Proper mapping is essential to achieve **load balancing, minimize communication overhead, and improve performance**.

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1. Different Mapping Schemes and Their Types

Mapping schemes are broadly classified into:

A. Static Mapping (Static Task-Processor Mapping)

- **Definition:** Task assignments are **determined before execution** and do not change during runtime.
- **Types of Static Mapping:**
    1. **Block Mapping** – Divides tasks/data into contiguous blocks and assigns them to processors.
    2. **Cyclic Mapping** – Assigns tasks to processors in a round-robin manner.
    3. **Block-Cyclic Mapping** – Combines block and cyclic mapping; assigns blocks of tasks in a cyclic order.

B. Dynamic Mapping (Dynamic Task-Processor Mapping)

- **Definition:** Task assignments are **decided during runtime** based on processor availability and load.
- **Types of Dynamic Mapping:**
    1. **Centralized Dynamic Mapping** – A central scheduler assigns tasks to processors dynamically.
    2. **Distributed Dynamic Mapping** – Each processor independently decides which task to execute next.
    3. **Adaptive Mapping** – Adjusts mapping in real-time based on workload variations.

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2. Static Task-Processor Mapping Based on Data Partitioning

Static mapping based on **data partitioning** divides data among processors to ensure **balanced workload and reduced communication**. Some commonly used schemes are:

a) Block Partitioning

- **Description:** Data is divided into contiguous blocks and each block is assigned to a processor.
- **Example:** A matrix of size 8×8 assigned to 4 processors:
    - Processor 0 → rows 0–1
    - Processor 1 → rows 2–3
    - Processor 2 → rows 4–5
    - Processor 3 → rows 6–7
- **Advantages:** Simple and efficient for uniform data.
- **Disadvantages:** Can lead to load imbalance if tasks have variable execution times.

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b) Cyclic Partitioning

- **Description:** Data elements are assigned to processors **in a round-robin fashion**.
- **Example:** Matrix rows assigned as:
    - Processor 0 → rows 0, 4
    - Processor 1 → rows 1, 5
    - Processor 2 → rows 2, 6
    - Processor 3 → rows 3, 7
- **Advantages:** Balances load when tasks have non-uniform execution times.
- **Disadvantages:** Can increase communication overhead if tasks depend on contiguous data.

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c) Block-Cyclic Partitioning

- **Description:** Divides data into **blocks of fixed size** and distributes them **cyclically** among processors.
- **Example:** With block size = 2, and 4 processors:
  - Processor 0 → rows 0–1, 8–9
  - Processor 1 → rows 2–3, 10–11
  - Processor 2 → rows 4–5, 12–13
  - Processor 3 → rows 6–7, 14–15
- **Advantages:** Combines benefits of block and cyclic; good for load balancing and locality.
- **Disadvantages:** Slightly more complex to implement.

Summary:

- **Static mapping** is decided before execution, while **dynamic mapping** adapts at runtime.
- **Data partitioning-based static schemes**—block, cyclic, and block-cyclic—help **distribute workload evenly** and improve **parallel efficiency**.

If you want, I can also make a **diagram showing block, cyclic, and block-cyclic data mapping** for better visualization. This usually helps in exams or assignments. Do you want me to do that?

Q4. Highlight the importance of GPUs in parallelism.How can we differentiate between the execution model of CPU and GPUs ? Also discuss the data migration and OpenCL plateform model.

Importance of GPUs in Parallelism

GPUs (Graphics Processing Units) are specialized hardware designed for **highly parallel computations**. Unlike CPUs, which are optimized for sequential task performance, GPUs excel at **handling many tasks simultaneously**, making them essential in modern parallel computing.

Key Points of Importance:

1. **Massive Parallelism:**
   - GPUs have thousands of cores capable of executing thousands of threads concurrently.
   - Ideal for tasks like matrix multiplication, image processing, AI, and scientific simulations.
2. **High Throughput:**
   - GPUs are designed to process **large volumes of data quickly**, achieving higher throughput than CPUs for parallel workloads.
3. **Efficiency in SIMD Workloads:**

    - Works best with **Single Instruction Multiple Data (SIMD)** patterns, where the same operation is applied to many data points simultaneously.
4. **Energy and Cost Efficiency:**
    - For certain parallel workloads, GPUs can perform computations faster and with less energy per operation than CPUs.

CPU vs GPU Execution Model

Feature	CPU	GPU
Purpose	General-purpose, sequential tasks	Data-parallel, high-throughput tasks
Number of Cores	Few cores (4–64 typically)	Thousands of small cores
Memory Hierarchy	Large cache, low-latency	Smaller caches per core, high-bandwidth global memory
Execution Model	MIMD (Multiple Instruction Multiple Data)	SIMD/SIMT (Single Instruction Multiple Threads)
Latency vs Throughput	Optimized for low latency	Optimized for high throughput
Control Complexity	Handles complex branching efficiently	Best for uniform, regular computations

Summary: CPUs are optimized for complex, sequential tasks, while GPUs excel at **parallel execution of similar operations across large datasets**.

Data Migration in GPU Computing

- **Definition:** Moving data between **CPU memory (host)** and **GPU memory (device)**.
- **Steps:**
    1. **Allocate memory** on the GPU device.
    2. **Copy input data** from host memory to GPU memory.
    3. **Execute kernel** (parallel computation) on GPU.
    4. **Copy results back** to host memory.
- **Importance:** Minimizing data transfer is critical because **memory transfer between host and device is slower** than GPU computation.

OpenCL Platform Model

OpenCL (Open Computing Language) is a framework for writing programs that execute across **heterogeneous platforms** (CPUs, GPUs, FPGAs).

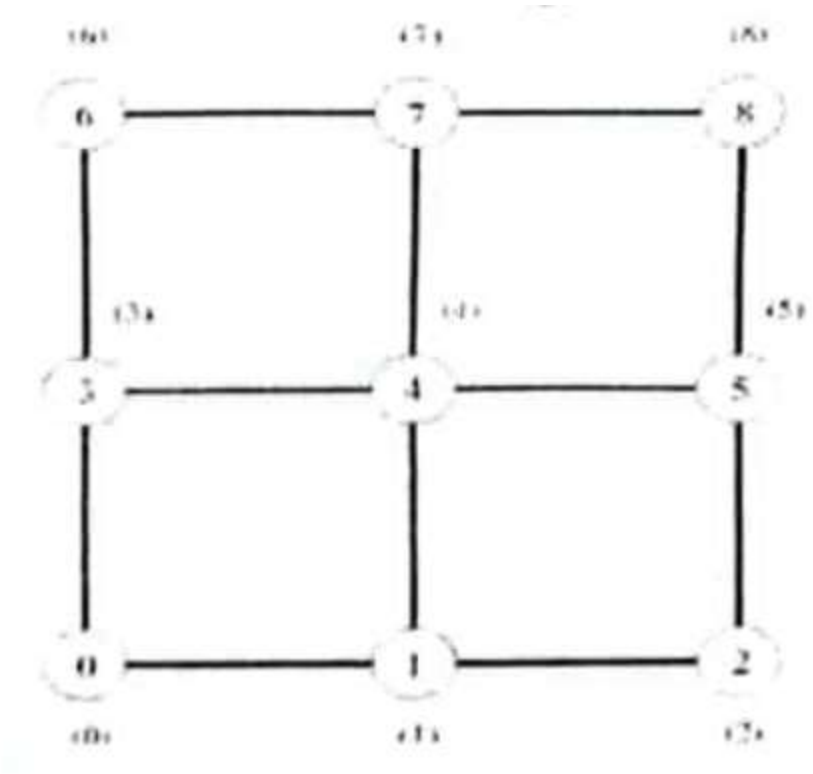
Platform Model Components:

1. **Host:**
   - The CPU acts as a host controlling computation, managing memory, and launching kernels.
2. **Compute Devices:**
   - GPUs, CPUs, or other accelerators that execute the parallel tasks.
3. **Compute Units (CUs):**
   - Each device has multiple compute units; each unit contains **processing elements** (threads) for parallel execution.
4. **Memory Hierarchy:**
   - **Global Memory:** Accessible by all threads.
   - **Local Memory:** Shared among threads in a compute unit.
   - **Private Memory:** Private to each thread.
5. **Kernels:**
   - Functions written in OpenCL C executed on compute devices in parallel.

Summary: OpenCL provides a **portable, cross-platform framework** to leverage CPU and GPU parallelism efficiently, controlling **data placement and execution hierarchy**.

If you want, I can also **draw a diagram showing CPU vs GPU execution, data migration, and OpenCL model**, which makes it much easier to visualize and remember. Do you want me to do that?

Q5. Briefly descibe basic communication operation One-to-All broadcast and All-to-One Reduction. Discuss the stpes for data distribution using all to all broadcast on the following 3x3 Mesh with initialdata distribution given



The diagram you provided shows a **3×3 mesh network** of 9 nodes (0–8), connected horizontally and vertically. Let's break down the MPI **basic communication operations** and how data distribution works using **All-to-All Broadcast** on this mesh.

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1. One-to-All Broadcast

Definition:
A communication operation where **one process (root) sends the same data to all other processes** in a network.

Steps:

1. The root process prepares the data to be sent.
2. The data is transmitted along the network links, typically using a tree or mesh-based algorithm to minimize communication steps.
3. Each receiving node receives the data and can forward it if necessary to other nodes (depending on the network topology).

Example on 3×3 mesh:

- If **Node 4** is the root and wants to broadcast its data:
    1. Node 4 sends data to its neighbors: Node 1, Node 3, Node 5, Node 7.
    2. Each neighbor forwards data to its unvisited neighbors:

    - Node 1 → Nodes 0, 2
    - Node 3 → Node 0, 6
    - Node 5 → Node 2, 8
    - Node 7 → Nodes 6, 8
- Finally, all nodes have received the broadcast data.

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2. All-to-One Reduction

Definition:
A communication operation where **all nodes contribute data that is combined (reduced) using a function such as sum, max, or min** at a **single root node**.

Steps:

1. Each node starts with its local data.
2. Neighboring nodes exchange data according to the reduction tree.
3. Data is combined using the reduction function at each step.
4. Eventually, the root node receives the final reduced value from all nodes.

Example on 3×3 mesh:

- If **Node 4** is the root and we want to compute the sum:
    1. Leaf nodes send their data to adjacent nodes.
    2. Intermediate nodes sum incoming data with their own and forward it towards the root.
    3. Node 4 finally receives the sum of all node data.

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3. Steps for Data Distribution Using All-to-All Broadcast

Initial data distribution: Let's assume the nodes have initial data as follows:

Node	Data
0	d0
1	d1
2	d2
3	d3

Node	Data
4	d4
5	d5
6	d6
7	d7
8	d8

All-to-All Broadcast: Every node sends its data to **all other nodes**, so that at the end **every node has all 9 data elements**.

Step-wise approach on a 3×3 mesh:

1. **Step 1 (Horizontal communication):**
   - Each row exchanges data among nodes:
     - Row 0 (Nodes 0,1,2) → each node shares its data with the other two nodes in the row.
     - Row 1 (Nodes 3,4,5) → same.
     - Row 2 (Nodes 6,7,8) → same.
2. **Step 2 (Vertical communication):**
   - Each column exchanges accumulated data:
     - Column 0 (Nodes 0,3,6) → each node now has data from all nodes in its row and column.
     - Column 1 (Nodes 1,4,7)
     - Column 2 (Nodes 2,5,8)
3. **Step 3 (Final merging):**
   - After these horizontal and vertical steps, each node contains all data elements: d0–d8.

This **mesh-based all-to-all broadcast** reduces the number of communication steps compared to sending directly from each node to all others.

If you want, I can **draw a step-by-step illustration on this 3×3 mesh** showing how data moves in **all-to-all broadcast**, which makes it much easier to understand for assignments or exams.

Do you want me to do that?

Here's a **step-by-step illustration of All-to-All Broadcast** on your 3×3 mesh (nodes 0–8) with initial data (d_0) to (d_8). The goal: **every node ends up with all 9 data elements**.

Step 0 – Initial Data Distribution

Node	Data
0	d0
1	d1
2	d2
3	d3
4	d4
5	d5
6	d6
7	d7
8	d8

```
Mesh Layout:

6 --- 7 --- 8
|     |     |
3 --- 4 --- 5
|     |     |
0 --- 1 --- 2
```

Step 1 – Horizontal Communication (Row-wise Broadcast)

- Each node in a row shares its data with other nodes in the same row.

Resulting Row Data:

Row	Nodes	Data at each node
0	0,1,2	d0, d1, d2
1	3,4,5	d3, d4, d5
2	6,7,8	d6, d7, d8

Step 2 – Vertical Communication (Column-wise Broadcast)

- Nodes in each column share their accumulated row data with other nodes in the same column.

Column Communication:

- Column 0: Nodes 0, 3, 6 → each gets all data from the column → d0, d3, d6, plus row data → d0,d1,d2,d3,d6 (merged fully later)

- Column 1: Nodes 1, 4, 7 → merge row and column data → all data in column
- Column 2: Nodes 2, 5, 8 → same

Result: After vertical exchange, each node in a column has **all row data from other rows in the same column**.

Step 3 – Final Merging

- Each node now merges all received data from row and column exchanges.
- **At the end:** every node contains all 9 data elements:

[
d_0, d_1, d_2, d_3, d_4, d_5, d_6, d_7, d_8
]

Visualization:

```
Step 0:                  Step 1 (row broadcast):            Step 2 (column
exchange):
Node 0: d0               Node 0: d0,d1,d2                   Node 0:
d0,d1,d2,d3,d6,d4,d5,d7,d8
Node 1: d1               Node 1: d0,d1,d2                   Node 1:
d0,d1,d2,d3,d6,d4,d5,d7,d8
Node 2: d2               Node 2: d0,d1,d2                   Node 2:
d0,d1,d2,d3,d6,d4,d5,d7,d8
Node 3: d3               Node 3: d3,d4,d5                   Node 3:
d0,d1,d2,d3,d6,d4,d5,d7,d8
Node 4: d4               Node 4: d3,d4,d5                   Node 4:
d0,d1,d2,d3,d6,d4,d5,d7,d8
Node 5: d5               Node 5: d3,d4,d5                   Node 5:
d0,d1,d2,d3,d6,d4,d5,d7,d8
Node 6: d6               Node 6: d6,d7,d8                   Node 6:
d0,d1,d2,d3,d6,d4,d5,d7,d8
Node 7: d7               Node 7: d6,d7,d8                   Node 7:
d0,d1,d2,d3,d6,d4,d5,d7,d8
Node 8: d8               Node 8: d6,d7,d8                   Node 8:
d0,d1,d2,d3,d6,d4,d5,d7,d8
```

✅ **Summary of Steps:**

1. **Row-wise broadcast:** Each node shares data within its row.
2. **Column-wise exchange:** Each node shares accumulated data with nodes in the same column.
3. **Final merge:** Every node combines received data → all nodes have complete dataset.

If you want, I can also **draw this as a colored diagram with arrows showing data movement** across the mesh—it's much easier to visualize than text.

Do you want me to make that diagram?

Based on the syllabus and lecture plan of **Parallel and Distributed Computing** at the University of Gujrat (IT Department), the questions you shared fall under the following **topics/lectures**:

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1. Message Passing Interface (MPI)

- **Related Questions:**
  - "Why do we use MPI interfaces?"
  - "Discuss MPI communication along with point-to-point and collective communication methods."
- **Lecture References:**
  - Lec #11 (Basic Communication Operations)
  - Lec #19 (MPI in Tools section)
- **Topic Area:** Parallel programming, distributed memory programming, inter-process communication.

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2. Mapping Schemes and Load Balancing

- **Related Questions:**
  - "Analyze the role of mapping schemes in parallel and distributed computing."
  - "Different schemes used for load balancing."
  - "Static task-process mapping based on data partitioning."
- **Lecture References:**
  - Lec #8 (Memory Consistency Model, Memory Hierarchies, Mapping Schemes)
  - Extra Week 1 (Load Balancing)
- **Topic Area:** Task assignment, data partitioning, performance optimization.

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3. GPUs and Parallelism

- **Related Questions:**
  - "Highlight the importance of GPUs in parallelism."
  - "Difference between CPU and GPU execution model."
  - "Data migration and OpenCL platform model."
- **Lecture References:**

    - Lec #14 (GPU Architecture and Programming)
    - Lec #16(2) & Lec #16(1) (CUDA Programming)
- **Topic Area:** SIMD/SIMT execution, heterogeneous computing, accelerator programming, OpenCL/CUDA.

Supporting Topics Covered in the Course

Other relevant topics that connect to your questions:

1. **Parallel Architectures and Execution Models**
    - MIMD/SIMD (Extra Week 2)
    - Multithreaded programming and OpenMP (Lec #10, #20)
2. **Data Partitioning and Task Decomposition**
    - Decomposition techniques (Lec #7)
    - Memory consistency & hierarchies (Lec #8)
3. **Performance & Scalability**
    - Performance analysis and tuning (Extra Week 4)
    - Scheduling and scalability (Lec #13)

✅ **Summary:**

Question Topic	Lecture/Week Reference	Concept Area
MPI and communications	Lec #11, Lec #19	Message-passing, distributed memory, point-to-point, collective
Mapping schemes & load balancing	Lec #8, Extra Week 1	Task-process mapping, static/dynamic, block/cyclic/block-cyclic
GPU importance & execution model	Lec #14, Lec #16	SIMD/SIMT, CPU vs GPU, data migration, OpenCL/CUDA
Parallel algorithms & multithreading	Lec #10, Lec #20	OpenMP, threads, shared memory programming