DESIGN & IMPLEMENATION OF HARWARE INTERFACE TO XADC USING FPGA NEXYS 4DDR BOARD

COURSE PROJECT

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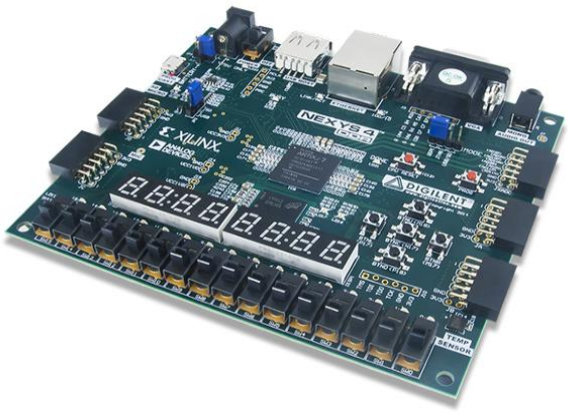
1. Introduction to FPGA board

The Nexys 4 DDR board is a complete, ready-to-use digital circuit development platform based on the latest Artix-7$^{T\ M}$ Field Programmable Gate Array (FPGA) from Xilinx^{R} . With its large, high-capacity FPGA (Xilinx part number XC7A100T 1CSG324C), generous external memories, and collection of USB, Ethernet, and other ports, the Nexys 4 DDR can host designs ranging from introductory combinational circuits to powerful embedded processors. Several built-in peripherals, including an accelerometer, temperature sensor, MEMs digital microphone, a speaker ampli er, and several I/O devices allow the Nexys 4 DDR to be used for a wide range of designs without needing any other components.

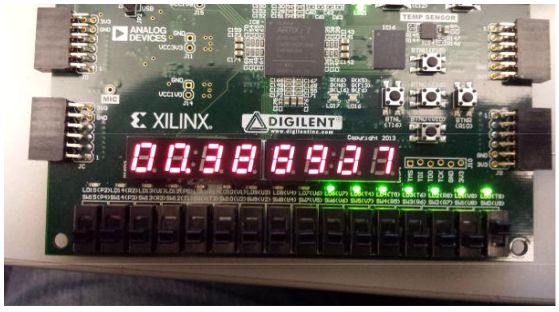


The XADC core within the Artix-7 is a dual channel 12-bit analog-to-digital converter capable of operating at 1 MSPS. Either channel can be driven by any of the auxiliary analog input pairs connected to the JXADC header. The XADC core is controlled and accessed from a user design via the Dynamic Reconfiguration Port (DRP). The DRP also provides access to voltage monitors that are present on each of the FPGAs power rails, and a temperature sensor that is internal to the FPGA.

NEXYS 4 DDR XADC Description

This simple XADC Demo project demonstrates a simple usage of the Nexys-4DDR's XADC port capability. The behavior is as follows:

- ✓ The 16 User LEDs increment from right to left as the voltage difference on the selected XADC pins gets larger.
- ✓ The two seven segment displays show the voltage difference on the AD11, AD10, AD2, AD3 pins in volts.
- ✓ sw0 and sw1 select which channel to read from.



2. Features Used in the project

- ✓ 16 User Switches
- ✓ 16 User LEDs.
- ✓ Two 4-digit 7-segment displays.
- ✓ Pmod for XADC signals.

2.1 Prerequisite

- ✓ Nexys 4 DDR FPGA board.
- ✓ Micro-USB cable.
- ✓ Wires and a voltage to measure.
- ✓ Vivado Design Suite 2016.4 (Software)

3. Modular Approach

I have utilized the XADC IP core which is embedded into Nexys 4 DDR board of Xilinx. XADC cab be operated in two modes unipolar & bipolar. I have used in XADC in unipolar mode & have divided the entire Verilog codes into small chunks depicting each its own important function and later they all are instantiated into the main XADC file. I have designed Verilog files separately for seven segment decoder, four-bit-Mux, Counter, segment clock driver & XADC IP core itself.

The following output received as I applied the Vpp from the Function generator to the XADC pins.

S. No	VPP (External)	Seven Segment Display (Output)
1	0.100 V	0.0660 V
2	0.200 V	0.1000 V
3	0.300 V	0.1500 V
4	0.400 V	0.2000 V
5	0.500 V	0.2500 V
6	0.600 V	0.3000 V
7	0.700 V	0.3500 V
8	0.800 V	0.4000 V
9	0.900 V	0.4500 V
10	1.000 V	0.5000 V
11	1.100 V	0.5500 V
12	1.200 V	0.6000 V
13	1.300 V	0.6500 V
14	1.400 V	0.7000 V
15	1.500 V	0.7500 V
16	1.600 V	0.8000 V
17	1.700 V	0.8500 V
18	1.800 V	0.9000 V
19	1.900 V	0.9500 V
20	2.000 V	1.0000 V

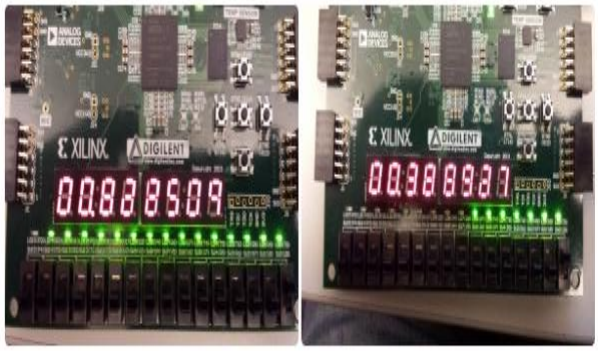
4. Steps to perform the Demo of the project

Applying voltage to XADC port

For this demo, the AD11P and AD11N pins are used on the JXADC header. We have used potentiometer, input of potentiometer is connected to voltage generator and output is directly given to the AD11P and AD11N. All of the other pins were grounded to avoid coupling.

Segment Display and LEDs

The 7-Segment display shows the current voltage across the selected xadc pins. The LEDs turn on from right to left as the input voltage increases.



Selecting a Channel

To view the level of a different XADC channel on the display and LEDs, change sw0 and sw1 to the desired channel number.

5 Conclusion

The built in AD11N and AD11P XADC pmod inputs are used to test the working of analog to digital converter using Nexys 4 DDR board. Potentiometer is used to provide variable analog voltage to the XADC pmod pins. Increasing the voltages affected the 16 User LEDs increment from right to left is observed. And two seven segment displays are used to observe the voltage difference on the AD11, AD10, AD2, AD3 pins in volts.

Githubb: https://github.com/Muzammil-ux/XADC-Demo
Youtube Video Link: https://www.youtube.com/watch?v=4QppEJrEJ2c