Combinational Logic

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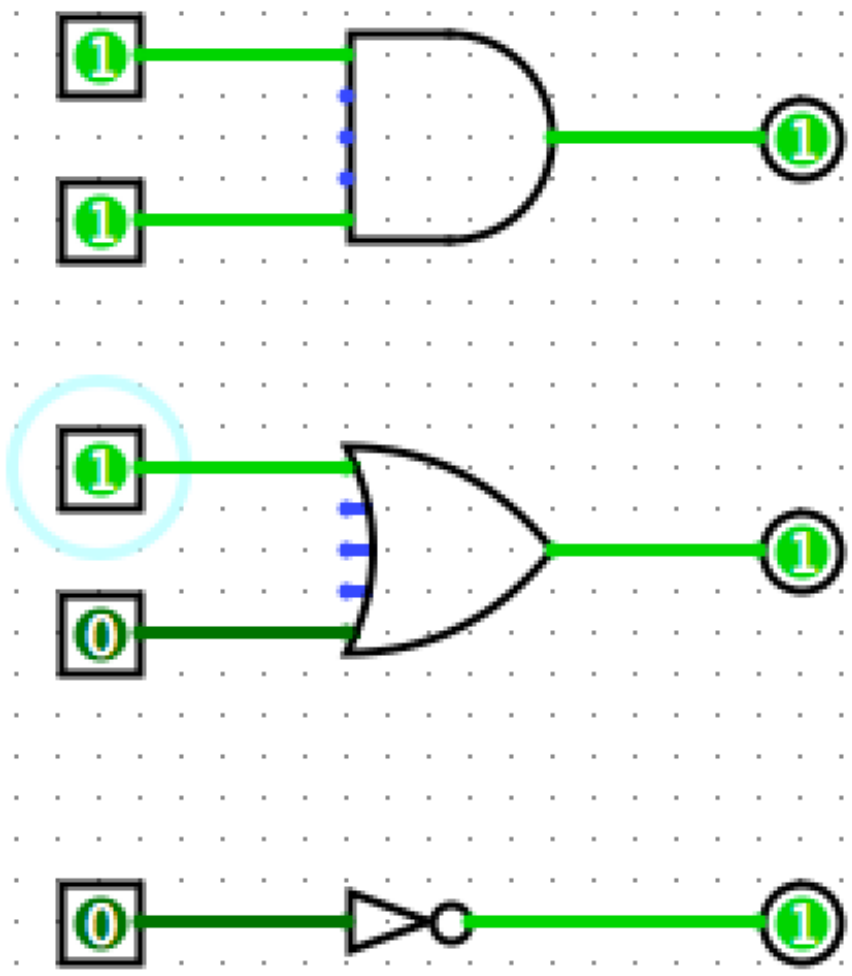
CS448H: Agile Hardware Design
Winter 2017

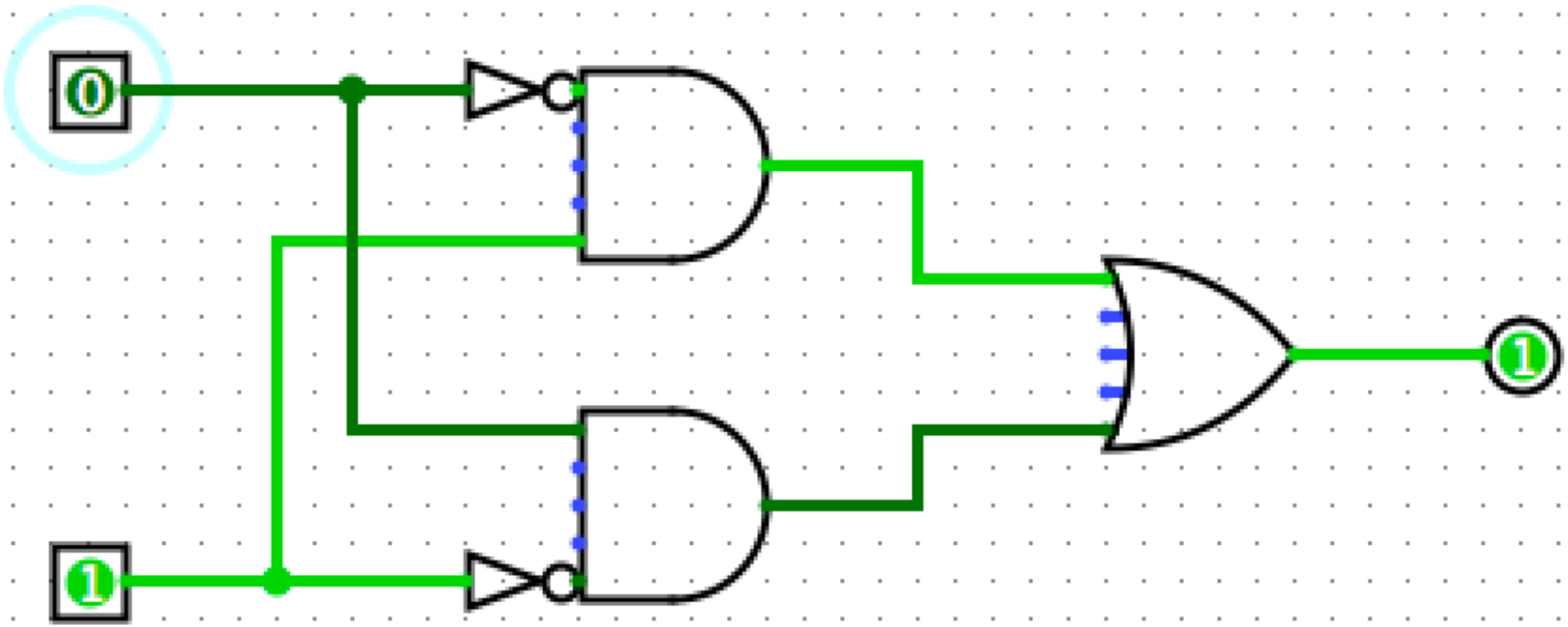
logisim

Logic.circ



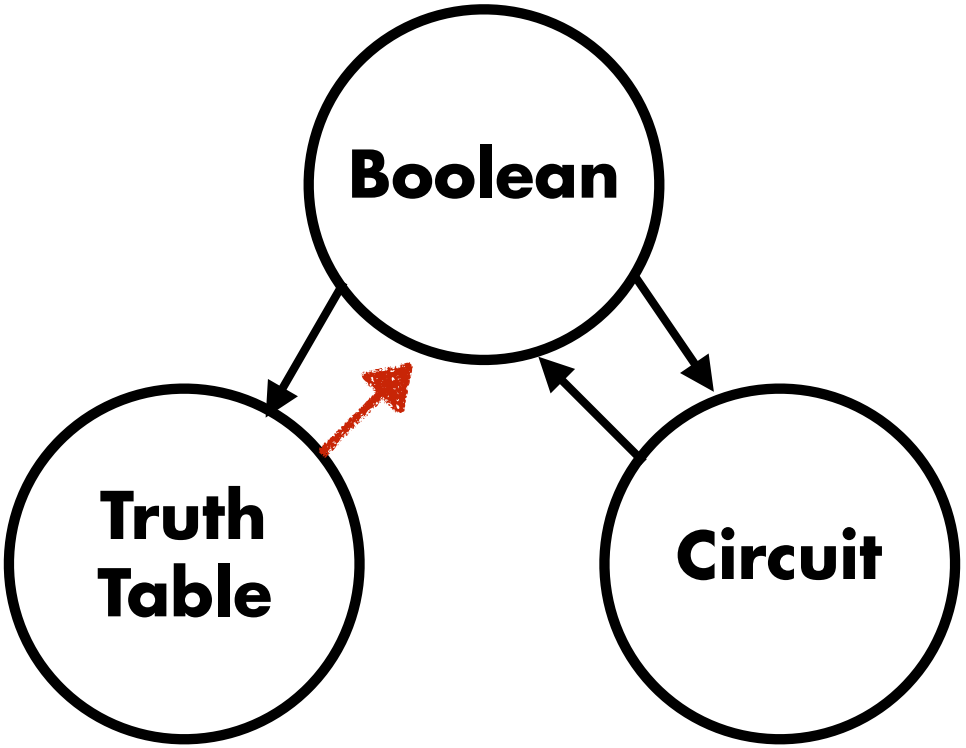
Logisim

Xor.circ



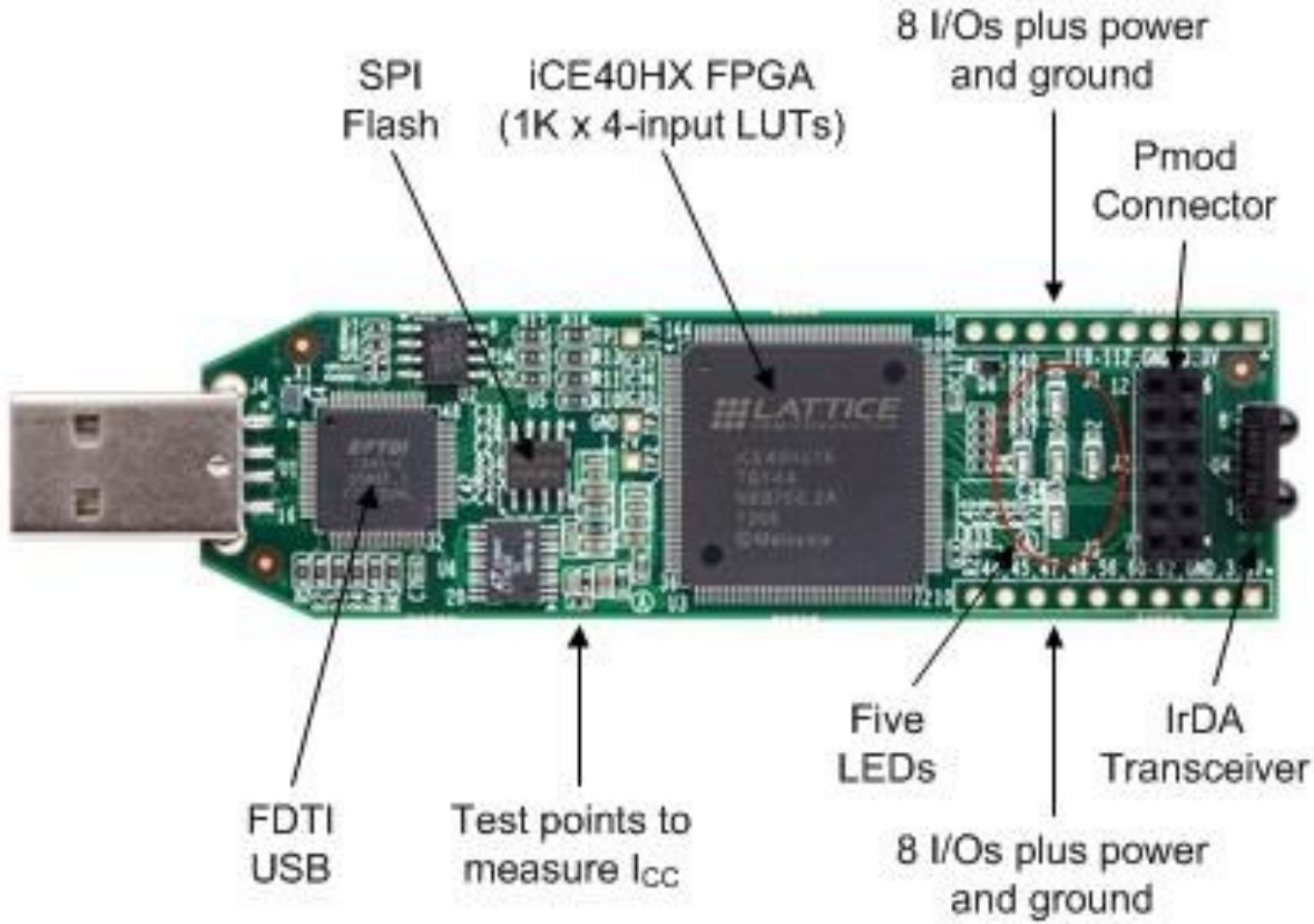
Logisim

Three Representations



Unique

Many formulas (minimum gates, sum of products)

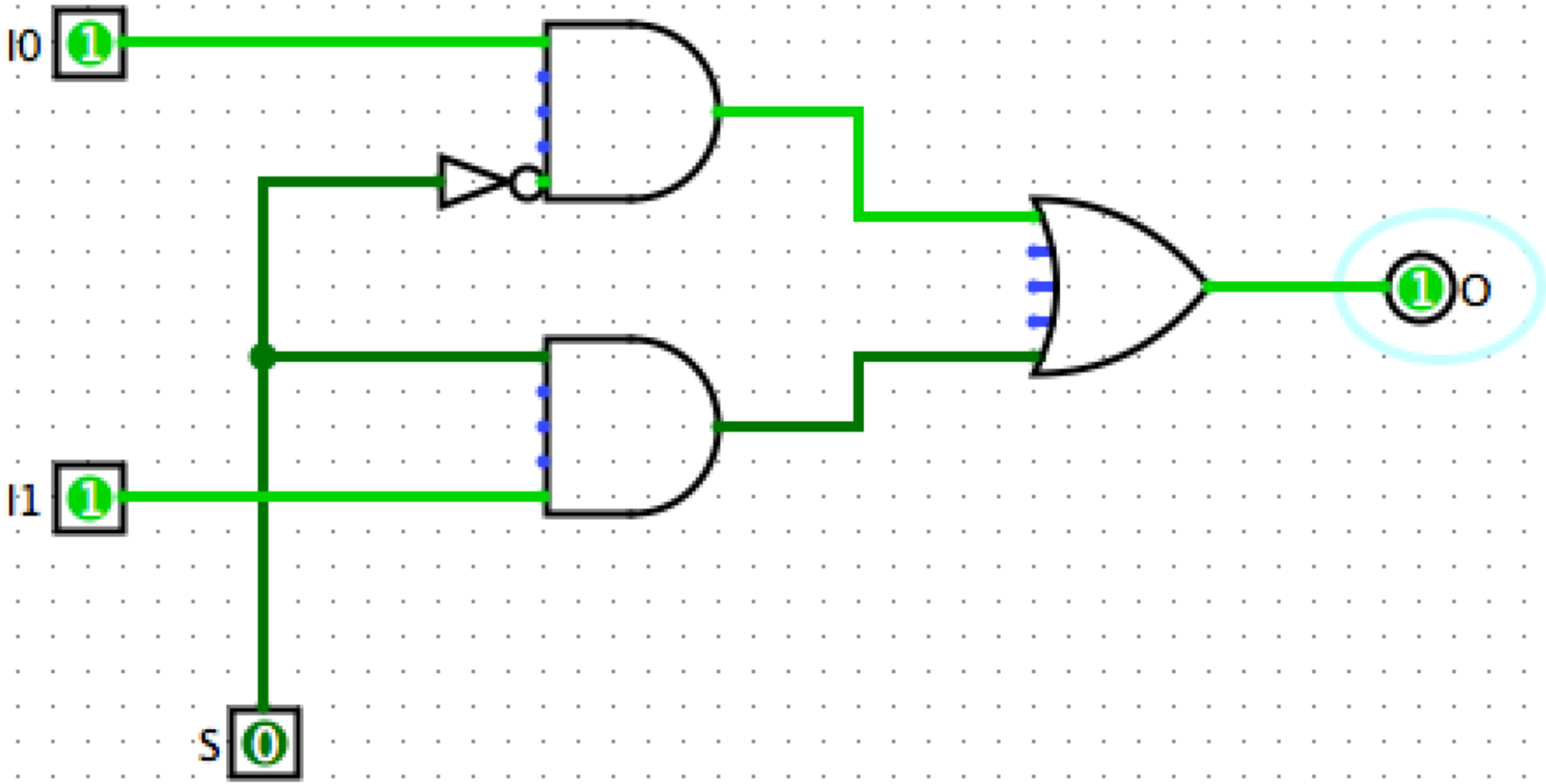

8 I/Os plus power
and ground
SPI
Flash
iCE40HX FPGA
(1K x 4-input LUTs)
Pmod
Connector
LATTICE
Five
LEDs
IrDA
Transceiver
FDTI
USB
Test points to
measure I_{CC}
8 I/Os plus power
and ground

IceStick

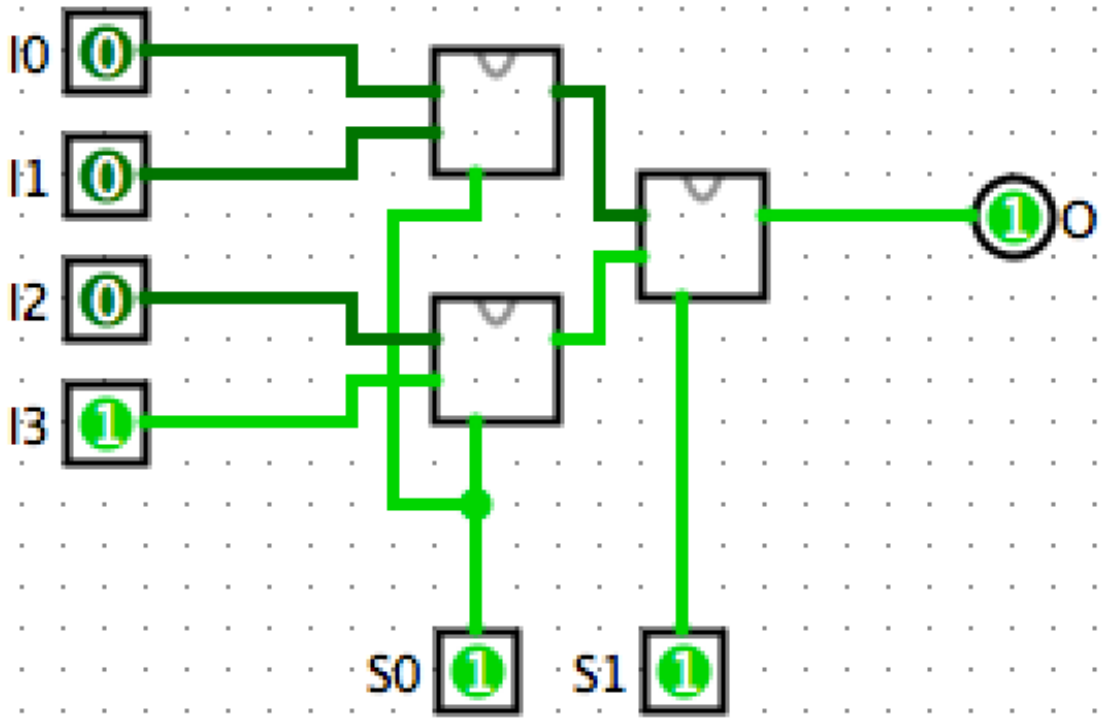
and2.v

xor2.v

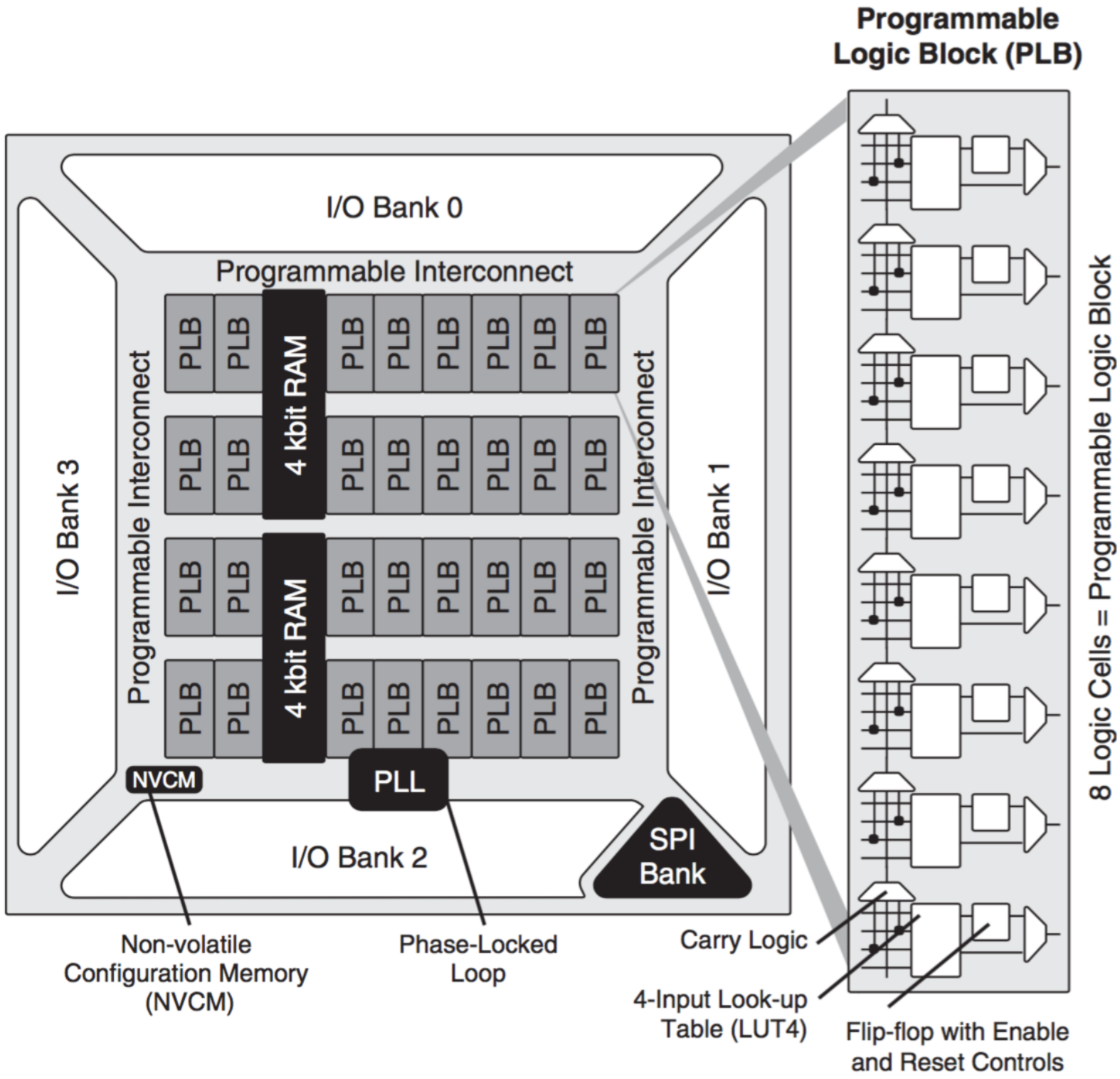
Xor2 -> Mux2

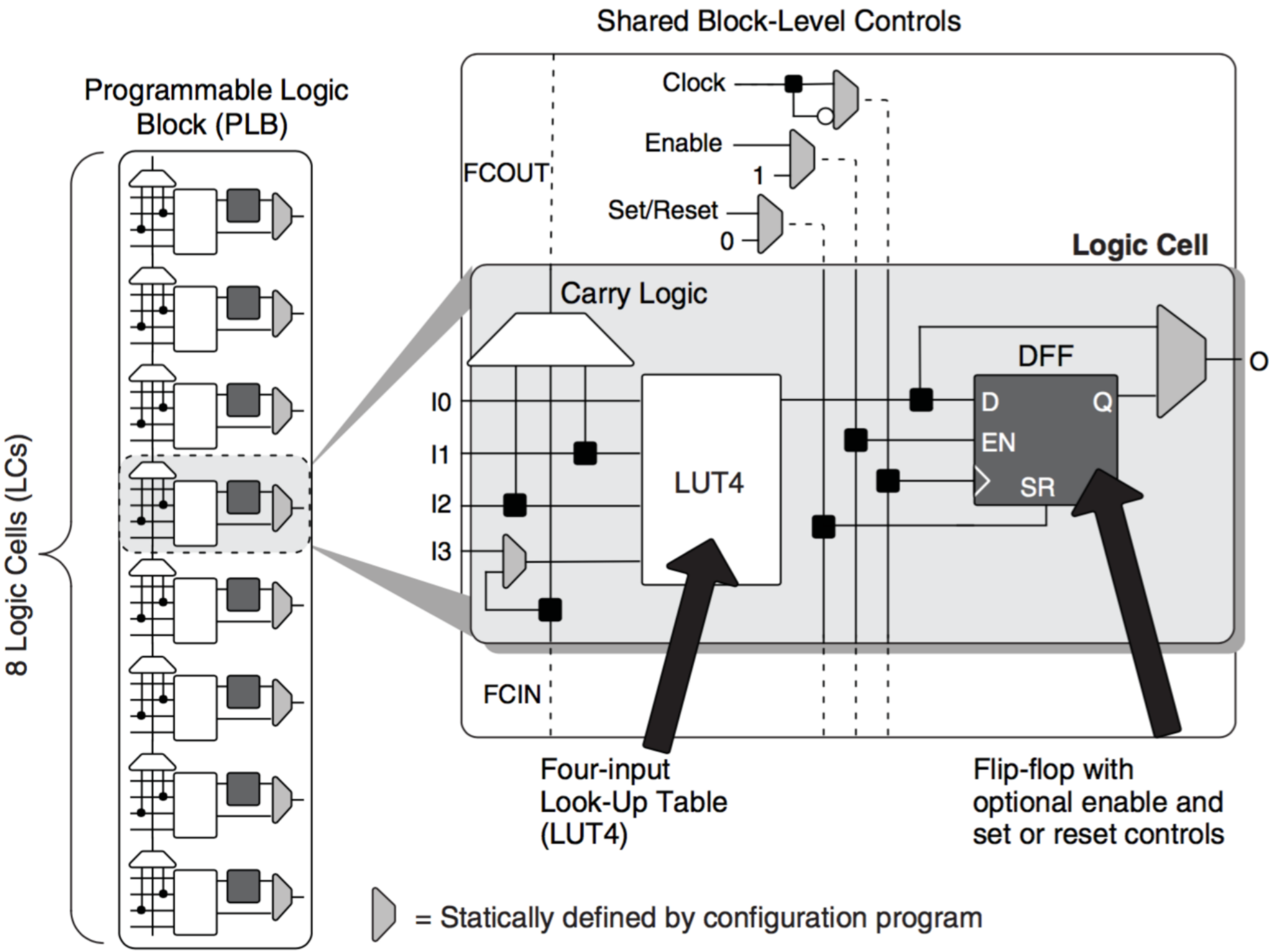


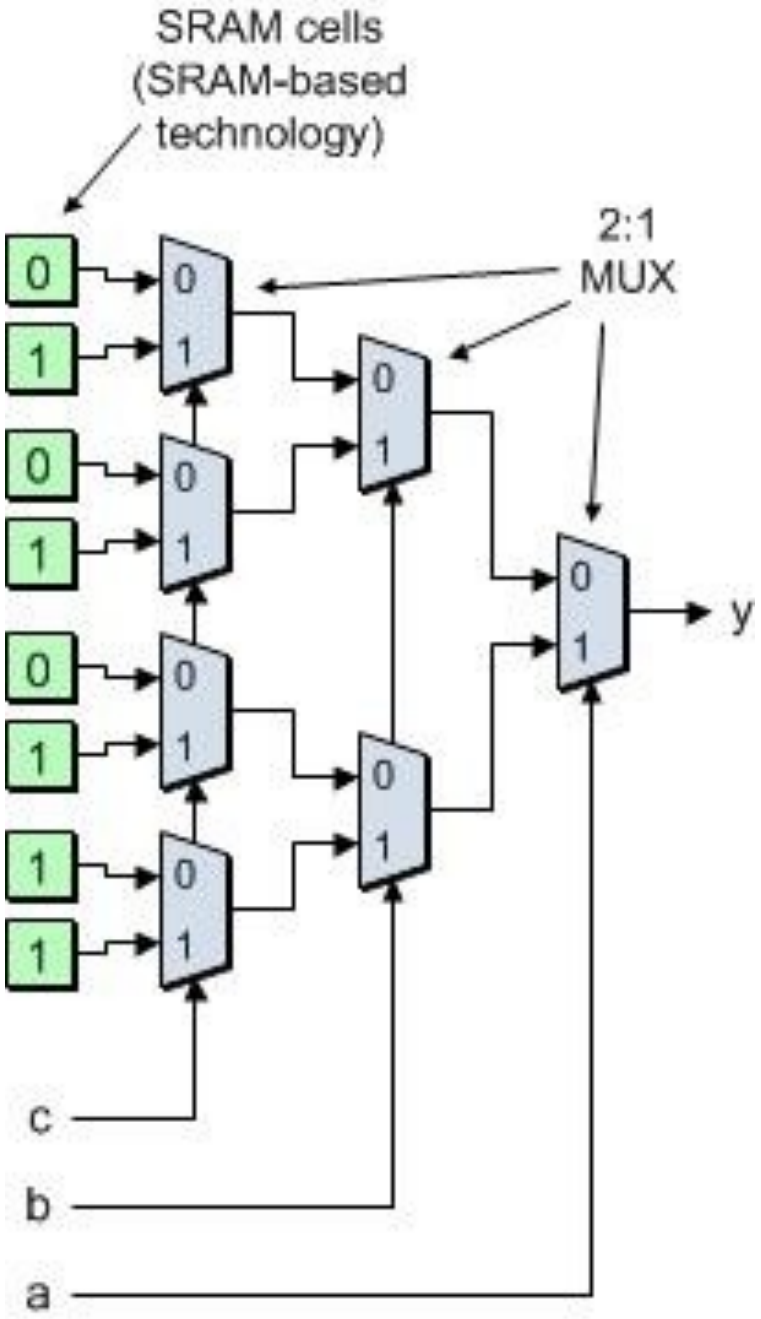
Mux4

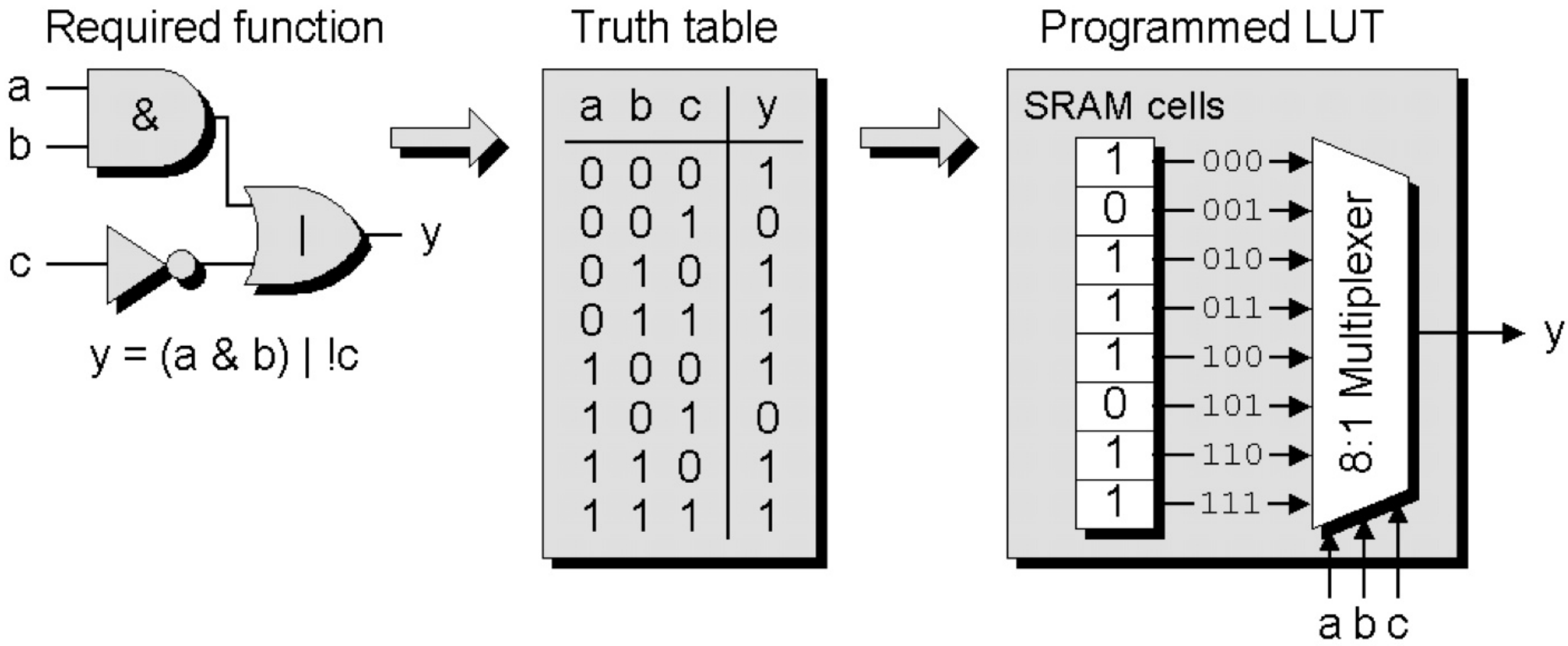


ice40


Programmable
Logic Block (PLB)
I/O Bank 0
Programmable Interconnect
I/O Bank 3
Programmable Interconnect
Programmable Interconnect
I/O Bank 1
PLB
4 kbit RAM
4 kbit RAM
NVCM
PLL
I/O Bank 2
SPI
Bank
8 Logic Cells = Programmable Logic Block
Non-volatile
Configuration Memory
(NVCM)
Phase-Locked
Loop
Carry Logic
4-Input Look-up
Table (LUT4)
Flip-flop with Enable
and Reset Controls


Shared Block-Level Controls
Programmable Logic Block (PLB)
Clock
Enable
1
Set/Reset
0
FCOUT
Logic Cell
Carry Logic
DFF
O
I0
I1
I2
I3
LUT4
D
Q
EN
SR
FCIN
8 Logic Cells (LCs)
Four-input Look-Up Table (LUT4)
Flip-flop with optional enable and set or reset controls
= Statically defined by configuration program


SRAM cells
(SRAM-based
technology)
2:1
MUX
0
1
0
1
0
1
0
1
0
1
0
1
0
1
0
1
0
1
y
c
b
a



LUT4 has 16 entries

lut4.v
and2.v, or2.v, xor2.v

```
// Represent functions as bit patterns
//  see lut.py
I0 = 0b1010101010101010
I1 = 0x1100110011001100
I2 = 0x1111000011110000
I3 = 0x1111111100000000

AND4 = I0 & I1 & I2 & I3
XOR4 = I0 ^ I1 ^ I2 ^ I3
MUX2 = (~I2&I0)|(I2&I1)
```

Combinational Functions

Logic

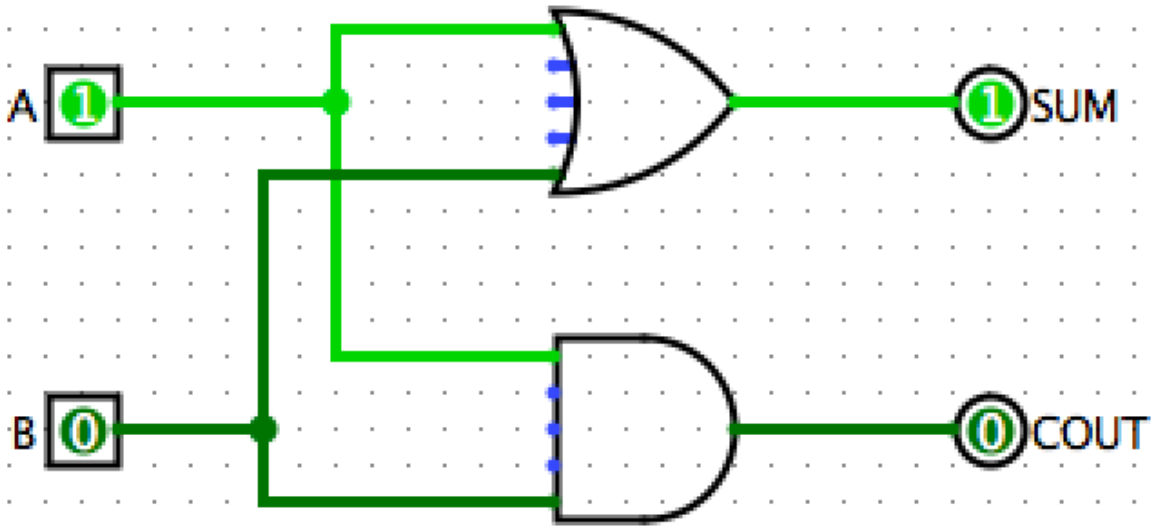
Arithmetic

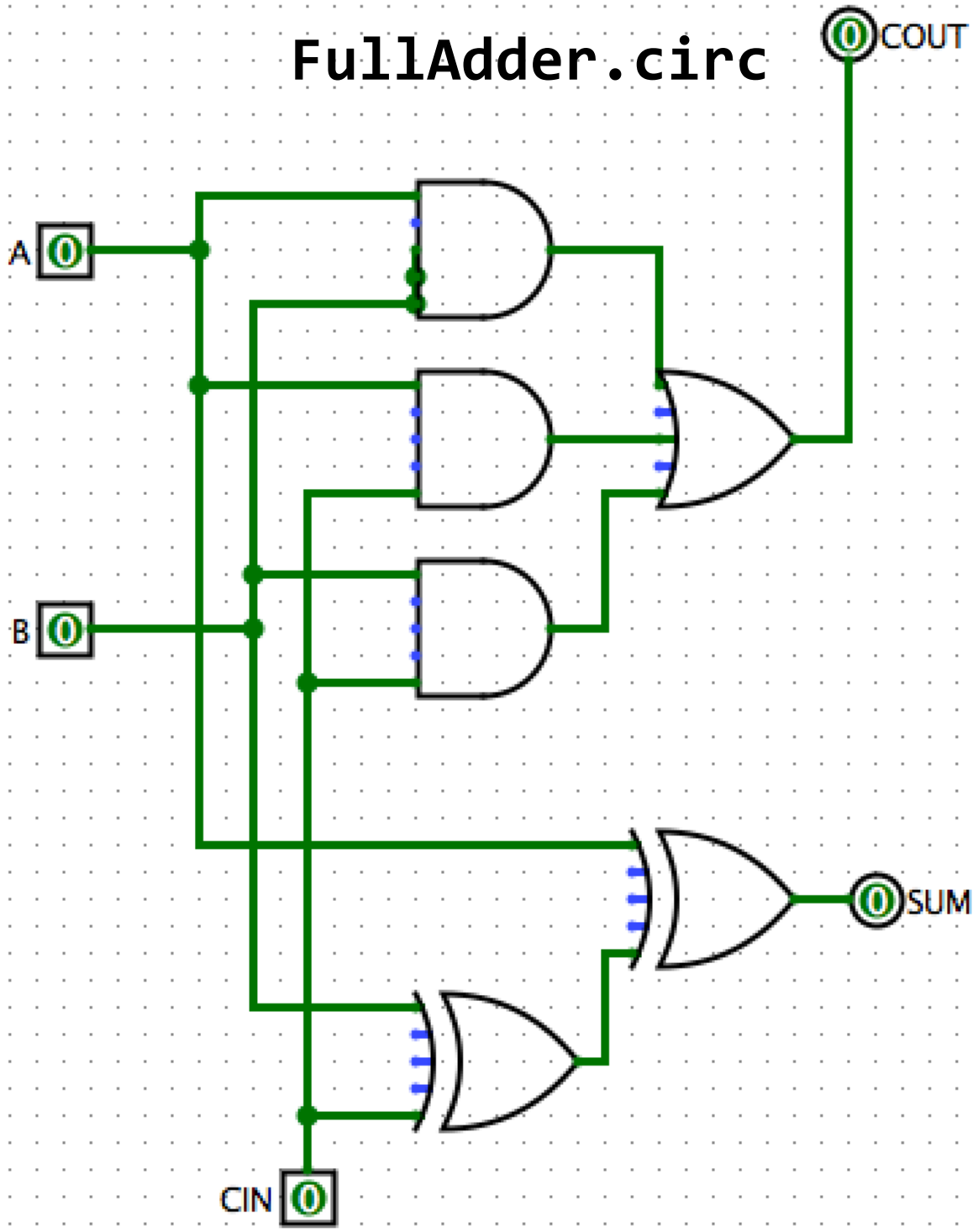
Comparisons

Multiplexers

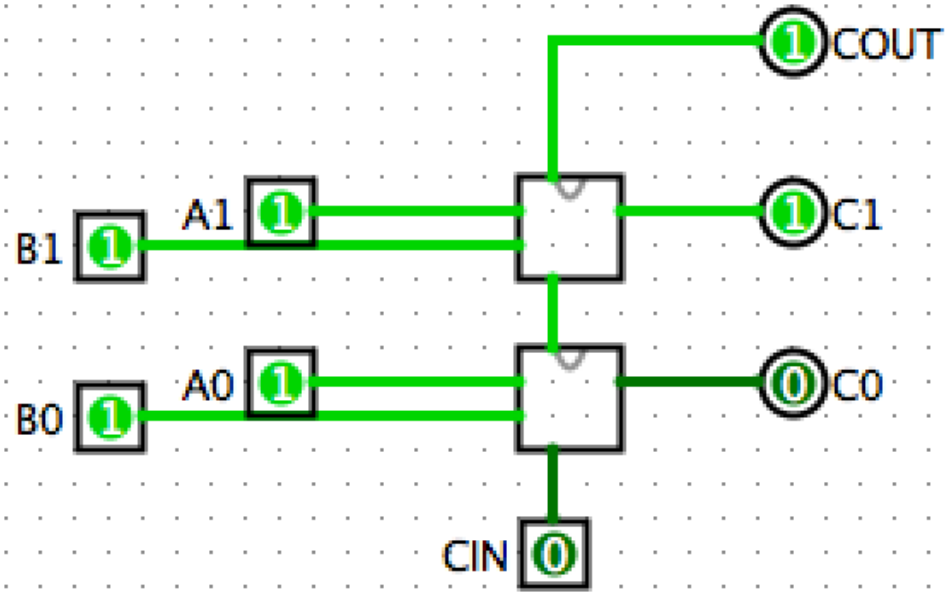
Decoders and Encoders

HalfAdder.circ

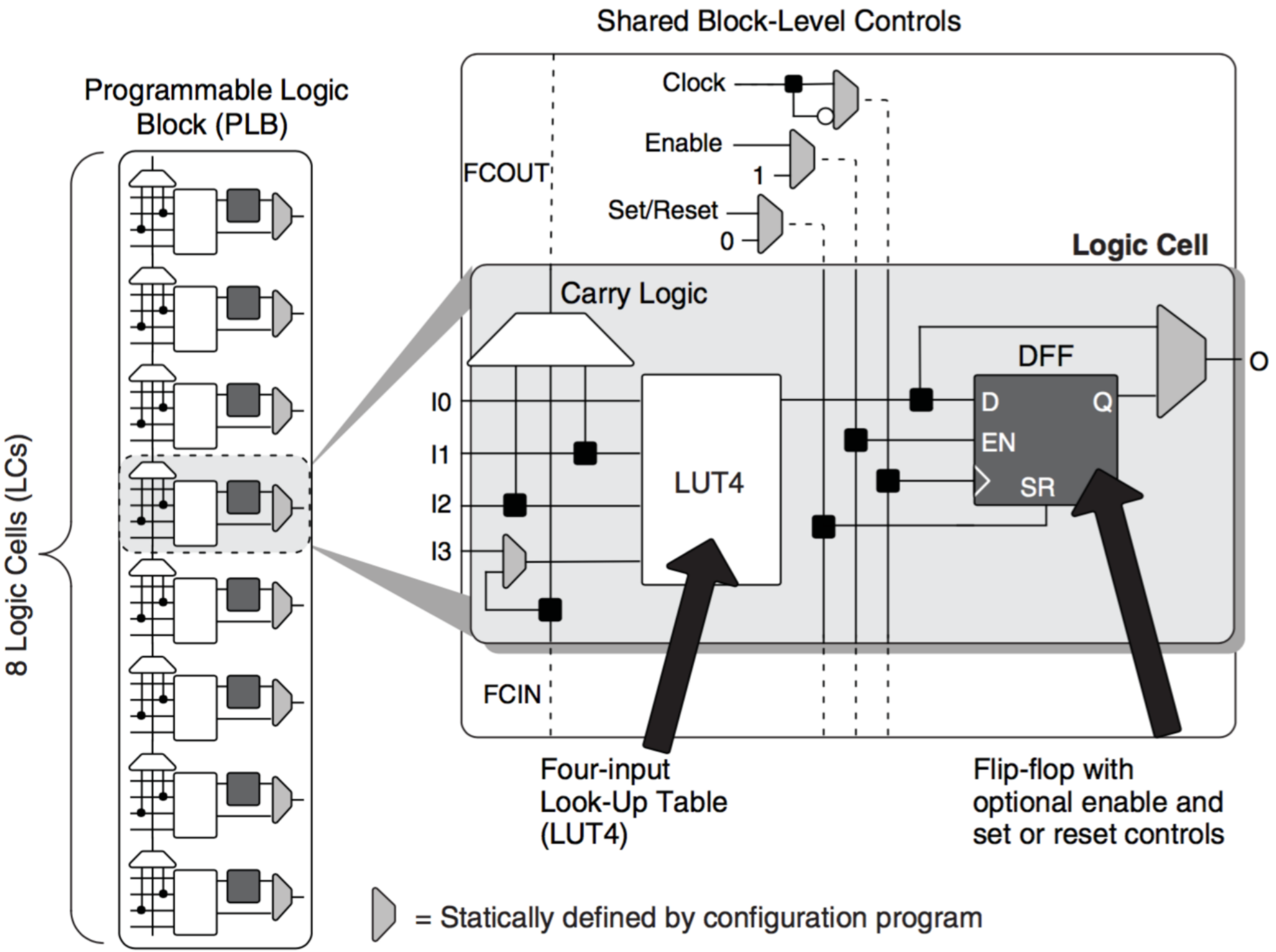



FullAdder.circ
COUT
A
B
SUM
CIN

Add2.circ



fa.v, add4.v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I3
LUT4
D
Q
EN
SR
FCIN
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iceadd4.v

Rules of Comb. Logic

Combinational logic is an expression involving logic gates

1. **All gates should have valid inputs**
2. **No cycles**

2 inverters - 2 valid states

3 inverters - oscillate?

SR Flip Flop