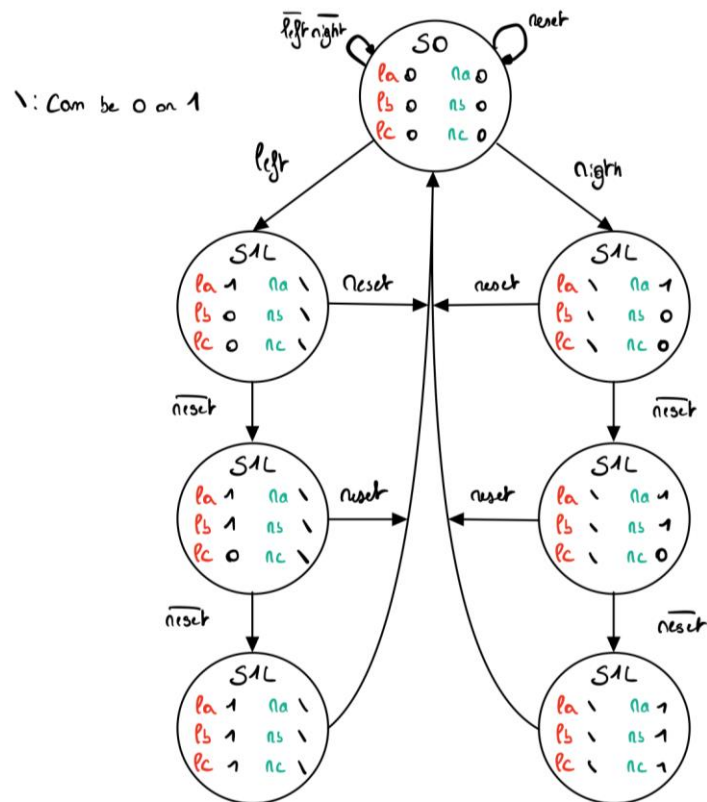


1. FSM design



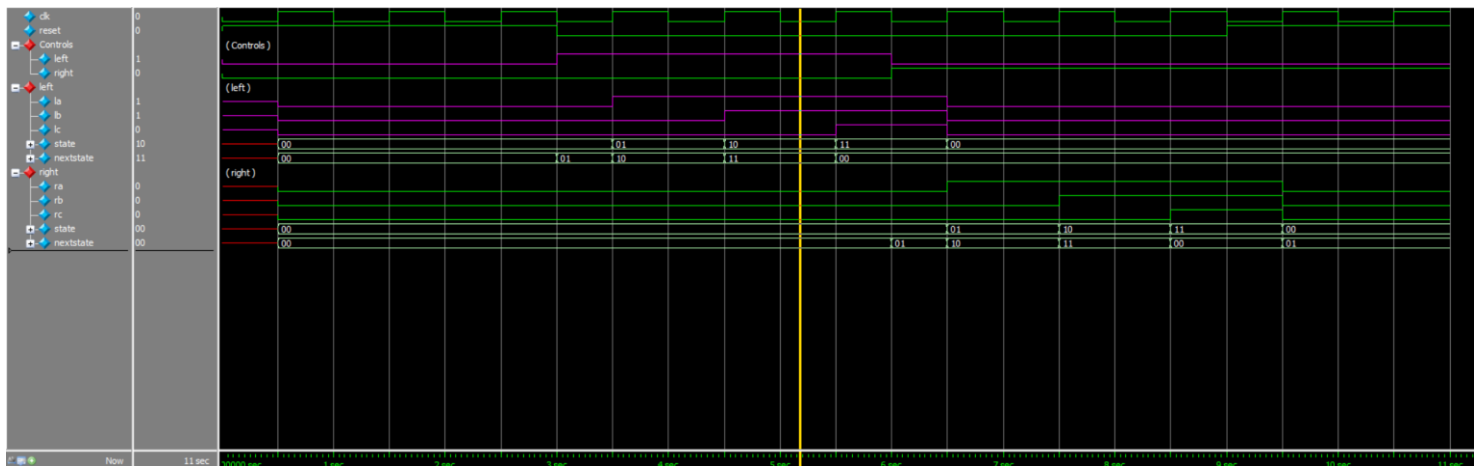
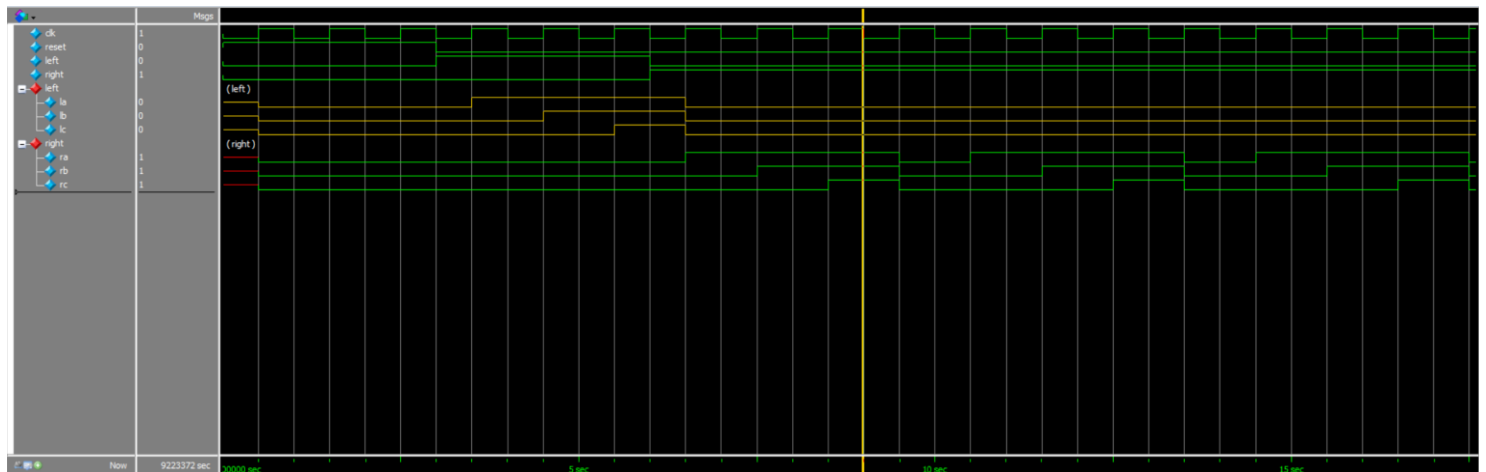
2. Homework_3.sv

```
1 module Homework_3(input logic clk,
2     input logic reset,
3     input logic left, right,
4     output logic la, lb, lc, ra, rb, rc);
5
6 Thunderbird TBleft(
7     .clk(clk),
8     .reset(reset),
9     .active(left),
10    .a(la),
11    .b(lb),
12    .c(lc)
13 );
14
15 Thunderbird TBright(
16     .clk(clk),
17     .reset(reset),
18     .active(right),
19     .a(ra),
20     .b(rb),
21     .c(rc)
22 );
23
24 endmodule
25
26 module Thunderbird(input logic clk,
27     input logic reset,
28     input logic active,
29     output logic a, b, c);
30
31     reg [1:0] state, nextstate;
32
33     parameter S0 = 2'b00;
34     // parameter S1 = 2'b01;
35     // parameter S2 = 2'b10;
36     // parameter S3 = 2'b11;
37
38     always_ff @(posedge clk) begin
39         if (reset) state <= S0;
40         else state <= nextstate;
41     end
42
43     always_comb
44         case (state)
45             S0: nextstate = (active) ? state + 1 : state;
46             default: nextstate = state + 1;
47         endcase
48
49     assign a = state[0] | state[1];
50     assign b = state[1];
51     assign c = state[0] & state[1];
52
53 endmodule
```

3. Homework_3_tb.sv

```
1  `timescale 1ms/1ms
2
3  module testbench_homework_3();
4
5      logic clk, reset, left, right;
6      logic la, lb, lc, ra, rb, rc;
7
8      Homework_3 hw3(
9          .clk(clk),
10         .reset(reset),
11         .left(left),
12         .right(right),
13         .la(la),
14         .lb(lb),
15         .lc(lc),
16         .ra(ra),
17         .rb(rb),
18         .rc(rc)
19     );
20
21     always
22     begin
23         clk = 0;
24         #500;
25         clk = 1;
26         #500;
27     end
28
29     initial begin
30         clk = 0;
31         reset = 1;
32         left = 0;
33         right = 0;
34         #3000
35         reset = 0;
36         left = 1;
37         #3000
38         left = 0;
39         right = 1;
40         #3000
41         reset = 1;
42         #2000
43
44         $stop;
45     end
46
47 endmodule
```

4. Modelsim



5. Registers and I/O pins

I have 2x2 of two bits registers and 10 I/O pins. The registers are used for the current state and the next state which are both two bits and they are used for the right tail lights and left tail so we multiply the number of register by two. For the I/O pins, there is six for the LEDs, two for the clock and for the reset and finally two for the left and right controls.