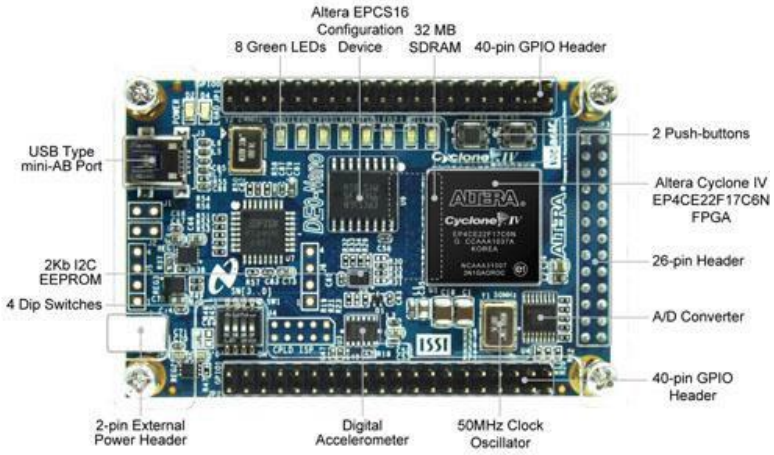
Programming the DE0-Nano Board, Part A

In the previous lab sessions, you used the ModelSim simulator to test the basic aspects of SystemVerilog designs. You also used Quartus to synthesize a real digital circuit from its given description in an HDL language and to perform gate-level simulation. But that remained a purely theoretical exercise and things are now getting more concrete: you are asked to design a circuit that will be implemented in a physical device, in this case a reconfigurable chip called field programmable gate array (FPGA).

In this session, we will cover the following aspects:

- Introduction to the DE0-Nano development board
- Implementation of a circuit design on the DE0-Nano using Quartus
- Programming the FPGA
- Using SignalTap for in-circuit debugging

Introducing the DE0-Nano board



This is the DE0-Nano board from terasIC. It is a fine beast with an Altera **Cyclone IV** FPGA, 32MB SDRAM and a plethora of fancy accessories such as an accelerometer, analog-to-digital converter (ADC), non-volatile memory, LEDs, buttons, and a host of input-outputs (IO) connections.

For this first part we ask you to:

- Read (again) section A.1 to A.4 (included) of the book's appendix A "Digital System Implementation"
- Download the DE0-Nano user manual, have a look at the table of contents and read chapters 1 & 2 to fully discover the board.
- Download as well the associated CD-ROM, which contains many useful tools; check its content (some of it is introduced in the user manual).
- Download Quartus II handbook, read the first two pages of vol. 3, chap. 13 (on Signal Tap) and browse the rest of the chapter.