Homework 8 – ARM Pipelined Processor

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Hazard Module

Put a screenshot of the code (in order to have the color syntax!) for the Hazard Module

```
module hazard(input  logic      clk, reset,
              input  logic    Match_1E_M, Match_1E_W,
Match_2E_M, Match_2E_W, Match_12D_E,
              input  logic    RegWriteM, RegWriteW,
              input  logic    BranchTakenE, MemtoRegE,
              input  logic    PCWrPendingF, PCSrcW,
              output logic [1:0]  ForwardAE, ForwardBE,
              output logic    StallF, StallD,
              output logic    FlushD, FlushE);


// forwarding logic

always_comb begin
  if (Match_1E_M & RegWriteM) ForwardAE = 2'b10; // Mem write
newer info
  else if (Match_1E_W & RegWriteW) ForwardAE = 2'b01; //
Write back older info
  else ForwardAE = 2'b00;

  // Same logic for B operand
  if (Match_2E_M & RegWriteM) ForwardBE = 2'b10;
  else if (Match_2E_W & RegWriteW) ForwardBE = 2'b01;
  else ForwardBE = 2'b00;
end

// stalls and flushes
// Load RAW
//  when an instruction reads a register loaded by the
previous,
//    stall in the decode stage until it is ready
```

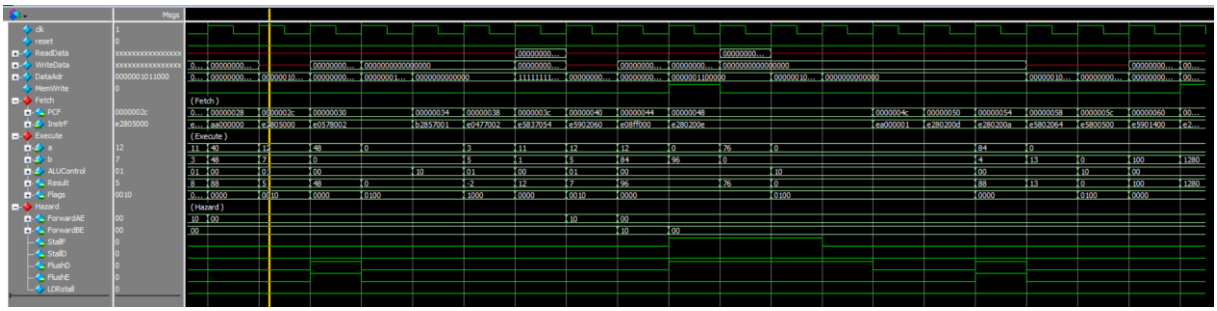
```
// Branch hazard
//  When a branch is taken, flush the incorrectly fetched
instrs
//    from decode and execute stages
// PC Write Hazard
//  When the PC might be written, stall all following
instructions
//  by stalling the fetch and flushing the decode stage
// when a stage stalls, stall all previous and flush next

logic LDRstall;
assign LDRstall = Match_12D_E & MemtoRegE;

assign StallD = LDRstall;
assign StallF = LDRstall | PCWrPendingF;
assign FlushE = LDRstall | BranchTakenE;
assign FlushD = PCSrcW | BranchTakenE | PCWrPendingF;

endmodule
```

Put a screenshot of ModelSim. Check that the waveforms are zoomed out enough that the grader can read your bus values



Put a screenshot of INGInious showing the final result

Homework - SystemVerilog-8

Implement a Pipelined ARM Processor

Votre réponse a passé les tests ! Votre note est de 90.0%. [Soumission #656ce1bc0bcda0a7577e3eec] ×

Great! Your design works just as expected. A penalty of 10 was applied on your score for your previous erroneous submissions.