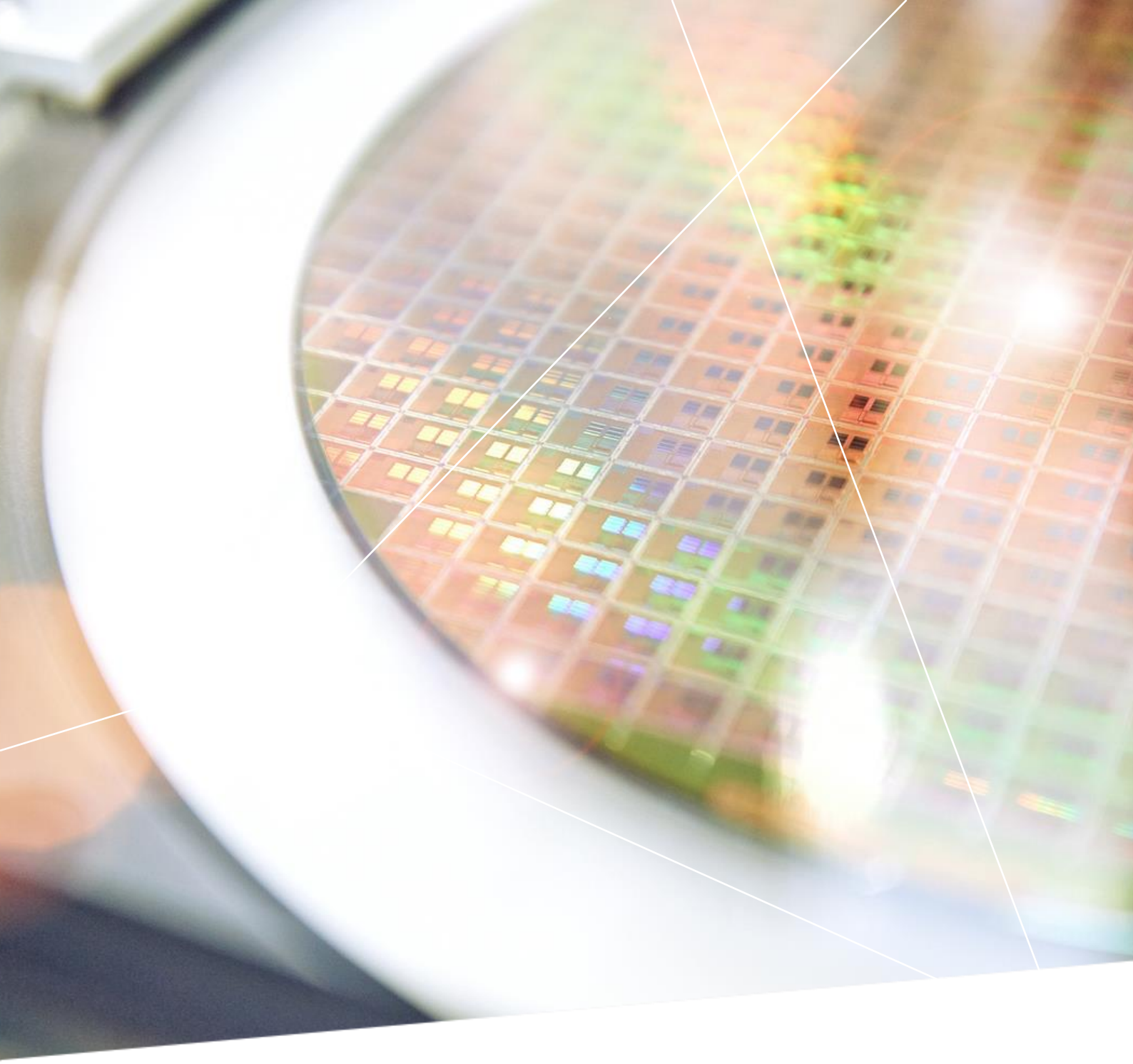

TRAVEO™ T2G Sample Driver Library Release Notes

v8.1.0, March 8, 2024

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Release Notes

TRAVEO™ T2G Sample Driver Library

Release Date: March 8, 2024

Thank you for your interest in Infineon TRAVEO™ T2G Sample Driver Library (SDL) version 8.1.0. This document lists the content of release package.

1 Contents

Infineon provides the Sample Driver Library (SDL) to simplify software development for the TRAVEO™ T2G family of devices.

The release provides the following features:

- Drivers for the extensive set of peripherals supported on TRAVEO™ T2G devices
- The Arm® Cortex Microcontroller Software Interface Standard (CMSIS®) core access header files from the CMSIS v5.9.0 release.
- CMSIS® complaint device header files, startup code (platform initialization) and device configuration header files
- Application Programming Interface Reference Manual specific to every device
- FreeRTOS support for the main application cores
- Examples to evaluate various peripherals
- Multiple build systems via command line using CMake

If you have technical questions, visit Infineon Technical Support for help or contact information.

2 Releases Details

SDL Release	Description - Supported Devices
1.0.0	**PSVP**: TVIIBE1M/a
2.0.0	**PSVP**: TVIIBE1M/a **Silicon**: TVIIBE1M/a
2.0.1	**PSVP**: TVIIBE1M/a **Silicon**: TVIIBE1M/a, Update and Fixes
3.0.0	**PSVP**: TVIIBE1M/b, TVIIBE2M/a, TVIIBH8M/a
4.0.0	**PSVP**: TVIIBE1M/b, TVIIBE2M/a, TVIIBH8M/a, TVIIC2D6M/a
5.0.0	**PSVP**: TVIIBE1M/b, TVIIBE2M/a, TVIIBH8M/a, TVIIC2D6M/a **Silicon**: TVIIBH8M/a 176-TEQFP
6.0.0	**PSVP**: TVIIBE1M/b, TVIIBE2M/a, TVIIBH8M/a, TVIIC2D6M/a **Silicon**: TVIIBH8M/a 320-BGA, TVIIBE2M/a
6.1.0	**PSVP**: TVIIBE1M/b, TVIIBE2M/a, TVIIBH8M/a, TVIIC2D6M/a, **Silicon**: TVIIBE1M/b, TVIIBE2M/a, TVIIBH8M/a 176-TEQFP/320-BGA
6.2.0	**PSVP**: TVIIBE1M/b/c, TVIIBE2M/a/b, TVIIBH8M/a/b, TVIIC2D6M/a, **Silicon**: TVIIBE1M/b/c, TVIIBE2M/a/b, TVIIBH8M/a/b 176-TEQFP/320-BGA, TVIIC2D6M/a 500-BGA Addition of untested TVIIBH4M/a
6.3.0	**PSVP**: TVIIBE1M/b/c, TVIIBE2M/a/b, TVIIBH8Ma/b, TVIIC2D6M/a, **Silicon**: TVIIBE1M/b/c, TVIIBE2Ma/b/c, TVIIBH8M/a/b/c 176-TEQFP/320-BGA, TVIIC2D6M/a 500-BGA, TVIIBH4M/a 176-TEQFP/272-BGA Addition of untested TVIIC2D4M/a, TVIIBE1M/d
6.4.0	**PSVP**: TVIIBE1M/b/c, TVIIBE2M/a/b, TVIIBH8M/a/b, TVIIC2D6M/a, TVIIC2D4M/a **Silicon**: TVIIBE1M/b/c/d, TVIIBE2M/a/b/c, TVIIBH8M/b/c 176-TEQFP/320-BGA, TVIIC2D6M/a 327-/500-BGA, TVIIBH4M/a 176-TEQFP/272-BGA Untested: TVIIBH8M/d, TVIIBE4M/a (new device)
6.5.0	**PSVP**: TVIIBE1M/b/c, TVIIBE2M/a/b, TVIIBH8M/a/b, TVIIC2D6M/a, TVIIC2D4M/a **Silicon**: TVIIBE1M/b/c/d, TVIIBE2M/a/b/c, TVIIBH8M/b/c/d, TVIIC2D6M/a, TVIIBH4M/a/b Untested: TVIIBE512K/d, TVIIBE4M/a (new devices)
6.6.0	**PSVP**: TVIIBE1M/b/c, TVIIBE2M/a/b, TVIIBH8M/a/b, TVIIC2D6M/a, TVIIC2D4M/a **Silicon**: TVIIBE1M/b/c/d, TVIIBE2M/a/b/c, TVIIBH8M/b/c/d, TVIIC2D6M/a, TVIIBH4M/a/b, TVIIBE512K/a, TVIIBE4M/a, TVIIC2D4M/a
7.0.0	**PSVP**: TVIIBE1M/b/c, TVIIBE2M/a/b, TVIIBH8M/a/b, TVIIC2D6M/a/b, TVIIC2D4M/a, TVIIC2D6MDDR/a (Partially tested) **Silicon**: TVIIBE1M/b/c/d, TVIIBE2M/a/b/c, TVIIBH8M/b/c/d, TVIIC2D6M/a, TVIIBH4M/a/b, TVIIBE512K/d, TVIIBE4M/a, TVIIC2D4M/a
7.1.0	**PSVP**: TVIIBE1M/b/c, TVIIBE2M/a/b, TVIIBH8M/a/b, TVIIC2D6M/a/b, TVIIC2D4M/a, TVIIC2D6MDDR/a (Partially tested) **Silicon**: TVIIBE1M/b/c/d, TVIIBE2M/a/b/c, TVIIBH8M/b/c/d, TVIIC2D6M/a/b, TVIIBH4M/a/b, TVIIBE512K/d, TVIIBE4M/a, TVIIC2D4M/a
7.2.0	**PSVP**: TVIIBE1M/b/c, TVIIBE2M/a/b, TVIIBH8M/a/b, TVIIC2D6M/a/b, TVIIC2D4M/a, TVIIC2D6MDDR/a (Partially tested), TVIICE4M/a (Partially tested) **Silicon**: TVIIBE1M/b/c/d, TVIIBE2M/a/b/c, TVIIBH8M/b/c/d, TVIIC2D6M/a/b, TVIIBH4M/a/b, TVIIBE512K/d, TVIIBE4M/a, TVIIC2D4M/a
7.3.0	**PSVP**: TVIIBE1M/b/c, TVIIBE2M/a/b, TVIIBH8M/a/b, TVIIC2D6M/a/b, TVIIC2D4M/a, TVIIC2D6MDDR/a (Partially tested), TVIICE4M/a (Partially tested) **Silicon**: TVIIBE1M/b/c/d, TVIIBE2M/a/b/c, TVIIBH8M/b/c/d, TVIIC2D6M/a/b/c, TVIIBH4M/a/b, TVIIBE512K/d, TVIIBE4M/a, TVIIC2D4M/a/b, TVIICE4M/a
7.4.0	**PSVP**: TVIIBE1M/b/c, TVIIBE2M/a/b, TVIIBH8M/a/b, TVIIC2D6M/a/b, TVIIC2D4M/a, TVIIC2D6MDDR/a (Partially tested), TVIICE4M/a (Partially tested) **Silicon**: TVIIBE1M/b/c/d, TVIIBE2M/a/b/c, TVIIBH8M/b/c/d, TVIIC2D6M/a/b/c, TVIIBH4M/a/b, TVIIBE512K/d, TVIIBE4M/a, TVIIC2D4M/a/b/c, TVIICE4M/a
7.5.0	**PSVP**: TVIIBE1M/b/c, TVIIBE2M/a/b, TVIIBH8M/a/b, TVIIC2D6M/a/b, TVIIC2D4M/a, TVIIC2D6MDDR/a (Partially tested), TVIICE4M/a (Partially tested) **Silicon**: TVIIBE1M/b/c/d, TVIIBE2M/a/b/c, TVIIBH8M/b/c/d, TVIIC2D6M/a/b/c, TVIIBH4M/a/b, TVIIBE512K/d, TVIIBE4M/a, TVIIC2D4M/a/b/c, TVIICE4M/a
7.6.0	**PSVP**: TVIIBE1M/b/c, TVIIBE2M/a/b, TVIIBH8M/a/b, TVIIC2D6M/a/b, TVIIC2D4M/a, TVIIC2D6MDDR/a (Partially tested), TVIICE4M/a (Partially tested) **Silicon**: TVIIBE1M/b/c/d, TVIIBE2M/a/b/c, TVIIBH8M/b/c/d, TVIIC2D6M/b/c, TVIIBH4M/a/b, TVIIBE512K/d, TVIIBE4M/a, TVIIC2D4M/a/b/c, TVIICE4M/a, TVIIC2D6MDDR/a
7.7.0	**PSVP**: TVIIBE1M/b/c, TVIIBE2M/a/b, TVIIBH8M/a/b, TVIIC2D6M/a/b, TVIIC2D4M/a, TVIIC2D6MDDR/a (Partially tested), TVIICE4M/a (Partially tested), TVIIBH16M/a (Partially tested) **Silicon**: TVIIBE1M/b/c/d, TVIIBE2M/a/b/c, TVIIBH8M/b/c/d, TVIIC2D6M/b/c, TVIIBH4M/a/b, TVIIBE512K/d, TVIIBE4M/a, TVIIC2D4M/a/b/c, TVIICE4M/a, TVIIC2D6MDDR/a
7.8.0	**PSVP**: TVIIBE1M/b/c, TVIIBE2M/a/b, TVIIBH8M/a/b, TVIIC2D6M/a/b, TVIIC2D4M/a, TVIIC2D6MDDR/a (Partially tested), TVIICE4M/a (Partially tested), TVIIBH16M/a (Partially tested) **Silicon**: TVIIBE1M/b/c/d, TVIIBE2M/a/b/c, TVIIBH8M/b/c/d, TVIIC2D6M/b/c, TVIIBH4M/a/b, TVIIBE512K/d, TVIIBE4M/a, TVIIC2D4M/a/b/c, TVIICE4M/a, TVIIC2D6MDDR/a
7.9.0	**PSVP**: TVIIBE1M/b/c, TVIIBE2M/a/b, TVIIBH8M/a/b, TVIIC2D6M/a/b, TVIIC2D4M/a, TVIIC2D6MDDR/a (Partially tested), TVIICE4M/a (Partially tested), TVIIBH16M/a (Partially tested) **Silicon**: TVIIBE1M/b/c/d, TVIIBE2M/a/b/c, TVIIBH8M/b/c/d, TVIIC2D6M/b/c, TVIIBH4M/a/b, TVIIBE512K/d, TVIIBE4M/a, TVIIC2D4M/a/b/c, TVIICE4M/a, TVIIC2D6MDDR/a, TVIIBH16M/a
8.0.0	**PSVP**: TVIIBE1M/b/c, TVIIBE2M/a/b, TVIIBH8M/a/b, TVIIC2D6M/a/b, TVIIC2D4M/a, TVIIC2D6MDDR/a (Partially tested), TVIICE4M/a (Partially tested), TVIIBH16M/a (Partially tested) **Silicon**: TVIIBE1M/b/c/d, TVIIBE2M/a/b/c, TVIIBH8M/b/c/d, TVIIC2D6M/b/c, TVIIBH4M/a/b, TVIIBE512K/d, TVIIBE4M/a, TVIIC2D4M/a/b/c, TVIICE4M/a, TVIIC2D6MDDR/a, TVIIBH16M/a
8.1.0	**PSVP**: TVIIBE1M/b/c, TVIIBE2M/a/b, TVIIBH8M/a/b, TVIIC2D6M/a/b, TVIIC2D4M/a, TVIIC2D6MDDR/a (Partially tested), TVIICE4M/a (Partially tested), TVIIBH16M/a (Partially tested) **Silicon**: TVIIBE1M/b/c/d, TVIIBE2M/a/b/c, TVIIBH8M/b/c/d, TVIIC2D6M/b/c, TVIIBH4M/a/b, TVIIBE512K/d, TVIIBE4M/a, TVIIC2D4M/a/b/c, TVIICE4M/a, TVIIC2D6MDDR/a, TVIIBH16M/a

3 Device Support

The SDL includes:

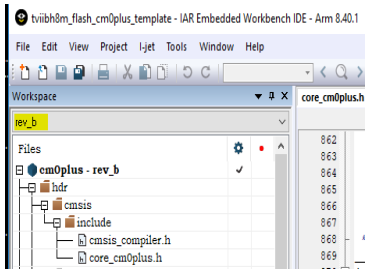
- Device-specific header files that provide a complete definition of all peripheral registers and bits in the device.
- CMSIS-compliant startup code to initialize the system after device reset, and transfer the code execution to “main ()”.
- Linker files for each supported device and toolchain (IAR/GHS, DIAB for TVIIBE1M)
- SVD files with a detailed description of peripherals, registers, fields, and bit values.
- GRD files to support register level debugging in GHS
- FreeRTOS support for all devices (Tested only on TVIIBE2M and TVIIC2D4M devices)

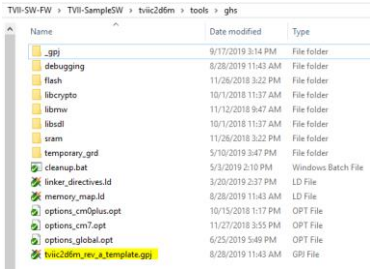
Table 1: Device RTL and MPN Revision Mapping

Device	Device RTL Revision	Datasheet MPN/SDL Revision
TVIIBE1M	B0	B
	B1	C
	B2	D
TVIIBE2M	A0	A
	A1	B
	A2	C
TVIIBH8M	B0	B
	B1	C
	B2	D
TVIIC2D6M	B0	B
	B1	C
TVIIBH4M	A0	A
	A1	B
TVIIC2D4M	A0	A
	A1	B
	A2	C
TVIIBE4M	A0	A
TVIIBE512K	B2	D
TVIIC2D6MDDR	A0	A
TVIICE4M	A0	A
TVIIBH16M	A0	A

4 Project configuration

1. Choose proper build and then perform the compilation in IAR. In case of GHS, device revision is part of the main project file.





2. **TVIIBE1M: Rev_B, Rev_C, Rev_D**
   a. PSVP 176-LQFP: CY_USE_PSVP=1 and either CYT2B78XAX (176-LQFP package fixed for PSVP and no other package supported)
   b. Silicon 176-LQFP: CY_USE_PSVP=0 and either CYT2B78XAX
   c. Supports both REV *A and REV *C CPU boards through the selection of CPU_BOARD_REVA or CPU_BOARD_REVC respectively
   d. Rev_D has initial 2KB of SRAM reserved for internal purposes, and for other revisions last 6KB is reserved
3. **TVIIBE2M: Rev_A, Rev_B, Rev_C**
   a. PSVP: CY_USE_PSVP=1 and either CYT2B98XAX (176-LQFP package fixed for PSVP and no other package supported)
   b. Silicon 176-LQFP: CY_USE_PSVP=0 and either CYT2B98XAX
   c. Supports both REV *A and REV *C CPU boards through the selection of CPU_BOARD_REVA or CPU_BOARD_REVC respectively
   d. Rev_C has initial 2KB of SRAM reserved for internal purposes, and for other revisions last 6KB is reserved
4. **TVIIBH8M: Rev_B, Rev_C, Rev_D**
   a. Defines CY_CORE_CM7_0 or CY_CORE_CM7_1 for either core CM7_0 or CM7_1 selection
   b. PSVP 320-BGA: CY_USE_PSVP=1 and either CYT4BFCCXX (320-BGA package fixed for PSVP and no other package supported)
   c. Silicon 320-BGA: CY_USE_PSVP=0 and either CYT4BFCCXX
      (IAR linker “use_psvp = 0” in its ICF file, GHS relies on global definition CY_USE_PSVP=0)
   d. Silicon 176-TEQFP: CY_USE_PSVP=0 and either CYT4BF8CXX / CYT4A0100S
      (IAR linker “use_psvp = 0” in its ICF file, GHS relies on global definition CY_USE_PSVP=0)
   e. Rev_C onwards has initial 2KB of SRAM reserved for internal purposes, and for other revisions last 6KB is reserved
   f. Rev_A support is removed
5. **TVIIC2D6M: Rev_B, Rev_C**
   a. PSVP: CY_USE_PSVP=1 and tviic2d6m, CYT4DNDBHS
      (Rev_B only in PSVP, SMIF/ETH/LIN modules have not been tested due to limitations in the bitfile)
   b. Silicon 327-BGA: CY_USE_PSVP=0 and tviic2d6m, CYT4DNJBHS
      (IAR linker “use_psvp = 0” in its ICF file, GHS relies on global definition CY_USE_PSVP=0)
   c. Defines CY_CORE_CM7_0 or CY_CORE_CM7_1 for either core CM7_0 or CM7_1 selection
   d. Rev_B onwards has initial 2KB of SRAM reserved for internal purposes, and for other revisions last 6KB is reserved
   e. Rev_B, 500-BGA support removed. Only 327-BGA devices are supported.
   f. Rev_A, support removed.
6. **TVIIBH4M: Rev_A, Rev_B**
   a. Defines CY_CORE_CM7_0 or CY_CORE_CM7_1 for either core CM7_0 or CM7_1 selection

b. Silicon 272-BGA: CY_USE_PSVP=0 and either CYT4BBBCEX

(IAR linker “use_psvp = 0” in its ICF file, GHS relies on global definition CY_USE_PSVP=0)

c. Silicon 176-TEQFP: CY_USE_PSVP=0 and either CYT4BB8CEX

(IAR linker “use_psvp = 0” in its ICF file, GHS relies on global definition CY_USE_PSVP=0)

d. Initial 2KB of SRAM reserved for internal purposes

e. CYT3BB support added

7. **TVIIC2D4M: Rev_A, Rev_B, Rev_C**

a. PSVP: CY_USE_PSVP=1 and tviic2d4m, CYT3DLBBHS.

b. Silicon 216-TEQFP: CY_USE_PSVP=0 and CYT3DLABAS / CYT3DLABBS / CYT3DLABCS / CYT3DLABDS / CYT3DLABES / CYT3DLABFS / CYT3DLABGS / CYT3DLABHS

(IAR linker “use_psvp = 0” in its ICF file, GHS relies on global definition CY_USE_PSVP=0)

c. Initial 2KB of SRAM reserved for internal purposes

8. **TVIIBE4M: Rev_A**

a. Silicon: 176-LQFP: CY_USE_PSVP=0 and either CYT2BL8XAX / CYT2BL7XAX / CYT2BL5XAX / CYT2BL4XAX / CYT2BL3XAX

b. Rev_A has initial 2KB of SRAM reserved for internal purposes

9. **TVIIBE512K: Rev_D**

a. Silicon: 100-LQFP: CY_USE_PSVP=0 and either CYT2B65BAS / CYT2B65BAE / CYT2B65CAS / CYT2B65CAE

b. Rev_D has initial 2KB of SRAM reserved for internal purposes

10. **TVIIC2D6MDDR: Rev_A**

a. PSVP: CY_USE_PSVP=1, Device CYT4ENDBAS, MCU revision as CY_MCU_rev_a

b. Silicon 500-BGA: CY_USE_PSVP=0, Device as CYT4ENDBAS or CYT4ENDBCS or CYT4ENDBES or CYT4ENDBGS or CYT4ENDBJS or CYT4ENDBLS or CYT4ENDBNS or CYT4ENDBQS, MCU revision CY_MCU_rev_a, EVK revision CY_500BGA_EVK_rev_a

(IAR linker “use_psvp = 0” in its ICF file, GHS uses global definition CY_USE_PSVP=0)

c. Rev_A has initial 2KB of SRAM reserved for internal purposes

11. **TVIICE4M: Rev_A**

a. PSVP: CY_USE_PSVP=1, Device CYT2CL8BAS, MCU revision as CY_MCU_rev_a

b. Silicon 176-LQFP: CY_USE_PSVP=0 and CYT2CL8BAS (IAR linker “use_psvp = 0” in its ICF file, GHS relies on global definition CY_USE_PSVP=0), MCU revision CY_MCU_rev_a, EVK revision CY_176LQFP_EVK_REV_A

c. Rev_A has initial 2KB of SRAM reserved for internal purposes

12. **TVIIBH16M: Rev_A**

a. PSVP: CY_USE_PSVP=1, Device CYT6BJCCJS, MCU revision as CY_MCU_rev_a, Only IAR supports all core download and debug. GHS supports only CM0+/CM7_0/CM7_1.

b. Silicon 320-BGA: CY_USE_PSVP=0 and CYT6BJCDHE (IAR linker “use_psvp = 0” in its ICF file, GHS relies on global definition CY_USE_PSVP=0), MCU revision CY_MCU_rev_a, EVK revision CY_320BGA_EVK_rev_a

c. Rev_A has initial 2KB of SRAM reserved for internal purposes

Note:

- ‘X’ in the device MPN above signifies different package variants or temperatures supported. Please check the device specific datasheet for more details.
- In all devices, last 6kB of SRAM cannot be used for retention.
- SRAM reserved for internal purposes is NOT available for the user.

Table 2: Device Memory Map

Device	Type	Brief Device Description
TVIIBE1M	PSVP	Dual core CM0+/CM4, Flash 1088-KB, SRAM 128-KB, Work flash 96-KB
	176-LQFP	Dual core CM0+/CM4, Flash 1088-KB, SRAM 128-KB, Work flash 96-KB
TVIIBE2M	PSVP	Dual core CM0+/CM4, Flash 2112-KB, SRAM 256-KB, Work flash 128-KB
	176-LQFP	Dual core CM0+/CM4, Flash 2112-KB, SRAM 256-KB, Work flash 128-KB
TVIIBH8M	PSVP	Triple core CM0+/CM7_0/CM7_1, Flash 2048-KB, SRAM 1024-KB, Work flash 256-KB
	320-BGA 176-TEQFP	Triple core CM0+/CM7_0/CM7_1, Flash 8384-KB, SRAM 1024-KB, Work flash 256-KB
TVIIC2D6M	PSVP	Triple core CM0+/CM7_0/CM7_1, Flash 1024-KB, SRAM 1024-KB, Work flash 128-KB
	327-BGA	Triple core CM0+/CM7_0/CM7_1, Flash 6336-KB, SRAM 640-KB, Work flash 128-KB
TVIIBH4M	176-TEQFP 272-BGA	Triple core CM0+/CM7_0/CM7_1, Flash 4160-KB, SRAM 768-KB, Work flash 256-KB
TVIIC2D4M	216-TEQFP	Dual core CM0+/CM7_0, Flash 4160-KB, SRAM 384-KB, Work flash 128-KB
TVIIBE4M	176-LQFP	Dual core CM0+/CM4, Flash 4160-KB, SRAM 512-KB, Work flash 128-KB
TVIIBE512K	100-LQFP	Dual core CM0+/CM4, Flash 576-KB, SRAM 64-KB, Work flash 64-KB
TVIIC2D6MDDR	PSVP	Triple core CM0+/CM7_0/CM7_1, Flash 1024-KB, SRAM 1024-KB, Work flash 128-KB
	500-BGA	Triple core CM0+/CM7_0/CM7_1, Flash 6336-KB, SRAM 640-KB, Work flash 128-KB
TVIICE4M	PSVP	Dual core CM0+/CM4, Flash 1024-KB (Split), SRAM 512-KB, Work flash 128-KB
	176-LQFP	Dual core CM0+/CM4, Flash 4160-KB, SRAM 512-KB, Work flash 128-KB
TVIIBH16M	PSVP	Five cores CM0+/CM7_0/CM7_1/CM7_2/CM7_3, Flash 2560-KB, SRAM 2048-KB, Work flash 256-KB
	320-BGA	Five cores CM0+/CM7_0/CM7_1/CM7_2/CM7_3, Flash 16768-KB, SRAM 2048-KB, Work flash 512-KB

5 Supported Toolchains

- Green Hills MULTI: 7.1.4, Compiler: 2017.1.4, Probe Version: 5.6.5
    - *DEVELOPMENT AUTOBUILD 5.6 634260/AB as of patch #12996, or higher*
    - *Flash loaders are not available as part of SDL, will be provided on case by case basis through Cypress Customer Support (Patches are of size in GBs)*
- IAR Embedded Workbench for ARM 8.22.1 (EWARM-CD-8221-xxxxx.exe), IAR I-Jet Debugger
    - *Supported only for tviic2d4m, tviic2d6m, and tviic2d6mddr devices for flash projects*
    - *Flash loaders are available at the location*
        - *"\misc\tools\iar\IAR_EWARM_8222_FlashLoader_Patch_TraveoII"*
- IAR Embedded Workbench for ARM 9.30.1 (EWARM-9301-50054.exe), IAR I-Jet Debugger
    - *This EWARM revision is NOT functional safety complaint*
    - *Flash loaders are available at the location*
        - *"\misc\tools\iar\IAR_EWARM_9301_FlashLoader_Patch_TraveoII.7z"*
    - *Go through "\misc\tools\iar\Readme_Patch.txt" to update the TRAVEO™ T2G patch for IAR.*
- Windriver DIAB revision diab-5.9.8.1 (Right now only for TVIIBE1M, later will be extended to all devices. Only via command line-based system via CMake)
- Arm® GNU GCC revision 11.3, rel1 (via CMake)

6 Peripheral Drivers

The SDL provides a high-level API to configure, initialize, and use a peripheral driver. The drivers are designed for peripheral IP blocks, therefore work on all TRAVEO™ T2G products that instantiate that IP block.

Following driver (src/driver) modules have been tested and the respective examples are available in the src/examples folder. Some of these drivers/mw are available in the common/src/drivers or common/src/mw which are common across dies, and some are specific to a particular die is available in the die specific drivers/mw say, tviibh8m/src/drivers or tviibh8m/src/mw.

Table 3: Drivers

Driver	Description	API Functionality
ADC	Analog to Digital Converter	Manage ADC operations
Audioss	Sound Subsystem for I^2S, DAC, Mixer, PWM, SG, TDM (TVIIC devices only)	Manages I2S, Audio DAC, Mixer, PCM-PWM, Sound Generator, TDM as part of sound subsystem
AXIDMA	M-DMA on AXI bus	Memory to memory transfer over AXI bus
CAN FD	Controller Area Network Flexible Data-Rate	Manages Classic and FD operations
CPU	CPU driver	Enables core of CPU specific features
CRYPTO	Cryptographic Operations	Perform cryptographic operations on user-designated data. Available as libraries.
CXPI	Clock eXtension Peripheral Interface	Manages communication over CXPI interface
DAC	Audio DAC	Provides global DAC defines and API function definitions
DMA	Direct Access Memory (AHB bus)	Perform memory-to-memory (M-DMA) and peripheral-to-memory (P-DMA) (and vice versa) operations
EVTGEN	Event Generator	Performs event generation for interrupts and triggers in active power mode
FLASH	Flash Memory	Manage code/work flash memory operations
FLEXRAY	FlexRay Interface	Manages FlexRay communication
FPDLINK	FDP-Link or LVDS	Analog LVDS video driver
GPIO	General Purpose I/O Ports	Configure and access device input/output pins
I^2S	Inter-IC Sound (TVIIBH4M/8M all revisions)	Manage Inter-IC Sound. I2S is used to send digital audio streaming data to external I2S devices, such as audio codecs or simple DACs. It can also receive digital audio streaming data.
IPC	Inter Process Communication	Manage data transfer between CPUs or processes in a device
LIN	Local Interconnect Network	Provides master and slave data transfer capabilities
LVD	Low Voltage Detection	Provides LVD capabilities
LPDDR4	Low-Power DDR SDRAM	Provides basic capabilities to access DDR memories
MCWDT	Multi-counter Watchdog timer	Provides control and status capabilities
MIPI-CSI2	Video Input	Manage and control analog video inputs
Mixer	Audio Mixer for I2S, PWM etc.	Provides global Mixer defines and API function definitions
MPU	Memory Protection Unit	Manages the configuration of MPU
PROT	Memory and Peripheral Protection	Manage the MPU, Shared MPU (SMPU), and Peripheral Protection Unit (PPU)
PWM	Audio Pulse Width Modulation	PWM interface drives PWM output lines and their complementary output lines.
SCB	Serial Communication Block	Manage serial communication as EZI2C, I2C, SPI, or UART
SEGLCD	Segment LCD	Manage Segment LCD interfaces
SD_HOST	Secure Digital Host Controller	Manages SD and eMMC devices
SG	Audio Sound Generator	Helps produce PWM tone (frequency) and amplitude (volume) signals
SMART IO	Smart I/O	Configure and access the Smart I/O hardware present between the GPIOs (pins) and HSIOMs (pin multiplexers) on select device ports. It can be used to perform simple logic operations on peripheral and GPIO signals at the GPIO port
SMIF	Serial Memory Interface	SPI-based communication interface for interfacing external memory devices to T2G. The SMIF supports Octal-SPI, Dual Quad-SPI, Quad-SPI, DSPI, and SPI. This interface also supports xSPI interfaces like HyperRAM and HyperFlash devices.
SROM	Internal SROM driver	APIs to support some basic access to SROM System calls
SYSCLK	System Clock	Provides APIs to control and read status of various clocking capabilities of the device
SYSFLT	System Fault	Controls CPUs fault processing Subsystem
SYSINT	System Interrupt	Manage interrupts and exceptions, in conjunction with the CMSIS core NVIC API
SYSLIB	System Library	Utility functions to handle delays, register read/write, asserts, silicon unique ID, and more
SYSPM	System Power Modes	Controls device power modes
SYSREGHC/ SYSPMIC	REGHC/PMIC Control and Status	Controls High Current Regulator or the PMIC module

SYSRESET	System Reset	Provides APIs for reading reset reason and clearing them
SYSRTC	System Real Time Clock	Provides capabilities to handle RTC, Alarms etc.
SYSTICK	System Tick Timer	Manage a 24-bit down-counter timer
SYSWDT	Free running Watchdog timer	Provides control and status capabilities
TDM	Audio Time-division multiplexing	TDM transmitter and a TDM receiver, I2S support also included in latest revisions.
TCPWM	Timer Counter PWM	Manage a 16- or 32-bit periodic Counter, PWM, Quadrature decoder, Shift register
TRIGMUX	Trigger Multiplexer	Manage the multiplexing of trigger outputs to specific trigger inputs across multiple peripherals

Table 4: Device Specific Middleware

Middleware	Description	API Functionality
GFX_ENV	Graphics Environment Setup	Supported only for TVIIC2D6M/TVIIC2D4M (Graphics environment setup support)
MIPI_SENSOR	MIPI CSI2 controller	Support top level MIPI CSI2 APIs for camera access map to capture interface of VIDEOSS IP
POWER	REGHC or PMIC based power control	REGHC or PMIC controller middleware (REGHC/TVIIBH4M/TVIIBH8M, PMIC/TVIIC2D6M/TVIIC2D4M)
SMIF_MEM	SMIF SPI/Hyper Access Control	SPI or xSPI specific device support

Table 5: Common Middleware

Middleware	Description	API Functionality
Button	Button middle layer	APIs to support buttons
Semihosting	SCB/UART middle layer	Support top level UART APIs for debugging
SW_Timer	Software Timer	Enables multiple software timers
Flash	Code and work flash	User level APIs for ease of use
AIC261	Audio Codec	Provides APIs for audio codec (ADC/DAC) TI AIC 261

Hardware-specific middleware such as CS42488, DP83867, AIC26, TJA110, etc.

7 Release Contents

The SDL is organized into several folders. The following table shows the SDL folder structure.

Table 6: SDL Folder Structure

Path/Folder	Description
cmake	CMake device, toolchain specific configurations, debug template files, usage documentation, etc.
common/hdr/cmsis	CMSIS core access headers
common/src/drivers	Drivers common across all the devices
common/src/mw	Middleware common across all the devices
common/src/rtos	FreeRTOS support for application cores
common/src/startup	Tool specific startup code for all the devices
docs	API Documentation
misc/tools	GHS/IAR specific flash loaders, SVD files
TRAVEO™ T2G Body, and Cluster Entry Devices (tviibe1m/2m/4m/512k, tviice4m)	
hdr/rev_x	Device specific header files, BSP for T2G CPU/Base Board, GPIO assignments
hdr/rev_x/ip	Device IP specific headers, register representation
hdr/rev_x/mcureg	IP Specific Register Addresses
src/drivers	Driver source and respective headers specific to the device
src/examples	Code examples in accordance to the device
src/system	Device's system specific code and system header for clock configurations
src/main_cm0plus.c	Sample main source file for CM0+ core
src/interrupts/cy_interrupt_map_cm0plus.h	User interrupt mapping file
src/main_cm4.c	Sample main source file for CM4 core
src/interrupts/cy_interrupt_map_cm4.h	User interrupt mapping file
tools/ghs	GHS MULTI workspaces for SRAM/Flash for CM0+/CM4 core, linker specific files, and GRD files
tools/iar	IAR workspaces for SRAM/Flash for CM0+/CM4 cores, linker specific files
TRAVEO™ T2G Body High, and Cluster 2D Devices (tviibh4m/8m/16m, tviic2d4m/6m/6mddr)	
hdr/rev_x/	Device specific header files, BSP for T2G CPU/Base Board, GPIO assignments
hdr/rev_x/ip	Device IP specific headers, register representation
hdr/rev_x/mcureg	IP Specific Register Addresses
src/drivers	Driver source and respective headers specific to the device
src/mw/	Middleware support
src/examples	Code examples in accordance device specific
src/system	Device system specific code and system header for clock configurations
src/main_cm0plus.c	Sample main source file for CM0+ core
src/interrupts/cy_interrupt_map_cm0plus.h	User interrupt mapping file
src/main_cm7_0.c	Sample main source file for CM7_0 core
src/interrupts/cy_interrupt_map_cm7_0.h	User interrupt mapping file
src/main_cm7_1.c	Sample main source file for CM7_1 core
src/interrupts/cy_interrupt_map_cm7_1.h	User interrupt mapping file
src/main_cm7_2.c	Sample main source file for CM7_2 core (tviibh16m only)
src/interrupts/cy_interrupt_map_cm7_2.h	User interrupt mapping file (tviibh16m only)
src/main_cm7_3.c	Sample main source file for CM7_3 core (tviibh16m only)
src/interrupts/cy_interrupt_map_cm7_3.h	User interrupt mapping file (tviibh16m only)
tools/ghs	GHS MULTI workspaces for SRAM/Flash for CM0+/CM7_0/CM7_1/CM7_2/CM7_3 cores, linker specific files, and GRD files
tools/iar	IAR workspaces for SRAM/Flash for CM0+/CM7_0/CM7_1/ CM7_2/CM7_3 cores, linker specific files

8 Documentation

API Reference Manual are located in the \docs subdirectory of the SDL installation directory.

9 General Notes

a. Application address mapping,

a. *TVIIBE1M/TVIIBE2M/TVIIBE4M/TVIIBE512K/TVIICE4M: In the header "system_cyt2b7.h" / "system_cyt2b9.h" / "system_cyt2bl.h" / "system_cyt2b6.h"/ "system_cyt2cl.h" macro "CY_CORTEX_M4_APPL_ADDR" needs to be updated to CM4 start address as per the linker config file, it is picked by the respective tool chain automatically*

b. *TVIIBH4M/TVIIBH8M/TVIIC2D4M/TVIIC2D6M: In the header "system_cyt4bf.h" /" system_cyt4bb.h" /" system_tviic2d6m.h" macro "CY_CORTEX_M7_0_APPL_ADDR" and "CY_CORTEX_M7_1_APPL_ADDR" needs to be updated to CM7_0/CM7_1 start address as per the linker config file, it is picked by the respective tool chain automatically*

c. *TVIIC2D4M: In the header "system_cyt3dl.h" macro "CY_CORTEX_M7_0_APPL_ADDR" needs to be updated to CM7_0 start address as per the linker config file, it is picked by the respective tool chain automatically*

b. Clock Configuration

Table 7: PSVP Clock Configuration

Sl. No.	Device (PSVP)	Clock	Clock Frequency
2	TVIIBE1M, TVIIBE2M	CM0+/CM4	24 MHz
3	TVIIBH8M, TVIIC2D6M, TVIIC2D4M	CM0+/CM7_x	24 MHz
4	TVIIC2D6M, TVIIC2D4M, TVIIC2D6MDDR, TVIIBH16M	IMO	8 MHz
5	TVIIBE1M, TVIIBE2M	ILO	32.9 kHz
6	TVIIBH8M, TVIIC2D6M, TVIIC2D4M, TVIIC2D6MDDR	ILO	12.8 kHz
7	TVIIC2D6MDDR	CM0+/CM7_x	26.6 MHz
8		LPDDR	80 MHz
9	TVIICE4M	CM0+/CM4	24 MHz
		IMO/ILO	8MHz/12.8kHz
10	TVIIBH16M	CM0+/CM7_x	20 MHz (PLL_OUT)
		ILO	14.178 kHz

Table 8: Silicon Clock Configuration

Sl. No.	Device (Silicon)	Clock	Clock Frequency
1	TVIIBH8M/b/c/d 320-BGA, 176-TEQFP TVIIBH4M/a/b 176-TEQFP, 272-BGA	CM0+	80 MHz
		CM7_0, CM7_1	250/350 MHz
		Bus	160 MHz
		IMO	8 MHz
		ILO	~32 kHz
2	TVIIBE2M/a/b/c 176-LQFP	CM0+	80 MHz
		CM4	160 MHz
		Bus	80 MHz
		IMO	8 MHz
		ILO	~32 kHz
3	TVIIBE1M/b/c/d 176-LQFP	CM0+	80 MHz
		CM4	160 MHz
		Bus	80 MHz
		IMO	8 MHz
		ILO	~32 kHz
4	TVIIC2D6M/b/c 327-BGA	CM0+	80 MHz
		CM7_0, CM7_1	320 MHz
		Bus	160 MHz
		IMO	8 MHz
		ILO	~32 kHz
		SMIF	166 MHz
5	TVIIC2D4M/a/b/c 216-TEQFP	CM0+	80 MHz
		CM7_0	240 MHz
		Bus	160 MHz
		IMO	8 MHz
		ILO	~32 kHz
6	TVIIBE512K/d 100-LQFP	CM0+	80 MHz
		CM4	160 MHz
		Bus	80 MHz
		IMO	8 MHz
		ILO	~32 kHz
7	TVIICE4M/a 176-LQFP	CM0+	80 MHz
		CM4	160 MHz
		Bus	80 MHz
		IMO	8 MHz
		ILO	~32 kHz
8	TVIIC2D6MDDR/a 500-BGA	CM0+	80 MHz

		CM7_0, CM7_1	320 MHz
		Bus	160 MHz
		IMO	8 MHz
		ILO	~32 kHz
		LPDDR4	752 MHz
		VIDEOSS	266 MHz
9	TVIIBH16M/a 320-BGA	CM0+	80 MHz
		CM7_0, CM7_1, CM7_2, CM7_3	250/350 MHz
		Bus	160 MHz
		IMO	8 MHz
		ILO	~32 kHz

c. CM0+ samples shall not use IRQs 0/1 (CPUIntIdx0_IRQn/CPUIntIdx1_IRQn), as they are internally used by the SROM based System calls. This can be seen as part of the examples for reference. It would cause hard fault, if used.

d. Interrupt usage:

All the examples are modified to use the IRQ table in SRAM and thereby relives from maintaining core specific interrupt map headers (example: cy_interrupt_map_cm7_0.h)

For IRQs part of SRAM

a. No need to update core specific interrupt map headers for any IP specific ISRs, instead update respective example as below (default interrupt map headers at src level will be used as is without any modifications)

b. Cy_SysInt_SetSystemIrqVector(irq_cfg.sysIntSrc, ButtonIntHandler); // typical use case example

For IRQs part of flash region

a. Users will still need to update the core specific interrupt map header against the IP which is being tested and remove the below define from the respective header,
#define CY_LINK_SYSTEM_IRQ_TABLE_TO_RAM

Table 9: Device to SMIF revision mapping

Device	Device Revision	SMIF Revision
TVIIBH4M/TVIIBH8M/TVIIBH16M	All	v2
TVIIC2D4M	Rev_A/Rev_B/Rev_C	v3.1
TVIIC2D6M	Rev_B/Rev_C	v4.0
TVIIC2D6MDDR	Rev_A	v4.0
TVIICE4M	Rev_A	v3.1

10 Change Log from v8.0.0 to v8.1.0

Sl. No.	Change	Files	Action
1	Added dummy configuration to avoid build errors: “RELEASE_BUILD_DUMMY_CONFIG”	TVII-SampleSW/tviic2d6mddr/src/drivers/lpddr4/cy_dramconfsel.h	Modified
2	Updated “Cy_Lpddr_ReadDQSOscValue()” in the LPDDR4 driver configuration file for: - corrected check for DQS Osc max values to 0xFFFF - corrected abort condition - changed the condition to detect the read for a channel completed.	TVII-SampleSW/tviic2d6mddr/src/drivers/lpddr4/cy_lpddr4.c	Modified
3	Updated the LPDDR4 driver to 3.0: - added JESD209_4B_NS_TDQS2DQ_MIN and JESD209_4B_NS_TDQS2DQ_MAX - added new datatype for reading the DRAM vendor - added new datatype for reading the channel density - added a data type for easy register access for lpddr4 - added function for DLL Re-Initialization Cy_LPDDR4_DLLResMCStoSta()	TVII-SampleSW/tviic2d6mddr/src/drivers/lpddr4/cy_lpddr4.h	Updated
4	Updated the LPDDR4 driver: - added software aided training. - added DLL re-initialization - added the support for to replace the DQS2DQ HW re-training by SW	TVII-SampleSW/tviibh8m/src/drivers/ lpddr4/cy_lpddr4.h	Updated
5	Updated the LPDDR4 driver: - added SW aided training feature for read and write	TVII-SampleSW/tviic2d6mddr/src/drivers/lpddr4/cy_dram_config.h	Updated
6	Updated the eMMC driver: - Added CLK_IN and CLK_OUT delay APIs - Added the DDR mode support for eMMC	TVII-SampleSW/tviibh8m/src/drivers/sd_host/cy_sd_host.c	Updated
7	Minor warning fixes on the FPD_LINK driver	TVII-SampleSW/tviibh8m/src/drivers/fpdlink/cy_fpdlink.h	Modified

11 Change Log from v7.9.0 to v8.0.0

Sl. No.	Change	Files	Action
1	Adds the fix for the SD Host driver to include new line at the end of the file.	TVII-SampleSW/tviibh8m/src/drivers/sd_host/cy_sd_host.c	Modified
2	Adds Ethernet driver files with proper licencing and terms.	TVII-SampleSW/tviibh8m/src/drivers/ethernet/cdn_errno.h TVII-SampleSW/tviibh8m/src/drivers/ethernet/cdn_stdint.h TVII-SampleSW/tviibh8m/src/drivers/ethernet/cedi.h TVII-SampleSW/tviibh8m/src/drivers/ethernet/cps_v2.h TVII-SampleSW/tviibh8m/src/drivers/ethernet/cy_ethif.c TVII-SampleSW/tviibh8m/src/drivers/ethernet/cy_ethif.h TVII-SampleSW/tviibh8m/src/drivers/ethernet/edd.c TVII-SampleSW/tviibh8m/src/drivers/ethernet/edd_int.h TVII-SampleSW/tviibh8m/src/drivers/ethernet/edd_rx.c TVII-SampleSW/tviibh8m/src/drivers/ethernet/edd_tx.c TVII-SampleSW/tviibh8m/src/drivers/ethernet/emac_regs.h TVII-SampleSW/tviibh8m/src/drivers/ethernet/emac_regs_macro.h TVII-SampleSW/tviibh8m/src/drivers/ethernet/log.h	Modified
3	Moved the LPDDR4 power sequencing function out of the system initialization.	TVII-SampleSW/tviic2d6mddr/src/system/rev_a/system_tviic2d6mddr_cm7.c	Modified
4	Adds new JEDEC timing parameter ODTLON which is calculated based on FSP[1] and the used WL Set refer JEDED209-4C.	TVII-SampleSW/tviic2d6mddr/src/drivers/lpddr4/cy_dram_config.h	Modified
5	Adds some JEDEC timing parameters related to JESD209_4B_NS	TVII-SampleSW/tviic2d6mddr/src/drivers/lpddr4/cy_dram_config.h	Modified
6	Adds support to configure LPDDR4 Inline ECC Addresses via linker file using the macro: ECC_USE_LINKER_ADDRESSES	TVII-SampleSW/tviic2d6mddr/src/drivers/lpddr4/cy_dram_config.h	Modified
7	Corrected PLL SSCG setting in PLL manual configuration function.	TVII-SampleSW/tviic2d6mddr/src/drivers/lpddr4/cy_lpddr4.c	Modified
8	Changed the attribute volatile to driver context variable.	TVII-SampleSW/tviic2d6mddr/src/drivers/lpddr4/cy_lpddr4.c	Modified
9	Adds re-training detection, direction with new driver context fields based on tDQS2DQ value	TVII-SampleSW/tviic2d6mddr/src/drivers/lpddr4/cy_lpddr4.c	Added
10	Adds the feature for the retraining detection, adds additional functions for the AXI performance counter usage.	TVII-SampleSW/tviic2d6mddr/src/drivers/lpddr4/cy_lpddr4.h	Added
11	Updates LPDDR4 default config from the Solution Designer.	TVII-SampleSW/tviic2d6mddr/src/drivers/lpddr4/cy_dramconfsel.h	Modified
12	Fixes the opcode bug in API's Cy_Flash_ConfigureFMIntr() and Cy_Flash_ConfigureFMIntr1() from flash driver.	TVII-SampleSW/common/src/drivers/flash/cy_flash.c	Modified

12 Change Log from v7.8.0 to v7.9.0

Sl. No.	Change	Files	Action
1	Adds and adjusted BSP for C2D4M lite kit in tviic2d4m device.	TVII-SampleSW/tviic2d4m/hdr/rev_c/bb_bsp_tviic2d4m.h TVII-SampleSW/tviic2d4m/hdr/rev_c/bsp/bsp_tviic2d4m_216teqfp_device_revc_evk_reva.h TVII-SampleSW/tviic2d4m/hdr/rev_c/bsp/bsp_tviic2d4m_272bga_device_revc_evklite_reva.h	Modified
2	Add D-Cache maintenance to SROM and Flash driver	TVII-SampleSW/common/src/drivers/flash/cy_flash.c TVII-SampleSW/common/src/drivers/srom/cy_srom.c TVII-SampleSW/common/src/drivers/syslib/cy_syslib.c TVII-SampleSW/common/src/drivers/syslib/cy_syslib.h	Modified
3	Added the defines for the LPDDR4 config file versioning	TVII-SampleSW/tviic2d6mddr/src/examples/lpddr4/Sol_Designer_Sample/lpddr4_cfg.h	Modified
4	Added additional defines for the frequency set points and changed the write latency in dram config	TVII-SampleSW/tviic2d6mddr/src/drivers/lpddr4/cy_dram_config.h	Modified
5	Corrected the RTT_SEL cy_en_lpddr4_rtt_sel_t to n+1 added RANGE0 to cy_en_lpddr4_vtgc_ivrefr_t	TVII-SampleSW/tviic2d6mddr/src/drivers/lpddr4/cy_en_lpddr4.h	Modified
6	Added some training/re-training status/ error information in the driver context	TVII-SampleSW/tviic2d6mddr/src/drivers/lpddr4/cy_lpddr4.c	Modified
7	Added a training status/errors and counter for retraining events	TVII-SampleSW/tviic2d6mddr/src/drivers/lpddr4/cy_lpddr4.h	Modified
8	Added versioning for LPDDR driver which includes the SVN Rev and SVN Date of the driver per software	TVII-SampleSW/tviic2d6mddr/src/drivers/lpddr4/cy_lpddr4.c	Modified
9	Corrected a condition in DQS2DQ re-training for unOPSTT_CHx	TVII-SampleSW/tviic2d6mddr/src/drivers/lpddr4/cy_lpddr4.c	Modified
10	Added the possibility to set change controller related parameter like drive strength for DQ/CA, SOC ODT in the cy_dram_config.h	TVII-SampleSW/tviic2d6mddr/src/drivers/lpddr4/cy_dram_config.h	Modified
11	Moved the command for starting the DQS Osc to the end of monitoring function. Adds a function to correct SEC ECC faults.	TVII-SampleSW/tviic2d6mddr/src/drivers/lpddr4/cy_lpddr4.c	Modified
12	Added new datatype to support PLL800CONFIG.stcField.unlockerr	TVII-SampleSW/tviic2d6mddr/src/drivers/lpddr4/cy_lpddr4.h TVII-SampleSW/tviic2d6mddr/src/drivers/lpddr4/cy_lpddr4.c	Modified
13	Replaced the functionality for starting/reading the DQS Osc in Cy_Lpddr_RequestDQS2DQRetrain ()	TVII-SampleSW/tviic2d6mddr/src/drivers/lpddr4/cy_lpddr4.c	Modified
14	Added a possibility to change the DQS2DQ retraining by manual adjustment or PVT compensation.	TVII-SampleSW/tviic2d6mddr/src/drivers/lpddr4/cy_dram_config.h	Modified
15	Added a feature to calculate the delta manual adjustment for the DLLs in PTSR5..13 Added function to calculate the DQS Osc runtime in clks of FSP[1]	TVII-SampleSW/tviic2d6mddr/src/drivers/lpddr4/cy_lpddr4.c	Modified
16	Added a callback which can be triggered during Vertical Blanking Added extra functions to update parameters during DQS2DQ training.	TVII-SampleSW/tviic2d6mddr/src/drivers/lpddr4/cy_lpddr4.h TVII-SampleSW/tviic2d6mddr/src/drivers/lpddr4/cy_lpddr4.c	Modified
17	Updates the header to support the "READ_FUSE_BYTE_MARGIN" and "BLOW_FUSE_BIT" features	TVII-SampleSW/common/src/drivers/srom/cy_srom.h	Modified
18	Add initialization of CH_IDX registers which are undefined after reset and can cause malfunction on the first transfer of a channel	TVII-SampleSW/common/src/drivers/dma/cy_mdma.c TVII-SampleSW/common/src/drivers/dma/cy_pdma.c	Modified

19	Fix/improve delay implementation for resetting S28H in case of builds with optimization enabled	TVII-SampleSW/tviic2d6m/src/mw/gfx_env/cy_gfx_env.c TVII-SampleSW/tviic2d6mddr/src/mw/gfx_env/cy_gfx_env.c	Modified
20	Add tviic2d4m Lite Kit as CMake preset, fix some problems in BSP header and GfxEnv to make it build	TVII-SampleSW/CMakePresets.json TVII-SampleSW/cmake/t2g_device_config/tviic2d4m.cmake TVII-SampleSW/tviic2d4m/src/mw/gfx_env/cy_gfx_env.c	Modified
21	Added a fix to initialize a PDMA channel's SRAM ECC properly before accessing control bits to avoid unwanted ECC faults.	TVII-SW-FW/TVII-SampleSW/common/src/drivers/dma/cy_pdma.c	Modified
22	Updates the BSP for the lite kit T2G_BE_4M_LITE.	TVII-SampleSW/tviibe4m/hdr/rev_a/bb_bsp_tviibe4m.h TVII-SampleSW/tviibe4m/hdr/rev_a/bb_bsp_tviibe4m_lite_kit.h	Modified
23	Bug fix for the: DCache issue after read/write Clock fixed to 100MHz for proper operation	TVII-SampleSW/tviibh8m/src/drivers/sd_host/cy_sd_host.c	Modified

13 Change Log from v7.7.0 to v7.8.0

Sl. No.	Change	Files	Action
1	Device headers for Silicon updated for TVII-B-H-16M, untested	TVII-SampleSW/tviibh16m/hdr/rev_a	Modified
2	Arm GNU GCC start up files added for use with Cmake	TVII-SampleSW/common/src/startup/gcc	Addition
3	IAR EWARM workspaces updated from v8.42.1 to v9.30.1 Note: TVIIBH16M was already supported on v9.30.1 Flash patch updated accordingly.	TVIIBE1M/2M/4M/512K, TVIIBH4M/8M, TVIICE4M, TVIIC2D4M/6M/6MDDR	Modified
4	changed default FSP[1] speed to 752 MHz enabled RDBI/WDBI by default corrected JEDEC default value Optimized some APIs added macro define which can by used to select if training is done in ons step or stepwise for testing purpose added the possibility to do a stepwise training code clean up and flow optimization reduced API overhead and optimized process flow in Cy_Lpddr_RequestDQS2DQRetrain() and Cy_Lpddr_StartDQSOscillator() to reduce memory blackout times deleted some unused debug code- some changes to avoid warnings from GCC -get rid of CY_ASSERT() function -set initial values for mr18Value and mr18Value in Cy_Lpddr_ReadDQSOscValue() to avoid GCC compiler warning changed parameter tINIT3 min 2ms --> 2.1ms Parameter is defined as minimum 2ms in the JEDEC spec.In Micron Report the time measured was slightly below 2ms. As Parameter is min. value we can just slightly increase it to be within Spec Limits	TVII-SampleSW/tviic2d6mddr/src/drivers/lpddr4/cy_dram_config.h TVII-SampleSW/tviic2d6mddr/src/drivers/lpddr4/cy_lpddr4.c	Modified
5	ETH drivers removed from SDL, replaced with dummy files.	TVII-SampleSW/tviibh8m/src/drivers/ethernet TVIIBH4M/8M/16M, TVIIC2D4M/6M/6MDDR	Removed
6	RTOS update for GCC support	TVII-SampleSW/common/src/rtos/portable/GCC	Addition
7	Fix warning about implicit conversion from float to double when compiling via CMake and IAR 9.30.1	TVII-SampleSW/common/src/drivers/adc/cy_adc.c	Modified
8	GCC support linker file added to all devices except TVIIBH16M	TVIIBE1M/2M/4M/512K, TVIIBH4M/8M/16M, TVIICE4M, TVIIC2D4M/6M/6MDDR	Addition
9	Removed ver3_0. not needed any more since TVIIC2D6M rev_a support was also removed earlier.	TVII-SampleSW/common/src/drivers/smif/ver3_0	Removed
10	Fixes for GCC integration	TVII-SampleSW/common/src/drivers/syslib/cy_syslib.h TVII-SampleSW/common/src/drivers/scb/cy_scb_spi.c TVII-SampleSW/tviibe1m/src/drivers/sysclk/cy_sysclk.h TVII-SampleSW/tviibe4m/src/drivers/sysclk/cy_sysclk.h TVII-SampleSW/tviibe512k/src/drivers/sysclk/cy_sysclk.h TVII-SampleSW/tviibh8m/src/drivers/sysclk/cy_sysclk.h TVII-SampleSW/tviice4m/src/drivers/sysclk/cy_sysclk.h TVII-SampleSW/common/src/drivers/flash/cy_flash.h TVII-SampleSW/common/src/drivers/mcwdt/cy_mcwdt.h TVII-SampleSW/common/src/drivers/trigmux/cy_trigmux.c TVII-SampleSW/common/src/drivers/trigmux/cy_trigmux.h	Modified

11	fix compiler warning for potential use of non-initialized var Fix GCC warning about unused var in release cfg	TVII-SampleSW/tviibh8m/src/drivers/flexray/ccal/cy_fr_ccal_rx_handler.c TVII-SampleSW/tviibh8m/src/drivers/flexray/ccal/cy_fr_ccal_tx_handler.c TVII-SampleSW/tviibh8m/src/system/rev_d/system_tviibh8m_cm0plus.c TVII-SampleSW/tviibh8m/src/mw/smif_mem/cy_smif_hb_flash.c TVII-SampleSW/tviibh8m/src/drivers/audioss/cy_i2s.h TVII-SampleSW/common/src/mw/aic261/cy_aic261.c TVII-SampleSW/tviibh8m/src/mw/smif_mem/cy_smif_device_common.c TVII-SampleSW/tviibh8m/src/mw/smif_mem/cy_smif_device_common.h TVII-SampleSW/tviibh16m/src/system/rev_a/system_tviibh16m_cm0plus.c TVII-SampleSW/tviibh4m/src/system/rev_a/system_tviibh4m_cm0plus.c TVII-SampleSW/tviibh4m/src/system/rev_b/system_tviibh4m_cm0plus.c TVII-SampleSW/tviibh8m/src/system/rev_b/system_tviibh8m_cm0plus.c TVII-SampleSW/tviibh8m/src/system/rev_c/system_tviibh8m_cm0plus.c TVII-SampleSW/tviic2d4m/src/system/rev_a/system_tviic2d4m_cm0plus.c TVII-SampleSW/tviic2d4m/src/system/rev_b/system_tviic2d4m_cm0plus.c TVII-SampleSW/tviic2d4m/src/system/rev_c/system_tviic2d4m_cm0plus.c TVII-SampleSW/tviic2d6m/src/system/rev_b/system_tviic2d6m_cm0plus.c TVII-SampleSW/tviic2d6m/src/system/rev_c/system_tviic2d6m_cm0plus.c TVII-SampleSW/tviic2d6mddr/src/system/rev_a/system_tviic2d6mddr_cm0plus.c TVII-SampleSW/common/src/mw/flash/cy_mw_flash.c	Modified
12	Fix GCC warning about missing braces move "static" stuff from header to source to fix compiler warnings	TVII-SampleSW/tviic2d6m/src/mw/gfx_env/cy_gfx_env.c TVII-SampleSW/tviic2d6m/src/drivers/mipicsi2/cy_mipicsi2.c TVII-SampleSW/tviic2d6m/src/mw/mipi_sensor/cy_mipi_sensor.c TVII-SampleSW/tviic2d6m/src/mw/mipi_sensor/cy_mipi_sensor.h Similarly for TVIIC2D6MDDR	Modified
13	removed not needed enumerations (CM7s are not there in BE devices).	TVII-SW-FW/TVII-SampleSW/tviibe1m/src/drivers/cpu/cy_cpu.c TVII-SW-FW/TVII-SampleSW/tviibe1m/src/drivers/cpu/cy_cpu.h	Modified
14	Cy_SysClk_DeepSleepCallback adapted for correct usage. Before the DeepSleep, ECO->IMO for PLLs. After the exit of DeepSleep, IMO->ECO for PLLs.	TVII-SampleSW/tviibe1m/src/drivers/sysclk/cy_sysclk.c	Modified
15	Adapted to support all CM7s in BH16M device.	TVII-SampleSW/common/src/drivers/ipc/cy_ipc_config.h	Modified
16	Adding MCWDT to CM7_2, CM7_3 is not connected to any MCWDT module.	TVII-SampleSW/common/src/drivers/mcwdt/cy_mcwdt.h	Modified
17	Aligning power mode status for all cores, including CM7_2/3 Cy_SysPm_ReadStatus updated to support BH16M (CM7_2/3) Cy_SysPm_DeepSleep updated for application core handling (it was TBD earlier) device based macro added. fix for supporting only BH16M devices.	TVII-SampleSW/common/src/drivers/syspm/cy_syspm.h TVII-SampleSW/common/src/drivers/syspm/cy_syspm.c	Modified
18	cy_en_cpu_core_type_t encapsulating with bh16m macro.	TVII-SampleSW/tviibh8m/src/drivers/cpu/cy_cpu.h	Modified
19	Cy_SysClk_GetCoreFrequency adapted for supporting CM7_2/3 for fast 2/3 frequencies. BH16M support added Cy_SysClk_DeepSleepCallback timeout handling corrected.	TVII-SampleSW/tviibh8m/src/drivers/sysclk/cy_sysclk.c TVII-SampleSW/tviibh8m/src/drivers/sysclk/cy_sysclk.h	Modified
20	208-TEQFP removed from SDL for TVIIC2D4M device in rev_c (cyt3dl9*)	TVII-SampleSW/tviic2d4m/hdr/rev_c	Removed
21	CY_SYSPM_ACTIVE_TO_LP_WAIT_US and CY_SYSPM_LP_TO_ACTIVE_WAIT_AFTER_US changed from 1uS to 5uS.	TVII-SampleSW/common/src/drivers/syspm/cy_syspm.h	Modified
22	Removing CLK_TIMER APIs, as they are not supposed to be supported. Recently removed from the registers list.	TVII-SampleSW/tviibh8m/src/drivers/sysclk/cy_sysclk.c TVII-SampleSW/tviibh8m/src/drivers/sysclk/cy_sysclk.h	Removed
23	Bug Fixed. Cy_MPU_GetRegion->cfg->size = (cy_en_mpu_region_size_t) (rasr & MPU_RASR_ATTRS_Msk); modified to Cy_MPU_GetRegion->cfg->size = (cy_en_mpu_region_size_t) (rasr & MPU_RASR_SIZE_Msk);	TVII-SampleSW/common/src/drivers/mpu/cy_mpu.c	Modified

14 Change Log from v7.6.0 to v7.7.0

Sl. No.	Change	Files	Action
1	CMSIS v5.9.0 integration	TVII-SampleSW/common/hdr/cmsis/include/cachel1_armv7.h TVII-SampleSW/common/hdr/cmsis/include/cmsis_armcc.h TVII-SampleSW/common/hdr/cmsis/include/cmsis_armclang.h TVII-SampleSW/common/hdr/cmsis/include/cmsis_armclang_ltm.h TVII-SampleSW/common/hdr/cmsis/include/cmsis_compiler.h TVII-SampleSW/common/hdr/cmsis/include/cmsis_gcc.h TVII-SampleSW/common/hdr/cmsis/include/cmsis_iccarm.h TVII-SampleSW/common/hdr/cmsis/include/cmsis_version.h TVII-SampleSW/common/hdr/cmsis/include/core_cm0plus.h TVII-SampleSW/common/hdr/cmsis/include/core_cm4.h TVII-SampleSW/common/hdr/cmsis/include/core_cm7.h TVII-SampleSW/common/hdr/cmsis/include/mpu_armv7.h	Modified
2	Added missing AXI-DMA driver for tviic2d6mddr device workspaces	TVII-SampleSW/tviic2d6mddr/tools/ghs/_gpj/libsdl_source.gpj	Modified
3	FLASHC1 wait states added, FAST_CLK_2/3 added	TVII-SampleSW/tviibh16m/src/system/rev_a/system_tviibh16m_cm0plus.c	Modified

4	Corrections in mem reservation for PSVP.
	// cm0plus_code_flash_reserve = 512K; // 0x10000000 to 0x1007ffff
	// cm7_0_code_flash_reserve = 512K; // 0x10080000 to 0x100fffff
	// cm7_1_code_flash_reserve = 512K; // 0x10400000 to 0x1047ffff
	// cm7_2_code_flash_reserve = 512K; // 0x18000000 to 0x1807ffff
	// cm7_3_code_flash_reserve = 512K; // 0x18400000 to 0x1847ffff
		TVII-SampleSW/tviibh16m/tools/iar/linker_directives.icf	Modified

5	CY_USB_SCB_TYPE -> CY_USB_SCB_UART_TYPE CY_USB_SCB_UART_RX_MUX -> CY_USB_SCB_UART_RX_PIN_MUX CY_USB_SCB_UART_TX_MUX -> CY_USB_SCB_UART_TX_PIN_MUX	TVII-SampleSW/tviic2d4m/hdr/rev_a/bb_bsp_tviic2d4m.h TVII-SampleSW/tviic2d4m/hdr/rev_b/bb_bsp_tviic2d4m.h TVII-SampleSW/tviic2d4m/hdr/rev_c/bb_bsp_tviic2d4m.h TVII-SampleSW/tviic2d4m/src/mw/gfx_env/cy_gfx_env.h TVII-SampleSW/tviic2d6m/hdr/rev_b/bb_bsp_tviic2d6m.h TVII-SampleSW/tviic2d6m/hdr/rev_c/bb_bsp_tviic2d6m.h TVII-SampleSW/tviic2d6m/src/mw/gfx_env/cy_gfx_env.h	Modified
6	BH16M update for CM7_2/3 support.	TVII-SampleSW/tviibh16m/src/drivers/cpu/cy_cpu.c TVII-SampleSW/tviibh16m/src/drivers/cpu/cy_cpu.h TVII-SampleSW/tviibh16m/src/interrupts/rev_a/cy_interrupt_map.c TVII-SampleSW/common/src/drivers/sysint/cy_sysint.c	Modified
7	Fixes for APIs to control power of memory and CPU power. WOUNDING registers are hidden, so removing the APIs associated.	TVII-SampleSW/tviibe1m/src/drivers/cpu/cy_cpu.c TVII-SampleSW/tviibe1m/src/drivers/cpu/cy_cpu.h TVII-SampleSW/tviibh8m/src/drivers/cpu/cy_cpu.c TVII-SampleSW/tviibh8m/src/drivers/cpu/cy_cpu.h	Modified
8	Incorrect SMIF SELECT1 assignment corrected	TVII-SampleSW/tviic2d6mddr/hdr/rev_a/bsp/bsp_tviic2d6mddr_500bga_device_reva_evk_reva.h	Modified
9	Updated the LPDDR4 power sequence with software trigger mode and added LPECO enable in system header.	TVII-SampleSW/tviic2d6mddr/src/system/rev_a/system_cyt4en.h TVII-SampleSW/tviic2d6mddr/src/system/rev_a/system_tviic2d6mddr_cm0plus.c TVII-SampleSW/tviic2d6mddr/src/system/rev_a/system_tviic2d6mddr_cm7.c	Modified
10	Adding RSA 4K part numbers to GHS odb file	TVII-SampleSW/misc/tools/ghs/ghs_comp_xxxxxx_defaults_flash/flash_chips_fcr4tcm.odb TVII-SampleSW/misc/tools/ghs/ghs_comp_xxxxxx_defaults_flash/generator/tvii_chip_list.csv	Modified
11	Addition of CSV code example for BE devices	TVII-SampleSW/tviibe1m/src/examples/sysclk/HfclkCSV	Addition
12	Addition of sd_card examples which were missing in previous releases	TVII-SampleSW/tviibh8m/src/examples/sd_host/sd_card	Addition
13	Updated eMMC driver to work at 40MHz.	TVII-SampleSW/tviibh8m/src/drivers/sd_host/cy_sd_host.c TVII-SampleSW/tviibh8m/src/drivers/sd_host/cy_sd_host.h TVII-SampleSW/tviic2d6mddr/src/system/rev_a/system_tviic2d6mddr_cm0plus.c	Modified

15 Change Log from v7.5.0 to v7.6.0

Sl. No.	Change	Files	Action
1	DIAB linker script file added to the remaining devices other than tviibe1m	All devices	Addition
2	Comment out CY_SMIF_CLKIF_SRC_CLK_PLL_DIRECT enum value, customers need to use CY_SMIF_CLKIF_SRC_CLK_PLL_NORMAL	TVII-SampleSW/common/src/drivers/smif/ver4/cy_smif_ver_specific.h	Modified
3	Support for tviibh16m PSVP added. (Only partiallly tested, CM7_2/3 does not work, flashc#1 not working still) WS/Project adaption to 9.30.1 IAR EWARM	TVII-SampleSW/tviibh16m/	Addition
4	Added MCAL examples (C sources and Tresos projects)	All devices Ex: TVII-SampleSW/tviibe1m/src/examples/mcal	Addition
5	Adding stub files from MCAL SW Framework	TVII-SampleSW/common/src/mcalstubs	Addition
6	Clock updates as per the datasheet	TVII-SampleSW/tviic2d6mddr/src/system/rev_a/system_tviic2d6mddr_cm0plus.c	Modified
7	Updated SD_host Driver and added working example for eMMC (Hynix)	TVII-SampleSW/tviibh8m/src/drivers/sd_host/cy_sd_host.c TVII-SampleSW/tviibh8m/src/drivers/sd_host/cy_sd_host.h	Modified
8	Add some APIs, change RX config to discard certain faulty frames	TVII-SampleSW/tviibh8m/src/drivers/ethernet/cy_ethif.c TVII-SampleSW/tviibh8m/src/drivers/ethernet/cy_ethif.h TVII-SampleSW/tviibh8m/src/mw/eth_phy/cy_dp83867.c TVII-SampleSW/tviibh8m/src/mw/eth_phy/cy_dp83867.h	Modified
9	Increase FreeRTOS heap (8KB -> 16KB) because the ethernet_stack example requires it	TVII-SampleSW/common/src/rtos/include/FreeRTOSConfig.h	Modified
10	Adding FreeRTOS+TCP Ethernet stack	TVII-SampleSW/common/src/ethstack	Addition
11	Adding DP83848Q-Q1 Ethernet PHY MW driver	TVII-SampleSW/tviibh8m/src/mw/eth_phy/cy_dp83848q_q1.c TVII-SampleSW/tviibh8m/src/mw/eth_phy/cy_dp83848q_q1.h TVII-SampleSW/tviibh8m/src/mw/eth_phy/cy_dp83867.h	Addition
12	OpCodes for FLASHC1 added	TVII-SampleSW/common/src/drivers/srom/cy_srom.h	Modified
13	Added support for BH16M Flashc and Flashc1	TVII-SampleSW/common/src/drivers/flash/cy_flash.c TVII-SampleSW/common/src/drivers/flash/cy_flash.h TVII-SampleSW/common/src/mw/flash/cy_mw_flash.c TVII-SampleSW/common/src/mw/flash/cy_mw_flash.h	Modified
14	corrected typo in macro define RELASE_BUILD_DUMMY_CONFIG --> RELEASE_BUILD_DUMMY_CONFIG added support for derating strategy changed the PLL input freq. settings 8MHz --> 20 MHz and the corresponding PLL deviders	TVII-SampleSW/tviic2d6mddr/src/drivers/lpddr4/cy_dramconfsel.h TVII-SampleSW/tviic2d6mddr/src/drivers/lpddr4/cy_dram_config_dummy.h	Modified
15	added the possibility for the user to select between dynamic derating (DERATING_STRATEGY == DERATING_DYNAMIC) based on MR4 reading or derating always active for 105°C (DERATING_STRATEGY == DERATING_ALWAYS_ON) The configured derating startegy can be read from lpddr4 driver context g_stc_lpddr_context.timingDeratingStrategy. When using MANUAL_CONFIG it can be set in cy_dram_config.h #define DERATING_ALWAYS_ON 0 #define DERATING_DYNAMIC 1 #define DERATING_STRATEGY DERATING_ALWAYS_ON in case of Solution Designer Configuration it can be configured in the Solution Designer and is then included in the lpddr4_cfg.h file added __attribute__((unused)) to Cy_Lpddr_PerformTimingDerating(..) as it is not used when derating is always active. To avoid wrning during compile time added function	TVII-SampleSW/tviic2d6mddr/src/drivers/lpddr4/cy_lpddr4.c TVII-SampleSW/tviic2d6mddr/src/drivers/lpddr4/cy_lpddr4.h	Modified

	Cy_Lpddr_GetContextRetrainActive(void) used to read if re-training is currently active or not from driver context corrected typos in comments added a Power Down Entry Command during Cy_Lpddr_ControllerDeInit(...) --> CKE=L before Supply can be switched off as proposed from Dolphin set DLYEVALEN = 0x0; during Training. adapted the PLL settings to reflect the latest change in PLL inout from CLK_PATH6 (20MHz)--> CLK_PATH10 (ECO=16MHz) . corrected error in JEDEC default JESD209_4B_FSP0_MR12_DEFAULT_VREFCA_VALUE 0x1D --> 0xD JESD209_4B_FSP0_MR14_DEFAULT_VREFDQ_VALUE 0x1D --> 0xD		
16	added enum for derating strategy cy_en_deratingstrategy_state_t added a field timingDeratingStrategy to lpddr4 driver context structure cy_stc_lpddr4_context_t added function Cy_Lpddr_GetContextRetrainActive(void) to read if a re-training is active or not corrected some typos	TVII-SampleSW/tviic2d6mddr/src/drivers/lpddr4/cy_lpddr4.h	Modified
17	Update the LPDDR4 sequencing API's in the system CM0+ Updates the LPDDR4 power enable for the HSIO_ENH domain Updates the ECO trim settings for the 16MHz in system files.	TVII-SampleSW/tviic2d6mddr/src/system/rev_a/system_cyt4en.h TVII-SampleSW/tviic2d6mddr/src/system/rev_a/system_tviic2d6mddr_cm0plus.c	Modified
18	Update CM7 assembler code to generically support up to quad CM7 core devices	TVII-SampleSW/common/src/startup/diab/startup_cm7.s TVII-SampleSW/common/src/startup/ghs/startup_cm7.arm TVII-SampleSW/common/src/startup/iar/startup_cm7.s	Modified
19	Reduce SMIF freq for tviic2d6m in GFXENV example to 166MHz as per latest datasheet	TVII-SampleSW/tviic2d6m/src/examples/gfx_env/fast_init/main_cm7_0.c TVII-SampleSW/tviic2d6m/src/examples/gfx_env/flexible_init/main_cm7_0.c	Modified

16 Change Log from v7.4.0 to v7.5.0

Sl. No.	Change	Files	Action
1	Command line-based build system integrated	All devices with IAR/GHS	Addition
2	Windriver DIAB compiler support added via command line ONLY . New startups . New linker definition file (for now only tveebe1m) . CMSIS specific support added . Existing TVIIBE1M device headers manually edited to support DIAB . Use __Vectors instead of __vector_table to avoid conflict with existing qualifier names in DIAB compiler	TVII-SampleSW/tviibe1m TVII-SampleSW/common/src/drivers/syslib/cy_syslib.c TVII-SampleSW/common/src/startup/startup.c TVII-SampleSW/common/src/startup/startup_customize.h	Addition
3	. Add new implementation of gfxenv for tviic2d6m rev_c now supporting memories on BGA327 board, make corresponding adaptions to gfxenv for tviic2d4m because interface (header file) changed, update/improve examples . Change RWDS drive mode to strong/pull-down	TVII-SampleSW/tviic2d4m/src/mw/gfx_env TVII-SampleSW/tviic2d4m/src/mw/gfx_env/cy_gfx_env.c TVII-SampleSW/tviic2d4m/src/mw/gfx_env/cy_gfx_env.h TVII-SampleSW/tviic2d6m/src/mw/gfx_env/cy_gfx_env.c TVII-SampleSW/tviic2d6m/src/mw/gfx_env/cy_gfx_env.h	Modified
4	Evengen Clock assignment corrections	All device system_x_cm0plus.c files Ex: TVII-SampleSW/tviibe2m/src/system/rev_a/system_tviibe2m_cm0plus.c	Modified
5	Add __set_PRIMASK/__get_PRIMASK macros for GHS CMSIS header file	TVII-SampleSW/common/hdr/cmsis/include/cmsis_ghs.h	Modified
6	. Driver specific updates . small correction in calculation timing parameters to avoid out of range warning	TVII-SampleSW/tviic2d6mddr/src/drivers/lpddr4/cy_dramconfsel.h TVII-SampleSW/tviic2d6mddr/src/drivers/lpddr4/cy_en_lpddr4.h TVII-SampleSW/tviic2d6mddr/src/drivers/lpddr4/cy_lpddr4.c TVII-SampleSW/tviic2d6mddr/src/drivers/lpddr4/cy_lpddr4.h	Modified
7	Add eth_phy MW to tviibh4m/8m	TVII-SampleSW/tviibh8m/src/mw/eth_phy TVII-SampleSW/tviibh8m/src/mw/eth_phy/cy_dp83867.c TVII-SampleSW/tviibh8m/src/mw/eth_phy/cy_dp83867.h	Addition
8	DAP authentication added into IAR patch	TVII-SampleSW/misc/tools/iar/IAR_EWARM_8421_FlashLoader_Patch_TraveoII.7z	Modified
9	Binary search alorithm added for Die temp measurement examples	Ex: TVII-SampleSW/tviibe1m/src/examples/adc/DieTempCalculation	Modified
10	Remove some DIAB compiler warnings in cy_sysclk (tviibe1m)	TVII-SampleSW/tviibe1m/src/drivers/sysclk/cy_sysclk.c	Modified

17 Change Log from v7.3.0 to v7.4.0

Sl. No.	Change	Files	Action
1	Remove Cy_Srom_CallApi_2 and related things. Cy_Srom_CallApi_2 is not required because all parameters can be carried by SRAM scratch pointed by IPC_DATA0. Send dummy data address to IPC_DATA1 because some SROM API read memory area pointed by IPC_DATA1. correct a typo.	TVII-SampleSW/common/src/drivers/srom/cy_srom.c TVII-SampleSW/common/src/drivers/srom/cy_srom.h	Modified
2	Clean up the drivers and added api's as per CDT#368048 to support: 1. TX/RX I2S_MODE selection 2. TX/RX_ROUTE_CTL selection	TVII-SampleSW/tviic2d4m/src/drivers/audioss/i2s/cy_i2s.c TVII-SampleSW/tviic2d4m/src/drivers/audioss/i2s/cy_i2s.h TVII-SampleSW/tviic2d6m/src/drivers/audioss/tdm/cy_tdm.c TVII-SampleSW/tviic2d6m/src/drivers/audioss/tdm/cy_tdm.h	Modified
3	Adds api to set the 'I2S_MODE' bit for I2S mode.	TVII-SampleSW/tviic2d4m/src/drivers/audioss/i2s/cy_i2s.h	Modified
4	Prevent unused variable warning in case NDEBUG would be defined (which inactivates CY_ASSERT calls)	All device system sources TVII-SampleSW/tviic2d6m/src/mw/gfx_env/cy_gfx_env.c TVII-SampleSW/tviic2d6mddr/src/mw/gfx_env/cy_gfx_env.c TVII-SampleSW/common/src/drivers/mcwdt/cy_mcwdt.h TVII-SampleSW/common/src/drivers/smif/common/cy_smif.c TVII-SampleSW/tviibh8m/src/mw/smif_mem/cy_smif_hb_flash.c	Modified
5	1. cy_stc_tcpwm_counter_config_t updated with correct members for trigger1/2, changed to trigger0EventCfg/trigger1EventCfg. 2. Config Struct cy_stc_tcpwm_pwm_config_t added with trigger0EventCfg/trigger1EventCfg, immediateKill, pwmOnDisable, Config Struct cy_stc_tcpwm_quaddec_config_t added with trigger0EventCfg/trigger1EventCfg, Config Struct cy_stc_tcpwm_sr_config_t added with trigger0EventCfg/trigger1EventCfg 3. Updates the driver with enum instead of macros for safer access. 4. Update the counter init for the one shot and continuous mode, need to check.	TVII-SampleSW/common/src/drivers/tcpwm/cy_tcpwm.h TVII-SampleSW/common/src/drivers/tcpwm/cy_tcpwm_pwm.c TVII-SampleSW/common/src/drivers/tcpwm/cy_tcpwm_pwm.h TVII-SampleSW/common/src/drivers/tcpwm/cy_tcpwm_quaddec.c TVII-SampleSW/common/src/drivers/tcpwm/cy_tcpwm_quaddec.h TVII-SampleSW/common/src/drivers/tcpwm/cy_tcpwm_sr.c TVII-SampleSW/common/src/drivers/tcpwm/cy_tcpwm_sr.h	Modified
6	1. added a function which cleans and invalidates core cache to syslib. change name "CY_SYSLIB_CACHE_MAINTENANCE" to "CY_SYSLIB_CORE_D_CACHE_MAINTENANCE". 2. Add CY_MIN / CY_MAX macros, unconditionally include string.h to prevent potential future issues when NDEBUG is defined.	TVII-SampleSW/common/src/drivers/syslib/cy_syslib.c TVII-SampleSW/common/src/drivers/syslib/cy_syslib.h	Addition
7	1. Correct copy and past error (CY_ETH_DEFINE_TOTAL_BD_PER_TXQUEUE -> CY_ETH_DEFINE_TOTAL_BD_PER_RXQUEUE) 2. Use syslib cache maintenance functions. delete unreasonable comments.	TVII-SampleSW/tviibh8m/src/drivers/ethernet/edd.c TVII-SampleSW/tviibh8m/src/drivers/ethernet/cy_ethif.c	Modified
8	Updates the system_init() to enable PLL5 from PLL400[5] to PLL200[0] for PSVP.	TVII-SampleSW/tviic2d6mddr/src/system/rev_a/system_tviic2d6mddr_cm0plus.c	Modified
9	Adapted the USB-UART interface definition for BSP macros generated from tool.	TVII-SampleSW/common/src/mw/semihosting/cy_semihosting.c	Modified
10	Updates the external slew_rate and drive_sel api's as per gpio_v5 updates.	TVII-SampleSW/common/src/drivers/gpio/cy_gpio.c TVII-SampleSW/common/src/drivers/gpio/cy_gpio.h	Addition
11	PDMA/MDMA: Add enum for trigger input deactivation type, add declaration for SW trigger APIs and fix copy/paste issue of that function in PDMA	TVII-SampleSW/common/src/drivers/dma/cy_mdma.h TVII-SampleSW/common/src/drivers/dma/cy_pdma.h	Modified
12	Use __ALIGNED(x) macro from CMSIS compiler abstraction header files	TVII-SampleSW/common/src/drivers/srom/cy_srom.c TVII-SampleSW/tviibh8m/src/drivers/ethernet/cy_ethif.c	Modified
13	FreeRTOS-Kernel-10.4.6 https://github.com/FreeRTOS/FreeRTOS-Kernel/releases/tag/V10.4.6 released this Nov 13, 2021	TVII-SampleSW/common/src/rtos	Modified

18 Change Log from v7.2.0 to v7.3.0

Sl. No.	Change	Files	Action
1	Add GHS --no_wrap_diagnostics option (consumer shall decide whether to wrap long output messages, can simplify some parsers if not wrapped)	T2G-SampleSW/tviixxx/tools/ghs/options_global.opt	Updated
2	add preprocessor check for existence of CM7_1	T2G-SampleSW/common/src/drivers/sysint/cy_sysint.c	Updated
3	Update with CYT2CL. tviice4m workspaces updated accordingly. Latest update with fix for ETB. Addition of CYT4EN. JTAG issues fixed.	T2G-SampleSW/misc/tools/iar/IAR_EWARM_8421_FlashLoader_Patch_TraveoII.7z	Updated
4	Adds api's for the EMPU unit from LPDDR4, only applicable for CYT4EN device.	T2G-SampleSW/common/src/drivers/prot/cy_prot.c T2G-SampleSW/common/src/drivers/prot/cy_prot.h	Updated
5	fixed a bug. SMIF cores were using common variable which each core should have its own. add #if defined(CY_SMIF_DRV_SMIF0_CORE1) so that compile succeeds for device which does not have SMIF Core 1.	T2G-SampleSW/common/src/drivers/smif/common/cy_smif.c T2G-SampleSW/common/src/drivers/smif/common/cy_smif.h	Updated
6	SwitchToExternal modified to get rid of the warning. Minor adjustments and corrections for SROM API calls. Add "if else" to separate VADJ setting by OFFSET value. Definition of "VADJ" changed,thus code updated. Handover Code has been updated. 1. Deleted the enable PMIC by register setting. 2. Updated the code according by AN-case2. The value of "VoltageAdjust" has been updated.	T2G-SampleSW/tviibh8m/src/mw/power/cy_power.c	Updated
7	Change the PMIC status wait time. AN suggest the value greater than 0.	T2G-SampleSW/tviibh8m/src/system/rev_d/system_tviibh8m_cm0plus.c	Updated
8	Changed function "Cy_IPC_Drv_SendMsgWord" to "Cy_IPC_Drv_SendMsgWord_2", it is used to send two 32-bit word message. Add parameters for API"LoadregulatorTrim".	T2G-SampleSW/common/src/drivers/srom/cy_srom.c T2G-SampleSW/common/src/drivers/srom/cy_srom.h	Updated
9	fix Cy_SysClk_ClkBak_LPECO_PrescalarOkay	T2G-SampleSW/tviibh8m/src/drivers/sysclk/cy_sysclk.h	Updated
10	cy_delayFreqMhz changed from uint8_t to unit32_t. Deleted the "useSromApi" in each file for BH and C2D devices	All device system sources	Updated
11	add workaround comment.	T2G-SampleSW/common/src/drivers/trigmux/cy_trigmux.c	Updated
12	tviic2d6m (GHS): Add offchip trace config for 327-BGA board (MCU Rev. B) and make it the default	T2G-SampleSW/tviic2d6m/tools/ghs/debugging/tvii_debug.py	Updated
13	user programmable SFLASH sections and WF added.	All devices latest revision IAR linker script files (*.icf) T2G-SampleSW/tviibe1m/tools/iar/linker_directives_tviibe_rev_d.icf T2G-SampleSW/tviibe2m/tools/iar/linker_directives_tviibe_rev_c.icf T2G-SampleSW/tviibe4m/tools/iar/linker_directives_tviibe4m.icf T2G-SampleSW/tviibe512k/tools/iar/linker_directives_tviibe512k.icf T2G-SampleSW/tviibh4m/tools/iar/linker_directives_tviibh.icf T2G-SampleSW/tviibh8m/tools/iar/linker_directives_tviibh_rev_c.icf T2G-SampleSW/tviic2d4m/tools/iar/linker_directives_tviic2d4m.icf T2G-SampleSW/tviic2d6m/tools/iar/linker_directives_tviic2d_rev_b.icf T2G-SampleSW/tviic2d6mddr/tools/iar/linker_directives_tviic2d6mddr.icf T2G-SampleSW/tviice4m/tools/iar/linker_directives_tviice4m.icf	Updated
14	support 2048, 3072 bits key length.	All device Crypto RSA examples	Updated
15	flt structure generated via the tool.	T2G-SampleSW/tviibe1m/src/drivers/sysflt/cy_sysflt_config.h T2G-SampleSW/tviibe512k/src/drivers/sysflt/cy_sysflt_config.h T2G-SampleSW/tviibh8m/src/drivers/sysflt/cy_sysflt_config.h T2G-SampleSW/tviic2d4m/src/drivers/sysflt/cy_sysflt_config.h T2G-SampleSW/tviic2d6m/src/drivers/sysflt/cy_sysflt_config.h T2G-SampleSW/tviic2d6mddr/src/drivers/sysflt/cy_sysflt_config.h T2G-SampleSW/tviice4m/src/drivers/sysflt/cy_sysflt_config.h	Updated

16	in Cy_Lpddr_ControllerInit() -replaced the time to wait for PLL lock CY_LPDDR4_PLL_MAX_LOCKTIME_ABOVE_7P92MHZ --> CY_LPDDR4_PLL_STABILIZATION_TIME through a common longer time as Cy_SysLib_DelayUs() does not delivery very accurate intervals - in cy-lpddr4.c function Cy_Lpddr_SendCmd() Disable Interrupts during programming commands to the controller and updating the driver internal controller state . Without this change it can happen that driver internal state gets out of sync. hence Cy_Lpddr_GetControllerRunState() deliver wrong ControllerRunState. Following user commands causing GSM_Fault because of wrong controller state. Check CDT 377697 - corrected the delay time in the PSVP Fake Training instead of 10us =>100us as we are running only with 80MHz	T2G-SampleSW/tviic2d6mddr/src/drivers/lpddr4/cy_lpddr4.c T2G-SampleSW/tviic2d6mddr/src/drivers/lpddr4/cy_lpddr4.h	Updated
17	1. fix bug in Cy_Mixer_SourceInit 2. add a function Cy_Mixer_Dst_FIFO_Used which reads FIFO used.	T2G-SampleSW/tviic2d6m/src/drivers/audioss/mixer/cy_mixer.c T2G-SampleSW/tviic2d6m/src/drivers/audioss/mixer/cy_mixer.h	Updated
18	Add Cy_EthIf_ProvideTxBuffer, Cy_EthIf_TransmitTrigger. Add PTP supporting functions. increase number of TX descriptor Support D cache enabled. - MDIO: Wrong logic state for polling was used ? with correct setting I believe you should be able to remove the wait-API call - u8EthIfInstance variable value was used before set to the right value ! leading to potential memory corruption - the Cy_EthIf_ClearBuffer calls are bad for performance add Cy_EthIf_SetTimerCompValue clean up refactor. - repeated expression to a routine such as deriving eth index, instances. - remove unused local variables. - make local variable scope shorter - rename variable - some uint8_t variable -> uint32_t variable - arbitrary change. combine cy_ethif_defines.h with cy_ethif.h remove unused parameter from function of providing buffer	T2G-SampleSW/tviibh8m/src/drivers/ethernet/cy_ethif.c T2G-SampleSW/tviibh8m/src/drivers/ethernet/cy_ethif.h T2G-SampleSW/tviibh8m/src/drivers/ethernet/cy_ethif_defines.h T2G-SampleSW/tviibh8m/src/drivers/ethernet/edd.c	Updated
19	Updated the die temperature measurement algorithm for approximation loop (RECALCULATE:) in the case of invalid calculated temperature.	T2G-SampleSW/common/src/drivers/adc/cy_adc.c	Updated
20	added dp83867 utilities for tviic2d4m/6m/6mddr	T2G-SampleSW/tviic2d6m/src/mw/eth_phy/cy_dp83867.c T2G-SampleSW/tviic2d6m/src/mw/eth_phy/cy_dp83867.h	Added

19 Change Log from v7.1.0 to v7.2.0

Sl. No.	Change	Files	Action
1	SDL FOSS package report added (Only Arm CMSIS modified files are listed)	docs/	Addition
2	All system sources and headers, startup assembly files. - Arm license details removed. - These can be adapted and will be local to where used.	NA	Modified
3	Device addition tviice4m, flash patch is not yet updated	T2G-SampleSW/tviice4m	Addition
4	initialization of local variable (smif context of "Cy_SMIF_SEMP_EnableHyperBusInterface").	T2G-SampleSW/tviibh8m/src/mw/smif_mem/cy_smif_semp.c	Modified
5	Doxygen fixes	T2G-SampleSW/common/src/drivers/flash T2G-SampleSW/common/src/drivers/sysrtc T2G-SampleSW/common/src/drivers/trigmux	Modified
6	Change GHS DEVICE define to CYT4DNJBRS ('R' marketing option)	T2G-SampleSW/tviic2d6m/tools/ghs/tviic2d6m_common.gpj	Modified
7	Removed CY_LED_TOGGLE_DELAY definition and usage	T2G-SampleSW/common/hdr/cy_project.h	Removed
8	. added the Quality of Service Registers to the lpddr4 config structure . change for Mode Register read when controller is running. The command must be send subsequentially to the controller as the controller can not handle the MRR reuqest to both channels when controller is running. . fixed issue which was present when reading DQS Oscillator sometimes catch old value triggering a retrain request. some correction for the release done this morning moved the static fuction to *.c added the inline function with extern inline to the *.c file to avoid compile error with IAR	T2G-SampleSW/tviic2d6mddr/src/drivers/lpddr4/	Modified
9	LPDDR4 update for compilation	T2G-SampleSW/tviic2d6mddr/tools/ghs/_gpj/libsdl_source.gpj	Addition
10	Adding special label __iar_init$$done to vector table definition in startup assembly files.	T2G-SampleSW/common/src/startup/iar/	Modified
11	improve interface of capture mode setting APIs more functional name for enum of ddr capture mode.	T2G-SampleSW/common/src/drivers/smif/ver4/cy_smif_ver_specific.c T2G-SampleSW/common/src/drivers/smif/ver4/cy_smif_ver_specific.h	Modified
12	update smif example/mw. S28H mode detecting function improved	T2G-SampleSW/tviibh8m/src/mw/smif_mem/cy_smif_semp.c T2G-SampleSW/tviibh8m/src/mw/smif_mem/cy_smif_semp.h	Modified
13	passTr setting: not use API (synchronize with rev_c)	T2G-SampleSW/tviibh8m/src/system/rev_d/system_tviibh8m_cm0plus.c	Modified
14	Enabling IRQ before SystemInit	All main sources of every device Example: T2G-SampleSW/tviibh4m/src/main_cm0plus.c T2G-SampleSW/tviibh4m/src/main_cm7_0.c T2G-SampleSW/tviibh4m/src/main_cm7_1.c	Modified
15	The parameters for "ConfigureRegulator" has been updated to the latest version.	T2G-SampleSW/common/src/drivers/srom/cy_srom.h T2G-SampleSW/tviibh8m/src/mw/power/cy_power.c	Modified
16	MPU driver defect: "execute" config value was not used in Cy_MPU_Setup	T2G-SampleSW/common/src/drivers/mpu/cy_mpu.c	Modified

20 Change Log from v7.0.0 to v7.1.0

Sl. No.	Change	Files	Action
1	AUTO ETH added	T2G-SampleSW/tviic2d6m/hdr/rev_b/bb_bsp_tviic2d6m.h	Modified
2	Added ul for integer in Cy_Tcpwm_Pwm_Init	T2G-SampleSW/common/src/drivers/tcpwm/cy_tcpwm_pwm.c	Modified
3	add a reading product index API	T2G-SampleSW/tviibe1m/src/drivers/cpu/cy_cpu.c T2G-SampleSW/tviibe1m/src/drivers/cpu/cy_cpu.h	Addition
4	add path input selection "CY_SYSCLK_CLKPATH_IN_LPECO" only when it is available.	T2G-SampleSW/tviibe1m/src/drivers/sysclk/cy_sysclk.h T2G-SampleSW/tviibe4m/src/drivers/sysclk/cy_sysclk.h T2G-SampleSW/tviibe512k/src/drivers/sysclk/cy_sysclk.h T2G-SampleSW/tviibh8m/src/drivers/sysclk/cy_sysclk.h	Addition
5	LPECO Clock source option added	T2G-SampleSW/common/src/drivers/sysrtc/cy_sysrtc.h	Addition
6	add WCO Enabling option to system files	All device and their revision system headers	Addition
7	Added LPECO definition and API's for CTL, PRESCALAR, STATUS registers in BACKUP domain.	T2G-SampleSW/tviibh8m/src/drivers/sysclk/cy_sysclk.h	Addition
8	. deleted function cy_en_lpddr4_retval_t Cy_Lpddr_ChangeFrequencySetPoint . added function to trigger the DQS2DQ retraining cy_en_lpddr4_retval_t Cy_Lpddr_RequestDQS2DQRetrain . added a function to read LPDDR4 Mode Registers cy_en_lpddr4_retval_t Cy_Lpddr_ReadModeRegister . added function to start the DQS Oscillator which is needed to detect retraining necessity cy_en_lpddr4_retval_t Cy_Lpddr_StartDQSOscillator	T2G-SampleSW/tviic2d6mddr/src/drivers/lpddr4/cy_lpddr4.c T2G-SampleSW/tviic2d6mddr/src/drivers/lpddr4/cy_lpddr4.h	Modified
9	SMIF Documentation fixed	T2G-SampleSW/common/src/drivers/smif/common/cy_smif.h T2G-SampleSW/common/src/drivers/smif/common/cy_smif_memslot.h T2G-SampleSW/common/src/drivers/smif/ver2/cy_smif_ver_specific.h T2G-SampleSW/common/src/drivers/smif/ver3_0/cy_smif_ver_specific.h T2G-SampleSW/common/src/drivers/smif/ver3_1/cy_smif_ver_specific.h T2G-SampleSW/common/src/drivers/smif/ver4/cy_smif_ver_specific.h	Modified
10	Faults updated	T2G-SampleSW/tviic2d6mddr/src/drivers/sysflt/cy_sysflt_config.h T2G-SampleSW/tviic2d6m/src/drivers/sysflt/cy_sysflt_config.h	Modified
11	FreeRTOS, CMSIS licenses added	T2G-SampleSW/common/hdr/cmsis/LICENSE.txt T2G-SampleSW/common/src/rtos/license.txt	Addition
12	Added temporary capture configuration function to adapt changes for ip version v4 on PSVP	T2G-SampleSW/common/src/drivers/smif/ver4/cy_smif_ver_specific.c T2G-SampleSW/common/src/drivers/smif/ver4/cy_smif_ver_specific.h	Modified
13	. moved the initialization of the BISTCFG Registers to Cy_Lpddr_SetupBISTRegister . deleted Cy_Lpddr_ChangeFrequencySetPoint which is no longer needed . commented out timeout time in Cy_Lpddr_WaitUserCMDReady() . Cy_Lpddr_RequestDQS2DQRetrain() added a check of the PTSR2 /3 register id retraining ended without error . changed tRFC Refresh cycle all banks to 280ns --> 180 ns as per datasheet . disabled postpone refresg feature DMCFG .u1REF_POST_PULL_EN = CY_LPDDR4_DISABLED . added some documentation . added CIOR_CHO/CH1 registers in the lpddr4_config these regs are used to set the Command/Address Phy IO driver settings . corrected editor TAB settings . changed some timing seetings to defines from cy_lddr4.h u10T_XSR added JESD209_4B_NS_TXSR,JESD209_4B_NCLK_TXSR, u7T_INIT5 u9T_CAENT u9T_FC u9T_VREFTIMELONG	T2G-SampleSW/tviic2d6mddr/src/drivers/lpddr4/cy_lpddr4.c T2G-SampleSW/tviic2d6mddr/src/drivers/lpddr4/cy_lpddr4.h	Modified
14	Updated the structure and function used for the temperature sensor measurements.	T2G-SampleSW/common/src/drivers/adc/cy_adc.c T2G-SampleSW/common/src/drivers/adc/cy_adc.h	Modified

15	CMSIS 5.7.0: 1. Instruction barrier macros updated 2. Arm architecture 8.1M support added 3. Consistency in using data and return types 4. Addition and fixes for some instructions 5. New APIs for NVIC features for priority encoding, decoding 6. Corrections in some APIs (Set and Get Vectors) 7. Corrections in ITM/ETM Data register definitions 8. Addition of registers for FPU 9. ITM Registers updated for CM7 10. Refactored vector table references for all Cortex-M devices	T2G-SampleSW/common/hdr/cmsis/include	Modified
16	move local var definitions to avoid compiler warnings in PSVP case	T2G-SampleSW/tviic2d6m/src/mw/gfx_env/cy_gfx_env.c	Modified
17	Harmonize i2s driver folder names across devices to prevent confusion Only i2s is used for rev_b I2S handling: - i2s is common across c2d4m a0, c2d6m b0 and c2d6mddr a0 - i2s_rev_a is obviously specific to c2d6m a0	T2G-SampleSW/tviic2d6m/src/drivers/audioss T2G-SampleSW/tviic2d6m/src/drivers/audioss/i2s T2G-SampleSW/tviic2d6m/src/drivers/audioss/i2s_rev_a	Modified
18	removed VRAM, added LPDDR4, moved CM7_x_[I|D]TCM and SMIF1 regions	T2G-SampleSW/tviic2d6mddr/tools/iar/linker_directives_tviic2d6mddr.icf	Modified
19	Fixed PSVP clocks for tviic2d6mddr, fixed usage of hardcoded PSVP frequency value in sysclk driver	T2G-SampleSW/tviibh8m/src/drivers/sysclk/cy_sysclk.c T2G-SampleSW/tviic2d6mddr/src/system/rev_a/system_tviic2d6mddr.h	Modified
20	Corrects the BSP definition under PSVP: 1. Audio SCB slave select pin, 2. TCPWM counters definition for SMART IO block	T2G-SampleSW/tviibh8m/hdr/rev_d/bb_bsp_tviibh8m.h T2G-SampleSW/tviibh4m/hdr/rev_a/bb_bsp_tviibh4m_reva.h T2G-SampleSW/tviibh4m/hdr/rev_a/bb_bsp_tviibh4m_revb.h T2G-SampleSW/tviibh4m/hdr/rev_b/bb_bsp_tviibh4m_reva.h T2G-SampleSW/tviibh4m/hdr/rev_b/bb_bsp_tviibh4m_revb.h	Modified
21	Updates the BSP macro definition for SMART IO for PSVP. Adds macro definition for TCPWM counter for SMART IO.	T2G-SampleSW/tviic2d6m/hdr/rev_a/bb_bsp_tviic2d6m.h T2G-SampleSW/tviic2d6m/hdr/rev_b/bb_bsp_tviic2d6m.h	Modified
22	Fixed temperature measurement state machine code for one of the corner case.	T2G-SampleSW/common/src/drivers/adc/cy_adc.c	Modified
23	added Cy_Lpddr_SetupCAIOCntrlRegs in the CY_Lpddr_ControllerInit() init sequence to setup the Command /Address IO Controll registers. - addd the Cy_pddr_WarmStartRefreshAdjust() to the Cy_Lpddr_ControllerInit() init sequence to check if the memory is already in a temperature range where TREFI needs adjustment or maybe also AC timing derating is needed - deleted the checking of the INTSTT_CH0/CH1 register in Cy_LPDDR_SendCmd. As the faultstructure/faulthandler is working now this additional test is no longer need as we would recognize possible problems by jumping to the faulthandler - new function Cy_Lpddr_PerformTimingDerating handling temperature related timing deration - new function Cy_Lpddr_RefreshandTimingAdjust which reads the MR4 DRAM register and is adjusting Refreshrate tREFI(TREG5) and also calling the Cy_Lpddr_PerformTimingDerating to adjust ´temperature depending timingRegister5	T2G-SampleSW/tviic2d6mddr/src/drivers/lpddr4/cy_lpddr4.c T2G-SampleSW/tviic2d6mddr/src/drivers/lpddr4/cy_lpddr4.h	Modified
24	. HIB Support for 10 pins updated. SIMO Buck related stuffs removed from compilation.	T2G-SampleSW/common/src/drivers/syspm/cy_syspm.c T2G-SampleSW/common/src/drivers/syspm/cy_syspm.h	Modified
25	some macros needed for SEGLCD driver.	T2G-SampleSW/common/src/drivers/syslib/cy_syslib.h	Addition
26	WCO is not available for SK and hence that portion of code is not needed to be executed.	T2G-SampleSW/tviibe1m/src/system/rev_d/system_cyt2b7.h T2G-SampleSW/tviibe2m/src/system/rev_c/system_cyt2b9.h	Modified
27	Updated the QSPI memory device definition to "CY_SMIF_S25FXXXS" for soldered board.	T2G-SampleSW/tviic2d4m/hdr/rev_a/bb_bsp_tviic2d4m.h	Modified
28	Updates the Button IRQ macro and SW reference as per the CPU board.	T2G-SampleSW/tviic2d6m/hdr/rev_b/bb_bsp_tviic2d6m.h	Modified
29	CM0+ SystemInit now takes care of globally enabling VIDEOSS IP (and power if applicable), so that VRAM is available already during CM7 startup. GfxEnv_EnableTestImage adapted accordingly	T2G-SampleSW/tviic2d4m/src/system/rev_a/system_tviic2d4m_cm0plus.c T2G-SampleSW/tviic2d6m/src/mw/gfx_env/cy_gfx_env.c T2G-SampleSW/tviic2d6m/src/system/rev_a/system_tviic2d6m_cm0plus.c T2G-SampleSW/tviic2d6m/src/system/rev_b/system_tviic2d6m_cm0plus.c	Modified

30	Cy_Tcpwm_ClearInterrupt doesn't have the code to readback the register after writing ptscTCPWM->unINTR.u32Register. Additional fix for SetInterrupt API to look at correct register.	T2G-SampleSW/common/src/drivers/tcpwm/cy_tcpwm.c	Modified
31	Replaced the defined delay with status check: -> Poll until read bit is set from Cy_Rtc_SyncRegisters() -> Wait until busy bit is cleared from Cy_Rtc_WriteEnable()	T2G-SampleSW/common/src/drivers/sysrtc/cy_sysrtc.c	Modified
32	IAR Patch updated	T2G-SampleSW/misc/tools/iar/IAR_EWARM_8421_FlashLoader_Patch_TraveoII.7z	Addition

21 Change Log from v6.6.0 to v7.0.0

Sl. No.	Change	Files	Action
1	Added SRAM-ECC example.	T2G-SampleSW/tviic2d6m/src/examples/sram T2G-SampleSW/tviic2d6m/src/examples/sram/ecc T2G-SampleSW/tviic2d6m/src/examples/sram/ecc/main_cm0plus.c T2G-SampleSW/tviic2d4m/src/examples/sram T2G-SampleSW/tviic2d4m/src/examples/sram/ecc T2G-SampleSW/tviic2d4m/src/examples/sram/ecc/main_cm0plus.c	Added
2	New driver addition	T2G-SampleSW/tviic2d6mddr/src/drivers/lpddr4/cy_lpddr4.c T2G-SampleSW/tviic2d6mddr/src/drivers/lpddr4/cy_lpddr4.h	Added
3	tvii_debug.py now clears some control bits in DHCSR before triggering reset to prevent a potential debugger issue GHS tvii_debug.py now prints a solution hint for updating ODB file if flashing results in "Could not detect flash device"	T2G-SampleSW/tviibe1m/tools/ghs/debugging/tvii_debug.py T2G-SampleSW/tviibe2m/tools/ghs/debugging/tvii_debug.py T2G-SampleSW/tviibe4m/tools/ghs/debugging/tvii_debug.py T2G-SampleSW/tviibe512k/tools/ghs/debugging/tvii_debug.py T2G-SampleSW/tviibh4m/tools/ghs/debugging/tvii_debug.py T2G-SampleSW/tviibh8m/tools/ghs/debugging/tvii_debug.py T2G-SampleSW/tviic2d4m/tools/ghs/debugging/tvii_debug.py T2G-SampleSW/tviic2d6m/tools/ghs/debugging/tvii_debug.py T2G-SampleSW/tviic2d6mddr/tools/ghs/debugging/tvii_debug.py	Modified
4	Added pin definition for CXPI channel in PSVP. Updated the CAN channel 0 and 1 macro supported by C2D6M-B0-PSVP.	T2G-SampleSW/tviic2d6m/hdr/rev_b/bb_bsp_tviic2d6m.h	Added
5	Device headers for rev_b added	T2G-SampleSW/tviic2d6m/hdr/rev_b	Added
6	This is a driver from c2d4m and tdm v2.0.	T2G-SampleSW/tviic2d6m/src/drivers/audioss/i2s_v2	Added
7	smif rev and i2s for 6m b0 changed	T2G-SampleSW/common/hdr/cy_project.h Workspaces adapted accordingly	Modified
8	change inclusion of some drivers based on MCU revision, update SMIF instance calculation because of different define meaning due to SMIF4.0, comment more code to prevent warnings	T2G-SampleSW/common/src/drivers/smif/ver4/cy_smif.h T2G-SampleSW/tviic2d6m/src/mw/gfx_env/cy_gfx_env.h T2G-SampleSW/tviic2d6m/tools/ghs/_gpj/libsdl_source.gpj	Modified
9	Adapted delay tap function	T2G-SampleSW/common/src/drivers/smif/ver4/cy_smif.c T2G-SampleSW/common/src/drivers/smif/ver4/cy_smif.h	Modified
10	Updated port assigns for SMARTIO (100-pin) EXT_CLK Port has been updated CAS/CAE devices added.	T2G-SampleSW/tviibe512k/hdr/rev_a/bb_bsp_tviibe512k.h	Modified
11	272-BGA framework added. Added BSP macros for B-H-8M-272 BGA Package	T2G-SampleSW/tviibh8m/hdr/rev_d/bb_bsp_tviibh8m.h	Modified
12	removed reputations of LED and ETH for 272. Updated proper pins for BB_LIN2 and Assigned proper SS Pin for BB_SPI_EEPROM.	T2G-SampleSW/tviibh4m/hdr/rev_b/bb_bsp_tviibh4m_revb.h	Modified
13	Workaround for 1 bit shift instructions.	T2G-SampleSW/common/src/drivers/crypto/src/cy_crypto_core_vu_hw.h	Modified
14	rev_a -> rev_d to match DS revision.	T2G-SampleSW/tviibe512k/hdr/rev_a T2G-SampleSW/tviibe512k/hdr/rev_d Workspaces also adapted	Modified
15	Update ECO configuration according to user guide.	T2G-SampleSW/tviibe1m/src/drivers/sysclk/cy_sysclk.c T2G-SampleSW/tviibe1m/src/drivers/sysclk/cy_sysclk.h	Modified
16	added ISB() instruction where required. removed comments which is no longer required.	T2G-SampleSW/common/src/drivers/prot/cy_prot.c T2G-SampleSW/common/src/drivers/prot/cy_prot.h	Modified
17	support svc handler in C.	T2G-SampleSW/common/src/drivers/syslib/cy_syslib.c T2G-SampleSW/common/src/startup/ghs/startup_cm0plus.arm T2G-SampleSW/common/src/startup/ghs/startup_cm4.arm T2G-SampleSW/common/src/startup/ghs/startup_cm7.arm T2G-SampleSW/common/src/startup/iar/startup_cm0plus.s T2G-SampleSW/common/src/startup/iar/startup_cm4.s T2G-SampleSW/common/src/startup/iar/startup_cm7.s	Added
18	crypto library reference corrections in some and tuning in all. Addition of button/sw_timer mw, which was missing, to stay consistent across projects.	IAR workspaces	Modified
19	Integrated Starter Kit SW into SDL	BE1M and BE2M devices	Added
20	remove pc_save accessing code. added comments for cy_en_prot_pc_t. e.g. PC0 can't be configured	T2G-SampleSW/common/src/drivers/prot/cy_prot.c T2G-SampleSW/common/src/drivers/prot/cy_prot.h	Modified
21	Fix wrong usage of CY_ASSERT in GfxEnv middleware and examples	T2G-SampleSW/tviic2d6m/src/mw/gfx_env/cy_gfx_env.c	Modified
22	Fix wrong usage of CY_ASSERT in all system and driver files	All device system and driver files	Modified

23	add smif version specific driver.	T2G-SampleSW/common/hdr/cy_project.h T2G-SampleSW/tviibh8m/src/mw/smif_mem/cy_smif_device_common.c T2G-SampleSW/tviibh8m/src/mw/smif_mem/cy_smif_device_common.h T2G-SampleSW/tviibh8m/src/mw/smif_mem/cy_smif_hb_flash.c T2G-SampleSW/tviibh8m/src/mw/smif_mem/cy_smif_hb_flash.h T2G-SampleSW/tviibh8m/src/mw/smif_mem/cy_smif_s25fl.c T2G-SampleSW/tviibh8m/src/mw/smif_mem/cy_smif_s25fl.h T2G-SampleSW/tviibh8m/src/mw/smif_mem/cy_smif_s25fs.c T2G-SampleSW/tviibh8m/src/mw/smif_mem/cy_smif_s25fs.h T2G-SampleSW/tviibh8m/src/mw/smif_mem/cy_smif_semp.c T2G-SampleSW/tviibh8m/src/mw/smif_mem/cy_smif_semp.h T2G-SampleSW/tviic2d6m/src/mw/gfx_env/cy_gfx_env.c T2G-SampleSW/tviic2d6m/src/mw/gfx_env/cy_gfx_env.h	Modified
24	support dlp functionality.	T2G-SampleSW/tviibh8m/src/mw/smif_mem/cy_smif_semp.c T2G-SampleSW/tviibh8m/src/mw/smif_mem/cy_smif_semp.h T2G-SampleSW/common/src/drivers/smif/ver2/cy_smif_ver_specific.c T2G-SampleSW/common/src/drivers/smif/ver2/cy_smif_ver_specific.h T2G-SampleSW/common/src/drivers/smif/ver3_0/cy_smif_ver_specific.c T2G-SampleSW/common/src/drivers/smif/ver3_0/cy_smif_ver_specific.h T2G-SampleSW/common/src/drivers/smif/ver3_1/cy_smif_ver_specific.c T2G-SampleSW/common/src/drivers/smif/ver3_1/cy_smif_ver_specific.h T2G-SampleSW/common/src/drivers/smif/ver4/cy_smif_ver_specific.c T2G-SampleSW/common/src/drivers/smif/ver4/cy_smif_ver_specific.h	Added
25	update ECO configure function in clock driver.	T2G-SampleSW/tviibe1m/src/drivers/sysclk/cy_sysclk.c T2G-SampleSW/tviibe1m/src/drivers/sysclk/cy_sysclk.h T2G-SampleSW/tviibh8m/src/drivers/sysclk/cy_sysclk.c T2G-SampleSW/tviibh8m/src/drivers/sysclk/cy_sysclk.h T2G-SampleSW/tviibe4m/src/drivers/sysclk/cy_sysclk.c T2G-SampleSW/tviibe4m/src/drivers/sysclk/cy_sysclk.h	Modified
26	FreeRTOS sources added from v202011.00 All devices configured to support in dual mode only, only be2m and c2d4m devices tested	T2G-SampleSW/common/src/rtos/	Added
27	New device headers added	tviic2d6mddr rev_a, tviic2d6m rev_b	Added
28	Change Cy_Flashc_InvalidateFlashCacheBuffer and Cy_Flashc_InvalidateFlashBuffer to ensure completion by HW	T2G-SampleSW/common/src/drivers/flash/cy_flash.h	Modified
29	added functions accessing BACKUP CAL_OUT.	T2G-SampleSW/common/src/drivers/sysrtc/cy_sysrtc.c T2G-SampleSW/common/src/drivers/sysrtc/cy_sysrtc.h	Added
30	Update from IAR	T2G-SampleSW/misc/tools/iar/IAR_EWARM_8421_FlashLoader_Patch_TraveoII.7z	Modified
31	fix flash check sum function.	T2G-SampleSW/common/src/drivers/flash/cy_flash.c T2G-SampleSW/common/src/drivers/flash/cy_flash.h T2G-SampleSW/common/src/drivers/srom/cy_srom.c T2G-SampleSW/common/src/drivers/srom/cy_srom.h	Modified
32	Add 6M-DDR PSVP	T2G-SampleSW/misc/tools/ghs/ghs_comp_xxxxxx_defaults_flash/flash_chips_fcr4tcm.odb T2G-SampleSW/misc/tools/ghs/ghs_comp_xxxxxx_defaults_flash/generator/tvii_chip_list.csv	Added
33	Move setting of global component enable bits in VIDEOSS from Cy_GfxEnv_Init to Cy_GfxEnv_EnableTestImage	T2G-SampleSW/tviic2d6m/src/mw/gfx_env/cy_gfx_env.c	Modified
34	uint8_t offset to int8_t uint8_t gain to int8_t	T2G-SampleSW/common/src/drivers/adc/cy_adc.h	Modified
35	added interrupt register readback, when clearing interrupt flag.	T2G-SampleSW/common/src/drivers/sysflt/cy_sysflt.c	Added

22 Change Log from v6.5.0 to v6.6.0

Sl. No.	Change	Files	Action
1	CM7 startup code: Added dummy read of CPUSS_CM7_X_CTL register to ensure that the changed setting is effective before proceeding	T2G-SampleSW/common/src/startup/ghs/startup_cm7.arm T2G-SampleSW/common/src/startup/iar/startup_cm7.s	Modified
2	Crypto libs (GHS build) added for tviibe512k and tviibe4m	T2G-SampleSW/ghs_build_crypto_libs.bat T2G-SampleSW/tviibe4m/src/drivers/crypto/libs/libcrypto_client_cm4_ghs.a T2G-SampleSW/tviibe4m/src/drivers/crypto/libs/libcrypto_server_cm0plus_ghs.a T2G-SampleSW/tviibe512k/src/drivers/crypto/libs/libcrypto_client_cm4_ghs.a T2G-SampleSW/tviibe512k/src/drivers/crypto/libs/libcrypto_server_cm0plus_ghs.a	Added
3	tviic2d4m: Make cy_gfx_env svn:external (from tviic2d6m)	T2G-SampleSW/tviic2d4m/src/mw T2G-SampleSW/tviic2d4m/src/mw/gfx_env	Modified
4	cy_gfx_env: Make code for global VIDEOSS IP enabling compatible with old and new register names	T2G-SampleSW/tviic2d6m/src/mw/gfx_env/cy_gfx_env.c	Modified
5	differential clock setup (within ext. memories) is now a config option	T2G-SampleSW/tviic2d6m/src/mw/gfx_env/cy_gfx_env.c T2G-SampleSW/tviic2d6m/src/mw/gfx_env/cy_gfx_env.h	Modified
6	static_inline qualifier was removed to the function Cy_SD_Host_PollTransferComplete and Cy_SD_Host_PollCmdComplete in cy_sd_host.c and also moved these function prototypes to cy_sd_host.h from cy_sd_host.c	T2G-SampleSW/tviibh8m/src/drivers/sd_host/cy_sd_host.c T2G-SampleSW/tviibh8m/src/drivers/sd_host/cy_sd_host.h	Modified
7	SMIF drivers moved from device specific to common based on their respective revisions	T2G-SampleSW/common/src/drivers/smif	Modified
8	. add volatile as required. . from smif ver 3 we have to use TX_DATA_MMIO_FIFO_STATUS for checking fifo status in MMIO mode. . describe connection between driver version and HW ip version. modify tx fifo register to be read. . update so that proper .h file would be included.	T2G-SampleSW/common/src/drivers/smif/ver3_0/cy_smif.h T2G-SampleSW/common/src/drivers/smif/ver3_1/cy_smif.h T2G-SampleSW/common/src/drivers/smif/ver4/cy_smif.h T2G-SampleSW/common/src/drivers/smif/ver2/Readme.txt T2G-SampleSW/common/src/drivers/smif/ver3_0/Readme.txt T2G-SampleSW/common/src/drivers/smif/ver3_0/cy_smif.h T2G-SampleSW/common/src/drivers/smif/ver3_1/Readme.txt T2G-SampleSW/common/src/drivers/smif/ver4/Readme.txt T2G-SampleSW/common/src/drivers/smif/ver2/cy_smif_memslot.c T2G-SampleSW/common/src/drivers/smif/ver2/cy_smif_memslot.h T2G-SampleSW/common/src/drivers/smif/ver3_0/cy_smif_memslot.c T2G-SampleSW/common/src/drivers/smif/ver3_0/cy_smif_memslot.h T2G-SampleSW/common/src/drivers/smif/ver3_1/cy_smif_memslot.c T2G-SampleSW/common/src/drivers/smif/ver3_1/cy_smif_memslot.h	Modified
9	Added code which enable HF1,because HF1 clock can be output from EXT_CLK pin. This is useful when we check the MCU has really gone to DeepSleep mode. examples which use DeepSleep will use EXT_CLK, thus I enabled HF1 by default.	T2G-SampleSW/tviibe1m/src/system/rev_b/system_tviibe1m_cm0plus.c T2G-SampleSW/tviibe1m/src/system/rev_c/system_tviibe1m_cm0plus.c T2G-SampleSW/tviibe1m/src/system/rev_d/system_tviibe1m_cm0plus.c T2G-SampleSW/tviibe512k/src/system/rev_a/system_tviibe512k_cm0plus.c T2G-SampleSW/tviibe2m/src/system/rev_a/system_tviibe2m_cm0plus.c T2G-SampleSW/tviibe2m/src/system/rev_b/system_tviibe2m_cm0plus.c T2G-SampleSW/tviibe2m/src/system/rev_c/system_tviibe2m_cm0plus.c	Modified
10	Delete code which disables FLL in sysInit() which should not be required.	T2G-SampleSW/tviibe1m/src/system/rev_b/system_tviibe1m_cm0plus.c T2G-SampleSW/tviibe1m/src/system/rev_c/system_tviibe1m_cm0plus.c T2G-SampleSW/tviibe1m/src/system/rev_d/system_tviibe1m_cm0plus.c T2G-SampleSW/tviibe2m/src/system/rev_a/system_tviibe2m_cm0plus.c T2G-SampleSW/tviibe2m/src/system/rev_b/system_tviibe2m_cm0plus.c T2G-SampleSW/tviibe2m/src/system/rev_c/system_tviibe2m_cm0plus.c T2G-SampleSW/tviibe4m/src/system/rev_a/system_tviibe4m_cm0plus.c T2G-SampleSW/tviibe512k/src/system/rev_a/system_tviibe512k_cm0plus.c T2G-SampleSW/tviibh4m/src/system/rev_a/system_tviibh4m_cm0plus.c T2G-SampleSW/tviibh4m/src/system/rev_b/system_tviibh4m_cm0plus.c T2G-SampleSW/tviibh8m/src/system/rev_b/system_tviibh8m_cm0plus.c T2G-SampleSW/tviibh8m/src/system/rev_c/system_tviibh8m_cm0plus.c T2G-SampleSW/tviibh8m/src/system/rev_d/system_tviibh8m_cm0plus.c T2G-SampleSW/tviic2d4m/src/system/rev_a/system_tviic2d4m_cm0plus.c T2G-SampleSW/tviic2d6m/src/system/rev_a/system_tviic2d6m_cm0plus.c T2G-SampleSW/tviic2d6m/src/system/rev_b/system_tviic2d6m_cm0plus.c T2G-SampleSW/tviic2d6mddr/src/system/rev_a/system_tviic2d6mddr_cm0plus.c	Modified

11	emulator value correction.delete duplicated changelog.	T2G-SampleSW/tviibh8m/src/drivers/sysclk/cy_sysclk.h	Modified
12	delete dummy define and unnecessary #include.	T2G-SampleSW/tviibh8m/src/mw/smif_mem/cy_smif_hb_flash.c T2G-SampleSW/tviibh8m/src/mw/smif_mem/cy_smif_hb_flash.h	Modified
13	align with cy_sysflt_config.h of T2G-2D-C-6M.	T2G-SampleSW/tviic2d4m/src/drivers/sysflt/cy_sysflt_config.h	Modified
14	add intr status reading function.	T2G-SampleSW/tviic2d4m/src/drivers/audioss/i2s/cy_i2s.h	Modified
15	add VIDOSS power enabling code.	T2G-SampleSW/tviic2d4m/src/system/rev_a/system_tviic2d4m_cm0plus.c	Added
16	some modification/addition mixer driver.	T2G-SampleSW/tviic2d6m/src/drivers/audioss/mixer/cy_mixer.c T2G-SampleSW/tviic2d6m/src/drivers/audioss/mixer/cy_mixer.h	Modified
17	CS42448 mw added	T2G-SampleSW/tviic2d4m/src/mw/audio	Added
18	New I2S driver added	T2G-SampleSW/tviic2d4m/src/drivers/audioss/i2s	Added

23 Change Log from v6.4.0 to v6.5.0

Sl. No.	Change	Files	Action
1	removing MISRA references and tables from comments.	/common/src/drivers/lvd/cy_lvd.h /common/src/drivers/smartio/cy_smartio.h /common/src/drivers/syslib/cy_syslib.h /common/src/drivers/syspm/cy_syspm.h /common/src/drivers/syswdt/cy_syswdt.h	Modified
2	cy_stc_gpio_pin_prt_config_t addition.	/common/src/drivers/gpio/cy_gpio.h	Modified
3	tviibe512k update	/common/src/drivers/canfd/cy_canfd.c /common/src/drivers/flash/cy_flash.h /common/src/drivers/sysint/cy_sysint.c	Modified
4	Drive strength 1/8 removed as it is not supported by T2G devices.	/common/src/drivers/gpio/cy_gpio.h	Modified
5	tviibh4m rev_b addition	/tviibh4m/src/interrupts/rev_b /tviibh4m/src/interrupts/rev_b/cy_interrupt_map.c /tviibh4m/src/interrupts/rev_b/cy_interrupt_map_cm0plus.h /tviibh4m/src/interrupts/rev_b/cy_interrupt_map_cm7_0.h /tviibh4m/src/interrupts/rev_b/cy_interrupt_map_cm7_1.h /tviibh4m/src/system/rev_b /tviibh4m/src/system/rev_b/system_cyt4bb.h /tviibh4m/src/system/rev_b/system_tviibh4m_cm0plus.c /tviibh4m/src/system/rev_b/system_tviibh4m_cm7.c	Added
6	removing MISRA references and tables from comments.	/tviibh8m/src/drivers/sd_host/cy_sd_host.h	Modified
7	removing MISRA references and tables from comments.	/tviibh8m/src/drivers/smif/cy_smif.h	Modified
8	removing MISRA references and tables from comments.	/tviibh8m/src/drivers/audioss/cy_i2s.h	Modified
9	DOXY group correction.	/tviibh8m/src/mw/smif_mem/cy_smif_hb_flash.h	Modified
10	removing MISRA references and tables from comments.	/tviic2d6m/src/drivers/audioss/pwm/cy_pwm.h	Modified
11	use enums from cy_sysclk.h for the targetDiv in system_*_cm0plus.c to reduce potential errors in future	All device and respective revision system .c files ex: tviibh4m/src/system/rev_a/system_tviibh4m_cm0plus.c	Modified
12	synchronized cy_gfx_env.c/h and examples for tviic2d4m and tviic2d6m	tviic2d4m/src/examples/gfx_env/fast_init/main_cm0plus.c tviic2d4m/src/examples/gfx_env/fast_init/main_cm7_0.c tviic2d4m/src/examples/gfx_env/flexible_init/main_cm0plus.c tviic2d4m/src/examples/gfx_env/flexible_init/main_cm7_0.c tviic2d4m/src/mw/gfx_env/cy_gfx_env.c tviic2d4m/src/mw/gfx_env/cy_gfx_env.h tviic2d6m/src/examples/gfx_env/fast_init/main_cm0plus.c tviic2d6m/src/examples/gfx_env/fast_init/main_cm7_0.c tviic2d6m/src/examples/gfx_env/flexible_init/main_cm0plus.c tviic2d6m/src/examples/gfx_env/flexible_init/main_cm7_0.c tviic2d6m/src/mw/gfx_env/cy_gfx_env.c tviic2d6m/src/mw/gfx_env/cy_gfx_env.h	Modified
13	fixed FDPLINK #1 ifdefs	tviic2d6m/src/drivers/fpdlink/cy_fpdlink.c tviic2d6m/src/drivers/fpdlink/cy_fpdlink.h	Modified
14	Modify drive GPIO drive strength definition.	/common/src/drivers/gpio/cy_gpio.h	Modified
15	Get Flash interface frequency function: Bug fixed.	/tviibh8m/src/drivers/sysclk/cy_sysclk.c	Modified
16	added new configure regulator scratch structure.	/common/src/drivers/srom/cy_srom.h	Modified
17	correct header.	/common/src/mw/button/cy_button.c	Modified
18	correct typo.	/common/src/drivers/srom/cy_srom.c	Modified

19	UL -> ul for AN. I2C examples cleaned for AN.	/common/src/drivers/scb/cy_scb_common.c /common/src/drivers/scb/cy_scb_common.h /common/src/drivers/scb/cy_scb_ezi2c.c /common/src/drivers/scb/cy_scb_ezi2c.h /common/src/drivers/scb/cy_scb_i2c.c /common/src/drivers/scb/cy_scb_i2c.h /common/src/drivers/scb/cy_scb_spi.c /common/src/drivers/scb/cy_scb_spi.h /common/src/drivers/scb/cy_scb_uart.c /common/src/drivers/scb/cy_scb_uart.h	Modified
20	added I2S audio DAC/ADC (AIC261 TI) interface.	/common/src/mw/aic261 /common/src/mw/aic261/cy_aic261.c /common/src/mw/aic261/cy_aic261.h	Added/Modified
21	added function which sets multiple pins.	/common/src/drivers/gpio/cy_gpio.c /common/src/drivers/gpio/cy_gpio.h	Modified
22	move cxpi driver to common folder.	tviibe2m/tviic2d4m/tviic2d6m workspaces aligned accordingly	Added/Modified
23	use temporary CPU register for peripheral register bit modification.	/common/src/drivers/tcpwm/cy_tcpwm.c /common/src/drivers/tcpwm/cy_tcpwm.h /common/src/drivers/tcpwm/cy_tcpwm_counter.c /common/src/drivers/tcpwm/cy_tcpwm_counter.h /common/src/drivers/tcpwm/cy_tcpwm_pwm.c /common/src/drivers/tcpwm/cy_tcpwm_pwm.h /common/src/drivers/tcpwm/cy_tcpwm_quaddec.c /common/src/drivers/tcpwm/cy_tcpwm_quaddec.h /common/src/drivers/tcpwm/cy_tcpwm_sr.c /common/src/drivers/tcpwm/cy_tcpwm_sr.h	Modified
24	minor beautify	/common/src/drivers/adc/cy_adc.c	Modified
25	Arbitrary beautify for application note.	/common/src/drivers/adc/cy_adc.c /common/src/drivers/adc/cy_adc.h	Modified
26	make them use SROM API driver. (Interface did not change.)	/common/src/drivers/flash/cy_flash.c /common/src/drivers/flash/cy_flash.h /common/src/mw/flash/cy_mw_flash.c /common/src/mw/flash/cy_mw_flash.h	Modified
27	Add non-blocking functions and other utilities.	/common/src/drivers/srom/cy_srom.c /common/src/drivers/srom/cy_srom.h	Modified
28	Added APIs which can access IPC_DATA1.	/common/src/drivers/ipc/cy_ipc_drv.c /common/src/drivers/ipc/cy_ipc_drv.h	Modified
29	move flash drivers to common folder.	/common/src/drivers/flash /common/src/drivers/flash/cy_flash.c /common/src/drivers/flash/cy_flash.h	Added/Modified
30	align structure definition.	/common/src/drivers/dma/cy_pdma.h	Modified
31	correct comments.	/common/src/drivers/trigmux/cy_trigmux.c	Modified
32	align with driver of B-H	/tviibe1m/src/drivers/sysclk/cy_sysclk.c /tviibe1m/src/drivers/sysclk/cy_sysclk.h	Modified
33	align with deriver of B-E.	/tviibh8m/src/drivers/sysclk/cy_sysclk.c /tviibh8m/src/drivers/sysclk/cy_sysclk.h	Modified
34	Add below functions. cy_en_sysclk_status_t Cy_SysClk_GetGroupFrequency cy_en_sysclk_status_t Cy_SysClk_GetFlashInterfaceFrequency cy_en_sysclk_status_t Cy_SysClk_GetRamFastFrequency cy_en_sysclk_status_t Cy_SysClk_GetRamSlowFrequency cy_en_sysclk_status_t Cy_SysClk_GetRomFastFrequency cy_en_sysclk_status_t Cy_SysClk_GetRomSlowFrequency	/tviibe1m/src/drivers/sysclk/cy_sysclk.c /tviibe1m/src/drivers/sysclk/cy_sysclk.h	Modified
35	clean.	/common/src/drivers/mpu/cy_mpu.c /common/src/drivers/mpu/cy_mpu.h	Modified
36	refactor	/tviibh8m/src/drivers/sysclk/cy_sysclk.c /tviibh8m/src/drivers/sysclk/cy_sysclk.h	Modified
37	increase value of descriptor can be negative value. hence, changed variable type uint32_t -> int32_t.	/common/src/drivers/dma/cy_mdma.h /common/src/drivers/dma/cy_pdma.h	Modified

38	Cleanup for Application note.	/common/src/drivers/dma/cy_mdma.c /common/src/drivers/dma/cy_mdma.h /common/src/drivers/dma/cy_pdma.c /common/src/drivers/dma/cy_pdma.h	Modified
39	clean up for Application Note.	/common/src/drivers/syswdt/cy_syswdt.c /common/src/drivers/syswdt/cy_syswdt.h	Modified
40	clean up for Application Note.	/common/src/drivers/sysrtc/cy_sysrtc.c /common/src/drivers/sysrtc/cy_sysrtc.h	Modified
41	arbitrary clean for smartio for Application note.	/common/src/drivers/smartio/cy_smartio.c /common/src/drivers/smartio/cy_smartio.h	Modified
42	modified the driver to adapt SMIF V3.0 and SMIF V2.0 IP	/tviibh8m/src/drivers/smif/cy_smif.h	Modified
43	IP enable bit name and the control register name is changed in videoss	/tviic2d4m/src/mw/gfx_env/cy_gfx_env.c	Modified

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