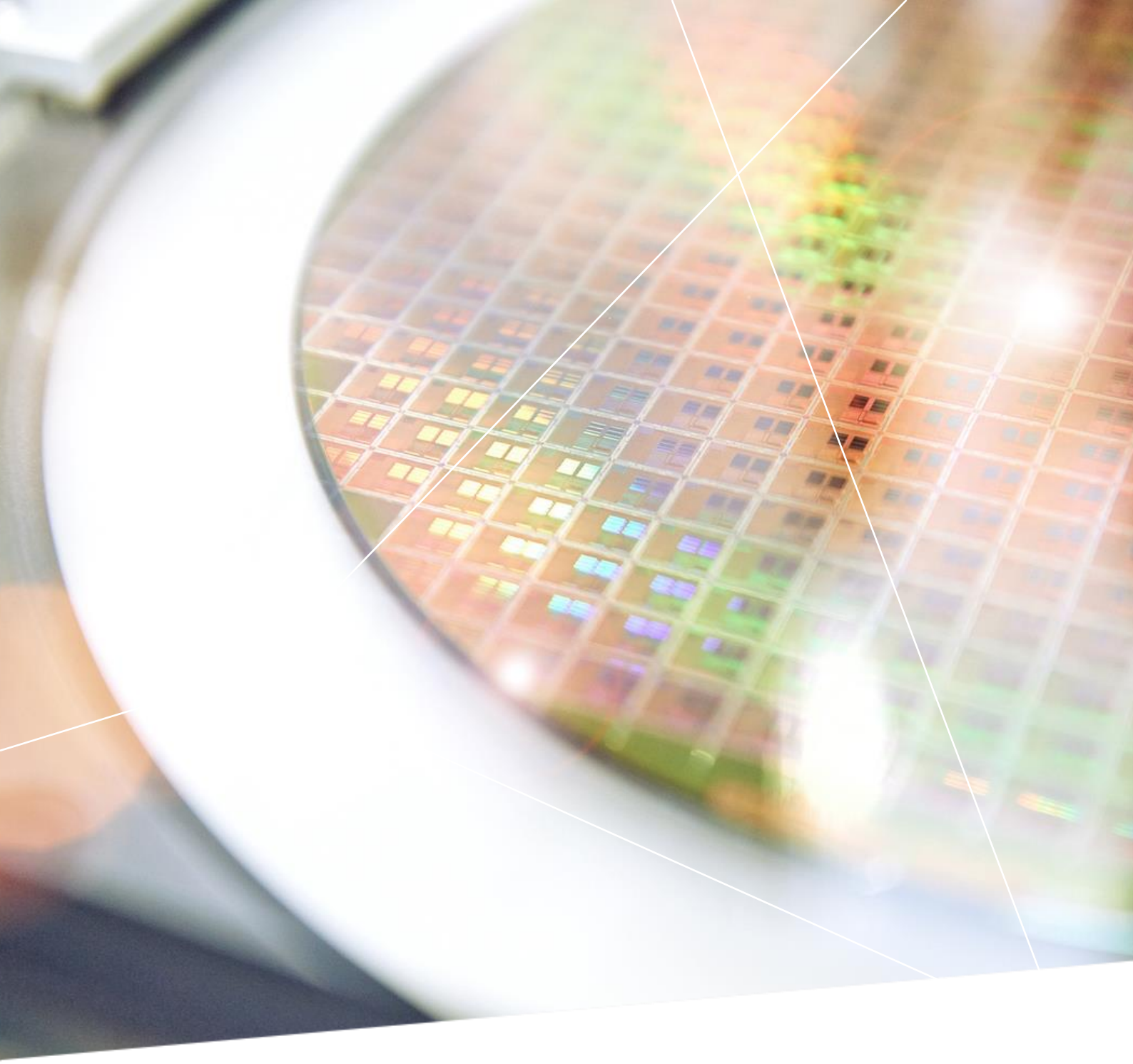

TRAVEO™ T2G SDL Known Issues

v8.1.0, March 6, 2024

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Known Issues

T2G Sample Driver Library

Release Date: March 8, 2024

Thank you for your interest in Infineon TRAVEO™ T2G Sample Driver Library (SDL) version 8.1.0. This document lists the known issues or limitations of the SDL.

Table of Contents

1 SDL Known Issues (CMake build system)

Driver/Feature	Limitation	Remarks
DIAB/GHS + IAR debug	IAR EWARM revision 8.42.1 used in the SDL has a limitation for download and debug output files from other tool chains	Latest revision will have this issue fixed and supported from May 2022
Device support	DIAB supports only TVIIBE1M, IAR/GHS supports all devices	DIAB will be upgraded to support all other devices
Examples test coverage	Only blinky/Semihosting examples are tested for functionality on TVIIBE1M device	All other examples will be randomly tested for next release
GNU GCC	Tested only on TVIIBE1M/TVIIBH8M devices, few functional tests ONLY.	

2 SDL Known Issues (PSVP)

Driver/Feature	Limitation	Remarks
Common		
CAN FD	Maximum CAN FD Data Bit rate (DBR) possible is 2 Mbps, example has only up to 1 Mbps	This is dependent on the PSVP CPU clock, which is limited to 24 MHz
SYSCLK	Cannot be fully tested	PSVP bypasses the clock paths, worst case register access alone could be tested on PSVP
ADC	Examples provide only random counter values	PSVP system does not support analog feature and ADC is just implemented as an internal counter
TVIIBH8M All Revisions		
RESET	Reset tests have not been checked in PSVP	
ETHERNET	Only 10 Mbps MII and RGMII have been tested	
SMIF	XIP program execution not tested	Unavailability of necessary programming tools
FLEXRAY	Not tested with Vector interface	Due to timing limitations of PSVP system, not tested with vector interfaces
TVIIC2D6M rev_a		
RESET	Reset tests have not been checked in PSVP	
ETHERNET	Automotive ethernet has not been tested	
Graphics	Only IRIS Test image rendering has been tested in SDL	
Audioss	None of the modules have been fully tested and not guaranteed to work	Resource and time crunch along with bit-file issues
TVIIC2D4M rev_a		
Basic/Common	Only tested GPIO, interrupt, MultiCore, UART	Remaining examples have not been tested and some of them might have compilation issues
Audioss	TDM/I2S not tested, only PCM-PWM tested	
RESET	Reset tests have not been checked in PSVP	
Graphics	IRIS pattern on Display 0/1	Image not very clear on Display 1
SMIF	Hyperflash and HyperRam	
ETH	Auto Ethernet (100Mbps MII)	
LIN	Only Master tested	
TCPWM	Only PWM tested	
SCB	Only UART feature tested	
TVIIC2D6M rev_b		
SMIF/ETH/LIN	Not tested	
TVIIC2D6MDDR rev_a		
Except for basic download and debug, LPDDR4 partially, no other modules are tested and not guaranteed to work for now.		
TVIICE4M rev_a		
Except for basic download and debug, LEDs, Buttons, Interrupts, UART, no other modules are tested and not guaranteed to work for now.		
TVIIBH16M rev_a		
Supports only 320-BGA device.		

3 SDL Known Issues (TVIIBH4M/TVIIBH8M 176-TEQFP Silicon)

Driver/Feature	Limitation	Remarks
ETHERNET	100 Mbps MII and RMII have been tested	Only Auto ETH available on CPU board, PHY does not support 10 Mbps
SMIF	XIP program execution tested manually programming via the example itself	Unavailability of necessary programming tools
SMIF	Clock only up to 32MHz	

4 SDL Known Issues (TVIIBH8M 320-BGA Silicon)

Driver/Feature	Limitation	Remarks
ETHERNET	RGMII does not seem to be stable	
SMIF	XIP program execution tested manually programming via the example itself	Unavailability of necessary programming tools
SMIF	Clock only up to 90MHz in SDR and 65MHz in DDR	

5 SDL Known Issues (TVIIC2D6M rev_a 500-BGA Silicon)

Driver/Feature	Limitation	Remarks
SMIF	Soldered board has Semper Flash (200MHz) mounted and we need to remove some resistors	R215, R217, R211, R212, R428, R210, R213, R216, R214, R209, R218, R220, R429 (REV_A CPU board only)
SMIF	Hyperflash on socketed boards have a max speed support up to 140MHz (limitation of the device)	
MIPI	Tested two resolutions in RGB888 (800x480, 640x480), capture to display	
TDM	Only waveforms observed	CPU board does not support any audio out
AUDIO DAC	Only waveforms observed	CPU board does not support any audio out

6 SDL Known Issues (TVIIC2D6M rev_a 327-BGA Silicon)

Driver/Feature	Limitation	Remarks
SMIF	Working up to 180MHz with RWDS clock.	
TDM	Only waveforms observed	
VIDEOSS	Only IRIS pattern observed	

7 SDL Known Issues (TVIIC2D4M rev_a/b/c 216-TEQFP Silicon)

Driver/Feature	Limitation	Remarks
SMIF	QSPI Dual Quad mode is not tested.	S25HL device does not support this feature.
TDM	TDM-RX does not support slave configuration	Codec CS42448 support only slave mode in TDM, so CPU should have master mode. Codec workaround: Short R675 and R676 for common MCLK. If I2C calls fail, remove and short resistor R664 and R665.
VIDEOSS	Only IRIS pattern observed	
MIPI	Tested with MIPI sensor module till VRAM data dump in VGA resolution (640x480).	
CXPI	Only waveform is tested in NRZ mode.	CPU board does not support CXPI transceiver.
ETHERNET	Only RMII mode with 10/100 Mbps.	Limitation of device package for MII support.

Generic Note:

1. Supports only CYTVII-C-2D-4M-216-CPU board.

8 SDL Known Issues (TVIIC2D6M rev_b 327-BGA Silicon)

Driver/Feature	Limitation	Remarks
SMIF	DLL unlock issue.	Dual, Quad, Dual Quad Socketed boards do not support. With S28H memory, Normal SDR/Octal SDR/Octal DDR worked and also HyperRAM.
GFXENV	Functional, but external memories shall not be configured.	
CXPI	Clock and TX Data verified; Bus activity observed.	
VIDEOSS Capture	Not tested during the bring up.	

Generic Note:

2. If user intends to trigger REGHC system calls for transitioning to PMIC or external transistor mode by using "useSromApi" as TRUE in Cy_Power_SwitchToPmic(), then user needs to ensure that CM0+ interrupts are enabled before that, for e.g., __enable_irq() should be called before SystemInit() of the associated CM0+ main file.
3. This re-alignment is already taken care for the src/main_*.c files, only examples are not adapted.
4. Only CYTVII-C-2D-6M-327-CPU board is supported.

9 SDL Known Issues (TVIIC2D6M rev_c 327-BGA Silicon)

Driver/Feature	Limitation	Remarks
SMIF	Dual, Quad, Dual Quad SPIs not tested	Dual, Quad, Dual Quad Socketed boards do not support.
GFXENV	Functional, but external memories shall not be configured.	FPD-LINK0, FPD-LINK1, Semi-hosting, User Buttons and SW timer tested.

Generic Note:

1. All the modules were not tested during bring-up.
   ADC, CANFD, CRYPTO, DMA, EVTGEN, SMART IO, IPC, LIN, CXPI, SYSWDT, SYSFLT, TCPWM, TRIGMUX, TDM/I2S, MIXER, DAC, TTL-DISPLAY, TTL-CAPTURE, MIPI-CSI2, JPEG and TRACE were not part of this.

10 SDL Known Issues (TVIICE4M rev_a 176-LQFP Silicon)

Driver/Feature	Limitation	Remarks
SMIF	HyperFlash, HyperRAM tested at 100MHz Single, Dual and QSPI are tested at 80MHz	QSPI devices are not mounted by default.
CXPI	Clock and TX Data verified; Bus activity observed only.	
TRACE	Not tested.	CPU board does not support trace connection by default.

Generic Note:

1. The segmented display viewing angle is vertical only, at an angle some inactive pixel may be visible. Use CM4 application core better performance and refresh rate.
2. Right now, SegLCD driver supports only high-speed clock.

11 SDL Known Issues (TVIIC2D6MDDR rev_a 500-BGA Silicon)

Driver/Feature	Limitation	Remarks
SMIF	180 MHz for Octal and 200 MHz for HYPERRAM	
GFX_ENV	SMIF via GFX_ENV is limited to 100 MHz	
Voltage level	SMIF tested with HSIO_ENH/1.8 V levels, and Ethernet with HSIO_STD/3.3 V levels ONLY	
LPDDR4	Power-up configuration uses HW and SW sequencing, please check the board marking and update CY_SYS_USE_LPDDR4_SEQ	To control the LPDDR4 power sequencing.
System	To configure the LPECO on-board, comment macro CY_SYSTEM_WCO_ENABLE and refer the board user guide for hardware related changes.	Some specific boards have LPECO enable by default.
LPDDR4	LPDDR4 power regulator sequencing timings can be adjusted by macro, CY_SYS_LPDDR4_POWER_DELAY_US	Increase the value in case power related failure are visible.

12 SDL Known Issues (TVIIBH16M rev_a 320-BGA Silicon)

Driver/Feature	Limitation	Remarks
SMIF	Clock only up to 90MHz in SDR and 65MHz in DDR	
SDHC	Tested the module only with Panasonic 8GB eMMC	
Core	Cores are tested with limited power applications	

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