
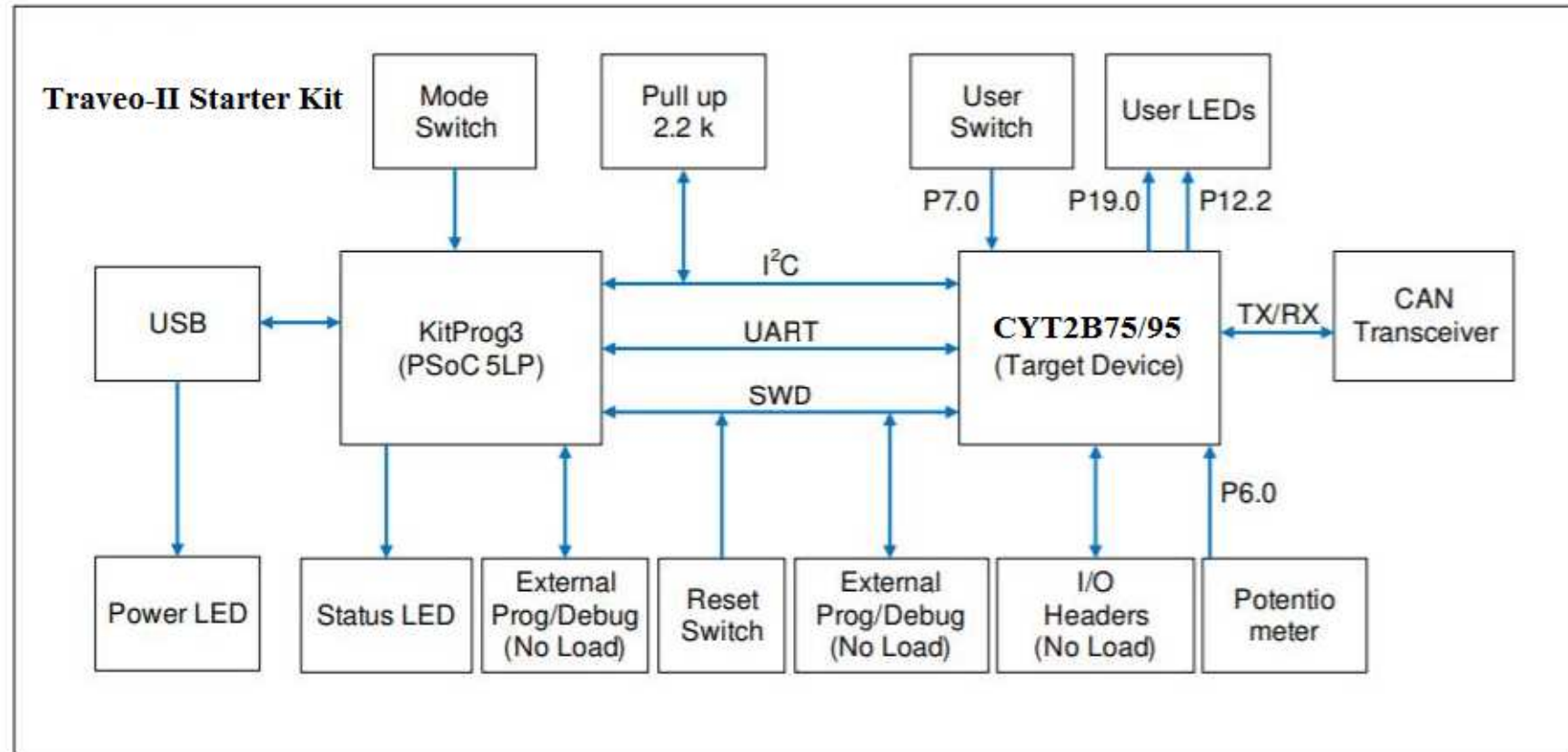


TraveoII Entry Family Starter Kit Rev 03

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BLOCK DIAGRAM



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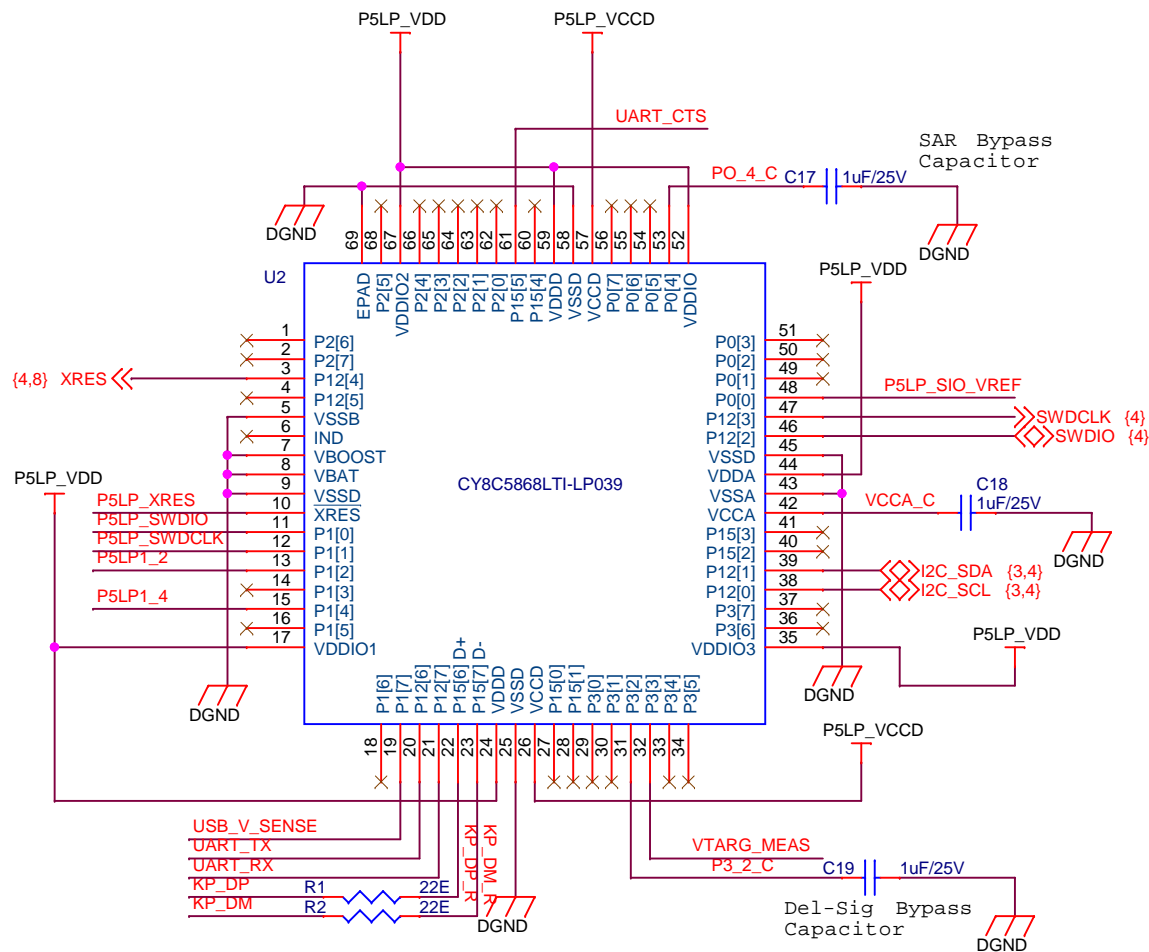
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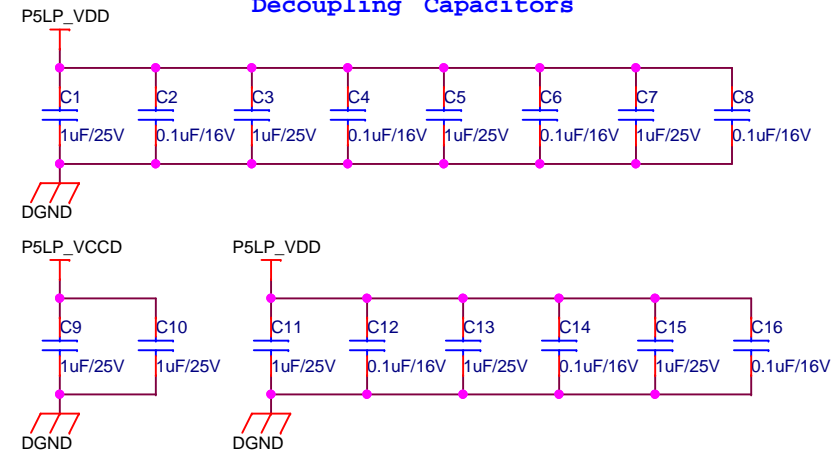
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PSoC 5LP based KitProg3



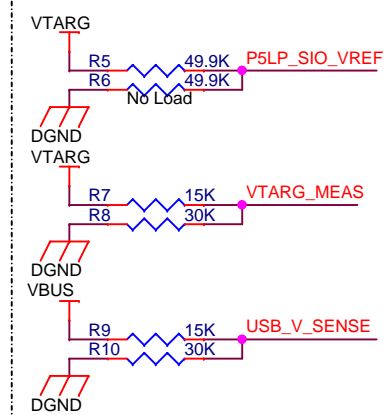
Decoupling Capacitors



KitProg3 Status LED



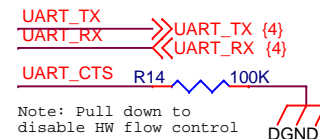
Voltage Monitoring



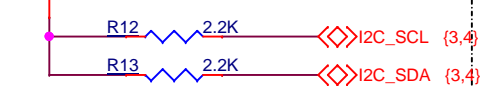
Power LED



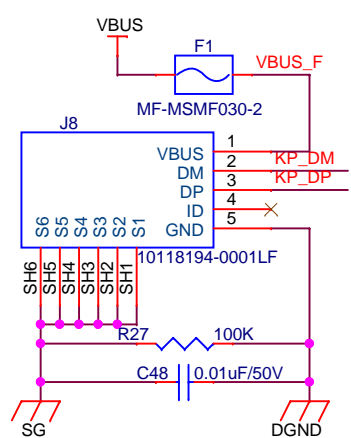
UART Interface



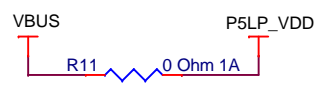
I2C Interface



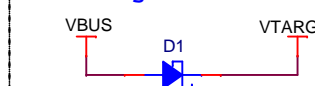
USB Micro Connector



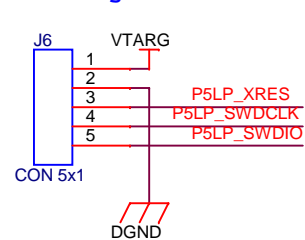
PSoC 5LP Power



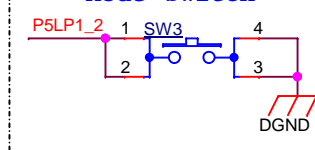
Target Power



PSoC 5LP Program/Debug Connector



Mode Switch



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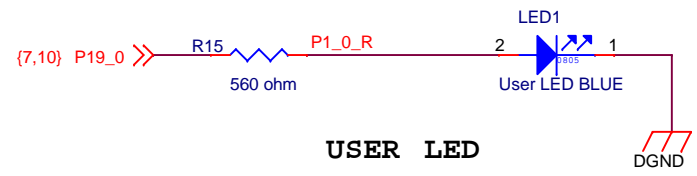
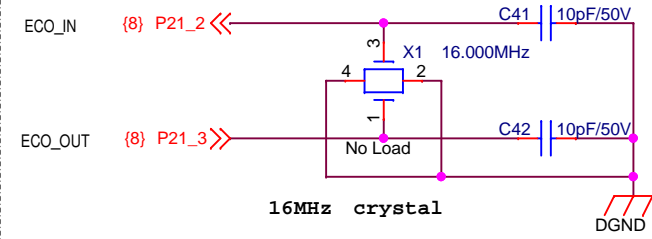
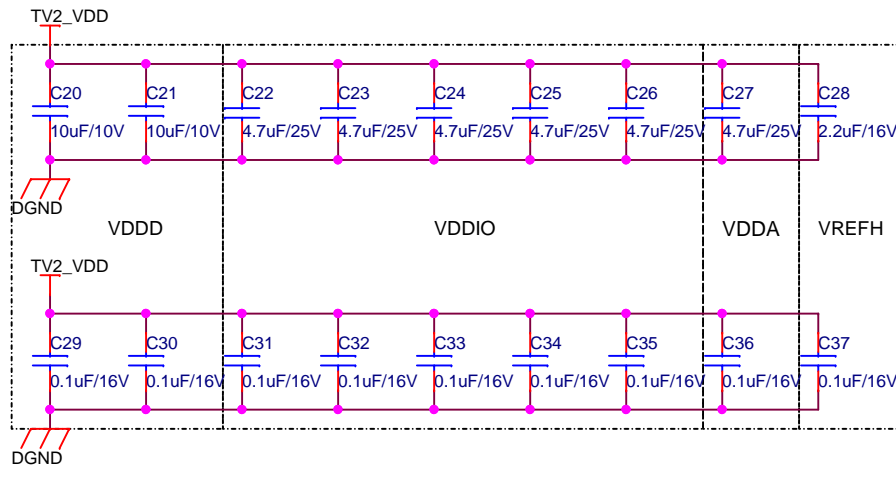
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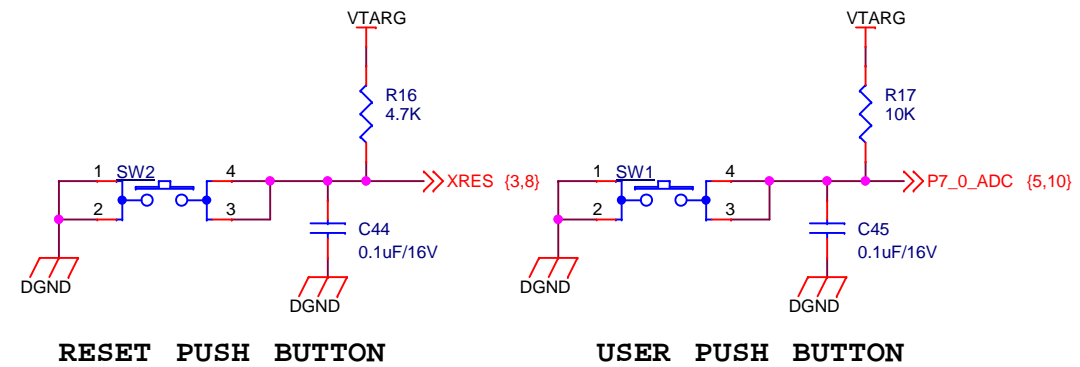
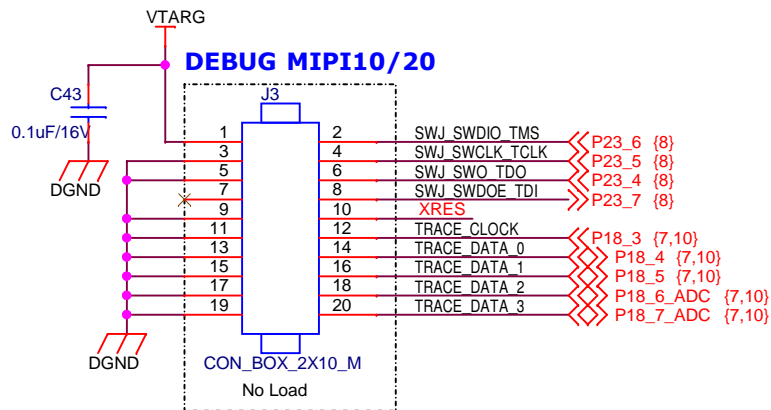
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TVII Decaps, clock, reset, and debug

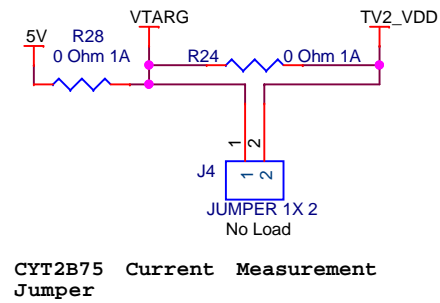
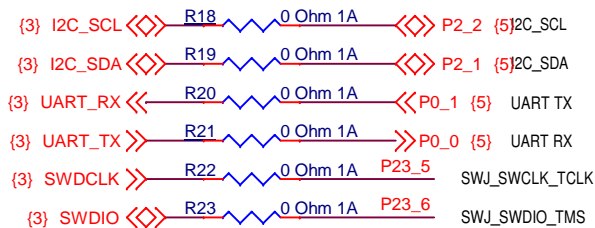
CYT2B75 Decoupling Capacitors



CYT2B75 Program/Debug Header



KitProg3 connection



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U1A

P0_0/PWM_18/PWM_22_N/TC_18_TR0/TC_22_TR1/SCB0_RX/SCB7_SDA/SCB0_MISO/LIN1_RX 2 << P0_0 {4}

P0_1/PWM_17/PWM_18_N/TC_17_TR0/TC_18_TR1/SCB0_TX/SCB7_SCL/SCB0_MOSI/LIN1_TX 3 << P0_1 {4}

P0_2/PWM_14/PWM_17_N/TC_14_TR0/TC_17_TR1/SCB0_RTS/SCB0_SCL/SCB0_CLK/LIN1_EN/CAN0_1_TX 4 << P0_2_SCB0_SCL {10,11}

P0_3/PWM_13/PWM_14_N/TC_13_TR0/TC_14_TR1/SCB0_CTS/SCB0_SDA/SCB0_SEL0/CAN0_1_RX 5 << P0_3_SCB0_SDA {10,11}

P2_0/PWM_7/PWM_8_N/TC_7_TR0/TC_8_TR1/SCB7_RX/SCB0_SEL1/SCB7_MISO/LIN0_RX/CAN0_0_TX/SWJ_TRSTN/TRIG_IN[2] 6 << P2_0 {10}

P2_1/PWM_6/PWM_7_N/TC_6_TR0/TC_7_TR1/SCB7_TX/SCB7_SDA/SCB0_SEL2/SCB7_MOSI/LIN0_TX/CAN0_0_RX/TRIG_IN[3] 7 << P2_1 {4}

P2_2/PWM_5/PWM_6_N/TC_5_TR0/TC_6_TR1/SCB7_RTS/SCB7_SCL/SCB0_SEL3/SCB7_CLK/LIN0_EN/TRIG_IN[4] 8 << P2_2 {4}

P2_3/PWM_4/PWM_5_N/TC_4_TR0/TC_5_TR1/SCB7_CTS/SCB7_SEL0/LIN5_RX/TRIG_IN[5] 9 << P2_3 {10}

P3_0/PWM_1/PWM_2_N/TC_1_TR0/TC_2_TR1/SCB6_RX/SCB6_MISO/TRIG_DBG[0] 10 << P3_0 {10}

P3_1/PWM_0/PWM_1_N/TC_0_TR0/TC_1_TR1/SCB6_TX/SCB6_SDA/SCB6_MOSI/TRIG_DBG[1] 11 << P3_1 {10}

P5_0/PWM_9/PWM_8_N/TC_9_TR0/TC_8_TR1/SCB5_SEL2/LIN7_RX 14 << P5_0 {10}

P5_1/PWM_10/PWM_9_N/TC_10_TR0/TC_9_TR1/LIN7_TX 15 << P5_1 {10}

P5_2/PWM_11/PWM_10_N/TC_11_TR0/TC_10_TR1/LIN7_EN 16 << P5_2 {10}

P5_3/PWM_12/PWM_11_N/TC_12_TR0/TC_11_TR1/LIN2_RX 17 << P5_3 {10}

P6_0/PWM_M_0/PWM_14_N/TC_M_0_TR0/TC_14_TR1/SCB4_RX/SCB4_MISO/LIN3_RX/ADC[0]_0 18 << P6_0_SCB4_MISO {10,11}

P6_1/PWM_0/PWM_M_0_N/TC_0_TR0/TC_M_0_TR1/SCB4_TX/SCB4_SDA/SCB4_MOSI/LIN3_TX/ADC[0]_1 19 << P6_1_SCB4_MOSI {10}

P6_2/PWM_M_1/PWM_0_N/TC_M_1_TR0/TC_0_TR1/SCB4_RTS/SCB4_SCL/SCB4_CLK/LIN3_EN/CAN0_2_TX/ADC[0]_2 20 << P6_2_SCB4_CLK {10}

P6_3/PWM_1/PWM_M_1_N/TC_1_TR0/TC_M_1_TR1/SCB4_CTS/SCB4_SEL0/LIN4_RX/CAN0_2_RX/CAL_SUP_NZ/ADC[0]_3 21 << P6_3_SCB4_SEL0 {10}

P6_4/PWM_M_2/PWM_1_N/TC_M_2_TR0/TC_1_TR1/SCB4_SEL1/LIN4_TX/ADC[0]_4 22 << P6_4_ADC {10}

P6_5/PWM_2/PWM_M_2_N/TC_2_TR0/TC_M_2_TR1/SCB4_SEL2/LIN4_EN/ADC[0]_5 23 << P6_5_ADC {10}

P7_0/PWM_M_4/PWM_3_N/TC_M_4_TR0/TC_3_TR1/SCB5_RX/SCB5_MISO/LIN4_RX/ADC[0]_8 29 << P7_0_ADC {4,10}

P7_1/PWM_15/PWM_M_4_N/TC_15_TR0/TC_M_4_TR1/SCB5_TX/SCB5_SDA/SCB5_MOSI/LIN4_TX/ADC[0]_9 30 << P7_1_SCB5_SDA {10}

P7_2/PWM_M_5/PWM_15_N/TC_M_5_TR0/TC_15_TR1/SCB5_RTS/SCB5_SCL/SCB5_CLK/LIN4_EN/ADC[0]_10 31 << P7_2_SCB5_SCL {10}

P7_3/PWM_16/PWM_M_5_N/TC_16_TR0/TC_M_5_TR1/SCB5_CTS/SCB5_SEL0/ADC[0]_11 32 << P7_3_ADC {10}

P7_4/PWM_M_6/PWM_16_N/TC_M_6_TR0/TC_16_TR1/SCB5_SEL1/ADC[0]_12 33 << P7_4_ADC {10}

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P7_5/PWM_17/PWM_M_6_N/TC_17_TR0/TC_M_6_TR1/SCB5_SEL2/ADC[0]_13	34	⟨⟨P7_5_ADC {10}
P8_0/PWM_19/PWM_18_N/TC_19_TR0/TC_18_TR1/LIN2_RX/CAN0_0_TX	35	⟨⟨P8_0_LIN2_RX {10}
P8_1/PWM_20/PWM_19_N/TC_20_TR0/TC_19_TR1/LIN2_TX/CAN0_0_RX/TRIG_IN[14]/ADC[0]_16	36	⟨⟨P8_1_LIN2_TX {10}
P8_2/PWM_21/PWM_20_N/TC_21_TR0/TC_20_TR1/LIN2_EN/TRIG_IN[15]/ADC[0]_17	37	⟨⟨P8_2 {10}
P11_0/ADC[0]_M	38	⟨⟨P11_0 {10}
P11_1/ADC[1]_M	39	⟨⟨P11_1 {10}
P11_2/ADC[2]_M	40	⟨⟨P11_2 {10}
P12_0/PWM_36/PWM_35_N/TC_36_TR0/TC_35_TR1/CAN0_2_TX/TRIG_IN[20]/ADC[1]_4	45	⟨⟨P12_0_CAN0_2_TX {10}
P12_1/PWM_37/PWM_36_N/TC_37_TR0/TC_36_TR1/LIN6_EN/CAN0_2_RX/TRIG_IN[21]/ADC[1]_5	46	⟨⟨P12_1_CAN0_2_RX {10}
P12_2/PWM_38/PWM_37_N/TC_38_TR0/TC_37_TR1/EXT_MUX[1]_EN/LIN6_RX/ADC[1]_6	47	⟨⟨P12_2 {10,11}
P12_3/PWM_39/PWM_38_N/TC_39_TR0/TC_38_TR1/EXT_MUX[1]_0/LIN6_TX/ADC[1]_7	48	⟨⟨P12_3 {10}
P12_4/PWM_40/PWM_39_N/TC_40_TR0/TC_39_TR1/EXT_MUX[1]_1/ADC[1]_8	49	⟨⟨P12_4 {10}
P13_0/PWM_M_8/PWM_43_N/TC_M_8_TR0/TC_43_TR1/EXT_MUX[2]_0/SCB3_RX/SCB3_MISO/ADC[1]_12	52	⟨⟨P13_0_SCB3_RX {10}
P13_1/PWM_44/PWM_M_8_N/TC_44_TR0/TC_M_8_TR1/EXT_MUX[2]_1/SCB3_TX/SCB3_SDA/SCB3_MOSI/ADC[1]_13	53	⟨⟨P13_1_SCB3_TX {10}
P13_2/PWM_M_9/PWM_44_N/TC_M_9_TR0/TC_44_TR1/EXT_MUX[2]_2/SCB3_RTS/SCB3_SCL/SCB3_CLK/ADC[1]_14	54	⟨⟨P13_2_ADC {10}
P13_3/PWM_45/PWM_M_9_N/TC_45_TR0/TC_M_9_TR1/EXT_MUX[2]_EN/SCB3_CTS/SCB3_SEL0/ADC[1]_15	55	⟨⟨P13_3 {10}
P13_4/PWM_M_10/PWM_45_N/TC_M_10_TR0/TC_45_TR1/SCB3_SEL1/ADC[1]_16	56	⟨⟨P13_4 {10}
P13_5/PWM_46/PWM_M_10_N/TC_46_TR0/TC_M_10_TR1/SCB3_SEL2/ADC[1]_17	57	⟨⟨P13_5 {10}

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P13_6/PWM_M_11/PWM_46_N/TC_M_11_TR0/TC_46_TR1/SCB3_SEL3/TRIG_IN[22]/ADC[1]_18 58 << P13_6 {10}

P13_7/PWM_47/PWM_M_11_N/TC_47_TR0/TC_M_11_TR1/TRIG_IN[23]/ADC[1]_19 59 << P13_7 {10}

P14_0/PWM_48/PWM_47_N/TC_48_TR0/TC_47_TR1/SCB2_RX/SCB2_MISO/CAN1_0_TX/ADC[1]_20 60 << P14_0_SCB2_RX {10}

P14_1/PWM_49/PWM_48_N/TC_49_TR0/TC_48_TR1/SCB2_TX/SCB2_SDA/SCB2_MOSI/CAN1_0_RX/ADC[1]_21 61 << P14_1_SCB2_TX {10}

P14_2/PWM_50/PWM_49_N/TC_50_TR0/TC_49_TR1/SCB2_RTS/SCB2_SCL/SCB2_CLK/LIN6_RX/ADC[1]_22 62 << P14_2_LIN6_RX {10}

P14_3/PWM_51/PWM_50_N/TC_51_TR0/TC_50_TR1/SCB2_CTS/SCB2_SEL0/LIN6_TX/ADC[1]_23 63 << P14_3_LIN6_TX {10}

P17_0/PWM_61/PWM_62_N/TC_61_TR0/TC_62_TR1/CAN1_1_TX 64 << P17_0 {10}

P17_1/PWM_60/PWM_61_N/TC_60_TR0/TC_61_TR1/PWM_H_2/SCB3_RX/SCB3_MISO/CAN1_1_RX 65 << P17_1_SCB3_RX {10}

P17_2/PWM_59/PWM_60_N/TC_59_TR0/TC_60_TR1/PWM_H_2_N/SCB3_TX/SCB3_SDA/SCB3_MOSI 66 << P17_2_SCB3_TX {10}

P18_0/PWM_M_6/PWM_M_5_N/TC_M_6_TR0/TC_M_5_TR1/PWM_H_0/SCB1_RX/SCB1_MISO/FAULT_OUT_0/ADC[2]_0 67 << P18_0_SCB1_RX {10}

P18_1/PWM_M_7/PWM_M_6_N/TC_M_7_TR0/TC_M_6_TR1/PWM_H_0_N/SCB1_TX/SCB1_SDA/SCB1_MOSI/FAULT_OUT_1/ADC[2]_1 68 << P18_1_SCB1_TX {10}

P18_2/PWM_55/PWM_M_7_N/TC_55_TR0/TC_M_7_TR1/PWM_H_1/SCB1_RTS/SCB1_SCL/SCB1_CLK/ADC[2]_2 69 << P18_2 {10}

P18_3/PWM_54/PWM_55_N/TC_54_TR0/TC_55_TR1/PWM_H_1_N/SCB1_CTS/SCB1_SEL0/TRACE_CLOCK/ADC[2]_3 70 << P18_3 {4,10}

P18_4/PWM_53/PWM_54_N/TC_53_TR0/TC_54_TR1/PWM_H_2/SCB1_SEL1/TRACE_DATA_0/ADC[2]_4 71 << P18_4 {4,10}


P18_5/PWM_52/PWM_53_N/TC_52_TR0/TC_53_TR1/PWM_H_2_N/SCB1_SEL2/TRACE_DATA_1/ADC[2]_5 72 << P18_5 {4,10}

P18_6/PWM_51/PWM_52_N/TC_51_TR0/TC_52_TR1/PWM_H_3/SCB1_SEL3/CAN1_2_TX/TRACE_DATA_2/ADC[2]_6 73 << P18_6_ADC {4,10}

P18_7/PWM_50/PWM_51_N/TC_50_TR0/TC_51_TR1/PWM_H_3_N/CAN1_2_RX/TRACE_DATA_3/ADC[2]_7 74 << P18_7_ADC {4,10}

P19_0/PWM_M_3/PWM_50_N/TC_M_3_TR0/TC_50_TR1/TC_H_0_TR0/SCB2_RX/SCB2_MISO/FAULT_OUT_2 77 << P19_0 {4,10}

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P19_1/PWM_26/PWM_M_3_N/TC_26_TR0/TC_M_3_TR1/TC_H_0_TR1/SCB2_TX/SCB2_SDA/SCB2_MOSI/FAULT_OUT_3
P19_2/PWM_27/PWM_26_N/TC_27_TR0/TC_26_TR1/TC_H_1_TR0/SCB2_RTS/SCB2_SCL/SCB2_CLK/TRIG_IN[28]
P19_3/PWM_28/PWM_27_N/TC_28_TR0/TC_27_TR1/TC_H_1_TR1/SCB2_CTS/SCB2_SEL0/TRIG_IN[29]
P21_0/PWM_42/PWM_43_N/TC_42_TR0/TC_43_TR1/SCB1_SEL2/WCO_IN
P21_1/PWM_41/PWM_42_N/TC_41_TR0/TC_42_TR1/WCO_OUT
P21_2/PWM_40/PWM_41_N/TC_40_TR0/TC_41_TR1/TRIG_DBG[1]/EXT_CLK/ECO_IN
P21_3/PWM_39/PWM_40_N/TC_39_TR0/TC_40_TR1/ECO_OUT
XRES
P21_5/PWM_37/PWM_38_N/TC_37_TR0/TC_38_TR1/LIN0_RX
P22_0/PWM_34/PWM_35_N/TC_34_TR0/TC_35_TR1/SCB6_RX/SCB6_MISO/CAN1_1_TX/TRACE_DATA_0
P22_1/PWM_33/PWM_34_N/TC_33_TR0/TC_34_TR1/SCB6_TX/SCB6_SDA/SCB6_MOSI/CAN1_1_RX/TRACE_DATA_1
P22_2/PWM_32/PWM_33_N/TC_32_TR0/TC_33_TR1/SCB6_RTS/SCB6_SCL/SCB6_CLK/TRACE_DATA_2
P22_3/PWM_31/PWM_32_N/TC_31_TR0/TC_32_TR1/SCB6_CTS/SCB6_SEL0/TRACE_DATA_3
P23_3/PWM_M_11/PWM_M_10_N/TC_M_11_TR0/TC_M_10_TR1/SCB7_CTS/SCB7_SEL0/FAULT_OUT_3/TRIG_IN[30]
P23_4/PWM_25/PWM_M_11_N/TC_25_TR0/TC_M_11_TR1/SCB7_SEL1/TRIG_DBG[0]/SWJ_SWO_TDO/TRIG_IN[31]
P23_5/PWM_24/PWM_25_N/TC_24_TR0/TC_25_TR1/SCB7_SEL2/SWJ_SWCLK_TCLK
P23_6/PWM_23/PWM_24_N/TC_23_TR0/TC_24_TR1/SWJ_SWDIO_TMS
P23_7/PWM_22/PWM_23_N/TC_22_TR0/TC_23_TR1/CAL_SUP_NZ/SWJ_SWDOE_TDI/EXT_CLK/HIBERNATE_WAKEUP[1]

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78 << P19_1_CXPI3_RX {10}
79 << P19_2_CXPI3_TX {10}
80 << P19_3_CXPI3_EN {10}
81 << P21_0 {10}
82 << P21_1 {10}
83 << P21_2 {4}
84 << P21_3 {4}
85 << XRES {3,4}
90 << P21_5 {10}
91 << P22_0_SCB6_MISO {10}
92 << P22_1_SCB6_MOSI {10}
93 << P22_2_SCB6_SCL {10}
94 << P22_3_SCB6_SEL0 {10}
95 << P23_3 {10}
96 << P23_4 {4}
97 << P23_5 {4}
98 << P23_6 {4}
99 << P23_7 {4}



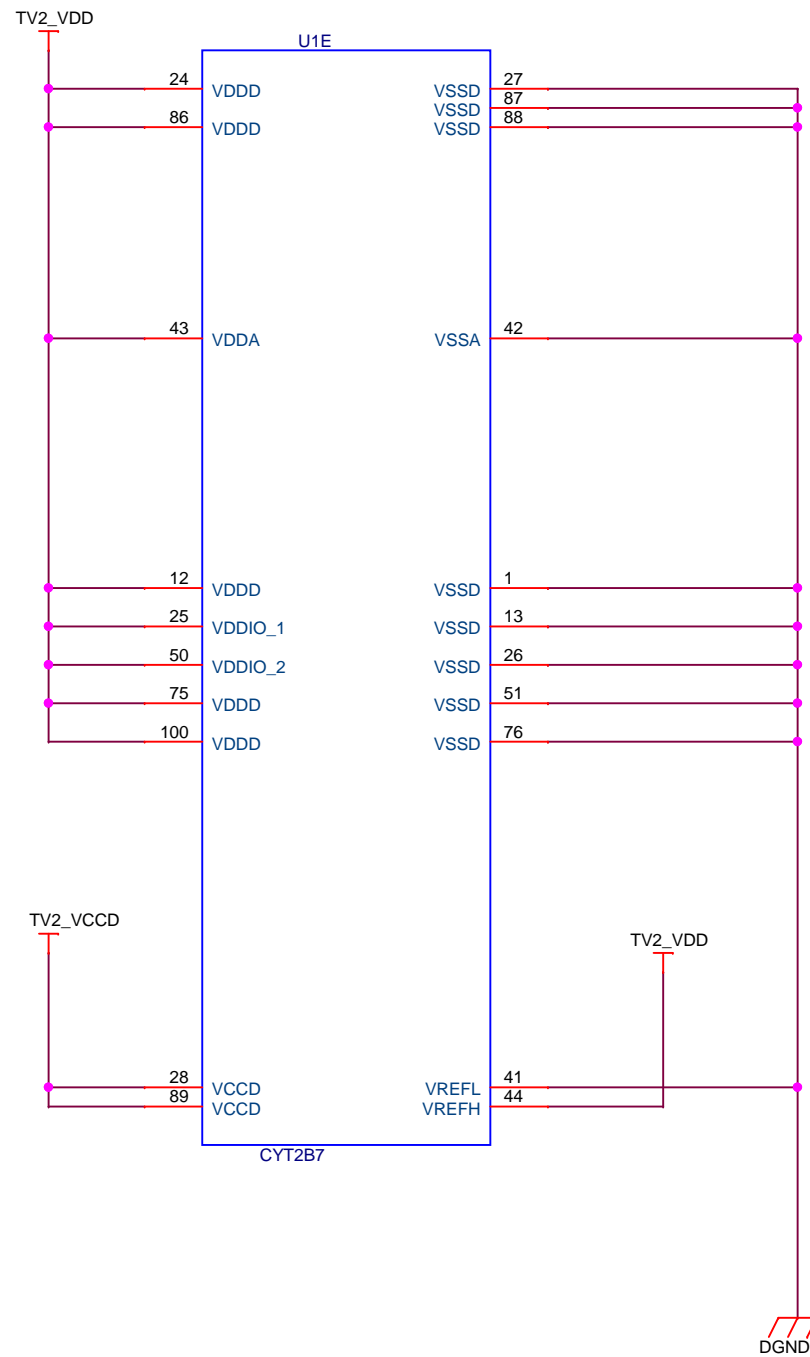
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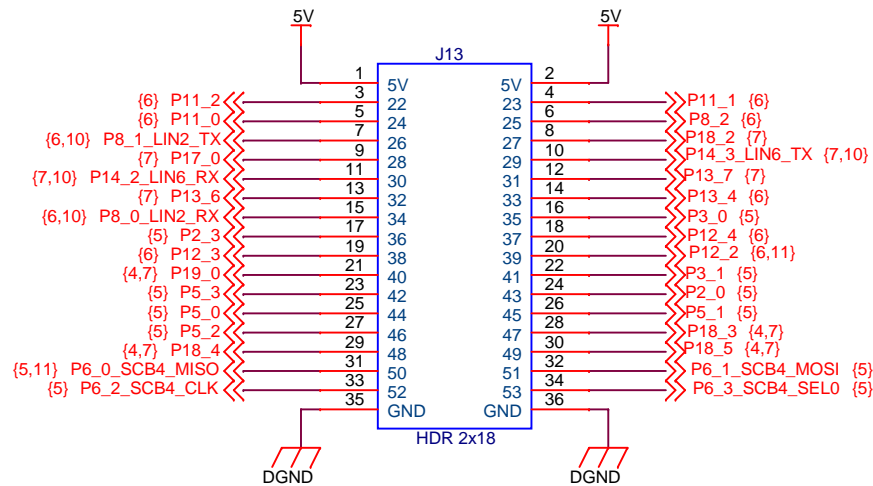
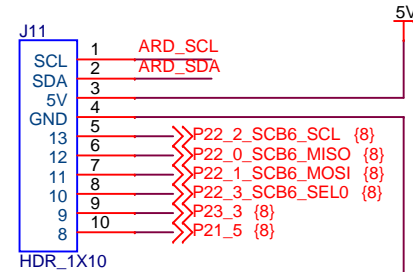
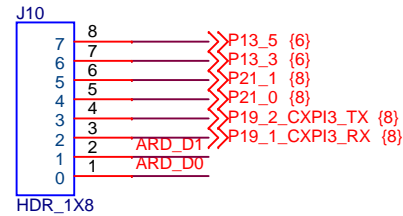
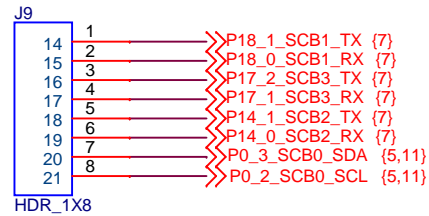
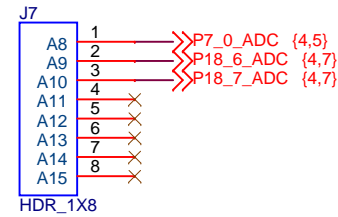
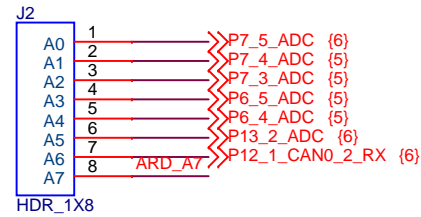
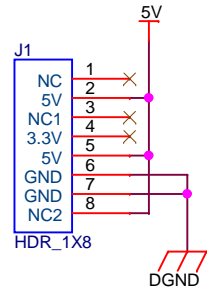
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Target Device





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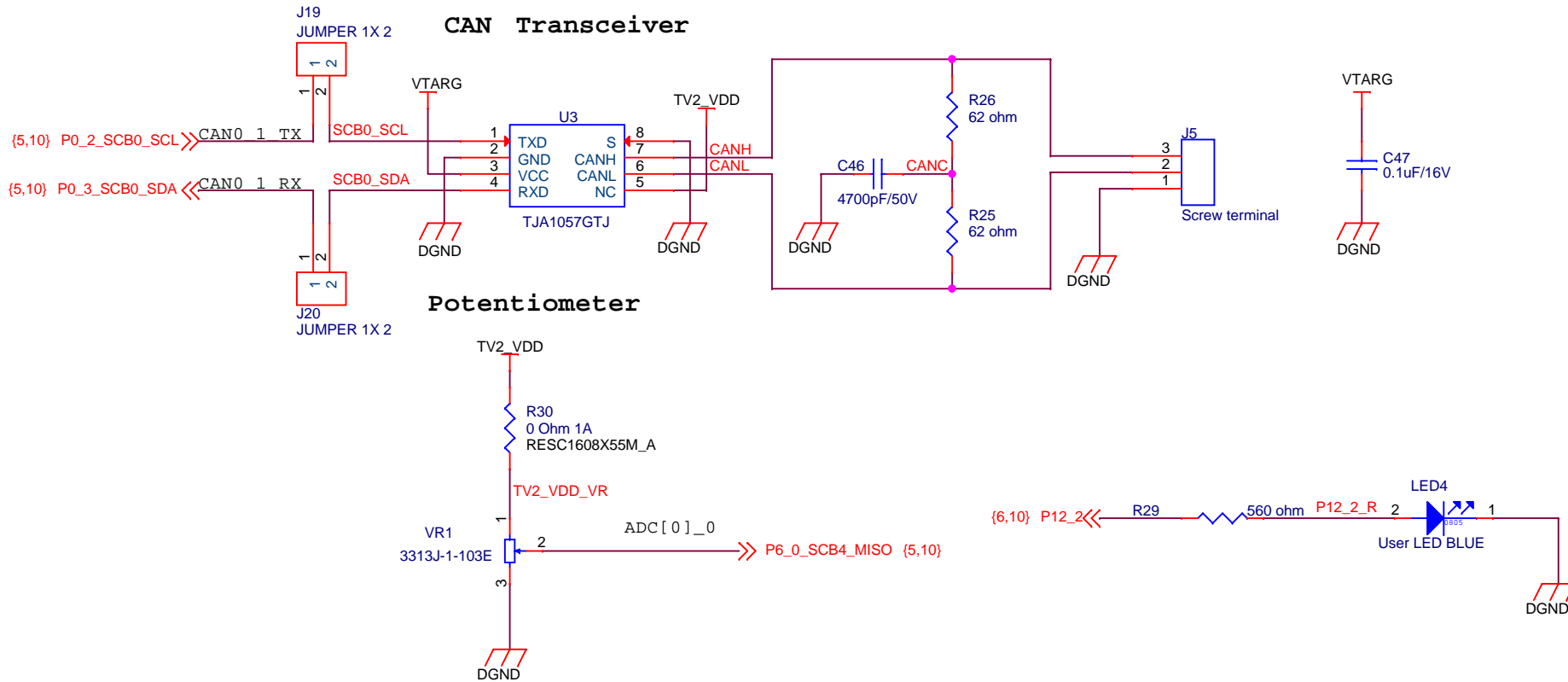
Page Title :Arduino compatible pin-headers

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CANFD, Potentiometer



REVISION HISTORY

Rev	DESCRIPTION	DATE
1.0	TVII-B-E-1M 100-pin Starter kit first version	
2.0	Modified the pin-headers for Arduino compatibility	06/06/2019
3.0	Added User LED and Jumpers for CAN Transceiver	22/11/2019



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Page Title :Revision History

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