TRAVEO(TM) T2G Automotive MCU: TVII-C-2D-4M cluster 2D registers technical reference manual: Differences between Rev 0E and Rev 0F

1 Important Notes

- Section "New Registers Added", lists newly added registers in the latest revision.

- Section "Registers Removed", lists the registers removed in the latest revision.

- Section "Fields of Register or Bitfield changed", details the register contents modified.

Top row indicates "Register: Bit-Field" targeted, and the bottom row indicates which field of the register or its bit-field is altered in the new revision. If the Bit-Field is not mentioned, then it is the bit-field name itself which is altered between revisions.

2 New Registers Added: Revision 0F

2.1 No register is added into the new revision

3 Registers Removed: Revision 0F

CLK_TIMER_CTL

4 Fields of Register or Bitfield changed: Revision 0F

PWR_LVD_STATUS: PWR_LVD_STATUS		
Field	**Rev 0E**	**Rev 0F**
Retention	Retained	Not Retained

PWR_LVD_STATUS2: PWR_LVD_STATUS2		
Field	**Rev 0E**	**Rev 0F**
Retention	Retained	Not Retained

CLK_CAL_CNT1: CLK_CAL_CNT1		
Field	**Rev 0E**	**Rev 0F**
Retention	Retained	Not Retained

CLK_CAL_CNT2: CLK_CAL_CNT2		
Field	**Rev 0E**	**Rev 0F**
Retention	Retained	Not Retained

PWR_CTL2: BGREF_LPMODE		
Field	**Rev 0E**	**Rev 0F**
F1Comment	Control the circuit-level power mode of the Bandgap Reference circuits. 0: Bandgap Reference circuits operate in higher current mode. 1: Bandgap Reference circuits operate in low power. Refer to documentation for restrictions.	Control the circuit-level power mode of the Bandgap Reference circuits. 0: Bandgap Reference circuits operate in higher current mode. 1: Bandgap Reference circuits operate in low power. Refer to documentation for restrictions. HT-variant: This register will not set unless CLK_ILO0_CONFIG.ILO0_ENABLE==1. When disabling low power operation, keep ILO0 enabled for at least 5 cycles after clearing this bit to allow for internal synchronization.

CLK_FLL_STATUS: CLK_FLL_STATUS		
Field	**Rev 0E**	**Rev 0F**
Retention	Retained	Not Retained

CLK_PLL400M0_STATUS: CLK_PLL400M0_STATUS		
Field	**Rev 0E**	**Rev 0F**
Retention	Retained	Not Retained

CLK_PLL400M1_STATUS: CLK_PLL400M1_STATUS		
Field	**Rev 0E**	**Rev 0F**
Retention	Retained	Not Retained

CLK_PLL400M2_STATUS: CLK_PLL400M2_STATUS		
Field	**Rev 0E**	**Rev 0F**
Retention	Retained	Not Retained

CLK_PLL400M3_STATUS: CLK_PLL400M3_STATUS		
Field	**Rev 0E**	**Rev 0F**
Retention	Retained	Not Retained

CLK_PLL400M4_STATUS: CLK_PLL400M4_STATUS		
Field	**Rev 0E**	**Rev 0F**
Retention	Retained	Not Retained

MCWDT0_CTR2_CNT: CNT2		
Field	**Rev 0E**	**Rev 0F**
F0Comment	Current value of subcounter 2 for this MCWDT. This field may lag the actual count value by up to one clk_lf cycle, due to internal synchronization. When this subcounter is disabled and unlocked, the count value can be written for verification and debugging purposes. Software writes are always ignored when the subcounter is enabled.	Current value of subcounter 2 for this MCWDT. This field may lag the actual count value by up to one clk_lf cycle, due to internal synchronization. When this subcounter is disabled and unlocked, the count value can be written for verification and debugging purposes. Software writes are always ignored when the subcounter is enabled. This register retains information during DeepSleep mode if SLEEPDEEP_PAUSE == 1.

MCWDT0_CTR0_CNT: CNT		
Field	**Rev 0E**	**Rev 0F**
F0Comment	Current value of subcounter for this MCWDT. This field may lag the actual count value by up to one clk_lf cycle, due to internal synchronization. When this subcounter is disabled and unlocked, the count value can be written for verification and debugging purposes. Software writes are always ignored when the subcounter is enabled.	Current value of subcounter for this MCWDT. This field may lag the actual count value by up to one clk_lf cycle, due to internal synchronization. When this subcounter is disabled and unlocked, the count value can be written for verification and debugging purposes. Software writes are always ignored when the subcounter is enabled.This register retains information during DeepSleep mode if SLEEPDEEP_PAUSE == 1.

MCWDT0_CTR1_CNT: CNT		
Field	**Rev 0E**	**Rev 0F**
F0Comment	Current value of subcounter for this MCWDT. This field may lag the actual count value by up to one clk_lf cycle, due to internal synchronization. When this subcounter is disabled and unlocked, the count value can be written for verification and debugging purposes. Software writes are always ignored when the subcounter is enabled.	Current value of subcounter for this MCWDT. This field may lag the actual count value by up to one clk_lf cycle, due to internal synchronization. When this subcounter is disabled and unlocked, the count value can be written for verification and debugging purposes. Software writes are always ignored when the subcounter is enabled.This register retains information during DeepSleep mode if SLEEPDEEP_PAUSE == 1.

MCWDT1_CTR2_CNT: CNT2		
Field	**Rev 0E**	**Rev 0F**
F0Comment	Current value of subcounter 2 for this MCWDT. This field may lag the actual count value by up to one clk_lf cycle, due to internal synchronization. When this subcounter is disabled and unlocked, the count value can be written for verification and debugging purposes. Software writes are always ignored when the subcounter is enabled.	Current value of subcounter 2 for this MCWDT. This field may lag the actual count value by up to one clk_lf cycle, due to internal synchronization. When this subcounter is disabled and unlocked, the count value can be written for verification and debugging purposes. Software writes are always ignored when the subcounter is enabled. This register retains information during DeepSleep mode if SLEEPDEEP_PAUSE == 1.

MCWDT1_CTR0_CNT: CNT		
Field	**Rev 0E**	**Rev 0F**
F0Comment	Current value of subcounter for this MCWDT. This field may lag the actual count value by up to one clk_lf cycle, due to internal synchronization. When this subcounter is disabled and unlocked, the count value can be written for verification and debugging purposes. Software writes are always ignored when the subcounter is enabled.	Current value of subcounter for this MCWDT. This field may lag the actual count value by up to one clk_lf cycle, due to internal synchronization. When this subcounter is disabled and unlocked, the count value can be written for verification and debugging purposes. Software writes are always ignored when the subcounter is enabled.This register retains information during DeepSleep mode if SLEEPDEEP_PAUSE == 1.

MCWDT1_CTR1_CNT: CNT		
Field	**Rev 0E**	**Rev 0F**
F0Comment	Current value of subcounter for this MCWDT. This field may lag the actual count value by up to one clk_lf cycle, due to internal synchronization. When this subcounter is disabled and unlocked, the count value can be written for verification and debugging purposes. Software writes are always ignored when the subcounter is enabled.	Current value of subcounter for this MCWDT. This field may lag the actual count value by up to one clk_lf cycle, due to internal synchronization. When this subcounter is disabled and unlocked, the count value can be written for verification and debugging purposes. Software writes are always ignored when the subcounter is enabled.This register retains information during DeepSleep mode if SLEEPDEEP_PAUSE == 1.

WDT_CNT: CNT		
Field	**Rev 0E**	**Rev 0F**
F0Comment	Current value of subcounter for this WDT. This field may lag the actual count value by up to one clk_ilo0 cycle, due to internal synchronization. When this subcounter is disabled and unlocked, the count value can be written for verification and debugging purposes. Software writes are always ignored when the subcounter is enabled.	Current value of subcounter for this WDT. This field may lag the actual count value by up to one clk_ilo0 cycle, due to internal synchronization. When this subcounter is disabled and unlocked, the count value can be written for verification and debugging purposes. Software writes are always ignored when the subcounter is enabled. This register retains information during DeepSleep or Hiberbate mode if DPSLP_PAUSE == 1 or HIB_PAUSE == 1.

WDT_INTR: WDT_INTR		
Field	**Rev 0E**	**Rev 0F**
Retention	Retained	Not Retained

WDT_INTR_MASKED: WDT_INTR_MASKED		
Field	**Rev 0E**	**Rev 0F**
Retention	Retained	Not Retained

GPIO_PRT11_CFG_SLEW_EXT: SLEW0		
Field	**Rev 0E**	**Rev 0F**
F7Comment	Enables slow slew rate for IO pin 0 HSIO_STDLIN: slew_ctl[SLEW_WIDTH] = All 0s: Fastest slew rate slew_ctl[SLEW_WIDTH] = All 1s: Slowest slew rate HSIO_ENH: slew_sel[SLEW_WIDTH] = All 0s: Fastest slew rate slew_sel[SLEW_WIDTH] = All 1s: Slowest slew rate	Enables slow slew rate for IO pin 0 HSIO_STDLN: slew_ctl[SLEW_WIDTH] = All 0s: Fastest slew rate slew_ctl[SLEW_WIDTH] = All 1s: Slowest slew rate HSIO_ENH: slew_sel[SLEW_WIDTH] = All 0s: Fastest slew rate slew_sel[SLEW_WIDTH] = All 1s: Slowest slew rate

GPIO_PRT12_CFG_SLEW_EXT: SLEW0		
Field	**Rev 0E**	**Rev 0F**
F7Comment	Enables slow slew rate for IO pin 0 HSIO_STDLIN: slew_ctl[SLEW_WIDTH] = All 0s: Fastest slew rate slew_ctl[SLEW_WIDTH] = All 1s: Slowest slew rate HSIO_ENH: slew_sel[SLEW_WIDTH] = All 0s: Fastest slew rate slew_sel[SLEW_WIDTH] = All 1s: Slowest slew rate	Enables slow slew rate for IO pin 0 HSIO_STDLN: slew_ctl[SLEW_WIDTH] = All 0s: Fastest slew rate slew_ctl[SLEW_WIDTH] = All 1s: Slowest slew rate HSIO_ENH: slew_sel[SLEW_WIDTH] = All 0s: Fastest slew rate slew_sel[SLEW_WIDTH] = All 1s: Slowest slew rate

GPIO_PRT13_CFG_SLEW_EXT: SLEW0		
Field	**Rev 0E**	**Rev 0F**
F7Comment	Enables slow slew rate for IO pin 0 HSIO_STDLIN: slew_ctl[SLEW_WIDTH] = All 0s: Fastest slew rate slew_ctl[SLEW_WIDTH] = All 1s: Slowest slew rate HSIO_ENH: slew_sel[SLEW_WIDTH] = All 0s: Fastest slew rate slew_sel[SLEW_WIDTH] = All 1s: Slowest slew rate	Enables slow slew rate for IO pin 0 HSIO_STDLN: slew_ctl[SLEW_WIDTH] = All 0s: Fastest slew rate slew_ctl[SLEW_WIDTH] = All 1s: Slowest slew rate HSIO_ENH: slew_sel[SLEW_WIDTH] = All 0s: Fastest slew rate slew_sel[SLEW_WIDTH] = All 1s: Slowest slew rate

GPIO_PRT14_CFG_SLEW_EXT: SLEW0		
Field	**Rev 0E**	**Rev 0F**
F7Comment	Enables slow slew rate for IO pin 0 HSIO_STDLIN: slew_ctl[SLEW_WIDTH] = All 0s: Fastest slew rate slew_ctl[SLEW_WIDTH] = All 1s: Slowest slew rate HSIO_ENH: slew_sel[SLEW_WIDTH] = All 0s: Fastest slew rate slew_sel[SLEW_WIDTH] = All 1s: Slowest slew rate	Enables slow slew rate for IO pin 0 HSIO_STDLN: slew_ctl[SLEW_WIDTH] = All 0s: Fastest slew rate slew_ctl[SLEW_WIDTH] = All 1s: Slowest slew rate HSIO_ENH: slew_sel[SLEW_WIDTH] = All 0s: Fastest slew rate slew_sel[SLEW_WIDTH] = All 1s: Slowest slew rate

GPIO_PRT15_CFG_SLEW_EXT: SLEW0		
Field	**Rev 0E**	**Rev 0F**
F7Comment	Enables slow slew rate for IO pin 0 HSIO_STDLIN: slew_ctl[SLEW_WIDTH] = All 0s: Fastest slew rate slew_ctl[SLEW_WIDTH] = All 1s: Slowest slew rate HSIO_ENH: slew_sel[SLEW_WIDTH] = All 0s: Fastest slew rate slew_sel[SLEW_WIDTH] = All 1s: Slowest slew rate	Enables slow slew rate for IO pin 0 HSIO_STDLN: slew_ctl[SLEW_WIDTH] = All 0s: Fastest slew rate slew_ctl[SLEW_WIDTH] = All 1s: Slowest slew rate HSIO_ENH: slew_sel[SLEW_WIDTH] = All 0s: Fastest slew rate slew_sel[SLEW_WIDTH] = All 1s: Slowest slew rate

GPIO_PRT16_CFG_SLEW_EXT: SLEW0		
Field	**Rev 0E**	**Rev 0F**
F7Comment	Enables slow slew rate for IO pin 0 HSIO_STDLIN: slew_ctl[SLEW_WIDTH] = All 0s: Fastest slew rate slew_ctl[SLEW_WIDTH] = All 1s: Slowest slew rate HSIO_ENH: slew_sel[SLEW_WIDTH] = All 0s: Fastest slew rate slew_sel[SLEW_WIDTH] = All 1s: Slowest slew rate	Enables slow slew rate for IO pin 0 HSIO_STDLN: slew_ctl[SLEW_WIDTH] = All 0s: Fastest slew rate slew_ctl[SLEW_WIDTH] = All 1s: Slowest slew rate HSIO_ENH: slew_sel[SLEW_WIDTH] = All 0s: Fastest slew rate slew_sel[SLEW_WIDTH] = All 1s: Slowest slew rate

GPIO_PRT17_CFG_SLEW_EXT: SLEW0		
Field	**Rev 0E**	**Rev 0F**
F7Comment	Enables slow slew rate for IO pin 0 HSIO_STDLIN: slew_ctl[SLEW_WIDTH] = All 0s: Fastest slew rate slew_ctl[SLEW_WIDTH] = All 1s: Slowest slew rate HSIO_ENH: slew_sel[SLEW_WIDTH] = All 0s: Fastest slew rate slew_sel[SLEW_WIDTH] = All 1s: Slowest slew rate	Enables slow slew rate for IO pin 0 HSIO_STDLN: slew_ctl[SLEW_WIDTH] = All 0s: Fastest slew rate slew_ctl[SLEW_WIDTH] = All 1s: Slowest slew rate HSIO_ENH: slew_sel[SLEW_WIDTH] = All 0s: Fastest slew rate slew_sel[SLEW_WIDTH] = All 1s: Slowest slew rate

GPIO_PRT18_CFG_SLEW_EXT: SLEW0		
Field	**Rev 0E**	**Rev 0F**
F7Comment	Enables slow slew rate for IO pin 0 HSIO_STDLIN: slew_ctl[SLEW_WIDTH] = All 0s: Fastest slew rate slew_ctl[SLEW_WIDTH] = All 1s: Slowest slew rate HSIO_ENH: slew_sel[SLEW_WIDTH] = All 0s: Fastest slew rate slew_sel[SLEW_WIDTH] = All 1s: Slowest slew rate	Enables slow slew rate for IO pin 0 HSIO_STDLN: slew_ctl[SLEW_WIDTH] = All 0s: Fastest slew rate slew_ctl[SLEW_WIDTH] = All 1s: Slowest slew rate HSIO_ENH: slew_sel[SLEW_WIDTH] = All 0s: Fastest slew rate slew_sel[SLEW_WIDTH] = All 1s: Slowest slew rate

GPIO_PRT19_CFG_SLEW_EXT: SLEW0		
Field	**Rev 0E**	**Rev 0F**
F7Comment	Enables slow slew rate for IO pin 0 HSIO_STDLIN: slew_ctl[SLEW_WIDTH] = All 0s: Fastest slew rate slew_ctl[SLEW_WIDTH] = All 1s: Slowest slew rate HSIO_ENH: slew_sel[SLEW_WIDTH] = All 0s: Fastest slew rate slew_sel[SLEW_WIDTH] = All 1s: Slowest slew rate	Enables slow slew rate for IO pin 0 HSIO_STDLN: slew_ctl[SLEW_WIDTH] = All 0s: Fastest slew rate slew_ctl[SLEW_WIDTH] = All 1s: Slowest slew rate HSIO_ENH: slew_sel[SLEW_WIDTH] = All 0s: Fastest slew rate slew_sel[SLEW_WIDTH] = All 1s: Slowest slew rate

GPIO_PRT20_CFG_SLEW_EXT: SLEW0		
Field	**Rev 0E**	**Rev 0F**
F7Comment	Enables slow slew rate for IO pin 0 HSIO_STDLIN: slew_ctl[SLEW_WIDTH] = All 0s: Fastest slew rate slew_ctl[SLEW_WIDTH] = All 1s: Slowest slew rate HSIO_ENH: slew_sel[SLEW_WIDTH] = All 0s: Fastest slew rate slew_sel[SLEW_WIDTH] = All 1s: Slowest slew rate	Enables slow slew rate for IO pin 0 HSIO_STDLN: slew_ctl[SLEW_WIDTH] = All 0s: Fastest slew rate slew_ctl[SLEW_WIDTH] = All 1s: Slowest slew rate HSIO_ENH: slew_sel[SLEW_WIDTH] = All 0s: Fastest slew rate slew_sel[SLEW_WIDTH] = All 1s: Slowest slew rate

GPIO_PRT21_CFG_SLEW_EXT: SLEW0		
Field	**Rev 0E**	**Rev 0F**
F7Comment	Enables slow slew rate for IO pin 0 HSIO_STDLIN: slew_ctl[SLEW_WIDTH] = All 0s: Fastest slew rate slew_ctl[SLEW_WIDTH] = All 1s: Slowest slew rate HSIO_ENH: slew_sel[SLEW_WIDTH] = All 0s: Fastest slew rate slew_sel[SLEW_WIDTH] = All 1s: Slowest slew rate	Enables slow slew rate for IO pin 0 HSIO_STDLN: slew_ctl[SLEW_WIDTH] = All 0s: Fastest slew rate slew_ctl[SLEW_WIDTH] = All 1s: Slowest slew rate HSIO_ENH: slew_sel[SLEW_WIDTH] = All 0s: Fastest slew rate slew_sel[SLEW_WIDTH] = All 1s: Slowest slew rate

TCPWM0_GRP0_CNT0_CTRL: ENABLED		
Field	**Rev 0E**	**Rev 0F**
F0Comment	Counter Enable '0': counter disabled. '1': counter enabled. Counter static configuration register fields should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out"). The following are Counter static configuration registers: CTRL (with the exception of DEBUG_FREEZE_EN bit), DT, TR_IN_SEL0, TR_IN_SEL1, TR_IN_EDGE_SEL, TR_PWM_CTRL_TR_OUT_SEL,INTR, INTR_MASK, INTR_MASKED Modifying these registers while the counter is running could produce unexcepted waveform results, but will not cause a fatal issue such as an illegal stop, lost control, or waveform stability issues.	Counter enable. '0': counter disabled. '1': counter enabled. Counter static configuration information (e.g. CTRL.MODE, all TR_IN_SEL, TR_IN_EDGE_SEL, TR_PWM_CTRL and TR_OUT_SEL register fields) should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out").

TCPWM0_GRP0_CNT0_CTRL: AUTO_RELOAD_PERIOD		
Field	**Rev 0E**	**Rev 0F**
F10Comment	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with an actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with and actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.

TCPWM0_GRP0_CNT1_CTRL: ENABLED		
Field	**Rev 0E**	**Rev 0F**
F0Comment	Counter Enable '0': counter disabled. '1': counter enabled. Counter static configuration register fields should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out"). The following are Counter static configuration registers: CTRL (with the exception of DEBUG_FREEZE_EN bit), DT, TR_IN_SEL0, TR_IN_SEL1, TR_IN_EDGE_SEL, TR_PWM_CTRL_TR_OUT_SEL,INTR, INTR_MASK, INTR_MASKED Modifying these registers while the counter is running could produce unexcepted waveform results, but will not cause a fatal issue such as an illegal stop, lost control, or waveform stability issues.	Counter enable. '0': counter disabled. '1': counter enabled. Counter static configuration information (e.g. CTRL.MODE, all TR_IN_SEL, TR_IN_EDGE_SEL, TR_PWM_CTRL and TR_OUT_SEL register fields) should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out").

TCPWM0_GRP0_CNT1_CTRL: AUTO_RELOAD_PERIOD		
Field	**Rev 0E**	**Rev 0F**
F10Comment	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with an actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with and actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.

TCPWM0_GRP0_CNT2_CTRL: ENABLED		
Field	**Rev 0E**	**Rev 0F**
F0Comment	Counter Enable '0': counter disabled. '1': counter enabled. Counter static configuration register fields should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out"). The following are Counter static configuration registers: CTRL (with the exception of DEBUG_FREEZE_EN bit), DT, TR_IN_SEL0, TR_IN_SEL1, TR_IN_EDGE_SEL, TR_PWM_CTRL_TR_OUT_SEL,INTR, INTR_MASK, INTR_MASKED Modifying these registers while the counter is running could produce unexcepted waveform results, but will not cause a fatal issue such as an illegal stop, lost control, or waveform stability issues.	Counter enable. '0': counter disabled. '1': counter enabled. Counter static configuration information (e.g. CTRL.MODE, all TR_IN_SEL, TR_IN_EDGE_SEL, TR_PWM_CTRL and TR_OUT_SEL register fields) should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out").

TCPWM0_GRP0_CNT2_CTRL: AUTO_RELOAD_PERIOD		
Field	**Rev 0E**	**Rev 0F**
F10Comment	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with an actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with and actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.

TCPWM0_GRP0_CNT3_CTRL: ENABLED		
Field	**Rev 0E**	**Rev 0F**
F0Comment	Counter Enable '0': counter disabled. '1': counter enabled. Counter static configuration register fields should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out"). The following are Counter static configuration registers: CTRL (with the exception of DEBUG_FREEZE_EN bit), DT, TR_IN_SEL0, TR_IN_SEL1, TR_IN_EDGE_SEL, TR_PWM_CTRL_TR_OUT_SEL,INTR, INTR_MASK, INTR_MASKED Modifying these registers while the counter is running could produce unexcepted waveform results, but will not cause a fatal issue such as an illegal stop, lost control, or waveform stability issues.	Counter enable. '0': counter disabled. '1': counter enabled. Counter static configuration information (e.g. CTRL.MODE, all TR_IN_SEL, TR_IN_EDGE_SEL, TR_PWM_CTRL and TR_OUT_SEL register fields) should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out").

TCPWM0_GRP0_CNT3_CTRL: AUTO_RELOAD_PERIOD		
Field	**Rev 0E**	**Rev 0F**
F10Comment	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with an actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with and actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.

TCPWM0_GRP0_CNT4_CTRL: ENABLED		
Field	**Rev 0E**	**Rev 0F**
F0Comment	Counter Enable '0': counter disabled. '1': counter enabled. Counter static configuration register fields should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out"). The following are Counter static configuration registers: CTRL (with the exception of DEBUG_FREEZE_EN bit), DT, TR_IN_SEL0, TR_IN_SEL1, TR_IN_EDGE_SEL, TR_PWM_CTRL_TR_OUT_SEL,INTR, INTR_MASK, INTR_MASKED Modifying these registers while the counter is running could produce unexcepted waveform results, but will not cause a fatal issue such as an illegal stop, lost control, or waveform stability issues.	Counter enable. '0': counter disabled. '1': counter enabled. Counter static configuration information (e.g. CTRL.MODE, all TR_IN_SEL, TR_IN_EDGE_SEL, TR_PWM_CTRL and TR_OUT_SEL register fields) should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out").

TCPWM0_GRP0_CNT4_CTRL: AUTO_RELOAD_PERIOD		
Field	**Rev 0E**	**Rev 0F**
F10Comment	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with an actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with and actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.

TCPWM0_GRP0_CNT5_CTRL: ENABLED		
Field	**Rev 0E**	**Rev 0F**
F0Comment	Counter Enable '0': counter disabled. '1': counter enabled. Counter static configuration register fields should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out"). The following are Counter static configuration registers: CTRL (with the exception of DEBUG_FREEZE_EN bit), DT, TR_IN_SEL0, TR_IN_SEL1, TR_IN_EDGE_SEL, TR_PWM_CTRL_TR_OUT_SEL,INTR, INTR_MASK, INTR_MASKED Modifying these registers while the counter is running could produce unexcepted waveform results, but will not cause a fatal issue such as an illegal stop, lost control, or waveform stability issues.	Counter enable. '0': counter disabled. '1': counter enabled. Counter static configuration information (e.g. CTRL.MODE, all TR_IN_SEL, TR_IN_EDGE_SEL, TR_PWM_CTRL and TR_OUT_SEL register fields) should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out").

TCPWM0_GRP0_CNT5_CTRL: AUTO_RELOAD_PERIOD		
Field	**Rev 0E**	**Rev 0F**
F10Comment	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with an actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with and actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.

TCPWM0_GRP0_CNT6_CTRL: ENABLED		
Field	**Rev 0E**	**Rev 0F**
F0Comment	Counter Enable '0': counter disabled. '1': counter enabled. Counter static configuration register fields should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out"). The following are Counter static configuration registers: CTRL (with the exception of DEBUG_FREEZE_EN bit), DT, TR_IN_SEL0, TR_IN_SEL1, TR_IN_EDGE_SEL, TR_PWM_CTRL_TR_OUT_SEL,INTR, INTR_MASK, INTR_MASKED Modifying these registers while the counter is running could produce unexcepted waveform results, but will not cause a fatal issue such as an illegal stop, lost control, or waveform stability issues.	Counter enable. '0': counter disabled. '1': counter enabled. Counter static configuration information (e.g. CTRL.MODE, all TR_IN_SEL, TR_IN_EDGE_SEL, TR_PWM_CTRL and TR_OUT_SEL register fields) should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out").

TCPWM0_GRP0_CNT6_CTRL: AUTO_RELOAD_PERIOD		
Field	**Rev 0E**	**Rev 0F**
F10Comment	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with an actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with and actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.

TCPWM0_GRP0_CNT7_CTRL: ENABLED		
Field	**Rev 0E**	**Rev 0F**
F0Comment	Counter Enable '0': counter disabled. '1': counter enabled. Counter static configuration register fields should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out"). The following are Counter static configuration registers: CTRL (with the exception of DEBUG_FREEZE_EN bit), DT, TR_IN_SEL0, TR_IN_SEL1, TR_IN_EDGE_SEL, TR_PWM_CTRL_TR_OUT_SEL,INTR, INTR_MASK, INTR_MASKED Modifying these registers while the counter is running could produce unexcepted waveform results, but will not cause a fatal issue such as an illegal stop, lost control, or waveform stability issues.	Counter enable. '0': counter disabled. '1': counter enabled. Counter static configuration information (e.g. CTRL.MODE, all TR_IN_SEL, TR_IN_EDGE_SEL, TR_PWM_CTRL and TR_OUT_SEL register fields) should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out").

TCPWM0_GRP0_CNT7_CTRL: AUTO_RELOAD_PERIOD		
Field	**Rev 0E**	**Rev 0F**
F10Comment	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with an actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with and actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.

TCPWM0_GRP0_CNT8_CTRL: ENABLED		
Field	**Rev 0E**	**Rev 0F**
F0Comment	Counter Enable '0': counter disabled. '1': counter enabled. Counter static configuration register fields should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out"). The following are Counter static configuration registers: CTRL (with the exception of DEBUG_FREEZE_EN bit), DT, TR_IN_SEL0, TR_IN_SEL1, TR_IN_EDGE_SEL, TR_PWM_CTRL_TR_OUT_SEL,INTR, INTR_MASK, INTR_MASKED Modifying these registers while the counter is running could produce unexcepted waveform results, but will not cause a fatal issue such as an illegal stop, lost control, or waveform stability issues.	Counter enable. '0': counter disabled. '1': counter enabled. Counter static configuration information (e.g. CTRL.MODE, all TR_IN_SEL, TR_IN_EDGE_SEL, TR_PWM_CTRL and TR_OUT_SEL register fields) should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out").

TCPWM0_GRP0_CNT8_CTRL: AUTO_RELOAD_PERIOD		
Field	**Rev 0E**	**Rev 0F**
F10Comment	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with an actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with and actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.

TCPWM0_GRP0_CNT9_CTRL: ENABLED		
Field	**Rev 0E**	**Rev 0F**
F0Comment	Counter Enable '0': counter disabled. '1': counter enabled. Counter static configuration register fields should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out"). The following are Counter static configuration registers: CTRL (with the exception of DEBUG_FREEZE_EN bit), DT, TR_IN_SEL0, TR_IN_SEL1, TR_IN_EDGE_SEL, TR_PWM_CTRL_TR_OUT_SEL,INTR, INTR_MASK, INTR_MASKED Modifying these registers while the counter is running could produce unexcepted waveform results, but will not cause a fatal issue such as an illegal stop, lost control, or waveform stability issues.	Counter enable. '0': counter disabled. '1': counter enabled. Counter static configuration information (e.g. CTRL.MODE, all TR_IN_SEL, TR_IN_EDGE_SEL, TR_PWM_CTRL and TR_OUT_SEL register fields) should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out").

TCPWM0_GRP0_CNT9_CTRL: AUTO_RELOAD_PERIOD		
Field	**Rev 0E**	**Rev 0F**
F10Comment	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with an actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with and actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.

TCPWM0_GRP0_CNT10_CTRL: ENABLED		
Field	**Rev 0E**	**Rev 0F**
F0Comment	Counter Enable '0': counter disabled. '1': counter enabled. Counter static configuration register fields should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out"). The following are Counter static configuration registers: CTRL (with the exception of DEBUG_FREEZE_EN bit), DT, TR_IN_SEL0, TR_IN_SEL1, TR_IN_EDGE_SEL, TR_PWM_CTRL_TR_OUT_SEL,INTR, INTR_MASK, INTR_MASKED Modifying these registers while the counter is running could produce unexcepted waveform results, but will not cause a fatal issue such as an illegal stop, lost control, or waveform stability issues.	Counter enable. '0': counter disabled. '1': counter enabled. Counter static configuration information (e.g. CTRL.MODE, all TR_IN_SEL, TR_IN_EDGE_SEL, TR_PWM_CTRL and TR_OUT_SEL register fields) should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out").

TCPWM0_GRP0_CNT10_CTRL: AUTO_RELOAD_PERIOD		
Field	**Rev 0E**	**Rev 0F**
F10Comment	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with an actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with and actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.

TCPWM0_GRP0_CNT11_CTRL: ENABLED		
Field	**Rev 0E**	**Rev 0F**
F0Comment	Counter Enable '0': counter disabled. '1': counter enabled. Counter static configuration register fields should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out"). The following are Counter static configuration registers: CTRL (with the exception of DEBUG_FREEZE_EN bit), DT, TR_IN_SEL0, TR_IN_SEL1, TR_IN_EDGE_SEL, TR_PWM_CTRL_TR_OUT_SEL,INTR, INTR_MASK, INTR_MASKED Modifying these registers while the counter is running could produce unexcepted waveform results, but will not cause a fatal issue such as an illegal stop, lost control, or waveform stability issues.	Counter enable. '0': counter disabled. '1': counter enabled. Counter static configuration information (e.g. CTRL.MODE, all TR_IN_SEL, TR_IN_EDGE_SEL, TR_PWM_CTRL and TR_OUT_SEL register fields) should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out").

TCPWM0_GRP0_CNT11_CTRL: AUTO_RELOAD_PERIOD		
Field	**Rev 0E**	**Rev 0F**
F10Comment	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with an actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with and actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.

TCPWM0_GRP0_CNT12_CTRL: ENABLED		
Field	**Rev 0E**	**Rev 0F**
F0Comment	Counter Enable '0': counter disabled. '1': counter enabled. Counter static configuration register fields should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out"). The following are Counter static configuration registers: CTRL (with the exception of DEBUG_FREEZE_EN bit), DT, TR_IN_SEL0, TR_IN_SEL1, TR_IN_EDGE_SEL, TR_PWM_CTRL_TR_OUT_SEL,INTR, INTR_MASK, INTR_MASKED Modifying these registers while the counter is running could produce unexcepted waveform results, but will not cause a fatal issue such as an illegal stop, lost control, or waveform stability issues.	Counter enable. '0': counter disabled. '1': counter enabled. Counter static configuration information (e.g. CTRL.MODE, all TR_IN_SEL, TR_IN_EDGE_SEL, TR_PWM_CTRL and TR_OUT_SEL register fields) should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out").

TCPWM0_GRP0_CNT12_CTRL: AUTO_RELOAD_PERIOD		
Field	**Rev 0E**	**Rev 0F**
F10Comment	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with an actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with and actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.

TCPWM0_GRP0_CNT13_CTRL: ENABLED		
Field	**Rev 0E**	**Rev 0F**
F0Comment	Counter Enable '0': counter disabled. '1': counter enabled. Counter static configuration register fields should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out"). The following are Counter static configuration registers: CTRL (with the exception of DEBUG_FREEZE_EN bit), DT, TR_IN_SEL0, TR_IN_SEL1, TR_IN_EDGE_SEL, TR_PWM_CTRL_TR_OUT_SEL,INTR, INTR_MASK, INTR_MASKED Modifying these registers while the counter is running could produce unexcepted waveform results, but will not cause a fatal issue such as an illegal stop, lost control, or waveform stability issues.	Counter enable. '0': counter disabled. '1': counter enabled. Counter static configuration information (e.g. CTRL.MODE, all TR_IN_SEL, TR_IN_EDGE_SEL, TR_PWM_CTRL and TR_OUT_SEL register fields) should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out").

TCPWM0_GRP0_CNT13_CTRL: AUTO_RELOAD_PERIOD		
Field	**Rev 0E**	**Rev 0F**
F10Comment	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with an actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with and actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.

TCPWM0_GRP0_CNT14_CTRL: ENABLED		
Field	**Rev 0E**	**Rev 0F**
F0Comment	Counter Enable '0': counter disabled. '1': counter enabled. Counter static configuration register fields should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out"). The following are Counter static configuration registers: CTRL (with the exception of DEBUG_FREEZE_EN bit), DT, TR_IN_SEL0, TR_IN_SEL1, TR_IN_EDGE_SEL, TR_PWM_CTRL_TR_OUT_SEL,INTR, INTR_MASK, INTR_MASKED Modifying these registers while the counter is running could produce unexcepted waveform results, but will not cause a fatal issue such as an illegal stop, lost control, or waveform stability issues.	Counter enable. '0': counter disabled. '1': counter enabled. Counter static configuration information (e.g. CTRL.MODE, all TR_IN_SEL, TR_IN_EDGE_SEL, TR_PWM_CTRL and TR_OUT_SEL register fields) should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out").

TCPWM0_GRP0_CNT14_CTRL: AUTO_RELOAD_PERIOD		
Field	**Rev 0E**	**Rev 0F**
F10Comment	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with an actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with and actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.

TCPWM0_GRP0_CNT15_CTRL: ENABLED		
Field	**Rev 0E**	**Rev 0F**
F0Comment	Counter Enable '0': counter disabled. '1': counter enabled. Counter static configuration register fields should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out"). The following are Counter static configuration registers: CTRL (with the exception of DEBUG_FREEZE_EN bit), DT, TR_IN_SEL0, TR_IN_SEL1, TR_IN_EDGE_SEL, TR_PWM_CTRL_TR_OUT_SEL,INTR, INTR_MASK, INTR_MASKED Modifying these registers while the counter is running could produce unexcepted waveform results, but will not cause a fatal issue such as an illegal stop, lost control, or waveform stability issues.	Counter enable. '0': counter disabled. '1': counter enabled. Counter static configuration information (e.g. CTRL.MODE, all TR_IN_SEL, TR_IN_EDGE_SEL, TR_PWM_CTRL and TR_OUT_SEL register fields) should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out").

TCPWM0_GRP0_CNT15_CTRL: AUTO_RELOAD_PERIOD		
Field	**Rev 0E**	**Rev 0F**
F10Comment	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with an actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with and actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.

TCPWM0_GRP0_CNT16_CTRL: ENABLED		
Field	**Rev 0E**	**Rev 0F**
F0Comment	Counter Enable '0': counter disabled. '1': counter enabled. Counter static configuration register fields should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out"). The following are Counter static configuration registers: CTRL (with the exception of DEBUG_FREEZE_EN bit), DT, TR_IN_SEL0, TR_IN_SEL1, TR_IN_EDGE_SEL, TR_PWM_CTRL_TR_OUT_SEL,INTR, INTR_MASK, INTR_MASKED Modifying these registers while the counter is running could produce unexcepted waveform results, but will not cause a fatal issue such as an illegal stop, lost control, or waveform stability issues.	Counter enable. '0': counter disabled. '1': counter enabled. Counter static configuration information (e.g. CTRL.MODE, all TR_IN_SEL, TR_IN_EDGE_SEL, TR_PWM_CTRL and TR_OUT_SEL register fields) should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out").

TCPWM0_GRP0_CNT16_CTRL: AUTO_RELOAD_PERIOD		
Field	**Rev 0E**	**Rev 0F**
F10Comment	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with an actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with and actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.

TCPWM0_GRP0_CNT17_CTRL: ENABLED		
Field	**Rev 0E**	**Rev 0F**
F0Comment	Counter Enable '0': counter disabled. '1': counter enabled. Counter static configuration register fields should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out"). The following are Counter static configuration registers: CTRL (with the exception of DEBUG_FREEZE_EN bit), DT, TR_IN_SEL0, TR_IN_SEL1, TR_IN_EDGE_SEL, TR_PWM_CTRL_TR_OUT_SEL,INTR, INTR_MASK, INTR_MASKED Modifying these registers while the counter is running could produce unexcepted waveform results, but will not cause a fatal issue such as an illegal stop, lost control, or waveform stability issues.	Counter enable. '0': counter disabled. '1': counter enabled. Counter static configuration information (e.g. CTRL.MODE, all TR_IN_SEL, TR_IN_EDGE_SEL, TR_PWM_CTRL and TR_OUT_SEL register fields) should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out").

TCPWM0_GRP0_CNT17_CTRL: AUTO_RELOAD_PERIOD		
Field	**Rev 0E**	**Rev 0F**
F10Comment	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with an actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with and actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.

TCPWM0_GRP0_CNT18_CTRL: ENABLED		
Field	**Rev 0E**	**Rev 0F**
F0Comment	Counter Enable '0': counter disabled. '1': counter enabled. Counter static configuration register fields should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out"). The following are Counter static configuration registers: CTRL (with the exception of DEBUG_FREEZE_EN bit), DT, TR_IN_SEL0, TR_IN_SEL1, TR_IN_EDGE_SEL, TR_PWM_CTRL_TR_OUT_SEL,INTR, INTR_MASK, INTR_MASKED Modifying these registers while the counter is running could produce unexcepted waveform results, but will not cause a fatal issue such as an illegal stop, lost control, or waveform stability issues.	Counter enable. '0': counter disabled. '1': counter enabled. Counter static configuration information (e.g. CTRL.MODE, all TR_IN_SEL, TR_IN_EDGE_SEL, TR_PWM_CTRL and TR_OUT_SEL register fields) should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out").

TCPWM0_GRP0_CNT18_CTRL: AUTO_RELOAD_PERIOD		
Field	**Rev 0E**	**Rev 0F**
F10Comment	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with an actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with and actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.

TCPWM0_GRP0_CNT19_CTRL: ENABLED		
Field	**Rev 0E**	**Rev 0F**
F0Comment	Counter Enable '0': counter disabled. '1': counter enabled. Counter static configuration register fields should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out"). The following are Counter static configuration registers: CTRL (with the exception of DEBUG_FREEZE_EN bit), DT, TR_IN_SEL0, TR_IN_SEL1, TR_IN_EDGE_SEL, TR_PWM_CTRL_TR_OUT_SEL,INTR, INTR_MASK, INTR_MASKED Modifying these registers while the counter is running could produce unexcepted waveform results, but will not cause a fatal issue such as an illegal stop, lost control, or waveform stability issues.	Counter enable. '0': counter disabled. '1': counter enabled. Counter static configuration information (e.g. CTRL.MODE, all TR_IN_SEL, TR_IN_EDGE_SEL, TR_PWM_CTRL and TR_OUT_SEL register fields) should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out").

TCPWM0_GRP0_CNT19_CTRL: AUTO_RELOAD_PERIOD		
Field	**Rev 0E**	**Rev 0F**
F10Comment	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with an actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with and actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.

TCPWM0_GRP0_CNT20_CTRL: ENABLED		
Field	**Rev 0E**	**Rev 0F**
F0Comment	Counter Enable '0': counter disabled. '1': counter enabled. Counter static configuration register fields should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out"). The following are Counter static configuration registers: CTRL (with the exception of DEBUG_FREEZE_EN bit), DT, TR_IN_SEL0, TR_IN_SEL1, TR_IN_EDGE_SEL, TR_PWM_CTRL_TR_OUT_SEL,INTR, INTR_MASK, INTR_MASKED Modifying these registers while the counter is running could produce unexcepted waveform results, but will not cause a fatal issue such as an illegal stop, lost control, or waveform stability issues.	Counter enable. '0': counter disabled. '1': counter enabled. Counter static configuration information (e.g. CTRL.MODE, all TR_IN_SEL, TR_IN_EDGE_SEL, TR_PWM_CTRL and TR_OUT_SEL register fields) should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out").

TCPWM0_GRP0_CNT20_CTRL: AUTO_RELOAD_PERIOD		
Field	**Rev 0E**	**Rev 0F**
F10Comment	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with an actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with and actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.

TCPWM0_GRP0_CNT21_CTRL: ENABLED		
Field	**Rev 0E**	**Rev 0F**
F0Comment	Counter Enable '0': counter disabled. '1': counter enabled. Counter static configuration register fields should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out"). The following are Counter static configuration registers: CTRL (with the exception of DEBUG_FREEZE_EN bit), DT, TR_IN_SEL0, TR_IN_SEL1, TR_IN_EDGE_SEL, TR_PWM_CTRL_TR_OUT_SEL,INTR, INTR_MASK, INTR_MASKED Modifying these registers while the counter is running could produce unexcepted waveform results, but will not cause a fatal issue such as an illegal stop, lost control, or waveform stability issues.	Counter enable. '0': counter disabled. '1': counter enabled. Counter static configuration information (e.g. CTRL.MODE, all TR_IN_SEL, TR_IN_EDGE_SEL, TR_PWM_CTRL and TR_OUT_SEL register fields) should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out").

TCPWM0_GRP0_CNT21_CTRL: AUTO_RELOAD_PERIOD		
Field	**Rev 0E**	**Rev 0F**
F10Comment	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with an actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with and actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.

TCPWM0_GRP0_CNT22_CTRL: ENABLED		
Field	**Rev 0E**	**Rev 0F**
F0Comment	Counter Enable '0': counter disabled. '1': counter enabled. Counter static configuration register fields should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out"). The following are Counter static configuration registers: CTRL (with the exception of DEBUG_FREEZE_EN bit), DT, TR_IN_SEL0, TR_IN_SEL1, TR_IN_EDGE_SEL, TR_PWM_CTRL_TR_OUT_SEL,INTR, INTR_MASK, INTR_MASKED Modifying these registers while the counter is running could produce unexcepted waveform results, but will not cause a fatal issue such as an illegal stop, lost control, or waveform stability issues.	Counter enable. '0': counter disabled. '1': counter enabled. Counter static configuration information (e.g. CTRL.MODE, all TR_IN_SEL, TR_IN_EDGE_SEL, TR_PWM_CTRL and TR_OUT_SEL register fields) should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out").

TCPWM0_GRP0_CNT22_CTRL: AUTO_RELOAD_PERIOD		
Field	**Rev 0E**	**Rev 0F**
F10Comment	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with an actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with and actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.

TCPWM0_GRP0_CNT23_CTRL: ENABLED		
Field	**Rev 0E**	**Rev 0F**
F0Comment	Counter Enable '0': counter disabled. '1': counter enabled. Counter static configuration register fields should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out"). The following are Counter static configuration registers: CTRL (with the exception of DEBUG_FREEZE_EN bit), DT, TR_IN_SEL0, TR_IN_SEL1, TR_IN_EDGE_SEL, TR_PWM_CTRL_TR_OUT_SEL,INTR, INTR_MASK, INTR_MASKED Modifying these registers while the counter is running could produce unexcepted waveform results, but will not cause a fatal issue such as an illegal stop, lost control, or waveform stability issues.	Counter enable. '0': counter disabled. '1': counter enabled. Counter static configuration information (e.g. CTRL.MODE, all TR_IN_SEL, TR_IN_EDGE_SEL, TR_PWM_CTRL and TR_OUT_SEL register fields) should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out").

TCPWM0_GRP0_CNT23_CTRL: AUTO_RELOAD_PERIOD		
Field	**Rev 0E**	**Rev 0F**
F10Comment	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with an actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with and actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.

TCPWM0_GRP0_CNT24_CTRL: ENABLED		
Field	**Rev 0E**	**Rev 0F**
F0Comment	Counter Enable '0': counter disabled. '1': counter enabled. Counter static configuration register fields should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out"). The following are Counter static configuration registers: CTRL (with the exception of DEBUG_FREEZE_EN bit), DT, TR_IN_SEL0, TR_IN_SEL1, TR_IN_EDGE_SEL, TR_PWM_CTRL_TR_OUT_SEL,INTR, INTR_MASK, INTR_MASKED Modifying these registers while the counter is running could produce unexcepted waveform results, but will not cause a fatal issue such as an illegal stop, lost control, or waveform stability issues.	Counter enable. '0': counter disabled. '1': counter enabled. Counter static configuration information (e.g. CTRL.MODE, all TR_IN_SEL, TR_IN_EDGE_SEL, TR_PWM_CTRL and TR_OUT_SEL register fields) should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out").

TCPWM0_GRP0_CNT24_CTRL: AUTO_RELOAD_PERIOD		
Field	**Rev 0E**	**Rev 0F**
F10Comment	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with an actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with and actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.

TCPWM0_GRP0_CNT25_CTRL: ENABLED		
Field	**Rev 0E**	**Rev 0F**
F0Comment	Counter Enable '0': counter disabled. '1': counter enabled. Counter static configuration register fields should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out"). The following are Counter static configuration registers: CTRL (with the exception of DEBUG_FREEZE_EN bit), DT, TR_IN_SEL0, TR_IN_SEL1, TR_IN_EDGE_SEL, TR_PWM_CTRL_TR_OUT_SEL,INTR, INTR_MASK, INTR_MASKED Modifying these registers while the counter is running could produce unexcepted waveform results, but will not cause a fatal issue such as an illegal stop, lost control, or waveform stability issues.	Counter enable. '0': counter disabled. '1': counter enabled. Counter static configuration information (e.g. CTRL.MODE, all TR_IN_SEL, TR_IN_EDGE_SEL, TR_PWM_CTRL and TR_OUT_SEL register fields) should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out").

TCPWM0_GRP0_CNT25_CTRL: AUTO_RELOAD_PERIOD		
Field	**Rev 0E**	**Rev 0F**
F10Comment	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with an actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with and actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.

TCPWM0_GRP0_CNT26_CTRL: ENABLED		
Field	**Rev 0E**	**Rev 0F**
F0Comment	Counter Enable '0': counter disabled. '1': counter enabled. Counter static configuration register fields should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out"). The following are Counter static configuration registers: CTRL (with the exception of DEBUG_FREEZE_EN bit), DT, TR_IN_SEL0, TR_IN_SEL1, TR_IN_EDGE_SEL, TR_PWM_CTRL_TR_OUT_SEL,INTR, INTR_MASK, INTR_MASKED Modifying these registers while the counter is running could produce unexcepted waveform results, but will not cause a fatal issue such as an illegal stop, lost control, or waveform stability issues.	Counter enable. '0': counter disabled. '1': counter enabled. Counter static configuration information (e.g. CTRL.MODE, all TR_IN_SEL, TR_IN_EDGE_SEL, TR_PWM_CTRL and TR_OUT_SEL register fields) should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out").

TCPWM0_GRP0_CNT26_CTRL: AUTO_RELOAD_PERIOD		
Field	**Rev 0E**	**Rev 0F**
F10Comment	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with an actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with and actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.

TCPWM0_GRP0_CNT27_CTRL: ENABLED		
Field	**Rev 0E**	**Rev 0F**
F0Comment	Counter Enable '0': counter disabled. '1': counter enabled. Counter static configuration register fields should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out"). The following are Counter static configuration registers: CTRL (with the exception of DEBUG_FREEZE_EN bit), DT, TR_IN_SEL0, TR_IN_SEL1, TR_IN_EDGE_SEL, TR_PWM_CTRL_TR_OUT_SEL,INTR, INTR_MASK, INTR_MASKED Modifying these registers while the counter is running could produce unexcepted waveform results, but will not cause a fatal issue such as an illegal stop, lost control, or waveform stability issues.	Counter enable. '0': counter disabled. '1': counter enabled. Counter static configuration information (e.g. CTRL.MODE, all TR_IN_SEL, TR_IN_EDGE_SEL, TR_PWM_CTRL and TR_OUT_SEL register fields) should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out").

TCPWM0_GRP0_CNT27_CTRL: AUTO_RELOAD_PERIOD		
Field	**Rev 0E**	**Rev 0F**
F10Comment	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with an actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with and actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.

TCPWM0_GRP0_CNT28_CTRL: ENABLED		
Field	**Rev 0E**	**Rev 0F**
F0Comment	Counter Enable '0': counter disabled. '1': counter enabled. Counter static configuration register fields should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out"). The following are Counter static configuration registers: CTRL (with the exception of DEBUG_FREEZE_EN bit), DT, TR_IN_SEL0, TR_IN_SEL1, TR_IN_EDGE_SEL, TR_PWM_CTRL_TR_OUT_SEL,INTR, INTR_MASK, INTR_MASKED Modifying these registers while the counter is running could produce unexcepted waveform results, but will not cause a fatal issue such as an illegal stop, lost control, or waveform stability issues.	Counter enable. '0': counter disabled. '1': counter enabled. Counter static configuration information (e.g. CTRL.MODE, all TR_IN_SEL, TR_IN_EDGE_SEL, TR_PWM_CTRL and TR_OUT_SEL register fields) should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out").

TCPWM0_GRP0_CNT28_CTRL: AUTO_RELOAD_PERIOD		
Field	**Rev 0E**	**Rev 0F**
F10Comment	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with an actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with and actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.

TCPWM0_GRP0_CNT29_CTRL: ENABLED		
Field	**Rev 0E**	**Rev 0F**
F0Comment	Counter Enable '0': counter disabled. '1': counter enabled. Counter static configuration register fields should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out"). The following are Counter static configuration registers: CTRL (with the exception of DEBUG_FREEZE_EN bit), DT, TR_IN_SEL0, TR_IN_SEL1, TR_IN_EDGE_SEL, TR_PWM_CTRL_TR_OUT_SEL,INTR, INTR_MASK, INTR_MASKED Modifying these registers while the counter is running could produce unexcepted waveform results, but will not cause a fatal issue such as an illegal stop, lost control, or waveform stability issues.	Counter enable. '0': counter disabled. '1': counter enabled. Counter static configuration information (e.g. CTRL.MODE, all TR_IN_SEL, TR_IN_EDGE_SEL, TR_PWM_CTRL and TR_OUT_SEL register fields) should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out").

TCPWM0_GRP0_CNT29_CTRL: AUTO_RELOAD_PERIOD		
Field	**Rev 0E**	**Rev 0F**
F10Comment	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with an actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with and actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.

TCPWM0_GRP0_CNT30_CTRL: ENABLED		
Field	**Rev 0E**	**Rev 0F**
F0Comment	Counter Enable '0': counter disabled. '1': counter enabled. Counter static configuration register fields should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out"). The following are Counter static configuration registers: CTRL (with the exception of DEBUG_FREEZE_EN bit), DT, TR_IN_SEL0, TR_IN_SEL1, TR_IN_EDGE_SEL, TR_PWM_CTRL_TR_OUT_SEL,INTR, INTR_MASK, INTR_MASKED Modifying these registers while the counter is running could produce unexcepted waveform results, but will not cause a fatal issue such as an illegal stop, lost control, or waveform stability issues.	Counter enable. '0': counter disabled. '1': counter enabled. Counter static configuration information (e.g. CTRL.MODE, all TR_IN_SEL, TR_IN_EDGE_SEL, TR_PWM_CTRL and TR_OUT_SEL register fields) should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out").

TCPWM0_GRP0_CNT30_CTRL: AUTO_RELOAD_PERIOD		
Field	**Rev 0E**	**Rev 0F**
F10Comment	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with an actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with and actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.

TCPWM0_GRP0_CNT31_CTRL: ENABLED		
Field	**Rev 0E**	**Rev 0F**
F0Comment	Counter Enable '0': counter disabled. '1': counter enabled. Counter static configuration register fields should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out"). The following are Counter static configuration registers: CTRL (with the exception of DEBUG_FREEZE_EN bit), DT, TR_IN_SEL0, TR_IN_SEL1, TR_IN_EDGE_SEL, TR_PWM_CTRL_TR_OUT_SEL,INTR, INTR_MASK, INTR_MASKED Modifying these registers while the counter is running could produce unexcepted waveform results, but will not cause a fatal issue such as an illegal stop, lost control, or waveform stability issues.	Counter enable. '0': counter disabled. '1': counter enabled. Counter static configuration information (e.g. CTRL.MODE, all TR_IN_SEL, TR_IN_EDGE_SEL, TR_PWM_CTRL and TR_OUT_SEL register fields) should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out").

TCPWM0_GRP0_CNT31_CTRL: AUTO_RELOAD_PERIOD		
Field	**Rev 0E**	**Rev 0F**
F10Comment	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with an actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with and actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.

TCPWM0_GRP0_CNT32_CTRL: ENABLED		
Field	**Rev 0E**	**Rev 0F**
F0Comment	Counter Enable '0': counter disabled. '1': counter enabled. Counter static configuration register fields should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out"). The following are Counter static configuration registers: CTRL (with the exception of DEBUG_FREEZE_EN bit), DT, TR_IN_SEL0, TR_IN_SEL1, TR_IN_EDGE_SEL, TR_PWM_CTRL_TR_OUT_SEL,INTR, INTR_MASK, INTR_MASKED Modifying these registers while the counter is running could produce unexcepted waveform results, but will not cause a fatal issue such as an illegal stop, lost control, or waveform stability issues.	Counter enable. '0': counter disabled. '1': counter enabled. Counter static configuration information (e.g. CTRL.MODE, all TR_IN_SEL, TR_IN_EDGE_SEL, TR_PWM_CTRL and TR_OUT_SEL register fields) should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out").

TCPWM0_GRP0_CNT32_CTRL: AUTO_RELOAD_PERIOD		
Field	**Rev 0E**	**Rev 0F**
F10Comment	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with an actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with and actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.

TCPWM0_GRP0_CNT33_CTRL: ENABLED		
Field	**Rev 0E**	**Rev 0F**
F0Comment	Counter Enable '0': counter disabled. '1': counter enabled. Counter static configuration register fields should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out"). The following are Counter static configuration registers: CTRL (with the exception of DEBUG_FREEZE_EN bit), DT, TR_IN_SEL0, TR_IN_SEL1, TR_IN_EDGE_SEL, TR_PWM_CTRL_TR_OUT_SEL,INTR, INTR_MASK, INTR_MASKED Modifying these registers while the counter is running could produce unexcepted waveform results, but will not cause a fatal issue such as an illegal stop, lost control, or waveform stability issues.	Counter enable. '0': counter disabled. '1': counter enabled. Counter static configuration information (e.g. CTRL.MODE, all TR_IN_SEL, TR_IN_EDGE_SEL, TR_PWM_CTRL and TR_OUT_SEL register fields) should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out").

TCPWM0_GRP0_CNT33_CTRL: AUTO_RELOAD_PERIOD		
Field	**Rev 0E**	**Rev 0F**
F10Comment	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with an actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with and actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.

TCPWM0_GRP0_CNT34_CTRL: ENABLED		
Field	**Rev 0E**	**Rev 0F**
F0Comment	Counter Enable '0': counter disabled. '1': counter enabled. Counter static configuration register fields should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out"). The following are Counter static configuration registers: CTRL (with the exception of DEBUG_FREEZE_EN bit), DT, TR_IN_SEL0, TR_IN_SEL1, TR_IN_EDGE_SEL, TR_PWM_CTRL_TR_OUT_SEL,INTR, INTR_MASK, INTR_MASKED Modifying these registers while the counter is running could produce unexcepted waveform results, but will not cause a fatal issue such as an illegal stop, lost control, or waveform stability issues.	Counter enable. '0': counter disabled. '1': counter enabled. Counter static configuration information (e.g. CTRL.MODE, all TR_IN_SEL, TR_IN_EDGE_SEL, TR_PWM_CTRL and TR_OUT_SEL register fields) should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out").

TCPWM0_GRP0_CNT34_CTRL: AUTO_RELOAD_PERIOD		
Field	**Rev 0E**	**Rev 0F**
F10Comment	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with an actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with and actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.

TCPWM0_GRP0_CNT35_CTRL: ENABLED		
Field	**Rev 0E**	**Rev 0F**
F0Comment	Counter Enable '0': counter disabled. '1': counter enabled. Counter static configuration register fields should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out"). The following are Counter static configuration registers: CTRL (with the exception of DEBUG_FREEZE_EN bit), DT, TR_IN_SEL0, TR_IN_SEL1, TR_IN_EDGE_SEL, TR_PWM_CTRL_TR_OUT_SEL,INTR, INTR_MASK, INTR_MASKED Modifying these registers while the counter is running could produce unexcepted waveform results, but will not cause a fatal issue such as an illegal stop, lost control, or waveform stability issues.	Counter enable. '0': counter disabled. '1': counter enabled. Counter static configuration information (e.g. CTRL.MODE, all TR_IN_SEL, TR_IN_EDGE_SEL, TR_PWM_CTRL and TR_OUT_SEL register fields) should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out").

TCPWM0_GRP0_CNT35_CTRL: AUTO_RELOAD_PERIOD		
Field	**Rev 0E**	**Rev 0F**
F10Comment	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with an actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with and actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.

TCPWM0_GRP0_CNT36_CTRL: ENABLED		
Field	**Rev 0E**	**Rev 0F**
F0Comment	Counter Enable '0': counter disabled. '1': counter enabled. Counter static configuration register fields should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out"). The following are Counter static configuration registers: CTRL (with the exception of DEBUG_FREEZE_EN bit), DT, TR_IN_SEL0, TR_IN_SEL1, TR_IN_EDGE_SEL, TR_PWM_CTRL_TR_OUT_SEL,INTR, INTR_MASK, INTR_MASKED Modifying these registers while the counter is running could produce unexcepted waveform results, but will not cause a fatal issue such as an illegal stop, lost control, or waveform stability issues.	Counter enable. '0': counter disabled. '1': counter enabled. Counter static configuration information (e.g. CTRL.MODE, all TR_IN_SEL, TR_IN_EDGE_SEL, TR_PWM_CTRL and TR_OUT_SEL register fields) should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out").

TCPWM0_GRP0_CNT36_CTRL: AUTO_RELOAD_PERIOD		
Field	**Rev 0E**	**Rev 0F**
F10Comment	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with an actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with and actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.

TCPWM0_GRP0_CNT37_CTRL: ENABLED		
Field	**Rev 0E**	**Rev 0F**
F0Comment	Counter Enable '0': counter disabled. '1': counter enabled. Counter static configuration register fields should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out"). The following are Counter static configuration registers: CTRL (with the exception of DEBUG_FREEZE_EN bit), DT, TR_IN_SEL0, TR_IN_SEL1, TR_IN_EDGE_SEL, TR_PWM_CTRL_TR_OUT_SEL,INTR, INTR_MASK, INTR_MASKED Modifying these registers while the counter is running could produce unexcepted waveform results, but will not cause a fatal issue such as an illegal stop, lost control, or waveform stability issues.	Counter enable. '0': counter disabled. '1': counter enabled. Counter static configuration information (e.g. CTRL.MODE, all TR_IN_SEL, TR_IN_EDGE_SEL, TR_PWM_CTRL and TR_OUT_SEL register fields) should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out").

TCPWM0_GRP0_CNT37_CTRL: AUTO_RELOAD_PERIOD		
Field	**Rev 0E**	**Rev 0F**
F10Comment	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with an actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with and actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.

TCPWM0_GRP1_CNT0_CTRL: ENABLED		
Field	**Rev 0E**	**Rev 0F**
F0Comment	Counter Enable '0': counter disabled. '1': counter enabled. Counter static configuration register fields should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out"). The following are Counter static configuration registers: CTRL (with the exception of DEBUG_FREEZE_EN bit), DT, TR_IN_SEL0, TR_IN_SEL1, TR_IN_EDGE_SEL, TR_PWM_CTRL_TR_OUT_SEL,INTR, INTR_MASK, INTR_MASKED Modifying these registers while the counter is running could produce unexcepted waveform results, but will not cause a fatal issue such as an illegal stop, lost control, or waveform stability issues.	Counter enable. '0': counter disabled. '1': counter enabled. Counter static configuration information (e.g. CTRL.MODE, all TR_IN_SEL, TR_IN_EDGE_SEL, TR_PWM_CTRL and TR_OUT_SEL register fields) should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out").

TCPWM0_GRP1_CNT0_CTRL: AUTO_RELOAD_LINE_SEL		
Field	**Rev 0E**	**Rev 0F**
F14Comment	Specifies switching of the LINE_SEL and LINE_BUFF_SEL values. This field has a function in PWM and PWM_PR modes. '0': never switch. '1': switch on a terminal count event with an actively pending switch event.	Specifies switching of the LINE_SEL and LINE_BUFF_SEL values. This field has a function in PWM and PWM_PR modes. '0': never switch. '1': switch on a terminal count event with and actively pending switch event.

TCPWM0_GRP1_CNT0_CTRL: AUTO_RELOAD_PERIOD		
Field	**Rev 0E**	**Rev 0F**
F15Comment	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with an actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with and actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.

TCPWM0_GRP1_CNT1_CTRL: ENABLED		
Field	**Rev 0E**	**Rev 0F**
F0Comment	Counter Enable '0': counter disabled. '1': counter enabled. Counter static configuration register fields should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out"). The following are Counter static configuration registers: CTRL (with the exception of DEBUG_FREEZE_EN bit), DT, TR_IN_SEL0, TR_IN_SEL1, TR_IN_EDGE_SEL, TR_PWM_CTRL_TR_OUT_SEL,INTR, INTR_MASK, INTR_MASKED Modifying these registers while the counter is running could produce unexcepted waveform results, but will not cause a fatal issue such as an illegal stop, lost control, or waveform stability issues.	Counter enable. '0': counter disabled. '1': counter enabled. Counter static configuration information (e.g. CTRL.MODE, all TR_IN_SEL, TR_IN_EDGE_SEL, TR_PWM_CTRL and TR_OUT_SEL register fields) should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out").

TCPWM0_GRP1_CNT1_CTRL: AUTO_RELOAD_LINE_SEL		
Field	**Rev 0E**	**Rev 0F**
F14Comment	Specifies switching of the LINE_SEL and LINE_BUFF_SEL values. This field has a function in PWM and PWM_PR modes. '0': never switch. '1': switch on a terminal count event with an actively pending switch event.	Specifies switching of the LINE_SEL and LINE_BUFF_SEL values. This field has a function in PWM and PWM_PR modes. '0': never switch. '1': switch on a terminal count event with and actively pending switch event.

TCPWM0_GRP1_CNT1_CTRL: AUTO_RELOAD_PERIOD		
Field	**Rev 0E**	**Rev 0F**
F15Comment	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with an actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with and actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.

TCPWM0_GRP1_CNT2_CTRL: ENABLED		
Field	**Rev 0E**	**Rev 0F**
F0Comment	Counter Enable '0': counter disabled. '1': counter enabled. Counter static configuration register fields should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out"). The following are Counter static configuration registers: CTRL (with the exception of DEBUG_FREEZE_EN bit), DT, TR_IN_SEL0, TR_IN_SEL1, TR_IN_EDGE_SEL, TR_PWM_CTRL_TR_OUT_SEL,INTR, INTR_MASK, INTR_MASKED Modifying these registers while the counter is running could produce unexcepted waveform results, but will not cause a fatal issue such as an illegal stop, lost control, or waveform stability issues.	Counter enable. '0': counter disabled. '1': counter enabled. Counter static configuration information (e.g. CTRL.MODE, all TR_IN_SEL, TR_IN_EDGE_SEL, TR_PWM_CTRL and TR_OUT_SEL register fields) should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out").

TCPWM0_GRP1_CNT2_CTRL: AUTO_RELOAD_LINE_SEL		
Field	**Rev 0E**	**Rev 0F**
F14Comment	Specifies switching of the LINE_SEL and LINE_BUFF_SEL values. This field has a function in PWM and PWM_PR modes. '0': never switch. '1': switch on a terminal count event with an actively pending switch event.	Specifies switching of the LINE_SEL and LINE_BUFF_SEL values. This field has a function in PWM and PWM_PR modes. '0': never switch. '1': switch on a terminal count event with and actively pending switch event.

TCPWM0_GRP1_CNT2_CTRL: AUTO_RELOAD_PERIOD		
Field	**Rev 0E**	**Rev 0F**
F15Comment	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with an actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with and actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.

TCPWM0_GRP1_CNT3_CTRL: ENABLED		
Field	**Rev 0E**	**Rev 0F**
F0Comment	Counter Enable '0': counter disabled. '1': counter enabled. Counter static configuration register fields should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out"). The following are Counter static configuration registers: CTRL (with the exception of DEBUG_FREEZE_EN bit), DT, TR_IN_SEL0, TR_IN_SEL1, TR_IN_EDGE_SEL, TR_PWM_CTRL_TR_OUT_SEL,INTR, INTR_MASK, INTR_MASKED Modifying these registers while the counter is running could produce unexcepted waveform results, but will not cause a fatal issue such as an illegal stop, lost control, or waveform stability issues.	Counter enable. '0': counter disabled. '1': counter enabled. Counter static configuration information (e.g. CTRL.MODE, all TR_IN_SEL, TR_IN_EDGE_SEL, TR_PWM_CTRL and TR_OUT_SEL register fields) should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out").

TCPWM0_GRP1_CNT3_CTRL: AUTO_RELOAD_LINE_SEL		
Field	**Rev 0E**	**Rev 0F**
F14Comment	Specifies switching of the LINE_SEL and LINE_BUFF_SEL values. This field has a function in PWM and PWM_PR modes. '0': never switch. '1': switch on a terminal count event with an actively pending switch event.	Specifies switching of the LINE_SEL and LINE_BUFF_SEL values. This field has a function in PWM and PWM_PR modes. '0': never switch. '1': switch on a terminal count event with and actively pending switch event.

TCPWM0_GRP1_CNT3_CTRL: AUTO_RELOAD_PERIOD		
Field	**Rev 0E**	**Rev 0F**
F15Comment	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with an actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with and actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.

TCPWM0_GRP1_CNT4_CTRL: ENABLED		
Field	**Rev 0E**	**Rev 0F**
F0Comment	Counter Enable '0': counter disabled. '1': counter enabled. Counter static configuration register fields should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out"). The following are Counter static configuration registers: CTRL (with the exception of DEBUG_FREEZE_EN bit), DT, TR_IN_SEL0, TR_IN_SEL1, TR_IN_EDGE_SEL, TR_PWM_CTRL_TR_OUT_SEL,INTR, INTR_MASK, INTR_MASKED Modifying these registers while the counter is running could produce unexcepted waveform results, but will not cause a fatal issue such as an illegal stop, lost control, or waveform stability issues.	Counter enable. '0': counter disabled. '1': counter enabled. Counter static configuration information (e.g. CTRL.MODE, all TR_IN_SEL, TR_IN_EDGE_SEL, TR_PWM_CTRL and TR_OUT_SEL register fields) should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out").

TCPWM0_GRP1_CNT4_CTRL: AUTO_RELOAD_LINE_SEL		
Field	**Rev 0E**	**Rev 0F**
F14Comment	Specifies switching of the LINE_SEL and LINE_BUFF_SEL values. This field has a function in PWM and PWM_PR modes. '0': never switch. '1': switch on a terminal count event with an actively pending switch event.	Specifies switching of the LINE_SEL and LINE_BUFF_SEL values. This field has a function in PWM and PWM_PR modes. '0': never switch. '1': switch on a terminal count event with and actively pending switch event.

TCPWM0_GRP1_CNT4_CTRL: AUTO_RELOAD_PERIOD		
Field	**Rev 0E**	**Rev 0F**
F15Comment	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with an actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with and actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.

TCPWM0_GRP1_CNT5_CTRL: ENABLED		
Field	**Rev 0E**	**Rev 0F**
F0Comment	Counter Enable '0': counter disabled. '1': counter enabled. Counter static configuration register fields should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out"). The following are Counter static configuration registers: CTRL (with the exception of DEBUG_FREEZE_EN bit), DT, TR_IN_SEL0, TR_IN_SEL1, TR_IN_EDGE_SEL, TR_PWM_CTRL_TR_OUT_SEL,INTR, INTR_MASK, INTR_MASKED Modifying these registers while the counter is running could produce unexcepted waveform results, but will not cause a fatal issue such as an illegal stop, lost control, or waveform stability issues.	Counter enable. '0': counter disabled. '1': counter enabled. Counter static configuration information (e.g. CTRL.MODE, all TR_IN_SEL, TR_IN_EDGE_SEL, TR_PWM_CTRL and TR_OUT_SEL register fields) should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out").

TCPWM0_GRP1_CNT5_CTRL: AUTO_RELOAD_LINE_SEL		
Field	**Rev 0E**	**Rev 0F**
F14Comment	Specifies switching of the LINE_SEL and LINE_BUFF_SEL values. This field has a function in PWM and PWM_PR modes. '0': never switch. '1': switch on a terminal count event with an actively pending switch event.	Specifies switching of the LINE_SEL and LINE_BUFF_SEL values. This field has a function in PWM and PWM_PR modes. '0': never switch. '1': switch on a terminal count event with and actively pending switch event.

TCPWM0_GRP1_CNT5_CTRL: AUTO_RELOAD_PERIOD		
Field	**Rev 0E**	**Rev 0F**
F15Comment	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with an actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with and actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.

TCPWM0_GRP1_CNT6_CTRL: ENABLED		
Field	**Rev 0E**	**Rev 0F**
F0Comment	Counter Enable '0': counter disabled. '1': counter enabled. Counter static configuration register fields should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out"). The following are Counter static configuration registers: CTRL (with the exception of DEBUG_FREEZE_EN bit), DT, TR_IN_SEL0, TR_IN_SEL1, TR_IN_EDGE_SEL, TR_PWM_CTRL_TR_OUT_SEL,INTR, INTR_MASK, INTR_MASKED Modifying these registers while the counter is running could produce unexcepted waveform results, but will not cause a fatal issue such as an illegal stop, lost control, or waveform stability issues.	Counter enable. '0': counter disabled. '1': counter enabled. Counter static configuration information (e.g. CTRL.MODE, all TR_IN_SEL, TR_IN_EDGE_SEL, TR_PWM_CTRL and TR_OUT_SEL register fields) should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out").

TCPWM0_GRP1_CNT6_CTRL: AUTO_RELOAD_LINE_SEL		
Field	**Rev 0E**	**Rev 0F**
F14Comment	Specifies switching of the LINE_SEL and LINE_BUFF_SEL values. This field has a function in PWM and PWM_PR modes. '0': never switch. '1': switch on a terminal count event with an actively pending switch event.	Specifies switching of the LINE_SEL and LINE_BUFF_SEL values. This field has a function in PWM and PWM_PR modes. '0': never switch. '1': switch on a terminal count event with and actively pending switch event.

TCPWM0_GRP1_CNT6_CTRL: AUTO_RELOAD_PERIOD		
Field	**Rev 0E**	**Rev 0F**
F15Comment	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with an actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with and actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.

TCPWM0_GRP1_CNT7_CTRL: ENABLED		
Field	**Rev 0E**	**Rev 0F**
F0Comment	Counter Enable '0': counter disabled. '1': counter enabled. Counter static configuration register fields should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out"). The following are Counter static configuration registers: CTRL (with the exception of DEBUG_FREEZE_EN bit), DT, TR_IN_SEL0, TR_IN_SEL1, TR_IN_EDGE_SEL, TR_PWM_CTRL_TR_OUT_SEL,INTR, INTR_MASK, INTR_MASKED Modifying these registers while the counter is running could produce unexcepted waveform results, but will not cause a fatal issue such as an illegal stop, lost control, or waveform stability issues.	Counter enable. '0': counter disabled. '1': counter enabled. Counter static configuration information (e.g. CTRL.MODE, all TR_IN_SEL, TR_IN_EDGE_SEL, TR_PWM_CTRL and TR_OUT_SEL register fields) should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out").

TCPWM0_GRP1_CNT7_CTRL: AUTO_RELOAD_LINE_SEL		
Field	**Rev 0E**	**Rev 0F**
F14Comment	Specifies switching of the LINE_SEL and LINE_BUFF_SEL values. This field has a function in PWM and PWM_PR modes. '0': never switch. '1': switch on a terminal count event with an actively pending switch event.	Specifies switching of the LINE_SEL and LINE_BUFF_SEL values. This field has a function in PWM and PWM_PR modes. '0': never switch. '1': switch on a terminal count event with and actively pending switch event.

TCPWM0_GRP1_CNT7_CTRL: AUTO_RELOAD_PERIOD		
Field	**Rev 0E**	**Rev 0F**
F15Comment	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with an actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with and actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.

TCPWM0_GRP1_CNT8_CTRL: ENABLED		
Field	**Rev 0E**	**Rev 0F**
F0Comment	Counter Enable '0': counter disabled. '1': counter enabled. Counter static configuration register fields should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out"). The following are Counter static configuration registers: CTRL (with the exception of DEBUG_FREEZE_EN bit), DT, TR_IN_SEL0, TR_IN_SEL1, TR_IN_EDGE_SEL, TR_PWM_CTRL_TR_OUT_SEL,INTR, INTR_MASK, INTR_MASKED Modifying these registers while the counter is running could produce unexcepted waveform results, but will not cause a fatal issue such as an illegal stop, lost control, or waveform stability issues.	Counter enable. '0': counter disabled. '1': counter enabled. Counter static configuration information (e.g. CTRL.MODE, all TR_IN_SEL, TR_IN_EDGE_SEL, TR_PWM_CTRL and TR_OUT_SEL register fields) should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out").

TCPWM0_GRP1_CNT8_CTRL: AUTO_RELOAD_LINE_SEL		
Field	**Rev 0E**	**Rev 0F**
F14Comment	Specifies switching of the LINE_SEL and LINE_BUFF_SEL values. This field has a function in PWM and PWM_PR modes. '0': never switch. '1': switch on a terminal count event with an actively pending switch event.	Specifies switching of the LINE_SEL and LINE_BUFF_SEL values. This field has a function in PWM and PWM_PR modes. '0': never switch. '1': switch on a terminal count event with and actively pending switch event.

TCPWM0_GRP1_CNT8_CTRL: AUTO_RELOAD_PERIOD		
Field	**Rev 0E**	**Rev 0F**
F15Comment	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with an actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with and actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.

TCPWM0_GRP1_CNT9_CTRL: ENABLED		
Field	**Rev 0E**	**Rev 0F**
F0Comment	Counter Enable '0': counter disabled. '1': counter enabled. Counter static configuration register fields should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out"). The following are Counter static configuration registers: CTRL (with the exception of DEBUG_FREEZE_EN bit), DT, TR_IN_SEL0, TR_IN_SEL1, TR_IN_EDGE_SEL, TR_PWM_CTRL_TR_OUT_SEL,INTR, INTR_MASK, INTR_MASKED Modifying these registers while the counter is running could produce unexcepted waveform results, but will not cause a fatal issue such as an illegal stop, lost control, or waveform stability issues.	Counter enable. '0': counter disabled. '1': counter enabled. Counter static configuration information (e.g. CTRL.MODE, all TR_IN_SEL, TR_IN_EDGE_SEL, TR_PWM_CTRL and TR_OUT_SEL register fields) should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out").

TCPWM0_GRP1_CNT9_CTRL: AUTO_RELOAD_LINE_SEL		
Field	**Rev 0E**	**Rev 0F**
F14Comment	Specifies switching of the LINE_SEL and LINE_BUFF_SEL values. This field has a function in PWM and PWM_PR modes. '0': never switch. '1': switch on a terminal count event with an actively pending switch event.	Specifies switching of the LINE_SEL and LINE_BUFF_SEL values. This field has a function in PWM and PWM_PR modes. '0': never switch. '1': switch on a terminal count event with and actively pending switch event.

TCPWM0_GRP1_CNT9_CTRL: AUTO_RELOAD_PERIOD		
Field	**Rev 0E**	**Rev 0F**
F15Comment	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with an actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with and actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.

TCPWM0_GRP1_CNT10_CTRL: ENABLED		
Field	**Rev 0E**	**Rev 0F**
F0Comment	Counter Enable '0': counter disabled. '1': counter enabled. Counter static configuration register fields should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out"). The following are Counter static configuration registers: CTRL (with the exception of DEBUG_FREEZE_EN bit), DT, TR_IN_SEL0, TR_IN_SEL1, TR_IN_EDGE_SEL, TR_PWM_CTRL_TR_OUT_SEL,INTR, INTR_MASK, INTR_MASKED Modifying these registers while the counter is running could produce unexcepted waveform results, but will not cause a fatal issue such as an illegal stop, lost control, or waveform stability issues.	Counter enable. '0': counter disabled. '1': counter enabled. Counter static configuration information (e.g. CTRL.MODE, all TR_IN_SEL, TR_IN_EDGE_SEL, TR_PWM_CTRL and TR_OUT_SEL register fields) should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out").

TCPWM0_GRP1_CNT10_CTRL: AUTO_RELOAD_LINE_SEL		
Field	**Rev 0E**	**Rev 0F**
F14Comment	Specifies switching of the LINE_SEL and LINE_BUFF_SEL values. This field has a function in PWM and PWM_PR modes. '0': never switch. '1': switch on a terminal count event with an actively pending switch event.	Specifies switching of the LINE_SEL and LINE_BUFF_SEL values. This field has a function in PWM and PWM_PR modes. '0': never switch. '1': switch on a terminal count event with and actively pending switch event.

TCPWM0_GRP1_CNT10_CTRL: AUTO_RELOAD_PERIOD		
Field	**Rev 0E**	**Rev 0F**
F15Comment	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with an actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with and actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.

TCPWM0_GRP1_CNT11_CTRL: ENABLED		
Field	**Rev 0E**	**Rev 0F**
F0Comment	Counter Enable '0': counter disabled. '1': counter enabled. Counter static configuration register fields should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out"). The following are Counter static configuration registers: CTRL (with the exception of DEBUG_FREEZE_EN bit), DT, TR_IN_SEL0, TR_IN_SEL1, TR_IN_EDGE_SEL, TR_PWM_CTRL_TR_OUT_SEL,INTR, INTR_MASK, INTR_MASKED Modifying these registers while the counter is running could produce unexcepted waveform results, but will not cause a fatal issue such as an illegal stop, lost control, or waveform stability issues.	Counter enable. '0': counter disabled. '1': counter enabled. Counter static configuration information (e.g. CTRL.MODE, all TR_IN_SEL, TR_IN_EDGE_SEL, TR_PWM_CTRL and TR_OUT_SEL register fields) should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out").

TCPWM0_GRP1_CNT11_CTRL: AUTO_RELOAD_LINE_SEL		
Field	**Rev 0E**	**Rev 0F**
F14Comment	Specifies switching of the LINE_SEL and LINE_BUFF_SEL values. This field has a function in PWM and PWM_PR modes. '0': never switch. '1': switch on a terminal count event with an actively pending switch event.	Specifies switching of the LINE_SEL and LINE_BUFF_SEL values. This field has a function in PWM and PWM_PR modes. '0': never switch. '1': switch on a terminal count event with and actively pending switch event.

TCPWM0_GRP1_CNT11_CTRL: AUTO_RELOAD_PERIOD		
Field	**Rev 0E**	**Rev 0F**
F15Comment	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with an actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with and actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.

TCPWM0_GRP2_CNT0_CTRL: ENABLED		
Field	**Rev 0E**	**Rev 0F**
F0Comment	Counter Enable '0': counter disabled. '1': counter enabled. Counter static configuration register fields should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out"). The following are Counter static configuration registers: CTRL (with the exception of DEBUG_FREEZE_EN bit), DT, TR_IN_SEL0, TR_IN_SEL1, TR_IN_EDGE_SEL, TR_PWM_CTRL_TR_OUT_SEL,INTR, INTR_MASK, INTR_MASKED Modifying these registers while the counter is running could produce unexcepted waveform results, but will not cause a fatal issue such as an illegal stop, lost control, or waveform stability issues.	Counter enable. '0': counter disabled. '1': counter enabled. Counter static configuration information (e.g. CTRL.MODE, all TR_IN_SEL, TR_IN_EDGE_SEL, TR_PWM_CTRL and TR_OUT_SEL register fields) should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out").

TCPWM0_GRP2_CNT0_CTRL: AUTO_RELOAD_PERIOD		
Field	**Rev 0E**	**Rev 0F**
F10Comment	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with an actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with and actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.

TCPWM0_GRP2_CNT1_CTRL: ENABLED		
Field	**Rev 0E**	**Rev 0F**
F0Comment	Counter Enable '0': counter disabled. '1': counter enabled. Counter static configuration register fields should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out"). The following are Counter static configuration registers: CTRL (with the exception of DEBUG_FREEZE_EN bit), DT, TR_IN_SEL0, TR_IN_SEL1, TR_IN_EDGE_SEL, TR_PWM_CTRL_TR_OUT_SEL,INTR, INTR_MASK, INTR_MASKED Modifying these registers while the counter is running could produce unexcepted waveform results, but will not cause a fatal issue such as an illegal stop, lost control, or waveform stability issues.	Counter enable. '0': counter disabled. '1': counter enabled. Counter static configuration information (e.g. CTRL.MODE, all TR_IN_SEL, TR_IN_EDGE_SEL, TR_PWM_CTRL and TR_OUT_SEL register fields) should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out").

TCPWM0_GRP2_CNT1_CTRL: AUTO_RELOAD_PERIOD		
Field	**Rev 0E**	**Rev 0F**
F10Comment	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with an actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with and actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.

TCPWM0_GRP2_CNT2_CTRL: ENABLED		
Field	**Rev 0E**	**Rev 0F**
F0Comment	Counter Enable '0': counter disabled. '1': counter enabled. Counter static configuration register fields should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out"). The following are Counter static configuration registers: CTRL (with the exception of DEBUG_FREEZE_EN bit), DT, TR_IN_SEL0, TR_IN_SEL1, TR_IN_EDGE_SEL, TR_PWM_CTRL_TR_OUT_SEL,INTR, INTR_MASK, INTR_MASKED Modifying these registers while the counter is running could produce unexcepted waveform results, but will not cause a fatal issue such as an illegal stop, lost control, or waveform stability issues.	Counter enable. '0': counter disabled. '1': counter enabled. Counter static configuration information (e.g. CTRL.MODE, all TR_IN_SEL, TR_IN_EDGE_SEL, TR_PWM_CTRL and TR_OUT_SEL register fields) should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out").

TCPWM0_GRP2_CNT2_CTRL: AUTO_RELOAD_PERIOD		
Field	**Rev 0E**	**Rev 0F**
F10Comment	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with an actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with and actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.

TCPWM0_GRP2_CNT3_CTRL: ENABLED		
Field	**Rev 0E**	**Rev 0F**
F0Comment	Counter Enable '0': counter disabled. '1': counter enabled. Counter static configuration register fields should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out"). The following are Counter static configuration registers: CTRL (with the exception of DEBUG_FREEZE_EN bit), DT, TR_IN_SEL0, TR_IN_SEL1, TR_IN_EDGE_SEL, TR_PWM_CTRL_TR_OUT_SEL,INTR, INTR_MASK, INTR_MASKED Modifying these registers while the counter is running could produce unexcepted waveform results, but will not cause a fatal issue such as an illegal stop, lost control, or waveform stability issues.	Counter enable. '0': counter disabled. '1': counter enabled. Counter static configuration information (e.g. CTRL.MODE, all TR_IN_SEL, TR_IN_EDGE_SEL, TR_PWM_CTRL and TR_OUT_SEL register fields) should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out").

TCPWM0_GRP2_CNT3_CTRL: AUTO_RELOAD_PERIOD		
Field	**Rev 0E**	**Rev 0F**
F10Comment	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with an actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with and actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.

TCPWM0_GRP2_CNT4_CTRL: ENABLED		
Field	**Rev 0E**	**Rev 0F**
F0Comment	Counter Enable '0': counter disabled. '1': counter enabled. Counter static configuration register fields should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out"). The following are Counter static configuration registers: CTRL (with the exception of DEBUG_FREEZE_EN bit), DT, TR_IN_SEL0, TR_IN_SEL1, TR_IN_EDGE_SEL, TR_PWM_CTRL_TR_OUT_SEL,INTR, INTR_MASK, INTR_MASKED Modifying these registers while the counter is running could produce unexcepted waveform results, but will not cause a fatal issue such as an illegal stop, lost control, or waveform stability issues.	Counter enable. '0': counter disabled. '1': counter enabled. Counter static configuration information (e.g. CTRL.MODE, all TR_IN_SEL, TR_IN_EDGE_SEL, TR_PWM_CTRL and TR_OUT_SEL register fields) should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out").

TCPWM0_GRP2_CNT4_CTRL: AUTO_RELOAD_PERIOD		
Field	**Rev 0E**	**Rev 0F**
F10Comment	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with an actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with and actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.

TCPWM0_GRP2_CNT5_CTRL: ENABLED		
Field	**Rev 0E**	**Rev 0F**
F0Comment	Counter Enable '0': counter disabled. '1': counter enabled. Counter static configuration register fields should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out"). The following are Counter static configuration registers: CTRL (with the exception of DEBUG_FREEZE_EN bit), DT, TR_IN_SEL0, TR_IN_SEL1, TR_IN_EDGE_SEL, TR_PWM_CTRL_TR_OUT_SEL,INTR, INTR_MASK, INTR_MASKED Modifying these registers while the counter is running could produce unexcepted waveform results, but will not cause a fatal issue such as an illegal stop, lost control, or waveform stability issues.	Counter enable. '0': counter disabled. '1': counter enabled. Counter static configuration information (e.g. CTRL.MODE, all TR_IN_SEL, TR_IN_EDGE_SEL, TR_PWM_CTRL and TR_OUT_SEL register fields) should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out").

TCPWM0_GRP2_CNT5_CTRL: AUTO_RELOAD_PERIOD		
Field	**Rev 0E**	**Rev 0F**
F10Comment	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with an actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with and actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.

TCPWM0_GRP2_CNT6_CTRL: ENABLED		
Field	**Rev 0E**	**Rev 0F**
F0Comment	Counter Enable '0': counter disabled. '1': counter enabled. Counter static configuration register fields should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out"). The following are Counter static configuration registers: CTRL (with the exception of DEBUG_FREEZE_EN bit), DT, TR_IN_SEL0, TR_IN_SEL1, TR_IN_EDGE_SEL, TR_PWM_CTRL_TR_OUT_SEL,INTR, INTR_MASK, INTR_MASKED Modifying these registers while the counter is running could produce unexcepted waveform results, but will not cause a fatal issue such as an illegal stop, lost control, or waveform stability issues.	Counter enable. '0': counter disabled. '1': counter enabled. Counter static configuration information (e.g. CTRL.MODE, all TR_IN_SEL, TR_IN_EDGE_SEL, TR_PWM_CTRL and TR_OUT_SEL register fields) should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out").

TCPWM0_GRP2_CNT6_CTRL: AUTO_RELOAD_PERIOD		
Field	**Rev 0E**	**Rev 0F**
F10Comment	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with an actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with and actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.

TCPWM0_GRP2_CNT7_CTRL: ENABLED		
Field	**Rev 0E**	**Rev 0F**
F0Comment	Counter Enable '0': counter disabled. '1': counter enabled. Counter static configuration register fields should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out"). The following are Counter static configuration registers: CTRL (with the exception of DEBUG_FREEZE_EN bit), DT, TR_IN_SEL0, TR_IN_SEL1, TR_IN_EDGE_SEL, TR_PWM_CTRL_TR_OUT_SEL,INTR, INTR_MASK, INTR_MASKED Modifying these registers while the counter is running could produce unexcepted waveform results, but will not cause a fatal issue such as an illegal stop, lost control, or waveform stability issues.	Counter enable. '0': counter disabled. '1': counter enabled. Counter static configuration information (e.g. CTRL.MODE, all TR_IN_SEL, TR_IN_EDGE_SEL, TR_PWM_CTRL and TR_OUT_SEL register fields) should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out").

TCPWM0_GRP2_CNT7_CTRL: AUTO_RELOAD_PERIOD		
Field	**Rev 0E**	**Rev 0F**
F10Comment	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with an actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with and actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.

TCPWM0_GRP2_CNT8_CTRL: ENABLED		
Field	**Rev 0E**	**Rev 0F**
F0Comment	Counter Enable '0': counter disabled. '1': counter enabled. Counter static configuration register fields should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out"). The following are Counter static configuration registers: CTRL (with the exception of DEBUG_FREEZE_EN bit), DT, TR_IN_SEL0, TR_IN_SEL1, TR_IN_EDGE_SEL, TR_PWM_CTRL_TR_OUT_SEL,INTR, INTR_MASK, INTR_MASKED Modifying these registers while the counter is running could produce unexcepted waveform results, but will not cause a fatal issue such as an illegal stop, lost control, or waveform stability issues.	Counter enable. '0': counter disabled. '1': counter enabled. Counter static configuration information (e.g. CTRL.MODE, all TR_IN_SEL, TR_IN_EDGE_SEL, TR_PWM_CTRL and TR_OUT_SEL register fields) should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out").

TCPWM0_GRP2_CNT8_CTRL: AUTO_RELOAD_PERIOD		
Field	**Rev 0E**	**Rev 0F**
F10Comment	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with an actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with and actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.

TCPWM0_GRP2_CNT9_CTRL: ENABLED		
Field	**Rev 0E**	**Rev 0F**
F0Comment	Counter Enable '0': counter disabled. '1': counter enabled. Counter static configuration register fields should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out"). The following are Counter static configuration registers: CTRL (with the exception of DEBUG_FREEZE_EN bit), DT, TR_IN_SEL0, TR_IN_SEL1, TR_IN_EDGE_SEL, TR_PWM_CTRL_TR_OUT_SEL,INTR, INTR_MASK, INTR_MASKED Modifying these registers while the counter is running could produce unexcepted waveform results, but will not cause a fatal issue such as an illegal stop, lost control, or waveform stability issues.	Counter enable. '0': counter disabled. '1': counter enabled. Counter static configuration information (e.g. CTRL.MODE, all TR_IN_SEL, TR_IN_EDGE_SEL, TR_PWM_CTRL and TR_OUT_SEL register fields) should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out").

TCPWM0_GRP2_CNT9_CTRL: AUTO_RELOAD_PERIOD		
Field	**Rev 0E**	**Rev 0F**
F10Comment	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with an actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with and actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.

TCPWM0_GRP2_CNT10_CTRL: ENABLED		
Field	**Rev 0E**	**Rev 0F**
F0Comment	Counter Enable '0': counter disabled. '1': counter enabled. Counter static configuration register fields should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out"). The following are Counter static configuration registers: CTRL (with the exception of DEBUG_FREEZE_EN bit), DT, TR_IN_SEL0, TR_IN_SEL1, TR_IN_EDGE_SEL, TR_PWM_CTRL_TR_OUT_SEL,INTR, INTR_MASK, INTR_MASKED Modifying these registers while the counter is running could produce unexcepted waveform results, but will not cause a fatal issue such as an illegal stop, lost control, or waveform stability issues.	Counter enable. '0': counter disabled. '1': counter enabled. Counter static configuration information (e.g. CTRL.MODE, all TR_IN_SEL, TR_IN_EDGE_SEL, TR_PWM_CTRL and TR_OUT_SEL register fields) should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out").

TCPWM0_GRP2_CNT10_CTRL: AUTO_RELOAD_PERIOD		
Field	**Rev 0E**	**Rev 0F**
F10Comment	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with an actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with and actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.

TCPWM0_GRP2_CNT11_CTRL: ENABLED		
Field	**Rev 0E**	**Rev 0F**
F0Comment	Counter Enable '0': counter disabled. '1': counter enabled. Counter static configuration register fields should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out"). The following are Counter static configuration registers: CTRL (with the exception of DEBUG_FREEZE_EN bit), DT, TR_IN_SEL0, TR_IN_SEL1, TR_IN_EDGE_SEL, TR_PWM_CTRL_TR_OUT_SEL,INTR, INTR_MASK, INTR_MASKED Modifying these registers while the counter is running could produce unexcepted waveform results, but will not cause a fatal issue such as an illegal stop, lost control, or waveform stability issues.	Counter enable. '0': counter disabled. '1': counter enabled. Counter static configuration information (e.g. CTRL.MODE, all TR_IN_SEL, TR_IN_EDGE_SEL, TR_PWM_CTRL and TR_OUT_SEL register fields) should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out").

TCPWM0_GRP2_CNT11_CTRL: AUTO_RELOAD_PERIOD		
Field	**Rev 0E**	**Rev 0F**
F10Comment	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with an actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with and actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.

TCPWM0_GRP2_CNT12_CTRL: ENABLED		
Field	**Rev 0E**	**Rev 0F**
F0Comment	Counter Enable '0': counter disabled. '1': counter enabled. Counter static configuration register fields should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out"). The following are Counter static configuration registers: CTRL (with the exception of DEBUG_FREEZE_EN bit), DT, TR_IN_SEL0, TR_IN_SEL1, TR_IN_EDGE_SEL, TR_PWM_CTRL_TR_OUT_SEL,INTR, INTR_MASK, INTR_MASKED Modifying these registers while the counter is running could produce unexcepted waveform results, but will not cause a fatal issue such as an illegal stop, lost control, or waveform stability issues.	Counter enable. '0': counter disabled. '1': counter enabled. Counter static configuration information (e.g. CTRL.MODE, all TR_IN_SEL, TR_IN_EDGE_SEL, TR_PWM_CTRL and TR_OUT_SEL register fields) should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out").

TCPWM0_GRP2_CNT12_CTRL: AUTO_RELOAD_PERIOD		
Field	**Rev 0E**	**Rev 0F**
F10Comment	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with an actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with and actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.

TCPWM0_GRP2_CNT13_CTRL: ENABLED		
Field	**Rev 0E**	**Rev 0F**
F0Comment	Counter Enable '0': counter disabled. '1': counter enabled. Counter static configuration register fields should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out"). The following are Counter static configuration registers: CTRL (with the exception of DEBUG_FREEZE_EN bit), DT, TR_IN_SEL0, TR_IN_SEL1, TR_IN_EDGE_SEL, TR_PWM_CTRL_TR_OUT_SEL,INTR, INTR_MASK, INTR_MASKED Modifying these registers while the counter is running could produce unexcepted waveform results, but will not cause a fatal issue such as an illegal stop, lost control, or waveform stability issues.	Counter enable. '0': counter disabled. '1': counter enabled. Counter static configuration information (e.g. CTRL.MODE, all TR_IN_SEL, TR_IN_EDGE_SEL, TR_PWM_CTRL and TR_OUT_SEL register fields) should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out").

TCPWM0_GRP2_CNT13_CTRL: AUTO_RELOAD_PERIOD		
Field	**Rev 0E**	**Rev 0F**
F10Comment	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with an actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with and actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.

TCPWM0_GRP2_CNT14_CTRL: ENABLED		
Field	**Rev 0E**	**Rev 0F**
F0Comment	Counter Enable '0': counter disabled. '1': counter enabled. Counter static configuration register fields should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out"). The following are Counter static configuration registers: CTRL (with the exception of DEBUG_FREEZE_EN bit), DT, TR_IN_SEL0, TR_IN_SEL1, TR_IN_EDGE_SEL, TR_PWM_CTRL_TR_OUT_SEL,INTR, INTR_MASK, INTR_MASKED Modifying these registers while the counter is running could produce unexcepted waveform results, but will not cause a fatal issue such as an illegal stop, lost control, or waveform stability issues.	Counter enable. '0': counter disabled. '1': counter enabled. Counter static configuration information (e.g. CTRL.MODE, all TR_IN_SEL, TR_IN_EDGE_SEL, TR_PWM_CTRL and TR_OUT_SEL register fields) should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out").

TCPWM0_GRP2_CNT14_CTRL: AUTO_RELOAD_PERIOD		
Field	**Rev 0E**	**Rev 0F**
F10Comment	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with an actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with and actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.

TCPWM0_GRP2_CNT15_CTRL: ENABLED		
Field	**Rev 0E**	**Rev 0F**
F0Comment	Counter Enable '0': counter disabled. '1': counter enabled. Counter static configuration register fields should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out"). The following are Counter static configuration registers: CTRL (with the exception of DEBUG_FREEZE_EN bit), DT, TR_IN_SEL0, TR_IN_SEL1, TR_IN_EDGE_SEL, TR_PWM_CTRL_TR_OUT_SEL,INTR, INTR_MASK, INTR_MASKED Modifying these registers while the counter is running could produce unexcepted waveform results, but will not cause a fatal issue such as an illegal stop, lost control, or waveform stability issues.	Counter enable. '0': counter disabled. '1': counter enabled. Counter static configuration information (e.g. CTRL.MODE, all TR_IN_SEL, TR_IN_EDGE_SEL, TR_PWM_CTRL and TR_OUT_SEL register fields) should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out").

TCPWM0_GRP2_CNT15_CTRL: AUTO_RELOAD_PERIOD		
Field	**Rev 0E**	**Rev 0F**
F10Comment	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with an actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with and actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.

TCPWM0_GRP2_CNT16_CTRL: ENABLED		
Field	**Rev 0E**	**Rev 0F**
F0Comment	Counter Enable '0': counter disabled. '1': counter enabled. Counter static configuration register fields should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out"). The following are Counter static configuration registers: CTRL (with the exception of DEBUG_FREEZE_EN bit), DT, TR_IN_SEL0, TR_IN_SEL1, TR_IN_EDGE_SEL, TR_PWM_CTRL_TR_OUT_SEL,INTR, INTR_MASK, INTR_MASKED Modifying these registers while the counter is running could produce unexcepted waveform results, but will not cause a fatal issue such as an illegal stop, lost control, or waveform stability issues.	Counter enable. '0': counter disabled. '1': counter enabled. Counter static configuration information (e.g. CTRL.MODE, all TR_IN_SEL, TR_IN_EDGE_SEL, TR_PWM_CTRL and TR_OUT_SEL register fields) should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out").

TCPWM0_GRP2_CNT16_CTRL: AUTO_RELOAD_PERIOD		
Field	**Rev 0E**	**Rev 0F**
F10Comment	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with an actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with and actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.

TCPWM0_GRP2_CNT17_CTRL: ENABLED		
Field	**Rev 0E**	**Rev 0F**
F0Comment	Counter Enable '0': counter disabled. '1': counter enabled. Counter static configuration register fields should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out"). The following are Counter static configuration registers: CTRL (with the exception of DEBUG_FREEZE_EN bit), DT, TR_IN_SEL0, TR_IN_SEL1, TR_IN_EDGE_SEL, TR_PWM_CTRL_TR_OUT_SEL,INTR, INTR_MASK, INTR_MASKED Modifying these registers while the counter is running could produce unexcepted waveform results, but will not cause a fatal issue such as an illegal stop, lost control, or waveform stability issues.	Counter enable. '0': counter disabled. '1': counter enabled. Counter static configuration information (e.g. CTRL.MODE, all TR_IN_SEL, TR_IN_EDGE_SEL, TR_PWM_CTRL and TR_OUT_SEL register fields) should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out").

TCPWM0_GRP2_CNT17_CTRL: AUTO_RELOAD_PERIOD		
Field	**Rev 0E**	**Rev 0F**
F10Comment	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with an actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with and actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.

TCPWM0_GRP2_CNT18_CTRL: ENABLED		
Field	**Rev 0E**	**Rev 0F**
F0Comment	Counter Enable '0': counter disabled. '1': counter enabled. Counter static configuration register fields should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out"). The following are Counter static configuration registers: CTRL (with the exception of DEBUG_FREEZE_EN bit), DT, TR_IN_SEL0, TR_IN_SEL1, TR_IN_EDGE_SEL, TR_PWM_CTRL_TR_OUT_SEL,INTR, INTR_MASK, INTR_MASKED Modifying these registers while the counter is running could produce unexcepted waveform results, but will not cause a fatal issue such as an illegal stop, lost control, or waveform stability issues.	Counter enable. '0': counter disabled. '1': counter enabled. Counter static configuration information (e.g. CTRL.MODE, all TR_IN_SEL, TR_IN_EDGE_SEL, TR_PWM_CTRL and TR_OUT_SEL register fields) should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out").

TCPWM0_GRP2_CNT18_CTRL: AUTO_RELOAD_PERIOD		
Field	**Rev 0E**	**Rev 0F**
F10Comment	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with an actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with and actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.

TCPWM0_GRP2_CNT19_CTRL: ENABLED		
Field	**Rev 0E**	**Rev 0F**
F0Comment	Counter Enable '0': counter disabled. '1': counter enabled. Counter static configuration register fields should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out"). The following are Counter static configuration registers: CTRL (with the exception of DEBUG_FREEZE_EN bit), DT, TR_IN_SEL0, TR_IN_SEL1, TR_IN_EDGE_SEL, TR_PWM_CTRL_TR_OUT_SEL,INTR, INTR_MASK, INTR_MASKED Modifying these registers while the counter is running could produce unexcepted waveform results, but will not cause a fatal issue such as an illegal stop, lost control, or waveform stability issues.	Counter enable. '0': counter disabled. '1': counter enabled. Counter static configuration information (e.g. CTRL.MODE, all TR_IN_SEL, TR_IN_EDGE_SEL, TR_PWM_CTRL and TR_OUT_SEL register fields) should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out").

TCPWM0_GRP2_CNT19_CTRL: AUTO_RELOAD_PERIOD		
Field	**Rev 0E**	**Rev 0F**
F10Comment	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with an actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with and actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.

TCPWM0_GRP2_CNT20_CTRL: ENABLED		
Field	**Rev 0E**	**Rev 0F**
F0Comment	Counter Enable '0': counter disabled. '1': counter enabled. Counter static configuration register fields should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out"). The following are Counter static configuration registers: CTRL (with the exception of DEBUG_FREEZE_EN bit), DT, TR_IN_SEL0, TR_IN_SEL1, TR_IN_EDGE_SEL, TR_PWM_CTRL_TR_OUT_SEL,INTR, INTR_MASK, INTR_MASKED Modifying these registers while the counter is running could produce unexcepted waveform results, but will not cause a fatal issue such as an illegal stop, lost control, or waveform stability issues.	Counter enable. '0': counter disabled. '1': counter enabled. Counter static configuration information (e.g. CTRL.MODE, all TR_IN_SEL, TR_IN_EDGE_SEL, TR_PWM_CTRL and TR_OUT_SEL register fields) should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out").

TCPWM0_GRP2_CNT20_CTRL: AUTO_RELOAD_PERIOD		
Field	**Rev 0E**	**Rev 0F**
F10Comment	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with an actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with and actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.

TCPWM0_GRP2_CNT21_CTRL: ENABLED		
Field	**Rev 0E**	**Rev 0F**
F0Comment	Counter Enable '0': counter disabled. '1': counter enabled. Counter static configuration register fields should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out"). The following are Counter static configuration registers: CTRL (with the exception of DEBUG_FREEZE_EN bit), DT, TR_IN_SEL0, TR_IN_SEL1, TR_IN_EDGE_SEL, TR_PWM_CTRL_TR_OUT_SEL,INTR, INTR_MASK, INTR_MASKED Modifying these registers while the counter is running could produce unexcepted waveform results, but will not cause a fatal issue such as an illegal stop, lost control, or waveform stability issues.	Counter enable. '0': counter disabled. '1': counter enabled. Counter static configuration information (e.g. CTRL.MODE, all TR_IN_SEL, TR_IN_EDGE_SEL, TR_PWM_CTRL and TR_OUT_SEL register fields) should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out").

TCPWM0_GRP2_CNT21_CTRL: AUTO_RELOAD_PERIOD		
Field	**Rev 0E**	**Rev 0F**
F10Comment	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with an actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with and actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.

TCPWM0_GRP2_CNT22_CTRL: ENABLED		
Field	**Rev 0E**	**Rev 0F**
F0Comment	Counter Enable '0': counter disabled. '1': counter enabled. Counter static configuration register fields should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out"). The following are Counter static configuration registers: CTRL (with the exception of DEBUG_FREEZE_EN bit), DT, TR_IN_SEL0, TR_IN_SEL1, TR_IN_EDGE_SEL, TR_PWM_CTRL_TR_OUT_SEL,INTR, INTR_MASK, INTR_MASKED Modifying these registers while the counter is running could produce unexcepted waveform results, but will not cause a fatal issue such as an illegal stop, lost control, or waveform stability issues.	Counter enable. '0': counter disabled. '1': counter enabled. Counter static configuration information (e.g. CTRL.MODE, all TR_IN_SEL, TR_IN_EDGE_SEL, TR_PWM_CTRL and TR_OUT_SEL register fields) should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out").

TCPWM0_GRP2_CNT22_CTRL: AUTO_RELOAD_PERIOD		
Field	**Rev 0E**	**Rev 0F**
F10Comment	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with an actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with and actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.

TCPWM0_GRP2_CNT23_CTRL: ENABLED		
Field	**Rev 0E**	**Rev 0F**
F0Comment	Counter Enable '0': counter disabled. '1': counter enabled. Counter static configuration register fields should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out"). The following are Counter static configuration registers: CTRL (with the exception of DEBUG_FREEZE_EN bit), DT, TR_IN_SEL0, TR_IN_SEL1, TR_IN_EDGE_SEL, TR_PWM_CTRL_TR_OUT_SEL,INTR, INTR_MASK, INTR_MASKED Modifying these registers while the counter is running could produce unexcepted waveform results, but will not cause a fatal issue such as an illegal stop, lost control, or waveform stability issues.	Counter enable. '0': counter disabled. '1': counter enabled. Counter static configuration information (e.g. CTRL.MODE, all TR_IN_SEL, TR_IN_EDGE_SEL, TR_PWM_CTRL and TR_OUT_SEL register fields) should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out").

TCPWM0_GRP2_CNT23_CTRL: AUTO_RELOAD_PERIOD		
Field	**Rev 0E**	**Rev 0F**
F10Comment	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with an actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with and actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.

TCPWM0_GRP2_CNT24_CTRL: ENABLED		
Field	**Rev 0E**	**Rev 0F**
F0Comment	Counter Enable '0': counter disabled. '1': counter enabled. Counter static configuration register fields should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out"). The following are Counter static configuration registers: CTRL (with the exception of DEBUG_FREEZE_EN bit), DT, TR_IN_SEL0, TR_IN_SEL1, TR_IN_EDGE_SEL, TR_PWM_CTRL_TR_OUT_SEL,INTR, INTR_MASK, INTR_MASKED Modifying these registers while the counter is running could produce unexcepted waveform results, but will not cause a fatal issue such as an illegal stop, lost control, or waveform stability issues.	Counter enable. '0': counter disabled. '1': counter enabled. Counter static configuration information (e.g. CTRL.MODE, all TR_IN_SEL, TR_IN_EDGE_SEL, TR_PWM_CTRL and TR_OUT_SEL register fields) should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out").

TCPWM0_GRP2_CNT24_CTRL: AUTO_RELOAD_PERIOD		
Field	**Rev 0E**	**Rev 0F**
F10Comment	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with an actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with and actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.

TCPWM0_GRP2_CNT25_CTRL: ENABLED		
Field	**Rev 0E**	**Rev 0F**
F0Comment	Counter Enable '0': counter disabled. '1': counter enabled. Counter static configuration register fields should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out"). The following are Counter static configuration registers: CTRL (with the exception of DEBUG_FREEZE_EN bit), DT, TR_IN_SEL0, TR_IN_SEL1, TR_IN_EDGE_SEL, TR_PWM_CTRL_TR_OUT_SEL,INTR, INTR_MASK, INTR_MASKED Modifying these registers while the counter is running could produce unexcepted waveform results, but will not cause a fatal issue such as an illegal stop, lost control, or waveform stability issues.	Counter enable. '0': counter disabled. '1': counter enabled. Counter static configuration information (e.g. CTRL.MODE, all TR_IN_SEL, TR_IN_EDGE_SEL, TR_PWM_CTRL and TR_OUT_SEL register fields) should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out").

TCPWM0_GRP2_CNT25_CTRL: AUTO_RELOAD_PERIOD		
Field	**Rev 0E**	**Rev 0F**
F10Comment	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with an actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with and actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.

TCPWM0_GRP2_CNT26_CTRL: ENABLED		
Field	**Rev 0E**	**Rev 0F**
F0Comment	Counter Enable '0': counter disabled. '1': counter enabled. Counter static configuration register fields should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out"). The following are Counter static configuration registers: CTRL (with the exception of DEBUG_FREEZE_EN bit), DT, TR_IN_SEL0, TR_IN_SEL1, TR_IN_EDGE_SEL, TR_PWM_CTRL_TR_OUT_SEL,INTR, INTR_MASK, INTR_MASKED Modifying these registers while the counter is running could produce unexcepted waveform results, but will not cause a fatal issue such as an illegal stop, lost control, or waveform stability issues.	Counter enable. '0': counter disabled. '1': counter enabled. Counter static configuration information (e.g. CTRL.MODE, all TR_IN_SEL, TR_IN_EDGE_SEL, TR_PWM_CTRL and TR_OUT_SEL register fields) should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out").

TCPWM0_GRP2_CNT26_CTRL: AUTO_RELOAD_PERIOD		
Field	**Rev 0E**	**Rev 0F**
F10Comment	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with an actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with and actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.

TCPWM0_GRP2_CNT27_CTRL: ENABLED		
Field	**Rev 0E**	**Rev 0F**
F0Comment	Counter Enable '0': counter disabled. '1': counter enabled. Counter static configuration register fields should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out"). The following are Counter static configuration registers: CTRL (with the exception of DEBUG_FREEZE_EN bit), DT, TR_IN_SEL0, TR_IN_SEL1, TR_IN_EDGE_SEL, TR_PWM_CTRL_TR_OUT_SEL,INTR, INTR_MASK, INTR_MASKED Modifying these registers while the counter is running could produce unexcepted waveform results, but will not cause a fatal issue such as an illegal stop, lost control, or waveform stability issues.	Counter enable. '0': counter disabled. '1': counter enabled. Counter static configuration information (e.g. CTRL.MODE, all TR_IN_SEL, TR_IN_EDGE_SEL, TR_PWM_CTRL and TR_OUT_SEL register fields) should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out").

TCPWM0_GRP2_CNT27_CTRL: AUTO_RELOAD_PERIOD		
Field	**Rev 0E**	**Rev 0F**
F10Comment	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with an actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with and actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.

TCPWM0_GRP2_CNT28_CTRL: ENABLED		
Field	**Rev 0E**	**Rev 0F**
F0Comment	Counter Enable '0': counter disabled. '1': counter enabled. Counter static configuration register fields should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out"). The following are Counter static configuration registers: CTRL (with the exception of DEBUG_FREEZE_EN bit), DT, TR_IN_SEL0, TR_IN_SEL1, TR_IN_EDGE_SEL, TR_PWM_CTRL_TR_OUT_SEL,INTR, INTR_MASK, INTR_MASKED Modifying these registers while the counter is running could produce unexcepted waveform results, but will not cause a fatal issue such as an illegal stop, lost control, or waveform stability issues.	Counter enable. '0': counter disabled. '1': counter enabled. Counter static configuration information (e.g. CTRL.MODE, all TR_IN_SEL, TR_IN_EDGE_SEL, TR_PWM_CTRL and TR_OUT_SEL register fields) should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out").

TCPWM0_GRP2_CNT28_CTRL: AUTO_RELOAD_PERIOD		
Field	**Rev 0E**	**Rev 0F**
F10Comment	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with an actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with and actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.

TCPWM0_GRP2_CNT29_CTRL: ENABLED		
Field	**Rev 0E**	**Rev 0F**
F0Comment	Counter Enable '0': counter disabled. '1': counter enabled. Counter static configuration register fields should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out"). The following are Counter static configuration registers: CTRL (with the exception of DEBUG_FREEZE_EN bit), DT, TR_IN_SEL0, TR_IN_SEL1, TR_IN_EDGE_SEL, TR_PWM_CTRL_TR_OUT_SEL,INTR, INTR_MASK, INTR_MASKED Modifying these registers while the counter is running could produce unexcepted waveform results, but will not cause a fatal issue such as an illegal stop, lost control, or waveform stability issues.	Counter enable. '0': counter disabled. '1': counter enabled. Counter static configuration information (e.g. CTRL.MODE, all TR_IN_SEL, TR_IN_EDGE_SEL, TR_PWM_CTRL and TR_OUT_SEL register fields) should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out").

TCPWM0_GRP2_CNT29_CTRL: AUTO_RELOAD_PERIOD		
Field	**Rev 0E**	**Rev 0F**
F10Comment	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with an actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with and actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.

TCPWM0_GRP2_CNT30_CTRL: ENABLED		
Field	**Rev 0E**	**Rev 0F**
F0Comment	Counter Enable '0': counter disabled. '1': counter enabled. Counter static configuration register fields should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out"). The following are Counter static configuration registers: CTRL (with the exception of DEBUG_FREEZE_EN bit), DT, TR_IN_SEL0, TR_IN_SEL1, TR_IN_EDGE_SEL, TR_PWM_CTRL_TR_OUT_SEL,INTR, INTR_MASK, INTR_MASKED Modifying these registers while the counter is running could produce unexcepted waveform results, but will not cause a fatal issue such as an illegal stop, lost control, or waveform stability issues.	Counter enable. '0': counter disabled. '1': counter enabled. Counter static configuration information (e.g. CTRL.MODE, all TR_IN_SEL, TR_IN_EDGE_SEL, TR_PWM_CTRL and TR_OUT_SEL register fields) should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out").

TCPWM0_GRP2_CNT30_CTRL: AUTO_RELOAD_PERIOD		
Field	**Rev 0E**	**Rev 0F**
F10Comment	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with an actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with and actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.

TCPWM0_GRP2_CNT31_CTRL: ENABLED		
Field	**Rev 0E**	**Rev 0F**
F0Comment	Counter Enable '0': counter disabled. '1': counter enabled. Counter static configuration register fields should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out"). The following are Counter static configuration registers: CTRL (with the exception of DEBUG_FREEZE_EN bit), DT, TR_IN_SEL0, TR_IN_SEL1, TR_IN_EDGE_SEL, TR_PWM_CTRL_TR_OUT_SEL,INTR, INTR_MASK, INTR_MASKED Modifying these registers while the counter is running could produce unexcepted waveform results, but will not cause a fatal issue such as an illegal stop, lost control, or waveform stability issues.	Counter enable. '0': counter disabled. '1': counter enabled. Counter static configuration information (e.g. CTRL.MODE, all TR_IN_SEL, TR_IN_EDGE_SEL, TR_PWM_CTRL and TR_OUT_SEL register fields) should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out").

TCPWM0_GRP2_CNT31_CTRL: AUTO_RELOAD_PERIOD		
Field	**Rev 0E**	**Rev 0F**
F10Comment	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with an actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with and actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff.

CXPI0_CH0_CTL0:		
Field	**Rev 0E**	**Rev 0F**
F5Name	FILTER_EN	PRESAMPLE_EN

CXPI0_CH0_CTL0: PRESAMPLE_EN		
Field	**Rev 0E**	**Rev 0F**
F5LoBit	8	9

CXPI0_CH0_CTL0: PRESAMPLE_EN		
Field	**Rev 0E**	**Rev 0F**
F5HiBit	8	9

CXPI0_CH0_CTL0: PRESAMPLE_EN		
Field	**Rev 0E**	**Rev 0F**
F5Comment	RX filter enable (for "cxpi_rx_in") '0': No filter '1': Median 3 (default value) operates on the last three "cxpi_rx_in" values. The sequences '000', '001', '010', and '100' result in a filtered value '0'. The sequences '111', '110', '101', and '011' result in a filtered value '1'.	Pre-sample enable for PWM mode. '0': Disbaled. '1': Enabled When sampling counter's value is greater than CTL1.T_LOW1, pre-sample FF will be set to "1" as long as detecting any "1" on "cxpi_rx_in" and be cleared to "0" after sampling moment. At the sampling moment, if pre-sample FF or "cxpi_rx_in" is "1", sample value will be "1", otherwise "0".

CXPI0_CH0_CTL0:		
Field	**Rev 0E**	**Rev 0F**
F6Name	RXPIDZERO_CHECK_EN	FILTER_EN

CXPI0_CH0_CTL0: FILTER_EN		
Field	**Rev 0E**	**Rev 0F**
F6LoBit	7	8

CXPI0_CH0_CTL0: FILTER_EN		
Field	**Rev 0E**	**Rev 0F**
F6HiBit	7	8

CXPI0_CH0_CTL0: FILTER_EN		
Field	**Rev 0E**	**Rev 0F**
F6Comment	Receive PID Zero Check Enable. 0 - No action if received PID[6:0] = 0 and PID[7]=1'b1. 1 - If received PID[6:0] = 0 and PID[7]=1'b1, HW (slave) does not clear CMD.RX_HEADER and will anticipate receiving header again (CMD.TX_HEADER=0). If CMD.TX_HEADER=1 in the same scenario, then HW (slave) clears CMD.RX_HEADER upon receiving the header follow by transmit PID. This mode is useful for case where polling method is used and CXPI controller is configured as slave. This would reduce dependency on SW to react to the header received within IBS=1.	RX filter enable (for "cxpi_rx_in") '0': No filter '1': Median 3 (default value) operates on the last three "cxpi_rx_in" values. The sequences '000', '001', '010', and '100' result in a filtered value '0'. The sequences '111', '110', '101', and '011' result in a filtered value '1'.

CXPI0_CH0_CTL0:		
Field	**Rev 0E**	**Rev 0F**
F7Name	AUTO_EN	RXPIDZERO_CHECK_EN

CXPI0_CH0_CTL0: RXPIDZERO_CHECK_EN		
Field	**Rev 0E**	**Rev 0F**
F7LoBit	4	7

CXPI0_CH0_CTL0: RXPIDZERO_CHECK_EN		
Field	**Rev 0E**	**Rev 0F**
F7HiBit	4	7

CXPI0_CH0_CTL0: RXPIDZERO_CHECK_EN		
Field	**Rev 0E**	**Rev 0F**
F7Comment	CXPI transceiver auto enable: '0': Disabled. '1': Enabled. The TX_RX_STATUS.EN_OUT field is controlled by HW.	Receive PID Zero Check Enable. 0 - No action if received PID[6:0] = 0 and PID[7]=1'b1. 1 - If received PID[6:0] = 0 and PID[7]=1'b1, HW (slave) does not clear CMD.RX_HEADER and will anticipate receiving header again (CMD.TX_HEADER=0). If CMD.TX_HEADER=1 in the same scenario, then HW (slave) clears CMD.RX_HEADER upon receiving the header follow by transmit PID. This mode is useful for case where polling method is used and CXPI controller is configured as slave. This would reduce dependency on SW to react to the header received within IBS=1.

CXPI0_CH0_CTL0: RXPIDZERO_CHECK_EN		
Field	**Rev 0E**	**Rev 0F**
F7DefaultVal	1	0

CXPI0_CH0_CTL0:		
Field	**Rev 0E**	**Rev 0F**
F8Name	MODE	AUTO_EN

CXPI0_CH0_CTL0: AUTO_EN		
Field	**Rev 0E**	**Rev 0F**
F8LoBit	0	4

CXPI0_CH0_CTL0: AUTO_EN		
Field	**Rev 0E**	**Rev 0F**
F8HiBit	0	4

CXPI0_CH0_CTL0: AUTO_EN		
Field	**Rev 0E**	**Rev 0F**
F8Comment	Mode of operation: '0': NRZ mode. '1': PWM mode.	CXPI transceiver auto enable: '0': Disabled. '1': Enabled. The TX_RX_STATUS.EN_OUT field is controlled by HW.

CXPI0_CH0_CTL0: AUTO_EN		
Field	**Rev 0E**	**Rev 0F**
F8DefaultVal	0	1

CXPI0_CH0_CTL0: : F9Name: Newly Added

CXPI0_CH0_CTL0: MODE: F9LoBit: Newly Added

CXPI0_CH0_CTL0: MODE: F9HiBit: Newly Added

CXPI0_CH0_CTL0: MODE: F9SW: Newly Added

CXPI0_CH0_CTL0: MODE: F9HW: Newly Added

CXPI0_CH0_CTL0: MODE: F9Comment: Newly Added

CXPI0_CH0_CTL0: MODE: F9DefaultVal: Newly Added

CXPI0_CH0_CTL1: T_LOW1		
Field	**Rev 0E**	**Rev 0F**
F2Comment	Low count for logic 1. This is valid only for PWM mode. The count value here indicates the number of clocks per clk_cxpi_ch to drive a '0' at CXPI bus before releasing it to indicate a logical '1'. 0: means 1 clock. 1: means 2 clocks .. 15: means 16 clocks. .. 399: means 400 clocks. Any value above 399 is invalid. Note that for NRZ mode, this field is ignored. Note that this field is used for TX.	Low count for logic 1. This is valid only for PWM mode. For master node, The count value here indicates the number of clocks per clk_cxpi_ch to drive a '0' at CXPI bus before releasing it to indicate a logical '1'. For slave node and pre-sample enabled, the count value indicates the number of clocks per clk_cxpi_ch to disable pre-sampling. 0: means 1 clock. 1: means 2 clocks .. 15: means 16 clocks. .. 399: means 400 clocks. Any value above 399 is invalid. Note that for NRZ mode, this field is ignored. Note that it must be set less than CTL1.T_OFFSET for slave node if pre-sample mode enabled. Note that it is also effective for pre-sample mode of master node.

CXPI0_CH0_CTL2:		
Field	**Rev 0E**	**Rev 0F**
F1Name	TIMEOUT_LENGTH	RXTX_DELAY

CXPI0_CH0_CTL2: RXTX_DELAY		
Field	**Rev 0E**	**Rev 0F**
F1LoBit	16	22

CXPI0_CH0_CTL2: RXTX_DELAY		
Field	**Rev 0E**	**Rev 0F**
F1HiBit	19	29

CXPI0_CH0_CTL2: RXTX_DELAY		
Field	**Rev 0E**	**Rev 0F**
F1Comment	Timeout Length (in Tbits). Specifies the number of Tbits to exceed timeout between frame bytes within a message frame. CXPI spec states that the maximum allowed inter byte space (IBS) is 9Tbits. This field is valid only when TIMEOUT_SEL=1/2. "0" - 1Tbit "1" - 2Tbits .. "9" - 10Tbits Values >9 is invalid per CXPI spec. Note for NRZ mode, although there are propagation delay from transceiver to CXPI controller, the delay is cancelled out as the timeout is compared on the RX (for transmit case, HW waits for the feedback on RX).	Insert addtional delay from the falling edge of RX to the falling edge of TX for slave node transmitting "0". This is valid only for PWM mode. The count value here indicates the number of clocks per clk_cxpi_ch. 0: None 1: means 1 clock. 2: means 2 clocks. ... 255: means 255 clocks. Note it must be set less than CTL1.T_LOW0. Note make sure that the falling edge of tx_out is ahead of the rising edge of master node clock when CTL0.PRESAMPLE_EN=1.

CXPI0_CH0_CTL2:		
Field	**Rev 0E**	**Rev 0F**
F2Name	T_WAKEUP_LENGTH	TIMEOUT_LENGTH

CXPI0_CH0_CTL2: TIMEOUT_LENGTH		
Field	**Rev 0E**	**Rev 0F**
F2LoBit	8	16

CXPI0_CH0_CTL2: TIMEOUT_LENGTH		
Field	**Rev 0E**	**Rev 0F**
F2HiBit	13	19

CXPI0_CH0_CTL2: TIMEOUT_LENGTH		
Field	**Rev 0E**	**Rev 0F**
F2Comment	Specifies the wake up pulse low period in Tbits that is transmitted during Standby mode. '0': 1 bit period '1': 2 bit period .. '49': 50 bit period Any value above 49 is invalid. This field is only valid if TX_WAKE_PULSE is set to 1.	Timeout Length (in Tbits). Specifies the number of Tbits to exceed timeout between frame bytes within a message frame. CXPI spec states that the maximum allowed inter byte space (IBS) is 9Tbits. This field is valid only when TIMEOUT_SEL=1/2. "0" - 1Tbit "1" - 2Tbits .. "9" - 10Tbits Values >9 is invalid per CXPI spec. Note for NRZ mode, although there are propagation delay from transceiver to CXPI controller, the delay is cancelled out as the timeout is compared on the RX (for transmit case, HW waits for the feedback on RX).

CXPI0_CH0_CTL2:		
Field	**Rev 0E**	**Rev 0F**
F3Name	RETRY	T_WAKEUP_LENGTH

CXPI0_CH0_CTL2: T_WAKEUP_LENGTH		
Field	**Rev 0E**	**Rev 0F**
F3LoBit	0	8

CXPI0_CH0_CTL2: T_WAKEUP_LENGTH		
Field	**Rev 0E**	**Rev 0F**
F3HiBit	1	13

CXPI0_CH0_CTL2: T_WAKEUP_LENGTH		
Field	**Rev 0E**	**Rev 0F**
F3Comment	Number of retries after arbitration lost. '0': No retries. .. '3': 3 retries. HW will immediately retry after arbitration lost i.e. after the message frame that won the arbitration is complete and fulfilled IFS. If SW wants to manage the retransmission then SW can program RETRY =0. In this case, HW will not retry after arbitration lost and will set TX_HEADER_ARB_LOST bit. SW needs to trigger HW to resend by programming the CMD fields again.	Specifies the wake up pulse low period in Tbits that is transmitted during Standby mode. '0': 1 bit period '1': 2 bit period .. '49': 50 bit period Any value above 49 is invalid. This field is only valid if TX_WAKE_PULSE is set to 1.

CXPI0_CH0_CTL2: : F4Name: Newly Added

CXPI0_CH0_CTL2: RETRY: F4LoBit: Newly Added

CXPI0_CH0_CTL2: RETRY: F4HiBit: Newly Added

CXPI0_CH0_CTL2: RETRY: F4SW: Newly Added

CXPI0_CH0_CTL2: RETRY: F4HW: Newly Added

CXPI0_CH0_CTL2: RETRY: F4Comment: Newly Added

CXPI0_CH0_CTL2: RETRY: F4DefaultVal: Newly Added

CXPI0_CH0_INTR: TX_FRAME_ERROR		
Field	**Rev 0E**	**Rev 0F**
F0Comment	HW sets this field to '1', when the stop bit of a byte frame is incorrect. This error would be a subset of TX_BIT_ERROR and also subjected to BIT_ERROR_IGNORE field. Note: The ongoing message transfer is aborted (INTR.TX_HEADER_DONE/RX_HEADER_DONE and INTR.TX_RESPONSE_DONE are NOT activated) and the TX_HEADER and TX_RESPONSE commands are set to '0'. Note: When CTL0.BIT_ERROR_IGNORE is '0', the ongoing message transfer is aborted (INTR.TX_HEADER_DONE and INTR.TX_RESPONSE_DONE is NOT activated) and the TX_HEADER and TX_RESPONSE commands are set to '0'. When CTL0.BIT_ERROR_IGNORE is '1', the ongoing message transfer would be transferred.	HW sets this field to '1', when the stop bit of a byte frame is incorrect. This error would be a subset of TX_BIT_ERROR and also subjected to BIT_ERROR_IGNORE field. Note: The ongoing message transfer is aborted (RX_HEADER_DONE and INTR.TX_RESPONSE_DONE are NOT activated. INTR.TX_HEADER_DONE is NOT activated if frame error occurs during the transmission of header byte) and the TX_HEADER and TX_RESPONSE commands are set to '0'. Note: When CTL0.BIT_ERROR_IGNORE is '0', the ongoing message transfer is aborted (INTR.TX_RESPONSE_DONE is NOT activated. INTR.TX_HEADER_DONE is NOT activated if frame error occurs during the transmission of header byte) and the TX_HEADER and TX_RESPONSE commands are set to '0'. When CTL0.BIT_ERROR_IGNORE is '1', the ongoing message transfer would be transferred.

CXPI0_CH0_INTR: RX_FRAME_ERROR		
Field	**Rev 0E**	**Rev 0F**
F1Comment	HW sets this field to '1', when the stop bit of a byte frame is incorrect. Note: The ongoing message transfer is aborted (INTR.RX_RESPONSE_DONE is NOT activated and the INTR.RX_HEADER_DONE/TX_HEADER_DONE is NOT activated if the frame error occurs during header byte or if frame error occurs during response byte (if the HEADER and RESPONSE commands are set together)).	HW sets this field to '1', when the stop bit of a byte frame is incorrect. Note: The ongoing message transfer is aborted (INTR.RX_RESPONSE_DONE is NOT activated and the INTR.RX_HEADER_DONE is NOT activated if the frame error occurs during header byte or if frame error occurs during response byte (if the HEADER and RESPONSE commands are set together)).

CXPI0_CH0_INTR: TX_BIT_ERROR		
Field	**Rev 0E**	**Rev 0F**
F10Comment	HW sets this field to '1', when a transmitted "cxpi_tx_out" value does NOT match a received "cxpi_rx_in" value. The match is performed for the PID fields or PType (for the START bit and STOP bit only) and for the rest of the response i.e. frame information fields, data fields and the crc field (for the START bit, DATA bits, and STOP bits). Note: When CTL0.BIT_ERROR_IGNORE is '0', the ongoing message transfer is aborted (INTR.TX_HEADER_DONE and INTR.TX_RESPONSE_DONE is NOT activated) and the TX_HEADER and TX_RESPONSE commands are set to '0'. When CTL0.BIT_ERROR_IGNORE is '1', the ongoing message transfer would be transferred.	HW sets this field to '1', when a transmitted "cxpi_tx_out" value does NOT match a received "cxpi_rx_in" value. The match is performed for the PID fields or PType (for the START bit and STOP bit only) and for the rest of the response i.e. frame information fields, data fields and the crc field (for the START bit, DATA bits, and STOP bits). Note: When CTL0.BIT_ERROR_IGNORE is '0', the ongoing message transfer is aborted (INTR.TX_RESPONSE_DONE is NOT activated. INTR.TX_HEADER_DONE is NOT activated if bit error occurs during the transmission of header byte) and the TX_HEADER and TX_RESPONSE commands are set to '0'. When CTL0.BIT_ERROR_IGNORE is '1', the ongoing message transfer would be transferred.

CXPI0_CH0_INTR: TX_HEADER_DONE		
Field	**Rev 0E**	**Rev 0F**
F22Comment	HW sets this field to '1', when a frame header (PID field or PType field) is transmitted (the CMD.TX_HEADER is completed). Specifically: - For PID transmission only and without prior transmission of PTYPE, when followed by CMD.TX_RESPONSE or CMD.RX_RESPONSE, this field is set to '1' after completion of the message frame transfer. - For PID transmission only and without prior transmission of PTYPE, when not followed by a response command, this field is set to '1' after completion of the header transfer. -Note for the case of PTYPE is transmitted follow by CMD.RX_RESPONSE or no following response, HW sets this field to '1' after transmitting PTYPE.	HW sets this field to '1', when a frame header (PID field or PType field) is transmitted (the CMD.TX_HEADER is completed).

CXPI0_CH1_CTL0:		
Field	**Rev 0E**	**Rev 0F**
F5Name	FILTER_EN	PRESAMPLE_EN

CXPI0_CH1_CTL0: PRESAMPLE_EN		
Field	**Rev 0E**	**Rev 0F**
F5LoBit	8	9

CXPI0_CH1_CTL0: PRESAMPLE_EN		
Field	**Rev 0E**	**Rev 0F**
F5HiBit	8	9

CXPI0_CH1_CTL0: PRESAMPLE_EN		
Field	**Rev 0E**	**Rev 0F**
F5Comment	RX filter enable (for "cxpi_rx_in") '0': No filter '1': Median 3 (default value) operates on the last three "cxpi_rx_in" values. The sequences '000', '001', '010', and '100' result in a filtered value '0'. The sequences '111', '110', '101', and '011' result in a filtered value '1'.	Pre-sample enable for PWM mode. '0': Disbaled. '1': Enabled When sampling counter's value is greater than CTL1.T_LOW1, pre-sample FF will be set to "1" as long as detecting any "1" on "cxpi_rx_in" and be cleared to "0" after sampling moment. At the sampling moment, if pre-sample FF or "cxpi_rx_in" is "1", sample value will be "1", otherwise "0".

CXPI0_CH1_CTL0:		
Field	**Rev 0E**	**Rev 0F**
F6Name	RXPIDZERO_CHECK_EN	FILTER_EN

CXPI0_CH1_CTL0: FILTER_EN		
Field	**Rev 0E**	**Rev 0F**
F6LoBit	7	8

CXPI0_CH1_CTL0: FILTER_EN		
Field	**Rev 0E**	**Rev 0F**
F6HiBit	7	8

CXPI0_CH1_CTL0: FILTER_EN		
Field	**Rev 0E**	**Rev 0F**
F6Comment	Receive PID Zero Check Enable. 0 - No action if received PID[6:0] = 0 and PID[7]=1'b1. 1 - If received PID[6:0] = 0 and PID[7]=1'b1, HW (slave) does not clear CMD.RX_HEADER and will anticipate receiving header again (CMD.TX_HEADER=0). If CMD.TX_HEADER=1 in the same scenario, then HW (slave) clears CMD.RX_HEADER upon receiving the header follow by transmit PID. This mode is useful for case where polling method is used and CXPI controller is configured as slave. This would reduce dependency on SW to react to the header received within IBS=1.	RX filter enable (for "cxpi_rx_in") '0': No filter '1': Median 3 (default value) operates on the last three "cxpi_rx_in" values. The sequences '000', '001', '010', and '100' result in a filtered value '0'. The sequences '111', '110', '101', and '011' result in a filtered value '1'.

CXPI0_CH1_CTL0:		
Field	**Rev 0E**	**Rev 0F**
F7Name	AUTO_EN	RXPIDZERO_CHECK_EN

CXPI0_CH1_CTL0: RXPIDZERO_CHECK_EN		
Field	**Rev 0E**	**Rev 0F**
F7LoBit	4	7

CXPI0_CH1_CTL0: RXPIDZERO_CHECK_EN		
Field	**Rev 0E**	**Rev 0F**
F7HiBit	4	7

CXPI0_CH1_CTL0: RXPIDZERO_CHECK_EN		
Field	**Rev 0E**	**Rev 0F**
F7Comment	CXPI transceiver auto enable: '0': Disabled. '1': Enabled. The TX_RX_STATUS.EN_OUT field is controlled by HW.	Receive PID Zero Check Enable. 0 - No action if received PID[6:0] = 0 and PID[7]=1'b1. 1 - If received PID[6:0] = 0 and PID[7]=1'b1, HW (slave) does not clear CMD.RX_HEADER and will anticipate receiving header again (CMD.TX_HEADER=0). If CMD.TX_HEADER=1 in the same scenario, then HW (slave) clears CMD.RX_HEADER upon receiving the header follow by transmit PID. This mode is useful for case where polling method is used and CXPI controller is configured as slave. This would reduce dependency on SW to react to the header received within IBS=1.

CXPI0_CH1_CTL0: RXPIDZERO_CHECK_EN		
Field	**Rev 0E**	**Rev 0F**
F7DefaultVal	1	0

CXPI0_CH1_CTL0:		
Field	**Rev 0E**	**Rev 0F**
F8Name	MODE	AUTO_EN

CXPI0_CH1_CTL0: AUTO_EN		
Field	**Rev 0E**	**Rev 0F**
F8LoBit	0	4

CXPI0_CH1_CTL0: AUTO_EN		
Field	**Rev 0E**	**Rev 0F**
F8HiBit	0	4

CXPI0_CH1_CTL0: AUTO_EN		
Field	**Rev 0E**	**Rev 0F**
F8Comment	Mode of operation: '0': NRZ mode. '1': PWM mode.	CXPI transceiver auto enable: '0': Disabled. '1': Enabled. The TX_RX_STATUS.EN_OUT field is controlled by HW.

CXPI0_CH1_CTL0: AUTO_EN		
Field	**Rev 0E**	**Rev 0F**
F8DefaultVal	0	1

CXPI0_CH1_CTL0: : F9Name: Newly Added

CXPI0_CH1_CTL0: MODE: F9LoBit: Newly Added

CXPI0_CH1_CTL0: MODE: F9HiBit: Newly Added

CXPI0_CH1_CTL0: MODE: F9SW: Newly Added

CXPI0_CH1_CTL0: MODE: F9HW: Newly Added

CXPI0_CH1_CTL0: MODE: F9Comment: Newly Added

CXPI0_CH1_CTL0: MODE: F9DefaultVal: Newly Added

CXPI0_CH1_CTL1: T_LOW1		
Field	**Rev 0E**	**Rev 0F**
F2Comment	Low count for logic 1. This is valid only for PWM mode. The count value here indicates the number of clocks per clk_cxpi_ch to drive a '0' at CXPI bus before releasing it to indicate a logical '1'. 0: means 1 clock. 1: means 2 clocks .. 15: means 16 clocks. .. 399: means 400 clocks. Any value above 399 is invalid. Note that for NRZ mode, this field is ignored. Note that this field is used for TX.	Low count for logic 1. This is valid only for PWM mode. For master node, The count value here indicates the number of clocks per clk_cxpi_ch to drive a '0' at CXPI bus before releasing it to indicate a logical '1'. For slave node and pre-sample enabled, the count value indicates the number of clocks per clk_cxpi_ch to disable pre-sampling. 0: means 1 clock. 1: means 2 clocks .. 15: means 16 clocks. .. 399: means 400 clocks. Any value above 399 is invalid. Note that for NRZ mode, this field is ignored. Note that it must be set less than CTL1.T_OFFSET for slave node if pre-sample mode enabled. Note that it is also effective for pre-sample mode of master node.

CXPI0_CH1_CTL2:		
Field	**Rev 0E**	**Rev 0F**
F1Name	TIMEOUT_LENGTH	RXTX_DELAY

CXPI0_CH1_CTL2: RXTX_DELAY		
Field	**Rev 0E**	**Rev 0F**
F1LoBit	16	22

CXPI0_CH1_CTL2: RXTX_DELAY		
Field	**Rev 0E**	**Rev 0F**
F1HiBit	19	29

CXPI0_CH1_CTL2: RXTX_DELAY		
Field	**Rev 0E**	**Rev 0F**
F1Comment	Timeout Length (in Tbits). Specifies the number of Tbits to exceed timeout between frame bytes within a message frame. CXPI spec states that the maximum allowed inter byte space (IBS) is 9Tbits. This field is valid only when TIMEOUT_SEL=1/2. "0" - 1Tbit "1" - 2Tbits .. "9" - 10Tbits Values >9 is invalid per CXPI spec. Note for NRZ mode, although there are propagation delay from transceiver to CXPI controller, the delay is cancelled out as the timeout is compared on the RX (for transmit case, HW waits for the feedback on RX).	Insert addtional delay from the falling edge of RX to the falling edge of TX for slave node transmitting "0". This is valid only for PWM mode. The count value here indicates the number of clocks per clk_cxpi_ch. 0: None 1: means 1 clock. 2: means 2 clocks. ... 255: means 255 clocks. Note it must be set less than CTL1.T_LOW0. Note make sure that the falling edge of tx_out is ahead of the rising edge of master node clock when CTL0.PRESAMPLE_EN=1.

CXPI0_CH1_CTL2:		
Field	**Rev 0E**	**Rev 0F**
F2Name	T_WAKEUP_LENGTH	TIMEOUT_LENGTH

CXPI0_CH1_CTL2: TIMEOUT_LENGTH		
Field	**Rev 0E**	**Rev 0F**
F2LoBit	8	16

CXPI0_CH1_CTL2: TIMEOUT_LENGTH		
Field	**Rev 0E**	**Rev 0F**
F2HiBit	13	19

CXPI0_CH1_CTL2: TIMEOUT_LENGTH		
Field	**Rev 0E**	**Rev 0F**
F2Comment	Specifies the wake up pulse low period in Tbits that is transmitted during Standby mode. '0': 1 bit period '1': 2 bit period .. '49': 50 bit period Any value above 49 is invalid. This field is only valid if TX_WAKE_PULSE is set to 1.	Timeout Length (in Tbits). Specifies the number of Tbits to exceed timeout between frame bytes within a message frame. CXPI spec states that the maximum allowed inter byte space (IBS) is 9Tbits. This field is valid only when TIMEOUT_SEL=1/2. "0" - 1Tbit "1" - 2Tbits .. "9" - 10Tbits Values >9 is invalid per CXPI spec. Note for NRZ mode, although there are propagation delay from transceiver to CXPI controller, the delay is cancelled out as the timeout is compared on the RX (for transmit case, HW waits for the feedback on RX).

CXPI0_CH1_CTL2:		
Field	**Rev 0E**	**Rev 0F**
F3Name	RETRY	T_WAKEUP_LENGTH

CXPI0_CH1_CTL2: T_WAKEUP_LENGTH		
Field	**Rev 0E**	**Rev 0F**
F3LoBit	0	8

CXPI0_CH1_CTL2: T_WAKEUP_LENGTH		
Field	**Rev 0E**	**Rev 0F**
F3HiBit	1	13

CXPI0_CH1_CTL2: T_WAKEUP_LENGTH		
Field	**Rev 0E**	**Rev 0F**
F3Comment	Number of retries after arbitration lost. '0': No retries. .. '3': 3 retries. HW will immediately retry after arbitration lost i.e. after the message frame that won the arbitration is complete and fulfilled IFS. If SW wants to manage the retransmission then SW can program RETRY =0. In this case, HW will not retry after arbitration lost and will set TX_HEADER_ARB_LOST bit. SW needs to trigger HW to resend by programming the CMD fields again.	Specifies the wake up pulse low period in Tbits that is transmitted during Standby mode. '0': 1 bit period '1': 2 bit period .. '49': 50 bit period Any value above 49 is invalid. This field is only valid if TX_WAKE_PULSE is set to 1.

CXPI0_CH1_CTL2: : F4Name: Newly Added

CXPI0_CH1_CTL2: RETRY: F4LoBit: Newly Added

CXPI0_CH1_CTL2: RETRY: F4HiBit: Newly Added

CXPI0_CH1_CTL2: RETRY: F4SW: Newly Added

CXPI0_CH1_CTL2: RETRY: F4HW: Newly Added

CXPI0_CH1_CTL2: RETRY: F4Comment: Newly Added

CXPI0_CH1_CTL2: RETRY: F4DefaultVal: Newly Added

CXPI0_CH1_INTR: TX_FRAME_ERROR		
Field	**Rev 0E**	**Rev 0F**
F0Comment	HW sets this field to '1', when the stop bit of a byte frame is incorrect. This error would be a subset of TX_BIT_ERROR and also subjected to BIT_ERROR_IGNORE field. Note: The ongoing message transfer is aborted (INTR.TX_HEADER_DONE/RX_HEADER_DONE and INTR.TX_RESPONSE_DONE are NOT activated) and the TX_HEADER and TX_RESPONSE commands are set to '0'. Note: When CTL0.BIT_ERROR_IGNORE is '0', the ongoing message transfer is aborted (INTR.TX_HEADER_DONE and INTR.TX_RESPONSE_DONE is NOT activated) and the TX_HEADER and TX_RESPONSE commands are set to '0'. When CTL0.BIT_ERROR_IGNORE is '1', the ongoing message transfer would be transferred.	HW sets this field to '1', when the stop bit of a byte frame is incorrect. This error would be a subset of TX_BIT_ERROR and also subjected to BIT_ERROR_IGNORE field. Note: The ongoing message transfer is aborted (RX_HEADER_DONE and INTR.TX_RESPONSE_DONE are NOT activated. INTR.TX_HEADER_DONE is NOT activated if frame error occurs during the transmission of header byte) and the TX_HEADER and TX_RESPONSE commands are set to '0'. Note: When CTL0.BIT_ERROR_IGNORE is '0', the ongoing message transfer is aborted (INTR.TX_RESPONSE_DONE is NOT activated. INTR.TX_HEADER_DONE is NOT activated if frame error occurs during the transmission of header byte) and the TX_HEADER and TX_RESPONSE commands are set to '0'. When CTL0.BIT_ERROR_IGNORE is '1', the ongoing message transfer would be transferred.

CXPI0_CH1_INTR: RX_FRAME_ERROR		
Field	**Rev 0E**	**Rev 0F**
F1Comment	HW sets this field to '1', when the stop bit of a byte frame is incorrect. Note: The ongoing message transfer is aborted (INTR.RX_RESPONSE_DONE is NOT activated and the INTR.RX_HEADER_DONE/TX_HEADER_DONE is NOT activated if the frame error occurs during header byte or if frame error occurs during response byte (if the HEADER and RESPONSE commands are set together)).	HW sets this field to '1', when the stop bit of a byte frame is incorrect. Note: The ongoing message transfer is aborted (INTR.RX_RESPONSE_DONE is NOT activated and the INTR.RX_HEADER_DONE is NOT activated if the frame error occurs during header byte or if frame error occurs during response byte (if the HEADER and RESPONSE commands are set together)).

CXPI0_CH1_INTR: TX_BIT_ERROR		
Field	**Rev 0E**	**Rev 0F**
F10Comment	HW sets this field to '1', when a transmitted "cxpi_tx_out" value does NOT match a received "cxpi_rx_in" value. The match is performed for the PID fields or PType (for the START bit and STOP bit only) and for the rest of the response i.e. frame information fields, data fields and the crc field (for the START bit, DATA bits, and STOP bits). Note: When CTL0.BIT_ERROR_IGNORE is '0', the ongoing message transfer is aborted (INTR.TX_HEADER_DONE and INTR.TX_RESPONSE_DONE is NOT activated) and the TX_HEADER and TX_RESPONSE commands are set to '0'. When CTL0.BIT_ERROR_IGNORE is '1', the ongoing message transfer would be transferred.	HW sets this field to '1', when a transmitted "cxpi_tx_out" value does NOT match a received "cxpi_rx_in" value. The match is performed for the PID fields or PType (for the START bit and STOP bit only) and for the rest of the response i.e. frame information fields, data fields and the crc field (for the START bit, DATA bits, and STOP bits). Note: When CTL0.BIT_ERROR_IGNORE is '0', the ongoing message transfer is aborted (INTR.TX_RESPONSE_DONE is NOT activated. INTR.TX_HEADER_DONE is NOT activated if bit error occurs during the transmission of header byte) and the TX_HEADER and TX_RESPONSE commands are set to '0'. When CTL0.BIT_ERROR_IGNORE is '1', the ongoing message transfer would be transferred.

CXPI0_CH1_INTR: TX_HEADER_DONE		
Field	**Rev 0E**	**Rev 0F**
F22Comment	HW sets this field to '1', when a frame header (PID field or PType field) is transmitted (the CMD.TX_HEADER is completed). Specifically: - For PID transmission only and without prior transmission of PTYPE, when followed by CMD.TX_RESPONSE or CMD.RX_RESPONSE, this field is set to '1' after completion of the message frame transfer. - For PID transmission only and without prior transmission of PTYPE, when not followed by a response command, this field is set to '1' after completion of the header transfer. -Note for the case of PTYPE is transmitted follow by CMD.RX_RESPONSE or no following response, HW sets this field to '1' after transmitting PTYPE.	HW sets this field to '1', when a frame header (PID field or PType field) is transmitted (the CMD.TX_HEADER is completed).

CANFD0_CH0_CREL: CANFD0_CH0_CREL		
Field	**Rev 0E**	**Rev 0F**
Default	0x00000000	0x32380609

CANFD0_CH0_CREL: REL		
Field	**Rev 0E**	**Rev 0F**
F0DefaultVal	0	3

CANFD0_CH0_CREL: STEP		
Field	**Rev 0E**	**Rev 0F**
F1DefaultVal	0	2

CANFD0_CH0_CREL: SUBSTEP		
Field	**Rev 0E**	**Rev 0F**
F2DefaultVal	0	3

CANFD0_CH0_CREL: YEAR		
Field	**Rev 0E**	**Rev 0F**
F3DefaultVal	0	8

CANFD0_CH0_CREL: MON		
Field	**Rev 0E**	**Rev 0F**
F4DefaultVal	0	6

CANFD0_CH0_CREL: DAY		
Field	**Rev 0E**	**Rev 0F**
F5DefaultVal	0	9

CANFD0_CH0_RXF0S: F0GI		
Field	**Rev 0E**	**Rev 0F**
F3Comment	Rx FIFO 0 Get Index Rx FIFO 0 read index pointer, range 0 to 63. This field is updated by the software writing to RxF0A.F0AI	Rx FIFO 0 Get Index Rx FIFO 0 read index pointer, range 0 to 63. This field is updated by the software writing to RXF0A.F0AI. When the software reading the value immediately after writing to RXF0A.F0AI, this value should be read twice to ensure that the update is reflected.

CANFD0_CH0_RXF0S: F0FL		
Field	**Rev 0E**	**Rev 0F**
F4Comment	Rx FIFO 0 Fill Level Number of elements stored in Rx FIFO 0, range 0 to 64.	Rx FIFO 0 Fill Level Number of elements stored in Rx FIFO 0, range 0 to 64. When the software reading the value immediately after writing to RXF0A.F0AI, this value should be read twice to ensure that the update is reflected.

CANFD0_CH0_RXF1S: F1GI		
Field	**Rev 0E**	**Rev 0F**
F4Comment	Rx FIFO 1 Get Index Rx FIFO 1 read index pointer, range 0 to 63. This field is updated by the software writing to RxF1A.FAI	Rx FIFO 1 Get Index Rx FIFO 1 read index pointer, range 0 to 63. This field is updated by the software writing to RXF1A.F1AI. When the software reading the value immediately after writing to RXF1A.F1AI, this value should be read twice to ensure that the update is reflected.

CANFD0_CH0_RXF1S: F1FL		
Field	**Rev 0E**	**Rev 0F**
F5Comment	Rx FIFO 1 Fill Level Number of elements stored in Rx FIFO 1, range 0 to 64.	Rx FIFO 1 Fill Level Number of elements stored in Rx FIFO 1, range 0 to 64. When the software reading the value immediately after writing to RXF1A.F1AI, this value should be read twice to ensure that the update is reflected.

CANFD0_CH0_TXEFS: EFGI		
Field	**Rev 0E**	**Rev 0F**
F3Comment	Event FIFO Get Index Tx Event FIFO read index pointer, range 0 to 31.	Event FIFO Get Index Tx Event FIFO read index pointer, range 0 to 31. This field is updated by the software writing to TXEFA.EFAI. When the software reading the value immediately after writing to TXEFA.EFAI, this value should be read twice to ensure that the update is reflected.

CANFD0_CH0_TXEFS: EFFL		
Field	**Rev 0E**	**Rev 0F**
F4Comment	Event FIFO Fill Level Number of elements stored in Tx Event FIFO, range 0 to 32.	Event FIFO Fill Level Number of elements stored in Tx Event FIFO, range 0 to 32. When the software reading the value immediately after writing to TXEFA.EFAI, this value should be read twice to ensure that the update is reflected.

CANFD0_CH0_TTOST: CANFD0_CH0_TTOST		
Field	**Rev 0E**	**Rev 0F**
Default	0x00000000	0x00000080

CANFD0_CH0_TTOST: QCS		
Field	**Rev 0E**	**Rev 0F**
F9DefaultVal	0	1

CANFD0_CH1_CREL: CANFD0_CH1_CREL		
Field	**Rev 0E**	**Rev 0F**
Default	0x00000000	0x32380609

CANFD0_CH1_CREL: REL		
Field	**Rev 0E**	**Rev 0F**
F0DefaultVal	0	3

CANFD0_CH1_CREL: STEP		
Field	**Rev 0E**	**Rev 0F**
F1DefaultVal	0	2

CANFD0_CH1_CREL: SUBSTEP		
Field	**Rev 0E**	**Rev 0F**
F2DefaultVal	0	3

CANFD0_CH1_CREL: YEAR		
Field	**Rev 0E**	**Rev 0F**
F3DefaultVal	0	8

CANFD0_CH1_CREL: MON		
Field	**Rev 0E**	**Rev 0F**
F4DefaultVal	0	6

CANFD0_CH1_CREL: DAY		
Field	**Rev 0E**	**Rev 0F**
F5DefaultVal	0	9

CANFD0_CH1_RXF0S: F0GI		
Field	**Rev 0E**	**Rev 0F**
F3Comment	Rx FIFO 0 Get Index Rx FIFO 0 read index pointer, range 0 to 63. This field is updated by the software writing to RxF0A.F0AI	Rx FIFO 0 Get Index Rx FIFO 0 read index pointer, range 0 to 63. This field is updated by the software writing to RXF0A.F0AI. When the software reading the value immediately after writing to RXF0A.F0AI, this value should be read twice to ensure that the update is reflected.

CANFD0_CH1_RXF0S: F0FL		
Field	**Rev 0E**	**Rev 0F**
F4Comment	Rx FIFO 0 Fill Level Number of elements stored in Rx FIFO 0, range 0 to 64.	Rx FIFO 0 Fill Level Number of elements stored in Rx FIFO 0, range 0 to 64. When the software reading the value immediately after writing to RXF0A.F0AI, this value should be read twice to ensure that the update is reflected.

CANFD0_CH1_RXF1S: F1GI		
Field	**Rev 0E**	**Rev 0F**
F4Comment	Rx FIFO 1 Get Index Rx FIFO 1 read index pointer, range 0 to 63. This field is updated by the software writing to RxF1A.FAI	Rx FIFO 1 Get Index Rx FIFO 1 read index pointer, range 0 to 63. This field is updated by the software writing to RXF1A.F1AI. When the software reading the value immediately after writing to RXF1A.F1AI, this value should be read twice to ensure that the update is reflected.

CANFD0_CH1_RXF1S: F1FL		
Field	**Rev 0E**	**Rev 0F**
F5Comment	Rx FIFO 1 Fill Level Number of elements stored in Rx FIFO 1, range 0 to 64.	Rx FIFO 1 Fill Level Number of elements stored in Rx FIFO 1, range 0 to 64. When the software reading the value immediately after writing to RXF1A.F1AI, this value should be read twice to ensure that the update is reflected.

CANFD0_CH1_TXEFS: EFGI		
Field	**Rev 0E**	**Rev 0F**
F3Comment	Event FIFO Get Index Tx Event FIFO read index pointer, range 0 to 31.	Event FIFO Get Index Tx Event FIFO read index pointer, range 0 to 31. This field is updated by the software writing to TXEFA.EFAI. When the software reading the value immediately after writing to TXEFA.EFAI, this value should be read twice to ensure that the update is reflected.

CANFD0_CH1_TXEFS: EFFL		
Field	**Rev 0E**	**Rev 0F**
F4Comment	Event FIFO Fill Level Number of elements stored in Tx Event FIFO, range 0 to 32.	Event FIFO Fill Level Number of elements stored in Tx Event FIFO, range 0 to 32. When the software reading the value immediately after writing to TXEFA.EFAI, this value should be read twice to ensure that the update is reflected.

CANFD0_CH1_TTOST: CANFD0_CH1_TTOST		
Field	**Rev 0E**	**Rev 0F**
Default	0x00000000	0x00000080

CANFD0_CH1_TTOST: QCS		
Field	**Rev 0E**	**Rev 0F**
F9DefaultVal	0	1

CANFD1_CH0_CREL: CANFD1_CH0_CREL		
Field	**Rev 0E**	**Rev 0F**
Default	0x00000000	0x32380609

CANFD1_CH0_CREL: REL		
Field	**Rev 0E**	**Rev 0F**
F0DefaultVal	0	3

CANFD1_CH0_CREL: STEP		
Field	**Rev 0E**	**Rev 0F**
F1DefaultVal	0	2

CANFD1_CH0_CREL: SUBSTEP		
Field	**Rev 0E**	**Rev 0F**
F2DefaultVal	0	3

CANFD1_CH0_CREL: YEAR		
Field	**Rev 0E**	**Rev 0F**
F3DefaultVal	0	8

CANFD1_CH0_CREL: MON		
Field	**Rev 0E**	**Rev 0F**
F4DefaultVal	0	6

CANFD1_CH0_CREL: DAY		
Field	**Rev 0E**	**Rev 0F**
F5DefaultVal	0	9

CANFD1_CH0_RXF0S: F0GI		
Field	**Rev 0E**	**Rev 0F**
F3Comment	Rx FIFO 0 Get Index Rx FIFO 0 read index pointer, range 0 to 63. This field is updated by the software writing to RxF0A.F0AI	Rx FIFO 0 Get Index Rx FIFO 0 read index pointer, range 0 to 63. This field is updated by the software writing to RXF0A.F0AI. When the software reading the value immediately after writing to RXF0A.F0AI, this value should be read twice to ensure that the update is reflected.

CANFD1_CH0_RXF0S: F0FL		
Field	**Rev 0E**	**Rev 0F**
F4Comment	Rx FIFO 0 Fill Level Number of elements stored in Rx FIFO 0, range 0 to 64.	Rx FIFO 0 Fill Level Number of elements stored in Rx FIFO 0, range 0 to 64. When the software reading the value immediately after writing to RXF0A.F0AI, this value should be read twice to ensure that the update is reflected.

CANFD1_CH0_RXF1S: F1GI		
Field	**Rev 0E**	**Rev 0F**
F4Comment	Rx FIFO 1 Get Index Rx FIFO 1 read index pointer, range 0 to 63. This field is updated by the software writing to RxF1A.FAI	Rx FIFO 1 Get Index Rx FIFO 1 read index pointer, range 0 to 63. This field is updated by the software writing to RXF1A.F1AI. When the software reading the value immediately after writing to RXF1A.F1AI, this value should be read twice to ensure that the update is reflected.

CANFD1_CH0_RXF1S: F1FL		
Field	**Rev 0E**	**Rev 0F**
F5Comment	Rx FIFO 1 Fill Level Number of elements stored in Rx FIFO 1, range 0 to 64.	Rx FIFO 1 Fill Level Number of elements stored in Rx FIFO 1, range 0 to 64. When the software reading the value immediately after writing to RXF1A.F1AI, this value should be read twice to ensure that the update is reflected.

CANFD1_CH0_TXEFS: EFGI		
Field	**Rev 0E**	**Rev 0F**
F3Comment	Event FIFO Get Index Tx Event FIFO read index pointer, range 0 to 31.	Event FIFO Get Index Tx Event FIFO read index pointer, range 0 to 31. This field is updated by the software writing to TXEFA.EFAI. When the software reading the value immediately after writing to TXEFA.EFAI, this value should be read twice to ensure that the update is reflected.

CANFD1_CH0_TXEFS: EFFL		
Field	**Rev 0E**	**Rev 0F**
F4Comment	Event FIFO Fill Level Number of elements stored in Tx Event FIFO, range 0 to 32.	Event FIFO Fill Level Number of elements stored in Tx Event FIFO, range 0 to 32. When the software reading the value immediately after writing to TXEFA.EFAI, this value should be read twice to ensure that the update is reflected.

CANFD1_CH0_TTOST: CANFD1_CH0_TTOST		
Field	**Rev 0E**	**Rev 0F**
Default	0x00000000	0x00000080

CANFD1_CH0_TTOST: QCS		
Field	**Rev 0E**	**Rev 0F**
F9DefaultVal	0	1

CANFD1_CH1_CREL: CANFD1_CH1_CREL		
Field	**Rev 0E**	**Rev 0F**
Default	0x00000000	0x32380609

CANFD1_CH1_CREL: REL		
Field	**Rev 0E**	**Rev 0F**
F0DefaultVal	0	3

CANFD1_CH1_CREL: STEP		
Field	**Rev 0E**	**Rev 0F**
F1DefaultVal	0	2

CANFD1_CH1_CREL: SUBSTEP		
Field	**Rev 0E**	**Rev 0F**
F2DefaultVal	0	3

CANFD1_CH1_CREL: YEAR		
Field	**Rev 0E**	**Rev 0F**
F3DefaultVal	0	8

CANFD1_CH1_CREL: MON		
Field	**Rev 0E**	**Rev 0F**
F4DefaultVal	0	6

CANFD1_CH1_CREL: DAY		
Field	**Rev 0E**	**Rev 0F**
F5DefaultVal	0	9

CANFD1_CH1_RXF0S: F0GI		
Field	**Rev 0E**	**Rev 0F**
F3Comment	Rx FIFO 0 Get Index Rx FIFO 0 read index pointer, range 0 to 63. This field is updated by the software writing to RxF0A.F0AI	Rx FIFO 0 Get Index Rx FIFO 0 read index pointer, range 0 to 63. This field is updated by the software writing to RXF0A.F0AI. When the software reading the value immediately after writing to RXF0A.F0AI, this value should be read twice to ensure that the update is reflected.

CANFD1_CH1_RXF0S: F0FL		
Field	**Rev 0E**	**Rev 0F**
F4Comment	Rx FIFO 0 Fill Level Number of elements stored in Rx FIFO 0, range 0 to 64.	Rx FIFO 0 Fill Level Number of elements stored in Rx FIFO 0, range 0 to 64. When the software reading the value immediately after writing to RXF0A.F0AI, this value should be read twice to ensure that the update is reflected.

CANFD1_CH1_RXF1S: F1GI		
Field	**Rev 0E**	**Rev 0F**
F4Comment	Rx FIFO 1 Get Index Rx FIFO 1 read index pointer, range 0 to 63. This field is updated by the software writing to RxF1A.FAI	Rx FIFO 1 Get Index Rx FIFO 1 read index pointer, range 0 to 63. This field is updated by the software writing to RXF1A.F1AI. When the software reading the value immediately after writing to RXF1A.F1AI, this value should be read twice to ensure that the update is reflected.

CANFD1_CH1_RXF1S: F1FL		
Field	**Rev 0E**	**Rev 0F**
F5Comment	Rx FIFO 1 Fill Level Number of elements stored in Rx FIFO 1, range 0 to 64.	Rx FIFO 1 Fill Level Number of elements stored in Rx FIFO 1, range 0 to 64. When the software reading the value immediately after writing to RXF1A.F1AI, this value should be read twice to ensure that the update is reflected.

CANFD1_CH1_TXEFS: EFGI		
Field	**Rev 0E**	**Rev 0F**
F3Comment	Event FIFO Get Index Tx Event FIFO read index pointer, range 0 to 31.	Event FIFO Get Index Tx Event FIFO read index pointer, range 0 to 31. This field is updated by the software writing to TXEFA.EFAI. When the software reading the value immediately after writing to TXEFA.EFAI, this value should be read twice to ensure that the update is reflected.

CANFD1_CH1_TXEFS: EFFL		
Field	**Rev 0E**	**Rev 0F**
F4Comment	Event FIFO Fill Level Number of elements stored in Tx Event FIFO, range 0 to 32.	Event FIFO Fill Level Number of elements stored in Tx Event FIFO, range 0 to 32. When the software reading the value immediately after writing to TXEFA.EFAI, this value should be read twice to ensure that the update is reflected.

CANFD1_CH1_TTOST: CANFD1_CH1_TTOST		
Field	**Rev 0E**	**Rev 0F**
Default	0x00000000	0x00000080

CANFD1_CH1_TTOST: QCS		
Field	**Rev 0E**	**Rev 0F**
F9DefaultVal	0	1

SCB0_INTR_TX: UNDERFLOW		
Field	**Rev 0E**	**Rev 0F**
F4Comment	Attempt to read from an empty TX FIFO. This happens when SCB is ready to transfer data and EMPTY is '1'. Only used in FIFO mode.	Attempt to read from an empty TX FIFO. This happens when SCB is ready to transfer data and EMPTY is '1'. Only used in FIFO mode. (Note: This bit may be set unintentionally, even if the FIFO is not empty. Workaround: Ignore the bit when the clock frequency of the AHB bus is greater than 3x the internal frequency of SCB and the FIFO is not empty)

SCB1_INTR_TX: UNDERFLOW		
Field	**Rev 0E**	**Rev 0F**
F4Comment	Attempt to read from an empty TX FIFO. This happens when SCB is ready to transfer data and EMPTY is '1'. Only used in FIFO mode.	Attempt to read from an empty TX FIFO. This happens when SCB is ready to transfer data and EMPTY is '1'. Only used in FIFO mode. (Note: This bit may be set unintentionally, even if the FIFO is not empty. Workaround: Ignore the bit when the clock frequency of the AHB bus is greater than 3x the internal frequency of SCB and the FIFO is not empty)

SCB2_INTR_TX: UNDERFLOW		
Field	**Rev 0E**	**Rev 0F**
F4Comment	Attempt to read from an empty TX FIFO. This happens when SCB is ready to transfer data and EMPTY is '1'. Only used in FIFO mode.	Attempt to read from an empty TX FIFO. This happens when SCB is ready to transfer data and EMPTY is '1'. Only used in FIFO mode. (Note: This bit may be set unintentionally, even if the FIFO is not empty. Workaround: Ignore the bit when the clock frequency of the AHB bus is greater than 3x the internal frequency of SCB and the FIFO is not empty)

SCB3_INTR_TX: UNDERFLOW		
Field	**Rev 0E**	**Rev 0F**
F4Comment	Attempt to read from an empty TX FIFO. This happens when SCB is ready to transfer data and EMPTY is '1'. Only used in FIFO mode.	Attempt to read from an empty TX FIFO. This happens when SCB is ready to transfer data and EMPTY is '1'. Only used in FIFO mode. (Note: This bit may be set unintentionally, even if the FIFO is not empty. Workaround: Ignore the bit when the clock frequency of the AHB bus is greater than 3x the internal frequency of SCB and the FIFO is not empty)

SCB4_INTR_TX: UNDERFLOW		
Field	**Rev 0E**	**Rev 0F**
F4Comment	Attempt to read from an empty TX FIFO. This happens when SCB is ready to transfer data and EMPTY is '1'. Only used in FIFO mode.	Attempt to read from an empty TX FIFO. This happens when SCB is ready to transfer data and EMPTY is '1'. Only used in FIFO mode. (Note: This bit may be set unintentionally, even if the FIFO is not empty. Workaround: Ignore the bit when the clock frequency of the AHB bus is greater than 3x the internal frequency of SCB and the FIFO is not empty)

SCB5_INTR_TX: UNDERFLOW		
Field	**Rev 0E**	**Rev 0F**
F4Comment	Attempt to read from an empty TX FIFO. This happens when SCB is ready to transfer data and EMPTY is '1'. Only used in FIFO mode.	Attempt to read from an empty TX FIFO. This happens when SCB is ready to transfer data and EMPTY is '1'. Only used in FIFO mode. (Note: This bit may be set unintentionally, even if the FIFO is not empty. Workaround: Ignore the bit when the clock frequency of the AHB bus is greater than 3x the internal frequency of SCB and the FIFO is not empty)

SCB6_INTR_TX: UNDERFLOW		
Field	**Rev 0E**	**Rev 0F**
F4Comment	Attempt to read from an empty TX FIFO. This happens when SCB is ready to transfer data and EMPTY is '1'. Only used in FIFO mode.	Attempt to read from an empty TX FIFO. This happens when SCB is ready to transfer data and EMPTY is '1'. Only used in FIFO mode. (Note: This bit may be set unintentionally, even if the FIFO is not empty. Workaround: Ignore the bit when the clock frequency of the AHB bus is greater than 3x the internal frequency of SCB and the FIFO is not empty)

SCB7_INTR_TX: UNDERFLOW		
Field	**Rev 0E**	**Rev 0F**
F4Comment	Attempt to read from an empty TX FIFO. This happens when SCB is ready to transfer data and EMPTY is '1'. Only used in FIFO mode.	Attempt to read from an empty TX FIFO. This happens when SCB is ready to transfer data and EMPTY is '1'. Only used in FIFO mode. (Note: This bit may be set unintentionally, even if the FIFO is not empty. Workaround: Ignore the bit when the clock frequency of the AHB bus is greater than 3x the internal frequency of SCB and the FIFO is not empty)

SCB8_INTR_TX: UNDERFLOW		
Field	**Rev 0E**	**Rev 0F**
F4Comment	Attempt to read from an empty TX FIFO. This happens when SCB is ready to transfer data and EMPTY is '1'. Only used in FIFO mode.	Attempt to read from an empty TX FIFO. This happens when SCB is ready to transfer data and EMPTY is '1'. Only used in FIFO mode. (Note: This bit may be set unintentionally, even if the FIFO is not empty. Workaround: Ignore the bit when the clock frequency of the AHB bus is greater than 3x the internal frequency of SCB and the FIFO is not empty)

SCB9_INTR_TX: UNDERFLOW		
Field	**Rev 0E**	**Rev 0F**
F4Comment	Attempt to read from an empty TX FIFO. This happens when SCB is ready to transfer data and EMPTY is '1'. Only used in FIFO mode.	Attempt to read from an empty TX FIFO. This happens when SCB is ready to transfer data and EMPTY is '1'. Only used in FIFO mode. (Note: This bit may be set unintentionally, even if the FIFO is not empty. Workaround: Ignore the bit when the clock frequency of the AHB bus is greater than 3x the internal frequency of SCB and the FIFO is not empty)

SCB10_INTR_TX: UNDERFLOW		
Field	**Rev 0E**	**Rev 0F**
F4Comment	Attempt to read from an empty TX FIFO. This happens when SCB is ready to transfer data and EMPTY is '1'. Only used in FIFO mode.	Attempt to read from an empty TX FIFO. This happens when SCB is ready to transfer data and EMPTY is '1'. Only used in FIFO mode. (Note: This bit may be set unintentionally, even if the FIFO is not empty. Workaround: Ignore the bit when the clock frequency of the AHB bus is greater than 3x the internal frequency of SCB and the FIFO is not empty)

SCB11_INTR_TX: UNDERFLOW		
Field	**Rev 0E**	**Rev 0F**
F4Comment	Attempt to read from an empty TX FIFO. This happens when SCB is ready to transfer data and EMPTY is '1'. Only used in FIFO mode.	Attempt to read from an empty TX FIFO. This happens when SCB is ready to transfer data and EMPTY is '1'. Only used in FIFO mode. (Note: This bit may be set unintentionally, even if the FIFO is not empty. Workaround: Ignore the bit when the clock frequency of the AHB bus is greater than 3x the internal frequency of SCB and the FIFO is not empty)

MIXER0_MIXER_DST_STRUCT_INTR_DST_MASKED: MIXER0_MIXER_DST_STRUCT_INTR_DST_MASKED		
Field	**Rev 0E**	**Rev 0F**
Retention	Retained	Not Retained

MIXER1_MIXER_DST_STRUCT_INTR_DST_MASKED: MIXER1_MIXER_DST_STRUCT_INTR_DST_MASKED		
Field	**Rev 0E**	**Rev 0F**
Retention	Retained	Not Retained

PASS0_SAR0_CH0_SAMPLE_CTL: SAMPLE_TIME		
Field	**Rev 0E**	**Rev 0F**
F1Comment	Sample time (aperture) in ADC clock cycles. Minimum is 1 (0 gives the same result as 1), minimum time needed for proper settling is at least 300ns, i.e. 6 clock cycles at the max frequency of 20MHz.	Sample time (aperture) in ADC clock cycles. Minimum is 1 (0 gives the same result as 1), minimum time needed for proper settling is at least 412ns, i.e.11 clock cycles at the max frequency of 26.7MHz.

PASS0_SAR0_CH0_RESULT: PASS0_SAR0_CH0_RESULT		
Field	**Rev 0E**	**Rev 0F**
Retention	Retained	Not Retained

PASS0_SAR0_CH1_SAMPLE_CTL: SAMPLE_TIME		
Field	**Rev 0E**	**Rev 0F**
F1Comment	Sample time (aperture) in ADC clock cycles. Minimum is 1 (0 gives the same result as 1), minimum time needed for proper settling is at least 300ns, i.e. 6 clock cycles at the max frequency of 20MHz.	Sample time (aperture) in ADC clock cycles. Minimum is 1 (0 gives the same result as 1), minimum time needed for proper settling is at least 412ns, i.e.11 clock cycles at the max frequency of 26.7MHz.

PASS0_SAR0_CH1_RESULT: PASS0_SAR0_CH1_RESULT		
Field	**Rev 0E**	**Rev 0F**
Retention	Retained	Not Retained

PASS0_SAR0_CH2_SAMPLE_CTL: SAMPLE_TIME		
Field	**Rev 0E**	**Rev 0F**
F1Comment	Sample time (aperture) in ADC clock cycles. Minimum is 1 (0 gives the same result as 1), minimum time needed for proper settling is at least 300ns, i.e. 6 clock cycles at the max frequency of 20MHz.	Sample time (aperture) in ADC clock cycles. Minimum is 1 (0 gives the same result as 1), minimum time needed for proper settling is at least 412ns, i.e.11 clock cycles at the max frequency of 26.7MHz.

PASS0_SAR0_CH2_RESULT: PASS0_SAR0_CH2_RESULT		
Field	**Rev 0E**	**Rev 0F**
Retention	Retained	Not Retained

PASS0_SAR0_CH3_SAMPLE_CTL: SAMPLE_TIME		
Field	**Rev 0E**	**Rev 0F**
F1Comment	Sample time (aperture) in ADC clock cycles. Minimum is 1 (0 gives the same result as 1), minimum time needed for proper settling is at least 300ns, i.e. 6 clock cycles at the max frequency of 20MHz.	Sample time (aperture) in ADC clock cycles. Minimum is 1 (0 gives the same result as 1), minimum time needed for proper settling is at least 412ns, i.e.11 clock cycles at the max frequency of 26.7MHz.

PASS0_SAR0_CH3_RESULT: PASS0_SAR0_CH3_RESULT		
Field	**Rev 0E**	**Rev 0F**
Retention	Retained	Not Retained

PASS0_SAR0_CH4_SAMPLE_CTL: SAMPLE_TIME		
Field	**Rev 0E**	**Rev 0F**
F1Comment	Sample time (aperture) in ADC clock cycles. Minimum is 1 (0 gives the same result as 1), minimum time needed for proper settling is at least 300ns, i.e. 6 clock cycles at the max frequency of 20MHz.	Sample time (aperture) in ADC clock cycles. Minimum is 1 (0 gives the same result as 1), minimum time needed for proper settling is at least 412ns, i.e.11 clock cycles at the max frequency of 26.7MHz.

PASS0_SAR0_CH4_RESULT: PASS0_SAR0_CH4_RESULT		
Field	**Rev 0E**	**Rev 0F**
Retention	Retained	Not Retained

PASS0_SAR0_CH5_SAMPLE_CTL: SAMPLE_TIME		
Field	**Rev 0E**	**Rev 0F**
F1Comment	Sample time (aperture) in ADC clock cycles. Minimum is 1 (0 gives the same result as 1), minimum time needed for proper settling is at least 300ns, i.e. 6 clock cycles at the max frequency of 20MHz.	Sample time (aperture) in ADC clock cycles. Minimum is 1 (0 gives the same result as 1), minimum time needed for proper settling is at least 412ns, i.e.11 clock cycles at the max frequency of 26.7MHz.

PASS0_SAR0_CH5_RESULT: PASS0_SAR0_CH5_RESULT		
Field	**Rev 0E**	**Rev 0F**
Retention	Retained	Not Retained

PASS0_SAR0_CH6_SAMPLE_CTL: SAMPLE_TIME		
Field	**Rev 0E**	**Rev 0F**
F1Comment	Sample time (aperture) in ADC clock cycles. Minimum is 1 (0 gives the same result as 1), minimum time needed for proper settling is at least 300ns, i.e. 6 clock cycles at the max frequency of 20MHz.	Sample time (aperture) in ADC clock cycles. Minimum is 1 (0 gives the same result as 1), minimum time needed for proper settling is at least 412ns, i.e.11 clock cycles at the max frequency of 26.7MHz.

PASS0_SAR0_CH6_RESULT: PASS0_SAR0_CH6_RESULT		
Field	**Rev 0E**	**Rev 0F**
Retention	Retained	Not Retained

PASS0_SAR0_CH7_SAMPLE_CTL: SAMPLE_TIME		
Field	**Rev 0E**	**Rev 0F**
F1Comment	Sample time (aperture) in ADC clock cycles. Minimum is 1 (0 gives the same result as 1), minimum time needed for proper settling is at least 300ns, i.e. 6 clock cycles at the max frequency of 20MHz.	Sample time (aperture) in ADC clock cycles. Minimum is 1 (0 gives the same result as 1), minimum time needed for proper settling is at least 412ns, i.e.11 clock cycles at the max frequency of 26.7MHz.

PASS0_SAR0_CH7_RESULT: PASS0_SAR0_CH7_RESULT		
Field	**Rev 0E**	**Rev 0F**
Retention	Retained	Not Retained

PASS0_SAR0_CH8_SAMPLE_CTL: SAMPLE_TIME		
Field	**Rev 0E**	**Rev 0F**
F1Comment	Sample time (aperture) in ADC clock cycles. Minimum is 1 (0 gives the same result as 1), minimum time needed for proper settling is at least 300ns, i.e. 6 clock cycles at the max frequency of 20MHz.	Sample time (aperture) in ADC clock cycles. Minimum is 1 (0 gives the same result as 1), minimum time needed for proper settling is at least 412ns, i.e.11 clock cycles at the max frequency of 26.7MHz.

PASS0_SAR0_CH8_RESULT: PASS0_SAR0_CH8_RESULT		
Field	**Rev 0E**	**Rev 0F**
Retention	Retained	Not Retained

PASS0_SAR0_CH9_SAMPLE_CTL: SAMPLE_TIME		
Field	**Rev 0E**	**Rev 0F**
F1Comment	Sample time (aperture) in ADC clock cycles. Minimum is 1 (0 gives the same result as 1), minimum time needed for proper settling is at least 300ns, i.e. 6 clock cycles at the max frequency of 20MHz.	Sample time (aperture) in ADC clock cycles. Minimum is 1 (0 gives the same result as 1), minimum time needed for proper settling is at least 412ns, i.e.11 clock cycles at the max frequency of 26.7MHz.

PASS0_SAR0_CH9_RESULT: PASS0_SAR0_CH9_RESULT		
Field	**Rev 0E**	**Rev 0F**
Retention	Retained	Not Retained

PASS0_SAR0_CH10_SAMPLE_CTL: SAMPLE_TIME		
Field	**Rev 0E**	**Rev 0F**
F1Comment	Sample time (aperture) in ADC clock cycles. Minimum is 1 (0 gives the same result as 1), minimum time needed for proper settling is at least 300ns, i.e. 6 clock cycles at the max frequency of 20MHz.	Sample time (aperture) in ADC clock cycles. Minimum is 1 (0 gives the same result as 1), minimum time needed for proper settling is at least 412ns, i.e.11 clock cycles at the max frequency of 26.7MHz.

PASS0_SAR0_CH10_RESULT: PASS0_SAR0_CH10_RESULT		
Field	**Rev 0E**	**Rev 0F**
Retention	Retained	Not Retained

PASS0_SAR0_CH11_SAMPLE_CTL: SAMPLE_TIME		
Field	**Rev 0E**	**Rev 0F**
F1Comment	Sample time (aperture) in ADC clock cycles. Minimum is 1 (0 gives the same result as 1), minimum time needed for proper settling is at least 300ns, i.e. 6 clock cycles at the max frequency of 20MHz.	Sample time (aperture) in ADC clock cycles. Minimum is 1 (0 gives the same result as 1), minimum time needed for proper settling is at least 412ns, i.e.11 clock cycles at the max frequency of 26.7MHz.

PASS0_SAR0_CH11_RESULT: PASS0_SAR0_CH11_RESULT		
Field	**Rev 0E**	**Rev 0F**
Retention	Retained	Not Retained

PASS0_SAR0_CH12_SAMPLE_CTL: SAMPLE_TIME		
Field	**Rev 0E**	**Rev 0F**
F1Comment	Sample time (aperture) in ADC clock cycles. Minimum is 1 (0 gives the same result as 1), minimum time needed for proper settling is at least 300ns, i.e. 6 clock cycles at the max frequency of 20MHz.	Sample time (aperture) in ADC clock cycles. Minimum is 1 (0 gives the same result as 1), minimum time needed for proper settling is at least 412ns, i.e.11 clock cycles at the max frequency of 26.7MHz.

PASS0_SAR0_CH12_RESULT: PASS0_SAR0_CH12_RESULT		
Field	**Rev 0E**	**Rev 0F**
Retention	Retained	Not Retained

PASS0_SAR0_CH13_SAMPLE_CTL: SAMPLE_TIME		
Field	**Rev 0E**	**Rev 0F**
F1Comment	Sample time (aperture) in ADC clock cycles. Minimum is 1 (0 gives the same result as 1), minimum time needed for proper settling is at least 300ns, i.e. 6 clock cycles at the max frequency of 20MHz.	Sample time (aperture) in ADC clock cycles. Minimum is 1 (0 gives the same result as 1), minimum time needed for proper settling is at least 412ns, i.e.11 clock cycles at the max frequency of 26.7MHz.

PASS0_SAR0_CH13_RESULT: PASS0_SAR0_CH13_RESULT		
Field	**Rev 0E**	**Rev 0F**
Retention	Retained	Not Retained

PASS0_SAR0_CH14_SAMPLE_CTL: SAMPLE_TIME		
Field	**Rev 0E**	**Rev 0F**
F1Comment	Sample time (aperture) in ADC clock cycles. Minimum is 1 (0 gives the same result as 1), minimum time needed for proper settling is at least 300ns, i.e. 6 clock cycles at the max frequency of 20MHz.	Sample time (aperture) in ADC clock cycles. Minimum is 1 (0 gives the same result as 1), minimum time needed for proper settling is at least 412ns, i.e.11 clock cycles at the max frequency of 26.7MHz.

PASS0_SAR0_CH14_RESULT: PASS0_SAR0_CH14_RESULT		
Field	**Rev 0E**	**Rev 0F**
Retention	Retained	Not Retained

PASS0_SAR0_CH15_SAMPLE_CTL: SAMPLE_TIME		
Field	**Rev 0E**	**Rev 0F**
F1Comment	Sample time (aperture) in ADC clock cycles. Minimum is 1 (0 gives the same result as 1), minimum time needed for proper settling is at least 300ns, i.e. 6 clock cycles at the max frequency of 20MHz.	Sample time (aperture) in ADC clock cycles. Minimum is 1 (0 gives the same result as 1), minimum time needed for proper settling is at least 412ns, i.e.11 clock cycles at the max frequency of 26.7MHz.

PASS0_SAR0_CH15_RESULT: PASS0_SAR0_CH15_RESULT		
Field	**Rev 0E**	**Rev 0F**
Retention	Retained	Not Retained

PASS0_SAR0_CH16_SAMPLE_CTL: SAMPLE_TIME		
Field	**Rev 0E**	**Rev 0F**
F1Comment	Sample time (aperture) in ADC clock cycles. Minimum is 1 (0 gives the same result as 1), minimum time needed for proper settling is at least 300ns, i.e. 6 clock cycles at the max frequency of 20MHz.	Sample time (aperture) in ADC clock cycles. Minimum is 1 (0 gives the same result as 1), minimum time needed for proper settling is at least 412ns, i.e.11 clock cycles at the max frequency of 26.7MHz.

PASS0_SAR0_CH16_RESULT: PASS0_SAR0_CH16_RESULT		
Field	**Rev 0E**	**Rev 0F**
Retention	Retained	Not Retained

PASS0_SAR0_CH17_SAMPLE_CTL: SAMPLE_TIME		
Field	**Rev 0E**	**Rev 0F**
F1Comment	Sample time (aperture) in ADC clock cycles. Minimum is 1 (0 gives the same result as 1), minimum time needed for proper settling is at least 300ns, i.e. 6 clock cycles at the max frequency of 20MHz.	Sample time (aperture) in ADC clock cycles. Minimum is 1 (0 gives the same result as 1), minimum time needed for proper settling is at least 412ns, i.e.11 clock cycles at the max frequency of 26.7MHz.

PASS0_SAR0_CH17_RESULT: PASS0_SAR0_CH17_RESULT		
Field	**Rev 0E**	**Rev 0F**
Retention	Retained	Not Retained

PASS0_SAR0_CH18_SAMPLE_CTL: SAMPLE_TIME		
Field	**Rev 0E**	**Rev 0F**
F1Comment	Sample time (aperture) in ADC clock cycles. Minimum is 1 (0 gives the same result as 1), minimum time needed for proper settling is at least 300ns, i.e. 6 clock cycles at the max frequency of 20MHz.	Sample time (aperture) in ADC clock cycles. Minimum is 1 (0 gives the same result as 1), minimum time needed for proper settling is at least 412ns, i.e.11 clock cycles at the max frequency of 26.7MHz.

PASS0_SAR0_CH18_RESULT: PASS0_SAR0_CH18_RESULT		
Field	**Rev 0E**	**Rev 0F**
Retention	Retained	Not Retained

PASS0_SAR0_CH19_SAMPLE_CTL: SAMPLE_TIME		
Field	**Rev 0E**	**Rev 0F**
F1Comment	Sample time (aperture) in ADC clock cycles. Minimum is 1 (0 gives the same result as 1), minimum time needed for proper settling is at least 300ns, i.e. 6 clock cycles at the max frequency of 20MHz.	Sample time (aperture) in ADC clock cycles. Minimum is 1 (0 gives the same result as 1), minimum time needed for proper settling is at least 412ns, i.e.11 clock cycles at the max frequency of 26.7MHz.

PASS0_SAR0_CH19_RESULT: PASS0_SAR0_CH19_RESULT		
Field	**Rev 0E**	**Rev 0F**
Retention	Retained	Not Retained

PASS0_SAR0_CH20_SAMPLE_CTL: SAMPLE_TIME		
Field	**Rev 0E**	**Rev 0F**
F1Comment	Sample time (aperture) in ADC clock cycles. Minimum is 1 (0 gives the same result as 1), minimum time needed for proper settling is at least 300ns, i.e. 6 clock cycles at the max frequency of 20MHz.	Sample time (aperture) in ADC clock cycles. Minimum is 1 (0 gives the same result as 1), minimum time needed for proper settling is at least 412ns, i.e.11 clock cycles at the max frequency of 26.7MHz.

PASS0_SAR0_CH20_RESULT: PASS0_SAR0_CH20_RESULT		
Field	**Rev 0E**	**Rev 0F**
Retention	Retained	Not Retained

PASS0_SAR0_CH21_SAMPLE_CTL: SAMPLE_TIME		
Field	**Rev 0E**	**Rev 0F**
F1Comment	Sample time (aperture) in ADC clock cycles. Minimum is 1 (0 gives the same result as 1), minimum time needed for proper settling is at least 300ns, i.e. 6 clock cycles at the max frequency of 20MHz.	Sample time (aperture) in ADC clock cycles. Minimum is 1 (0 gives the same result as 1), minimum time needed for proper settling is at least 412ns, i.e.11 clock cycles at the max frequency of 26.7MHz.

PASS0_SAR0_CH21_RESULT: PASS0_SAR0_CH21_RESULT		
Field	**Rev 0E**	**Rev 0F**
Retention	Retained	Not Retained

PASS0_SAR0_CH22_SAMPLE_CTL: SAMPLE_TIME		
Field	**Rev 0E**	**Rev 0F**
F1Comment	Sample time (aperture) in ADC clock cycles. Minimum is 1 (0 gives the same result as 1), minimum time needed for proper settling is at least 300ns, i.e. 6 clock cycles at the max frequency of 20MHz.	Sample time (aperture) in ADC clock cycles. Minimum is 1 (0 gives the same result as 1), minimum time needed for proper settling is at least 412ns, i.e.11 clock cycles at the max frequency of 26.7MHz.

PASS0_SAR0_CH22_RESULT: PASS0_SAR0_CH22_RESULT		
Field	**Rev 0E**	**Rev 0F**
Retention	Retained	Not Retained

PASS0_SAR0_CH23_SAMPLE_CTL: SAMPLE_TIME		
Field	**Rev 0E**	**Rev 0F**
F1Comment	Sample time (aperture) in ADC clock cycles. Minimum is 1 (0 gives the same result as 1), minimum time needed for proper settling is at least 300ns, i.e. 6 clock cycles at the max frequency of 20MHz.	Sample time (aperture) in ADC clock cycles. Minimum is 1 (0 gives the same result as 1), minimum time needed for proper settling is at least 412ns, i.e.11 clock cycles at the max frequency of 26.7MHz.

PASS0_SAR0_CH23_RESULT: PASS0_SAR0_CH23_RESULT		
Field	**Rev 0E**	**Rev 0F**
Retention	Retained	Not Retained

PASS0_SAR0_CH24_SAMPLE_CTL: SAMPLE_TIME		
Field	**Rev 0E**	**Rev 0F**
F1Comment	Sample time (aperture) in ADC clock cycles. Minimum is 1 (0 gives the same result as 1), minimum time needed for proper settling is at least 300ns, i.e. 6 clock cycles at the max frequency of 20MHz.	Sample time (aperture) in ADC clock cycles. Minimum is 1 (0 gives the same result as 1), minimum time needed for proper settling is at least 412ns, i.e.11 clock cycles at the max frequency of 26.7MHz.

PASS0_SAR0_CH24_RESULT: PASS0_SAR0_CH24_RESULT		
Field	**Rev 0E**	**Rev 0F**
Retention	Retained	Not Retained

PASS0_SAR0_CH25_SAMPLE_CTL: SAMPLE_TIME		
Field	**Rev 0E**	**Rev 0F**
F1Comment	Sample time (aperture) in ADC clock cycles. Minimum is 1 (0 gives the same result as 1), minimum time needed for proper settling is at least 300ns, i.e. 6 clock cycles at the max frequency of 20MHz.	Sample time (aperture) in ADC clock cycles. Minimum is 1 (0 gives the same result as 1), minimum time needed for proper settling is at least 412ns, i.e.11 clock cycles at the max frequency of 26.7MHz.

PASS0_SAR0_CH25_RESULT: PASS0_SAR0_CH25_RESULT		
Field	**Rev 0E**	**Rev 0F**
Retention	Retained	Not Retained

PASS0_SAR0_CH26_SAMPLE_CTL: SAMPLE_TIME		
Field	**Rev 0E**	**Rev 0F**
F1Comment	Sample time (aperture) in ADC clock cycles. Minimum is 1 (0 gives the same result as 1), minimum time needed for proper settling is at least 300ns, i.e. 6 clock cycles at the max frequency of 20MHz.	Sample time (aperture) in ADC clock cycles. Minimum is 1 (0 gives the same result as 1), minimum time needed for proper settling is at least 412ns, i.e.11 clock cycles at the max frequency of 26.7MHz.

PASS0_SAR0_CH26_RESULT: PASS0_SAR0_CH26_RESULT		
Field	**Rev 0E**	**Rev 0F**
Retention	Retained	Not Retained

PASS0_SAR0_CH27_SAMPLE_CTL: SAMPLE_TIME		
Field	**Rev 0E**	**Rev 0F**
F1Comment	Sample time (aperture) in ADC clock cycles. Minimum is 1 (0 gives the same result as 1), minimum time needed for proper settling is at least 300ns, i.e. 6 clock cycles at the max frequency of 20MHz.	Sample time (aperture) in ADC clock cycles. Minimum is 1 (0 gives the same result as 1), minimum time needed for proper settling is at least 412ns, i.e.11 clock cycles at the max frequency of 26.7MHz.

PASS0_SAR0_CH27_RESULT: PASS0_SAR0_CH27_RESULT		
Field	**Rev 0E**	**Rev 0F**
Retention	Retained	Not Retained

PASS0_SAR0_CH28_SAMPLE_CTL: SAMPLE_TIME		
Field	**Rev 0E**	**Rev 0F**
F1Comment	Sample time (aperture) in ADC clock cycles. Minimum is 1 (0 gives the same result as 1), minimum time needed for proper settling is at least 300ns, i.e. 6 clock cycles at the max frequency of 20MHz.	Sample time (aperture) in ADC clock cycles. Minimum is 1 (0 gives the same result as 1), minimum time needed for proper settling is at least 412ns, i.e.11 clock cycles at the max frequency of 26.7MHz.

PASS0_SAR0_CH28_RESULT: PASS0_SAR0_CH28_RESULT		
Field	**Rev 0E**	**Rev 0F**
Retention	Retained	Not Retained

PASS0_SAR0_CH29_SAMPLE_CTL: SAMPLE_TIME		
Field	**Rev 0E**	**Rev 0F**
F1Comment	Sample time (aperture) in ADC clock cycles. Minimum is 1 (0 gives the same result as 1), minimum time needed for proper settling is at least 300ns, i.e. 6 clock cycles at the max frequency of 20MHz.	Sample time (aperture) in ADC clock cycles. Minimum is 1 (0 gives the same result as 1), minimum time needed for proper settling is at least 412ns, i.e.11 clock cycles at the max frequency of 26.7MHz.

PASS0_SAR0_CH29_RESULT: PASS0_SAR0_CH29_RESULT		
Field	**Rev 0E**	**Rev 0F**
Retention	Retained	Not Retained

PASS0_SAR0_CH30_SAMPLE_CTL: SAMPLE_TIME		
Field	**Rev 0E**	**Rev 0F**
F1Comment	Sample time (aperture) in ADC clock cycles. Minimum is 1 (0 gives the same result as 1), minimum time needed for proper settling is at least 300ns, i.e. 6 clock cycles at the max frequency of 20MHz.	Sample time (aperture) in ADC clock cycles. Minimum is 1 (0 gives the same result as 1), minimum time needed for proper settling is at least 412ns, i.e.11 clock cycles at the max frequency of 26.7MHz.

PASS0_SAR0_CH30_RESULT: PASS0_SAR0_CH30_RESULT		
Field	**Rev 0E**	**Rev 0F**
Retention	Retained	Not Retained

PASS0_SAR0_CH31_SAMPLE_CTL: SAMPLE_TIME		
Field	**Rev 0E**	**Rev 0F**
F1Comment	Sample time (aperture) in ADC clock cycles. Minimum is 1 (0 gives the same result as 1), minimum time needed for proper settling is at least 300ns, i.e. 6 clock cycles at the max frequency of 20MHz.	Sample time (aperture) in ADC clock cycles. Minimum is 1 (0 gives the same result as 1), minimum time needed for proper settling is at least 412ns, i.e.11 clock cycles at the max frequency of 26.7MHz.

PASS0_SAR0_CH31_RESULT: PASS0_SAR0_CH31_RESULT		
Field	**Rev 0E**	**Rev 0F**
Retention	Retained	Not Retained

VIDEOSS0_MIPICSI0_MIPICSI_STRUCT_MIPICSI_WRAP_DPHY_CTL: ENP_DESER		
Field	**Rev 0E**	**Rev 0F**
F0Comment	To override the deserializer token detector and enable token detection in CIL. 1'b1: Sync token detection in the CIL. 1'b0: Sync token detection in the hard macro. For characterization and debug, we can disable this feature and enable it in the CIL (can be set to '1' for INT_LB, HSRX_SEQ and HSRX tests). With ENP_DESER=1 every lane operates independent, with ENP_DESER=0 all lanes at RX side will depend on lane 0 (default for CSI application).	To override the deserializer token detector and enable token detection in CIL. 1'b1: Sync token detection in the CIL. 1'b0: Sync token detection in the hard macro. For characterization and debug, we can disable this feature and enable it in the CIL (can be set to '1' for INT_LB, HSRX_SEQ and HSRX tests). With ENP_DESER=1 every lane operates independent, with ENP_DESER=0 all lanes at RX side will depend on lane 0 (default for CSI application). Note: Internal loopback test (INT_LB) shall use ENP_DESER=1.