TJA1021

ISO 17987/LIN 2.x/SAE J2602 transceiver

Rev. 9 — 10 February 2023 Product data sheet

1 General description

The TJA1021 is the interface between the Local Interconnect Network (LIN) commander/responder protocol controller and the physical bus in a LIN. It is primarily intended for in-vehicle sub-networks using baud rates from 1 kBd up to 20 kBd (/20 and B variants) and is compliant with LIN 2.0, LIN 2.1, LIN 2.2, LIN 2.2A, SAE J2602 and ISO 17987-4:2016 (12 V). The TJA1021 is pin-to-pin compatible with the TJA1020 and MC33662(B).

The transmit data stream of the protocol controller at the transmit data input (TXD) is converted by the TJA1021 into a bus signal with optimized slew rate and wave shaping to minimize ElectroMagnetic Emission (EME). The LIN bus output pin is pulled HIGH via an internal termination resistor. For a commander application, an external resistor in series with a diode should be connected between pin INH or pin V_{BAT} and pin LIN. The receiver detects the data stream at the LIN bus input pin and transfers it via pin RXD to the microcontroller.

In Sleep mode, the power consumption of the TJA1021 is very low. In failure modes, the power consumption is reduced to a minimum.

2 Features and benefits

2.1 General

- LIN 2.x/ISO 17987-4:2016 (12 V)/SAE J2602 compliant
- Baud rate up to 20 kBd (/20 and B variants)
- Very low ElectroMagnetic Emission (EME)
- High ElectroMagnetic Immunity (EMI)
- Passive behavior in unpowered state
- Input levels compatible with 3.3 V and 5 V devices
- Integrated termination resistor for LIN responder applications
- Wake-up source recognition (local or remote)
- K-line compatible
- Pin-to-pin compatible with TJA1020 and MC33662(B)
- Available in SO8 and HVSON8 packages
- Leadless HVSON8 package (3.0 mm × 3.0 mm) with low thermal resistance supporting Automated Optical Inspection (AOI) capability

2.2 Low power management

- Very low current consumption in Sleep mode with local and remote wake-up

2.3 Protection mechanisms

- High ESD robustness: ±6 kV according to IEC 61000-4-2 for pins LIN, V_{BAT} and WAKE_N
- Transmit data (TXD) dominant time-out function
- Bus terminal and battery pin protected against transients in the automotive environment (ISO 7637)
- Bus terminal short-circuit proof to battery and ground
- Thermally protected

3 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{BAT}	battery supply voltage	limiting value with respect to GND	-0.3	-	+40	V
I_{BAT}	battery supply current	Sleep mode; $V_{LIN} = V_{BAT}$; $V_{WAKE\_N} = V_{BAT}$; $V_{TXD} = 0$ V; $V_{SLP\_N} = 0$ V	2	7	10	µA
		Standby mode; bus recessive $V_{INH} = V_{BAT}$; $V_{LIN} = V_{BAT}$; $V_{WAKE\_N} = V_{BAT}$; $V_{TXD} = 0$ V; $V_{SLP\_N} = 0$ V	150	450	1000	µA
		Standby mode; bus dominant $V_{BAT} = 12$ V; $V_{INH} = 12$ V; $V_{LIN} = 0$ V; $V_{WAKE\_N} = 12$ V; $V_{TXD} = 0$ V; $V_{SLP\_N} = 0$ V	300	800	1200	µA
		Normal mode; bus recessive $V_{INH} = V_{BAT}$; $V_{LIN} = V_{BAT}$; $V_{WAKE\_N} = V_{BAT}$; $V_{TXD} = 5$ V; $V_{SLP\_N} = 5$ V	300	800	1600	µA
		Normal mode; bus dominant $V_{BAT} = 12$ V; $V_{INH} = 12$ V; $V_{WAKE\_N} = 12$ V; $V_{TXD} = 0$ V; $V_{SLP\_N} = 5$ V	1	2	4	mA
V_{LIN}	voltage on pin LIN	limiting value with respect to GND, V_{BAT} and V_{WAKE_N}	-40	-	+40	V
T_{vj}	virtual junction temperature	limiting value	-40	-	+150	°C

4 Ordering information

Table 2. Ordering information

Type number[1]	Package		
	Name	Description	Version
TJA1021T/10 TJA1021T/20 TJA1021AT TJA1021BT	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1
TJA1021TK/10 TJA1021TK/20 TJA1021ATK TJA1021BTK	HVSON8	plastic thermal enhanced very thin small outline package; no leads; 8 terminals; body 3 × 3 × 0.85 mm	SOT782-1

[1] TJA1021T(K)/10 and TJA1021AT(K): low slope variants supporting baud rates up to 10.4 kBd (SAE J2602); TJA1021T(K)/20 and TJA1021BT(K): normal slope variants supporting baud rates up to 20 kBd.

5 Block diagram

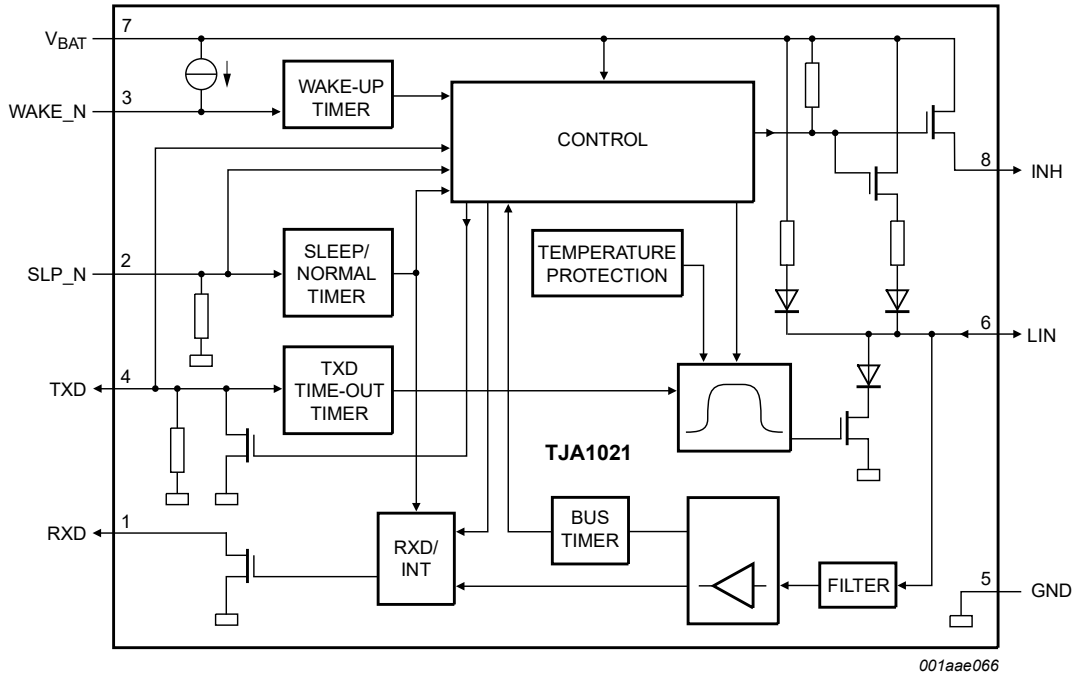


Figure 1. Block diagram

6 Pinning information

6.1 Pinning

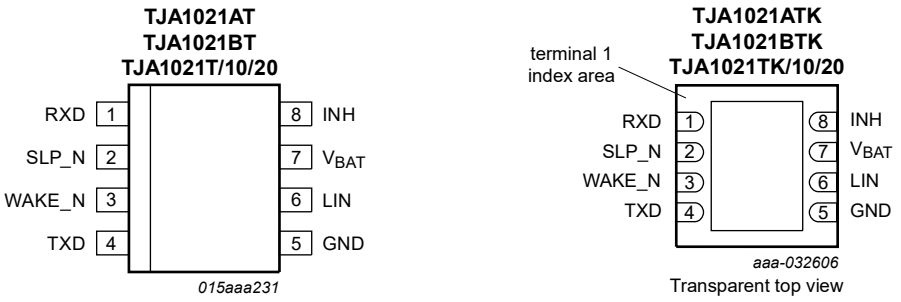


Figure 2. Pin configuration diagrams

6.2 Pin description

Table 3. Pin description

Symbol	Pin	Type[1]	Description
RXD	1	O	receive data output (open-drain); active LOW after a wake-up event
SLP_N	2	I	sleep control input (active LOW); controls inhibit output; resets wake-up source flag on TXD and wake-up request on RXD
WAKE_N	3	I	local wake-up input (active LOW); negative edge triggered
TXD	4	I	transmit data input; active LOW output after a local wake-up event
GND	5[2]	G	ground
LIN	6	AIO	LIN bus line input/output
V_{BAT}	7	P	battery supply voltage
INH	8	O	battery related inhibit output for controlling an external voltage regulator; active HIGH after a wake-up event

[1] I: digital input; O: digital output; AIO: analog input/output; P: power supply; G: ground.

[2] HVSON8 package die supply ground is connected to both the GND pin and the exposed center pad. The GND pin must be soldered to board ground. For enhanced thermal and electrical performance, it is recommended that the exposed center pad also be soldered to board ground.

7 Functional description

The TJA1021 is the interface between the LIN commander/responder protocol controller and the physical bus in a Local Interconnect Network (LIN). The TJA1021 is LIN 2.0, LIN 2.1, LIN 2.2, LIN 2.2A, SAE J2602 and ISO 17987-4:2016 (12 V) compliant and provides optimum ElectroMagnetic Compatibility (EMC) performance due to wave shaping of the LIN output.

The LIN physical layer is independent of higher OSI model layers (e.g., the LIN protocol). Consequently, nodes containing an ISO 17987-compliant physical layer can be combined, without restriction, with LIN physical layer nodes that comply with earlier revisions (LIN 1.0, LIN 1.1, LIN 1.2, LIN 1.3, LIN 2.0, LIN 2.1, LIN 2.2 and LIN 2.2A).

The TJA1021T(K)/20 and TJA1021B(K) are optimized for the maximum specified LIN transmission speed of 20 kBd; the TJA1021T(K)/10 and TJA1021AT(K) are optimized for the LIN transmission speed of 10.4 kBd as specified by the SAE J2602.

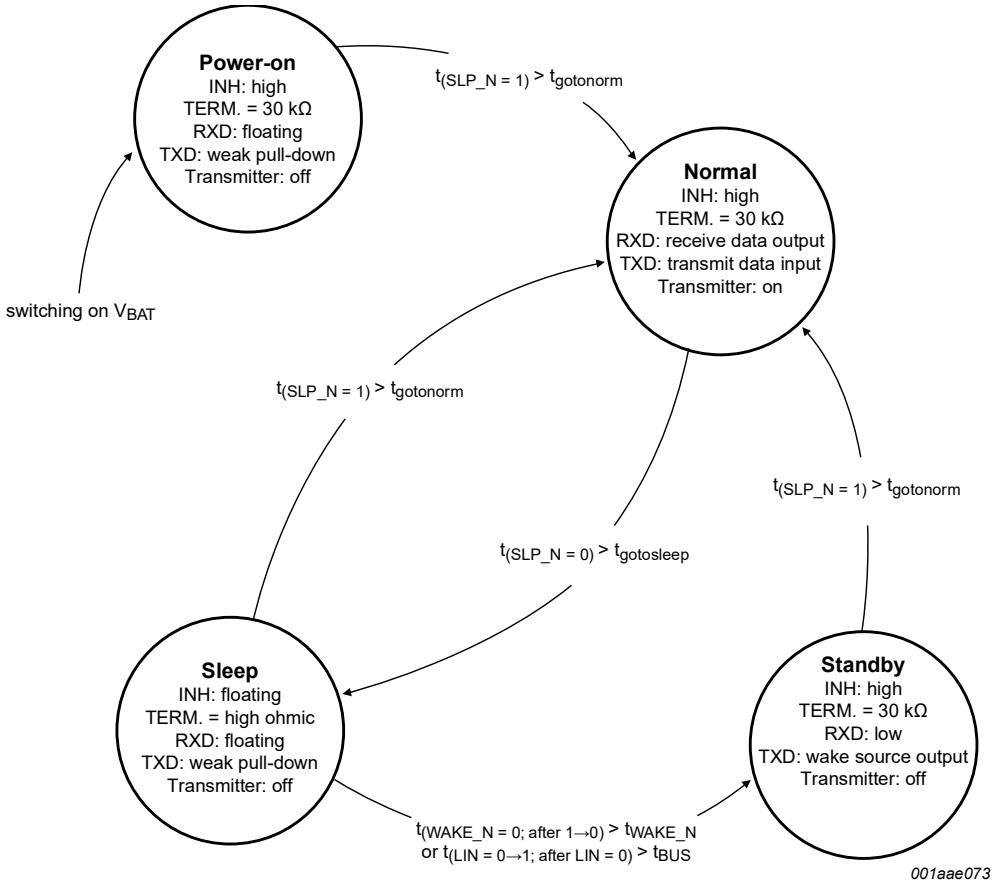
7.1 Operating modes

The TJA1021 supports modes for normal operation (Normal mode), power-up (Power-on mode) and very-low-power operation (Sleep mode). An intermediate wake-up mode between Sleep and Normal modes is also supported (Standby mode). Figure 3 shows the state diagram.

Table 4. Operating modes

Mode	SLP_N	TXD (output)	RXD	INH	Transmitter	Remarks
Sleep mode	0	weak pull-down	floating	floating	off	no wake-up request detected
Standby[1] mode	0	weak pull-down if remote wake-up; strong pull-down if local wake-up[2]	LOW[3]	HIGH	off	wake-up request detected; in this mode the microcontroller can read the wake-up source: remote or local wake-up
Normal mode	1	HIGH: recessive state LOW: dominant state	HIGH: recessive state LOW: dominant state	HIGH	Normal mode	[2][3][4]
Power-on mode	0	weak pull-down	floating	HIGH	off	[5]

[1] Standby mode is entered automatically upon any local or remote wake-up event during Sleep mode. Pin INH and the 30 kΩ termination resistor at pin LIN are switched on.
[2] The internal wake-up source flag (set if a local wake-up did occur and fed to pin TXD) will be reset after a positive edge on pin SLP_N.
[3] The wake-up interrupt (on pin RXD) is released after a positive edge on pin SLP_N.
[4] Normal mode is entered after a positive edge on SLP_N. As long as TXD is LOW, the transmitter is off. In the event of a short-circuit to ground on pin TXD, the transmitter will be disabled.
[5] Power-on mode is entered after switching on V_{BAT}.



TERM.: responder termination resistor, connected between pins LIN and V_{BAT}.

Figure 3. State diagram

7.2 Sleep mode

This mode is the most power-saving mode of the TJA1021. Despite its extreme low current consumption, the TJA1021 can still be woken up remotely via pin LIN, or woken up locally via pin WAKE_N, or activated directly via pin SLP_N. Filters at the inputs of the receiver (LIN), of pin WAKE_N and of pin SLP_N prevent unwanted wake-up events due to automotive transients or EMI. All wake-up events must be maintained for a certain time period ($t_{wake(dom)LIN}$, $t_{wake(dom)WAKE\_N}$ and $t_{gotonorm}$).

Sleep mode is initiated by a falling edge on pin SLP_N in Normal mode. To enter Sleep mode successfully (INH becomes floating), the sleep command (pin SLP_N = LOW) must be maintained for at least $t_{gotosleep}$.

In Sleep mode the internal responder termination between pins LIN and V_{BAT} is disabled to minimize the power dissipation in the event that pin LIN is short-circuited to ground. Only a weak pull-up between pins LIN and V_{BAT} is present.

Sleep mode can be activated independently from the actual level on pin LIN, pin TXD or pin WAKE_N. This guarantees that the lowest power consumption is achievable even in case of a continuous dominant level on pin LIN or a continuous LOW on pin WAKE_N.

When V_{BAT} drops below the power-on-reset threshold $V_{th(POR)L}$, the TJA1021 enters Sleep mode.

7.3 Standby mode

Standby mode is entered automatically whenever a local or remote wake-up occurs while the TJA1021 is in Sleep mode. These wake-up events activate pin INH and enable the responder termination resistor at the pin LIN. As a result of the HIGH condition on pin INH the voltage regulator and the microcontroller can be activated.

Standby mode is signalled by a LOW-level on pin RXD which can be used as an interrupt for the microcontroller.

In Standby mode (pin SLP_N is still LOW), the condition of pin TXD (weak pull-down or strong pull-down) indicates the wake-up source: weak pull-down for a remote wake-up request and strong pull-down for a local wake-up request.

Setting pin SLP_N HIGH during Standby mode results in the following events:

- An immediate reset of the wake-up source flag; thus releasing the possible strong pull-down at pin TXD before the actual mode change (after $t_{gotonorm}$) is performed
- A change into Normal mode if the HIGH level on pin SLP_N has been maintained for a certain time period ($t_{gotonorm}$)
- An immediate reset of the wake-up request signal on pin RXD

7.4 Normal mode

In Normal mode the TJA1021 is able to transmit and receive data via the LIN bus line. The receiver detects the data stream at the LIN bus input pin and transfers it via pin RXD to the microcontroller (see Figure 1): HIGH at a recessive level and LOW at a dominant level on the bus. The receiver has a supply-voltage related threshold with hysteresis and an integrated filter to suppress bus line noise. The transmit data stream of the protocol controller at the TXD input is converted by the transmitter into a bus signal with optimized slew rate and wave shaping to minimize EME. The LIN bus output pin is pulled HIGH via an internal responder termination resistor. For a commander application an external resistor in series with a diode should be connected between pin INH or V_{BAT} on one side and pin LIN on the other side (see Figure 7).

When in Sleep, Standby or Power-up mode, the TJA1021 enters Normal mode whenever a HIGH level on pin SLP_N is maintained for a time of at least $t_{gotonorm}$. The LIN transmit and receive functions are enabled after an initialization time, $t_{init(norm)}$.

The TJA1021 switches to Sleep mode in case of a LOW-level on pin SLP_N, maintained for a time of at least $t_{gotosleep}$.

7.5 Wake-up

When V_{BAT} exceeds the power-on-reset threshold voltage $V_{th(POR)H}$, the TJA1021 enters Power-on mode. Though the TJA1021 is powered-up and INH is HIGH, both the transmitter and receiver are still inactive. If SLP_N = 1 for $t > t_{gotonorm}$, the TJA1021 enters Normal mode.

There are three ways to wake-up a TJA1021 which is in Sleep mode:

1. Remote wake-up via a dominant bus state of at least $t_{wake(dom)LIN}$
2. Local wake-up via a negative edge at pin WAKE_N
3. Mode change (pin SLP_N is HIGH) from Sleep mode to Normal mode

7.6 Remote and local wake-up

A falling edge at pin LIN followed by a LOW level maintained for a certain time period ($t_{wake(dom)LIN}$) and a rising edge at pin LIN respectively (see Figure 4) results in a remote wake-up. It should be noted that the time period $t_{wake(dom)LIN}$ is measured either in Normal mode while TXD is HIGH, or in Sleep mode irrespective of the status of pin TXD.

A falling edge at pin WAKE_N followed by a LOW level maintained for a certain time period ($t_{wake(dom)WAKE\_N}$) results in a local wake-up. The pin WAKE_N provides an internal pull-up towards pin V_{BAT}. In order to prevent EMI issues, it is recommended to connect an unused pin WAKE_N to pin V_{BAT}.

After a local or remote wake-up, pin INH is activated (it goes HIGH) and the internal responder termination resistor is switched on. The wake-up request is indicated by a LOW active wake-up request signal on pin RXD to interrupt the microcontroller.

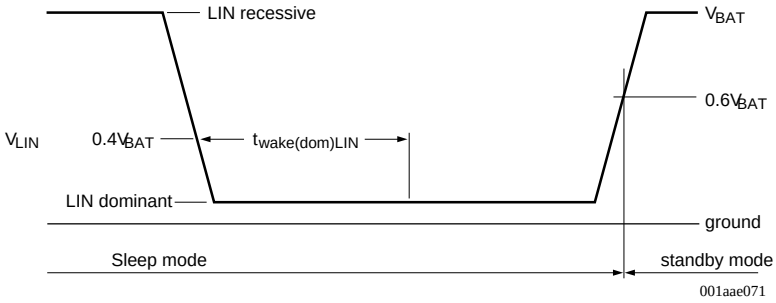


Figure 4. Remote wake-up behavior

7.7 Wake-up via mode transition

It is also possible to set pin INH HIGH with a mode transition towards Normal mode via pin SLP_N. This is useful for applications with a continuously powered microcontroller.

7.8 Wake-up source recognition

The TJA1021 can distinguish between a local wake-up request on pin WAKE_N and a remote wake-up request via a dominant bus state. 'A local wake-up request sets the wake-up source flag. The wake-up source can be read on pin TXD in the Standby mode. If an external pull-up resistor on pin TXD to the power supply voltage of the microcontroller has been added, a HIGH level indicates a remote wake-up request (weak pull-down at pin TXD) and a LOW level indicates a local wake-up request (strong pull-down at pin TXD; much stronger than the external pull-up resistor).

The wake-up request flag (signalled on pin RXD) as well as the wake-up source flag (signalled on pin TXD) are reset immediately after the microcontroller sets pin SLP_N HIGH.

7.9 TXD dominant time-out function

A TXD dominant time-out timer circuit prevents the bus line from being driven to a permanent dominant state (blocking all network communication) if pin TXD is forced permanently LOW by a hardware and/or software application failure. The timer is triggered by a negative edge on pin TXD. If the duration of the LOW-level on pin TXD

exceeds the internal timer value ($t_{to(dom)TXD}$), the transmitter is disabled, driving the bus line into a recessive state. The timer is reset by a positive edge on pin TXD.

7.10 Fail-safe features

Pin TXD provides a pull-down to GND in order to force a predefined level on input pin TXD in case the pin TXD is unsupplied.

Pin SLP_N provides a pull-down to GND in order to force the transceiver into Sleep mode in case the pin SLP_N is unsupplied.

Pin RXD is set floating in case of lost power supply on pin V_{BAT}.

The current of the transmitter output stage is limited in order to protect the transmitter against short circuit to pins V_{BAT} or GND.

A loss of power (pins V_{BAT} and GND) has no impact on the bus line and the microcontroller. There are no reverse currents from the bus. The LIN transceiver can be disconnected from the power supply without influencing the LIN bus.

The output driver at pin LIN is protected against overtemperature conditions. If the junction temperature exceeds the shutdown junction temperature $T_{j(sd)}$, the thermal protection circuit disables the output driver. The driver is enabled again when the junction temperature has dropped below $T_{j(sd)}$ and a recessive level is present at pin TXD.

If V_{BAT} drops below $V_{th(VBATL)L}$, a protection circuit disables the output driver. The driver is enabled again when $V_{BAT} > V_{th(VBATL)H}$ and a recessive level is present at pin TXD.

8 Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134); all voltages are referenced to ground; positive currents flow into the IC.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{BAT}	battery supply voltage[1]	with respect to GND	-0.3	+40	V
V_{TXD}	voltage on pin TXD[1]	I_{TXD} no limitation	-0.3	+6	V
		I_{TXD} < 500 µA	-0.3	+7	V
V_{RXD}	voltage on pin RXD[1]	I_{RXD} no limitation	-0.3	+6	V
		I_{RXD} < 500 µA	-0.3	+7	V
V_{SLP_N}	voltage on pin SLP_N[1]	I_{SLP_N} no limitation	-0.3	+6	V
		I_{SLP_N} < 500 µA	-0.3	+7	V
V_{LIN}	voltage on pin LIN[1]	with respect to GND, V_{BAT} and V_{WAKE_N}	-40	+40	V
V_{WAKE_N}	voltage on pin WAKE_N[1]		-0.3	+40	V
I_{WAKE_N}	current on pin WAKE_N	only relevant if $V_{WAKE\_N} < V_{GND}$ - 0.3 current will flow into pin GND	-15	-	mA
V_{INH}	voltage on pin INH[1]		-0.3	V_{BAT} +0.3	V
$I_{O(INH)}$	output current on pin INH		-50	+15	mA
V_{trt}	transient voltage	on pin V_{BAT} via reverse polarity diode/ capacitor; on pin LIN via 1 nF coupling capacitor [2]			
		pulse 1	-100	-	V
		pulse 2a	-	75	V
		pulse 3a	-150	-	V
		pulse 3b	-	100	V
V_{ESD}	electrostatic discharge voltage	IEC 61000-4-2 (150 pF, 330 Ω discharge circuit) [3]			
		on pins WAKE_N, LIN and V_{BAT}	-6	+6	kV
		Human Body Model (HBM)			
		on any pin [4]	-2	+2	kV
		on pins WAKE_N, LIN, V_{BAT} and INH [5]	-8	-8	kV
		Machine Model (MM); 200 pF, 0.75 µH, 10 Ω [6]			
		on any pin	-200	+200	V
		Charged Device Model (CDM) [7]			
		on any pin	-750	+750	V
T_{vj}	virtual junction temperature	[8]	-40	+150	°C
T_{stg}	storage temperature	[9]	-55	+150	°C

[1] The device can sustain voltages up to the specified values over the product lifetime, provided applied voltages (including transients) never exceed these values.

[2] Verified by an external test house according to LIN Conformance Test Specification Package for LIN 2.1; parameters for standard pulses defined in ISO 7637.

[3] Verified by an external test house according to LIN Conformance Test Specification Package for LIN 2.1.
[4] According to AEC-Q100-002.
[5] Pins stressed to reference group containing all ground and supply pins, emulating the application circuit (Figure 7). HBM pulse as specified in AEC-Q100-002 used.
[6] According to AEC-Q100-003.
[7] According to AEC-Q100-011.
[8] In accordance with IEC 60747-1. An alternative definition of virtual junction temperature is: $T_{vj} = T_{amb} + P \times R_{th(vj-a)}$, where $R_{th(vj-a)}$ is a fixed value to be used for the calculation of T_{vj}. The rating for T_{vj} limits the allowable combinations of power dissipation (P) and ambient temperature (T_{amb}).
[9] T_{stg} in application according to IEC61360-4. For component transport and storage conditions, see instead IEC61760-2.

9 Thermal characteristics

Table 6. Thermal characteristics

Value determined for free convection conditions on a JEDEC 2S2P board.

Symbol	Parameter	Conditions[1]	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	SO8 package; in free air	93	K/W
		HVSON8 package; in free air	54	K/W
$R_{th(j-c)}$	thermal resistance from junction to case	HVSON8 package; in free air	15	K/W
Ψ_{j-top}	thermal characterization parameter from junction to top of package	SO8 package; in free air	13	K/W
		HVSON8 package; in free air	7	K/W

[1] According to JEDEC JESD51-2, JESD51-5 and JESD51-7 at natural convection on 2s2p board. Board with two inner copper layers (thickness: 35 µm) and thermal via array under the exposed pad connected to the first inner copper layer (thickness: 70 µm).

10 Static characteristics

Table 7. Static characteristics

V_{BAT} = 5.5 V to 27 V; T_{vj} = -40 °C to +150 °C; $R_{L(LIN-VBAT)}$ = 500 Ω; typical values are given at V_{BAT} = 12 V unless otherwise specified; all voltages are defined with respect to ground; positive currents flow into the IC.[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply						
I_{BAT}	battery supply current	Sleep mode; $V_{LIN} = V_{BAT}$; $V_{WAKE\_N} = V_{BAT}$; V_{TXD} = 0 V; V_{SLP_N} = 0 V	2	7	10	µA
		Standby mode; bus recessive; $V_{INH} = V_{BAT}$; $V_{LIN} = V_{BAT}$; $V_{WAKE\_N} = V_{BAT}$; V_{TXD} = 0 V; V_{SLP_N} = 0 V	150	450	1000	µA
		Standby mode; bus dominant V_{BAT} = 12 V; V_{INH} = 12 V; V_{LIN} = 0 V; V_{WAKE_N} = 12 V; V_{TXD} = 0 V; V_{SLP_N} = 0 V	300	800	1200	µA
		Normal mode; bus recessive $V_{INH} = V_{BAT}$; $V_{LIN} = V_{BAT}$; $V_{WAKE\_N} = V_{BAT}$; V_{TXD} = 5 V; V_{SLP_N} = 5 V	300	800	1600	µA
		Normal mode; bus dominant V_{BAT} = 12 V; V_{INH} = 12 V; V_{WAKE_N} = 12 V; V_{TXD} = 0 V; V_{SLP_N} = 5 V	1	2	4	mA

Table 7. Static characteristics...*continued*

V_{BAT} = 5.5 V to 27 V; T_{vj} = -40 °C to +150 °C; $R_{L(LIN-VBAT)}$ = 500 Ω; typical values are given at V_{BAT} = 12 V unless otherwise specified; all voltages are defined with respect to ground; positive currents flow into the IC.[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Power-on reset						
$V_{th(POR)L}$	LOW-level power-on reset threshold voltage	power-on reset	1.6	3.1	3.9	V
$V_{th(POR)H}$	HIGH-level power-on reset threshold voltage		2.3	3.4	4.3	V
$V_{hys(POR)}$	power-on reset hysteresis voltage		0.05	0.3	1	V
$V_{th(VBATL)L}$	LOW-level V_{BAT} LOW threshold voltage		3.9	4.4	4.7	V
$V_{th(VBATL)H}$	HIGH-level V_{BAT} LOW threshold voltage		4.2	4.7	4.9	V
$V_{hys(VBATL)}$	V_{BAT} LOW hysteresis voltage		0.05	0.3	1	V
Pin TXD						
V_{IH}	HIGH-level input voltage		2	-	7	V
V_{IL}	LOW-level input voltage		-0.3	-	+0.8	V
V_{hys}	hysteresis voltage		50	200	400	mV
$R_{PD(TXD)}$	pull-down resistance on pin TXD	V_{TXD} = 5 V	140	500	1200	kΩ
I_{IL}	LOW-level input current	V_{TXD} = 0 V	-5	-	+5	µA
I_{OL}	LOW-level output current	local wake-up request Standby mode; V_{WAKE_N} = 0 V; $V_{LIN} = V_{BAT}$; V_{TXD} = 0.4 V	1.5	-	-	mA
Pin SLP_N						
V_{IH}	HIGH-level input voltage		2	-	7	V
V_{IL}	LOW-level input voltage		-0.3	-	+0.8	V
V_{hys}	hysteresis voltage		50	200	400	mV
$R_{PD(SLP\_N)}$	pull-down resistance on pin SLP_N	V_{SLP_N} = 5 V	140	500	1200	kΩ
I_{IL}	LOW-level input current	V_{SLP_N} = 0 V	-5	0	+5	µA
Pin RXD (open-drain)						
I_{OL}	LOW-level output current	Normal mode V_{LIN} = 0 V; V_{RXD} = 0.4 V	1.5	-	-	mA
I_{LH}	HIGH-level leakage current	Normal mode $V_{LIN} = V_{BAT}$; V_{RXD} = 5 V	-5	0	+5	µA
Pin WAKE_N						
V_{IH}	HIGH-level input voltage		V_{BAT} - 1	-	V_{BAT} + 0.3	V
V_{IL}	LOW-level input voltage		-0.3	-	V_{BAT} - 3.3	V
$I_{pu(L)}$	LOW-level pull-up current	V_{WAKE_N} = 0 V	-30	-12	-1	µA

Table 7. Static characteristics*...continued*

V_{BAT} = 5.5 V to 27 V; T_{vj} = -40 °C to +150 °C; $R_{L(LIN-VBAT)}$ = 500 Ω; typical values are given at V_{BAT} = 12 V unless otherwise specified; all voltages are defined with respect to ground; positive currents flow into the IC.[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{LH}	HIGH-level leakage current	V_{WAKE_N} = 27 V; V_{BAT} = 27 V	-5	0	+5	µA
Pin INH						
$R_{sw(VBAT-INH)}$	switch-on resistance between pins V_{BAT} and INH	Standby; Normal and Power-on modes; I_{INH} = -15 mA; V_{BAT} = 12 V	-	20	50	Ω
I_{LH}	HIGH-level leakage current	Sleep mode V_{INH} = 27 V; V_{BAT} = 27 V	-5	0	+5	µA
Pin LIN						
I_{BUS_LIM}	current limitation for driver dominant state	V_{BAT} = 18 V; V_{LIN} = 18 V; V_{TXD} = 0 V	40	-	100	mA
R_{pu}	pull-up resistance	Sleep mode; V_{SLP_N} = 0 V	50	160	250	kΩ
$I_{BUS\_PAS\_rec}$	receiver recessive input leakage current	V_{LIN} = 27 V; V_{BAT} = 5.5 V; V_{TXD} = 5 V	-	-	1	µA
$I_{BUS\_PAS\_dom}$	receiver dominant input leakage current including pull-up resistor	Normal mode; V_{TXD} = 5 V; V_{LIN} = 0 V; V_{BAT} = 12 V	-600	-	-	µA
$V_{SerDiode}$	voltage drop at the serial diode	in pull-up path with R_{res}; $I_{SerDiode}$ = 10 µA [2]	0.4	-	1.0	V
$I_{BUS\_NO\_GND}$	loss-of-ground bus current	V_{BAT} = 27 V; V_{LIN} = 0 V	-750	-	+10	µA
$I_{BUS\_NO\_BAT}$	loss-of-battery bus current	V_{BAT} = 0 V; V_{LIN} = 27 V	-	-	1	µA
V_{BUSdom}	receiver dominant state		-	-	$0.4V_{BAT}$	V
V_{BUSrec}	receiver recessive state		$0.6V_{BAT}$	-	-	V
V_{BUS_CNT}	receiver center voltage	V_{BUS_CNT} = (V_{BUSrec} + V_{BUSdom}) / 2	$0.475V_{BAT}$	$0.5V_{BAT}$	$0.525V_{BAT}$	V
V_{HYS}	receiver hysteresis voltage	V_{HYS} = V_{BUSrec} - V_{BUSdom}	-	-	$0.175V_{BAT}$	V
R_{res}	responder resistance	connected between pins LIN and V_{BAT}; V_{LIN} = 0 V; V_{BAT} = 12 V	20	30	47	kΩ
C_{LIN}	capacitance on pin LIN	[2]	-	-	30	pF
$V_{o(dom)}$	dominant output voltage	Normal mode; V_{TXD} = 0 V; V_{BAT} = 7.0 V	-	-	1.4	V
		Normal mode; V_{TXD} = 0 V; V_{BAT} = 18 V	-	-	2.0	V
Thermal shutdown						
$T_{j(sd)}$	shutdown junction temperature	[2]	150	175	200	°C

[1] All parameters are guaranteed over the virtual junction temperature range by design. Factory testing uses correlated test conditions to cover the specified temperature and power supply voltage range.

[2] Not tested in production; guaranteed by design.

11 Dynamic characteristics

Table 8. Dynamic characteristics

V_{BAT} = 5.5 V to 18 V; T_{vj} = -40 °C to +150 °C; $R_{L(LIN-VBAT)}$ = 500 Ω; typical values are given at V_{BAT} = 12 V, see Figure 6, unless otherwise specified; all voltages are defined with respect to ground.[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Duty cycles						
δ1	duty cycle 1	$V_{th(rec)(max)}$ = 0.744 × V_{BAT}; $V_{th(dom)(max)}$ = 0.581 × V_{BAT}; t_{bit} = 50 µs; V_{BAT}= 7 V to 18 V [2][3][4][5]	0.396	-	-	
		$V_{th(rec)(max)}$ = 0.76 × V_{BAT}; $V_{th(dom)(max)}$ = 0.593 × V_{BAT}; t_{bit} = 50 µs; V_{BAT} = 5.5 V to 7.0 V [2][3][4][5]	0.396	-	-	
δ2	duty cycle 2	$V_{th(rec)(min)}$ = 0.422 × V_{BAT}; $V_{th(dom)(min)}$ = 0.284 × V_{BAT}; t_{bit} = 50 µs; V_{BAT} = 7.6 V to 18 V [2][4][6][5]	-	-	0.581	
		$V_{th(rec)(min)}$ = 0.41 × V_{BAT}; $V_{th(dom)(min)}$ = 0.275 × V_{BAT}; t_{bit} = 50 µs; V_{BAT} = 6.1 V to 7.6 V [2][4][6][5]	-	-	0.581	
δ3	duty cycle 3	$V_{th(rec)(max)}$ = 0.778 × V_{BAT}; $V_{th(dom)(max)}$ = 0.616 × V_{BAT}; t_{bit} = 96 µs; V_{BAT}= 7 V to 18 V [3][4][5]	0.417	-	-	
		$V_{th(rec)(max)}$ = 0.797 × V_{BAT}; $V_{th(dom)(max)}$ = 0.630 × V_{BAT}; t_{bit} = 96 µs; V_{BAT} = 5.5 V to 7 V [3][4][5]	0.417	-	-	
δ4	duty cycle 4	$V_{th(rec)(min)}$ = 0.389 × V_{BAT}; $V_{th(dom)(min)}$ = 0.251 × V_{BAT}; t_{bit} = 96 µs; V_{BAT} = 7.6 V to 18 V [4][6][5]	-	-	0.590	
		$V_{th(rec)(min)}$ = 0.378 × V_{BAT}; $V_{th(dom)(min)}$ = 0.242 × V_{BAT}; t_{bit} = 96 µs; V_{BAT} = 6.1 V to 7.6 V [4][6][5]	-	-	0.590	
Timing characteristics						
t_f	fall time	[2][4]	-	-	22.5	µs
t_r	rise time	[2][4]	-	-	22.5	µs
$\Delta t_{(r-f)}$	difference between rise and fall time	V_{BAT} = 7.3 V [2][4]	-5	-	+5	µs
t_{tx_pd}	transmitter propagation delay	rising and falling [2]	-	-	6	µs
t_{tx_sym}	transmitter propagation delay symmetry	[2]	-2.5	-	+2.5	µs
t_{rx_pd}	receiver propagation delay	rising and falling [7]	-	-	6	µs
t_{rx_sym}	receiver propagation delay symmetry	[7]	-2	-	+2	µs
$t_{wake(dom)LIN}$	LIN dominant wake-up time	Sleep mode [8]	30	80	150	µs

Table 8. Dynamic characteristics...*continued*

V_{BAT} = 5.5 V to 18 V; T_{vj} = -40 °C to +150 °C; $R_{L(LIN-VBAT)}$ = 500 Ω; typical values are given at V_{BAT} = 12 V, see Figure 6, unless otherwise specified; all voltages are defined with respect to ground.[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{wake(dom)WAKE\_N}$	dominant wake-up time on pin WAKE_N	Sleep modec [9]	7	30	50	µs
$t_{gotonorm}$	go to normal time	time period for mode change from Sleep, Power-on or Standby mode to Normal mode [10]	2	5	10	µs
$t_{init(norm)}$	normal mode initialization time	[11]	5	-	20	µs
$t_{gotosleep}$	go to sleep time	time period for mode change from Normal mode to Sleep mode [10]	2	5	10	µs
$t_{to(dom)TXD}$	TXD dominant time-out time	V_{TXD} = 0 V [12]	27	55	90	ms

[1] All parameters are guaranteed over the virtual junction temperature range by design. Factory testing uses correlated test conditions to cover the specified temperature and power supply voltage range.

[2] Not applicable for the /10 or A variants of the TJA1021.

[3] $\delta 1, \delta 3 = \frac{t_{bus(rec)(min)}}{2 \times t_{bit}}$. Variable $t_{bus(rec)(min)}$ is illustrated in the LIN timing diagram in Figure 6.

[4] Bus load conditions are: C_{BUS} = 1 nF and R_{BUS} = 1 kΩ; C_{BUS} = 6.8 nF and R_{BUS} = 660 Ω; C_{BUS} = 10 nF and R_{BUS} = 500 Ω.

[5] For V_{BAT} > 18 V the LIN transmitter might be suppressed. If TXD is HIGH then the LIN transmitter output is recessive.

[6] $\delta 2, \delta 4 = \frac{t_{bus(rec)(max)}}{2 \times t_{bit}}$. Variable $t_{bus(rec)(max)}$ is illustrated in the LIN timing diagram in Figure 6.

[7] Load condition pin RXD: C_{RXD} = 20 pF and R_{RXD} = 2.4 kΩ.

[8] A falling edge on pin LIN, folllowed by LOW level of least t_{max}, followed by a rising edge on pin LIN is guranteed to trigger a remote wake-up (see Section 7.6. A LOW level of less than t_{min} will not trigger a wake-up event.

[9] A falling edge on pin WAKE_N, folllowed by a LOW level of least t_{max} is guranteed to trigger a local wake-up (Section 7.6). A LOW level of less than t_{min} will not trigger a wake-up event.

[10] Mode change is guaranteed to have been completed after t_{max} and will not be completed before t_{min}.

[11] LIN transmit and receive functions are guaranteed to have been enabled after t_{max} and will not be enabled before t_{min}.

[12] Time-out is guaranteed to have been triggered after t_{max} and will not be triggered before t_{min}.

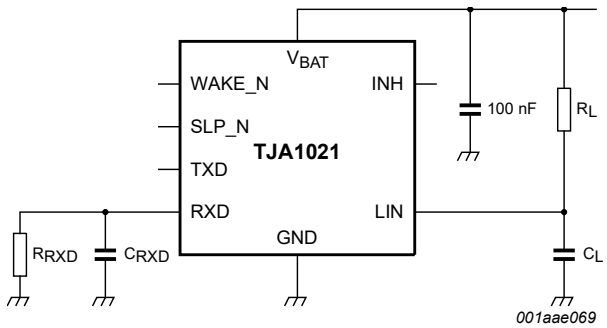


Figure 5. Timing test circuit for LIN transceiver

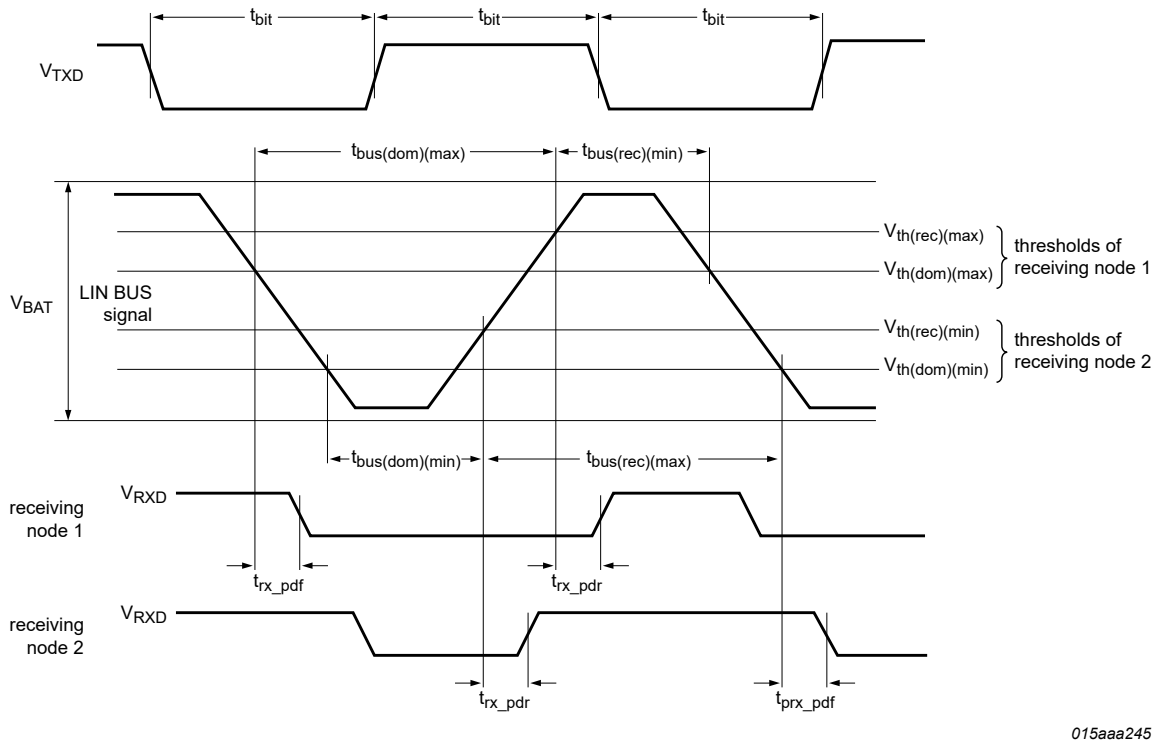
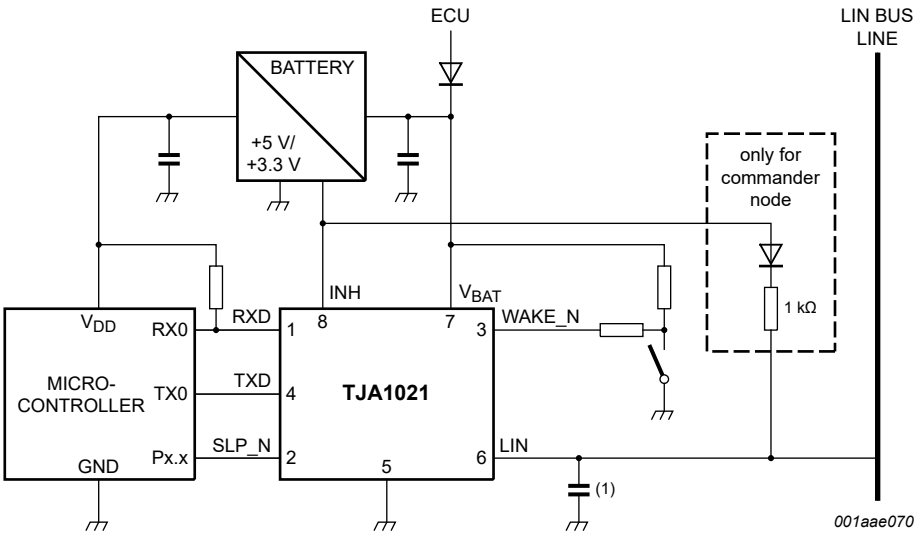


Figure 6. Timing diagram LIN transceiver

12 Application information

The minimum external circuitry needed with the TJA1021 is shown in Figure 7. See the Application Hints (Section 12.1) for further information about external components and PCB layout requirements.



1. Typically specified by car manufacturer, e.g. commander: C = 1 nF; responder: C = 220 pF.

Figure 7. Typical application of the TJA1021

12.1 Application hints

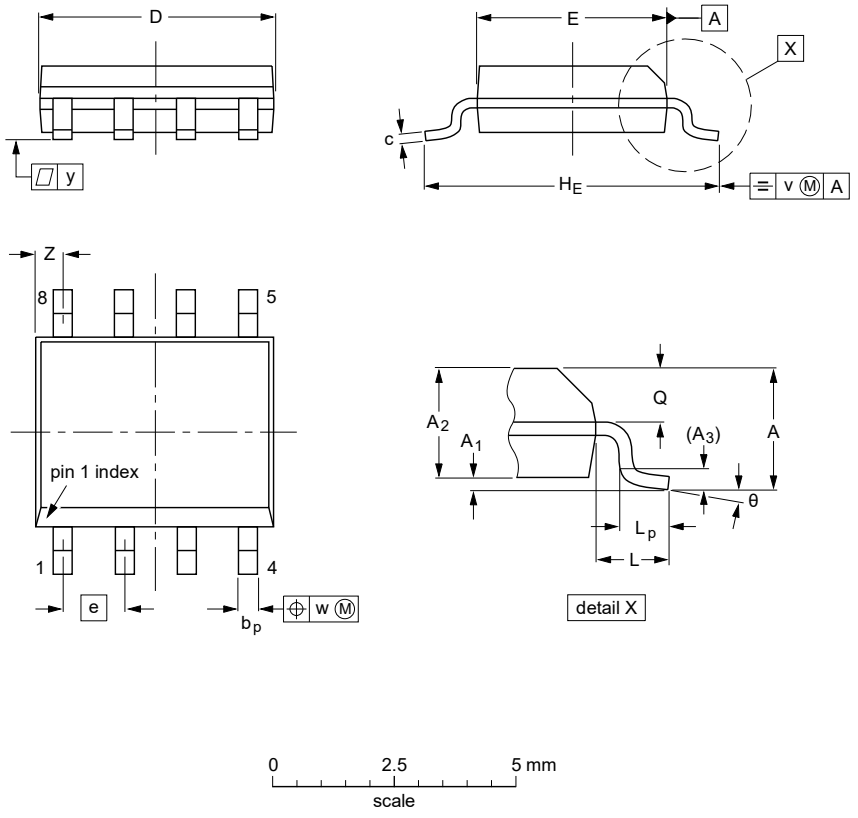
Further information on the application of the TJA1021 can be found in NXP application hints *AH1103 Application Hints - LIN transceiver TJA1021/TJA1022/TJA1024/TJA1027/TJA1029*.

13 Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard *Q100 Rev-G - Failure mechanism based stress test qualification for integrated circuits*, and is suitable for use in automotive applications.

14 Package outline

SO8: plastic small outline package; 8 leads; body width 3.9 mm **SOT96-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

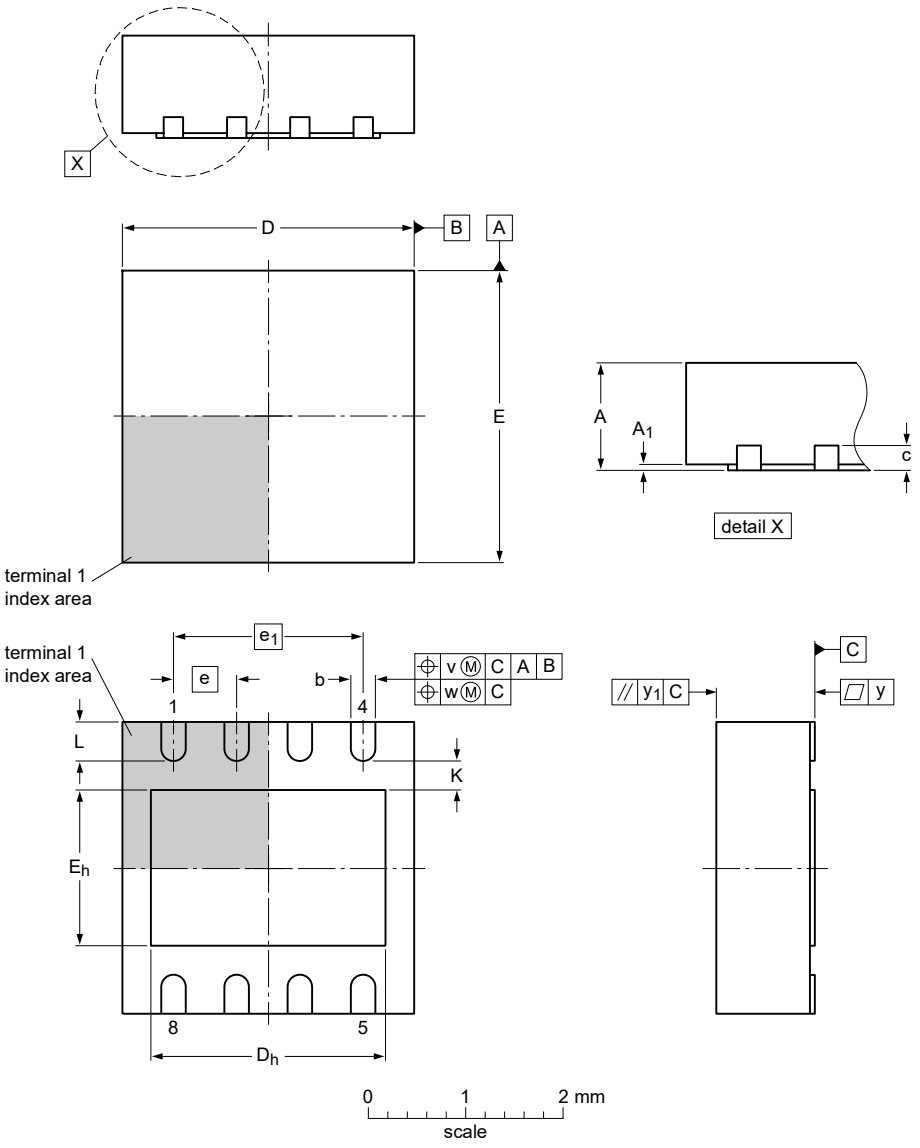
Notes

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT96-1	076E03	MS-012				~~99-12-27~~ 03-02-18

Figure 8. Package outline SOT96-1 (SO8)

HVSON8: plastic thermal enhanced very thin small outline package; no leads; 8 terminals; body 3 x 3 x 0.85 mm **SOT782-1**



Dimensions

Unit(1)		A	A_1	b	c	D	D_h	E	E_h	e	e_1	K	L	v	w	y	y_1
mm	max	1.00	0.05	0.35		3.10	2.45	3.10	1.65			0.35	0.45				
	nom	0.85	0.03	0.30	0.2	3.00	2.40	3.00	1.60	0.65	1.95	0.30	0.40	0.1	0.05	0.05	0.1
	min	0.80	0.00	0.25		2.90	2.35	2.90	1.55			0.25	0.35				

Note
1. Plastic or metal protrusions of 0.075 maximum per side are not included.

sot782-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT782-1	- - -	MO-229	- - -			~~09-08-25~~ 09-08-28

Figure 9. Package outline SOT782-1 (HVSON8)

15 Handling information

All input and output pins are protected against ElectroStatic Discharge (ESD) under normal handling. When handling ensure that the appropriate precautions are taken as described in *JESD625-A* or equivalent standards.

16 Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

16.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

16.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

16.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

16.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 10) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 9 and Table 10

Table 9. SnPb eutectic process (from J-STD-020D)

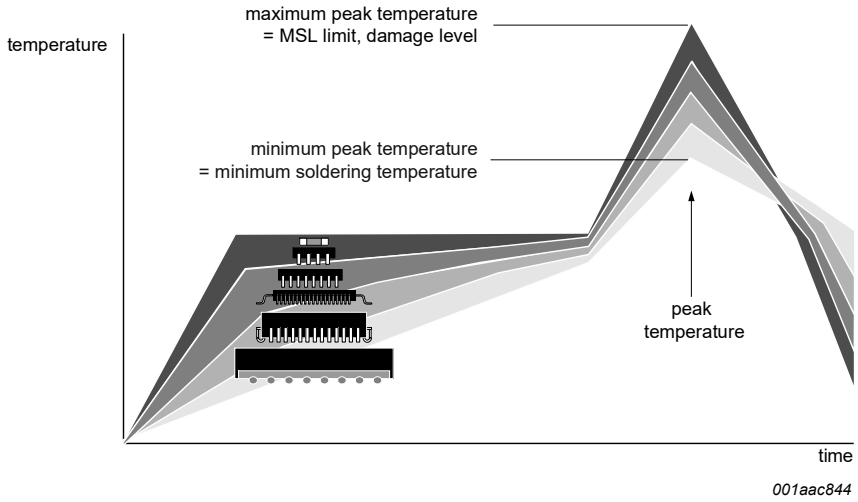
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm³)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 10. Lead-free process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm³)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 10.



MSL: Moisture Sensitivity Level

Figure 10. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

17 Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TJA1021 v.9	20230210	Product data sheet		TJA1021 v.8
Modifications:	• Added variants TJA1021AT(K) and TJA1021BT(K) • 'master/slave' replaced by 'commander/responder' throughout document • Table 3: added pin type column • Table 5: format and footnotes revised; V_{trt}, transient voltage specification, added • Table 6: parameter definitions and specifications updated • Table 8: footnotes added • Section 12: : introductory paragraph added • Section 12.1: added • Section 13: updated • Section 18: legal information updated			
TJA1021 v.8	20181218	Product data sheet	-	TJA1021 v.7
TJA1021 v.7	20110325	Product data sheet	-	TJA1021 v.6
TJA1021 v.6	20101230	Product data sheet	-	TJA1021 v.5
TJA1021 v.5	20091022	Product data sheet	-	TJA1021 v.4
TJA1021 v.4	20090119	Product data sheet	-	TJA1021 v.3
TJA1021 v.3	20071008	Product data sheet	-	TJA1021 v.2
TJA1021 v.2	20070903	Preliminary data sheet	-	TJA1021 v.1
TJA1021 v.1	20061016	Objective data sheet	-	-

18 Legal information

18.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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