# Ethernet Training – Session II
# Frame format, Auto-negotiation, Auto-MDIX & Introduction to MII layers

Pavel-Ioan Duta (IFAG ATV MC TM CES1)
Merwin Ebenezer (IFINS ATV MC TM PEW)
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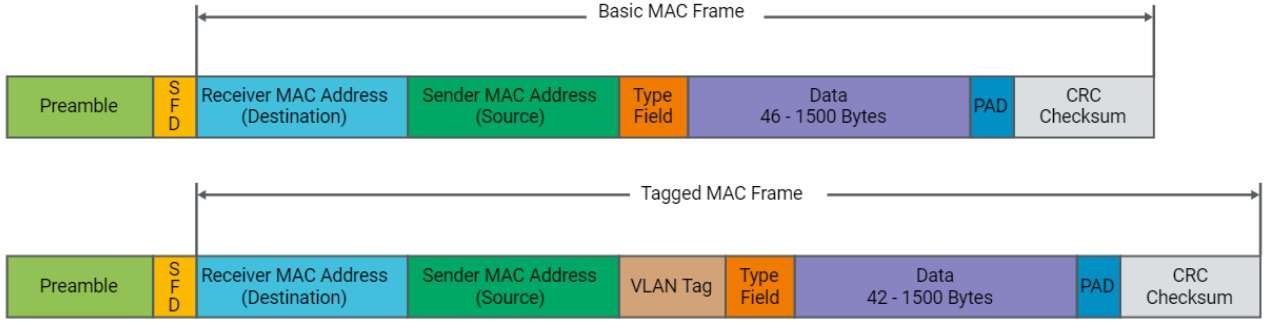
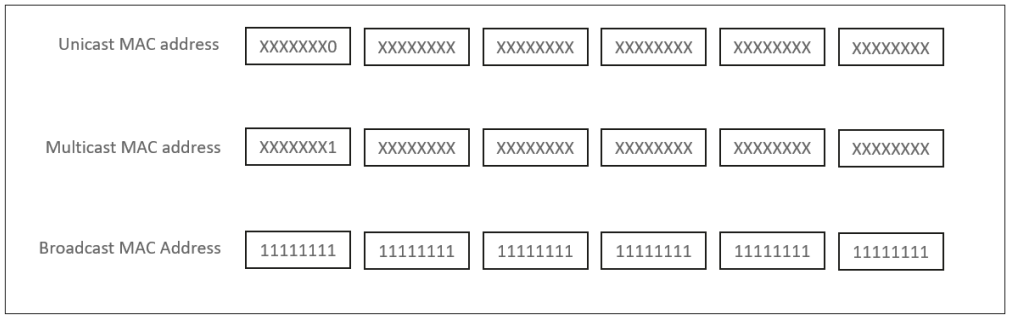
# Ethernet Frame Format

The skeleton of a standard Ethernet Frame can be decomposed into

- Preamble + Start-of-Frame Delimiter - 8 bytes (7*0xAA + 1*0xAB)
- Destination MAC Address (DA) - 6 bytes
- Source MAC Address (SA) - 6 bytes
- 802.1Q – VLAN Tag - 4 bytes (opt)
- Ether-Type/Length (T/L) - 2 bytes
- Data Payload - 46 to 1500 bytes
- Frame Check Sequence (CRC/FCS) - 4 bytes

Total frame size (excluding Preamble + SFD) - 64 to 1522 bytes



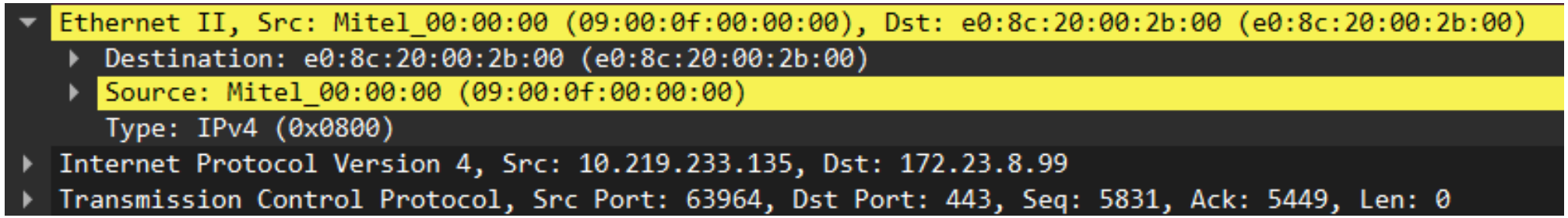




Infineon Technologies OUI – **00:03:19**:XX:XX:XX

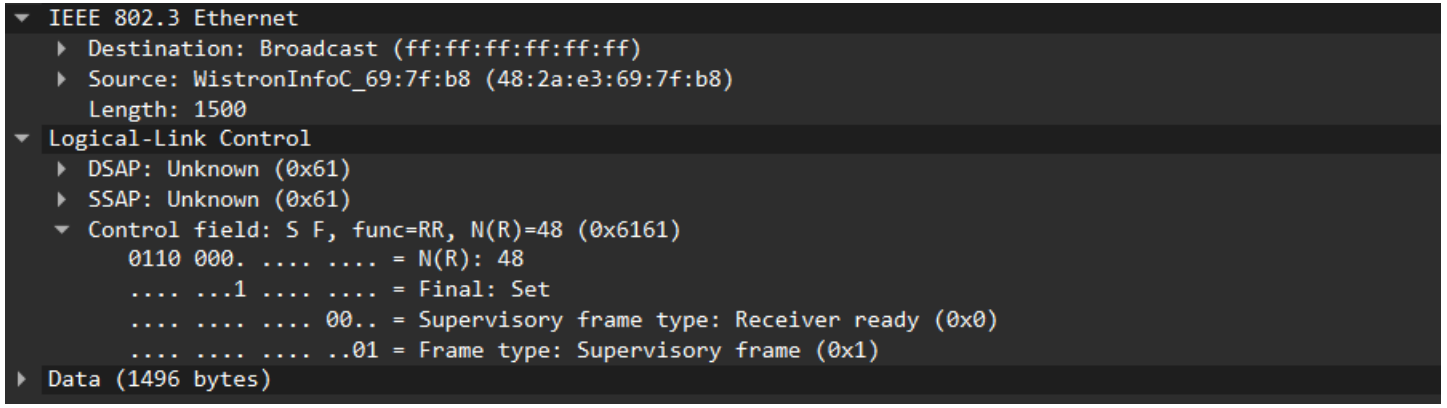
Multicast Address* – 01:80:C2:00:00:01

| Type Field | Description |
|---|---|
| 0x0800 | Payload contains IPv4 packet |
| 0x0806 | Payload contains ARP packet |
| 0x22F0 | Audio/Video Transport Protocol (AVTP) |
| 0x22EA | Multiple Stream Registration Protocol (MSRP) |
| 0x8100 | Ethernet VLAN Frame, Ether Type follows after tag |
| 0x86DD | Payload contains IPv6 packet |
| 0x88F5 | Multiple VLAN Registration Protocol (MVRP) |
| 0x88F6 | Multiple MAC Registration Protocol (MMRP) |
| 0x88F7 | Precision Time Protocol (PTP) |
| ... | ... |

# Ethernet-II Frame example




# IEEE 802.3 Ethernet Frame example




*Note: Almost all the applications uses Ethernet-II Frame format*

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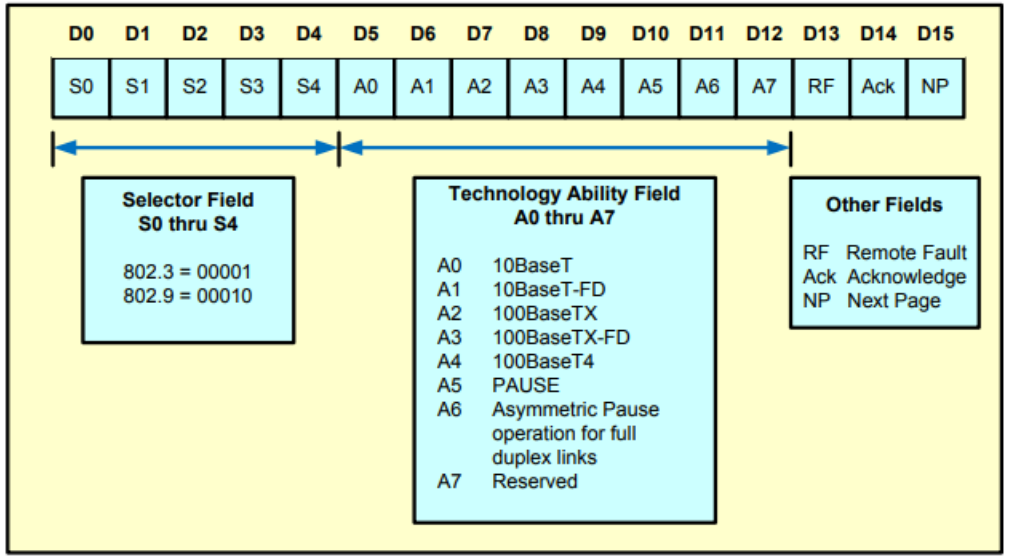
# Auto-negotiation

1) Auto-negotiation is a mechanism where a network device can advertise its capabilities and learn the capabilities of the remote link partner.

2) It leverages the Link Integrity Pulses (LIT) or NLP (Normal Link Pulse) and FLP bursts (Fast Link Pulse) to achieve this.
   - NLP (Normal Link Pulse) – Single Pulse for every 16ms when the Transmission is idle to keep the link alive. (like a heartbeat pulse)
   - FLP (Fast Link Pulse) – 33 pulses every 16ms, initially used in 100Base-TX now used in Auto-negotiation (16 data + 17 clock)

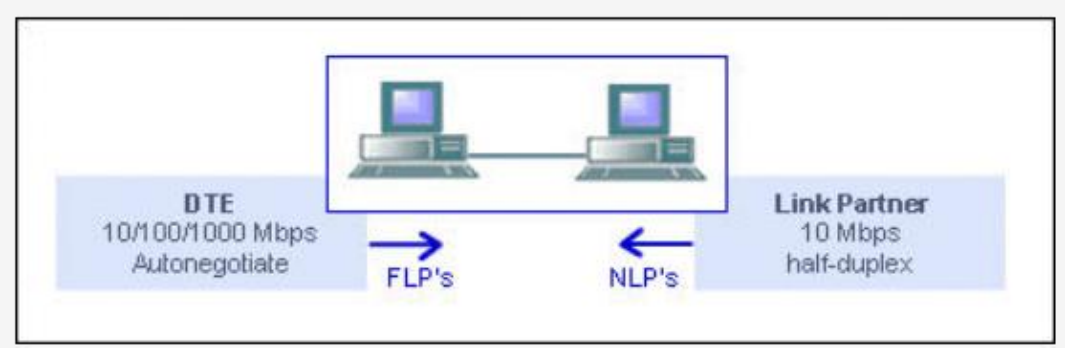




3) Auto-negotiation starts after Power-up,
command from Management Interface or from User interaction.

4) 10Base-T – Standard Ethernet (10Mbps)
100Base-Tx – Fast Ethernet (100Mbps)
1000Base-T – Gigabit Ethernet (1000Mbps)

# Auto-negotiation (contd..)

1. Mainly used to exchange Speed, Duplex and Flow Control in (10Base-T/100Base-TX) Ethernet (Standard/Fast Ethernet)
2. Additionally, Master/Slave configuration for Gigabit Ethernet (1000Base-T) (where clock is sourced for Tx)
3. Always recommended to enable on both sides of the link or completely disabled on both sides. If not, then Duplex mis-match may occur leading to serious network performance degradation.
4. Parallel detection – if a node does not support auto-negotiation, but the link partner can examine the signal to find whether it is 10Base-T, 100Base-TX or 100Base-T4 to know the speed. However, the duplex will be switched to half irrespective of the peer end.




*Note – Auto-negotiation is mandatory for Gigabit Ethernet.*

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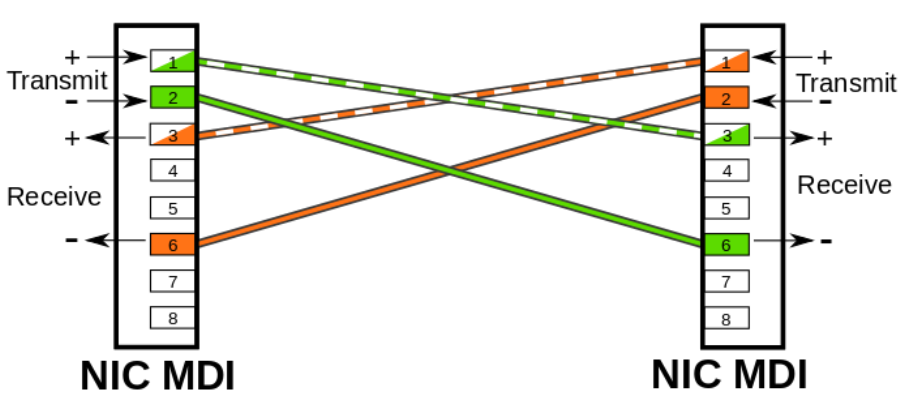
# Auto-MDIX

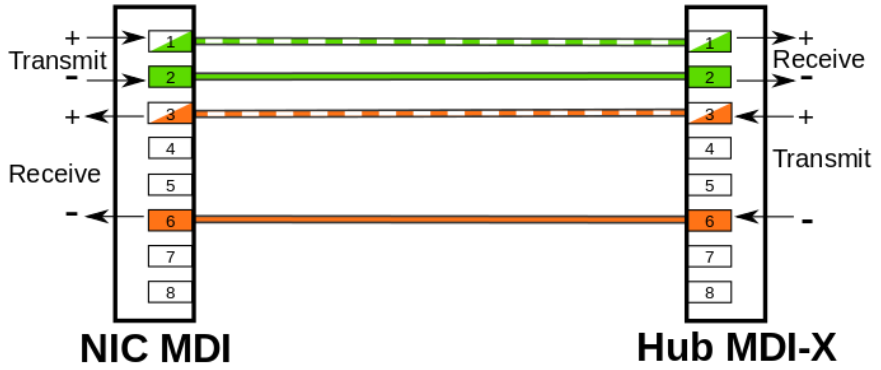
## Problem:

1. Early days Network devices(Hubs/Switches/TAPs) have their connections crossed (MDIX)
2. Local NICs(Network Interface Cards) or PC uses MDI connections.
3. A connection between a PC to a Switch – requires straight cable as the MDI is already crossed (Tx ←→ Rx)
4. A connection between PC to PC requires a crossover cable.

## Solution:

1. To solve this at the interface level, auto-MDIX was invented where the TX and RX pairs are swapped automatically.



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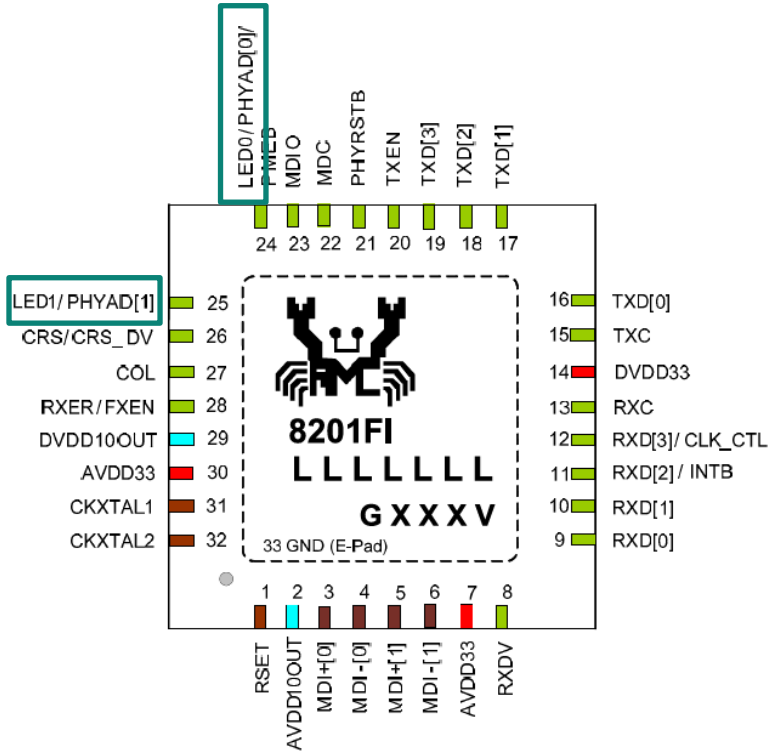
# Introduction to Management Data I/O

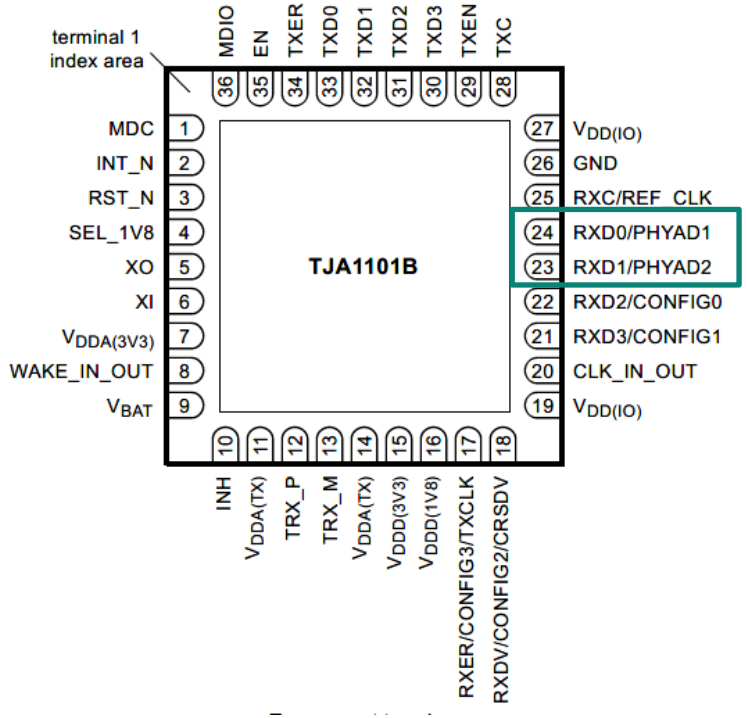
1. Management Data I/O (commonly termed as MDIO) is a simple two wire serial communication bus interface.
2. This interface is used to configure the Physical layer transceivers from the Host controller.
3. It uses two lines for communication (Like I2C)

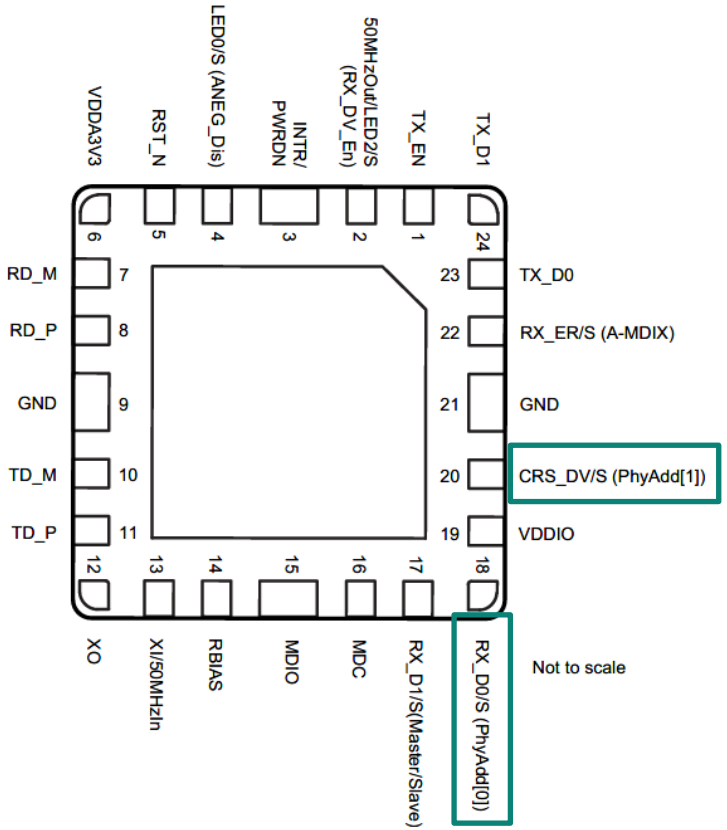
   MDC – Management Data clock (ideally 2.5Mhz but can be more depending on what the PHY supports) – bidirectional

   MDIO – Management Data I/O - sourced from MAC to PHY
4. There are two variants of the MDIO protocol we usually call them C22 (Clause 22) and C45 (Clause 45).
5. C45 was implemented to make the PHY vendors to integrate more additional functionalities inside the PHY
6. Like I2C, the PHYs on the MDIO bus would require an address.
7. C22 and C45 PHYs cannot exist on the same Bus as their electrical characteristics are different

# PHY Addresses configuration via HW Strap options



# Clause 22 – Frame Format

A Clause-22 MDIO Frame Format:

**PRE** - Preamble – 32 bits of logic 1's for Sync – there is option to suppress the Preamble as well (a MAC feature)

**ST** - Start of transmission (2b'01) on the line.

**OP** - Operation Code (for READ – 2b'10, WRITE – 2b'01)

**PHYAD** - Phy Address – 5 bits (so 31 PHYs on a single bus can be addressed)

- All PHYs on the Bus will respond to Address 5b'00000 (0x0) – Broadcast address.

**REGAD** – Register Address – 5 bits (upto 32 registers can be accessed)

**TA** – Turnaround – (2b'Z0 for read transaction, 2b'10 for write transaction)

**DATA** – Data-field 16 bits ($15^{th}$ bit is sent first on the line)

| | Management frame fields | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | PRE | ST | OP | PHYAD | REGAD | TA | DATA | IDLE |
| READ | 1...1 | 01 | 10 | AAAAA | RRRRR | Z0 | DDDDDDDDDDDDDDDD | Z |
| WRITE | 1...1 | 01 | 01 | AAAAA | RRRRR | 10 | DDDDDDDDDDDDDDDD | Z |

# C45 Frame Format

A Clause 45 frame format:

**PRE** - Preamble – 32 bits of logic 1's for Sync – there is option to suppress the Preamble as well (a MAC feature)

**ST** - Start of transmission (2b'01) on the line.

**OP** - Operation Code (for READ – 2b'10, WRITE – 2b'01)

**PRTAD** - Port Address – 5 bits (so 31 Ports on a single bus can be address) – this is PHY Address in C22

**DEVAD** – Device Address – 5 bits (upto 32 devices within a port can be accessed)

**TA** – Turnaround – (2b'Z0 for read transaction, 2b'10 for write transaction)

**ADDR/DATA** – Address/Data-field 16 bits ($15^{th}$ bit is sent first on the line)

| | Management frame fields | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Frame** | **PRE** | **ST** | **OP** | **PRTAD** | **DEVAD** | **TA** | **ADDRESS / DATA** | **IDLE** |
| Address | 1...1 | 00 | 00 | PPPPP | EEEEE | 10 | AAAAAAAAAAAAAAAA | Z |
| Write | 1...1 | 00 | 01 | PPPPP | EEEEE | 10 | DDDDDDDDDDDDDDDD | Z |
| Read | 1...1 | 00 | 11 | PPPPP | EEEEE | Z0 | DDDDDDDDDDDDDDDD | Z |
| Post-read-increment-address | 1...1 | 00 | 10 | PPPPP | EEEEE | Z0 | DDDDDDDDDDDDDDDD | Z |

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# Media Independent Interface (MII)

- The **media-independent interface** (**MII**) was originally defined as **a standard interface** in the **IEEE 802.3u** to connect a Fast Ethernet (i.e., 100 Mbit/s) medium access control (MAC) block to a PHY chip.

- The original MII transfers network data using 4-bit nibbles in each direction (4 transmit data bits, 4 receive data bits). The data is clocked at 25 MHz to achieve 100 Mbit/s throughput and the same data can be clocked at 2.5MHz to achieve a 10MBit/s throughput.

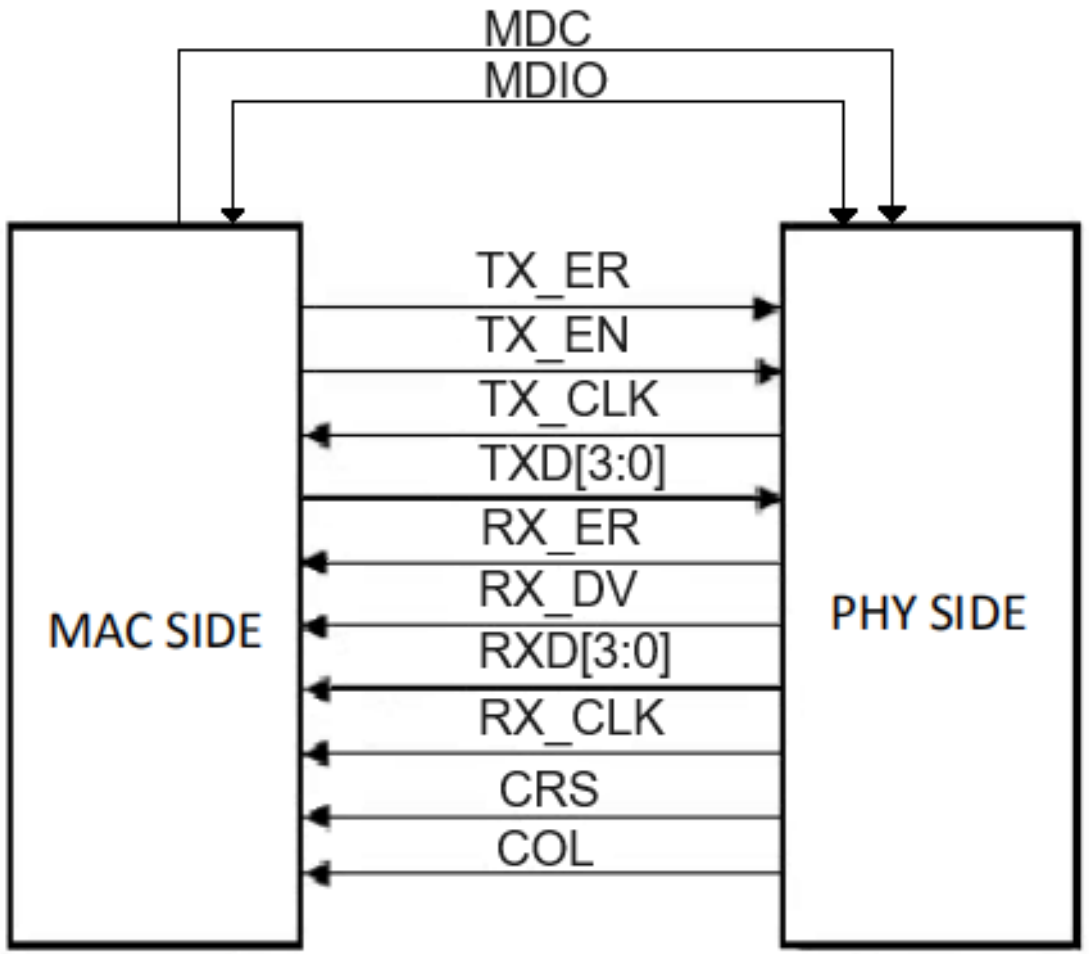
- The Management Data Input/Output (MDIO) serial bus is a subset of the MII that is used to transfer management information between MAC and PHY. At power up, using autonegotiation, the PHY usually adapts to whatever it is connected to unless settings are altered via the MDIO interface.

# Media Independent Interface (MII)

- The standard MII features a small set of registers such as:
  - Basic Mode Configuration (#0);
  - Status Word (#1);
  - PHY Identifier (#2, #3);
  - Auto-Negotiation Advertisement (#4).

- The MII Status Word is the most useful datum, since it may be used to detect whether an Ethernet NIC is connected to a network:
  - 0x6000 -> Capable of 100BASE-TX full/half duplex;
  - 0x0020 -> Autonegotiation complete;
  - 0x0004 -> Link established.

# Media Independent Interface (MII)



# Media Independent Interface (MII)

- Transmitter Signals:
  - TX_CLK Transmit clock Direction: PHY to MAC;
  - TXD0 Transmit data bit 0 (transmitted first) Direction: MAC to PHY;
  - TXD1 Transmit data bit 1 Direction: MAC to PHY;
  - TXD2 Transmit data bit 2 Direction: MAC to PHY;
  - TXD3 Transmit data bit 3 Direction: MAC to PHY;
  - TX_EN Transmit enable Direction: MAC to PHY;
  - TX_ER Transmit error (optional) Direction: MAC to PHY.

- The transmit clock is a free-running clock generated by the PHY based on the link speed (25 MHz for 100 Mbit/s, 2.5 MHz for 10 Mbit/s)!

- The remaining transmit signals are driven by the MAC synchronously on the rising edge of TX_CLK.

# Media Independent Interface (MII)

- The transmit enable signal is held high during frame transmission and low when the transmitter is idle.

- Transmit error may be raised for one or more clock periods during frame transmission to request the PHY to deliberately corrupt the frame in some visible way that precludes it from being received as valid.

- The MAC may omit the signal if it has no use for this functionality, in which case the signal should be tied low for the PHY.

- More recently, raising transmit error *outside* frame transmission is used to indicate the transmit data lines are being used for special-purpose signalling.

# Media Independent Interface (MII)

- Receiver Signals:
  - RX_CLK Receive clock Direction: PHY to MAC;
  - RXD0 Receive data bit 0 (received first) Direction: PHY to MAC;
  - RXD1 Receive data bit 1 Direction: PHY to MAC;
  - RXD2 Receive data bit 2 Direction: PHY to MAC;
  - RXD3 Receive data bit 3 Direction: PHY to MAC;
  - RX_DV Receive data valid Direction: PHY to MAC;
  - RX_ER Receive error Direction: PHY to MAC;
  - CRS Carrier sense Direction: PHY to MAC;
  - COL Collision detect Direction: PHY to MAC.

- The first seven receiver signals are entirely analogous to the transmitter signals, except RX_ER is not optional and used to indicate the received signal could not be decoded to valid data.

- The receive data valid signal (RX_DV) is not required to go high immediately when the frame starts but it must do so in time to ensure the "start of frame delimiter" byte is included in the received data. Some of the preamble nibbles may be lost.

# Media Independent Interface (MII)

- Similar to transmit, raising RX_ER outside a frame is used for special signaling.

- The CRS and COL signals are asynchronous to the receive clock, and are only meaningful in half-duplex mode. Carrier sense is high when transmitting, receiving, or the medium is otherwise sensed as being in use. If a collision is detected, COL also goes high while the collision persists.

- Management Signals:
  - MDIO Management data Direction: Bidirectional;
  - MDC Management data clock Direction: MAC to PHY;

- MDC and MDIO constitute a synchronous serial data interface similar to I²C. As with I²C, the interface is a multidrop bus so MDC and MDIO can be shared among multiple PHYs.

# Media Independent Interface (MII)

- The term ReverseMII (revMII) describes the scenario where 2 MAC's are connected back to back (with no phy). RevMII is fully compatible with IEEE Std. 802.3u. Other interfaces that are "reverse" such as Reverse RMII are vendor specific hence they are not defined in any standards.

- The link provided by RevMII is configurable via MDIO and the clock signal is now provided by one of the MACs.

- MII Limitations:
  - The interface requires 18 signals, out of which only two (MDIO and MDC) can be shared among multiple PHYs. This presents a problem, especially for multiport devices; for example, an eight-port switch using MII would need 8 × 16 + 2 = 130 signals.

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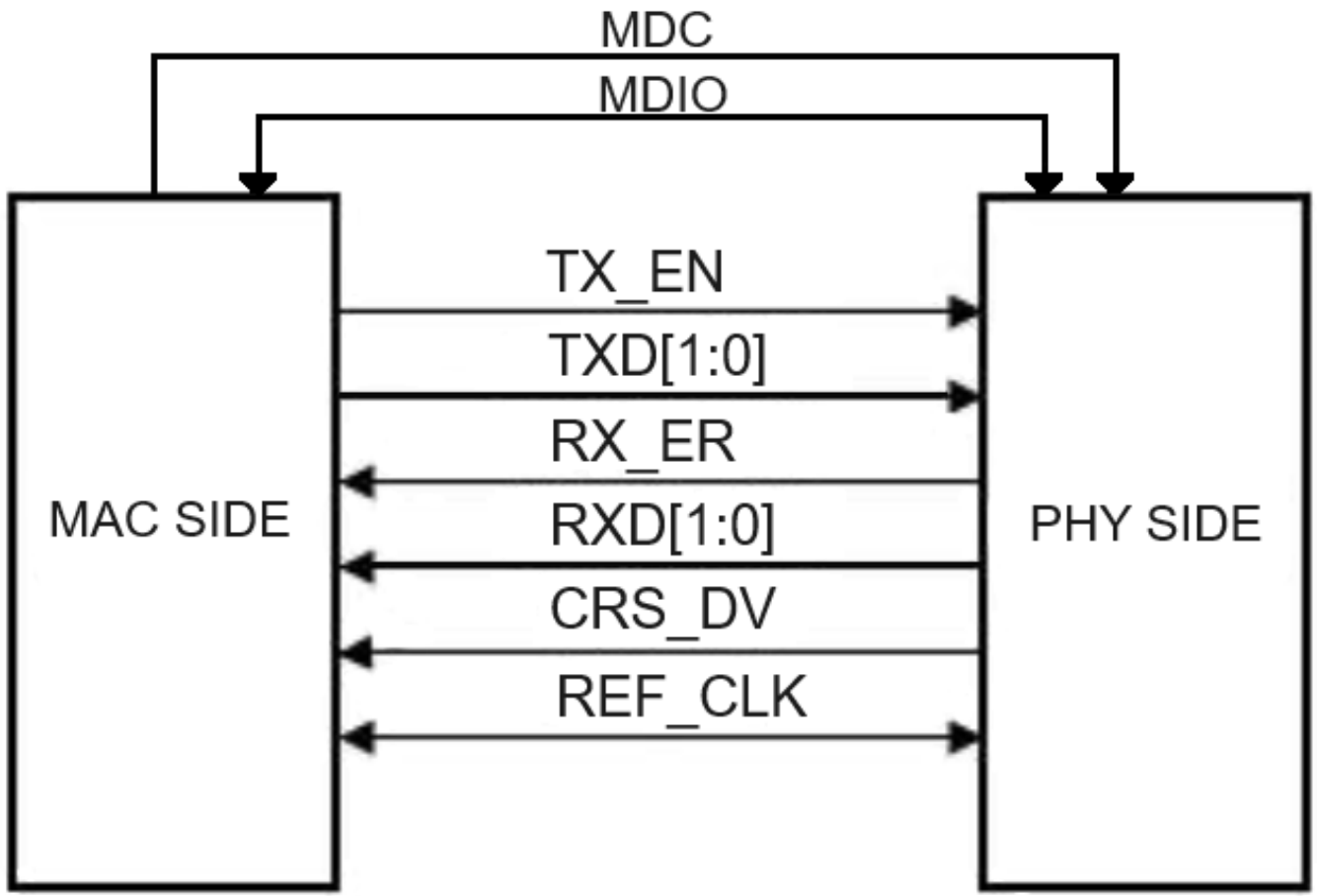
# Reduced Media-Independent Interface (RMII)

- Reduced media-independent interface (RMII) is a **de facto standard interface** which was developed to reduce the number of signals required to connect a PHY to a MAC and it is described in the RMII Consortium V1.2 document.
- RMII uses about half the number of signals compared to MII.
- The two MII clocks TXCLK and RXCLK are replaced by a single clock in RMII. This clock is an input to the PHY rather than an output, which allows the clock signal to be shared among all PHYs in a multiport device, such as a switch.
- The RMII clock frequency is doubled from 25 MHz to 50 MHz regardless of the transmission speed (10/100Mbit/s), while the data paths are narrowed from 4 bits to 2 bits.
- RXDV and CRS signals are multiplexed into one signal.
- The COL signal is removed.

# Reduced Media-Independent Interface (RMII)



# Reduced Media-Independent Interface (RMII)

- Transmitter Signals:
  - REF_CLK Continuous 50 MHz reference clock Direction: Not defined;
  - TXD0 Transmit data bit 0 (transmitted first) Direction: MAC to PHY;
  - TXD1 Transmit data bit 1 Direction: MAC to PHY;
  - TX_EN Transmit enable Direction: MAC to PHY.

- The reference clock may be an input on both devices from an external clock source, or may be driven from the MAC to the PHY, or may be driven from the PHY to the MAC!

- TX_EN signals indicates that the MAC is presenting di-bits on TXD[1:0] for transmission.

- A di-bit is a combination of two binary digits out of four possible combinations (00, 01, 10, 11).

# Reduced Media-Independent Interface (RMII)

- Receiver Signals:
  - RXD0 Receive data bit 0 (received first) Direction: PHY to MAC;
  - RXD1 Receive data bit 1 Direction: PHY to MAC;
  - CRS_DV Carrier Sense (CRS) and RX_Data Valid (RX_DV) Direction: PHY to MAC;
  - RX_ER Receive error (optional on switches) Direction: PHY to MAC.

- Carrier Sense (CRS) and RX_Data Valid (RX_DV) are multiplexed on alternate clock cycles. In 10 Mbit/s mode, it alternates every 10 clock cycles.

- The receiver signals are referenced to the REF_CLK, same as the transmitter signals.

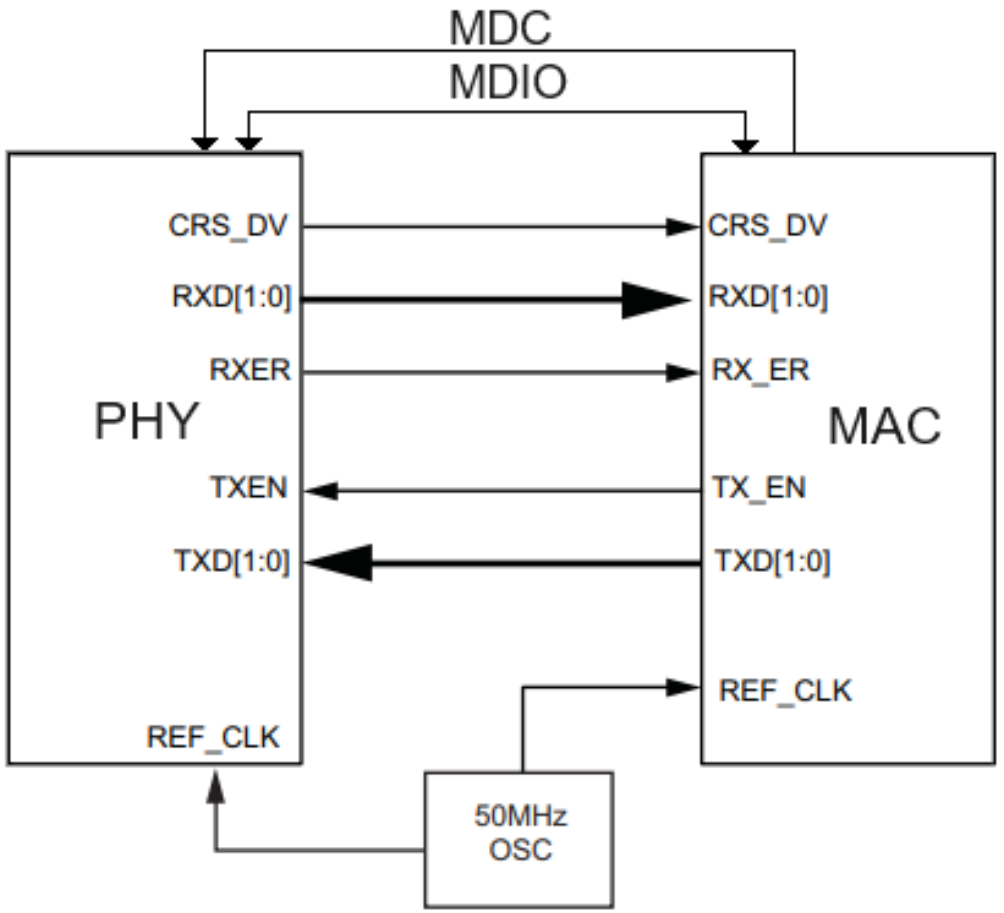
- Management Signals:
  - MDIO Management data Direction: Bidirectional;
  - MDC Management data clock Direction: MAC to PHY.

# Reduced Media-Independent Interface (RMII)

- RMII requires a 50 MHz clock where as MII requires a 25 MHz clock and data is clocked out two bits at a time vs 4 bits at a time for MII. Data is sampled on the rising edge only (i.e. it is not double-pumped).

- The REF_CLK operates at 50 MHz in both 100 Mbit/s mode and 10 Mbit/s mode. The transmitting side (PHY or MAC) must keep all signals valid for 10 clock cycles in 10 Mbit/s mode. The receiver (PHY or MAC) samples the input signals only every ten cycles in 10 Mbit/s mode.

# Reduced Media-Independent Interface (RMII)



# Reduced Media-Independent Interface (RMII)

- RMII limitations
  - MII interface requires 9 signals, versus MII's 18. Of those 9, on multiport devices, MDIO, MDC, and REF_CLK may be shared leaving 6 or 7 pins per port;
  - There is no signal which defines whether the interface is in full or half duplex mode, but both the MAC and the PHY need to agree. This must instead be communicated over the serial MDIO/MDC interface;
  - There is also no signal which defines whether the interface is in 10 or 100 Mbit/s mode, so this must also be handled using the MDIO/MDC interface;
  - On RMII CRS is asserted only for Rx frames, in comparison to MII where CRS is asserted for both Rx and Tx frames.

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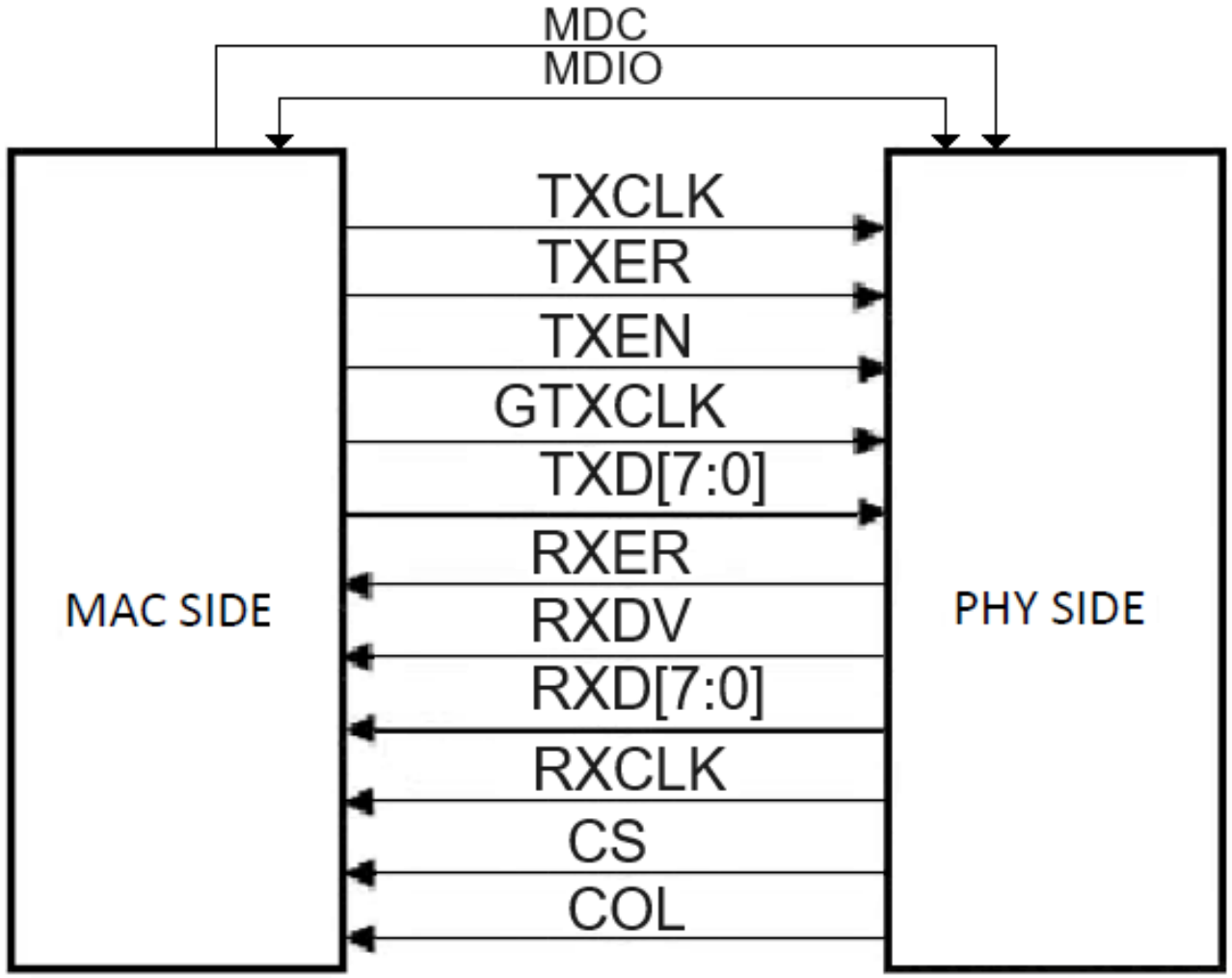
# Gigabit Media Independent Interface (GMII)

- The gigabit media-independent interface (GMII) is a **standard interface**, that was defined **in IEEE 802.3z-1998 as clause 35,** between the medium access control (MAC) device and the physical layer (PHY).

- The interface operates at speeds up to 1000 Mbit/s, implemented using a data interface clocked at 125 MHz with separate eight-bit data paths for receive and transmit, and is backwards compatible with the MII specification and can operate on fall-back speeds of 10 or 100 Mbit/s.

# Gigabit Media Independent Interface (GMII)



# Gigabit Media Independent Interface (GMII)

- Transmitter Signals:
  - GTXCLK Clock signal for gigabit TX signals (125 MHz) Direction: MAC to PHY;
  - TXCLK Clock signal for 10/100 Mbit/s signals Direction: MAC to PHY;
  - TXD[7..0] Data to be transmitted Direction: MAC to PHY;
  - TXEN Transmitter enable Direction: MAC to PHY;
  - TXER Transmitter error Direction: MAC to PHY.
- Receiver Signals:
  - RXCLK Received clock signal Direction: PHY to MAC;
  - RXD[7..0] Received data Direction: PHY to MAC;
  - RXDV Signifies data received is valid Direction: PHY to MAC;
  - RXER Signifies data received has errors Direction: PHY to MAC;
  - COL Collision detect (half-duplex connections only) Direction: PHY to MAC;
  - CS Carrier sense (half-duplex connections only) Direction: PHY to MAC.
- Management Signals:
  - MDIO Management data Direction: Bidirectional;
  - MDC Management data clock Direction: MAC to PHY.

# Gigabit Media Independent Interface (GMII)

- There are two transmitter clocks. The clock used depends on whether the PHY is operating at gigabit or 10/100 Mbit/s speeds.
- For gigabit operation, the GTXCLK is supplied to the PHY and the TXD, TXEN, TXER signals are synchronized to this.
- For 10 or 100 Mbit/s operation, the TXCLK is supplied by the PHY and is used for synchronizing those signals. This operates at either 25 MHz for 100 Mbit/s or 2.5 MHz for 10 Mbit/s connections. In contrast, the receiver uses a single clock signal recovered from the incoming data.
- GMII limitation:
  - Very high number of pins (27 pins with MDIO included) which makes this interface not the most preferred one.

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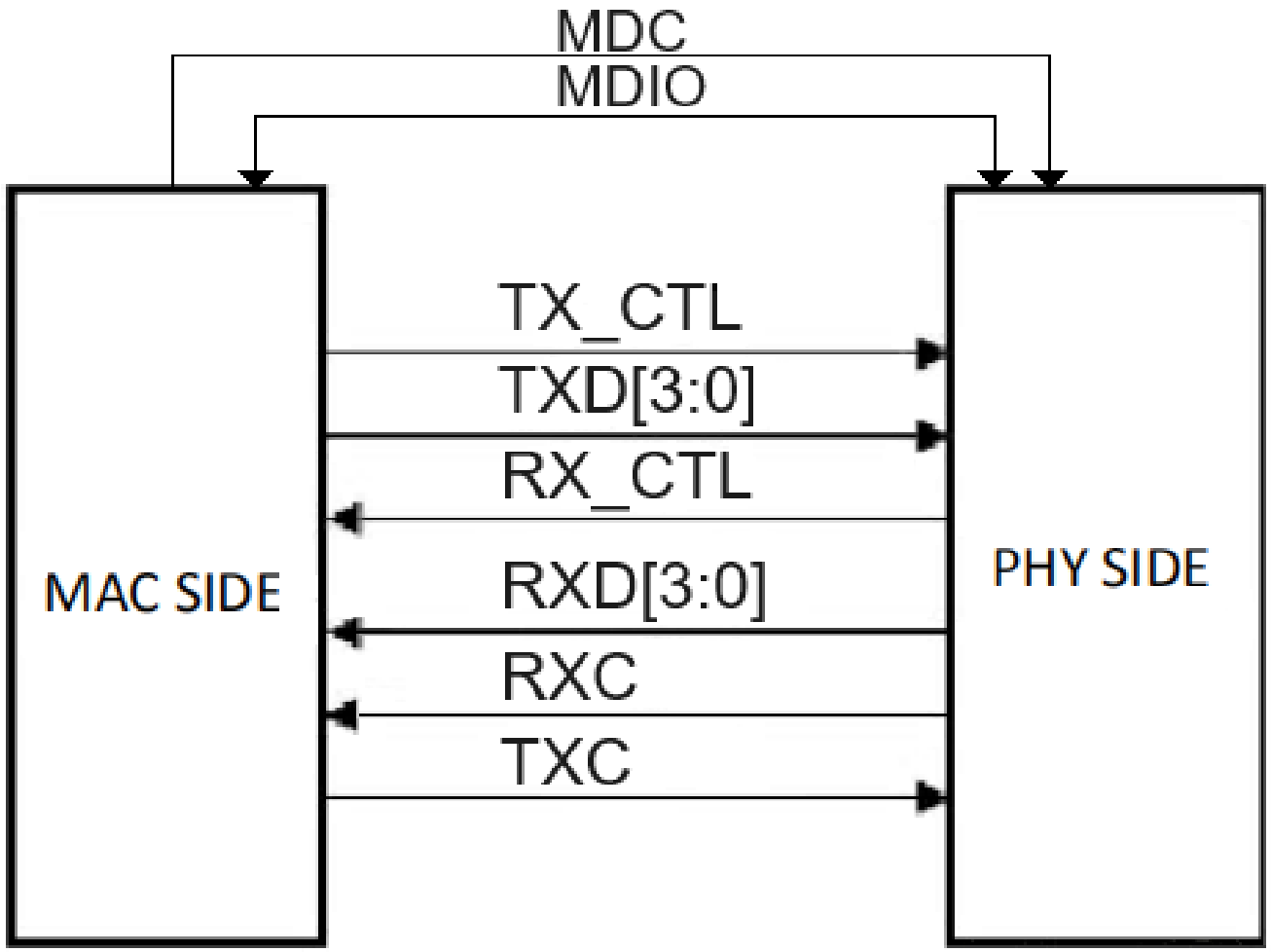
# Reduced Gigabit Media Independent Interface (RGMII)

- The Reduced Gigabit Media-Independent Interface (RGMII) is a **de facto standard interface** between a MAC and a PHY that uses half the number of data pins compared to the GMII interface. RGMII is described in the RGMII V1.3 document.

- This reduction is achieved by running half as many data lines at double speed, time multiplexing signals and by eliminating non-essential carrier-sense and collision-indication signals. Thus, RGMII consists only of 14 pins, as opposed to GMII's 24 to 27.

- Data is clocked on rising and falling edges for 1000 Mbit/s, and on rising edges only for 10/100 Mbit/s. The TX/RX clock signals for 1000 Mbit/s is 125 MHz, for 100 Mbit/s is 25 MHz and for 10 Mbit/s is 2.5MHz.

# Reduced Gigabit Media Independent Interface (RGMII)



# Reduced Gigabit Media Independent Interface (RGMII)

- Transmitter Signals:
  - TXC Clock signal Direction: MAC to PHY;
  - TXD[3..0] Data to be transmitted Direction: MAC to PHY;
  - TX_CTL Multiplexing of transmitter enable and transmitter error Direction: MAC to PHY.

- The TX_CTL signal likewise carries TXEN on rising edge and (TXEN xor TXER) on the falling edge. This is the case for both 1000 Mbit/s and 10/100 Mbit/s.

- Receiver Signals:
  - RXC Received clock signal Direction: PHY to MAC;
  - RXD[3..0] Received data Direction: PHY to MAC;
  - RX_CTL Multiplexing of data received is valid and receiver error Direction: PHY to MAC.

- The RX_CTL signal carries RXDV (data valid) on the rising edge, and (RXDV xor RXER) on the falling edge

# Reduced Gigabit Media Independent Interface (RGMII)

- Management Signals:
  - MDIO Management data Direction: Bidirectional;
  - MDC Management data clock Direction: MAC to PHY.

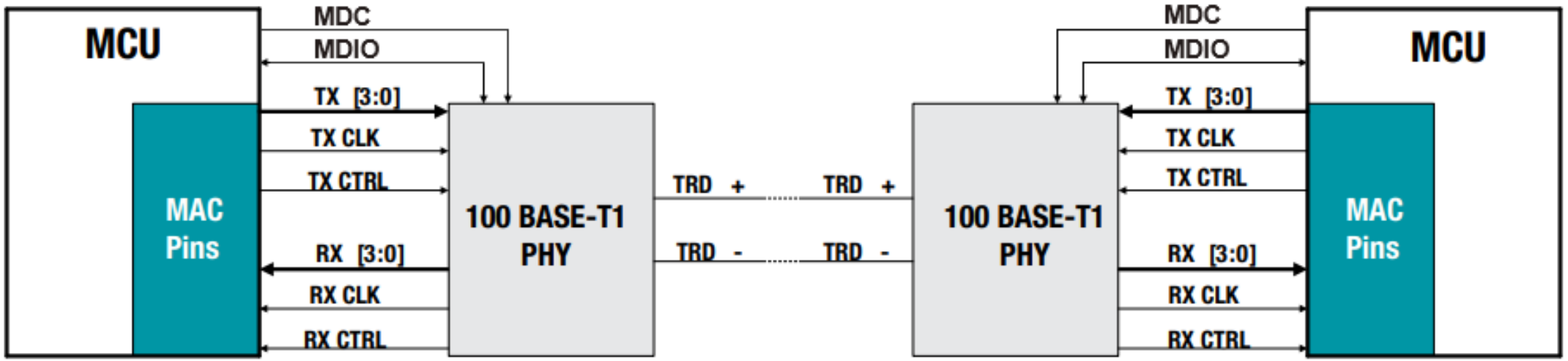
- The transmit clock signal is always provided by the MAC on the TXC line.

- The receive clock signal is always provided by the PHY on the RXC line.

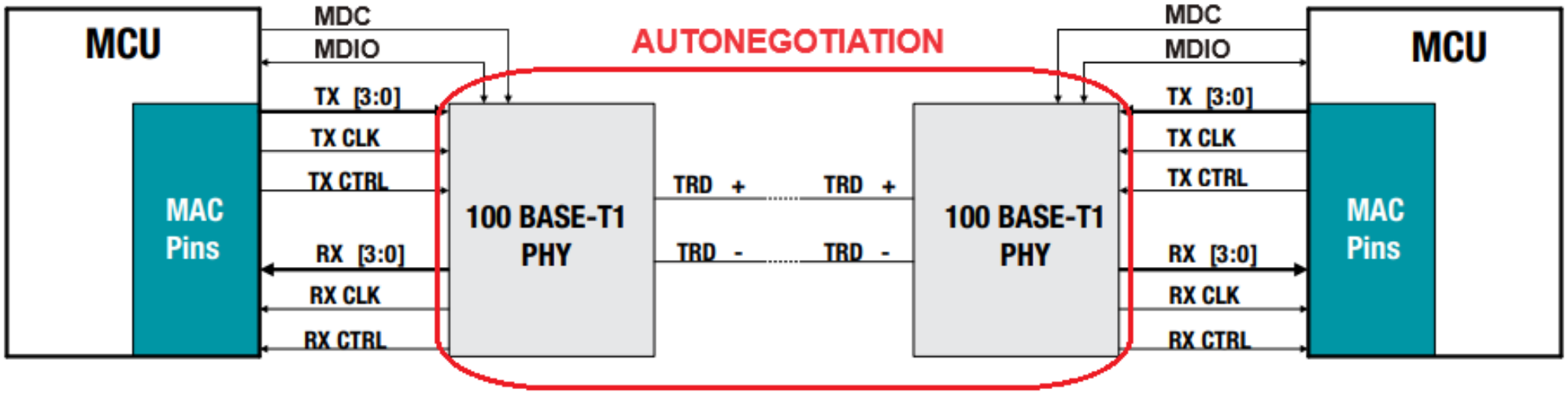
- RGMII specifies that the clock and data will be generated simultaneously by the transmitting source which requires a skew be introduced between clock and data. The skew can be achieved by PCB trace routing or by an internal delay in the transmitting or receiving node.

- There is an official standard release for the 1Gbps RGMII interface called “ISO 21111-2:2020 - Road vehicles”, which covers all the interface parameters, such as timing and physical layer parameters. This standard is only applicable for a 1Gbps 3V3 RGMII interface!

# Reduced Gigabit Media Independent Interface (RGMII)



# Reduced Gigabit Media Independent Interface (RGMII)



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# Useful links and Follow-ups

**Follow-up:**

1) What could we do if there is a need for more registers in a C22 capable PHY?
2) Difference between 1000Base-T and 1000Base-TX and which cables Cat 5/5e or Cat6
3) Parallel Detection in PHYs

**Links:**

MAC Address lookup - https://maclookup.app/search

Ether-Type list - https://www.iana.org/assignments/ieee-802-numbers/ieee-802-numbers.xml

Frame format - https://upload.wikimedia.org/wikipedia/commons/7/72/Ethernet_Frame.png


Infineon