

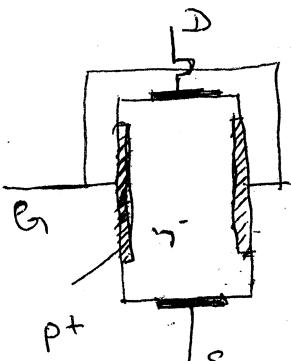
Field Effect Transistor (FET)

①

o) The FET is a device in which flow of current through the conducting region is controlled by an Electric field. Hence the name Field Effect Transistor (FET). As current conduction is only by majority carriers, the FET is said to be an Unipolar device.

Based on the construction, the FET can be classified into two types (i) Junction FET (JFET) and (ii) Metal Oxide Semiconductor FET (MOSFET) or Insulated gate FET (IGFET).

Semiconductor FET (MOSFET) or Metal Oxide Silicon Transistor (MOS)



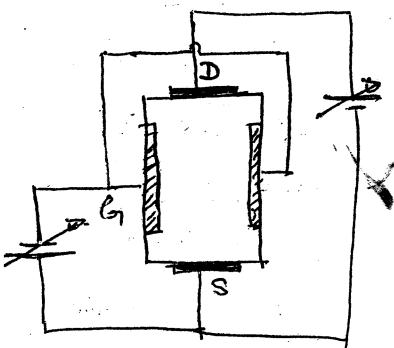
It consists of a N-type bar (lightly doped) which is made of Silicon. Ohmic contacts made at the two ends of the bar, are called Source and Drain.

Source (S) : This terminal is connected to the negative terminal of the battery. Electrons are the majority carriers in the N-type bar, which enter the bar through this terminal.

Drain (D) : This terminal is connected to the +ve terminal of the battery. The majority carriers leave the bar through this terminal.

Gate (G) : Heavily doped P-type Silicon is diffused on both the sides of the N-type Silicon bar by which PN junctions are formed. These layers are joined together and called Gate (G).

Channel : The region between the Gate is called the Channel. Majority carriers move from the source to drain through this channel, when a potential difference V_{DS} is applied between the source and drain.



When $V_{GS} = 0$ & $V_{DS} = 0$: when there is no voltage applied between drain and source (V_{DS}) and source and gate ($V_{GS} = 0$), the thickness of the depletion region round the p-n junction and it is uniform when $V_{DS} = 0$ and V_{GS} is decreased from zero ($V_{DS} = 0$).

In this case, the p-n junctions are reverse biased and hence the thickness of the depletion region is increased. The increase in the depletion region is uniform and at certain voltage of V_{GS} , both the depletion region make contact with each other, and the channel width is reduced to zero.

When $V_{GS} = 0$ and V_{DS} is increased from zero ($V_{GS} = 0$ $V_{DS} \neq 0$ $I_{DS} \neq 0$)

With increase in V_{DS} by keeping $V_{GS} = 0$, the majority carriers move from source to drain, therefore the conventional current I_{DS} moves from drain to source. Because of the resistance of the channel and the applied voltage V_{DS} , there is a gradual increase of positive potential along the channel from source to drain. Thus reverse voltage across the p-n junctions increase and the leakage current I_{DS} increases in depletion region. Therefore channel is tapered towards the drain or wedge shaped. As V_{DS} is increased, the cross-section area of the channel is reduced and it will become minimum at certain voltage of V_{DS} called V_p .

The following observations are made with increase in V_{DS}

- As V_{DS} is increased from zero, I_{DS} is increased and the rate of increase of I_{DS} with V_{DS} is decreased.
- At certain voltage of V_{DS} called V_p , the increase in I_{DS} becomes zero. i.e., I_{DS} becomes constant. The voltage V_p is called Pinch off Voltage. The region from $V_{DS} = 0$ to $V_{DS} = V_p$ is called Ohmic region.

Mutual Characteristic or Transfer Characteristic or Transconductance Curve

If V_{DS} is maintained constant, & it's greater than V_p (Pinch off voltage $V_{DS} = V_p$ ($V_{GS} = 0$)). The gate voltage is

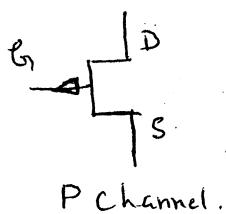
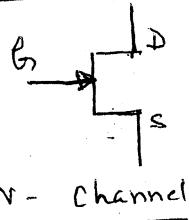
reduced ($V_{GS} \downarrow$) from zero till I_{DS} is reduced to zero (approximately). The V_{GS} at which the current I_{DS} is approximately becoming zero is called $V_{GS(\text{off})} = -V_p$.

The expression for the current is given by $I_{DS} = I_{DSs} \left(1 - \frac{V_{GS}}{V_{GS(\text{off})}} \right)^2$

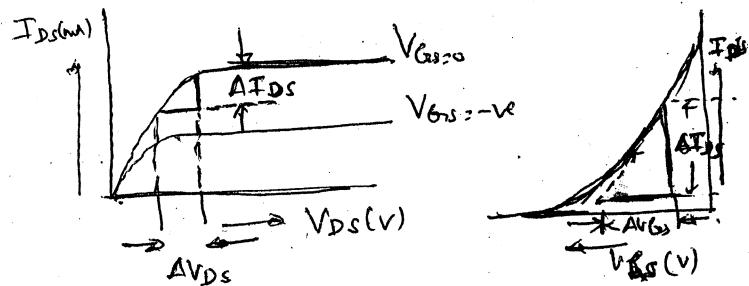
when $V_{GS} = 0$ $I_{DS} = I_{DSs} (\text{max current})$

$$V_{GS} = V_{GS(\text{off})} \Rightarrow I_{DS} \approx 0$$

Symbol



P Channel.



Parameters of the JFET

Drain Resistance r_d : It is the reciprocal of the slope of the drain characteristic and is defined by

$$r_d = \left. \frac{\partial V_{DS}}{\partial I_{DS}} \right|_{V_{GS}} = \left. \frac{\Delta V_{DS}}{\Delta I_{DS}} \right|_{V_{GS} = \text{const.}} = -\infty$$

Mutual Conductance or Transconductance g_m : It is the slope of the transfer characteristic

$$g_m = \left. \frac{\partial I_{DS}}{\partial V_{GS}} \right|_{V_{DS}} = \left. \frac{\Delta I_{DS}}{\Delta V_{GS}} \right|_{V_{DS} = \text{const.}} = -\infty (\text{s})$$

Amplification factor (μ)

$$\mu = - \left(\left. \frac{\partial V_{DS}}{\partial V_{GS}} \right| \right) \Big|_{I_{DS} = \text{const.}} = - \left. \frac{\Delta V_{DS}}{\Delta V_{GS}} \right| \Big|_{I_{DS} = \text{const.}} = -\infty$$

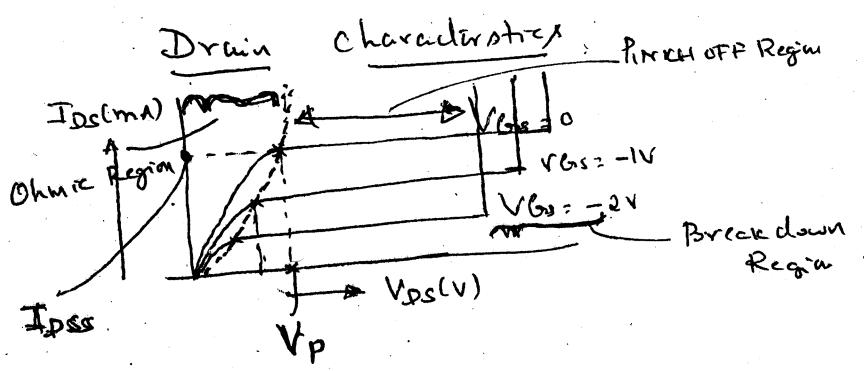
Negative sign indicates increase in negative value of V_{GS} ($V_{GS} \downarrow$), the V_{DS} has to be increased to maintain I_{DS} const

$$\mu = g_m r_d$$

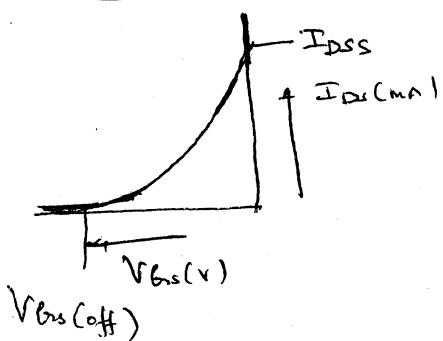
- (3)
- When $V_{DS} = V_p$ called the Pinch off Voltage, I_{DS} becomes constant (i.e., $\Delta I_{DS} = 0$). This value of I_{DS} is called I_{DSS} is the maximum current that can be obtained in FET. I_{DSS} is called Drain to Source Saturation Current or Drain to Source current when gate to source is short circuited ($V_{GS} = 0$) Any further increase in V_{DS} , the I_{DS} will not change. This region after $V_{DS} \geq V_p$ is called Pinch OFF Region.
 - At certain voltage of V_{DS} , the current I_{DS} increases suddenly. This effect is due to the avalanche multiplication of electrons caused by breaking of covalent bonds of silicon atoms in the depletion region between gate and drain. This region is called breakdown region. Any how the device cannot be used in this region because it damages the device.

When V_{GS} is negative and V_{DS} is increased

Since already V_{GS} is -ve, there is depletion region exists in the channel. Therefore if V_{DS} is increased channel width becomes minimum for lower value of V_{DS} when compared to earlier. i.e., the Pinch off Voltage is less when compared to $V_{GS} = 0$. The Avalanche breakdown occurs at lower value of V_{DS} . The value of I_{DS} is also smaller when compared to earlier.



Transconductance Curve OR Mutual Characteristics



(5)

Comparison of JFET and BJT

1. In FET the current depends only on the majority carriers. Therefore it is called Unipolar device. Whereas in BJT current depends on both majority and minority carriers. So it is called Bipolar device.
2. As FET has no junctions and the conduction is through an N-type or P-type semiconductor material. Therefore FET is less noisy than BJT.
3. As the input C.R. of FET is reverse biased, FET exhibits a much higher input impedance than BJT (In BJT I_p C.R. is forward biased).
4. The FET is a voltage controlled device i.e., Voltage at the I/P terminal controls the O/P current, whereas BJT is a current controlled device i.e., the I/P current controls O/P current.
5. FET's are much easier to fabricate and are particularly suitable for IC's because they occupy less space than BJT.
6. FET's are immune to Radiation but BJT's are susceptible to radiation.
7. FET's are thermally stable than BJT because
8. FET's have higher switching speed than BJT because FET's do not suffer from minority carrier storage.
9. FET amplifiers have low gain Bandwidth due to

(Disadvantage of FET)
 Junction capacitance effects and produce more signal distortion
 except for small signal operation

Application of JFET

- ① FET is used as a buffer in measuring instruments.
- ② FET's are used in RF amplifiers in FM tuner and communication equipment for the low noise level.

- (3) Since the device is Voltage Controlled, it is used as a
 (6) Voltage Variable resistor in operational amplifier and tone control
- (4) It is used in oscillator circuit because frequency drift is low
- (5) FET's are used in digital Ckt's in computer, memory etc because of its small size.

FET Equivalent Ckt for small signal and low frequency

we know that I_{DS} is a function of both V_{DS} and V_{GS}

$$I_{DS} = f(V_{DS}, V_{GS})$$

$$\Delta I_{DS} = \left(\frac{\partial I_{DS}}{\partial V_{DS}} \right) \Delta V_{DS} + \left(\frac{\partial I_{DS}}{\partial V_{GS}} \right) \Delta V_{GS}$$

when $V_{GS} = \text{constant}$; $\Delta V_{GS} = 0$

$$\therefore \frac{\partial I_{DS}}{\partial V_{DS}} = \frac{\Delta I_{DS}}{\Delta V_{DS}} = \frac{1}{r_d}$$

$$\text{or } r_d = \left. \frac{\Delta V_{DS}}{\Delta I_{DS}} \right|_{V_{GS}=\text{const}} = -v$$

when $V_{DS} = \text{constant}$ $\Delta V_{DS} = 0$

$$\therefore \frac{\partial I_{DS}}{\partial V_{GS}} = \frac{\Delta I_{DS}}{\Delta V_{GS}} = g_m$$

$$\left. \frac{\Delta I_{DS}}{\Delta V_{GS}} \right|_{V_{DS}=\text{const}} = g_m = -v$$

Then we can replace FET by its equivalent ckt by the following eqn

$$\Delta I_{DS} = \left(\frac{1}{r_d} \right) \Delta V_{DS} + g_m \Delta V_{GS}$$

$$i_{ds} = \left(\frac{1}{r_d} \right) v_{ds} + g_m v_{gs}$$



(7)

FET Current Equation

$$I_{DS} = I_{DSS} \left[1 - \frac{V_{GS}}{V_{GS(\text{off})}} \right]^2$$

where I_{DSS} = Current from Drain to Source with $V_{GS} = 0$ (i.e., Gate to Source is short)

$$\frac{dI_{DS}}{dV_{GS}} = -\frac{2I_{DSS}}{V_{GS(\text{off})}} \left[1 - \frac{V_{GS}}{V_{GS(\text{off})}} \right]$$

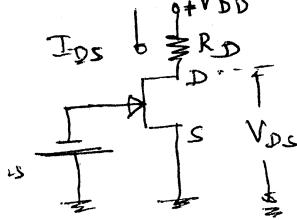
$$g_m = g_{mo} \left[1 - \frac{V_{GS}}{V_{GS(\text{off})}} \right]$$

$$\text{where } g_{mo} = \frac{-2I_{DSS}}{V_{GS(\text{off})}}$$

Biasing of the FET : For Proper functioning of a linear FET amplifier, it is necessary to maintain the operating point "Q" stable in the central portion of the Pinch Off region. The operating point should be independent of device parameter variations and ambient temperature changes. This can be achieved by suitably selecting the V_{GS} and I_{DS} , which is referred to as Biasing.

Different types of biasing ~~are~~ are :

(i) Gate bias or fixed bias : Here a dc voltage V_{DD} is connected to drain to source through a Resistor R_D , and that another dc voltage V_{GS} is applied between gate to source. This biasing method is called fixed bias, because, the gate to source voltage is fixed by a constant voltage across its terminals. It is also called as gate bias because the voltage source is connected at the Gate.

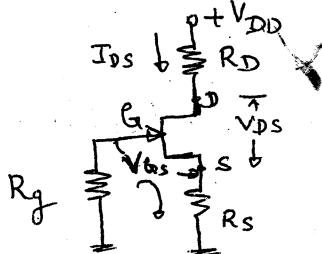


$$V_{DD} = I_{DS} R_D + V_{DSQ}$$

$$V_{DSQ} = V_{DD} - I_{DS} R_D$$

Here the Q point is not maintained constant to parameter variation of the device.

Self Bias: When V_{DD} is applied, a drain current I_{DS} flows even in the absence of gate voltage source V_g . The voltage drop across resistor R_s produced by drain current I_{DS} is given by $V_s = I_{DS}R_s$. This voltage drop reduces the V_{GS} required for FET operation.



$$V_{DS} = V_{DD} - I_{DS}(R_D + R_s)$$

applying KVL for Gs Loop $V_{GS} + I_g R_g + I_{DS} R_s = 0$

Since $I_g \approx 0$ $V_{GS} = -I_{DS} R_s$

$$V_s = I_{DS} R_s$$

Operation: When I_{DS} increases because of change in device parameters, increases the voltage drop across R_s . The increased voltage drop increases the reverse voltage applied to gate & V_{GS} which decreases the effective width of the channel and hence reduces the drain current.

If I_{DS} decreases the drop across R_s decreases, this will increase V_{GS} and increases I_{DS} .

$$I_{DS} \uparrow V_s \uparrow V_{GS} \uparrow I_{DS} \uparrow \quad I_{DS} \uparrow V_s \uparrow V_{GS} \uparrow I_{DS} \uparrow$$

Constant

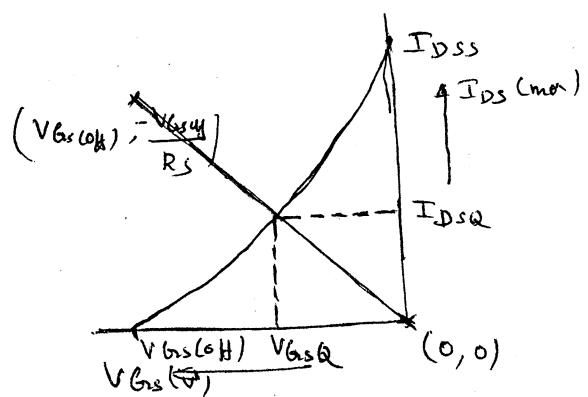
Because $I_{DS} = I_{DSS} \left(1 - \frac{V_{GS}}{V_{GS(\text{off})}}\right)^2$

Graphical Analysis (Procedure)

(b) Mutual Characteristic is drawn by using expression for current

$$I_{DS} = I_{DSS} \left(1 - \frac{V_{GS}}{V_{GS(\text{off})}}\right)^2$$

$V_{GS}(v)$	$I_{DS}(\text{mA})$
$V_{GS(\text{off})}$	0
$0.5 V_{GS(\text{off})}$	$\frac{I_{DSS}}{4}$
$0.3 V_{GS(\text{off})}$	$\frac{I_{DSS}}{2}$
0	I_{DSS}



(9)

② A bias line is drawn by using the expression

$$V_{GS} = -I_{DS}R_S$$

when $I_{DS} = 0$ $V_{GS} = 0$ first point is located at $(0,0)$

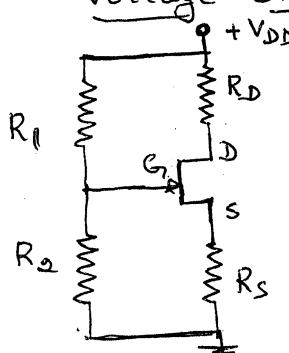
when $V_{GS} = V_{GS(\text{off})}$ calculate $I_{DS} = \frac{-V_{GS(\text{off})}}{R_S}$

Second point with coordinate $(V_{GS(\text{off})}, -\frac{V_{GS(\text{off})}}{R_S})$

These two above points are joined called bias line and its cut mutual characteristic at coordinate (V_{DSQ}, I_{DSQ})

$$\text{Then } V_{DSQ} = V_{DD} - I_{DSQ}(R_D + R_S)$$

Voltage Divider Bias



By applying Thevenin theorem to the Gate terminal we can write an eqn. Circ for load to source

$$V_{TH} = V_g = \frac{V_{DD}R_2}{R_1 + R_2}$$

$$R_{TH} = R_g = \frac{R_1 R_2}{R_1 + R_2}$$

In this circ the voltage V_{GS} is derived from V_{DD} and drop across R_S . The V_{GS} is calculated as follows

Applying KVL for Gate to Source loop

$$V_g = I_g R_g + V_{GS} + I_{DS}R_S$$

$$V_S = I_{DS}R_S$$

$$\therefore V_{GS} = V_g - I_{DS}R_S$$

Working: When I_{DS} increases because of variation of Parameter the drop across R_S increases, thus decreases V_S , this in turn decreases I_{DS} because of decrease in effective width of the channel. And vice versa for decrease in I_{DS}

$$I_{DS} \uparrow V_S \uparrow V_{GS} \downarrow I_{DS} \downarrow$$

compensated

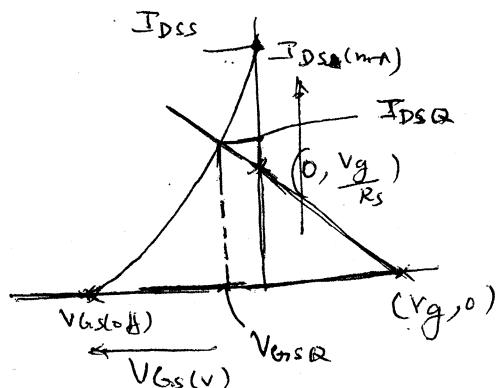
Graphical Analysis

(10)

- (1) To draw Mutual characteristic curve

$$I_{DS} = \sqrt{I_{DSS}^2 \left(1 - \frac{V_{GS}}{V_{GS(BH)}} \right)^2}$$

<u>$V_{GS}(V)$</u>	<u>$I_{DS}(mA)$</u>
$V_{GS(0A)}$	0
$0.5 V_{GS(BH)}$	$\frac{I_{DSS}}{4}$
$0.3 V_{GS(BH)}$	$\approx \frac{I_{DSS}}{2}$
0	$\star I_{DSS}$



- (2) To draw bias line

$$V_{GS} = V_g - I_{DS} R_s$$

$$\text{if } I_{DS} = 0 \quad V_{GS} = V_g \quad (V_g > 0)$$

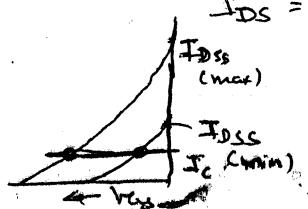
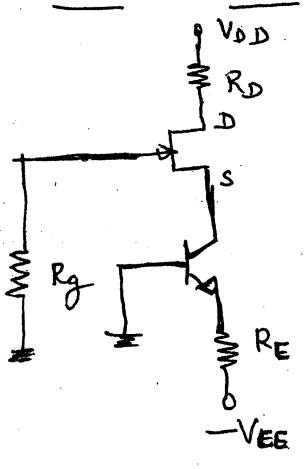
$$V_{GS} = 0 \quad I_{DS} = \frac{V_g}{R_s} \quad (0, \frac{V_g}{R_s})$$

The above two points are joined to get bias line
The intersection of bias line and Mutual characteristic giving the
coordinates of Qpt V_{GSQ} and I_{DSQ}

$$(3) \quad V_{DSQ} = V_{DD} - I_{DSQ} (R_D + R_s)$$

Current - Source Bias : when the drain supply is not large, there may not be enough gate voltage to swamp out the variations in V_{GS} . In this case this type of biasing is used. In this circuit the bipolar transistor pumps a fixed current through the FET. The drain current is given by

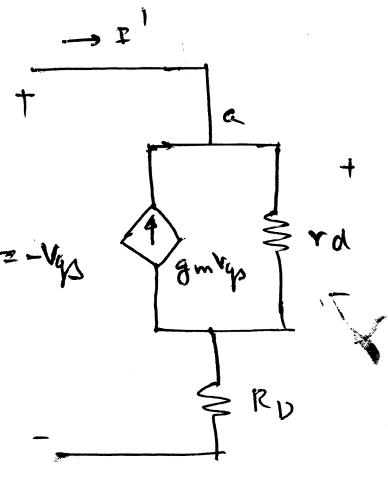
$$I_{DS} = \frac{V_{EE} - V_{BE}}{R_E}$$



Since both Qpoints are same. Although V_{GS} is different for each Qpoint V no longer has an effect on I_{DS}

To find Z

Apply KVL we get $V' - V_{rd} - V_{R_D} = 0$



$$V_{rd} = V' - V_{R_D}$$

$$I_{rd} r_d = V' - V_{R_D}$$

$$(I' + g_m V_{GS}) r_d = V' - V_{R_D}$$

$$(I' - g_m V') r_d = V' - I' R_D$$

$$I' (r_d + R_D) = V' (1 + g_m r_d)$$

$$Z_o = \frac{V'}{I'} = \frac{r_d + R_D}{1 + g_m r_d} = r_d \left(1 + \frac{R_D}{r_d} \right)$$

$$Z_o = \frac{1 + R_D/r_d}{\frac{1}{r_d} + g_m} \approx \frac{1}{g_m} \mid r_d \gg 10 R_D$$

$$Z_i = Z_o || R_S = R_S || 1/g_m \mid r_d \gg 10 R_D.$$

$$Z_o \text{ Setting } V_{ci} = 0 \quad Z_o = R_D || r_d.$$

$$Z_o = R_D \mid r_d \gg 10 R_D$$

A_v Applying KVL to above Ckt

$$V' = V_{rd} + V_o$$

$$V' = (I' + g_m V_{GS}) r_d + V_o$$

$$V = -V_{GS} = V_o$$

$$\therefore V_o = \left[\frac{V_o}{R_D} - g_m V_o \right] r_d + V_o$$

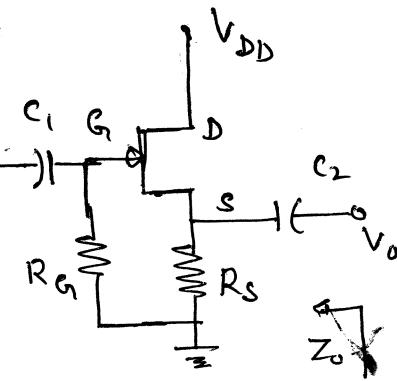
$$V_o [1 + g_m r_d] = V_o \left[\frac{r_d}{R_D} + 1 \right]$$

$$\frac{V_o}{V_o} = A_v = \frac{1 + g_m r_d}{1 + \frac{r_d}{R_D}} = \frac{R_D [1 + g_m r_d]}{R_D + r_d}$$

$$A_v = \frac{\left[g_m R_D + \frac{R_D}{r_d} \right]}{\left[1 + R_D/r_d \right]} = g_m R_D \mid r_d \gg 10 R_D.$$

Phase Relationship: Positive Value of A_v indicates that $o_1 < o_2$ Voltage or Inphase.

JFET Source-Follower (Common Drain) Configuration



$$Z_i = R_{G_s}$$

Z_o Set $V_i = 0$

$$\therefore V_{gs} + V_o = V_i$$

$$\therefore V_o = -V_{gs}$$

Apply KCL at op loop. $I_o + g_m V_{gs} = I_{R_D} + I_{rd}$

$$I_o + g_m V_{gs} = \frac{V_o}{R_S} + \frac{V_o}{r_d}$$

$$I_o = V_o \left[\frac{1}{R_S} + \frac{1}{r_d} \right] - g_m V_{gs}$$

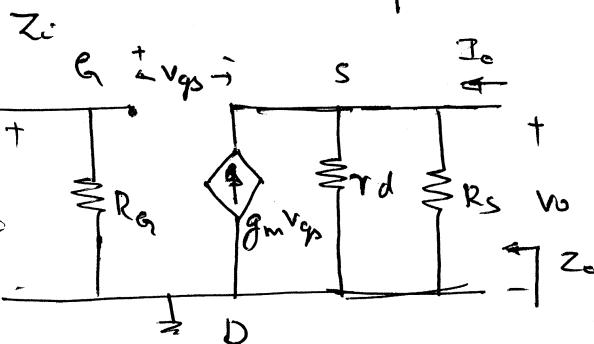
$$I_o = V_o \left[\frac{1}{R_S} + \frac{1}{r_d} \right] - g_m (-V_o)$$

$$I_o = V_o \left[\frac{1}{R_S} + \frac{1}{r_d} + g_m \right]$$

$$\frac{V_o}{I_o} = Z_o = \frac{1}{\frac{1}{R_S} + \frac{1}{r_d} + g_m} = \frac{1}{\frac{1}{R_S} + \frac{1}{r_d} + \frac{1}{g_m}}$$

$$Z_o = r_d \parallel R_S \parallel \frac{1}{g_m}$$

$$Z_o \approx R_S \parallel \frac{1}{g_m} \mid r_d > 10R_S$$



To find A_v

$$V_o = g_m V_{gs} (r_d \parallel R_S)$$

$$V_{gs} = V_i - V_o$$

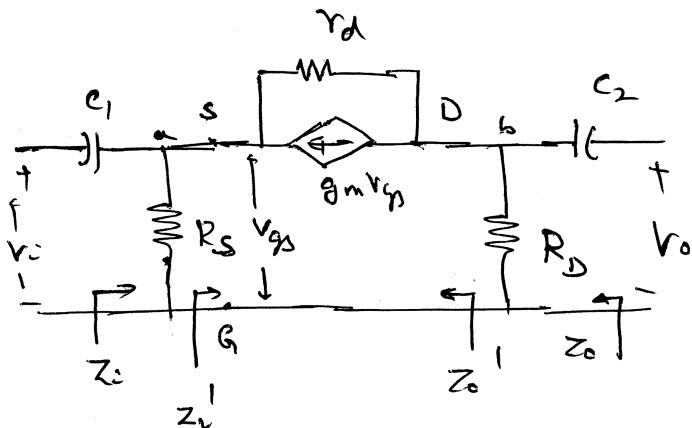
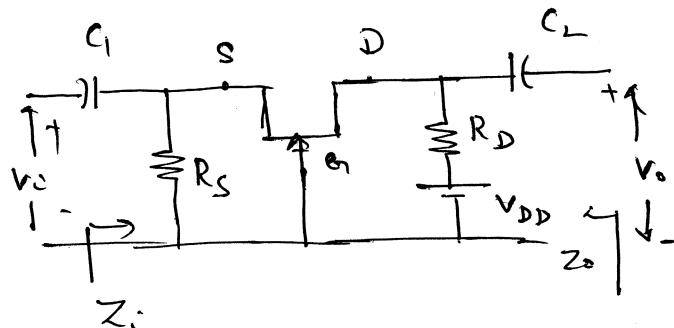
$$\therefore V_o = g_m (V_i - V_o) (r_d \parallel R_S)$$

$$V_o (1 + g_m (r_d \parallel R_S)) = g_m V_i (r_d \parallel R_S)$$

$$\frac{V_o}{V_i} = A_v = \frac{g_m (r_d \parallel R_S)}{1 + g_m (r_d \parallel R_S)} = \frac{g_m R_S}{1 + g_m R_S} \quad \mid r_d > 10R_S$$

Phase Relationship: Positive voltage gain indicates there is no phase shift between $I_{LP} \approx 0_{LP}$.

JFET Common-Gate Configuration



By Applying KCL to the o/p Loop we get

$$I_d = g_m V_{gs} + \frac{V_o - V_{gs}}{r_d}$$

$$I_d = g_m [V_i - I_d R_S] + \frac{(-I_d R_D) - (I_d R_S)}{r_d}$$

$$I_d \left[1 + g_m R_S + \frac{R_D + R_S}{r_d} \right] = g_m V_i$$

$$I_d = \frac{g_m V_i}{1 + g_m R_S + \frac{R_D + R_S}{r_d}}$$

The o/p Voltage $V_o = -I_d R_D = -\frac{g_m V_i R_D}{1 + g_m R_S + \frac{R_D + R_S}{r_d}}$

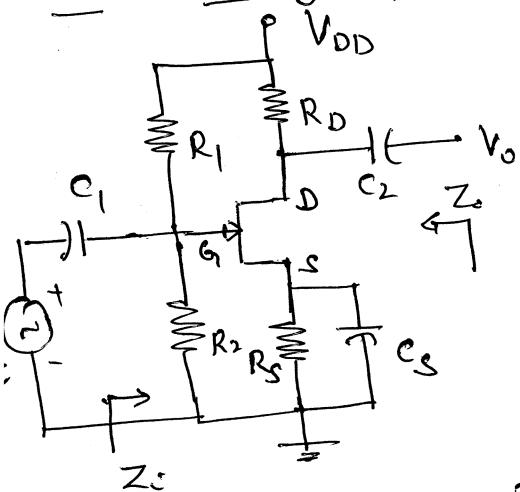
$$A_v = \frac{V_o}{V_i} = -\frac{g_m R_D}{1 + g_m R_S + \frac{R_D + R_S}{r_d}}$$

If $r_d \gg 10(R_D + R_S)$

$$A_v \approx -\frac{g_m R_D}{1 + g_m R_S}$$

Phase Relationship: Negative Sign Indicates 180° Phase shift between I/p & o/p.

JFET - Voltage Divider Bias Configuration:



$$Z_i = R_1 \parallel R_2$$

$$Z_o : \text{Setting } V_i = 0 = V_{gs} = g_m V_{gs}$$

$$\therefore Z_o = r_d \parallel R_D$$

$$Z_o = R_D / r_d \gg 10R_D$$

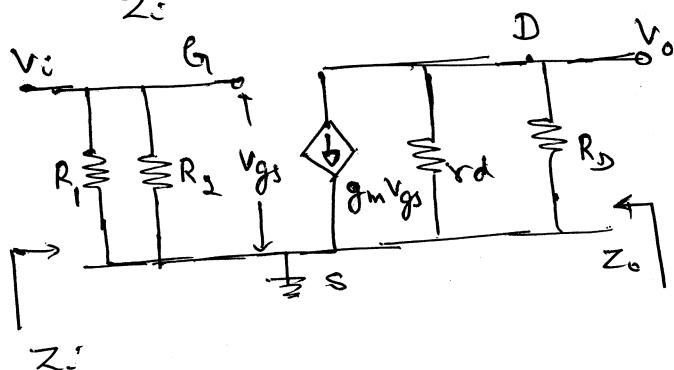
$$A_v = \frac{V_o}{V_i} = -g_m V_{gs} (r_d \parallel R_D)$$

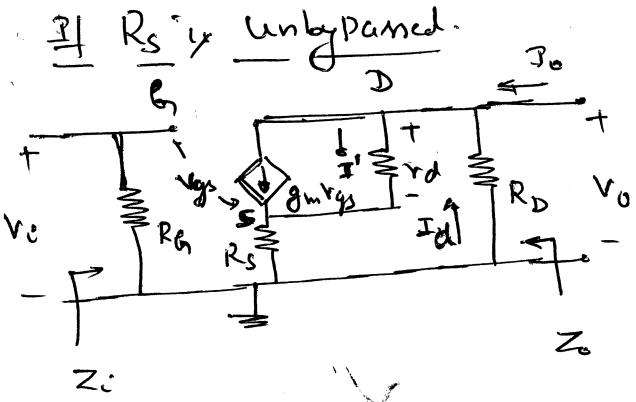
$$A_v = \frac{V_o}{V_i} = -\frac{g_m V_{gs} (r_d \parallel R_D)}{V_i}$$

$$V_{gs} = V_i$$

$$\therefore A_v = -g_m (r_d \parallel R_D)$$

$$A_v \approx -g_m R_D / r_d \gg 10R_D$$





$$Z_o = R_D$$

$$\text{To find } Z_o \quad V_i = 0$$

$$Z_o = \frac{V_o}{I_o} \quad |_{V_i=0} = -\frac{I_d R_D}{I_o}$$

$$I_o = g_m V_{gs} + I_{rd} - I_d$$

$$V_{rd} = V_o + V_{gs} \quad (\because V_{gs} + V_{rs} = V_i = 0 \\ \therefore V_{rs} = -V_{gs})$$

$$I_o = g_m V_{gs} + \frac{V_o + V_{gs}}{r_d} - I_d$$

$$I_o = g_m V_{gs} + \frac{(-I_d R_D) + V_{gs} - I_d}{r_d}$$

$$I_o = V_{gs} \left(g_m + \frac{1}{r_d} \right) - I_d \left(\frac{R_D}{r_d} + 1 \right)$$

$$V_{gs} = -V_{rs} = -(I_d + I_o) R_S$$

$$Z_o = -(I_d + I_o) R_S \left[g_m + \frac{1}{r_d} \right] - I_d \left[\frac{R_D}{r_d} + 1 \right]$$

$$I_o \left[1 + g_m R_S + \frac{R_S}{r_d} \right] = -I_d \left[1 + g_m R_S + \frac{R_S}{r_d} + \frac{R_D}{r_d} \right]$$

$$I_o = \frac{- \left[1 + g_m R_S + \frac{R_S}{r_d} + \frac{R_D}{r_d} \right] I_d}{1 + g_m R_S + \frac{R_S}{r_d}}$$

$$Z_o = \frac{V_o}{I_o} = \frac{-I_d R_D}{- \left[1 + g_m R_S + \frac{R_S}{r_d} + \frac{R_D}{r_d} \right] I_d} = \frac{R_D}{1 + g_m R_S + \frac{R_S}{r_d}}$$

$$= R_D \left[\frac{1 + g_m R_S + \frac{R_S}{r_d}}{1 + g_m R_S + \frac{R_S}{r_d} + \frac{R_D}{r_d}} \right]$$

If $\frac{r_d}{R_D} \gg 1$ or $\frac{R_D}{r_d} \ll 1$

$$Z_o = R_D \left[\frac{1 + g_m R_S + \frac{R_S}{r_d}}{1 + g_m R_S + \frac{R_S}{r_d}} \right] = R_D$$

To find A_v By applying Kirchhoff's voltage law to the I_{Dp} ckt result

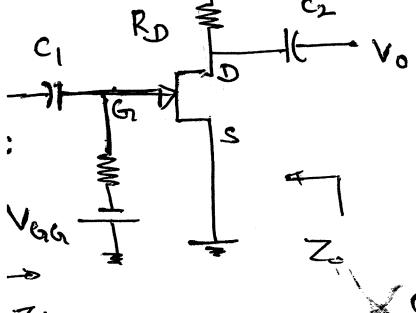
$$V_i - V_{gs} - V_{rs} = 0$$

$$V_{gs} = V_i - V_{rs}$$

$$V_{rd} = V_o - V_{rs}$$

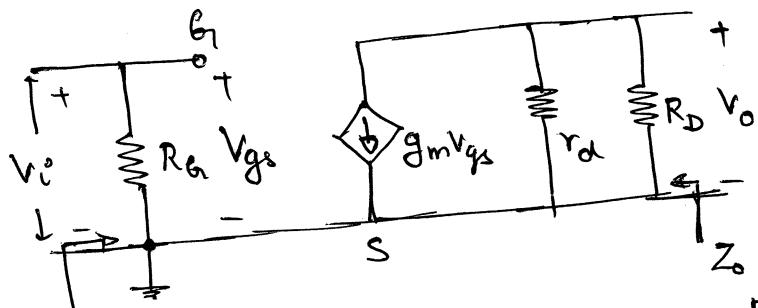
$$I' = I_{rd} = \frac{V_{rd}}{r_d} = \frac{V_o - V_{rs}}{r_d}$$

JFET Fixed Bias Configuration. g_d include Capacitance C_1 and C_2 which isolate the dc biasing arrangement from the applied signal and load; they act as short ckt equivalents for the ac analysis.



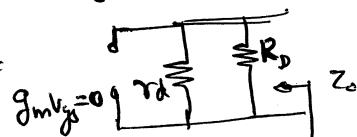
Once the levels of g_m and r_d are determined from the dc biasing arrangement, specification sheet or characteristics, the ac equivalent model can be substituted between the appropriate terminals.

$$Z_i = R_G$$



Z_o : By setting $V_i = 0$ as required by the definition of Z_o will establish $V_{gs} = 0$ which results in $g_m V_{gs} = 0$

Z_i : The equivalent ckt is



$$\therefore Z_o = r_d \parallel R_D$$

$$Z_o \approx R_D \quad | \quad r_d \gg 10R_D$$

$$\text{To find } A_v \quad V_o = -g_m V_{gs} \quad (r_d \parallel R_D)$$

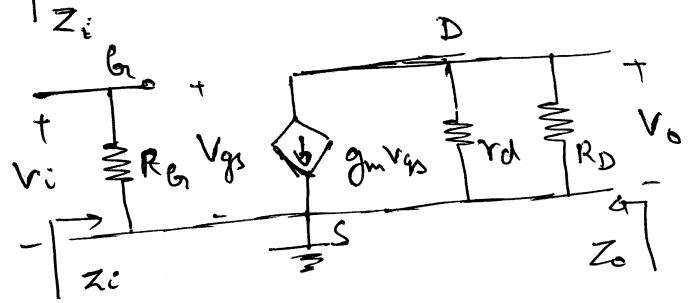
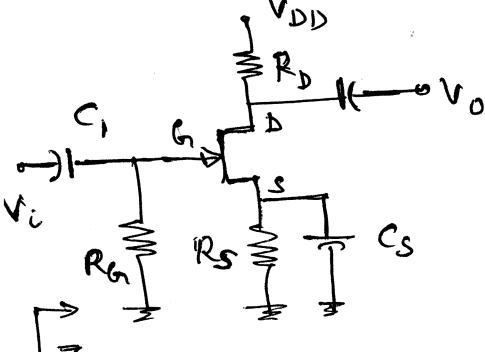
$$V_{gs} = V_i \quad \therefore V_o = -g_m V_i \quad (r_d \parallel R_D)$$

$$\frac{V_o}{V_i} = A_v = -g_m (r_d \parallel R_D) = -g_m R_D \quad | \quad r_d \gg 10R_D$$

Phase Relationship: The negative sign in the resulting equation for A_v , 180° between I_{p} & O_{p} voltages.

Clearly reveals a phase shift of 180° between V_i and V_o .

JFET Self-Bias Configuration: Since fixed bias requires two dc voltage sources, the self bias will become it uses only one voltage source. Under ac conditions C_1, C_2 and C_S will act as a short.



$$Z_i = R_G$$

$$Z_o = r_d \parallel R_D$$

$$Z_o \approx R_D \quad | \quad r_d \gg 10R_D$$

$$A_v = -g_m (r_d \parallel R_D)$$

$$A_v \approx -g_m R_D \quad | \quad r_d \gg 10R_D$$

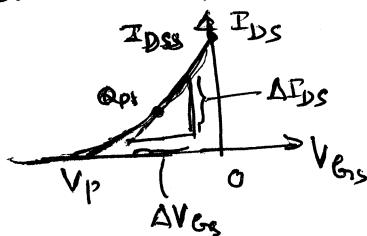
Phase Relationship: The negative sign in the solution for A_v again indicates a phase shift of 180° between V_i and V_o .

FET Small-Signal Model : The major component of the ac model will reflect the fact that an ac voltage applied to the I_{Dp} gate-to-source terminals will control the level of current from drain to source. The gate-to-source voltage controls the drain-to-source (channel) current of an FET. The dc gate-to-source voltage controls the level of dc current through the relationship known as Shockley's equation $I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_p}\right)^2$. The change in collector current that will result from a change in gate-to-source voltage can be determined using the transconductance factor g_m in the following manner.

$$\Delta I_D = g_m \Delta V_{GS}$$

The prefix trans- in the terminology applied to g_m reveals that it establishes a relationship between an ac ΔI_D & an I_{Dp} quantity $\therefore g_m = \frac{\Delta I_D}{\Delta V_{GS}}$

Graphical Determination of g_m : This can be calculated from the transfer characteristics.



$$\text{WKT } I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_p}\right)^2$$

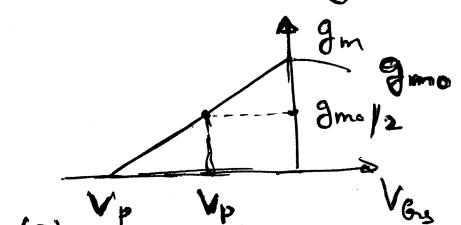
$$\begin{aligned} \frac{dI_D}{dV_{GS}} &= \frac{d}{dV_{GS}} \left[I_{DSS} \left(1 - \frac{V_{GS}}{V_p}\right)^2 \right] \\ &= I_{DSS} \frac{d}{dV_{GS}} \left[1 - \frac{V_{GS}}{V_p} \right]^2 \\ &= 2 I_{DSS} \left[1 - \frac{V_{GS}}{V_p} \right] \left[0 - \frac{1}{V_p} \right] \end{aligned}$$

$$g_m = \frac{2 I_{DSS}}{|V_p|} \left[1 - \frac{V_{GS}}{V_p} \right]$$

$|V_p|$ denotes only magnitude

$$g_m = g_{mo} \left[1 - \frac{V_{GS}}{V_p} \right]$$

$$\text{where } g_{mo} = g_m |_{V_{GS}=0} = \frac{2 I_{DSS}}{|V_p|} \left[1 - \frac{0}{V_p} \right] = \frac{2 I_{DSS}}{|V_p|} \quad (S)$$



Effect of I_D on g_m

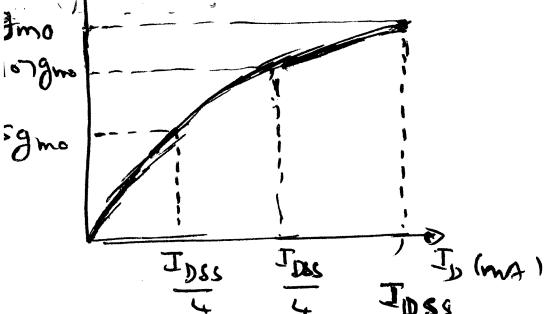
$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_p}\right)^2$$

$$\left(1 - \frac{V_{GS}}{V_p}\right) = \sqrt{\frac{I_D}{I_{DSS}}}$$

$$\text{WKT } g_m = g_{mo} \left(1 - \frac{V_{GS}}{V_p}\right)$$

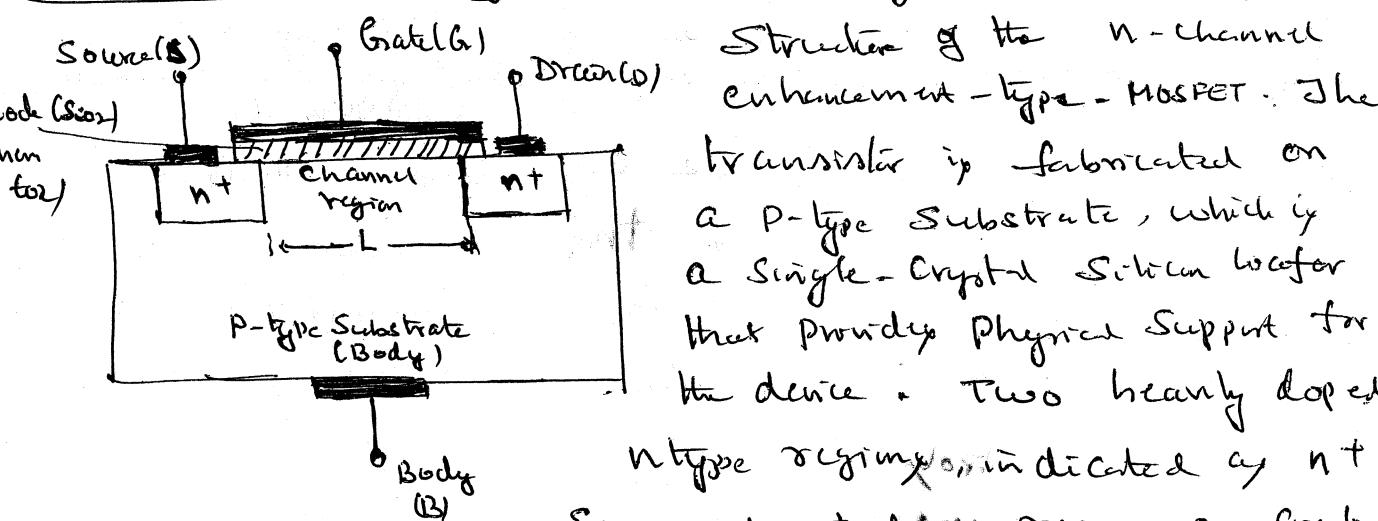
$$g_{mo} \left(1 - \frac{V_{GS}}{V_p}\right) = g_{mo} \sqrt{\frac{I_D}{I_{DSS}}}$$

$$g_m = g_{mo} \sqrt{\frac{I_D}{I_{DSS}}}$$



- MOSFETs Occupying Small Area in the Silicon IC Chip and Manufacturing Process is relatively Simple.
- Its Operation requires comparatively less Power
- To Implement Analog and digital functions utilizing MOSFET requires very few or no resistors.
- All above property makes using 100 million MOSFET in a Single Chip, which helps in VLSI Design like memory and microprocessor etc.
- They can be used in analog Circuits such as Amplifiers and filters and both Analog and digital Circuits can be implemented on the same chip, called mixed VLSI design.

Device Structure and Physical Operation



Structure of the N-channel enhancement-type MOSFET. The transistor is fabricated on a P-type Substrate, which is a single-crystal silicon wafer that provides physical support for the device. Two heavily doped N-type regions, indicated by n⁺, Source at n⁺ and Drain regions are created in the Substrate. A thin layer of silicon dioxide (SiO₂) layer of thickness t_{ox} (typically 2nm - 50nm), which is an excellent electrical insulator, is grown on the Surface of the Substrate covering the area between the Source and drain regions. Metal is deposited on the top of the oxide layer to form gate electrode of the device. Metal ~~and~~ Contact are also made to Source, drain region and the Substrate, also known as body. The four terminals of the device are Gate terminal (G), the Source terminal (S), the drain terminal (D) and the Substrate and body terminal (B).

The name of the device (Metal-Oxide-Semiconductor FET) is derived from the Physical Structure. In fact most modern

modern MOSFETs are fabricated using a process known as silicon gate technology, in which polysilicon is used to form the gate electrode.

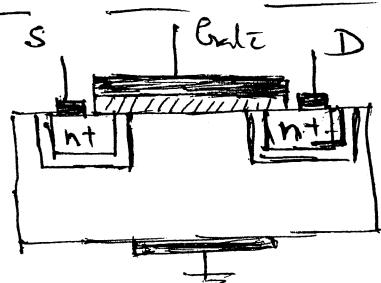
Another name for the MOSFET is the insulated gate FET or IGFET. They come from the fact that the gate electrode is electrically insulated from device body. Because they insulate the current by very low of the order 10^{-15} A .

The Substrate forms PN Junctions between Source and Drain regions. In normal operation these PN Junctions are kept reverse biased at all times. Since drain will be at a positive voltage relative to the source, the two PN Junctions can be effectively cut off by simply connecting the substrate terminal to the source terminal. Therefore the substrate will not have any effect in MOSFET operation.

and it can be treated as three terminal device, with terminal being the gate (G), the source (S) and the drain (D). It will be shown that the voltage applied to gate controls current flow from drain to source.

The current will flow in longitudinal direction from drain to source in the region labelled as 'Channel region'. This region will have length 'L' ranging from 0.1 mm to 3 mm and width 'W' in the range of 0.1 mm to 100 mm.

MOSFET is a symmetrical device, thus if source and drain can be interchanged with no change in device characteristics, Operation with no Gate Voltage



With no bias voltage applied to the gate, two back-to-back diodes exist in series between drain and source. One diode is formed by PN Junction

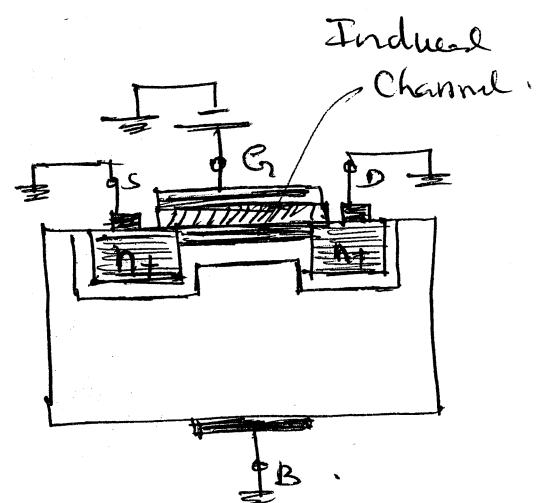
1-3

between the n^+ drain region and P-type Substrate and the other electrode is formed by the PN Junction between the P-type Substrate and the n^+ Source region. These back-to-back diodes prevent current conduction from drain to source when a voltage V_{DS} is applied. The resistance between drain and source has very high resistance of the order of $10^{12} \Omega$.

Creating a Channel for Current flow

Here a Positive Voltage is applied at the gate terminal and grounded Source and Drain. Since the Source is grounded, the gate voltage appears in effect between gate and source and thus is denoted as V_{GS} . The positive voltage on the gate causes the free holes to be repelled from the region of the substrate under the gate. As well, the positive gate voltage attracts electrons from n^+ source and drain regions into the channel region. When a sufficient number of electrons accumulate near the surface of the substrate under the gate, the connection is made between source and drain.

The induced n region thus forms a channel for current flow from drain to source, therefore it is called n channel MOSFET or alternatively NMOS transistor. The n channel MOSFET is formed on a P-type substrate. The channel is created by inverting the substrate surface from P to n type. Hence induced channel is also called as Inversion Layer.



The value of V_{GS} at which sufficient number of mobile electrons accumulate in the channel region to

form conducting channel is called threshold voltage V_t .
 V_t for n-channel MOSFET is positive and it typically lies in the range of 0.5V to 1V.

The gate and the channel region of the MOSFET form a parallel-plate capacitor with oxide layer acting as a capacitor dielectric. The positive gate voltage causes positive charge to accumulate on the top plate of the

capacitor (the gate electrode). The corresponding negative charge on the bottom plate is formed by the electrons in the induced channel. An electric field thus develops in the vertical direction. It is this field that controls the amount of charge in the channel and thus it determining the channel conductivity as current flows through the channel when a voltage V_{DS} is applied.

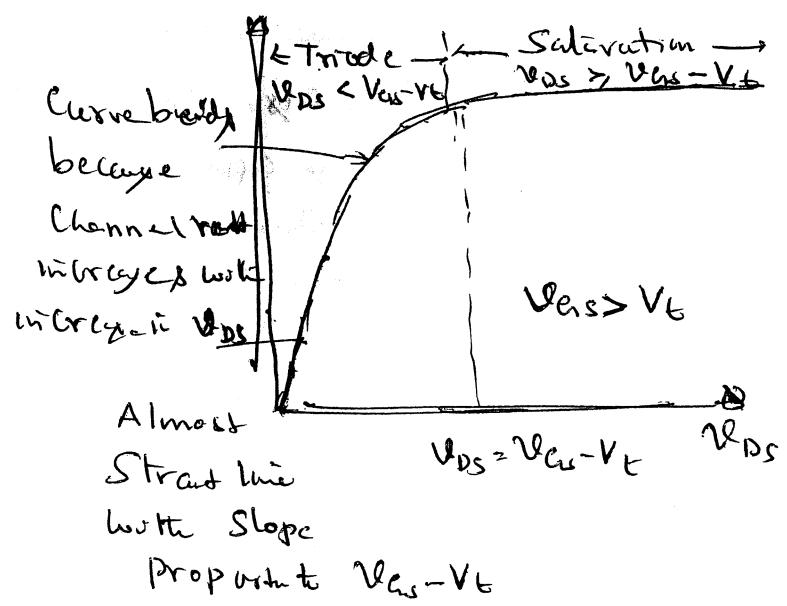
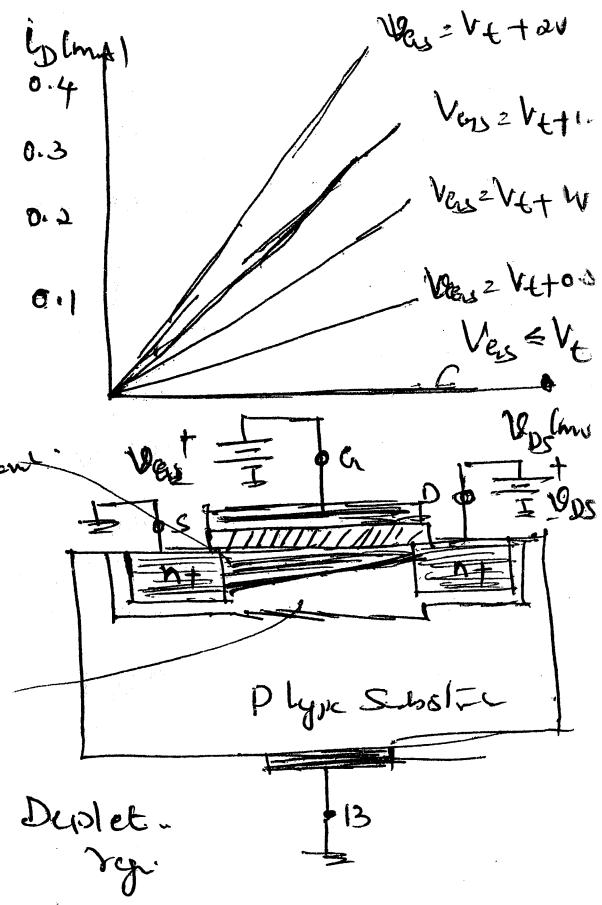
Applying a Small V_{DS} : First we consider a small V_{DS} is applied between drain and source (in tens mV). The voltage V_{DS} causes a current to flow through the induced channel. Current is carried by free electrons travelling from Source to Drain (hence its name Source and Drain). The current to will flow from Drain to Source which is opposite to flow of electrons. The magnitude of I_D depends on the density of electrons in the channel, which in turn depends on the magnitude of V_{DS} . Specifically $V_{DS} = V_t$, the channel is just induced and the current flow is negligibly small. As V_{DS} exceeds V_t , more electrons are attracted into the channel. We may visualize increase in charge carriers in the channel as an increase in channel depth. The increase in V_{DS} will decrease the resistance of the channel. In fact the conductance of the channel is proportional to

to the excess gate voltage ($V_{GS} - V_t$) also known as effective voltage or the overdrive voltage. It follows that the current I_D will be proportional to $V_{GS} - V_t$ and of course to the voltage V_{DS} , that causes I_D to flow.

The MOSFET is called enhancement MOSFET, because conductivity can be enhanced after applying a positive gate voltage with V_{GS} greater than V_t .

Operation as V_{DS} is increased

Here will consider V_{DS} is increased. Indeed by keeping V_{GS} constant and it is greater than V_t , note that V_{DS} appears as a voltage drop across the length of the channel. That is as we travel along the channel from source to drain, the voltage increases from 0 to V_{DS} . Thus the voltage between gate and point along the channel decreases from V_{GS} at some end to $V_{GS} - V_{DS}$ at the drain end. Since the channel depth depends on this voltage, we find that the channel is no longer of uniform depth, rather the channel tapers from as shown in the fig. As V_{DS} is increased, the channel becomes more tapered and the resistance increases increasing currents and

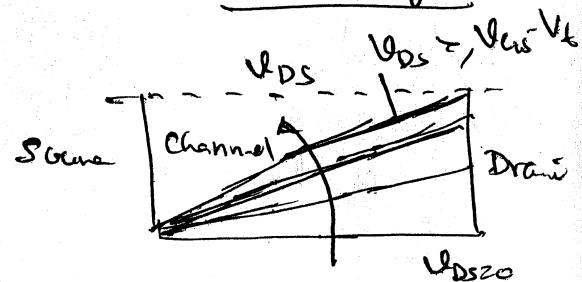


resistance increases currents and

When V_{DS} is increased to the value that reduces the voltage between gate and channel at the drain end to V_f that is $V_{GS} = V_f$ or $V_{GS} - V_{DS} = V_f$ or $V_{DS} = V_{GS} - V_f$. The channel depth at the drain end decreases to almost zero, and the channel is said to be Pinched off. Increasing V_{DS} beyond this value has little effect on the channel shape and the current through the channel remains constant at the value reached for $V_{DS} = V_{GS} - V_f$. The drain current thus saturates at this value and the MOSFET is said to have entered saturation region of operation. The voltage at which saturation occurs is denoted as $V_{DSsat} = V_{GS} - V_f$.

When $V_{DS} < V_{DSsat}$, the region called as the triode region.

The fig shows the effect of V_{DS} on the channel depth from Source to Drain region.

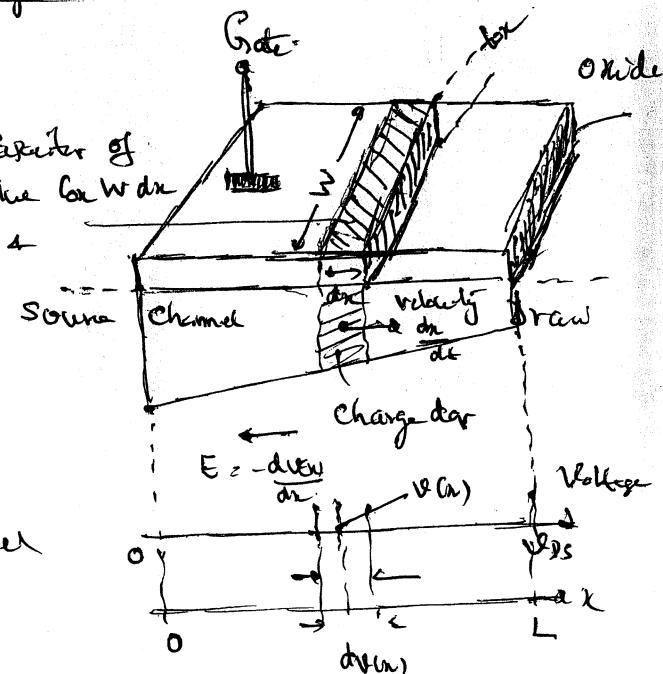


Derivation of the $I_D - V_{DS}$ Relationship

First we assume that V_{GS} is applied between gate and Source with $V_{GS} > V_f$ to induce channel. Also assuming that voltage V_{DS} is applied between drain and Source. Initially, we shall consider

operation in a triode region, for which the channel must be continuous and thus V_{GS} must be greater than V_f or $V_{GS} > V_{GS} - V_f$. In this case channel will have the tapered shape.

In the MOSFET, the gate and the channel region form a parallel plate capacitor for which the oxide layer serves as dielectric. If the capacitance per unit gate area is denoted by C_{ox} and thickness



of the Oxide layer is too thin

1.7

$$C_{ox} = \frac{E_{ox}}{t_{ox}} \quad \text{where } E_{ox} \text{ Permittivity of Silicon dioxide}$$
$$t_{ox} = 3.9 t_{ox} = 3.9 \times 8.854 \times 10^{-12}$$
$$= 3.45 \times 10^{-11} \text{ F/m}$$

The Oxide thickness is determined by the process technology used to fabricate the MOSFET. If $t_{ox} = 10 \text{ nm} (10 \times 10^{-9} \text{ m})$, then

$$C_{ox} = 3.45 \times 10^{-3} \text{ F/m}^2 \text{ or } 3.45 \text{ fF/um}^2 (3.45 \times 10^{-15} \text{ F/um}^2)$$

Now we will consider the infinitesimal strip of the gate at a distance x from the source. The Capacitance of this strip is $C_{ox} W dx$. To find the charge stored on this infinitesimal strip of the gate capacitance, we multiply the capacitance by the effective voltage between the gate and the channel at Point x , where the effective voltage that is responsible for inducing the channel at Point x is $V_{GS} - V(x) - V_t$, where $V(x)$ is the voltage in the channel at the point x . It follows that the electron charge dq in the infinitesimal portion of the channel at Point x is $dq = -C_{ox} W dx (V_{GS} - V(x) - V_t)$

where -ve sign indicates the fact that dq is negative charge

The voltage V_{GS} produces an electric field along the channel in the negative x direction. At Point x this field can be expressed as

$$E(x) = -\frac{dV(x)}{dx}$$

The electric field $E(x)$ causes the electron charge dq to drift toward the drain with a velocity dv/dt

$$\frac{dx}{dt} = -M_n E(x) = M_n \frac{dV(x)}{dx}$$

where M_n is the mobility of electrons in the channel

Therefore resulting drift current

$$i = \frac{dq}{dt} = \frac{dq}{dx} \cdot \frac{dx}{dt}$$

$$i = C_{ox} \cdot W \cdot dx (V_{GS} - V(x) - V_t) \cdot M_n \frac{dV(x)}{dx}$$

$$i = -Mn \operatorname{Cox} W [V_{GS} - V_t - V_b] \frac{dV_{DS}}{dx}, \quad i_D = -i$$

$$dI_{DS} = -i \cdot dn = -Mn \operatorname{Cox} W [V_{GS} - V_t - V_b] dV_{DS}$$

Integrating both sides of above eqn. from $x=0$ to $x=L$

$$\text{and } V(0) = 0 \text{ to } V(L) = V_{DS}$$

$$\int_0^L dn = \int_0^{V_{DS}} Mn \operatorname{Cox} W [V_{GS} - V_t - V_{DS}] dV_{DS}$$

$$I_D = Mn \operatorname{Cox} \frac{W}{L} \left[(V_{GS} - V_t) V_{DS} - \frac{1}{2} V_{DS}^2 \right]$$

The above expression for the I_D - V_{DS} characteristic in the triode region. The value of the current at the edge of the triode region or beginning of the saturation region can be obtained by substituting $V_{DS} = V_{GS} - V_t$ resulting in

$$I_D = \frac{1}{2} Mn \operatorname{Cox} \left(\frac{W}{L} \right) (V_{GS} - V_t)^2$$

For given V_{GS} I_D remains constant as V_{DS} varied.

If $Mn \operatorname{Cox}$ is called Process trans Conduction Parameter

$$k_n' = Mn \operatorname{Cox} A_V^{-2}$$

$$\frac{W}{L} = \text{Aspect ratio.}$$

Prob Consider a process technology for which $L_{min} = 0.4 \mu\text{m}$,

$$t_{ox} = 8 \text{ nm} \quad Mn = 450 \text{ cm}^2/\text{V} \quad V_t = 0.7 \text{ V}$$

(i) Find C_{ox} and k_n'

(ii) For a MOSFET with $W/L = 8 \mu\text{m}/0.4 \mu\text{m}$, calculate the value of V_{GS} at V_{DSmin} needed to operate the transistor in the saturation region with a dc current $I_D = 100 \text{ mA}$

(iii) For the device in (ii) find the value of V_{GS} required to cause the device to operate at 1000 μA current for very small V_{DS}

$$(i) C_{ox} = \frac{C_{ox}}{t_{ox}} = \frac{3.9 t_0}{t_{ox}} = \frac{3.9 \times 8.854 \times 10^{-12}}{8 \times 10^{-9}} = \frac{3.45 \times 10^{-11}}{8 \times 10^{-9}}$$

$$C_{ox} = 4.32 \times 10^{-3} \text{ F/m}^2$$

$$k_n' = Mn C_{ox} = 450 \times 10^8 (\text{cm}^2/\text{V-s}) \times 4.32 \times 10^{-11} \text{ F/mm}^2$$

$$k_n' = 194 \text{ mA/V}^2$$

(ii) In Saturation region

$$i_D = \frac{1}{2} k_n' \frac{W}{L} (V_{DS} - V_T)^2$$

$$100 = \frac{1}{2} \times 194 \times \frac{8}{0.8} (V_{DS} - 0.7)^2$$

$$V_{DS} = 1.02 \text{ V}$$

$$V_{DS_{min}} = V_{DS} - V_T = 1.02 - 0.7 = \underline{\underline{0.32 \text{ V}}}$$

(iii) If $V_{DS} \gg V_{DS_{min}}$

~~$i_D = k_n' \frac{W}{L} (V_{DS} - V_T) V_{DS}$~~

$$r_{DS} = \frac{V_{DS}}{i_D} \mid \text{small } V_{DS}$$

$$r_{DS} = \frac{1}{k_n' \frac{W}{L} (V_{DS} - V_T)} = \frac{1}{194 \times 10^{-6} \times 10 (V_{DS} - 0.7)}$$

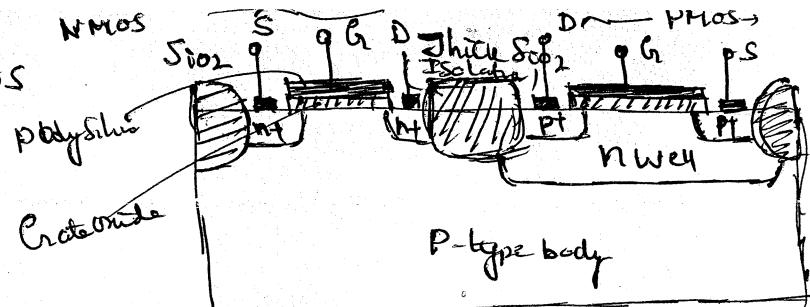
$$V_{DS} - 0.7 = 0.52$$

$$V_{DS} = 1.22 \text{ V}$$

The P Channel MOSFET: A P channel enhancement MOSFET (PMOS transistor), fabricated on an n-type substrate with p+ regions for the drain and source, has holes as charge carriers. It operates in the same manner as n-channel device except that V_{DS} and V_{GS} are negative and the threshold voltage V_T is negative. Also, the current flows into the source terminal and leaves through the drain terminal. Usually NMOS is preferred over PMOS because NMOS devices can be made smaller and they operate faster and also it requires lower supply voltages than PMOS. Both PMOS and NMOS transistors are utilized in complementary MOS or CMOS circuits.

Complementary MOS OR CMOS

Fig Shows the Cross Section of a CMOS Chip illustrating how the CMOS and NMOS transistors are fabricated. NMOS



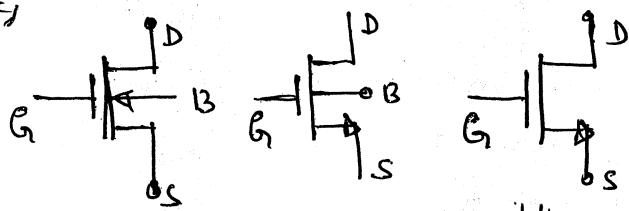
* NMOS is directly implemented in the P-type Substrate, the PMOS is implemented in a specially created N region known as an N well. The two devices are isolated from each other by thick regions of oxide that function as an insulator.

Operating the MOS Transistor in the Subthreshold Region If $V_{DS} < V_t$

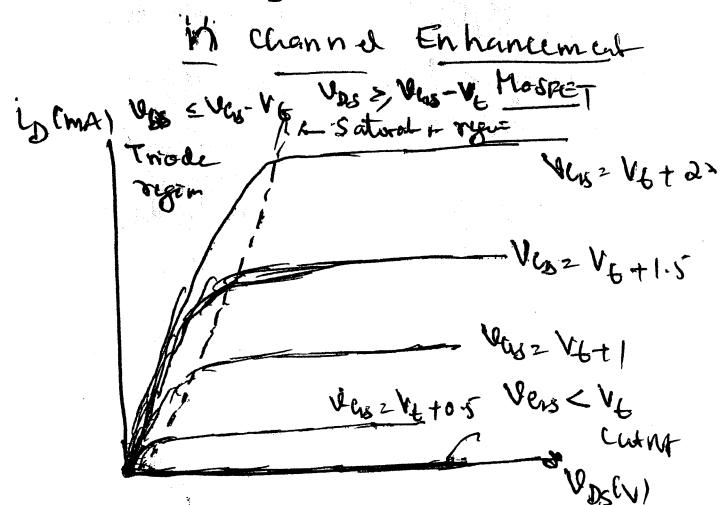
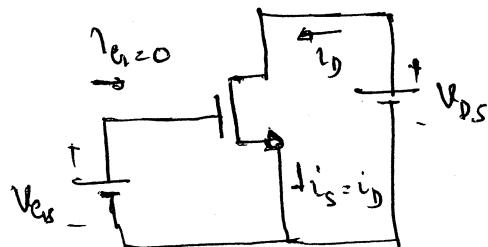
There is no current flow in the device to Cut-off. But this is not entirely true, for it has been found that for values of V_{DS} smaller than but close to V_t , a small drain current flows. In this Subthreshold region of operation the drain current is exponentially related to V_{DS} .

Current - Voltage Characteristics: These characteristics can be measured at dc or at low frequencies and are called Static Characteristics

Circuit Symbol



The $I_D - V_{DS}$ Characteristics



The MOSFET operates in 3 distinct regions of operation:
namely Cutoff region, the triode region and the Saturation region.
The Saturation region is used if MOSFET to be used as an amplifier.

For operation as a switch, the Cutoff and triode regions are used. The device is Cutoff when $V_{DS} < V_t$. To operate MOSFET in triode region we must first induce a channel.

$V_{GS} \geq V_t$ (Induced Channel)

and then keep V_{DS} small enough so that the channel remains continuous. This can be achieved by keeping the gate to drain voltage to $V_{DS} > V_t$ (continuous channel).

$$V_{DS} = V_{GS} - V_{DS} > V_t$$

or $V_{DS} < V_{GS} - V_t$ (continuous channel)

$$\text{In triode region } i_D = k_n \frac{W}{L} \left[(V_{GS} - V_t) V_{DS} - \frac{1}{2} V_{DS}^2 \right]$$

where $k_n = \mu n C_{ox}$ is the process transconductance parameter.

If V_{DS} is very small then we neglect V_{DS}^2

$$i_D = k_n \frac{W}{L} [(V_{GS} - V_t) V_{DS}]$$

This linear relationship represents the operation of the MOSFET as a linear resistance r_{DS} whose value is controlled by V_{GS} . Specifically if V_{GS} is a constant V_{GS} , then r_{DS} is given

$$\text{by } r_{DS} = \frac{V_{DS}}{i_D} \mid \begin{array}{l} V_{DS} = \text{small} \\ V_{GS} = V_{GS} \end{array} = \left[k_n \frac{W}{L} (V_{GS} - V_t) \right]^{-1}$$

If $V_{ov} = \text{gate to source overdrive voltage} = V_{GS} - V_t$

$$r_{DS} = \frac{1}{k_n \left(\frac{W}{L} \right) V_{ov}} \quad [\text{assuming } V_{DS} \ll 2V_{ov}]$$

To operate channel in saturation region, the channel must be induced. $V_{GS} \geq V_t$ (Induced channel)

and it is pinched off at the drain end by raising V_{DS} to a value that results in gate to drain voltage falling below V_t .

$V_{DS} \leq V_t$ (Pinched-off channel)

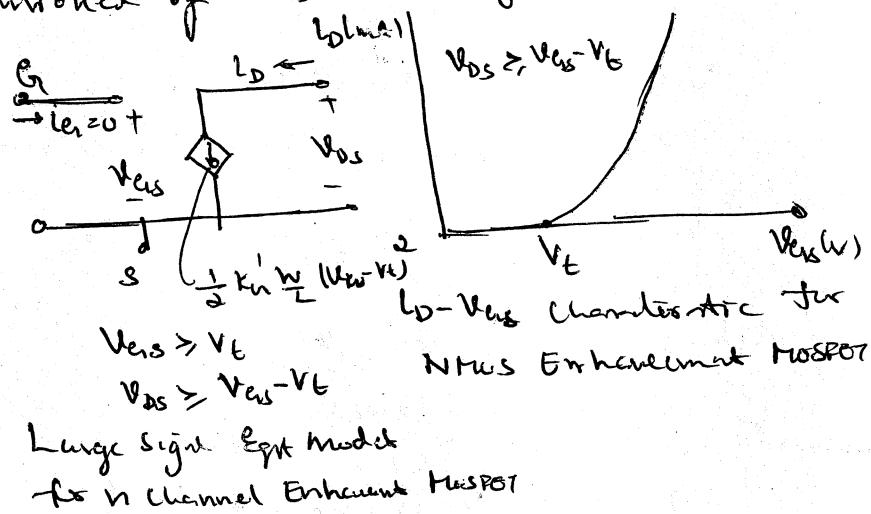
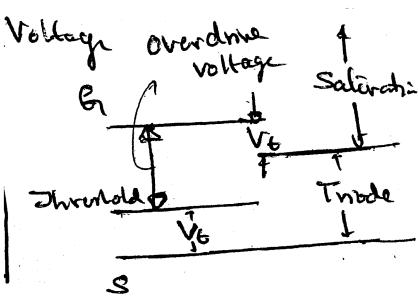
OR $V_{DS} \geq V_{GS} - V_t$ ("")

The boundary between the triode region and the saturation region is characterized by $V_{DS} = V_{GS} - V_t$ (Boundary)

$$\text{Saturation Current } I_D = \frac{1}{2} k_n \frac{W}{L} (V_{DS} - V_T)^2$$

In the saturation region, the MOSFET provides a drain current whose value is independent of the drain voltage V_{DS} and is determined by gate voltage V_{GS} according to the square-law relationship.

Since the drain current is independent of the drain voltage, the saturated MOSFET behaves as an ideal current source whose value is controlled by V_{GS} according to nonlinear relationship.

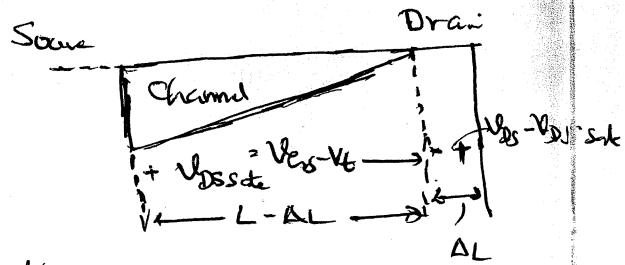


In the $I_D - V_{DS}$ characteristic, we note that boundary between the triode and saturation regions is shown by broken line. Since this curve is characterized by $V_{DS} = V_{GS} - V_T$, its equation can be found by substituting for $V_{GS} - V_T$ by V_{DS} in either the triode equation or the saturation-region equation. The result is

$$I_D = \frac{1}{2} k_n \frac{W}{L} V_{DS}^2$$

Finite Output Resistance in Saturation.

Initially we assumed that in saturation I_D is independent of V_{DS} and it remains constant. Therefore in saturation $\Delta I_D = 0$ and resistance is infinity. But in practice V_{DS} is increased beyond $V_{DS\text{sat}}$, the channel pinch-off point is moved slightly away from the drain, toward the source. From the fig we can see that the channel drop remains at $V_{DS\text{sat}} = V_{GS} - V_T$, but additional voltage drop $V_{DS} - V_{DS\text{sat}}$ appears across the narrow depletion region between the end of the channel to drain region.



The circuit diagram of the P-channel Mosfet

The figure shows three circuit configurations for a P-channel MOSFET (MOSFET P).

- (a) Common Drain:** The drain terminal is connected to the output node. The source terminal is connected to ground (-V_S) through a resistor R_S. The gate terminal is connected to the input node through a resistor R_G.
- (b) Common Source:** The source terminal is connected to ground (-V_S). The drain terminal is connected to the output node through a resistor R_D. The gate terminal is connected to the input node through a resistor R_G.
- (c) Common Gate:** The gate terminal is connected to the input node. The drain terminal is connected to the output node through a resistor R_D. The source terminal is connected to ground (-V_S) through a resistor R_S.

In all three cases, the drain voltage V_D is defined as the voltage across the drain resistor R_D, and the current I_D is the current flowing through R_D.

The drain current I_D is given by the equation:

$$I_D = \frac{K_P}{2} \frac{W}{L} (V_G - V_T)^2$$

where K_P = drain current / unit width = mobility of holes in channel.

To start = Saturation $V_{DS} \leq V_{GS} - V_T$ (Initial of char)

When $K_P = \frac{W}{L}$ then $I_D = K_P \frac{W}{L} [(V_G - V_T)(V_D - \frac{1}{2}V_T)]$

Want to get voltage by cut off

Want to get voltage by cut off $V_{GS} \geq V_T$

Want to get voltage by cut off $V_D \geq V_{GS} - V_T$ (minimum channel length)

If want to get voltage if $V_D \geq V_{GS} - V_T$ (minimum channel length)

at first step is this

or $V_{GS} \geq V_T$

Voltage $V_G \geq V_T$ (threshold Channel)

Channel to appear get voltage by more negative than the threshold voltage during the threshold voltage. To induce the p channel during the threshold voltage & negative. In lower resistance for normal operation as shown in fig (a). In lower resistance of the substrate, therefore fig (a) is best. In normal condition of the substrate, the normal current flows down to the substrate in the same direction. The normal direction of current flow is indicated in the diagram of the common drain configuration.

In the circuit shown the common drain Peltier is the normal direction of current flow.

$$R_o^2 = \frac{L}{I_D} = \frac{VA}{I_D} \text{ where } I_D \text{ is the drain current}$$

which changes light modulus

Effect is $I_D = \frac{1}{2} k_B \frac{h}{e} (V_{GS} - V_t)^2$

The large signal model is that of a current source with negative resistance

$$v_0 = \left[\sqrt{\frac{k_n}{m}} (V_{in} - V_t) \right]^{1/2}$$

$$V_{CS} = \frac{1}{\pi} \int_0^R ds$$

$$V_{\text{ext}} = \lim_{n \rightarrow \infty} \left[\frac{1}{n} \sum_{k=1}^n V_k \right]$$

The longer infinitely is successive as it is defined by

This voltage accelerates the electrons that reach the drain end of the channel and sweeps them across the depletion region into the drain. This reduces the channel length from L to $L - \Delta L$, and this phenomenon is known as Channel-length modulation. Now, since I_D is inversely proportional to the channel length, it increases with V_{DS} . To account for the dependence of I_D on V_{DS} in saturation we replace L by $L - \Delta L$ in the current equation.

$$I_D = \frac{1}{2} k_n' \frac{W}{L - \Delta L} (V_{DS} - V_t)^2$$

$$I_D = \frac{1}{2} k_n' \frac{W}{L} \cdot \frac{1}{\left(1 - \frac{\Delta L}{L}\right)} (V_{DS} - V_t)^2$$

$$I_D = \frac{1}{2} k_n' \frac{W}{L} \left(1 + \frac{\Delta L}{L}\right) (V_{DS} - V_t)^2 \quad \because \left(1 - \frac{1}{x}\right) \approx 1 + 2$$

Since $\frac{\Delta L}{L} \ll 1$ and ΔL is proportional to V_{DS}

$\Delta L = \lambda' V_{DS}$ where λ' is the process technology parameter with dimension mm/V

$$I_D = \frac{1}{2} k_n' \frac{W}{L} \left(1 + \frac{\lambda'}{L} V_{DS}\right) (V_{DS} - V_t)^2$$

Usually we denote $\frac{\lambda'}{L} = \lambda$ with unit V^{-1}

$$I_D = \frac{1}{2} k_n' \frac{W}{L} (1 + \lambda V_{DS}) (V_{DS} - V_t)^2$$

The fig shows the effect of channel length modulation and we observe that I_D depends on the factor $1 + \lambda V_{DS}$. We observe that $I_D = 0$ if

$$1 + \lambda V_{DS} = 0$$

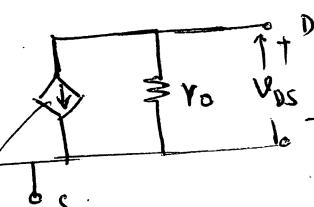
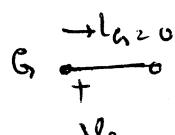
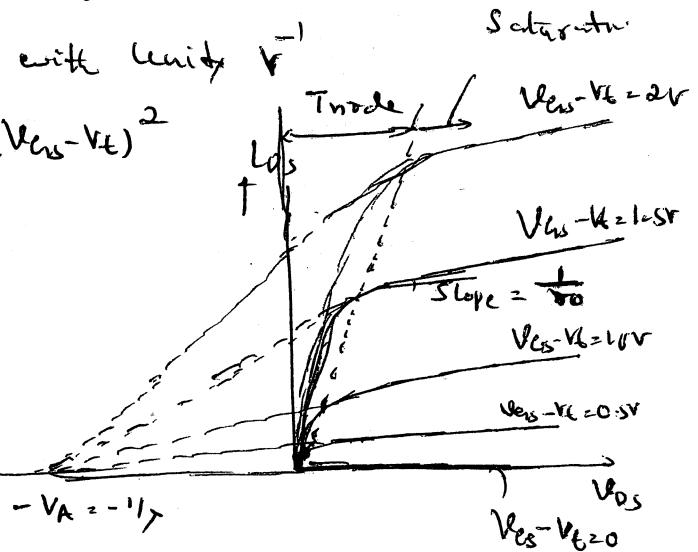
$$\therefore V_{DS} = -\frac{1}{\lambda} = -V_A$$

where V_A is positive.

$$i.e. V_A = \frac{1}{\lambda} \text{ denoted as } V \quad (\text{or } V_A = V_{AL})$$

Taking the effect of channel length modulation, the saturation value of I_D depends on V_{DS} . Thus for $V_{GS} = \text{const.} = V_{GS}$

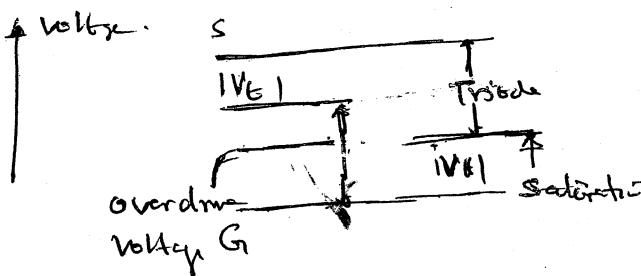
Change in V_{DS} yields change in I_D . Therefore op resistance



$$\frac{1}{2} k_n' \frac{W}{L} (V_{DS} - V_t)^2$$

while evaluating V_B , the magnitude of λ and V_{DS} are fixed - 115

The chart represents pictorial representation of operating conditions are shown below:



The Role of Substrate - The Body effect: In many applications the source terminal is connected to the substrate (or body) terminal B, which results in the pn junction between the substrate and induced channel having constant zero (cutoff) bias. In this case substrate does not play any role in circuit operation and it can be ignored.

In integrated circuits however, the substrate is usually common to many MOS transistors. In order to maintain the cutoff condition for all ~~the~~ substrate-to-channel junctions, the substrate is usually connected to the most negative supply in NMOS circuit (though the reverse is true in PMOS circuit). The resulting reverse-bias voltage between source and body (V_{SB} in the channel device) will have an effect on device operation. In case of NMOS transistor if the substrate made negative relative to the source, the reverse bias voltage will widen depletion region. This in turn reduces the channel depth. To return the channel to former case, V_{DS} has to be increased.

The effect of V_{SB} on the channel can be most conveniently represented as change in the threshold voltage V_t . Specifically it can be shown that increase in reverse substrate bias voltage V_{SB} results in increase in V_t according to relationship

$$V_t = V_{t0} + \gamma \left[\sqrt{2\phi_f} + V_{SB} - \sqrt{2\phi_f} \right]$$

where V_{t0} = Threshold voltage at $V_{SB}=0$. ϕ_f is the physical parameter with $2\phi_f$ being 0.6V and γ is the fabrication process parameter given by $\gamma = \frac{\sqrt{2qN_AeS}}{C_ox}$

where q is the electron charge = $1.6 \times 10^{-19} C$, N_A is the doping

Concentration of P type substrate and ϵ_s is the permittivity of Silicon $11.7 \text{ t}_0 = 11.7 \times 8.854 \times 10^{-14} = 1.04 \text{ F/Cm}$. The Parameter γ has the dimension of FV and it is typically $0.4 \text{ V}^{1/2}$. For P channel replace V_{GS} by $|V_{GS}|$ and γ is negative. While evaluating, N_A must be replaced by N_D , the doping concentration of the n well in which Pmosfet formed. For P channel device γ_{DOS} is typically 0.75V and γ typically $-0.5\text{V}^{1/2}$.

In the above equation incremental increase in V_{GS} results in incremental increase in V_t , which intern results in incremental change in I_D even though V_{GS} is constant. It follows the body voltage controls I_D , thus body acts as another gate in MOSFET. This phenomena is called body effect and γ is the body effect parameter. The body effect causes considerable degradation in the circuit performance.

Temperature effects: Both V_t and k' are temperature sensitive. The magnitude V_t decreases by about 2mV for every 1°C rise in temperature. This decrease in $|V_{GS}|$ increases the drain current. However, because of k' decreases with increase in temperature and its effect is dominant one, the overall observed effect of a temperature increase is a decrease in drain current. Thus effective decrease of current with increase in temperature Put MOSFET use in Power Circuits.

Breakdown and input protection: As the Voltage on the drain is increased, a value reached at which the PN junction between the drain region and substrate suffuses avalanche breakdown. This breakdown occurs at voltages of 20V to 150V and results in a somewhat rapid increase in current (known as heavy Avalanche).

Another breakdown effect that occurs at lower voltages ($\approx 20\text{V}$) in modern device is called punch-through. It occurs in the device with relatively short channels when the drain voltage is increased to the point that

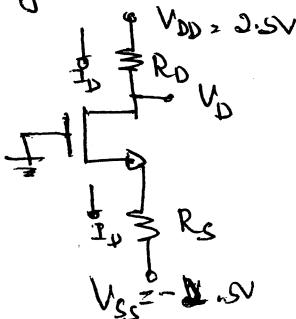
1.17

The depletion region surrounding the drain region extends through the channel to the source. The drain current then increases rapidly. Normally punch-through does not result in permanent damage to the device.

Yet another kind of breakdown occurs when gate-to-source voltage exceeds about 30V. This is the breakdown of gate oxide and results in permanent damage to the device. Although 30V may seem high, because the MOSFET has very high I_{DSS} resistance and a very small input capacitance, and thus small amount of static charge accumulating on the gate capacitor can cause its breakdown voltage to be exceeded.

MOSFET Circuit at DC : Having studied the current-voltage characteristics of MOSFET's, we now consider circuits in which only dc voltages and currents are concerned. In the following analysis we will neglect the channel-length modulation in the anode $\lambda \approx 0$, we will find it convenient to work in terms of the overdrive voltage; $V_{ov} = V_{GS} - V_t$. For NMOS V_t and V_{ov} are positive, while for PMOS, V_t and V_{ov} are negative. Therefore for PMOS we may write $V_{GS} = |V_{as}| = |V_t| + |V_{ov}|$

Prob
Design the circuit shown in the fig so that the transistor operates at $I_D = 0.4\text{mA}$ and $V_D = +0.5\text{V}$. The NMOS transistor with $V_t = 0.7\text{V}$, $mn_{Cox} = 100\text{mA/V}^2$, $L = 1\text{nm}$ and $W = 32\text{nm}$. Neglect the channel length modulation effect



Soln Since $V_{GS} = V_{as} - V_{DS} < V_t$
the NMOS transistor operates in saturation regime

$$\therefore I_D = \frac{1}{2} mn_{Cox} \frac{W}{L} (V_{as} - V_t)^2$$

$$V_{as} = V_{GS} - V_t$$

$$I_D = 400 = \frac{1}{2} (100) \left(\frac{32}{1}\right) V_{ov}^2$$

$$\therefore V_{ov} = 0.5\text{V}$$

$$\therefore I_{DS} = 400\text{mA}$$

$$V_{or} = V_{es} - V_t$$

$$\therefore V_{es} = V_{or} + V_t = 0.5 + 0.7 = 1.2V$$

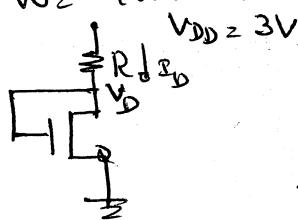
$$V_{es} = V_s - V_s = 0 - V_s = 1.2V$$

$$\boxed{V_s = -1.2V}$$

$$\therefore R_s = 1 \times \frac{V_s - V_{ss}}{I_D} = \frac{-1.2V - (-2.5V)}{0.4 \times 10^{-3}} = 3.25k\Omega$$

$$R_D = \frac{V_{DD} - V_D}{I_D} = \frac{2.5 - 0.5}{0.4} = 5k\Omega$$

Q) Design the circuit shown in the fig to obtain I_D of 80 mA. Find the value of R and find the de voltage V_D . Let the NMOS transistor have $V_t = 0.6V$, $UnCo = 200mV^2$, $L = 0.8\text{mm}$ and $W = 4\text{mm}$. Neglect channel length modulation effect ($\lambda = 0$)



$$\text{Since } V_{DS} = V_{es} - V_{DS} < V_t \\ = 0 < V_t$$

The NMOS transistor operates in saturation region

$$I_D = \frac{1}{2} UnCo \frac{W}{L} (V_{es} - V_t)^2$$

$$I_D = \frac{1}{2} UnCo \frac{W}{L} (V_{or})^2$$

$$V_{or} = \left[\frac{2I_D}{UnCo \frac{W}{L}} \right]^{\frac{1}{2}} = \left[\frac{2 \times 80}{(200)(4 \times 10^{-8})} \right]^{\frac{1}{2}} = 0.4V$$

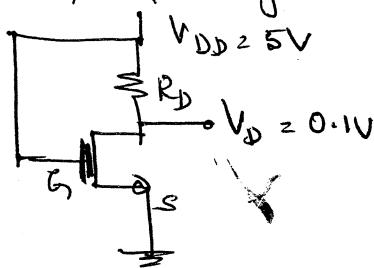
$$V_{or} = V_{es} - V_t$$

$$V_{es} = V_{or} + V_t = 0.4 + 0.6V = 1V$$

$$V_{es} = V_{DS} = 1V \quad \therefore R = \frac{V_{DD} - V_D}{I_D} = \frac{V_{DD} - V_{DS}}{I_D}$$

$$R = \frac{3-1}{0.08} = 25k\Omega$$

Design the Circuit shown in the fig to establish a drain voltage of 0.1V. What is the effective resistance between drain and source at this operating point? Let $V_t = 0$ and $k_n' (W/L) = 1 \text{ mA/V}^2$



$$V_{G,D} = V_{GS} - V_{DS} > V_t$$

The MOSFET operates in triode region

$$I_D = k_n' \frac{W}{L} \left((V_{GS} - V_t) V_{DS} - \frac{1}{2} V_{DS}^2 \right)$$

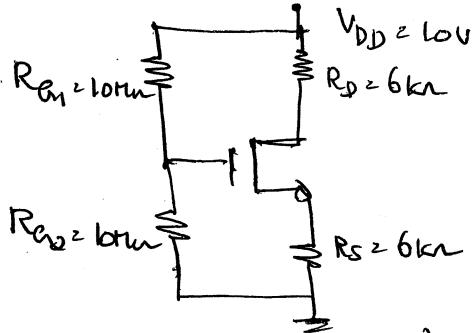
$$I_D = 1 \times 10^{-3} \left[(5-0) (0.1) - \frac{1}{2} (0.1)^2 \right]$$

$$I_D = 0.395 \text{ mA}$$

$$R_D = \frac{V_{DD} - V_D}{I_D} = \frac{5 - 0.1}{0.395 \times 10^{-3}} = 12.4 \text{ k}\Omega$$

$$r_{DS} = \frac{V_{DS}}{I_D} = \frac{V_D - V_S}{I_D} = \frac{0.1}{0.395 \times 10^{-3}} = 253 \text{ }\Omega$$

- (4) Analyze the Circuit shown in the fig to determine the voltages at all nodes and current through all branches. Let $V_t = 1\text{V}$ and $k_n' (W/L) = 1 \text{ mA/V}^2$. Neglect the channel length effect



$$V_{GS} = \frac{V_{DD} \cdot R_{G2}}{R_{G1} + R_{G2}} = 5\text{V}$$

Since voltage at the gate is +ve, the NMOS Transistor is on. But NMOS transistor maybe in triode region or in saturation region.

Assuming MOSFET is saturation

$$\text{we have } I_D = \frac{1}{2} k_n' (W/L) (V_{GS} - V_t)^2$$

$$V_{GS} = V_G - V_S = 5\text{V} - 6I_D$$

$$I_D = \frac{1}{2} \times 1 \times (5 - 6I_D - 1)^2$$

$$18I_D^2 - 25I_D + 8 = 0$$

$$\therefore I_D = 0.89 \text{ mA or } 0.5 \text{ mA}$$

$$\text{If } I_D = 0.89 \text{ mA then } V_S = 6 \times 0.89 \times 10^{-3} = 5.34 \text{ V}$$

which is greater than $V_t = 1\text{V}$ so I_D is not valid

$$I_D = 0.5 \text{ mA}$$

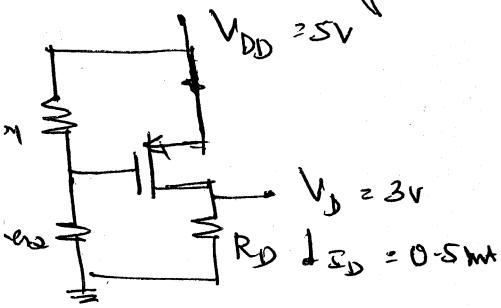
$$V_S = 0.5 \times 6 = 3 \text{ V}$$

$$V_{DS} = V_G - V_S = 5 - 3 = 2 \text{ V}$$

$$V_D = 10 - 6(0.5 \times 10^{-3}) = 7 \text{ V}$$

Since $V_D > V_D - V_t$, the MOSFET is Saturated.

Design the circuit shown in the fig so that the transistor operates in Saturation with $I_D = 0.5 \text{ mA}$ and $V_D = 3 \text{ V}$. Let enhancement PMOS transistors have $V_t = -W$ and $k_p' (W/L) = 1 \text{ mA/V}^2$. Assume $\lambda = 0$. What is the largest value that R_D can have while maintaining saturation region of operation?



$$I_D = \frac{1}{2} k_n \left(\frac{W}{L}\right) |V_{GS} - V_t|^2$$

$$I_D = \frac{1}{2} k_n \left(\frac{W}{L}\right) |V_{GS}|^2$$

$$0.5 = \frac{1}{2} (1) |V_{GS}|^2$$

$$V_{GS} = -1 \text{ V} \quad (\text{PMOS})$$

$$V_{DS} = V_t + V_{GS} = -1 - 1 = -2 \text{ V}$$

$$\text{Since } V_{DS} = -2 \text{ V} = V_D - V_S$$

$$V_D = -2 + V_S = -2 + 5 = 3 \text{ V}$$

$$V_D = V_{RS} = \frac{V_{DD} R_{RS}}{R_{RS} + R_{DS}} = 3 \text{ V}$$

$$\text{Choose } R_{RS} + R_{DS} = 5 \text{ mV}$$

$$R_{RS} = 2 \text{ mV} \quad R_{DS} = 3 \text{ mV}$$

$$R_D = \frac{V_D}{I_D} = \frac{3}{0.5} = 6 \text{ k}\Omega$$

To maintain in Saturation region

$$|V_{DS}| = |V_{GS} - V_t|$$

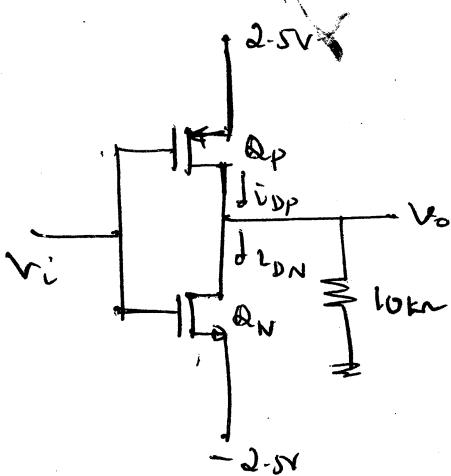
$$|V_{DS}| = |3 - 5 - (-1)|$$

$$|V_{DS}| = 1 = |V_D - V_S| \\ = |V_D - 5| \\ \therefore V_D = 4 \text{ V}$$

$$R_D = \frac{4}{0.5} = 8 \text{ k}\Omega$$

6. The NMOS and PMOS transistors are shown in the fig. Are 1:2 matched with $K_n^i (W_n/L_n) = K_p^i (W_p/L_p) = 1 \text{ mA/V}^2$

$V_{th} = -V_{tp} = 1 \text{ V}$ Assuming $\lambda = 0$ for both devices, find the drain current I_{Dp} at $V_{Dp} = 0$ as well as the voltages V_o for $V_i = 0 \text{ V}$, 2.5 V and -2.5 V .



If $V_i = 0$

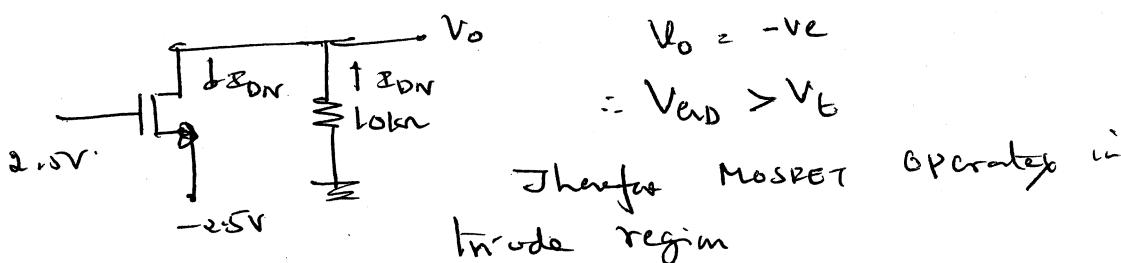
Then $|V_{ds}|$ for both NMOS and PMOS
to 2.5 V and $V_{Dp} = 0$ ($V_{Dp} < V_t$)

both device in saturation

$$\begin{aligned} I_{Dp} = I_{DN} &= \frac{1}{2} K_n^i \frac{W}{L} (V_{gs} - V_t)^2 \\ &= \frac{1}{2} \times 1 \times (2.5 - 1)^2 \\ &= \underline{\underline{1.125 \text{ mA}}} \end{aligned}$$

(ii) $V_i = 2.5 \text{ V}$

V_{gs} of $Q_p = 0 \therefore Q_p$ is cut off



$$I_{DN} = K_n^i \left(\frac{W}{L} \right) (V_{gs} - V_t) V_{ds}$$

$$I_{DN} = 1 [V_g - V_s - V_t] [V_o - (-2.5)]$$

$$I_{DN} = 1 [2.5 - (-2.5) - 1] [V_o + 2.5]$$

$$I_{DN} = [4][V_o + 2.5] =$$

$$I_{DN} = \frac{0 - V_o}{10k\Omega}$$

$$4V_o + 10 = -\frac{V_o}{10 \times 10^3}$$

$$4V_o + \frac{V_o}{10 \times 10^3} = -10$$

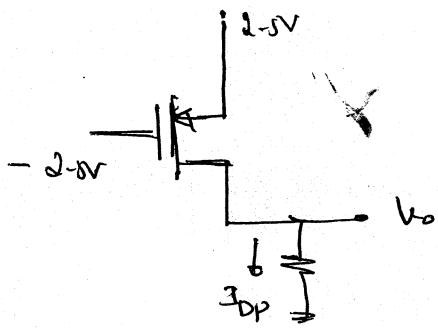
$$V_o = \frac{-10}{4.0001(4.1)} = -2.44 \text{ V}$$

$$\Rightarrow I_{DN} = 0.244 \text{ mA}$$

$$f V_i = -2.5V$$

$|V_{GS}|$ of NMOS = 0

$\Rightarrow Q_N \gg$ Cutoff



$$I_{DP} = k_p' (W/L) (V_{GS} - V_t) V_{DS}$$

$$I_{DP} = 1 [-2.5 - 2.5 - (-1)] [V_o - 2.5V]$$

$$I_{DP} = \frac{V_o}{10k\Omega}$$

$$-4 [V_o - 2.5] = \frac{V_o}{10k\Omega}$$

$$10 = 4 \cdot 10^3 k\Omega$$

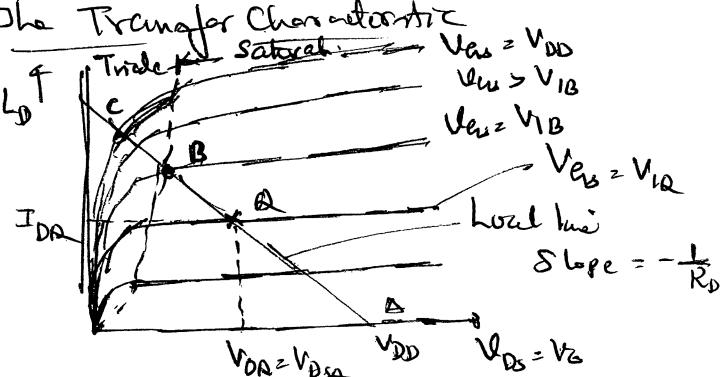
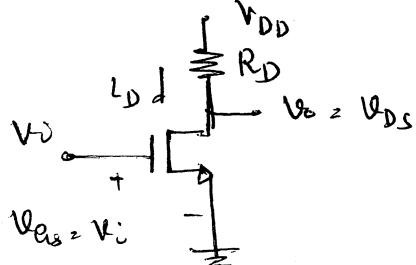
$$V_o = \frac{10}{4+1} = 2.44V$$

$$I_{DP} = \frac{V_o}{10k\Omega} = 0.244mA$$

The MOSFET As An Amplifier And As A Switch : MOSFET can be used in design of amplifier circuit. For this application, the MOSFET can be operated in saturation region, in this region the MOSFET acts as a Voltage Controlled Current Source. Change in Gate to Source voltage will give rise to change in I_D . Thus the saturated MOSFET can be used to implement a Transconductor amplifier. Since we are interested in linear amplification, we have to find a way to operate in linear region in a highly nonlinear relationship to V_D to V_{GS} .

The technique we will utilize to obtain linear amplification from a fundamentally nonlinear device is by Properly dc biasing the MOSFET by Properly choosing V_{GS} and I_D and then superimposing the voltage to be amplified, V_{GS} on the dc bias voltage V_{GS} . By keeping the signal V_{GS} small, the resulting change in current I_D can be made proportional to V_{GS} .

Large-Signal Operation - The Transfer Characteristic



Graphical derivation of the Transistor Characteristic

$$V_{DS} = V_{DD} - I_D R_D$$

$$I_D = \frac{V_{DD}}{R_D} - \frac{1}{R_D} V_{DS}$$

$$V_{DS} = V_{DD} \quad I_D = 0 \text{ has slope}$$

of $-1/R_D$ where R_D is the load resistor

One straight line shown in the fig is known as Loadline.

(i) If $V_i = V_{GS} < V_t$, the transistor is cut off

$$\therefore I_D = 0 \quad V_o = V_{DS} = V_{DD}$$

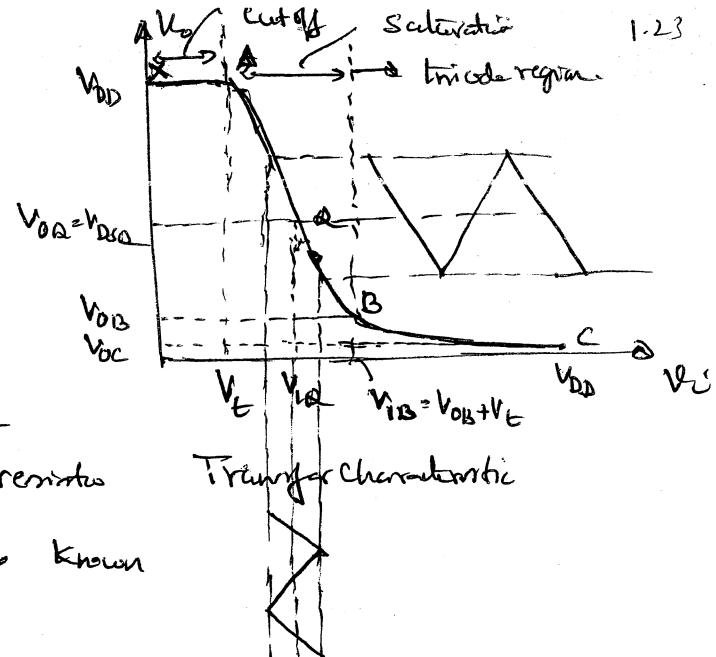
(ii) If $V_i = V_{GS}$ exceeds V_t , the transistor turns on, I_D increases and V_o decreases. Since $V_o = V_{DS}$ is initially high the transistor operates in Saturation Region. The operating point is selected between segment A and B. At P.t. $V_{GS} = V_{GA}$ and $V_{DS} = V_{DSA}$ at I_{DA} .

(iii) The Saturation region continues till V_o decreases to a point that is below V_i by V_t voltage. At this point $V_{DS} = V_{GS} - V_t$, the MOSFET enters into triode region. This is at the point B. i.e.

$$V_{DB} = V_{IB} - V_t$$

(iv) For $V_i > V_{IB}$, the transistor is driven deeper into triode region, then the o/p voltage decreases toward zero. Here $V_i = V_{DD}$, the corresponding output voltage is V_{OC} is very small.

Operation as a Switch : When MOSFET is used as a switch, it is operated at the extreme points of Transistor Characteristics. Specifically the device is turned off by keeping $V_i < V_t$, then $V_o = V_{DS} = V_{DD}$. The switch is turned on by applying $V_{GS} = V_i = V_{DD}$, then the resulting o/p voltage $V_o \approx 0$. This can be used as inverter.



1.23

Operation as a Linear Amplifier: To operate Mosfer as an amplifier we make use of the Saturation mode Segment of the transfer curve. The device is biased at a point located in the middle of the curve. This bias Point is also called Midpoint. The voltage that has to be amplitude to the superimposed on the dc voltage. By keeping V_i sufficiently small to restrict operation to an almost linear segment of the transfer curve, then the resulting output signal V_o will be proportional to V_i . Then the output voltage will have the same waveform as V_i except that it will be larger by a factor equal to the voltage gain of the amplifier at D where $A_v = \frac{dV_o}{dV_i} | V_i = V_{bias}$

Thus the voltage gain is equal to the slope of the transfer curve at bias point D. The slope negative indicates that the CS amplifier is inverting. If V_i is increased, then the output signal will be distorted since the operation will no longer be restricted to linear segment of transfer curve.

Selecting Criteria of the O/p

The D Point is selected at D_1 , then the transistor enters into triode region and the result is distortion in the negative cycle of the o/p. If D Point is selected at D_2 , then the transistor may enter into cutoff, then result is distortion in the +ve cycle of the o/p. Therefore O/p should be selected in such way that the o/p swing is maximum and undistorted.

Analytical Expression for the Transfer Characteristic

The Cutoff region Segment X A

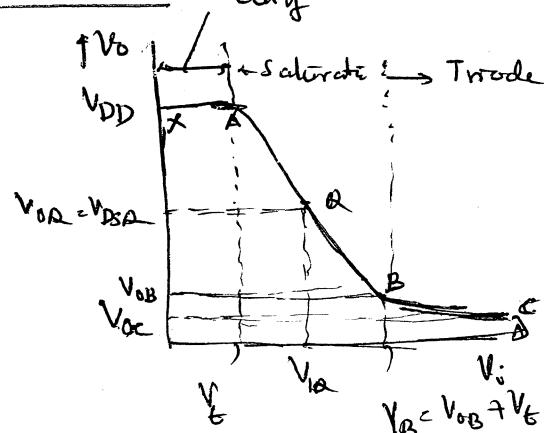
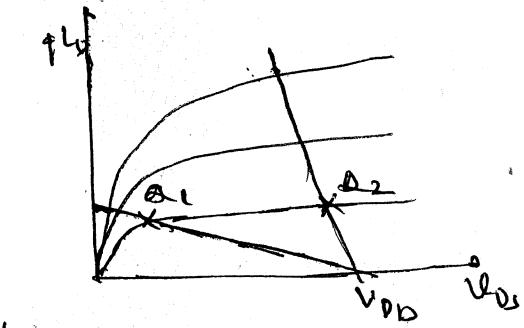
$$V_i < V_t \text{ and } V_o = V_{DD}$$

Saturation region Segment ADB

$$V_i > V_t \quad V_o \geq V_i - V_t$$

Neglecting Channel length modulation

$$I_D = \frac{1}{2} (\mu n C_s) \left(\frac{W}{L} \right) (V_i - V_t)^2$$



$$V_o = V_{DD} - R_D i_D$$

$$V_o = V_{DD} - \frac{1}{2} \frac{W}{L} \mu_n C_{ox} R_D (V_i - V_t)^2$$

The incremental voltage gain A_V at a break point & at which $V_i = V_{iQ}$ as follows

$$A_V = \left. \frac{dV_o}{dV_i} \right|_{V_i = V_{iQ}}$$

$$A_V = - R_D \mu_n C_{ox} \frac{W}{L} (V_{iQ} - V_t)$$

The voltage gain is proportional to R_D , transconductance parameter $\mu_n C_{ox}$, the transistor aspect ratio $\frac{W}{L}$ at overdrive voltage at the break point $V_{oQ} = V_{iQ} - V_t$

$$V_i = V_{iQ} \quad V_o = V_{oQ}, \text{ then}$$

$$V_{oQ} = V_{DD} + \frac{1}{2} A_V (V_{iQ} - V_t)$$

$$V_{oQ} = V_{DD} + \frac{1}{2} A_V V_{oQ}$$

$$A_V = - \frac{2(V_{DD} - V_{oQ})}{V_{oQ}} = - \frac{2V_{RD}}{V_{oQ}}$$

where $V_{RD} = V_{DD} - V_{oQ}$. is dc voltage drop across R_D

The end point of the saturation segment is characterized by $V_{oB} = V_{iB} - V_t$

The triode region segment BC

Here $V_i > V_t$ & $V_o \leq V_i - V_t$

$$i_D = \mu_n C_{ox} \frac{W}{L} [(V_i - V_t) V_o - \frac{1}{2} V_o^2]$$

$$V_o = V_{DD} - R_D i_D$$

$$V_o = V_{DD} - R_D \mu_n C_{ox} \frac{W}{L} [(V_i - V_t) V_o - \frac{1}{2} V_o^2]$$

V_o is very small. Then

$$V_o = V_{DD} - R_D \mu_n C_{ox} \frac{W}{L} (V_i - V_t) V_o$$

$$V_o = V_{DD} / [1 + R_D \mu_n C_{ox} \frac{W}{L} (V_i - V_t)]$$

$$\text{WKT } r_{DS} = \frac{1}{\mu_n C_{ox} \frac{W}{L} (V_i - V_t)}$$

$$V_o = \frac{V_{DD}}{1 + \frac{R_D}{r_{DS}}} = \frac{V_{DD} r_{DS}}{r_{DS} + R_D}$$

Usually $r_{DS} \ll R_D$.

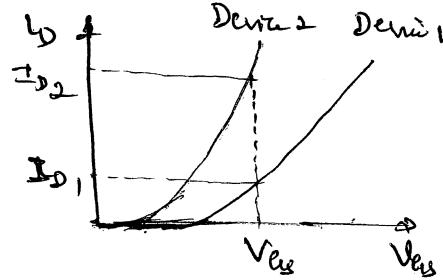
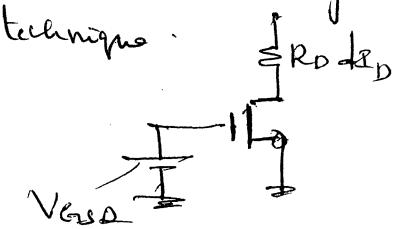
$$\therefore V_o = \frac{V_{DD} r_{DS}}{R_D}$$

Biasing in Mos Amplifier Circuit: The essential step in the design of Mos Amplifier Circuit is the establishment of an appropriate dc operating point for the transistor. This step is known as biasing or bias design. The Selection of Operating Point is to ensure that the Transistor operates in the saturation region for all expected input signal levels.

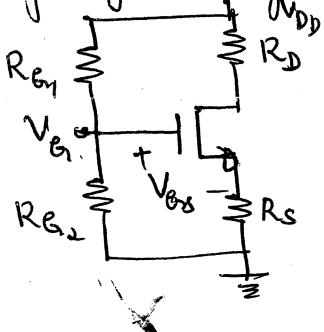
(i) Biasing by fixing V_{GS} : The most straightforward approach to biasing a MOSFET is to fix its gate to source voltage V_{GS} to the value required to provide the desired I_D . The voltage value can be derived from the Power Supply Voltage V_{DD} through the use of an appropriate voltage divider. Alternatively it can be derived from another suitable reference voltage V_t that might be available in the system. $\text{W.R.T. } I_D = \frac{1}{2} M \mu C_s \frac{W}{L} (V_{GS} - V_t)^2$

The value V_t , the oxide capacitance (to a lower contact), the transistor aspect ratio W/L vary widely among devices of same type and size. They are certainly in case of discrete device, in which large spread is in the values of these parameters occur among devices of the same manufacturer's part number. The spread is also large in integrated circuit, especially device fabricated on different wafer. Furthermore V_t at min is temperature dependent.

All these parameters makes current I_D to change in greater extent if one device is replaced by another device as shown in the fig. This means that fixing V_{GS} is not a good technique.



Bracing by fixing V_{GS} and connecting a resistance in the source.



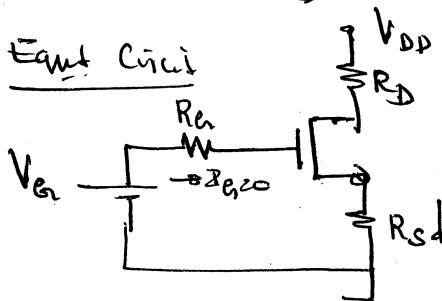
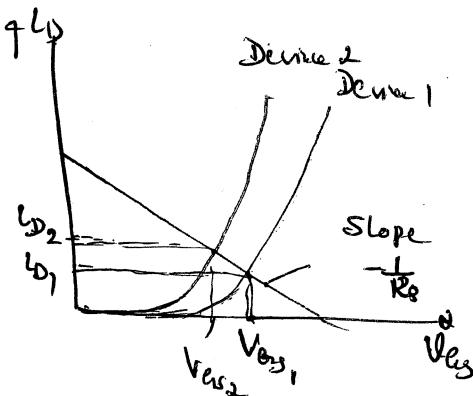
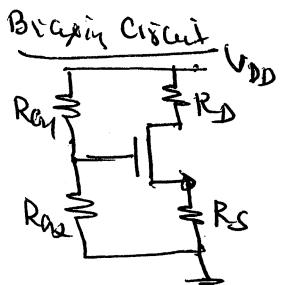
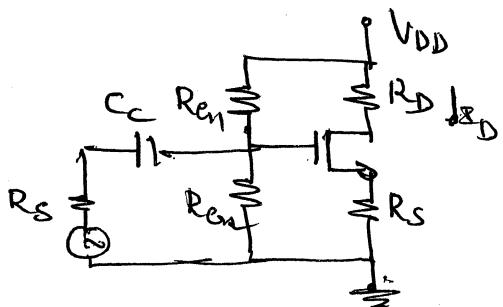
An excellent bracing technique for discrete MOSFET Circuits consisting of fixing the de voltage at the gate V_{GS} , and connecting a resistance in the Source lead.

$$V_{GS} = V_{GS0} + R_S I_D$$

$$V_{GS} = V_{GS0} - R_S I_D$$

Where R_S provides negative feedback, which acts to stabilize the value of the drain current I_D . When I_D increases, since V_G is constant, the V_{GS} decreases thus in turn decreasing I_D . Thus action of R_S works to keep I_D as constant as possible. This negative feedback action of R_S gives it the name degeneration resistance.

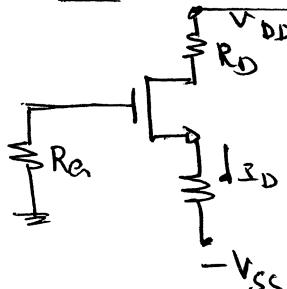
Circuit with one Supply



$$V_{GS} = V_{GS0} + R_S I_D$$

$$V_{GS} = V_{GS0} - R_S I_D$$

Circuit with two Supply



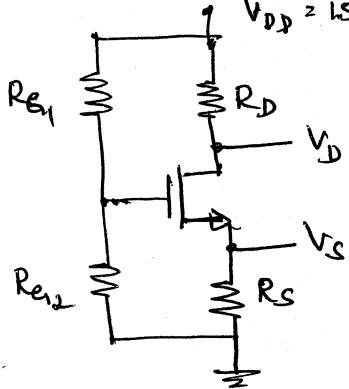
Applying G_2-S loop:

$$I_{DSS} + V_{GS0} + I_D R_S = V_{SS}$$

$$V_{GS0} = V_{SS} - I_D R_S$$

The Resistor R_S establishes a dc ground at the gate and presents a high input resistance to a signal source that may be connected to the gate through a coupling capacitor.

b It is required to design the circuit to establish a dc drawn current $I_D = 0.5 \text{ mA}$. The MOSFET is specified to have $V_t = 1\text{V}$ and $k_n W/L = 1 \text{ mA/V}^2$. Neglect the channel length modulation effect. The Power Supply $V_{DD} = 15\text{V}$. Calculate the percentage change in the value of I_D obtained when the MOSFET is replaced with another unit having the same $k_n W/L$ and $V_t = 1.5\text{V}$



$$\text{Chose } V_{RD} = V_{RS} = \frac{1}{3} V_{DD} = 5\text{V}$$

$$R_D = \frac{V_{DD} - V_D}{I_D} = \frac{15 - 10\text{V}}{0.5 \text{ mA}} = 10\text{k}\Omega$$

$$\text{WKT } I_D = \frac{1}{2} k_n \frac{W}{L} V_{ov}^2$$

$$0.5 = \frac{1}{2} \cdot 1 \text{ mA}^2$$

$$V_{ov} = 1\text{V} = V_{os} - V_t$$

$$V_{os} = V_{ov} + V_t = 2\text{V}$$

$$V_{R_{G2}} = V_o = V_{os} + V_{RS} = 2\text{V} + 5\text{V} = 7\text{V}$$

$$V_{R_{G2}} = \frac{V_{DD} R_{G2}}{R_m + R_{G2}} =$$

$$\text{Chose } R_m + R_{G2} = 15\text{M}\Omega$$

$$\therefore R_{G2} = \frac{V_{R_{G2}} (R_m + R_{G2})}{V_{DD}} = 7\text{M}\Omega$$

$$R_m = 8\text{M}\Omega$$

$$R_S = \frac{V_{RS}}{I_D} = \frac{5\text{V}}{0.5 \text{ mA}} = 10\text{k}\Omega$$

$V_D = 10\text{V}$ implying that it allows a positive swing of 5V

and negative swing of -4V . ($V_o - V_t$)

If NMOS transistor is replaced by another having $V_t = 1.5\text{V}$, the new value of $I_D = \frac{1}{2} (1) (V_{os} - V_t)^2$

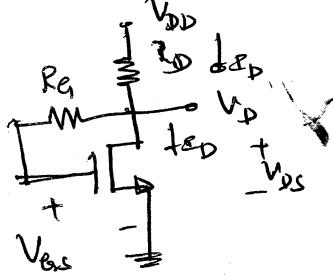
$$V_o = V_{os} + I_D R_S = V_{os} + 10 Z_D$$

$$I_D = \frac{1}{2} (7 - 10 Z_D - 1.5)^2 \Rightarrow Z_D = 0.458 \text{ M}\Omega$$

$$\Delta I_D = 0.455 - 0.5 = -0.045 \text{ mA}$$

$$\therefore \% \text{ Change} = \frac{-0.045}{0.5} \times 100 = -9\%$$

Braking Using a Drain to Gate Feedback Resistor



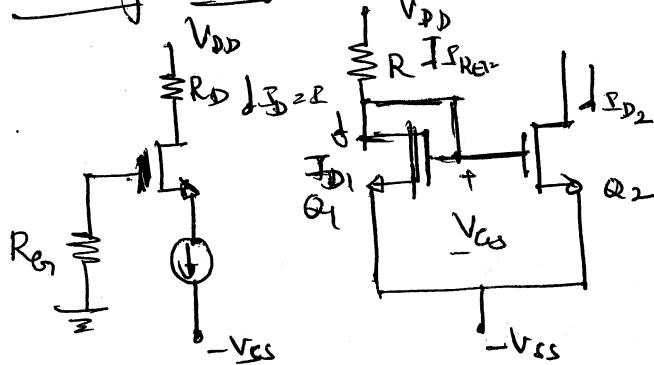
It is simple and effective braking circuit. Here large feed back resistance R_g (usually in MΩ) forces the dc voltage at the gate to equal to the drain.

$$V_{GS} = V_{DS} = V_{DD} - I_D R_D$$

If $I_D = V_{DS}/R_D$, then the negative feedback provided by R_g keeps the value of I_D constant. The ΔI_D is

provided by R_g . Keep the value of I_D constant. The ΔI_D is applied through a coupling capacitor so that it doesn't disturb the braking condition.

Braking Using a Constant Current Source:



R_g provides dc ground at the gate and provides large resistance to an input signal source that can be coupled to the gate through a capacitor.

R establishes an appropriate voltage at the drain to allow for the required output signal swing, while

ensuring that the transistor always stays in saturation region. Current mirror.

A circuit for implementing the Constant Current Source is shown in the fig. The heart of the circuit is transistors Q_1 whose drain is shorted to the gate and thus operating in saturation region. Such that $I_{D1} = k_n \left(\frac{W}{L} \right) (V_{GS} - V_t)^2$ By neglecting channel length modulation. The drain current of Q_1 is supplied by V_{DD} through a resistor R . Since gate current is zero.

$$I_{D1} = I_{REF} = \frac{V_{DD} + V_{SS} - V_{GS}}{R}$$

Current through resistor R is considered as reference current I_{REF} . Now consider transistor Q_2 , it has the same V_{GS} as Q_1 .

Thus if we assume that it's operating in saturation, the drain current, which is derived current I of current source, will be

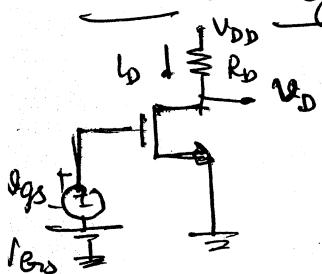
$$I = I_D = \frac{1}{2} k' n \left(\frac{w}{l}\right)_2 (V_{GS} - V_T)^2 \text{ neglecting channel length modulation effect.}$$

$$\frac{I}{I_D} = \frac{I}{I_{FRE}} = \frac{\frac{1}{2} k' n \left(\frac{w}{l}\right)_2 (V_{GS} - V_T)^2}{\frac{1}{2} k' n \left(\frac{w}{l}\right)_1 (V_{GS} - V_T)^2}$$

$$I = I_{FRE} \left(\frac{\left(\frac{w}{l}\right)_2}{\left(\frac{w}{l}\right)_1} \right)$$

The above circuit, known as Current mirror, is very popular in the design of IC Mes amplifiers.

Small-Signal Operation and Model



The DC Bias Point

The dc bias current I_D can be found by setting the signal $V_{GS} = 0$

$$I_D = \frac{1}{2} k' n \left(\frac{w}{l}\right) (V_{GS} - V_T)^2$$

$$\text{where } V_D = V_{DD} - I_D R_D$$

To ensure Saturation $V_D \geq V_{GS} - V_T$

Further, since the total voltage at the drain will have a signal component superimposed on V_D , V_D has to be sufficiently greater than $V_{GS} - V_T$ to allow for the required signal swing.

The Signal Current in the Drain Terminal

After applying signal V_{GS}

$$V_{GS} = V_{GS} + V_{GS}$$

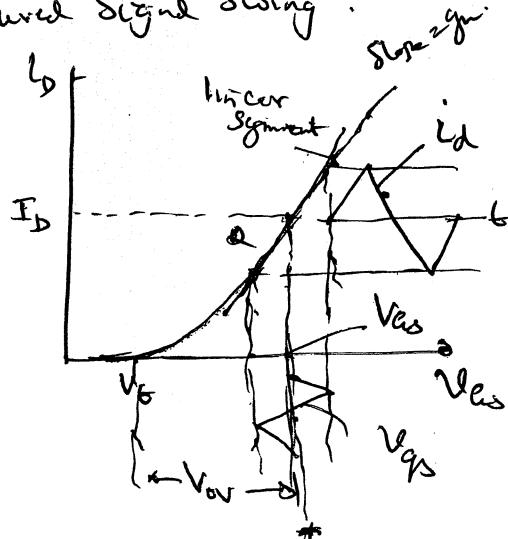
$$\therefore I_D = \frac{1}{2} k' n \left(\frac{w}{l}\right) (V_{GS} + V_{GS} - V_T)^2$$

$$I_D = \frac{1}{2} k' n \left(\frac{w}{l}\right) [V_{GS} - V_T]^2$$

$$+ \frac{1}{2} k' n \left(\frac{w}{l}\right) V_{GS}^2$$

$$+ k' n \frac{w}{l} (V_{GS} - V_T) V_{GS}$$

The 1st term is DC current, the third term represents the current proportional to I_D signal, but the second term is



Underdriven or lead to nonlinear characteristic. To reduce nonlinear distortion, the Z_{DP} signal should be very small

$$\frac{1}{2} k_n' \left(\frac{W}{L} \right) V_{GS}^2 \ll k_n' \frac{W}{L} (V_{GS} - V_T) V_{DS}$$

$$V_{GS} \ll 2(V_{GS} - V_T)$$

$$V_{GS} \ll 2V_{ov} \quad [V_{ov} = \text{overdrive voltage}]$$

If above condition is satisfied, then

$$I_D = I_D + I_d$$

$$\text{where } I_d = \frac{1}{2} k_n' \left(\frac{W}{L} \right) (V_{GS} - V_T) V_{DS}$$

$$\text{The drain current } g_m = \frac{I_d}{V_{DS}} = k_n' \left(\frac{W}{L} \right) (V_{GS} - V_T) = k_n' \frac{W}{L} V_{ov}$$

$$\text{From graph } g_m = \frac{I_d}{V_{DS}} \mid V_{GS} = V_{GS}$$

The voltage gain

$$\text{The drain voltage } V_D = V_{DD} - I_D R_D$$

$$V_D = V_{DD} - (I_D + I_d) R_D \quad V_{Dmin} \leq V_D \leq V_{Dmax}$$

The Signal component of drain voltage is, $V_d = -I_d R_D$. $V_{Dmin} \geq V_{GS} - V_T$

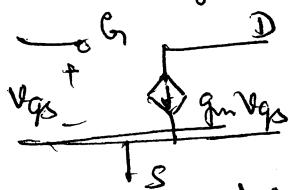
$$\text{but } I_d = g_m V_{GS}$$

$$V_d = -g_m V_{GS} R_D$$

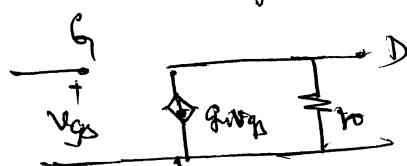
$$A_v = \frac{V_d}{V_{GS}} = -g_m R_D \quad [-ve \text{ sign indicates a phase shift of } 180^\circ]$$

$$\text{Condition is } V_{GS} \ll 2V_{ov} \quad V_{Dmax} = V_{DD} \quad V_{Dmin} = V_{GS} - V_T$$

Small Signal Equivalent Circuit Model : From the signal point of view MOSFET behaves as Voltage-controlled Current Source. It accepts a signal V_{GS} between gate and source and provides a current $g_m V_{GS}$ at the drain terminal. The input resistance of this controlled source is very high ideally infinite. Assuming the Z_{DP}阻抗 also high



Neglecting channel length modulation



Including Channel length modulation effect

$$\text{where } r_o = \frac{V_A}{I_D} \quad k_n = \frac{1}{L} \quad I_D = \frac{1}{2} k_n \frac{W}{L} V_{ov}^2$$

r_o varies between 10kΩ to 100kΩ

The model parameters g_m and r_o depends on the bias point of the MOSFET

$$A_V = \frac{V_d}{V_{gs}} = -g_m (R_D || r_o)$$

$$\text{Let } g_m = k_n \frac{W}{L} (V_{gs} - V_t) = k_n \frac{W}{L} V_{ov}$$

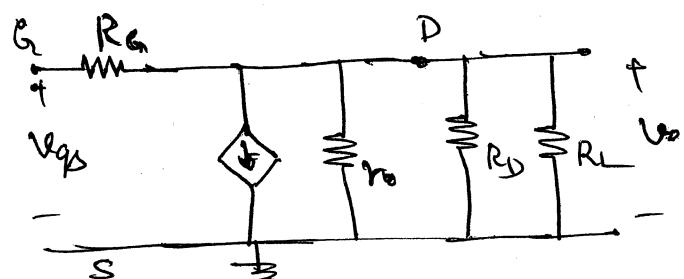
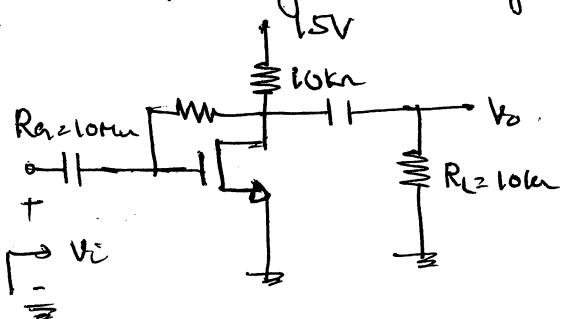
$$I_D = \frac{1}{2} k_n \frac{W}{L} (V_{ov})^2$$

$$V_{ov} = \left[\frac{2I_D}{k_n W L} \right]^{\frac{1}{2}}$$

$$\therefore g_m = \sqrt{2k_n} \cdot \sqrt{\frac{W}{L} \cdot \frac{I_D}{2}}$$

$$g_m = \frac{dI_D}{V_{gs} - V_t} = \frac{2I_D}{V_{ov}}$$

Determine the small signal voltage gain, the input resistance and the ~~large~~ largest allowable input signal. The transistor has $V_t = 1.5V$, $k_n(W/L) = 0.25 \text{ mA/V}^2$ at $V_A = 50V$. Assume the coupling capacitor to be sufficiently large so as to act as short circuit at the signal frequency of interest.



$$I_D = \frac{1}{2} k_n \frac{W}{L} (V_{gs} - V_t)^2 \quad V_{gs} = V_D = V_{DD} - I_D R_D$$

$$I_D = \frac{1}{2} (0.25) (V_D - 1.5)^2 \quad V_D = 15 - 10I_D$$

$$I_D = \frac{1}{2} (0.25) (15 - 10I_D - 1.5)^2$$

$$I_D = \frac{1}{2} (0.25) ((13.5 - 10I_D)^2)$$

$$I_D = 1.06 \text{ mA} \quad V_D = 4.4 \text{ V}$$

$$g_m = k_n \frac{W}{L} (V_{gs} - V_t) = 0.25 (4.4 - 1.5)$$

$$g_m = 0.725 \text{ mA/V} \quad = 47 \text{ kΩ}$$

$$r_o = V_A / I_D = 50 / 1.06 \times 10^{-3}$$

$$V_D = -g_m V_{GS} (R_D || R_L || r_o)$$

1-33

$$A_{v2} = -0.725 (10 || 10 || 47) = -3.3$$

$$I_i = \frac{V_C - V_D}{R_{G1}} = \frac{V_C - V_{GS} + V_t}{R_{G1}}$$

$$I_D = V_C \left(\frac{1 - A_V}{R_G} \right)$$

$$R_m = \frac{V_C}{I_i} = \frac{R_G}{1 - (-3.3)} = \frac{10}{4.3} = 2.33 \text{ M}\Omega$$

To keep MOSFET in Saturation

$$V_{DS} > V_{DS} - V_E$$

$$V_{DS\min} = V_{DS\max} - V_E$$

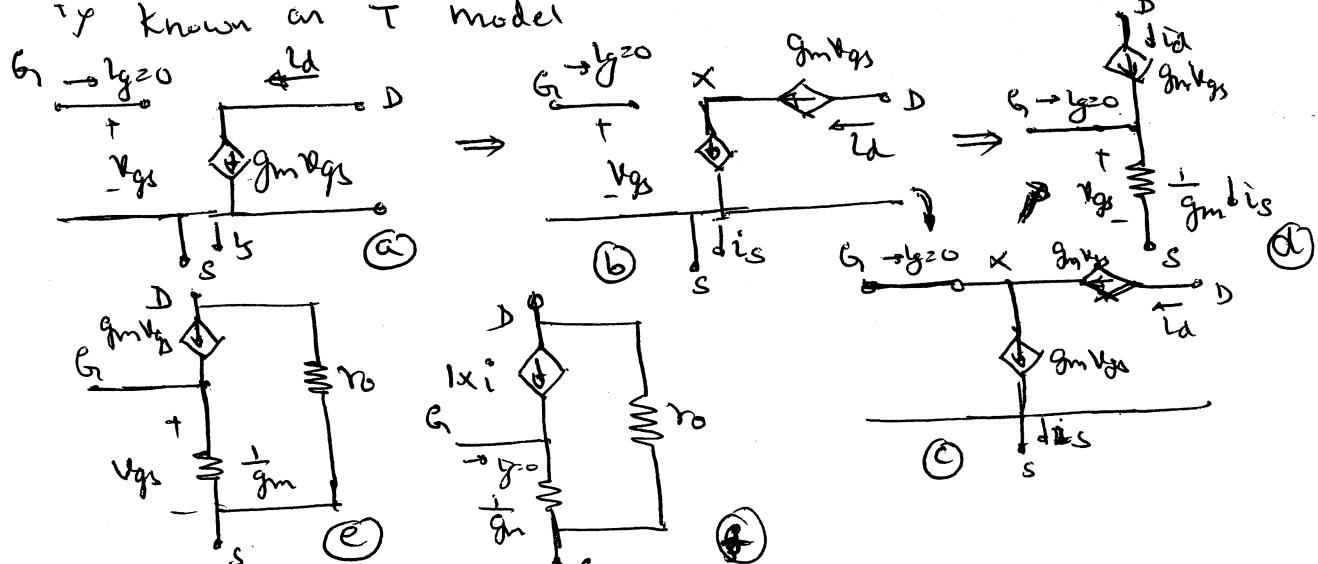
$$V_{DS} - I_A V_t / V_i = V_{GS} + V_D - V_E$$

$$4.4 - 3.3 V_i / V_i = 4.4 + V_D - 1.5$$

$$V_D = 0.34 \text{ V}$$

$V_{DS\min} = 4.4 - 0.34 \text{ V} = 4.06 \Rightarrow V_E$, therefore drain in conduction. The maximum allowable value of zpf Pds = 0.34W

The T Equivalent-Circuit Model : Through a simple circuit transformation it is possible to develop an alternate equivalent circuit model for the MOSFET. The development of such model is known as T model



The equivalent circuit model (a) shows without the effect of r_o .

In fig b a second $g_m V_{GS}$ current source is added in series with the original controlled source. It doesn't change terminal current

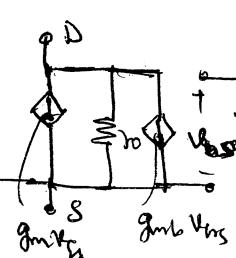
The Newly Created Circuit node, labeled X, is joined to the gate terminal G in fig (C). Observe that gate current doesn't change as it remains equal to I_{D0} and thus this connection doesn't alter the terminal characteristics. We have controlled Current Source gm_{VGS} connected across the Controlled Voltage V_{GS} . We can replace this Controlled Current Source by a resistance as long the resistance draws an equivalent current as source. As the resistance is $V_{GS}/gm_{VGS} = \frac{1}{gm}$. Then we observe that I_D is still I_{D0} , $I_D = gm_{VGS}$ and $I_S = V_{GS}/\frac{1}{gm} = gm_{VGS}$.

In above case we did not included r_o . Including the resistance (channel length modulation effect) r_o between drain and source is as shown in the fig (E). An alternative representation of the Voltage Controlled Source is replaced by Current Controlled Current Source as is shown in fig (F).

Modelling the Body effect: The body effect occurs in a MOSFET when the source is not tied to the substrate (which is always connected to the most-negative power supply in the integrated circuit for N-channel devices and to the most-positive for P-channel devices). Thus the substrate (body) will be at signal ground, but since source is not a signal voltage V_{BS} develops between the body (B) and the source (S). Here substrate acts as a second gate or backgate for the MOSFET.

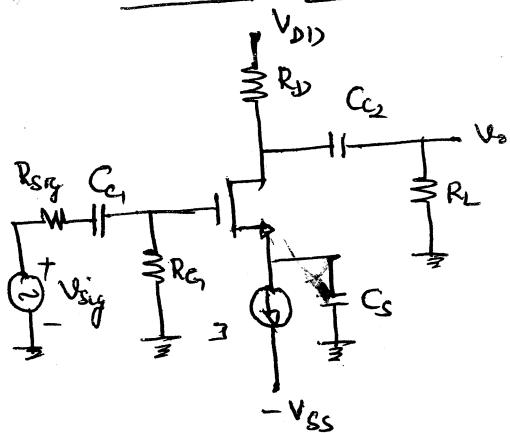
Thus the signal V_{BS} gives rise to a drain current component, we shall write as gm_{VBS} , where gm_b is the body transconductance defined as $gm_b = \frac{\partial I_D}{\partial V_{BS}} \Big|_{V_{DS} \text{ const}}$.

Since I_D depends on V_{BS} through the dependence of V_t on V_{BS} $\therefore gm_b = \lambda g_m$. where $\lambda = \frac{V_t}{V_{SB}} = \frac{2}{2 \sqrt{2} \sigma p + V_{SB}}$

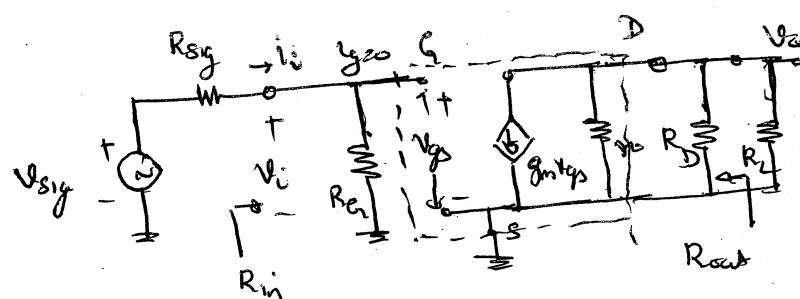


Typically the value of λ lies in the range 0.1 to 0.3. This model can be used whenever the source is not connected to substrate.

Analysis of Common-Source (CS) Amplifier



CS Amplifier Circuit



Small Signal model

The Common Source amplifier (S) or grounded - Source Configuration is most widely used of all MOSFET amplifier configuration. The Source is connected to ac ground by connecting a large value of Capacitor C_s called bypass capacitor. The R_{sig} is the internal resistance of Voltage Source and C_{g1} is the Coupling Capacitor, it blocks dc and acts as short for ac.

The voltage signal resulting at the drain is coupled to the load resistance R_L through Coupling Capacitor C_{g2} and it acts as short for ac and off voltage $V_d = V_d$. where R_d is the actual load or it is $\frac{1}{I_D}$ resistance of other stage.

They amplifiers unilateral, therefore R_{in} doesn't depend on R_L and they $R_{in} = R_i$, Also R_{out} will not depend on R_{sig} and $R_{out} = R_o$.

$$I_g = 0$$

$$R_{in} = R_{G_1}$$

$$V_i = V_{sig} \frac{R_i}{R_i + R_{sig}} = V_{sig} \frac{R_i}{R_i + R_{sig}}$$

$$\text{Since } R_i \gg R_{sig} \quad V_i = V_{sig} = V_{gs}$$

$$V_d = -g_m V_{gs} (r_o || R_d || R_L)$$

$$A_v = \frac{V_o}{V_{gs}} = -g_m (r_o || R_d || R_L)$$

$$\text{Open circuit Voltage gain } A_{vo} = -g_m r_o (R_d || R_L) \quad (R_L \gg R_o)$$

The overall Voltage gain from the Signal Source to the Load

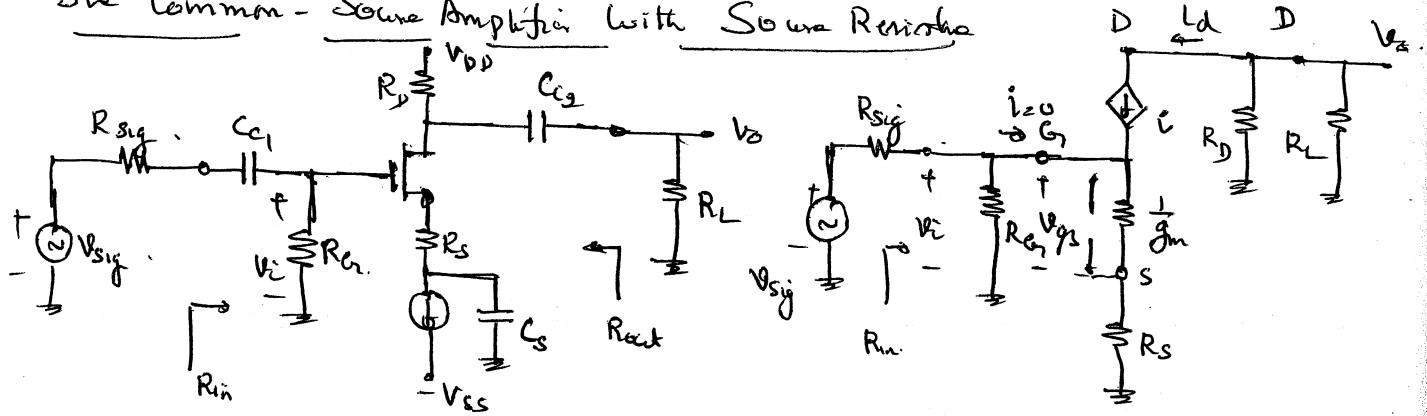
$$G_{av} = \frac{R_{in}}{R_{in} + R_{sig}} \quad A_v = -\frac{R_D}{R_E + R_{sig}} \quad g_m (R_D || R_L)$$

$$R_{out} = R_D \parallel R_D \quad (\text{with } R_L = \infty)$$

$$R_{out}' = R_D \parallel R_D \parallel R_L$$

Thus CS Amplifier has very high I_{Dp} resistance, a moderately high voltage gain and relatively high output resistance.

The Common-Source Amplifier with Source Resistor



Here we have neglected the effect of ' r_o '

$$R_{in} = R_i = R_E$$

$$V_i = V_{sig} \frac{R_E}{R_{sig} + R_E}$$

$$V_{gs} = \frac{V_i / g_m}{R_s + \frac{1}{g_m}} = \frac{V_i}{1 + g_m R_s}$$

Thus R_s is fixed to control the magnitude of V_{gs} so that the device will enter into nonlinear region.

$$I_d = i_s = \frac{V_i}{\frac{1}{g_m} + R_s} = \frac{g_m V_i}{1 + g_m R_s}$$

$$V_o = -i (R_D \parallel R_L) = -\frac{g_m (R_D \parallel R_L)}{1 + g_m R_s} V_i$$

$$A_v = \frac{V_o}{V_i} = \frac{-g_m (R_D \parallel R_L)}{1 + g_m R_s} = \frac{-g_m R_D}{1 + g_m R_s} \quad (\text{if } R_L = \infty)$$

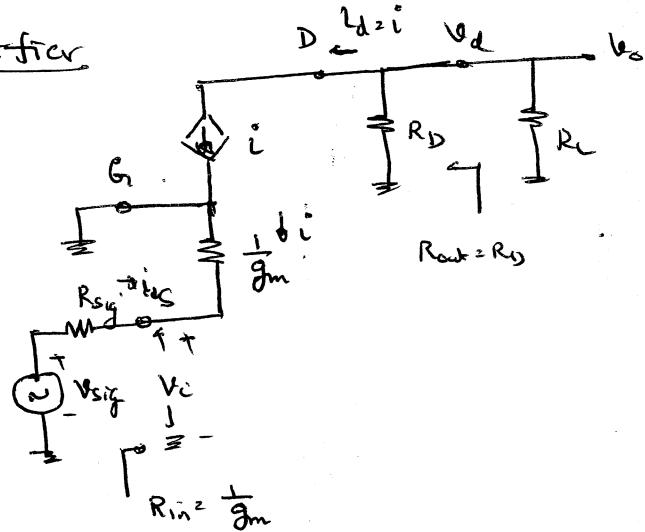
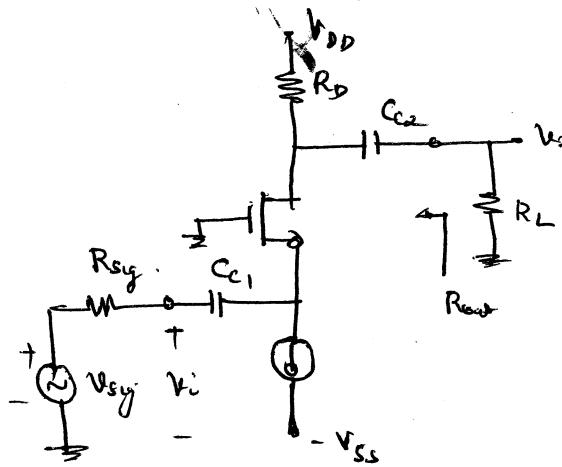
$$A_{vo} = \frac{-g_m R_D}{1 + g_m R_s}$$

$$G_{av} = -\frac{R_D}{R_{in} + R_{sig}} \left(\frac{g_m (R_D \parallel R_L)}{1 + g_m R_s} \right)$$

Gain Curve also interpreted as $\frac{R_D \parallel R_L}{\frac{1}{g_m} + R_S} = \frac{\text{Total Resistance down}}{\text{Total Resistance across}}$ 1.37

We observe that R_S called source degeneration resistance reduces the gain by a factor $1 + g_m R_S$

The Common-Base Amplifier



$$R_{in} = \frac{1}{g_m}$$

Since g_m is the order of 1 mA/V
the z_{lp} resistance is relatively low ($\leq 1 \text{ k}\Omega$)

$$V_i = V_{sig} \frac{R_{in}}{R_{in} + R_{sig}} = V_{sig} \left(\frac{1/g_m}{1/g_m + R_{sig}} \right) = \frac{V_{sig}}{1 + g_m R_{sig}}$$

This makes loss of z_{lp} signal while coupling to z_{lp} of CG Amplifier

$$\text{If } R_{sig} \ll \frac{1}{g_m}$$

$$V_i = V_{sig}$$

$$i_i = \frac{V_{sig}}{\frac{1}{g_m} + R_{sig}} = V_i g_m$$

$$I_d = -i_i = -g_m V_i$$

$$V_{oc} - I_d (R_D \parallel R_L) = g_m V_i (R_D \parallel R_L)$$

$$A_v = \frac{V_o}{V_i} = g_m (R_D \parallel R_L)$$

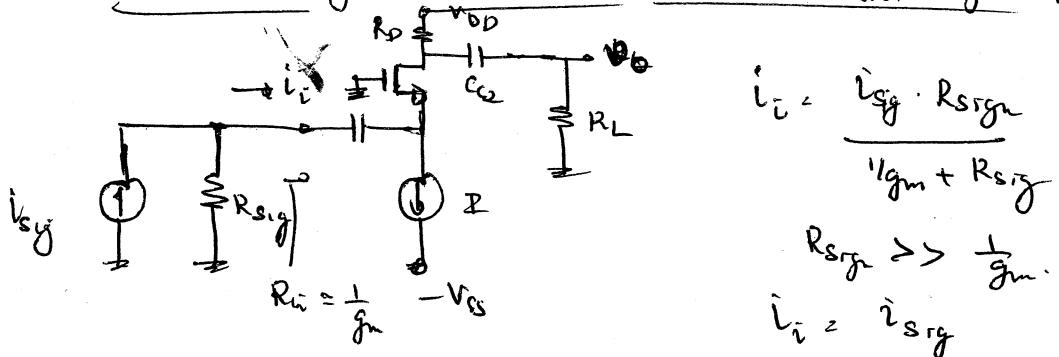
$$A_{vo} = g_m R_D \quad (R_L = \infty)$$

$$G_{in} = \frac{R_{in}}{R_{in} + R_{sig}} \quad A_v = \frac{1/g_m}{1/g_m + R_{sig}} \quad A_V = \frac{A_v}{1 + g_m R_{sig}} = \frac{g_m (R_D \parallel R_L)}{1 + g_m R_{sig}}$$

$$R_o = R_{out} = R_D$$

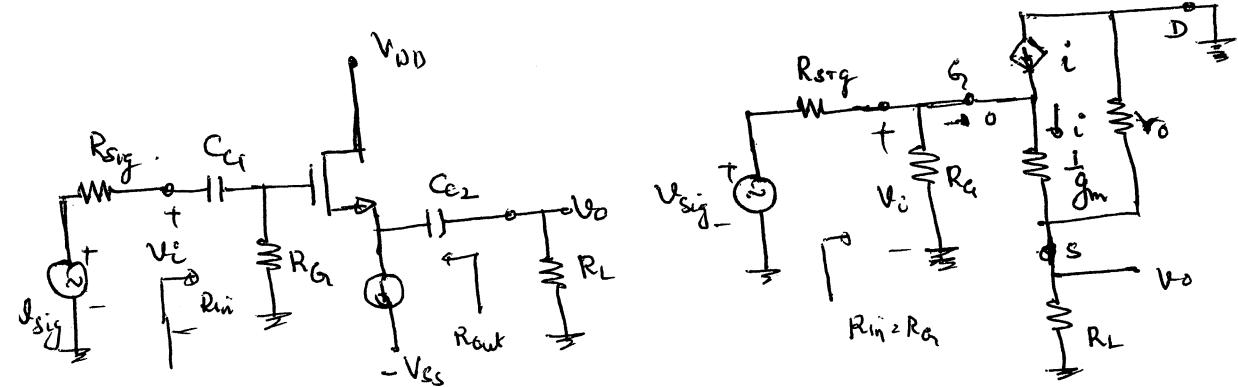
- (i) The C_{ds} Amplifier is Non-inverting
- (ii) Input Resistance C_{ds} Amplifier is low
- (iii) The Voltage gain of CS and C_{ds} Amplifiers same but the overall voltage gain here in C_{ds} Amplifier reduced by a factor $1 + g_m R_{sig}$.

The Common-gate Amplifier fed with a Current Signal i_{sig}



The circuit reproduces the current in the drain terminal at much higher OIP resistance. The circuit thus acts as Unity-gain Current Amplifier or a Current follower. Therefore it can be used in Cascode Circuits. This finds application in some very high frequency circuits.

The Common-Drain or Source-Follower Amplifier



In common drain amplifier, the drain will be common to both OIP and OPO .

$$R_{in} = R_B$$

$$V_i = V_{sig} \frac{R_B}{R_B + R_{sig}} = V_{sig} \frac{R_B}{R_B + R_{sig}} \approx V_{sig} \quad \because R_B \gg R_{sig}$$

The effect of r_o is parallel with R_L

$$\therefore V_o = \frac{V_i (R_L || r_o)}{(R_L || r_o) + \frac{1}{g_m}}$$

$$A_v = \frac{V_o}{V_i} = \frac{(R_L || r_o)}{(R_L || r_o) + \frac{1}{g_m}}$$

A_{V0} = open Circuit voltage gain

$$A_{V0} = \frac{r_o}{r_o + \frac{1}{g_m}} \quad R_L = \infty$$

If $r_o \gg \frac{1}{g_m}$

$$A_{V0} \approx 1$$

↳ The Voltage at the Source follows the I_{dp}, therefore it is
Called Source follower.

If $r_o \gg R_L$

$$A_V = \frac{R_L}{R_L + \frac{1}{g_m}}$$

$$\text{The overall voltage gain } G_V = \frac{R_L}{R_L + R_S g_m} \frac{(R_L) r_o}{(R_L) r_o + \frac{1}{g_m}}$$

$$R_{out} = r_o \parallel \frac{1}{g_m} \quad \text{Since } r_o \gg \frac{1}{g_m}$$

$$R_{out} \approx \frac{1}{g_m} \quad \text{which indicates } R_o \text{ is moderately low.}$$

In conclusion, the Source follower will have very high input resistance, a relatively low output resistance, and a voltage gain less than but close to unity. It can be used as unity gain voltage buffer amplifier.

