**IS332**

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M S RAMAIAH INSTITUTE OF TECHNOLOGY

(AUTONOMOUS INSTITUTE, AFFILIATED TO VTU)

BANGALORE – 560 054

SEMESTER END EXAMINATIONS -JANUARY 2016

Course & Branch : B.E.- Information Science & Engg. Semester : III
Subject : Computer Organization and Architecture Max. Marks : 100
Subject Code : IS332 Duration : 3 Hrs

Instructions to the Candidates:

- Answer one full question from each unit.

UNIT – I

1. a) Design a BCD to Excess – 3 code converter and write the circuit diagram. CO1 (10)
b) Design a four bit adder with carry lookahead generator. CO1 (10)
2. a) Derive the condition for correction? logic and design a BCD adder rephrase. CO1 (10)
b) What are the limitations of a plain encoder? Design a four input priority encoder using gates. CO1 (10)

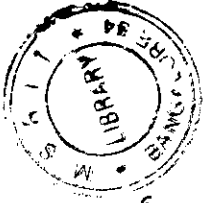
UNIT – II

3. a) Explain the working of SR latch with controlled input and D latch. CO2 (10)
b) Explain the working of:
i. Master Slave D flip-flop
ii. D-type positive edge triggered flip-flop. CO2 (10)
4. a) With a neat circuit diagram, explain the working of a 4-bit register with a parallel load. CO2 (10)
b) Design an n-bit serial adder using shift registers. CO2 (10)

UNIT – III

5. a) What are the limitations of measures like MIPS and MFLOPS? What are the desirable characteristics of a benchmark suite? Find the MIPS rate for the following program trace: *Processor speed is 400 MHz* CO3 (10)

Instruction Type	CPI	Instruction Mix
Arithmetic and Logic	1	60%
Load/store (Cache hit)	2	18%
Branch	4	12%
Memory reference(cache miss)	8	10%



- b) With neat diagrams, explain: CO3 (10)
- Top – level view of computer components.
 - Instruction Cycle states.
6. a) Explain system bus using both traditional and high-performance architectures. CO3 (10)
- b) List and explain any five key characteristics of memory systems. Draw a flow chart demonstrating cache read operation. CO3 (10)

UNIT – IV

7. a) With an examples, for each explain any five types of addressing modes. CO4 (10)
- b) Discuss the register organization of MC68000, 8086 and 80386 processors. CO4 (10)
8. a) What is pipelining? Explain the operation of a six stage instruction pipeline. CO4 (10)
- b) Explain three types of pipeline hazards. CO4 (10)

UNIT – V

9. a) With a neat diagram explain the Flynn's taxonomy of parallel processor architectures. CO5 (10)
- b) Discuss the working of MESI protocol with state transition diagrams. CO5 (10)
10. a) Explain the four principle approaches to explicit multithreading. CO5 (10)
- b) What is a cluster? Explain the typical cluster configurations with benefits. CO5 (10)
