Revision	Release Date	Remark
V0.1		Initial Version

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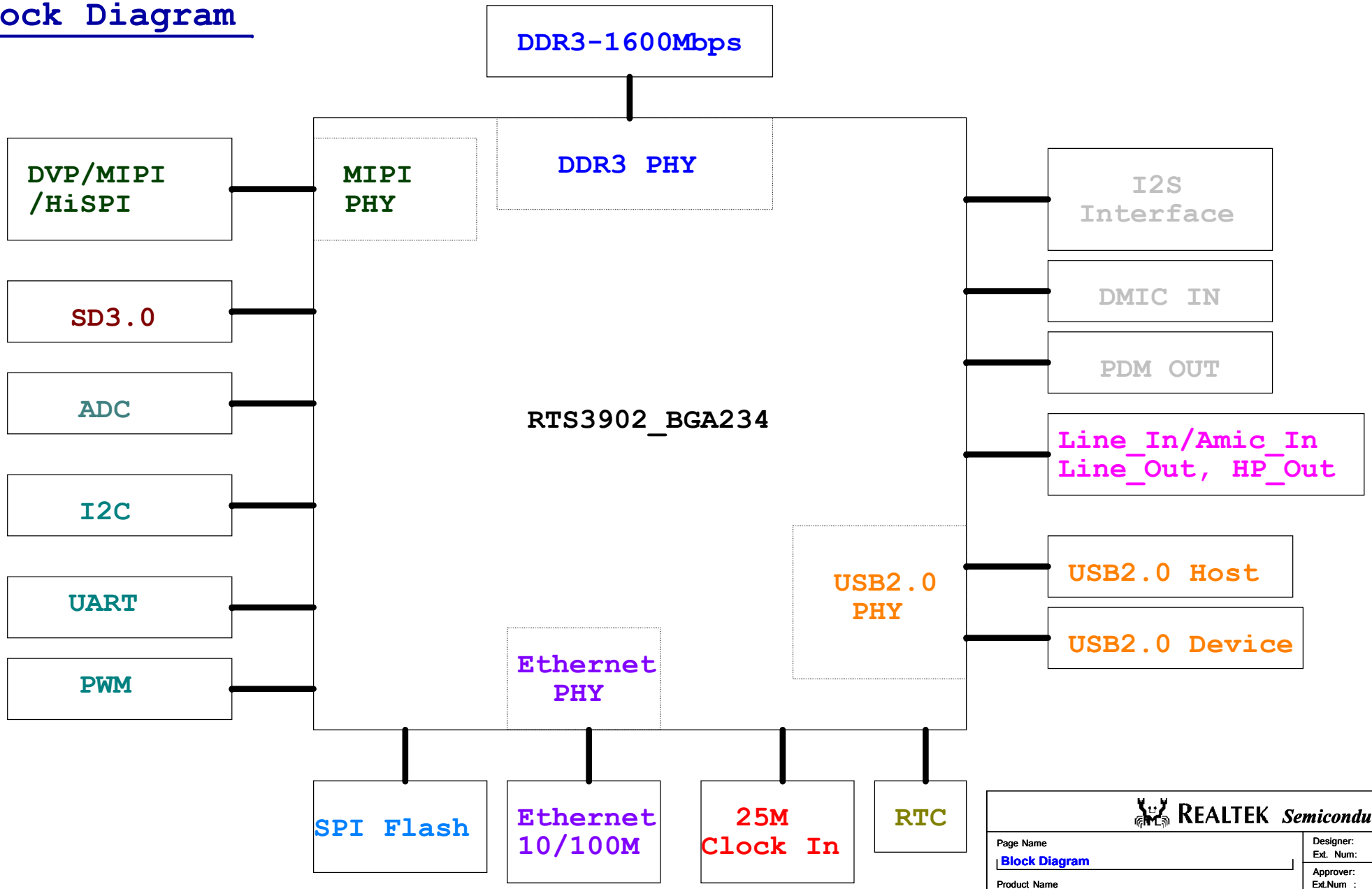
Block Diagram



REALTEK *Semiconductor Corp.*

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REALTEK *Semiconductor Corp.*

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	Approver: Ext.Num :
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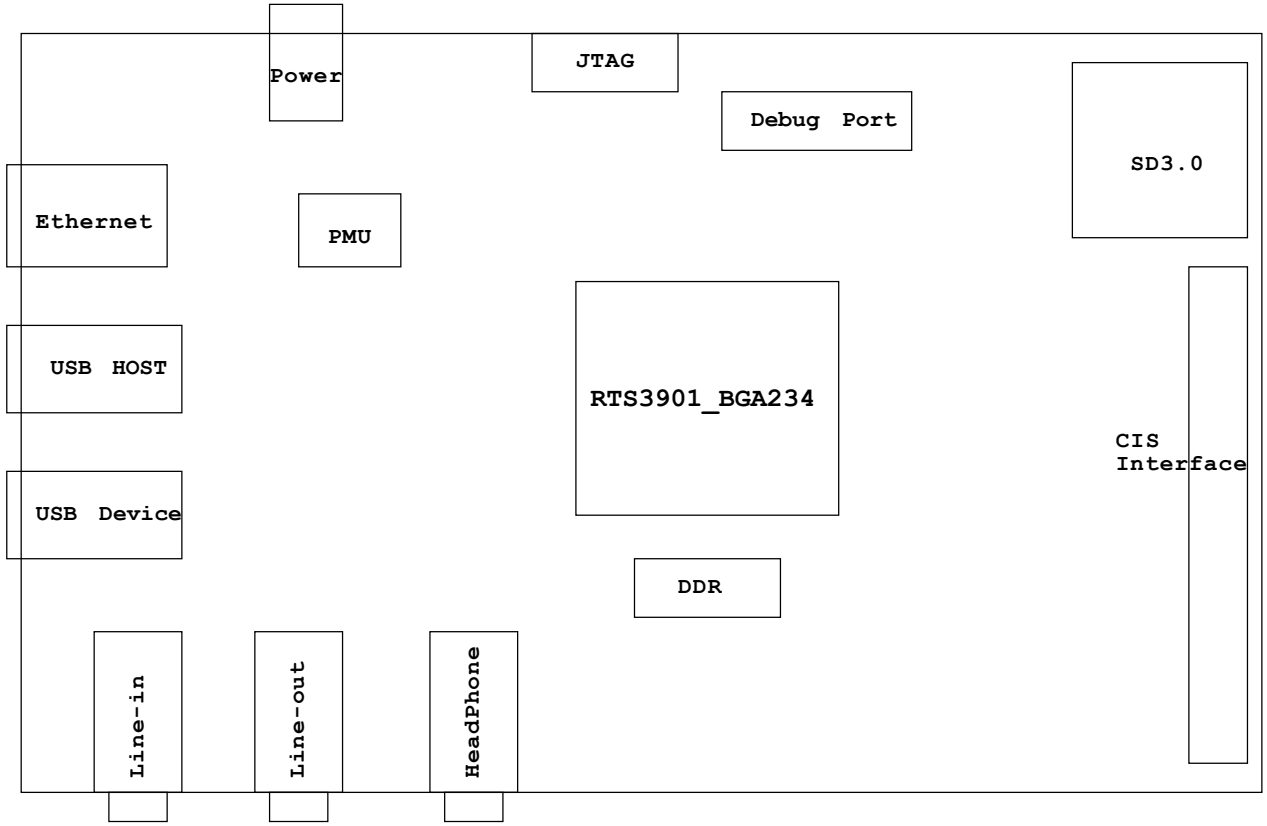
PCB Name RTS3901_BGA234_L4_Demo Board_V0.2	Rev 0.1 | Size C | Page 3 of 15

PCB Placement



REALTEK Semiconductor Corp.

Page Name: PCB Placement	Designer: Ext. Num:
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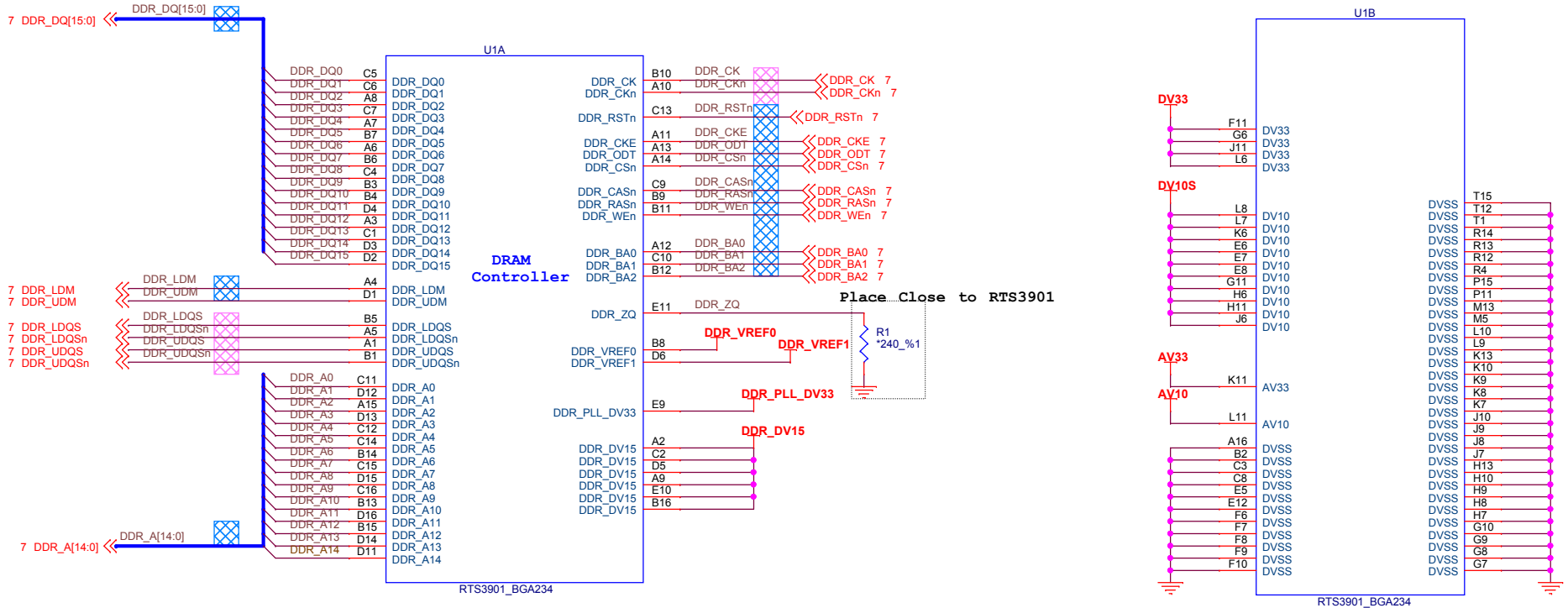
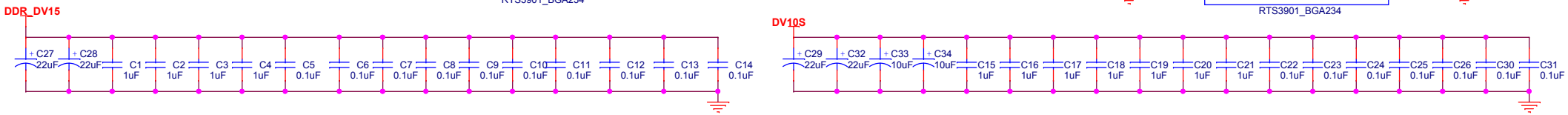
RTS3901_1

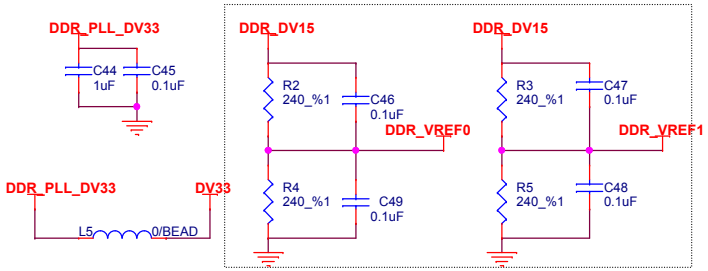
Single End
Z0=50ohm

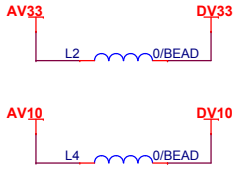
Differential Pairs
Z0=100ohm

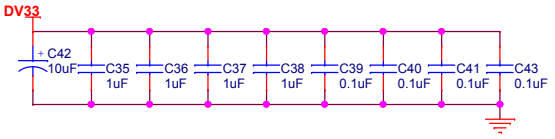


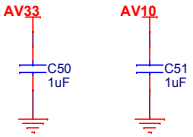


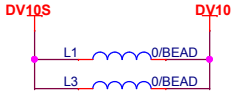
Place Close to RTS3901











REALTEK Semiconductor Corp.

Page Name: RTS3901_1	Designer: Ext. Num:
Product Name: RTS3901_BGA234_L4_Demo Board_V0.2	Approver: Ext.Num :
PCB Name: RTS3901_BGA234_L4_Demo Board_V0.2	Modify Date: Friday, February 26, 2016
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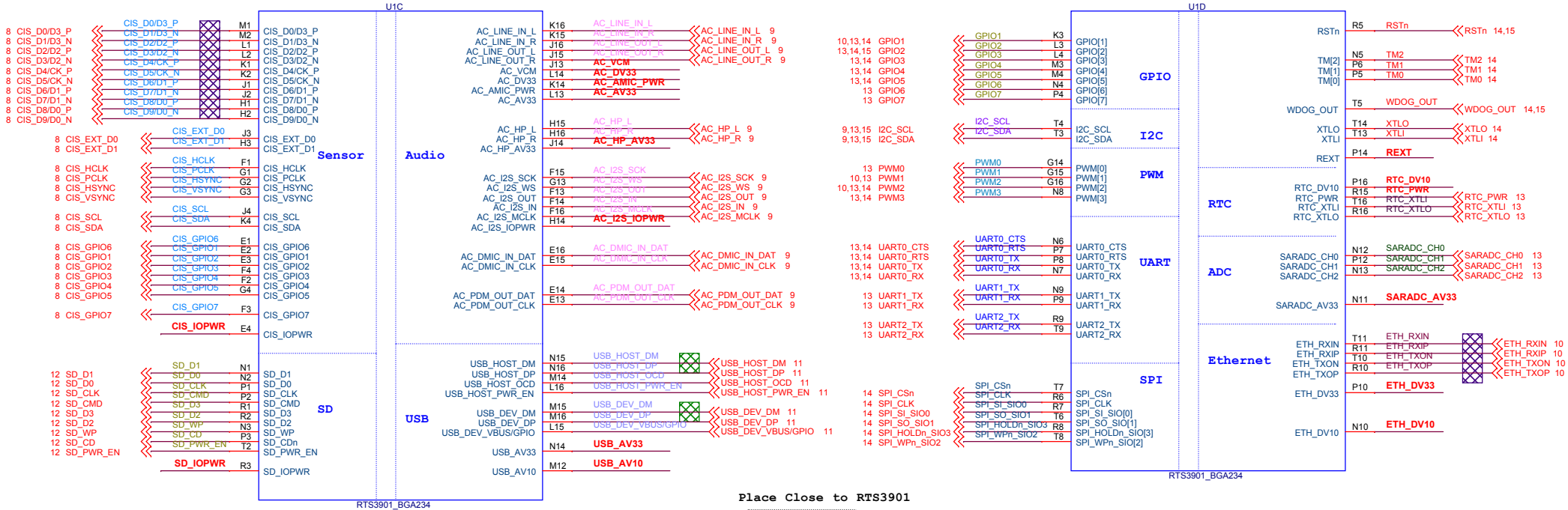
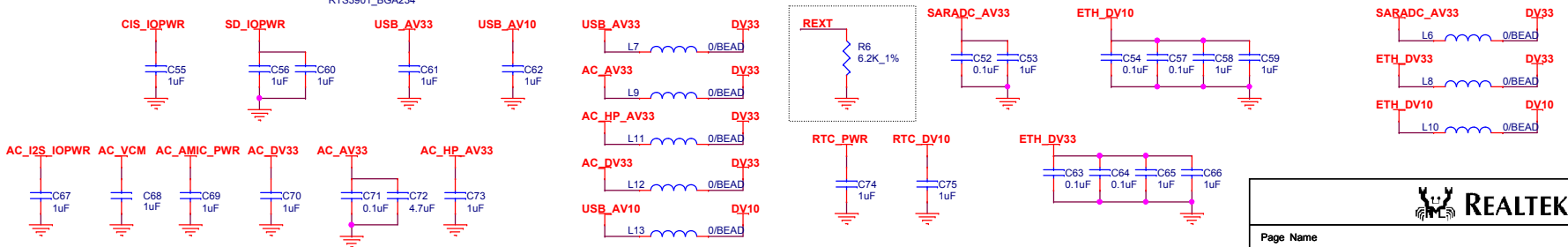
RTS3901_2

Differential Pairs
Z0=100ohm

Differential Pairs
Z0=90ohm



Place Close to RTS3901



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Product Name: RTS3901_BGA234_L4_Demo Board_V0.2	Approver: Ext.Num :
PCB Name: RTS3901_BGA234_L4_Demo Board_V0.2	Modify Date: Friday, February 26, 2016
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DDR3

Single End
Z0=50ohm

Differential Pairs
Z0=100ohm

5 DDR_DQ[15:0] — DDR_DQ[15:0]
DDR_DQ0 DDR_DQ1 DDR_DQ2 DDR_DQ3 DDR_DQ4 DDR_DQ5 DDR_DQ6 DDR_DQ7
DDR_DQ8 DDR_DQ9 DDR_DQ10 DDR_DQ11 DDR_DQ12 DDR_DQ13 DDR_DQ14 DDR_DQ15

5 DDR_A[14:0] — DDR_A[14:0]
DDR_A0 DDR_A1 DDR_A2 DDR_A3 DDR_A4 DDR_A5 DDR_A6 DDR_A7 DDR_A8 DDR_A9 DDR_A10 DDR_A11 DDR_A12 DDR_A13 DDR_A14

DDR_CSn DDR_A6 DDR_A2 DDR_A12 → DDRs_CSn DDRs_A6 DDRs_A2 DDRs_A12
DDR_BA0 DDR_BA2 DDR_ODT DDR_A10 → DDRs_BA0 DDRs_BA2 DDRs_ODT DDRs_A10
DDR_CK DDR_CKn → DDRs_CK DDRs_CKn
DDR_CKE → DDRs_CKE
DDR_A11 DDR_A5 DDR_A8 DDR_RSTn → DDRs_A11 DDRs_A5 DDRs_A8 DDRs_RSTn
DDR_A0 DDR_A3 DDR_A1 DDR_BA1 → DDRs_A0 DDRs_A3 DDRs_A1 DDRs_BA1
DDR_A9 DDR_A13 DDR_A4 DDR_A7 DDR_A14 → DDRs_A9 DDRs_A13 DDRs_A4 DDRs_A7 DDRs_A14

DDR_DQ13 DDR_DQ12 DDR_DQ10 DDR_DQ8 → DDRs_DQ13 DDRs_DQ12 DDRs_DQ10 DDRs_DQ8
DDR_DQ11 DDR_DQ9 DDR_DQ14 DDR_DQ15 → DDRs_DQ11 DDRs_DQ9 DDRs_DQ14 DDRs_DQ15
DDR_DQ6 DDR_DQ5 DDR_DQ4 DDR_DQ2 → DDRs_DQ6 DDRs_DQ5 DDRs_DQ4 DDRs_DQ2
DDR_DQ3 DDR_DQ1 DDR_DQ0 DDR_DQ7 → DDRs_DQ3 DDRs_DQ1 DDRs_DQ0 DDRs_DQ7
DDR_LDM DDR_UDM → DDRs_LDM DDRs_UDM

5 DDR_LDQS 5 DDR_LDQSn 5 DDR_UDQS 5 DDR_UDQSn → DDR_LDQS DDR_LDQSn DDR_UDQS DDR_UDQSn → DDRs_LDQS DDRs_LDQSn DDRs_UDQS DDRs_UDQSn
5 DDR_WEn 5 DDR_RASn 5 DDR_CASn → DDR_WEn DDR_RASn DDR_CASn → DDRs_WEn DDRs_RASn DDRs_CASn
5 DDR_CKn 5 DDR_CK → DDR_CKn DDR_CK
5 DDR_LDM 5 DDR_UDM → DDR_LDM DDR_UDM
5 DDR_RSTn 5 DDR_CSn 5 DDR_ODT 5 DDR_CKE → DDR_RSTn DDR_CSn DDR_ODT DDR_CKE
5 DDR_BA2 5 DDR_BA1 5 DDR_BA0 → DDR_BA2 DDR_BA1 DDR_BA0

DDR_DV15
C79 10uF
C76 C77 C78 C80 C81 C82 C83 C84 0.1uF

DDR_DV15
C100 10uF
C90 C91 C92 C93 C94 C95 C96 C97 C98 C99 0.1uF

DDR_DV15
VDDQ: H9 H2 F1 E9 D2 C9 C1 A8 A1
VDD: R9 R1 N9 N1 K8 K2 G7 D9 B2

U2
DDR3_FBGA96

DDRs_DQ0 DDRs_DQ1 DDRs_DQ2 DDRs_DQ3 DDRs_DQ4 DDRs_DQ5 DDRs_DQ6 DDRs_DQ7 DDRs_DQ8 DDRs_DQ9 DDRs_DQ10 DDRs_DQ11 DDRs_DQ12 DDRs_DQ13 DDRs_DQ14 DDRs_DQ15
E3 F7 F2 F8 H3 H8 G2 H7 D7 C3 C8 C2 A7 A2 B8 A3
DQ0 DQ1 DQ2 DQ3 DQ4 DQ5 DQ6 DQ7 DQ8 DQ9 DQ10 DQ11 DQ12 DQ13 DQ14 DQ15

DDRs_UDQS DDRs_UDQSn DDRs_LDQS DDRs_LDQSn
C7 B7 F3 G3
UDQS UDQS# LDQS LDQS#

DDRs_LDM DDRs_UDM
E7 D3
LDM UDM

DDRs_ODT
K1
ODT

L9 L1
NC NC

DDRs_VREFDQ
H1
VREFDQ

DDRs_ZQ
L8
ZQ

R7 240_%1

Place Close to DDR

A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10/AP A11 A12/BC A13 A14_NC A15_NC
N3 P7 P3 N2 P8 P2 R8 R2 T8 R3 L7 R7 N7 T3 T7 M7 M2
DDRs_A0 DDRs_A1 DDRs_A2 DDRs_A3 DDRs_A4 DDRs_A5 DDRs_A6 DDRs_A7 DDRs_A8 DDRs_A9 DDRs_A10 DDRs_A11 DDRs_A12 DDRs_A13 DDRs_A14

BA0 BA1 BA2
N8 M3
DDRs_BA0 DDRs_BA1 DDRs_BA2

WE CAS RAS CS
L3 K3 J3 L2
DDRs_WEn DDRs_CASn DDRs_RASn DDRs_CSn

CKE CK CK
K9 J7 K7
DDRs_CKE DDRs_CK DDRs_CKn

RESET
T2
DDRs_RSTn

NC NC
J1 J9

VREFCA
M8
DDRs_VREFCA

VSSQ: G9 G1 F9 E8 E2 D8 D1 B9 B1
VSS: T9 T1 P9 P1 M9 M1 J8 J2 G8 E1 B3 A9

DDRs_CKn DDRs_CK
R10 51
R11 51
C87 0.1uF

Place Close
to DRAM Side and at
the Trace end.

Place Close to DDR

DDR_DV15
R8 240_%1
C85 0.1uF
DDRs_VREFDQ
R12 240_%1
C88 0.1uF

DDR_DV15
R9 240_%1
C86 0.1uF
DDRs_VREFCA
R13 240_%1
C89 0.1uF

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PCB Name: RTS3901_BGA234_L4_Demo Board_V0.2	Modify Date: Friday, February 26, 2016
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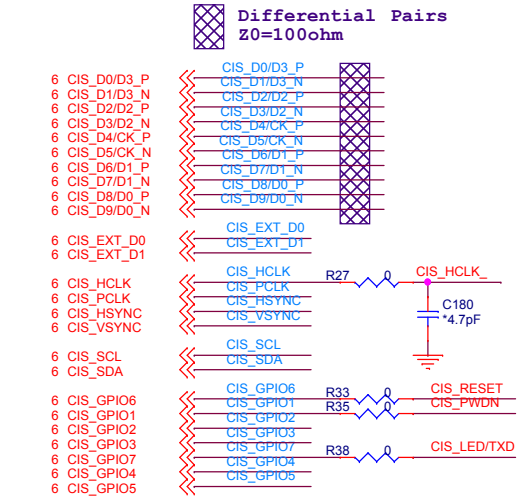
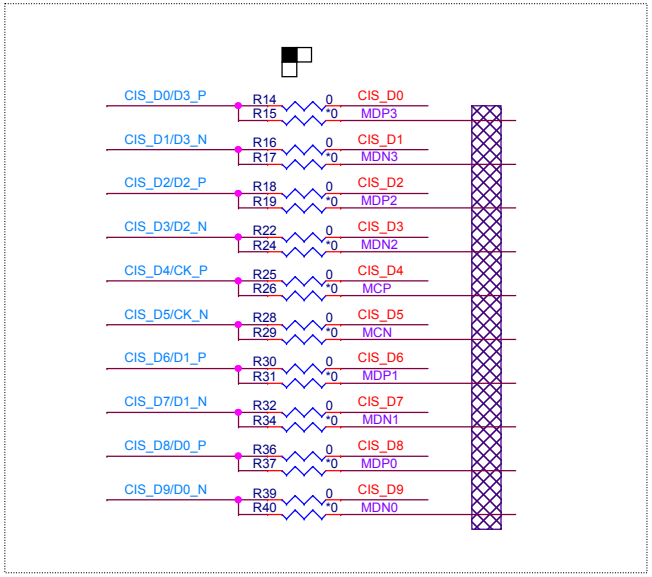
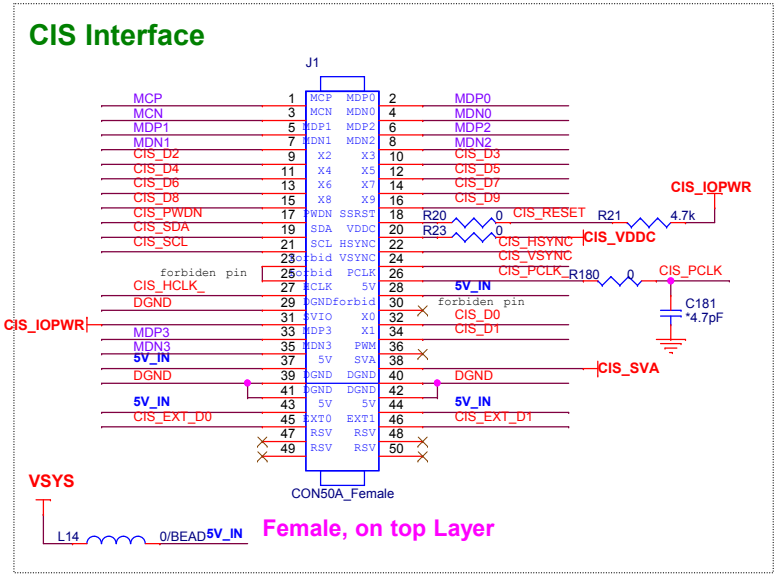
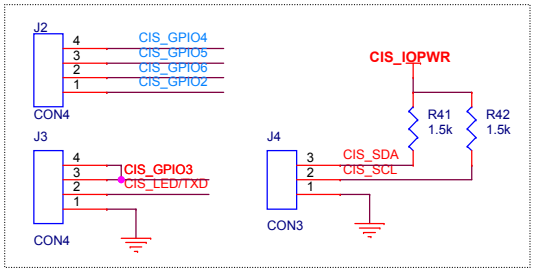
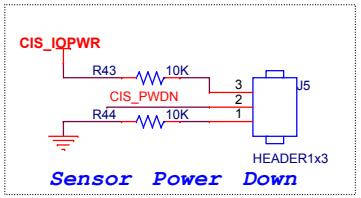
Video

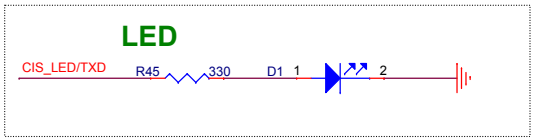












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Page Name: Video	Designer: Ext. Num:
Product Name: RTS3901_BGA234_L4_Demo Board_V0.2	Approver: Ext.Num :
PCB Name: RTS3901_BGA234_L4_Demo Board_V0.2	Modify Date: Friday, February 26, 2016
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Audio

6 AC_LINE_IN_L
6 AC_LINE_IN_R
6 AC_LINE_OUT_L
6 AC_LINE_OUT_R
AC_LINE_IN_L
AC_LINE_IN_R
AC_LINE_OUT_L
AC_LINE_OUT_R

6 AC_HP_L
6 AC_HP_R
AC_HP_L
AC_HP_R

6 AC_I2S_SCK
6 AC_I2S_WS
6 AC_I2S_OUT
6 AC_I2S_IN
6 AC_I2S_MCLK
AC_I2S_SCK
AC_I2S_WS
AC_I2S_OUT
AC_I2S_IN
AC_I2S_MCLK

6 AC_DMIC_IN_DAT
6 AC_DMIC_IN_CLK
AC_DMIC_IN_DAT
AC_DMIC_IN_CLK

6 AC_PDM_OUT_DAT
6 AC_PDM_OUT_CLK
AC_PDM_OUT_DAT
AC_PDM_OUT_CLK

6,13,15 I2C_SCL
6,13,15 I2C_SDA
I2C_SCL
I2C_SDA

AC_AMIC_PWR
C109 0.1uF
C110 1uF

AC_I2S_IOPWR
R56 *1.5k
R54 *1.5k
I2C_SDA
I2C_SCL

I2S Interface

J6
13 11 9 7 5 3 1
14 12 10 8 6 4 2
I2C_SDA
I2C_SCL
*AC_I2S_WS
*AC_I2S_SCK
*AC_I2S_IN
*AC_I2S_OUT
*AC_I2S_MCLK
CON_Female

Place bottom, Female
Mark the Net Name

Notice The Position on PCB

DMIC Interface

AC_DMIC_IN_CLK R50 0 DMIC_CLK
C105 *10pF

AC_DMIC_IN_DAT R51 0 DMIC_DATA
C106 *10pF

J8
DV33
2 4 6 8 10
1 3 5 7 9
DGND
DMIC_CLK
DMIC_DATA
DGND
DGND
DMIC_CLK
DMIC_DATA
DV33
Left Channel
Right Channel
HEADER2X5_Female

Notice The Position on PCB
Place on TOP

Place TOP, Female
Mark the Net Name

PDM Interface

AC_PDM_OUT_CLK R46 0 PDM_CLK_L
C101 *10pF
R47 0
PDM_CLK_R
C102 *10pF

AC_PDM_OUT_DAT R48 0 PDM_DAT_L
C103 *10pF
R49 0
PDM_DAT_R
C104 *10pF

J7
DGND 1
PDM_CLK_L 2
PDM_DAT_L 3
PDM_CLK_R 4
PDM_DAT_R 5
D1V8 6
CON6

for Codec/PDM Amp 1.8V

DV33
C107 1uF
R52 10k
U3
IN OUT
GND ADJ
EN
AP7365(ADJ)
D1V8
R53 1K_1%
R55 806_1%
C108 1uF

Line-In Share With AMIC

J9
LINE-IN_R
AC_LINE_IN_R
AMIC_R
HEADER1X3

R59 200K Line_IN_JD
LINE-IN_R R60 22 C112 1uF
LINE-IN_L R62 22 C114 1uF
PH2
LINE_IN
Connect-in 3 4 Short
Connect-out 3 4 Open

Line_IN_JD TP2
*TESTPOINT

Select Line-in or AMIC
Mark the Net Name

J10
LINE-IN_L
AC_LINE_IN_L
AMIC_L
HEADER1X3

AMIC_PWR R63 0
C116 0.1uF
C117 0.1uF
R66 2.2K
AMIC_R C182 1uF
SE1

AMIC_PWR R64 0
C118 0.1uF
C119 0.1uF
R67 2.2K
AMIC_L C183 1uF
SE2

AC_AMIC_PWR R181 NC/0 AMIC_PWR
AMIC_R R71 *22 AMIC_L

DV33
C184 1uF
R182 10K
U10
Vin Vout
GND
EN NC
C185 1uF
AMIC_PWR
AT5231-2.8-SOT25

Line-out

AC_LINE_OUT_R R58 22 C111 1uF LINE-OUT_R
AC_LINE_OUT_L R61 22 C113 1uF LINE-OUT_L
R57 200K Line_out_JD
PH1
LINE_OUT
Connect-in 3 4 Short
Connect-out 3 4 Open

Line_out_JD TP1
*TESTPOINT

HeadPhone

AC_HP_R R65 0 C115 1uF HPO_R
AC_HP_L R68 0 C120 1uF HPO_L
RJ1 200K HP_JD
PH3
HPOUT
Connect-in 3 4 Short
Connect-out 3 4 Open

C121 *0.1uF
C122 *0.1uF
R69 *22
R70 *22
TP3
HP_JD
*TESTPOINT

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Product Name: RTS3901_BGA234_L4_Demo Board_V0.2	Approver: Ext.Num :
PCB Name: RTS3901_BGA234_L4_Demo Board_V0.2	Modify Date: Monday, April 25, 2016
Rev 0.1	Size Custom
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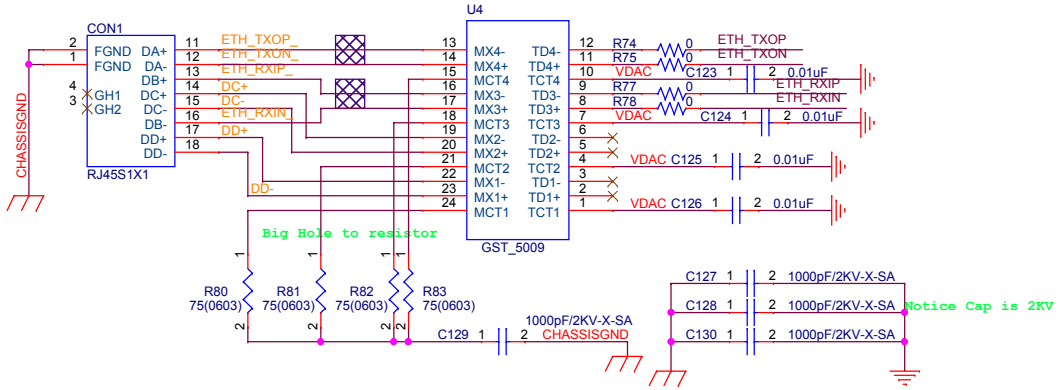
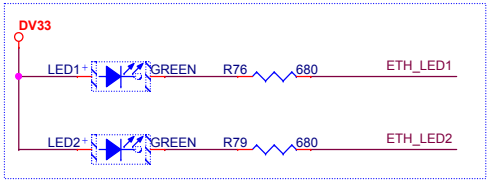
Ethernet

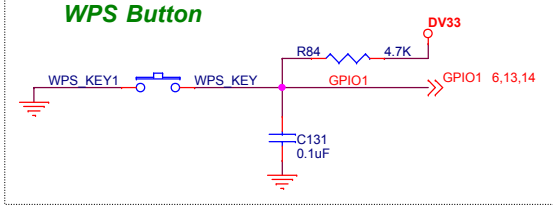
Differential Pairs
Z0=100ohm

Ethernet





WPS Button



REALTEK Semiconductor Corp.

Page Name: Ethernet	Designer: Ext. Num:
Product Name: RTS3901_BGA234_L4_Demo Board_V0.2	Approver: Ext.Num :
PCB Name: RTS3901_BGA234_L4_Demo Board_V0.2	Modify Date: Friday, February 26, 2016
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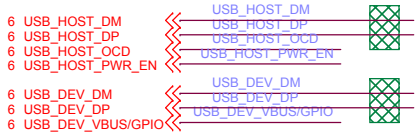
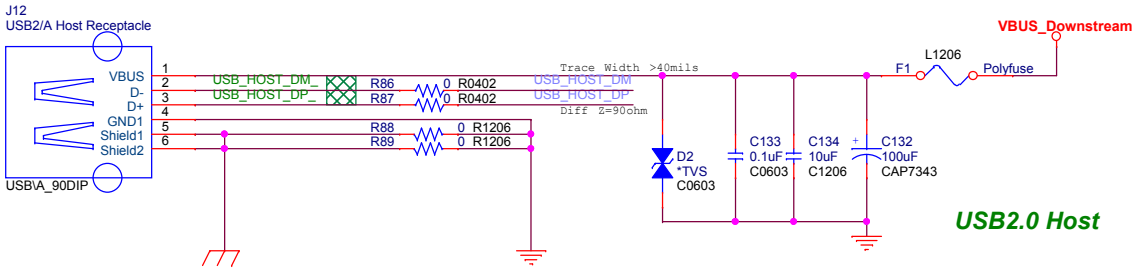
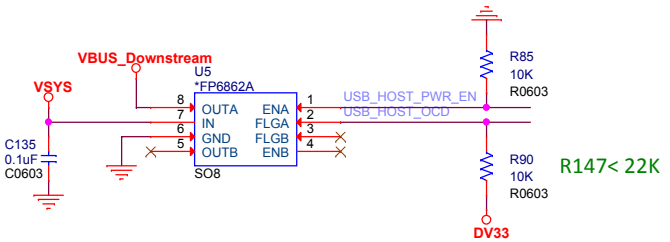
USB Host/Device



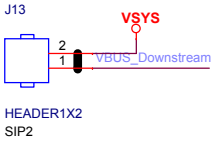
Differential Pairs
Z0=90ohm

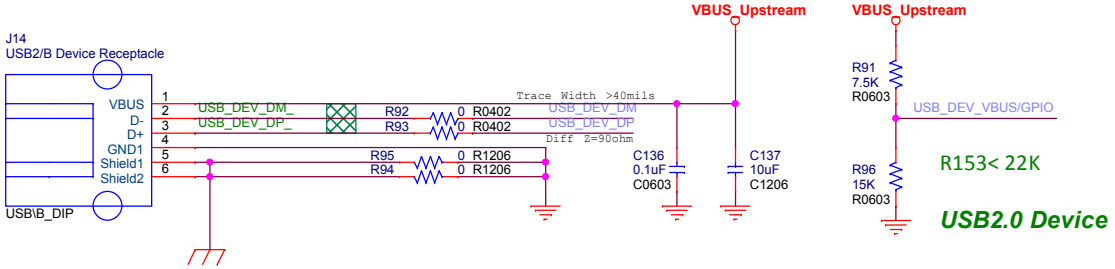


USB2.0 Host



R147< 22K





R153< 22K

USB2.0 Device

REALTEK Semiconductor Corp.	
Page Name: USB Host/Device	Designer: Ext. Num:
Product Name: RTS3901_BGA234_L4_Demo Board_V0.2	Approver: Ext.Num :
PCB Name: RTS3901_BGA234_L4_Demo Board_V0.2	Modify Date: Friday, February 26, 2016
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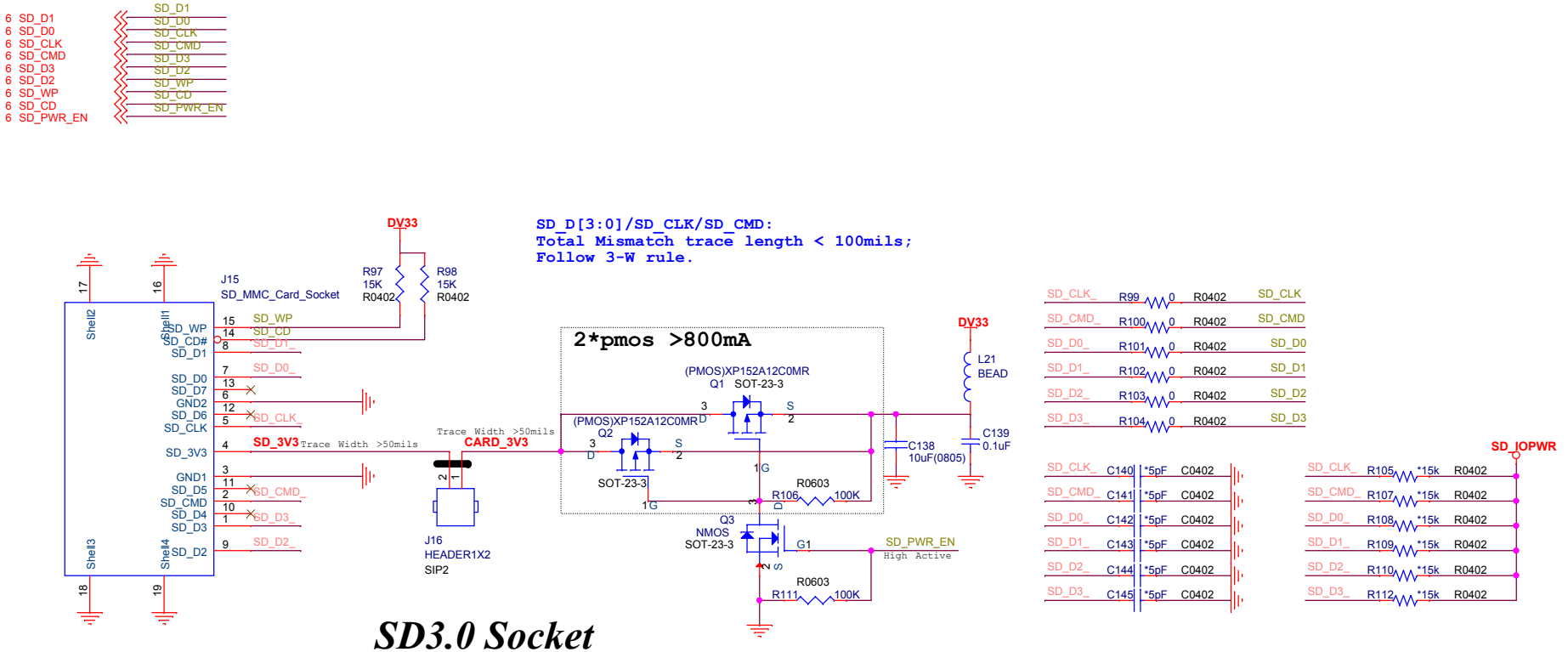
SD



REALTEK Semiconductor Corp.

Page Name: SD	Designer: Ext. Num:
Product Name: RTS3901_BGA234_L4_Demo Board_V0.2	Approver: Ext.Num :
PCB Name: RTS3901_BGA234_L4_Demo Board_V0.2	Modify Date: Thursday, April 28, 2016
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UART_I2C_PWM_ADC_GPIO

6,9,15 I2C_SCL → I2C_SCL
6,9,15 I2C_SDA → I2C_SDA

6 PWM0 → PWM0
6,10 PWM1 → PWM1
6,10,14 PWM2 → PWM2
6,14 PWM3 → PWM3

6,14 UART0_CTS → UART0_CTS
6,14 UART0_RTS → UART0_RTS
6,14 UART0_TX → UART0_TX
6,14 UART0_RX → UART0_RX

6 UART1_TX → UART1_TX
6 UART1_RX → UART1_RX

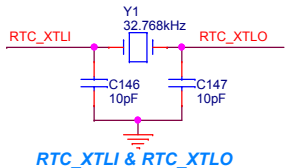
6 UART2_TX → UART2_TX
6 UART2_RX → UART2_RX

6 RTC_PWR → RTC_PWR
6 RTC_XTLI → RTC_XTLI
6 RTC_XTLO → RTC_XTLO

6 SARADC_CH0 → SARADC_CH0
6 SARADC_CH1 → SARADC_CH1
6 SARADC_CH2 → SARADC_CH2

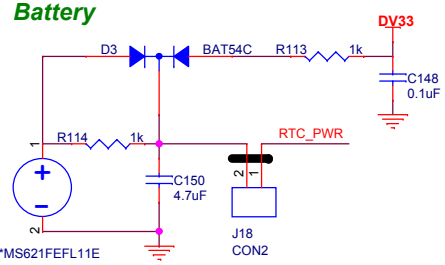
6,10,14 GPIO1 → GPIO1
6,14,15 GPIO2 → GPIO2
6,14 GPIO3 → GPIO3
6,14 GPIO4 → GPIO4
6,14 GPIO5 → GPIO5
6 GPIO6 → GPIO6
6 GPIO7 → GPIO7

RTC

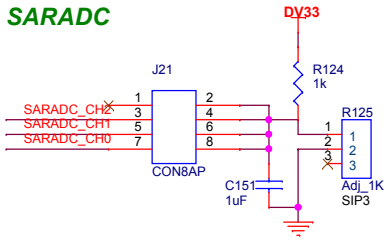


RTC_XTLI & RTC_XTLO

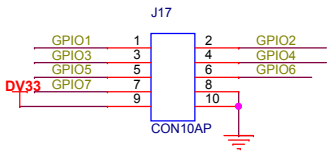
Battery



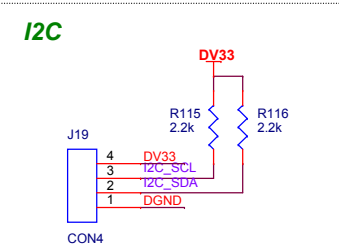
SARADC



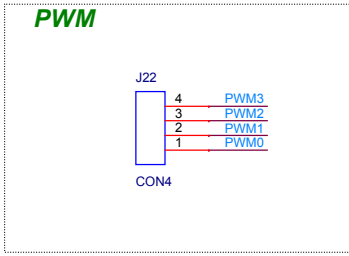
GPIO



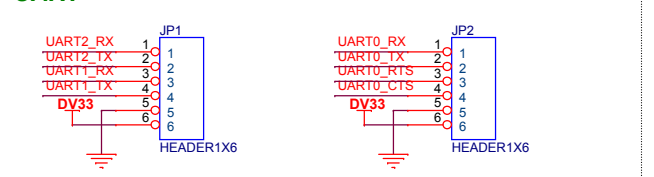
I2C



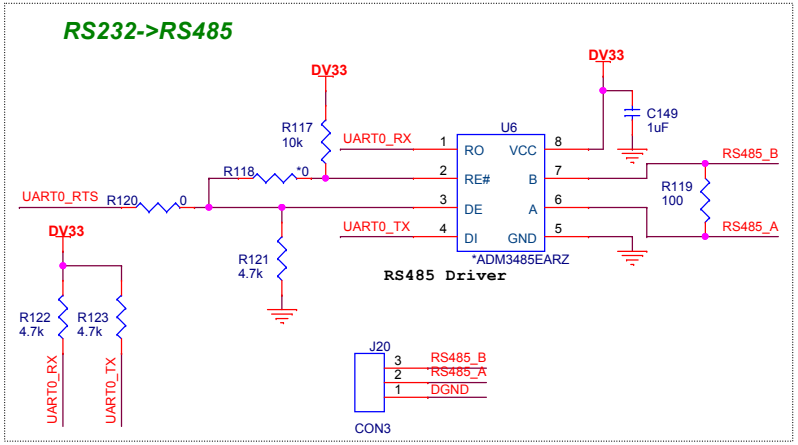
PWM



UART



RS232->RS485



Y2 *HOLE
Y3 *HOLE
Y4 *HOLE
Y5 *HOLE

REALTEK Semiconductor Corp.

Page Name: UART_I2C_PWM_ADC_GPIO	Designer: Ext. Num:
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JTAG_SPI_Clock_RSTn

6,15 RSTn — RSTn

6 TM2 — TM2
6 TM1 — TM1
6 TM0 — TM0

6,15 WDOG_OUT — WDOG_OUT

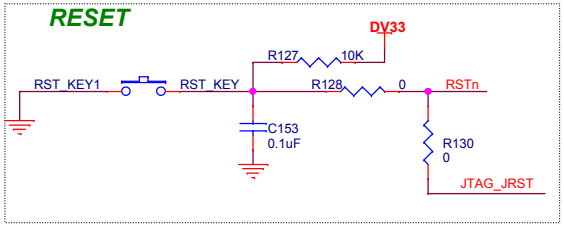
6 XTLO — XTLO
6 XTLI — XTLI

6 SPI_CSn — SPI_CSn
6 SPI_CLK — SPI_CLK
6 SPI_SI_SIO0 — SPI_SI_SIO0
6 SPI_SO_SIO1 — SPI_SO_SIO1
6 SPI_HOLDn_SIO3 — SPI_HOLDn_SIO3
6 SPI_WPn_SIO2 — SPI_WPn_SIO2

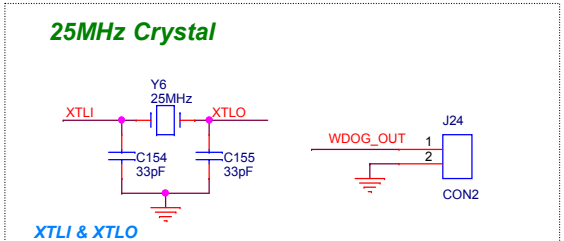
6,10,13 GPIO1 — GPIO1
6,13,15 GPIO2 — GPIO2
6,13 GPIO3 — GPIO3
6,13 GPIO4 — GPIO4
6,13 GPIO5 — GPIO5

6,13 PWM0 — PWM0
6,10,13 PWM1 — PWM1
6,10,13 PWM2 — PWM2
6,13 PWM3 — UART0_CTS
6,13 UART0_CTS — UART0_RTS
6,13 UART0_RTS — UART0_TX
6,13 UART0_TX — UART0_RX
6,13 UART0_RX

RESET

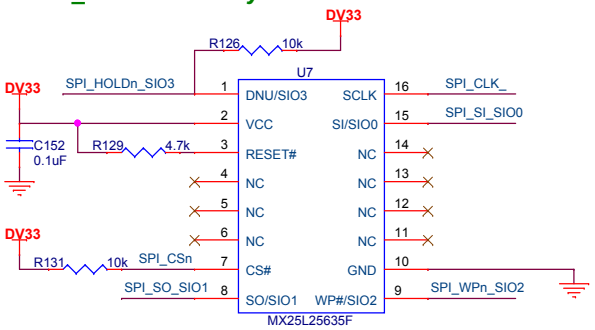


25MHz Crystal

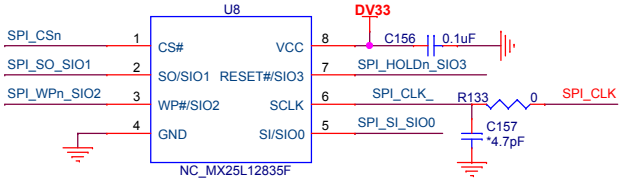


XTLI & XTLO

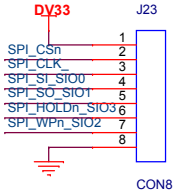
SPI_SOP16/8 co-lay



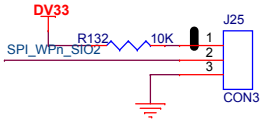
DECAL: 300mil , SOP16, 32MB



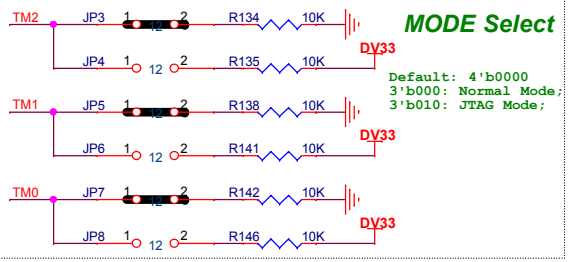
SPI_DEBUG



SPI_WPn Select

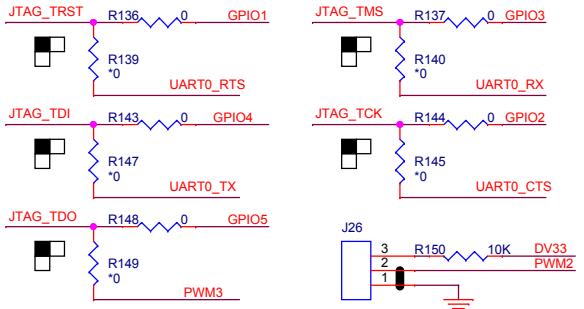


MODE Select



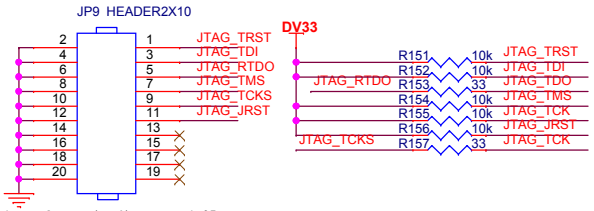
Default: 4'b0000
3'b000: Normal Mode;
3'b010: JTAG Mode;

JTAG Select



PWM2/JTAG_SEL
Default: JTAG Share With GPIO[5:1]
0: GPIO[5:1] share;
1: PWM3+UART0 share;

JTAG 3.3V IO



JP1 Decal : pin distance :1.27mm
pad: 24mil/40mil, DIP20

REALTEK Semiconductor Corp.

Page Name: JTAG_SPI_Clock_RSTn	Designer: Ext. Num:
Product Name: RTS3901_BGA234_L4_Demo Board_V0.2	Approver: Ext.Num :
PCB Name: RTS3901_BGA234_L4_Demo Board_V0.2	Modify Date: Friday, February 26, 2016
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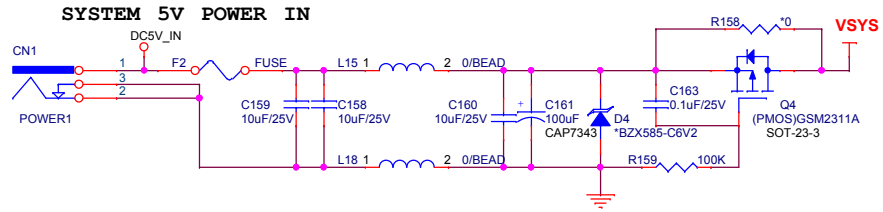
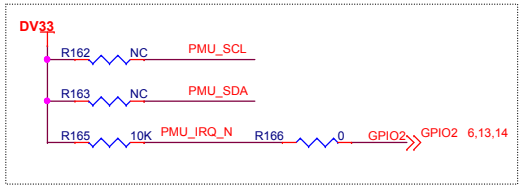
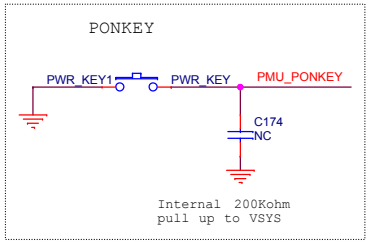
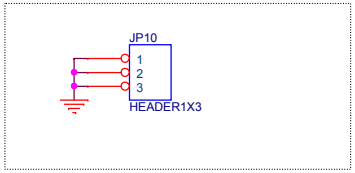
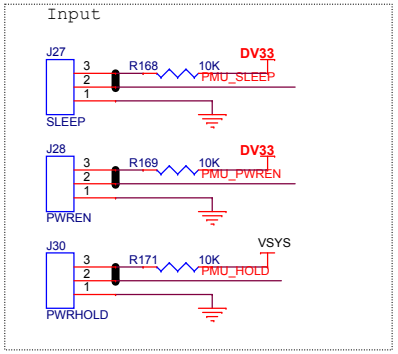
System_Power

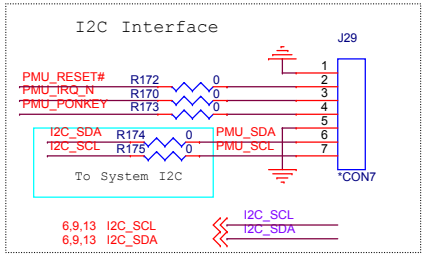


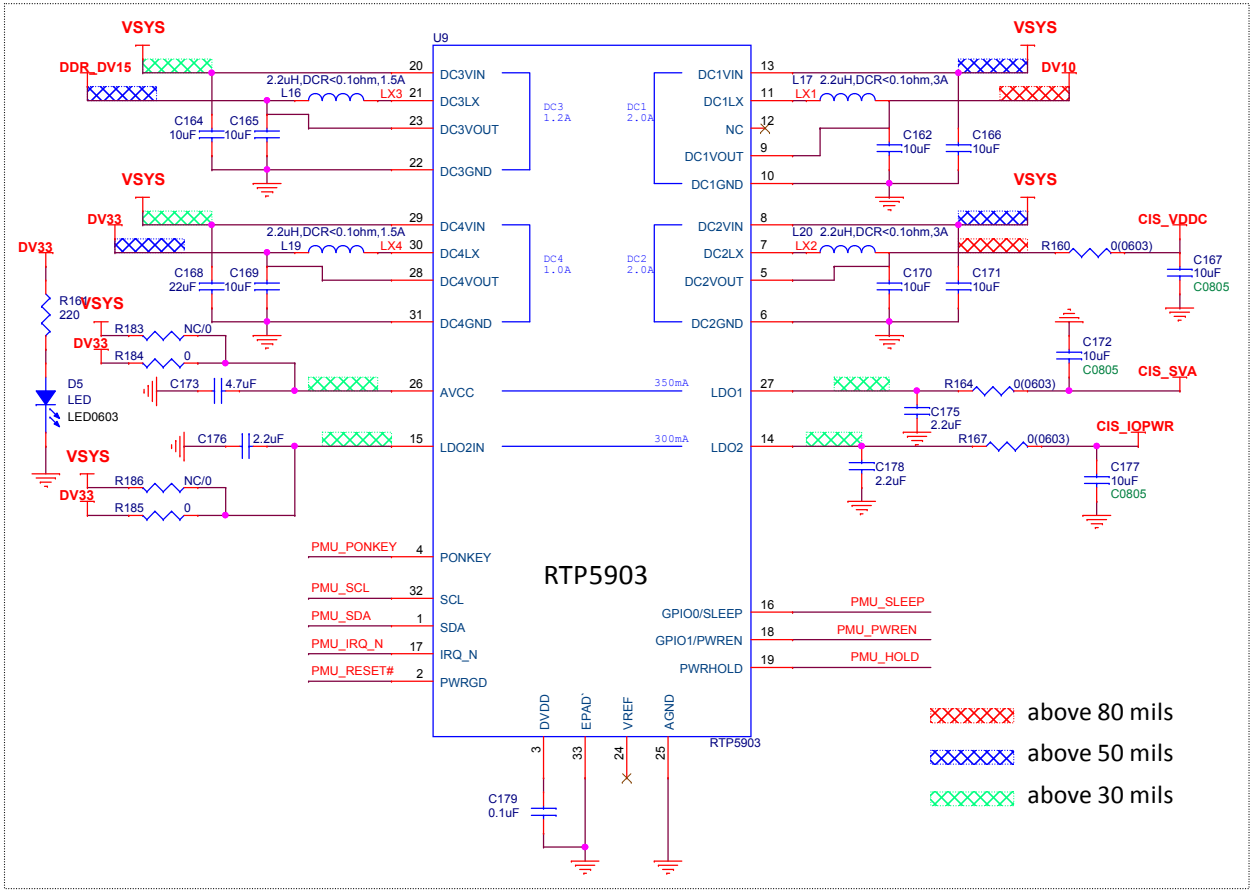


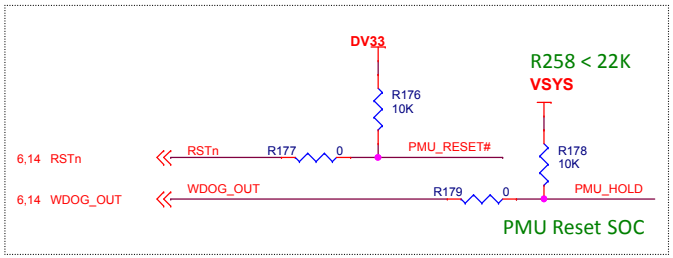


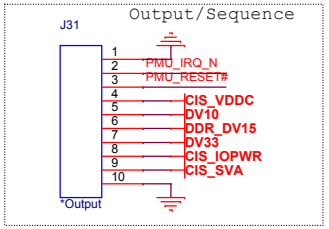












I/O Between PMU and SOC	IO Standard	PU/PD internal
PMU_SCL	Open Drain	NO Pull
PMU_SDA	Open Drain	NO Pull
PMU_IRQ_N	Open Drain	NO Pull
PMU_RESET#	Open Drain	NO Pull
PMU_HOLD	VIL=0.4V, VIH=1.4V	PD
PMU_PWREN	VIL=0.4V, VIH=1.4V	PD
PMU_SLEEP	VIL=0.4V, VIH=1.4V	PD

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Page Name: Power_2	Designer: Ext. Num:
Product Name: RTS3901_BGA234_L4_Demo Board_V0.2	Approver: Ext.Num :
PCB Name: RTS3901_BGA234_L4_Demo Board_V0.2	Modify Date: Wednesday, May 25, 2016
Rev 0.1	Size Custom
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