RTS3902
(Part Number: RTS3902-GR)

FHD H.264 IP CAMERA SoC

BRIEF DATASHEET

Rev. 0.80
28 July 2016

Realtek Semiconductor Corp.
No. 2, Innovation Road II, Hsinchu Science Park, Hsinchu 300, Taiwan
Tel.: +886-3-578-0211. Fax: +886-3-577-6047
www.realtek.com.tw

COPYRIGHT

DISCLAIMER

Realtek provides this document "as is", without warranty of any kind, neither expressed nor implied, including, but not limited to, the particular purpose. Realtek may make improvements and/or changes in this document or in the product described in this document at any time. This document could include technical inaccuracies or typographical errors.

TRADEMARKS

Realtek is a trademark, of Realtek Semiconductor Corporation. Other names mentioned in this document are trademarks/registered trademarks of their respective owners.

USING THIS DOCUMENT

This document is intended for the hardware and software engineer's general information on the Realtek RTS3902 PC camera IC.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide. In that event, please contact your Realtek representative for additional information that may help in the development process.

REVISION HISTORY

Revision	Release Date	Summary
0.50	2016/03/08	Initial release
0.60	2016/06/06	Update pin descriptions
0.70	2016/06/08	Update pin assignment and pin descriptions
0.80	2016/07/28	Modify supported Video Streaming

Table of Contents

List of Tables

List of Figures

1. General Description

1.1. Introduction

1.1.1. Application Scenarios

As a professional system-on-chip (SoC), the RTS3902 is designed for the IP camera. Based on application requirements, it encodes multiple streams in H.264 format and provides superior image signal processing (ISP) performance, high encoded video quality, and a high-performance intelligent acceleration engine. With these features, it meets customers' requirements for product functions, performance, and image quality, and helps customers significantly reduce the engineering bill of materials costs. The following describes typical 1080P IP camera solutions.

1.2. Overview

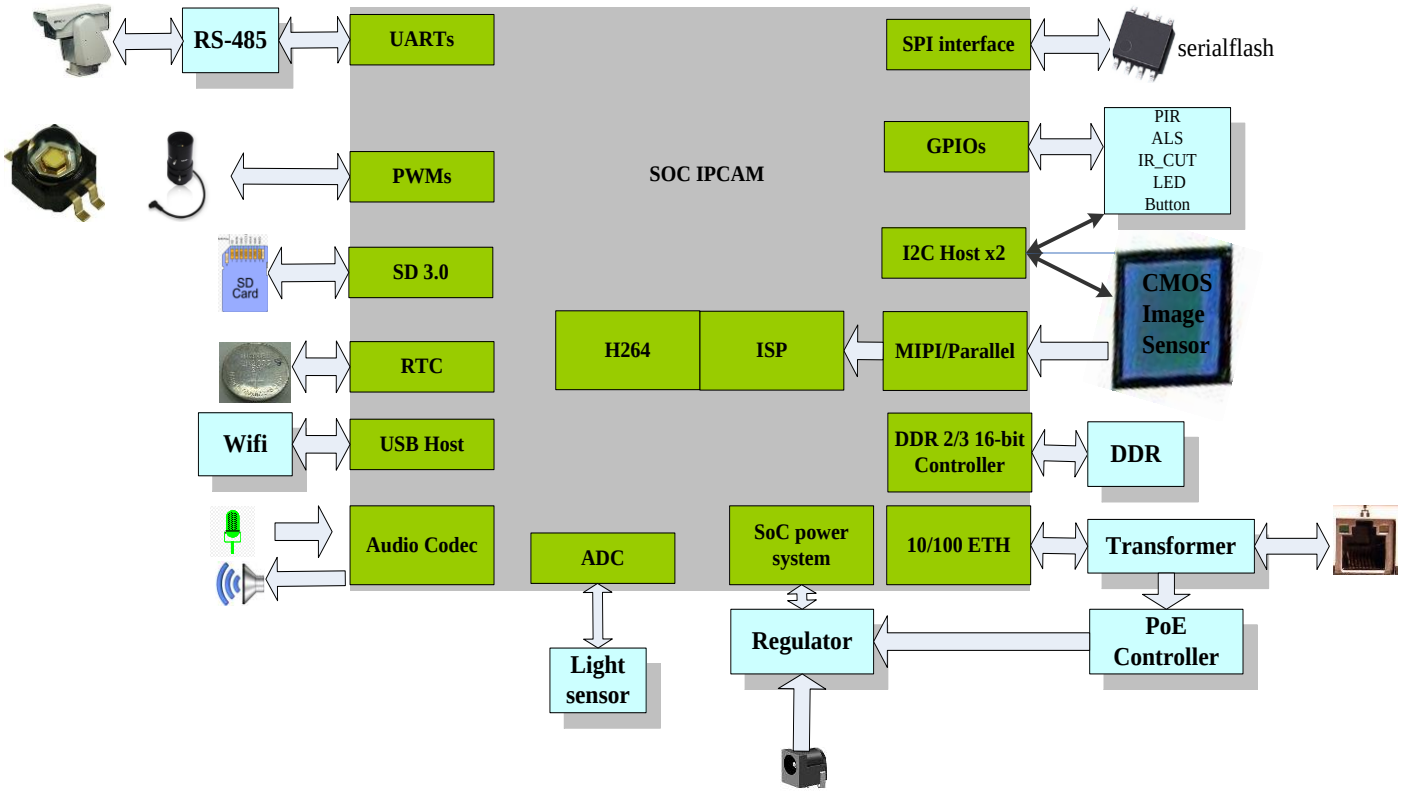


Figure 1-1 IP Camera solution

2. Architecture

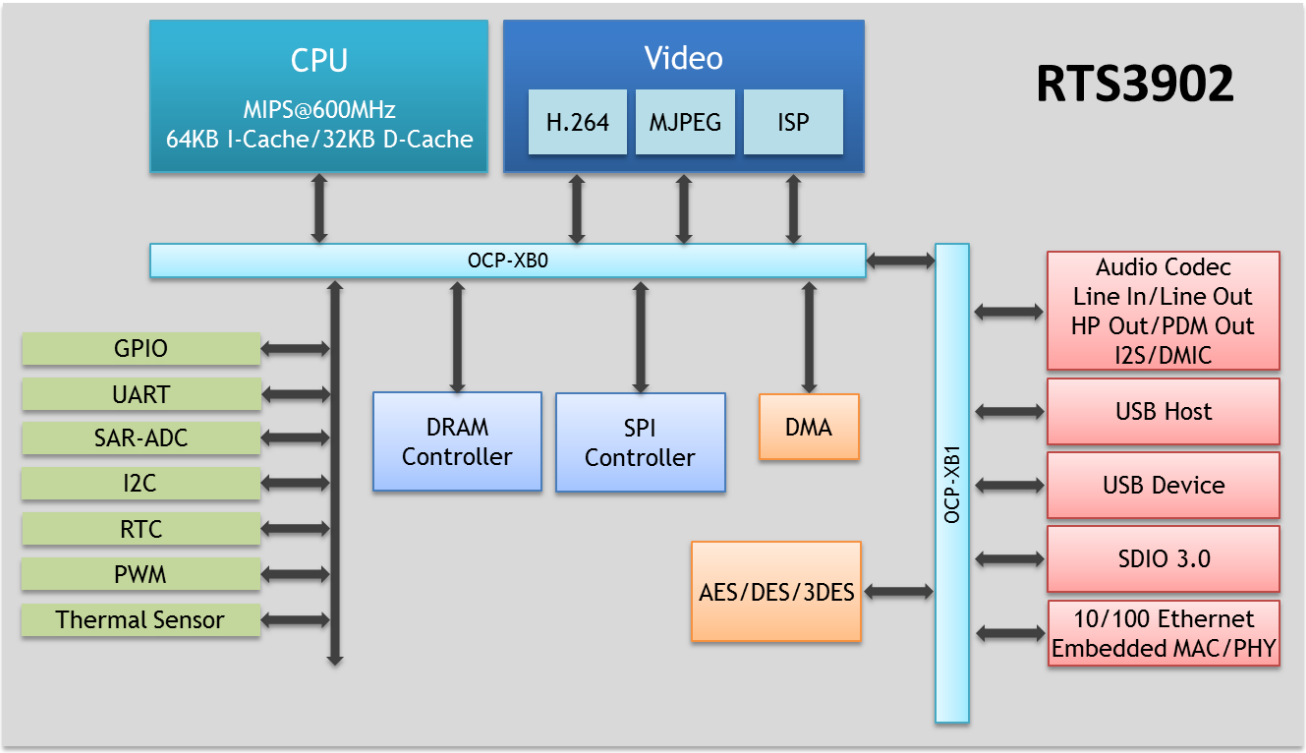


Figure 2-1 Architecture Diagram

2.1. System Profile

2.1.1. Central Processing Unit (CPU)

Table 2-1 RTS3902 CPU

CPU Type	System CPU	ISP MCU
	MIPS	DW8051
Operation Frequency	600MHz	120 MHz
I-Cache	64KB	2KB
D-Cache	32KB	-
IMEM0	8KB	-
IMEM1	8KB	-
DMEM0	16KB	-
DMEM1	16KB	-

2.1.1.1 ISP CPU (DW8051)

For ISP control we use DW8051 MCU, which run on 120MHz. It needs run four cycles per instruction. The code is stored on SPI flash. It has 2KB internal cache with 32byte per line to access serial flash. Code memory mapping size is configurable to any size from 1K to 124K bytes by MCU code bank function

2.1.1.2 System CPU

The system CPU will adapt MIPS with 64KB instruction cache and 32KB data cache. The CPU will run around 600MHz. It has individual internal instruction memory and data memory to promote software performance. EJTAG is supported for System CPU.

2.1.2. External Memory

- Support 16 bit DDR3@1600Mbps up to 2Gb

2.1.3. SPI Serial Flash

- Support QPI mode and 1/2/4 channel mode
- Support 16MB/32MB SPI flash
- Support 4 byte address mode for 32MB flash

2.1.4. Security Engine

- AES key 128/192/256bits
- AES data block length 128bits
- DES key 64bits
- 3DES key 192bits, support 3key/2key
- DES/3DES data block 64bits
- Support multi-buffer encryption/decryption
- Support inter-buffer data splicing
- Support auto-padding

2.2. Networking

2.2.1. Ethernet

- Embedded 10/100 Mac and Physical Layer

2.2.2. Wireless

- Support USB2.0 Wi-Fi module
- Support SDIO Wi-Fi module

2.3. Video Features

2.3.1. Sensor interface

- 4-lane MIPI
- Support parallel interface
- Support 8-Bit/10-Bit/12-Bit Raw Data input
- HCLK support 24MHz/27MHz or 54MHz/37.125MHz or 74.25MHz

2.3.2. Image Signal Processor

- Support 3A(AE/AWB/AF)
- 3D-denoise
- De-haze
- LDC
- Individual Len Shading Correction for R/G/B channel
- Support 2M resolution
- Rotate 90/270 degree(H.264)
- Mirror and flip

- Support WDR
- OSD support 6 areas and monochrome pictures with 4 channel, support alpha-blending OSD
- IQ tuning tool through Ethernet/Wi-Fi
- Private mask support 5 area
- Support 4 channel zoom out

2.3.3. Encoder

- Support H.264 & MJPEG encoder
- H.264 support 2 window ROI
- Maximum H.264 resolution is 2M
- H.264 encoder support Base Line/Main Profile /High Profile level 5.1

2.3.4. Video Streaming

- Support H.264 4-stream : 1080p@30fps+D1@30fps+VGA@30fps+QVGA@30fps
- H.264 stream support CBR & VBR
- Support MJPEG 2MP@30fp

2.3.5. Intelligent Video Analytics

- Motion detection
- Privacy mask

2.4. Audio Features

- Build-in one 24-bit audio codec
- Support Stereo ADC/DAC, DMIC input, PDM output
- One I2S interface for professional audio codec
- I2S PLL for MCLK 24MHz/512FS/256FS and BCLK
- Support sample rate: 48kHz/44.1kHz/32kHz/16kHz/8kHz
- Support G.711/G.726/AAC encoding
- Acoustic echo cancellation (SW or I2S Codec)
- Support mono mode

2.5. Peripheral

- GPIO x14
- PWM x4
- SARADC 3-channel
- RTC
- UART x3
- I2C interface
- Embedded thermal sensor

3. Pin Assignment

3.1. TFBGA-234

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
A	DDR_UDQS	DDR_DV15	DDR_DQ[12]	DDR_LDM	DDR_LDQSN	DDR_DQ[6]	DDR_DQ[4]	DDR_DQ[2]	DDR_DV15	DDR_CKN	DDR_CKE	DDR_BA[0]	DDR_ODT	DDR_CSN	DDR_A[2]	DVSS	A
B	DDR_UDQSN	DVSS	DDR_DQ[9]	DDR_DQ[10]	DDR_LDQS	DDR_DQ[7]	DDR_DQ[5]	DDR_VREF[0]	DDR_RASN	DDR_CK	DDR_WEN	DDR_BA[2]	DDR_A[10]	DDR_A[6]	DDR_A[12]	DDR_DV15	B
C	DDR_DQ[13]	DDR_DV15	DVSS	DDR_DQ[8]	DDR_DQ[0]	DDR_DQ[1]	DDR_DQ[3]	DVSS	DDR_CASN	DDR_BA[1]	DDR_A[0]	DDR_A[4]	DDR_RSTN	DDR_A[5]	DDR_A[7]	DDR_A[9]	C
D	DDR_UDM	DDR_DQ[15]	DDR_DQ[14]	DDR_DQ[11]	DDR_DV15	DDR_VREF[1]	x	x	x	x	DDR_A[14]	DDR_A[1]	DDR_A[3]	DDR_A[13]	DDR_A[8]	DDR_A[11]	D
E	CIS_GPIO[6]	CIS_GPIO[1]	CIS_GPIO[2]	CIS_IOPWR	DVSS	DV10	DV10	DV10	DDR_PLL_DV33	DDR_DV15	DDR_ZQ	DVSS	AC_PDM_OUT_CLK	AC_PDM_OUT_DAT	AC_DMIC_IN_CLK	AC_DMIC_IN_DAT	E
F	CIS_HCLK	CIS_GPIO[4]	CIS_GPIO[7]	CIS_GPIO[3]	x	DVSS	DVSS	DVSS	DVSS	DVSS	DV33	x	AC_I2S_OUT	AC_I2S_IN	AC_I2S_SCK	AC_I2S_MCLK	F
G	CIS_PCLK	CIS_HSYNC	CIS_VSYNC	CIS_GPIO[5]	x	DV33	DVSS	DVSS	DVSS	DVSS	DV10	x	AC_I2S_WS	PWM[0]	PWM[1]	PWM[2]	G
H	CIS_D[10]/D0_P	CIS_D[11]/D0_N	CIS_D[1]	x	x	DV10	DVSS	DVSS	DVSS	DVSS	DV10	x	DVSS	AC_I2S_IOPWR	AC_HP_L	AC_HP_R	H
J	CIS_D[8]/D1_P	CIS_D[9]/D1_N	CIS_D[0]	CIS_SCL	x	DV10	DVSS	DVSS	DVSS	DVSS	DV33	x	AC_VCM	AC_HP_AV33	AC_LINE_OUT_R	AC_LINE_OUT_L	J
K	CIS_D[6]/CK_P	CIS_D[7]/CK_N	GPIO[1]	CIS_SDA	x	DV10	DVSS	DVSS	DVSS	DVSS	AV33	x	DVSS	AC_AMIC_PWR	AC_LINE_IN_R	AC_LINE_IN_L	K
L	CIS_D[4]/D2_P	CIS_D[5]/D2_N	GPIO[2]	GPIO[3]	x	DV33	DV10	DV10	DVSS	DVSS	AV10	x	AC_AV33	AC_DV33	USB_DEV_VBUS/GPIO	USB_HOST_PWR_EN	L
M	CIS_D[2]/D3_P	CIS_D[3]/D3_N	GPIO[4]	GPIO[5]	DVSS	x	x	x	x	x	x	USB_AV10	DVSS	USB_HOST_OCD	USB_DEV_DM	USB_DEV_DP	M
N	SD_D[1]	SD_D[0]	SD_WP	GPIO[6]	TM[2]	UART0_CTS	UART0_RX	PWM[3]	UART1_TX	ETH_DV10	SARADC_AV33	SARADC_CH[0]	SARADC_CH[2]	USB_AV33	USB_HOST_DM	USB_HOST_DP	N
P	SD_CLK	SD_CMD	SD_CD	GPIO[7]	TM[0]	TM[1]	UART0_RTS	UART0_TX	UART1_RX	ETH_DV33	DVSS	SARADC_CH[1]	x	REXT	DVSS	RTC_DV10	P
R	SD_D[3]	SD_D[2]	SD_IOPWR	DVSS	RSTN	SPI_CLK	SPI_MOSI_SIO[0]	SPI_HOLDN_SIO[3]	UART2_TX	ETH_TXOP	ETH_RXIP	DVSS	DVSS	DVSS	RTC_PWR	RTC_XTLO	R
T	DVSS	SD_PWR_EN	I2C_SDA	I2C_SCL	WDOG_OUT	SPI_MISO_SIO[1]	SPI_CSN	SPI_WPN_SIO[2]	UART2_RX	ETH_TXON	ETH_RXIN	DVSS	XTLI	XTLO	DVSS	RTC_XTLI	T
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	

3.2. Package and Version Identification

Green package is indicated by a ‘G’ in the location marked ‘T’. The silicon and FW ROM version number is shown in the location marked ‘V’.

4. Pin Descriptions

Table 4-1 I/O Type Description

I/O Type	Description
I	Input
O	Output
IH	Input with internal pull-up 200K
IL	Input with internal pull-down 200K
I/O	Input/Output
IOH	Input/Output with internal pull-up 200K
IOL	Input/Output with internal pull-down 200K
IOSH	Input/Output with Schmitt trigger
IO-U	USB related IO
CLK	Clock related IO
PWR-O	Power output pin
PWR-I	Power input pin
GND	Ground related pin

4.1. USB Transceiver Interface

Table 4-2 USB Transceiver Pins

Name	Type	Ball No.	Description
USB_AV33	PWR-I	N14	USB BUS 3.3V input
USB_AV10	PWR-I	M12	USB BUS 1.0V input
USB_HOST_DM	IO-U	N15	USB host DM, downstream port
USB_HOST_DP	IO-U	N16	USB host DP, downstream port
USB_HOST_PWR_EN	O	L16	Control USB device power under this host.
USB_HOST_OCD	I	M14	Over-current indicator signal of the USB port,
USB_DEV_DM	IO-U	M15	USB device DM, upstream port
USB_DEV_DP	IO-U	M16	USB device DP, upstream port
USB_DEV_VBUS/GPIO	I/O	L15	Function 1: For detect the USB host device plug in to our USB device port Function 2:configure to GPIO
			Total: 9 Pins

4.2. System Interface

Table 4-3. System Interface Pins

Name	Type	Ball No.	Description
RSTn	I	R5	System reset, low active.
TM[2]	I	N5	Internal pull down. Test Mode refer to reference design
TM[1]	I	P6	Internal pull down. Test Mode refer to reference design
TM[0]	I	P5	Internal pull down. Test Mode refer to reference design
XTLO	O	T14	25M Crystal output
XTLI	I	T13	25M Crystal input

RTC_XTLI	I	T16	32.768KHz Crustal input
RTC_XTLO	O	R16	32.768KHz Crustal output
RTC_PWR	PWR-I	R15	It usually connect to button cell battery for RTC power
RTC_DV10	PWR-O	P16	Connect 0.1uF to GND
REXT	I	P14	External 6.2KOhm 1% resistor to ground for internal reference.
WDOG_OUT	O	T5	Watch dog reset out
I2C_SCL	I/O	T4	CPU I2C Bus Clock
I2C_SDA	I/O	T3	CPU I2C Bus Data
			Total: 14 Pins

4.3. SPI Serial Flash Interface

Table 4-4. Serial Flash Interface

Name	Type	Ball No.	Description
SPI_CSn	IOH	T7	SPI Flash interface, storage boot code.
SPI_CLK	IOH	R6	Clock signal
SPI_MOSI_SIO[0]	IOH	R7	Master Output Slave Input (for 1xI/O) / Serial Data Input & Output (for 2xI/O or 4xI/O read mode)
SPI_MISO_SIO[1]	IOH	T6	Master Input Slave Output (for 1xI/O) / Serial Data Input & Output (for 2xI/O or 4xI/O read mode)
SPI_HOLDn_SIO[3]	IOH	R8	Hold or Reset / Serial Data Input & Output (for 2xI/O or 4xI/O read mode)
tsSPI_WPn_SIO[2]	IOH	T8	Serial flash Write Protect / Serial Data Input & Output (for 2xI/O or 4xI/O read mode)
			Total: 6 Pins

4.4. SD 3.0 Interface

Table 4-5. SD3.0 Interface

Name	Type	Ball No.	Description
SD_D[1]	I/O	N1	SD data 1
SD_D[0]	I/O	N2	SD data 0
SD_CLK	O	P1	SD Clock pin
SD_IOPWR	PWR-O	R3	Add 1uF to GND, it can be changed to 1.8V at SD3.0 mode automatically.
SD_CMD	I/O	P2	SD Command pin
SD_D[3]	I/O	R1	SD Data 3
SD_D[2]	I/O	R2	SD Data 2
SD_WP	I/O	N3	SD card write protect
SD_CDn	I/O	P3	SD card detect
SD_PWR_EN	O	T2	Function 1: SD Power control. Function 2: GPIO
			Total: 10 Pins

4.5. UART Interface

Table 4-6. UART Interface

Name	Type	Ball No.	Description
UART0_CTS	I/O	N6	Function 1: UART0 CTS Function 2: JTAG_CLK Function 3: GPIO
UART0_RTS	I/O	P7	Function 1: UART0 RTS Function 2: JTAG_ RSTn Function 3: GPIO
UART0_TX	I/O	P8	Function 1: UART0 TX Function 2: JTAG_TDI Function 3: GPIO
UART0_RX	I/O	N7	Function 1: UART0 RX Function 2: JTAG_TMS Function 3: GPIO
UART1_TX	I/O	N9	Function 1: UART1 TX for console debug port Function 2: GPIO
UART1_RX	I/O	P9	Function 1:UART1 RX for console debug port Function 2: GPIO
UART2_TX	I/O	R9	Function 1: UART2 TX Function 2: GPIO
UART2_RX	I/O	T9	Function 1:UART2 RX Function 2: GPIO
			Total: 8 Pins

4.6. SAR-ADC Interface

Table 4-7. SAR-ADC Interface

Name	Type	Ball No.	Description
SARADC_AV33	PWR-I	N11	Internal SAR-ADC Power input
SARADC_CH[0]	I	N12	SAR-ADC channel 0
SARADC_CH[1]	I	P12	SAR-ADC channel 1
SARADC_CH[2]	I	N13	SAR-ADC channel 2
			Total: 4 Pins

4.7. DDR Interface

Table 4-8. DDR Interface

Name	Type	Ball No.	Description
DDR_PLL_DV33	PWR-I	E9	DDR PHY PLL 3.3V power input
DDR_ZQ	I	E11	Internal pull low 240 ohm to GND, please floating this pin on PCB

DDR_DV15	PWR-I	A2,A9,B16,C2, D5,E10	DDR2 1.5V power for internal DDR chip and DDR controller
DDR_VREF[0]	PWR-I	B8	DDR VREF0 power
DDR_VREF[1]	PWR-I	D6	DDR VREF1 power
DDR_CK	O	B10	Positive differential clock output
DDR_CKN	O	A10	negative differential clock output
DDR_RSTN	O	C13	Active Low Asynchronous Reset
DDR_CSN	O	A14	Chip Select signal
DDR_ODT	O	A13	On Die Termination
DDR_CKE	O	A11	Clock Enable signal
DDR_WEN	O	B11	Command Signal
DDR_RASN	O	B9	Command Signal
DDR_CASN	O	C9	Command Signal
DDR_LDM	O	A4	Data Mask
DDR_UDM	O	D1	Data Mask
DDR_BA[0]	O	A12	Bank Address
DDR_BA[1]	O	C10	Bank Address
DDR_BA[2]	O	B12	Bank Address
DDR_A[0]	O	C11	Address output
DDR_A[1]	O	D12	Address output
DDR_A[2]	O	A15	Address output
DDR_A[3]	O	D13	Address output
DDR_A[4]	O	C12	Address output
DDR_A[5]	O	C14	Address output
DDR_A[6]	O	B14	Address output
DDR_A[7]	O	C15	Address output
DDR_A[8]	O	D15	Address output
DDR_A[9]	O	C16	Address output
DDR_A[10]	O	B13	Address output
DDR_A[11]	O	D16	Address output
DDR_A[12]	O	B15	Address output
DDR_A[13]	O	D14	Address output
DDR_A[14]	O	D11	Address output
DDR_DQ[0]	I/O	C5	Data input/output
DDR_DQ[1]	I/O	C6	Data input/output
DDR_DQ[2]	I/O	A8	Data input/output
DDR_DQ[3]	I/O	C7	Data input/output
DDR_DQ[4]	I/O	A7	Data input/output
DDR_DQ[5]	I/O	B7	Data input/output
DDR_DQ[6]	I/O	A6	Data input/output
DDR_DQ[7]	I/O	B6	Data input/output
DDR_LDQS	I/O	B5	DDR_DQ[7:0] Data strobe
DDR_LDQSn	I/O	A5	DDR_DQ[7:0] Data strobe
DDR_DQ[8]	I/O	C4	Data input/output
DDR_DQ[9]	I/O	B3	Data input/output
DDR_DQ[10]	I/O	B4	Data input/output
DDR_DQ[11]	I/O	D4	Data input/output
DDR_DQ[12]	I/O	A3	Data input/output
DDR_DQ[13]	I/O	C1	Data input/output
DDR_DQ[14]	I/O	D3	Data input/output

DDR_DQ[15]	I/O	D2	Data input/output
DDR_UDQS	I/O	A1	DDR_DQ[15:8] Data strobe
DDR_UDQSn	I/O	B1	DDR_DQ[15:8] Data strobe
			Total: 59 Pins

4.8. CMOS Image Sensor Interface

Table 4-9. CMOS Image Sensor Interface

Name	Type	Ball No.	Description
CIS_GPIO[1]	I/O	E2	Function 1: For Sensor power down Function 2: GPIO
CIS_GPIO[2]	I/O	E3	Function 1: For Sensor LDO ON/OFF Function 2: MCU GPIO port2
CIS_GPIO[3]	I/O	F4	Function 1: IR-CUT enable and disable Function 2: MCU GPIO port3
CIS_GPIO[4]	I/O	F2	Function 1: IR_LED Control Function 2: MCU GPIO port4
CIS_GPIO[5]	I/O	G4	Function 1: PIR Status detect Function 2: MCU GPIO port4
CIS_GPIO[6]	I/O	E1	Function 1: For Sensor reset Function 2: GPIO
CIS_GPIO[7]	I/O	F3	Function 1: For Live view ready indicator LED Function 2: GPIO
CIS_HCLK	O	F1	System master clock of sensor
CIS_SDA	I/O	K4	MCU I2C Bus Data
CIS_SCL	O	J4	MCU I2C Bus Clock
CIS_VSYNC	I	G3	Vertical sync signal of sensor data
CIS_HSYNC	I	G2	Horizontal sync signal of senor data
CIS_PCLK	I	G1	Pixel clock of sensor
CIS_IOPWR	PWR-I	E4	Power input with the same IO voltage as CMOS image sensor.
CIS_D[11]/D0_N	I	H2	Pixel Data Bus Parallel interface:D11 Serial interface:D0_N
CIS_D[10]/D0_P	I	H1	Pixel Data Bus Parallel interface:D10 Serial interface:D0_P
CIS_D[9]/D1_N	I	J2	Pixel Data Bus Parallel interface:D9 Serial interface:D1_N
CIS_D[8]/D1_P	I	J1	Pixel Data Bus Parallel interface:D8 Serial interface:D1_P
CIS_D[7]/CK_N	I	K2	Pixel Data Bus Parallel interface:D7 Serial interface:ClK_N
CIS_D[6]/CK_P	I	K1	Pixel Data Bus Parallel interface:D6 Serial interface:CLK_P
CIS_D[5]/D2_N	I	L2	Pixel Data Bus Parallel interface:D5 Serial interface:D2_N

CIS_D[4]/D2_P	I	L1	Pixel Data Bus Parallel interface:D4 Serial interface:D2_P
CIS_D[3]/D3_N	I	M2	Pixel Data Bus Parallel interface:D3 Serial interface:D3_N
CIS_D[2]/D3_P	I	M1	Pixel Data Bus Parallel interface:D2 Serial interface:D3_P
CIS_ D[1]	I	H3	Pixel Data Bus Parallel interface:D1
CIS_D[0]	I	J3	Pixel Data Bus Parallel interface:D0
			Total: 26 Pins

4.9. PWM Interface

Table 4-10. PWM Interface

Name	Type	Ball No.	Description
PWM[0]	I/O	G14	Function 1: PWM0 OUTPUT Function 2: GPIO
PWM[1]	I/O	G15	Function 1: PWM1 OUTPUT Function 2: ETH_LED[0]. Function 3: GPIO
PWM[2]	I/O	G16	Function 1: PWM2 OUTPUT Function 2: ETH_LED[1] . Function 3：JTAG_SEL, 0: GPIO[5:1] for JTAG; 1: UART pin for JTAG. Function 4: GPIO
PWM[3]	I/O	N8	Function 1: PWM3 OUTPUT Function 2: ETH_LED[3] Function 3: JTAG_TDO Function 4: GPIO
			Total: 4 Pins

4.10. Audio Interface

Table 4-11. Audio Interface

Name	Type	Ball No.	Description
AC_DV33	PWR-I	L14	For AMIC power 3.3V input
AC_AMIC_PWR	PWR-O	K14	LDO output for AMIC bias
AC_AV33	PWR-I	L13	Audio DAC/ADC 3.3V power input
AC_LINE_IN_L	I	K16	Line in left channel
AC_LINE_IN_R	I	K15	Line in right channel
AC_VCM	PWR-O	J13	Common mode voltage, External 1uF to GND
AC_LINE_OUT_L	O	J16	Line out left channel
AC_LINE_OUT_R	O	J15	Line out right channel

AC_HP_OUT_L	O	H15	Headphone left channel
AC_HP_OUT_R	O	H16	Headphone right channel
AC_HP_A3V3	PWR-I	J14	Head Phone power input
AC_DMIC_IN_DAT	I	E16	Function 1: PDM in data, get back data from DMIC. Function 2: GPIO
AC_DMIC_IN_CLK	O	E15	Function 1: PDM in clock, output clock to external DMIC. Function 2: GPIO
AC_I2S_IOPWR	PWR-O	H14	I2S interface power output
AC_I2S_MCLK	O	F16	System master clock
AC_I2S_SCK	O	F15	I2S clock output
AC_I2S_WS	O	G13	I2S channel select
AC_I2S_SD_OUT	O	F13	I2S data output
AC_I2S_SD_IN	I	F14	I2S data input
AC_PDM_OUT_DAT	O	E14	PDM data output
AC_PDM_OUT_CLK	O	E13	PDM clock output
			Total: 21 Pins

4.11. Ethernet Interface

Table 4-12. Ethernet Interface

Name	Type	Ball No.	Description
ETH_DV33	PWR-I	P10	Ethernet PHY 3.3V input
ETH_DV10	PWR-I	N10	Ethernet PHY 1.0V input
ETN_TXOP	I/O	R10	100-ohm differential transmit positive output, support cross-over mode
ETN_TXON	I/O	T10	100-ohm differential transmit negative output, support cross-over mode
ETN_RXIP	I/O	R11	100-ohm differential receive positive input, support cross-over mode
ETN_RXIN	I/O	T11	100-ohm differential receive negative input ,support cross-over mode
			Total: 6 Pins

4.12. GPIO

Table 4-13. GPIO Interface

Name	Type	Ball No.	Description
GPIO[1]	I/O	K3	GPIO1
GPIO[2]	I/O	L3	GPIO2
GPIO[3]	I/O	L4	GPIO3
GPIO[4]	I/O	M3	GPIO4
GPIO[5]	I/O	M4	GPIO5
GPIO[6]	I/O	N4	GPIO6
GPIO[7]	I/O	P4	GPIO7
			Total: 7 Pins

4.13. Power/Ground

Table 4-14.Power and Ground pins

Name	Type	Ball No.	Description
DV10	PWR-I	E6,E7,E8,G11, H6,H11,J6,K6, L7,L8	Core power 1.0V power input
DV33	PWR-I	F11,G6,J11,L6	IO power 3.3V power input
AV33	PWR-I	K11	System PLL 3.3V power input
AV10	PWR-I	L11	Analog 1.0V power input
DVSS	GND	A16,B2,C3,C8, E5,E12,F6,F7, F8,F9,F10,G7, G8,G9,G10,H7 ,H8,H9,H10, H13,J7,J8,J9, J10,K7,K8,K9, K10,K13,L9, L10,M5,M13, P11,P15,R4, R12,R13,R14, T1,T12,T15	Ground
			Total: 58 Pins

5. Electrical Characteristics

5.1. DC Characteristics

5.1.1. Absolute Maximum Ratings

Table 5-1. Absolute Maximum Ratings

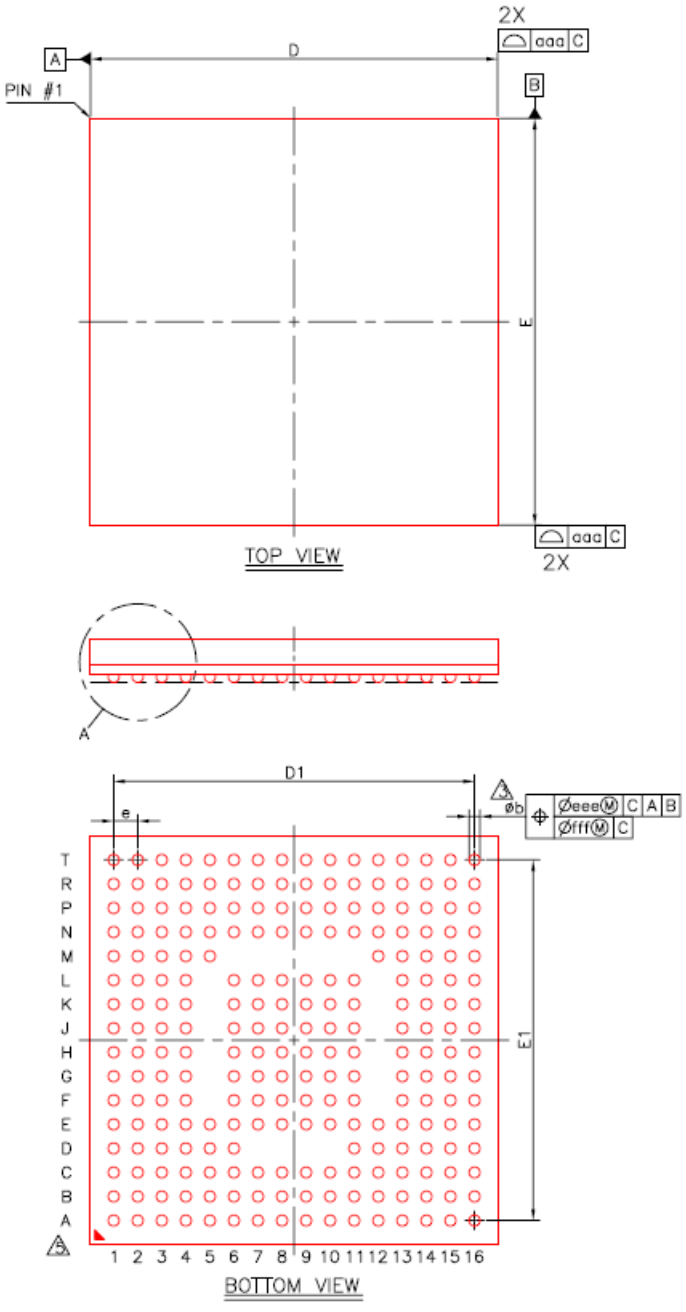
Parameter	Symbol	Minimum	Typical	Maximum	Units
Power Supply Input					
For RTS3902 CORE	DC1V0	0.95	1.0	1.05	V
For RTS3902 I/O	DC3V3	3.15	3.3	3.45	V
For RTS3902 DDR3	DC1V5	1.425	1.5	1.575	V
Operation Current					
For RTS3902 CORE	I_{DC1V0}		510		mA
For RTS3902 I/O	I_{DC3V3}		40		mA
For RTS3902 DDR3	I_{DC1V5}		160		mA
Power Dissipation	P_D		0.882		W
Ambient Operating Temperature	Ta	0	-	+70	^oC
Storage Temperature	Ts	-	-	+125	^oC
ESD (Electrostatic Discharge, Human Body Mode)					
	Susceptibility Voltage				
All Pins	4.5KV				

6. Application Circuits

To guarantee the best compatibility and image quality in hardware design with specific image sensor, please contact Realtek to get the up to date application circuits. Any modification is recommended to be double checked by Realtek. Realtek may update the latest application circuits without modifying this datasheet.

7. Package Mechanical Dimensions

7.1. TFBGA-234 Dimension



Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.10	1.17	1.24	0.043	0.046	0.049
A1	0.16	0.21	0.26	0.006	0.008	0.010
A2	0.91	0.96	1.01	0.036	0.038	0.040
c	0.22	0.26	0.30	0.009	0.010	0.012
D	10.90	11.00	11.10	0.429	0.433	0.437
E	10.90	11.00	11.10	0.429	0.433	0.437
D1	---	9.75	---	---	0.384	---
E1	---	9.75	---	---	0.384	---
e	---	0.65	---	---	0.026	---
b	0.25	0.30	0.35	0.010	0.012	0.014
aaa	0.15			0.006		
bbb	0.10			0.004		
ddd	0.08			0.003		
eee	0.15			0.006		
fff	0.08			0.003		
MD/ME	16 / 16					

NOTE :

1. CONTROLLING DIMENSION : MILLIMETER.
2. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
4. SPECIAL CHARACTERISTICS C CLASS: bbb , ddd
5. THE PATTERN OF PIN 1 FIDUCIAL IS FOR REFERENCE ONLY .
6. REFERANCE DOCUMENT : JEDEC PUBLICATION 95 DESIGN GUIDE 4.5

8. Ordering Information

Table 8-1. Ordering Information

Part Number	Package	Status
RTS3902-GR	TFBGA-234 11x11mm^2 ‘Green’ Package	Sample

Realtek Semiconductor Corp.
Headquarters
No. 2, Innovation Road II
Hsinchu Science Park, Hsinchu 300, Taiwan
Tel.: +886-3-578-0211. Fax: +886-3-577-6047
www.realtek.com.tw