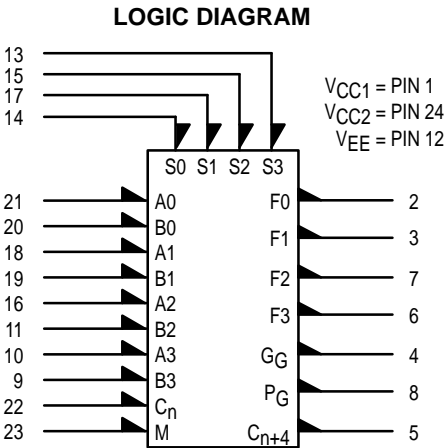


4-Bit Arithmetic Logic Unit/
Function Generator

The MC10181 is a high-speed arithmetic logic unit capable of performing 16 logic operations and 16 arithmetic operations on two four-bit words. Full internal carry is incorporated for ripple through operation.

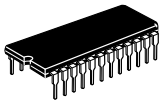
Arithmetic logic operations are selected by applying the appropriate binary word to the select inputs (S0 through S3) as indicated in the tables of arithmetic/logic functions. Group carry propagate (PG) and carry generate (GG) are provided to allow fast operations on very long words using a second order look ahead. The internal carry is enabled by applying a low level voltage to the mode control input (M).

PD = 600 mW typ/pkg (No Load)
tpd (typ): A1 to F = 6.5 ns
 Cn to Cn + 4 = 3.1 ns
 A1 to PG = 5.0 ns
 A1 to GG = 4.5 ns
 A1 to Cn + 4 = 5.0



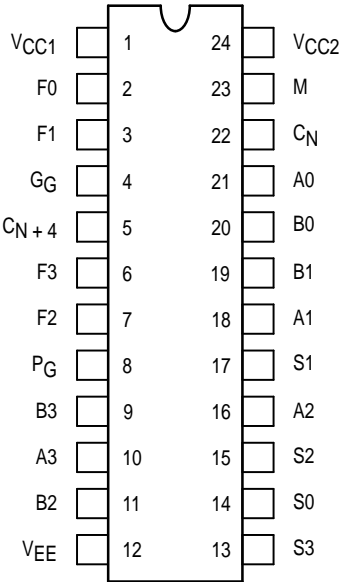
Function Select				Logic Functions	Arithmetic Operation
S3	S2	S1	S0	M is High C = D.C. F	M is Low Cn is low F
L	L	L	L	$F \equiv A$	$F = A$
L	L	L	H	$F = A + B$	$F = A \text{ plus } (A \cdot B)$
L	L	H	L	$F = A + B$	$F = A \text{ plus } (A \cdot B)$
L	L	H	H	F = Logical "1"	$F = A \text{ times } 2$
L	H	L	L	$F = A \cdot B$	$F = (A + B) \text{ plus } 0$
L	H	L	H	$F = B$	$F = (A + B) \text{ plus } (A \cdot B)$
L	H	H	L	$F = A \odot B$	$F = A \text{ plus } B$
L	H	H	H	$F = A + B$	$F = A \text{ plus } (A + B)$
H	L	L	L	$F = A \cdot B$	$F = (A + B) \text{ plus } 0$
H	L	L	H	$F = A \oplus B$	$F = A \text{ minus } B \text{ minus } 1$
H	L	H	L	$F = B$	$F = (A + B) \text{ plus } (A \cdot B)$
H	L	H	H	$F = A + B$	$F = A \text{ plus } (A + B)$
H	H	L	L	F = Logical "0"	$F = \text{minus } 1 \text{ (two's complement)}$
H	H	L	H	$F = A \cdot B$	$F = (A \cdot B) \text{ minus } 1$
H	H	H	L	$F = A \cdot B$	$F = (A \cdot B) \text{ minus } 1$
H	H	H	H	$F = A$	$F = A \text{ minus } 1$

MC10181

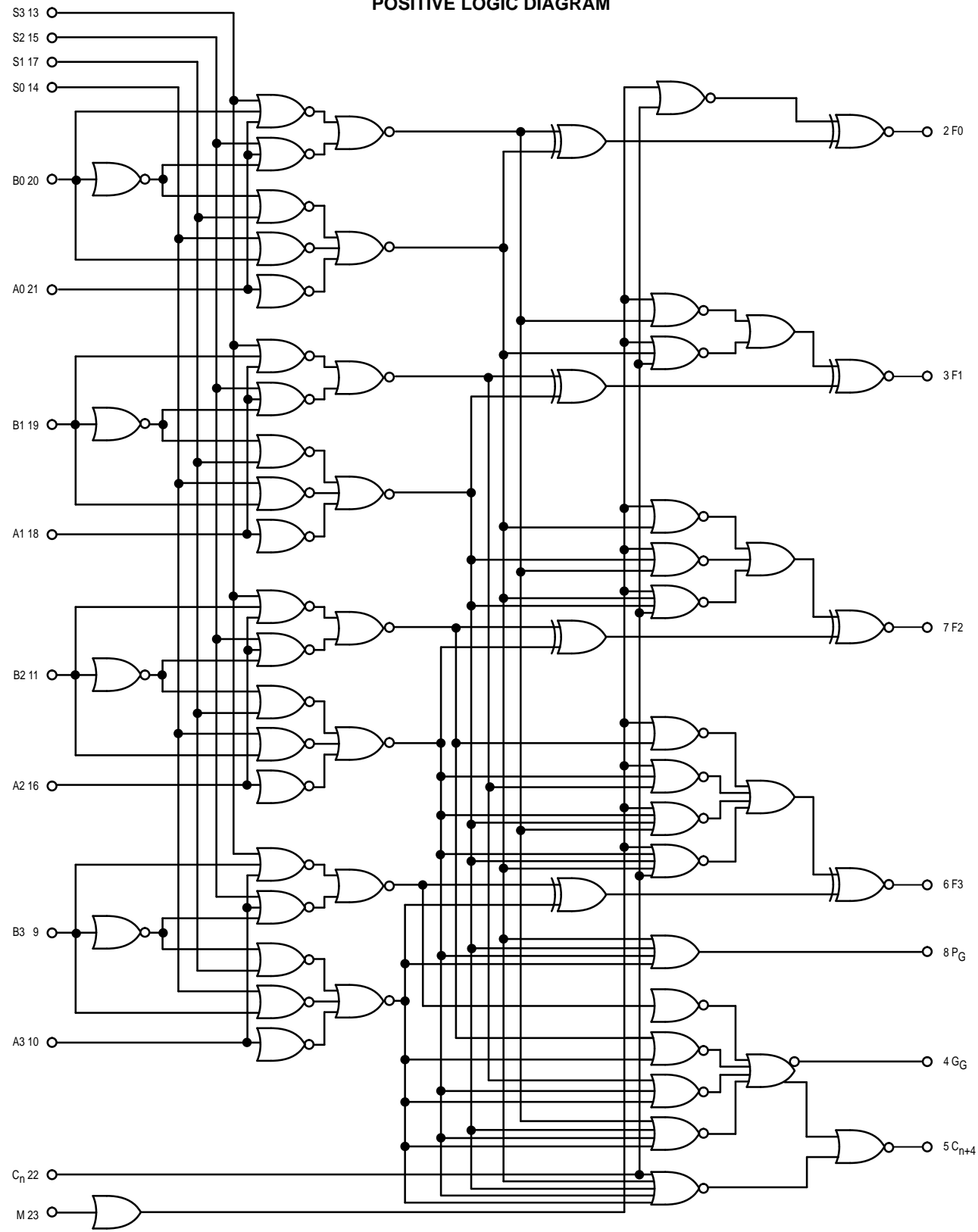


L SUFFIX
CERAMIC PACKAGE
CASE 623-05

PIN ASSIGNMENT



POSITIVE LOGIC DIAGRAM



ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	Test Limits							Unit
			−30°C		+25°C			+85°C		
			Min	Max	Min	Typ	Max	Min	Max	
Power Supply Drain Current	I _E	12		159			145		159	mAdc
Input Current	I _{inH}	9		390			245		245	μAdc
		10		350			220		220	
		11		390			245		245	
		13		320			200		200	
		14		425			265		265	
		15		425			265		265	
		16		350			220		220	
		17		425			265		265	
		18		350			220		220	
		19		390			245		245	
		20		390			245		245	
		21		350			220		220	
22		460			290		290			
23		320			200		200			
Input Leakage Current	I _{inL}	9	0.5		0.5			0.3		μAdc
		10	0.5		0.5			0.3		
		11	0.5		0.5			0.3		
		13	0.5		0.5			0.3		
		14	0.5		0.5			0.3		
		15	0.5		0.5			0.3		
		16	0.5		0.5			0.3		
		17	0.5		0.5			0.3		
		18	0.5		0.5			0.3		
		19	0.5		0.5			0.3		
		20	0.5		0.5			0.3		
		21	0.5		0.5			0.3		
22	0.5		0.5			0.3				
23	0.5		0.5			0.3				
Output Voltage Logic 1	V _{OH}	*	−1.060	−0.890	−0.960		−0.810	−0.890	−0.700	Vdc
Output Voltage Logic 0	V _{OL}	*	−2.000	−1.675	−1.990		−1.650	−1.920	−1.615	Vdc
Threshold Voltage Logic 1	V _{OHA}	*	−1.080		−0.980			−0.910		Vdc
Threshold Voltage Logic 0	V _{OLA}	*		−1.655			−1.630		−1.595	Vdc

* Test all input–output combinations according to Function Table.

** For threshold level test, apply threshold input level to only one input pin at a time.

ELECTRICAL CHARACTERISTICS (continued)

@ Test Temperature			TEST VOLTAGE VALUES (Volts)					(V _{CC}) Gnd
			V _{IHmax}	V _{ILmin}	V _{IHAmin}	V _{ILAmax}	V _{EE}	
			−0.890	−1.890	−1.205	−1.500	−5.2	
			+25°C	−0.810	−1.850	−1.105	−1.475	−5.2
			+85°C	−0.700	−1.825	−1.035	−1.440	−5.2
Characteristic	Symbol	Pin Under Test	TEST VOLTAGE APPLIED TO PINS LISTED BELOW					(V _{CC}) Gnd
			V _{IHmax}	V _{ILmin}	V _{IHAmin}	V _{ILAmax}	V _{EE}	
Power Supply Drain Current	I _E	12					12	1, 24
Input Current	I _{inH}	9	9				12	1, 24
		10	10				12	1, 24
		11	11				12	1, 24
		13	13				12	1, 24
		14	14				12	1, 24
		15	15				12	1, 24
		16	16				12	1, 24
		17	17				12	1, 24
		18	18				12	1, 24
		19	19				12	1, 24
		20	20				12	1, 24
		21	21				12	1, 24
		22	22				12	1, 24
		23	23				12	1, 24
Input Leakage Current	I _{inL}	9		9			12	1, 24
		10		10			12	1, 24
		11		11			12	1, 24
		13		13			12	1, 24
		14		14			12	1, 24
		15		15			12	1, 24
		16		16			12	1, 24
		17		17			12	1, 24
		18		18			12	1, 24
		19		19			12	1, 24
		20		20			12	1, 24
		21		21			12	1, 24
		22		22			12	1, 24
		23		23			12	1, 24
Output Voltage	Logic 1	V _{OH}	*	*	*		12	1, 24
Output Voltage	Logic 0	V _{OL}	*	*	*		12	1, 24
Threshold Voltage	Logic 1	V _{OHA}	*			**	**	12
Threshold Voltage	Logic 0	V _{OLA}	*			**	**	12

* Test all input–output combinations according to Function Table.

** For threshold level test, apply threshold input level to only one input pin at a time.

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50–ohm resistor to −2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

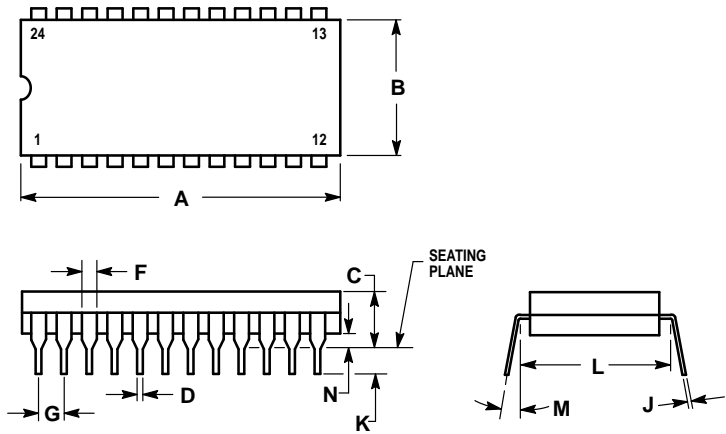
Characteristic	Symbol	Input	Output	Conditions†	AC Switching Characteristics								Unit
					-30°C *		+25°C			+85°C *			
					Min	Max	Min	Typ	Max	Min	Max		
Propagation Delay Rise Time, Fall Time	t ₊₊ , t ₋ – t ₊ , t ₋	C _n C _n	C _{n+4} C _{n+4}	A0, A1, A2, A3 A0, A1, A2, A3	1.0 1.0	5.1 3.2	1.1 1.0	3.1 2.0	5.0 3.0	1.1 1.0	5.4 3.2	ns ns	
Propagation Delay Rise Time, Fall Time	t ₊₊ , t ₊₋ t ₋ , t ₋ – t ₊ , t ₋	C _n C _n C _n	F1 F1 F1	A0 A0 A0	1.7 1.7 1.3	7.2 7.2 5.3	2.0 2.0 1.5	4.5 4.5 3.0	7.0 7.0 5.0	2.0 2.0 1.5	7.5 7.5 5.3	ns ns ns	
Propagation Delay Rise Time, Fall Time	t ₊₊ , t ₊₋ t ₋ , t ₋ – t ₊ , t ₋	A1 A1 A1	F1 F1 F1	— — —	2.6 2.6 1.3	10.4 10.4 5.4	3.0 3.0 1.5	6.5 6.5 3.0	10 10 5.0	3.0 3.0 1.5	10.8 10.8 5.3	ns ns ns	
Propagation Delay Rise Time, Fall Time	t ₊₊ , t ₋ – t ₊ , t ₋	A1 A1	P _G P _G	S0, S3 S0, S3	1.6 0.8	7.0 3.7	2.0 1.1	5.0 2.0	6.5 3.5	2.0 1.1	7.0 3.8	ns ns	
Propagation Delay Rise Time, Fall Time	t ₊₊ , t ₋ – t ₊ , t ₋	A1 A1	G _G G _G	A0, A2, A3, C _n A0, A2, A3, C _n	1.1 1.2	7.4 5.1	2.0 1.5	4.5 4.0	7.0 5.0	1.3 1.2	7.7 5.3	ns ns	
Propagation Delay Rise Time, Fall Time	t ₊₋ , t ₊₊ t ₊ , t ₋	A1 A1	C _{n+4} C _{n+4}	A0, A2, A3, C _n A0, A2, A3, C _n	1.7 1.0	7.3 3.1	2.0 1.0	5.0 2.0	7.0 3.0	2.0 1.0	7.8 3.2	ns ns	
Propagation Delay Rise Time, Fall Time	t ₊₊ , t ₊₊ t ₊ , t ₋	B1 B1	F1 F1	S3, C _n S3, C _n	2.7 1.2	11.3 5.3	3.0 1.5	8.0 3.5	11 5.0	3.0 1.5	11.9 5.3	ns ns	
Propagation Delay Rise Time, Fall Time	t ₊₊ , t ₋ – t ₊ , t ₋	B1 B1	P _G P _G	S0, A1 S0, A1	1.6 1.0	7.7 3.6	2.0 1.1	6.0 2.0	7.5 3.5	2.0 1.1	8.0 3.9	ns ns	
Propagation Delay Rise Time, Fall Time	t ₊₊ , t ₋ – t ₊ , t ₋	B1 B1	G _G G _G	S3, C _n S3, C _n	1.7 1.4	8.2 5.2	2.0 1.5	6.0 3.0	8.0 5.0	2.0 1.2	8.6 5.4	ns ns	
Propagation Delay Rise Time, Fall Time	t ₊₋ , t ₊₊ t ₊ , t ₋	B1 B1	C _{n+4} C _{n+4}	S3, C _n S3, C _n	1.8 0.9	8.2 3.1	2.0 1.0	6.0 2.0	8.0 3.0	2.0 1.0	8.7 3.2	ns ns	
Propagation Delay Rise Time, Fall Time	t ₊₊ , t ₊₋ t ₊ , t ₋	M M	F1 F1	— —	2.4 1.1	10.3 5.1	3.0 1.5	6.5 4.0	10 5.0	3.0 1.5	10.8 5.3	ns ns	
Propagation Delay Rise Time, Fall Time	t ₊₋ , t ₊₊ t ₊ , t ₋	S1 S1	F1 F1	A1, B1 A1, B1	2.5 1.0	10.7 5.4	3.0 1.5	6.5 3.0	10 5.0	3.0 1.5	10.8 5.4	ns ns	
Propagation Delay Rise Time, Fall Time	t ₋ , t ₊₋ t ₊ , t ₋	S1 S1	P _G P _G	A3, B3 A3, B3	1.7 0.8	8.3 5.1	2.0 1.1	6.0 3.0	8.0 5.0	2.0 1.1	8.4 5.2	ns ns	
Propagation Delay Rise Time, Fall Time	t ₊₋ , t ₊₊ t ₊ , t ₋	S1 S1	C _{n+4} C _{n+4}	A3, B3 A3, B3	1.6 0.9	9.3 5.3	2.0 1.1	6.0 3.0	9.0 5.0	2.0 1.0	9.9 5.2	ns ns	
Propagation Delay Rise Time, Fall Time	t ₊₋ , t ₊₊ t ₊ , t ₋	S1 S1	G _G G _G	A3, B3 A3, B3	1.5 0.8	9.6 6.2	2.0 0.8	6.0 3.0	9.0 6.0	1.9 0.8	9.7 6.5	ns ns	

† Logic high level (+1.11 Vdc) applied to pins listed. All other input pins are left floating or tied to +0.31 Vdc.
VCC1 = VCC2 = +2.0 Vdc, VEE = -3.2 Vdc

* L Suffix Only


OUTLINE DIMENSIONS

L SUFFIX
CERAMIC PACKAGE
CASE 623-05
ISSUE M



- NOTES:
- 1. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
 - 2. LEADS WITHIN 0.13 (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION (WHEN FORMED PARALLEL).

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	31.24	32.77	1.230	1.290
B	12.70	15.49	0.500	0.610
C	4.06	5.59	0.160	0.220
D	0.41	0.51	0.016	0.020
F	1.27	1.52	0.050	0.060
G	2.54 BSC		0.100 BSC	
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.27	0.020	0.050

Motorola reserves the right to make changes without further notice to any products herein. Motorola makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Motorola assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters which may be provided in Motorola data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. Motorola does not convey any license under its patent rights nor the rights of others. Motorola products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Motorola product could create a situation where personal injury or death may occur. Should Buyer purchase or use Motorola products for any such unintended or unauthorized application, Buyer shall indemnify and hold Motorola and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Motorola was negligent regarding the design or manufacture of the part. Motorola and  are registered trademarks of Motorola, Inc. Motorola, Inc. is an Equal Opportunity/Affirmative Action Employer.

How to reach us:
USA/EUROPE/Locations Not Listed: Motorola Literature Distribution;
P.O. Box 5405, Denver, Colorado 80217. 303-675-2140 or 1-800-441-2447

Mfax™: RMFAX0@email.sps.mot.com – TOUCHTONE 602-244-6609
INTERNET: <http://Design-NET.com>

JAPAN: Nippon Motorola Ltd.; Tatsumi-SPD-JLDC, 6F Seibu-Butsuryu-Center,
3-14-2 Tatsumi Koto-Ku, Tokyo 135, Japan. 81-3-3521-8315

ASIA/PACIFIC: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park,
51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852-26629298



This datasheet has been download from:

www.datasheetcatalog.com

Datasheets for electronics components.