

The screenshot displays a Verilog simulation waveform for a processor. The left pane lists various signals, and the right pane shows their values over time. A conflict is highlighted where two instructions use the same register (rs2) in the Decode stage.

Conflict Details:

- Instruction 1 (JAL):** PC = 80000024, ID = 3, RS2 = 2. It is decoded at time 7.
- Instruction 2 (ARITH JMM):** PC = 8000002C, ID = 3, RS2 = 3. It is decoded at time 111.

Both instructions use the same register (rs2) in the Decode stage, causing a conflict. The conflict is resolved by stalling the second instruction until the first instruction's writeback is complete.