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ФАКУЛЬТЕТ _____ «Информатика и системы управления»

КАФЕДРА _____ «Компьютерные системы и сети (ИУ6)»

НАПРАВЛЕНИЕ ПОДГОТОВКИ _____ «09.03.04 Программная инженерия»

ОТЧЕТ ПО ЛАБОРАТОРНОЙ РАБОТЕ №5
по курсу «Архитектура ЭВМ»

«Разработка ускорителей вычислений средствами САПР
высокоуровневого синтеза Xilinx Vitis HLS»

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Введение

Целью данной работы является изучение методики и технологии синтеза аппаратных устройств ускорения вычислений по описаниям на языках высокого уровня.

1 Основные теоретические сведения

2 Практическая часть

Листинг 2.1 – Программа варианта без оптимизаций

```
1 extern "C"
2 {
3     void var012_no_pragmas(int* c, const int* a, const int* b, const int len)
4     {
5         int ptr = 0;
6         for (int i = 0; i < len; i++)
7         {
8             ptr = b[i] % len;
9             c[i] = a[ptr] + i;
10        }
11    }
12 }
```

Листинг 2.2 – Программа варианта с конвейерной организацией

```
1 extern "C"
2 {
3     void var012_pipelined(int* c, const int* a, const int* b, const int len)
4     {
5         int ptr = 0;
6         for (int i = 0; i < len; i++)
7         {
8             #pragma HLS PIPELINE
9             ptr = b[i] % len;
10            c[i] = a[ptr] + i;
11        }
12    }
13 }
```

Листинг 2.3 – Программа варианта с разворачиванием цикла

```
1 extern "C"
2 {
3     void var012_unrolled(int* c, const int* a, const int* b, const int len)
4     {
5         int ptr = 0;
6         for (int i = 0; i < len; i++)
7         {
8             #pragma HLS UNROLL
9             ptr = b[i] % len;
10            c[i] = a[ptr] + i;

```

Листинг 2.3 (продолжение)

```
11     }  
12 }  
13 }
```

Листинг 2.4 – Программа варианта с конвейерной организацией и разворачиванием

```
1 extern "C"  
2 {  
3     void var012_pipe_unroll(int* c, const int* a, const int* b, const int len)  
4     {  
5         int ptr = 0;  
6         for (int i = 0; i < len; i++)  
7         {  
8             #pragma HLS DATAFLOW  
9             ptr = b[i] % len;  
10            c[i] = a[ptr] + i;  
11        }  
12    }  
13 }
```

Листинг 2.5 – Результаты Emulation-SW

```
1 [Console output redirected to file:/iu_home/iu7072/workspace/Alveo_lab2/  
   Emulation-SW/SystemDebugger_Alveo_lab2_system_Alveo_lab2.launch.log]  
2 Found Platform  
3 Platform Name: Xilinx  
4 INFO: Reading /iu_home/iu7072/workspace/Alveo_lab2_system/Emulation-SW/  
   binary_container_1.xclbin  
5 Loading: '/iu_home/iu7072/workspace/Alveo_lab2_system/Emulation-SW/  
   binary_container_1.xclbin'  
6 Trying to program device[0]: xilinx_u200_xdma_201830_2  
7 Device[0]: program successful!  
8 |-----+-----|  
9 | Kernel                | Wall-Clock Time (ns) |  
10 |-----+-----|  
11 | var012_no_pragmas      |                2070100 |  
12 |-----+-----|  
13 | var012_urolled         |                1262177 |  
14 |-----+-----|  
15 | var012_pipelined       |                438559 |  
16 |-----+-----|  
17 | var012_pipe_unroll     |                539648 |  
18 |-----+-----|  
19 Note: Wall Clock Time is meaningful for real hardware execution only, not for
```

Листинг 2.5 (продолжение)

```

    emulation.
20 Please refer to profile summary for kernel execution time for hardware emulation
    .
21 TEST PASSED.

```

| Name | Compute Units | Memory | SLR | Protocol Checker | Data Transfer | Execute Profiling | Stall Profiling |
|---------------------|---------------|--------|------|--------------------------|----------------------------|-------------------|--------------------------|
| binary_container_1 | | Auto | Auto | <input type="checkbox"/> | Default (Counters + Trace) | ✓ | <input type="checkbox"/> |
| var012_no_pragmas | 1 | Auto | Auto | <input type="checkbox"/> | Default (Counters + Trace) | ✓ | <input type="checkbox"/> |
| var012_no_pragmas_1 | | Auto | Auto | <input type="checkbox"/> | Default (Counters + Trace) | ✓ | <input type="checkbox"/> |
| c | | Auto | | <input type="checkbox"/> | Default (Counters + Trace) | ✓ | |
| a | | Auto | | <input type="checkbox"/> | Default (Counters + Trace) | ✓ | |
| b | | Auto | | <input type="checkbox"/> | Default (Counters + Trace) | ✓ | |
| len | | | | | | | |
| var012_pipelined | 1 | Auto | Auto | <input type="checkbox"/> | Default (Counters + Trace) | ✓ | <input type="checkbox"/> |
| var012_pipelined_1 | | Auto | Auto | <input type="checkbox"/> | Default (Counters + Trace) | ✓ | <input type="checkbox"/> |
| c | | Auto | | <input type="checkbox"/> | Default (Counters + Trace) | ✓ | |
| a | | Auto | | <input type="checkbox"/> | Default (Counters + Trace) | ✓ | |
| b | | Auto | | <input type="checkbox"/> | Default (Counters + Trace) | ✓ | |
| len | | | | | | | |

Рисунок 2.1 – Копия экрана Assistant View для Emulation-HW (часть 1)

| | | | | | | | |
|----------------------|---|------|------|--------------------------|----------------------------|---|--------------------------|
| var012_unrolled | 1 | Auto | Auto | <input type="checkbox"/> | Default (Counters + Trace) | ✓ | <input type="checkbox"/> |
| var012_unrolled_1 | | Auto | Auto | <input type="checkbox"/> | Default (Counters + Trace) | ✓ | <input type="checkbox"/> |
| c | | Auto | | <input type="checkbox"/> | Default (Counters + Trace) | ✓ | |
| a | | Auto | | <input type="checkbox"/> | Default (Counters + Trace) | ✓ | |
| b | | Auto | | <input type="checkbox"/> | Default (Counters + Trace) | ✓ | |
| len | | | | | | | |
| var012_pipe_unroll | 1 | Auto | Auto | <input type="checkbox"/> | Default (Counters + Trace) | ✓ | <input type="checkbox"/> |
| var012_pipe_unroll_1 | | Auto | Auto | <input type="checkbox"/> | Default (Counters + Trace) | ✓ | <input type="checkbox"/> |
| c | | Auto | | <input type="checkbox"/> | Default (Counters + Trace) | ✓ | |
| a | | Auto | | <input type="checkbox"/> | Default (Counters + Trace) | ✓ | |
| b | | Auto | | <input type="checkbox"/> | Default (Counters + Trace) | ✓ | |
| len | | | | | | | |

Рисунок 2.2 – Копия экрана Assistant View для Emulation-HW (часть 2)

Листинг 2.6 – Результаты Emulation-HW

```

1 [Console output redirected to file:/iu_home/iu7072/workspace/Alveo_lab2/
   Emulation-HW/SystemDebugger_Alveo_lab2_system_Alveo_lab2.launch.log]
2 Found Platform
3 Platform Name: Xilinx
4 INFO: Reading /iu_home/iu7072/workspace/Alveo_lab2_system/Emulation-HW/
   binary_container_1.xclbin
5 Loading: '/iu_home/iu7072/workspace/Alveo_lab2_system/Emulation-HW/
   binary_container_1.xclbin'
6 Trying to program device[0]: xilinx_u200_xdma_201830_2
7 INFO: [HW-EMU 01] Hardware emulation runs simulation underneath. Using a large
   data set will result in long simulation times. It is recommended that a small
   dataset is used for faster execution. The flow uses approximate models for
   DDR memory and interconnect and hence the performance data generated is
   approximate.
8 Device[0]: program successful!

```

Листинг 2.6 (продолжение)

```

9 |-----+-----|
10 | Kernel                | Wall-Clock Time (ns) |
11 |-----+-----|
12 | var012_no_pragmas      |          15008592508 |
13 |-----+-----|
14 INFO::[ Vitis-EM 22 ] [Time elapsed: 3 minute(s) 38 seconds, Emulation time:
    0.200175 ms]
15 Data transfer between kernel(s) and global memory(s)
16 var012_no_pragmas_1:m_axi_gmem-DDR[1]          RD = 8.000 KB          WR =
    4.000 KB
17 var012_pipe_unroll_1:m_axi_gmem-DDR[1]          RD = 0.000 KB          WR =
    0.000 KB
18 var012_pipelined_1:m_axi_gmem-DDR[1]            RD = 0.000 KB          WR =
    0.000 KB
19 var012_unrolled_1:m_axi_gmem-DDR[1]              RD = 0.301 KB          WR =
    0.125 KB
20
21 INFO::[ Vitis-EM 22 ] [Time elapsed: 8 minute(s) 39 seconds, Emulation time:
    0.466535 ms]
22 Data transfer between kernel(s) and global memory(s)
23 var012_no_pragmas_1:m_axi_gmem-DDR[1]          RD = 8.000 KB          WR =
    4.000 KB
24 var012_pipe_unroll_1:m_axi_gmem-DDR[1]          RD = 0.000 KB          WR =
    0.000 KB
25 var012_pipelined_1:m_axi_gmem-DDR[1]            RD = 0.000 KB          WR =
    0.000 KB
26 var012_unrolled_1:m_axi_gmem-DDR[1]              RD = 3.750 KB          WR =
    1.812 KB
27
28 INFO::[ Vitis-EM 22 ] [Time elapsed: 13 minute(s) 39 seconds, Emulation time:
    0.771576 ms]
29 Data transfer between kernel(s) and global memory(s)
30 var012_no_pragmas_1:m_axi_gmem-DDR[1]          RD = 8.000 KB          WR =
    4.000 KB
31 var012_pipe_unroll_1:m_axi_gmem-DDR[1]          RD = 0.000 KB          WR =
    0.000 KB
32 var012_pipelined_1:m_axi_gmem-DDR[1]            RD = 0.000 KB          WR =
    0.000 KB
33 var012_unrolled_1:m_axi_gmem-DDR[1]              RD = 7.699 KB          WR =
    3.812 KB
34
35 | var012_urolled        |          653277479951 |
36 |-----+-----|
37 | var012_pipelined      |          24012090705 |
38 |-----+-----|
39 INFO::[ Vitis-EM 22 ] [Time elapsed: 18 minute(s) 40 seconds, Emulation time:
    1.05055 ms]

```


Листинг 2.6 (продолжение)

```

40 Data transfer between kernel(s) and global memory(s)
41 var012_no_pragmas_1:m_axi_gmem-DDR[1]          RD = 8.000 KB          WR =
    4.000 KB
42 var012_pipe_unroll_1:m_axi_gmem-DDR[1]          RD = 2.270 KB          WR =
    1.133 KB
43 var012_pipelined_1:m_axi_gmem-DDR[1]            RD = 8.000 KB          WR =
    4.000 KB
44 var012_unrolled_1:m_axi_gmem-DDR[1]             RD = 8.000 KB          WR =
    4.000 KB
45
46 INFO::[ Vitis-EM 22 ] [Time elapsed: 23 minute(s) 40 seconds, Emulation time:
    1.25502 ms]
47 Data transfer between kernel(s) and global memory(s)
48 var012_no_pragmas_1:m_axi_gmem-DDR[1]          RD = 8.000 KB          WR =
    4.000 KB
49 var012_pipe_unroll_1:m_axi_gmem-DDR[1]          RD = 4.195 KB          WR =
    2.094 KB
50 var012_pipelined_1:m_axi_gmem-DDR[1]            RD = 8.000 KB          WR =
    4.000 KB
51 var012_unrolled_1:m_axi_gmem-DDR[1]             RD = 8.000 KB          WR =
    4.000 KB
52
53 INFO::[ Vitis-EM 22 ] [Time elapsed: 28 minute(s) 46 seconds, Emulation time:
    1.51806 ms]
54 Data transfer between kernel(s) and global memory(s)
55 var012_no_pragmas_1:m_axi_gmem-DDR[1]          RD = 8.000 KB          WR =
    4.000 KB
56 var012_pipe_unroll_1:m_axi_gmem-DDR[1]          RD = 6.672 KB          WR =
    3.332 KB
57 var012_pipelined_1:m_axi_gmem-DDR[1]            RD = 8.000 KB          WR =
    4.000 KB
58 var012_unrolled_1:m_axi_gmem-DDR[1]             RD = 8.000 KB          WR =
    4.000 KB
59
60 | var012_pipe_unroll          |          1028355914876 |
61 |-----+-----|
62 Note: Wall Clock Time is meaningful for real hardware execution only, not for
    emulation.
63 Please refer to profile summary for kernel execution time for hardware emulation
    .
64 TEST PASSED.
65 INFO::[ Vitis-EM 22 ] [Time elapsed: 33 minute(s) 46 seconds, Emulation time:
    1.73059 ms]
66 Data transfer between kernel(s) and global memory(s)
67 var012_no_pragmas_1:m_axi_gmem-DDR[1]          RD = 8.000 KB          WR =
    4.000 KB
68 var012_pipe_unroll_1:m_axi_gmem-DDR[1]          RD = 8.000 KB          WR =

```

Листинг 2.6 (продолжение)

```

    4.000 KB
69 var012_pipelined_1:m_axi_gmem-DDR[1]          RD = 8.000 KB          WR =
    4.000 KB
70 var012_unrolled_1:m_axi_gmem-DDR[1]          RD = 8.000 KB          WR =
    4.000 KB
71
72 INFO::[ Vitis-EM 22 ] [Time elapsed: 35 minute(s) 39 seconds, Emulation time:
    1.79479 ms]
73 Data transfer between kernel(s) and global memory(s)
74 var012_no_pragmas_1:m_axi_gmem-DDR[1]          RD = 8.000 KB          WR =
    4.000 KB
75 var012_pipe_unroll_1:m_axi_gmem-DDR[1]          RD = 8.000 KB          WR =
    4.000 KB
76 var012_pipelined_1:m_axi_gmem-DDR[1]          RD = 8.000 KB          WR =
    4.000 KB
77 var012_unrolled_1:m_axi_gmem-DDR[1]          RD = 8.000 KB          WR =
    4.000 KB
78
79 INFO: [HW-EMU 06-0] Waiting for the simulator process to exit

```

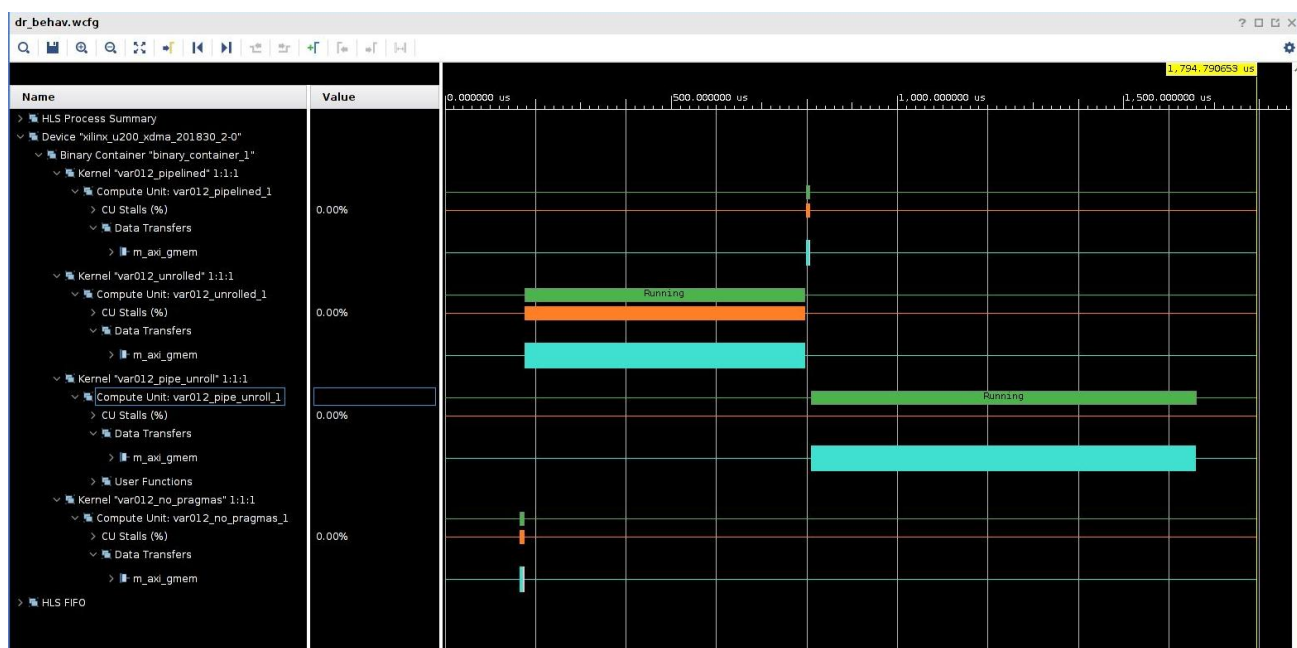


Рисунок 2.3 – Окно внутрисхемного отладчика Vivado для сборки в режиме Emulation-HW

Листинг 2.7 – Результаты Hardware

```

1 [Console output redirected to file:/iu_home/iu7072/workspace/Alveo_lab2/Hardware
  /SystemDebugger_Alveo_lab2_system_Alveo_lab2.launch.log]
2 Found Platform
3 Platform Name: Xilinx
4 INFO: Reading /iu_home/iu7072/workspace/Alveo_lab2_system/Hardware/
  binary_container_1.xclbin
5 Loading: '/iu_home/iu7072/workspace/Alveo_lab2_system/Hardware/
  binary_container_1.xclbin'
6 Trying to program device[0]: xilinx_u200_xdma_201830_2
7 Device[0]: program successful!
8 |-----+-----|
9 | Kernel                      | Wall-Clock Time (ns) |
10 |-----+-----|
11 | var012_no_pragmas           | 45233097              |
12 |-----+-----|
13 | var012_unrolled             | 662424184             |
14 |-----+-----|
15 | var012_pipelined            | 44303683              |
16 |-----+-----|
17 | var012_pipe_unroll          | 913769872             |
18 |-----+-----|
19 Note: Wall Clock Time is meaningful for real hardware execution only, not for
  emulation.
20 Please refer to profile summary for kernel execution time for hardware emulation
  .
21 TEST PASSED.

```

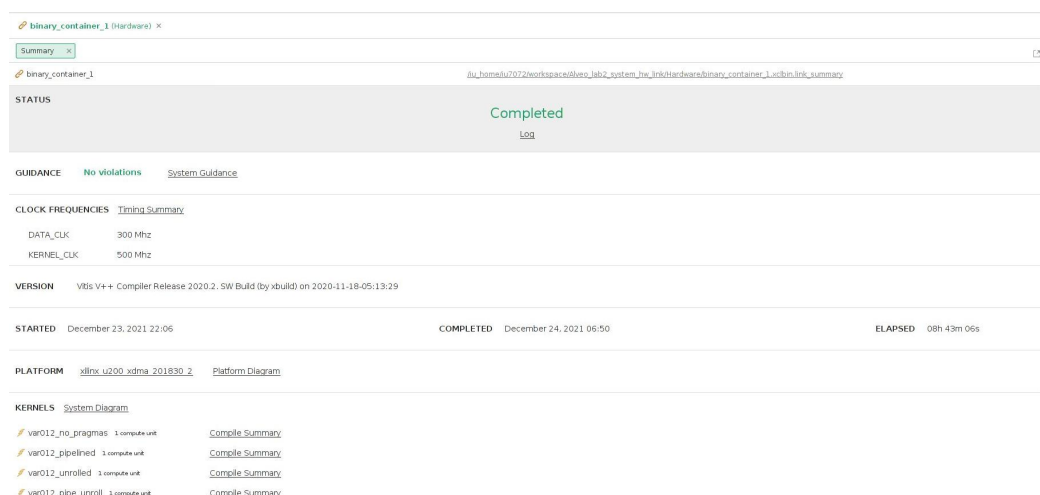


Рисунок 2.4 – Копия экрана вкладки Summary

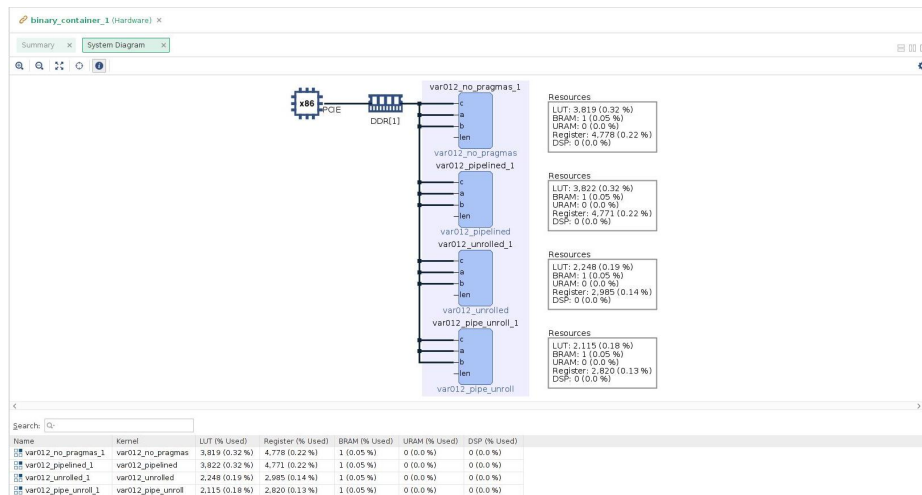


Рисунок 2.5 – Копия экрана вкладки System Diagram

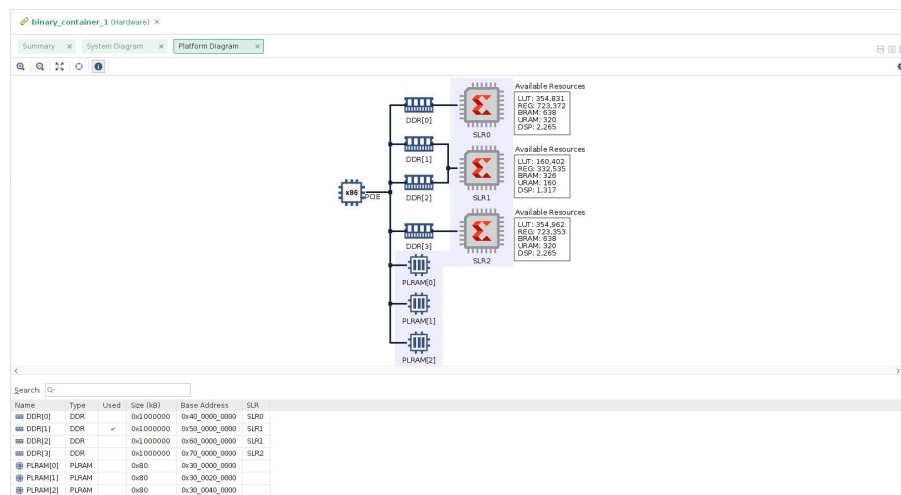


Рисунок 2.6 – Копия экрана вкладки Platform Diagram

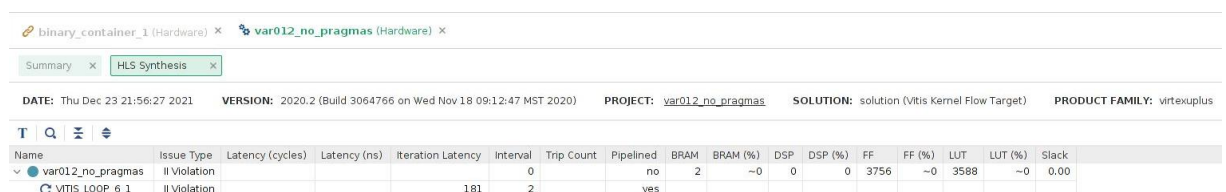


Рисунок 2.7 – Копия экрана вкладки HLSSynthesis (без прагм)



Рисунок 2.8 – Копия экрана вкладки HLSSynthesis (конвейер)

binary_container_1 (Hardware) ×

var012_no_pragmas (Hardware) ×

var012_pipelined (Hardware) ×

var012_unrolled (Hardware) ×

Summary ×

HLSSynthesis ×

DATE: Thu Dec 23 21:56:27 2021

VERSION: 2020.2 (Build 3064766 on Wed Nov 18 09:12:47 MST 2020)

PROJECT: var012_no_pragmas

SOLUTION: solution (Vitis Kernel Flow Target)

PRODUCT FAMILY: virtexuplus

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| Name | Issue Type | Latency (cycles) | Latency (ns) | Iteration Latency | Interval | Trip Count | Pipelined | BRAM | BRAM (%) | DSP | DSP (%) | FF | FF (%) | LUT | LUT (%) | Slack |
|-------------------|--------------|------------------|--------------|-------------------|----------|------------|-----------|------|----------|-----|---------|------|--------|------|---------|-------|
| var012_no_pragmas | II Violation | | | | 0 | | no | 2 | ~0 | 0 | 0 | 3756 | ~0 | 3588 | ~0 | 0.00 |
| VITIS_LOOP_6_1 | II Violation | | | 181 | 2 | | yes | | | | | | | | | |

Рисунок 2.9 – Копия экрана вкладки HLSSynthesis (разворачивание)

binary_container_1 (Hardware) ×

var012_no_pragmas (Hardware) ×

var012_pipelined (Hardware) ×

var012_unrolled (Hardware) ×

var012_pipe_unroll (Hardware) ×

Summary ×

HLSSynthesis ×

DATE: Thu Dec 23 21:56:59 2021

VERSION: 2020.2 (Build 3064766 on Wed Nov 18 09:12:47 MST 2020)

PROJECT: var012_pipe_unroll

SOLUTION: solution (Vitis Kernel Flow Target)

PRODUCT FAMILY: virtexuplus

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| Name | Issue Type | Latency (cycles) | Latency (ns) | Iteration Latency | Interval | Trip Count | Pipelined | BRAM | BRAM (%) | DSP | DSP (%) | FF | FF (%) | LUT | LUT (%) | Slack |
|---------------------------------|------------|------------------|--------------|-------------------|----------|------------|-----------|------|----------|-----|---------|------|--------|------|---------|-------|
| var012_pipe_unroll | | | | | | | no | 2 | ~0 | 0 | 0 | 2239 | ~0 | 3079 | ~0 | 0.00 |
| dataflow_in_loop_Vitis_LOOP_6_1 | | 248 | 827.000 | | | 249 | dataflow | 0 | 0 | 0 | 0 | 932 | ~0 | 1891 | ~0 | 0.00 |
| Block_entry_proc_proc | | 248 | 827.000 | | | 248 | no | 0 | 0 | 0 | 0 | 932 | ~0 | 1891 | ~0 | 0.00 |
| Vitis_LOOP_6_1 | | | | | | | no | | | | | | | | | |

Рисунок 2.10 – Копия экрана вкладки HLSSynthesis (конвейер + разворачивание)

3 Контрольные вопросы

Заключение