

tb/ext\_reset  
tb/sys\_clk  
tb/cyc\_cnt  
tb/uut/cpu/id\_block/decode  
id  
pc  
instruction  
valid  
addr\_valid  
tb/uut/cpu/id\_block/decode\_advance  
Decode  
tb/uut/cpu/decode\_and\_issue\_block/issue\_stage\_ready  
tb/uut/cpu/decode\_and\_issue\_block/issue\_ready  
tb/uut/cpu/decode\_and\_issue\_block/rs1\_conflict  
tb/uut/cpu/decode\_and\_issue\_block/rs2\_conflict  
tb/uut/cpu/decode\_and\_issue\_block/issue.instruction  
tb/uut/cpu/decode\_and\_issue\_block/issue  
pc  
instruction  
fn3  
opcode  
rs\_addr  
[1]  
[0]  
rd\_addr  
uses\_rs1  
uses\_rs2  
uses\_rd  
id  
stage\_valid  
addr\_valid  
tb/uut/cpu/decode\_and\_issue\_block/alu\_inputs  
tb/uut/cpu/decode\_and\_issue\_block/unit\_issue[0]/new\_request  
tb/uut/cpu/decode\_and\_issue\_block/unit\_issue[0]/id  
tb/uut/cpu/decode\_and\_issue\_block/ls\_inputs  
tb/uut/cpu/decode\_and\_issue\_block/unit\_issue[1]/new\_request

0					
0					
30	33	34	35	36	37
0 80...	1 80000014 0040a103...	2 80000018 002f8fb3 1 1	3 8000001c 0080a103 1 1		4 80000020 002f8fb3 1 1
0	1	2	3		4
8000...	80000014	80000018	8000001C		80000020
002F...	0040A103	002F8FB3	0080A103		002F8FB3
1					
1					
St1					
1					
0010	0001	0010	0001		0010
0					
0					
000...	002F8FB3	0040A103	002F8FB3		0080A103
8000...	80000010 002f8fb3 0 ...	80000014 0040a103 2 LOAD {...	80000018 002f8fb3 0 ARITH {02 1f} 1f 1 1 1 2 1 1		8000001c 0080a103 2 LOAD {...
8000...	80000010	80000014	80000018		8000001C
000...	002F8FB3	0040A103	002F8FB3		0080A103
2	0	2	0		2
LOAD	ARITH	LOAD	ARITH		LOAD
00 01	02 1f	04 01	02 1f		08 01
00	02	04	02		08
01	1F	01	1F		01
02	1F	02	1F		02
1					
0					
1					
7	0	1	2		3
1					
1					
1800...	00000000a 00000000...	180000050 00000000 80000...	00000000f 000000005 0000000f 05 0 0 1 ALU LOGIC ADD 0 0	00000000f 000000006 00000...	180000050 00000000 80000...
0					
7	0	1	2		3
8000...	0000000a 00000005 0...	80000050 00000000 004 2 1 0...	0000000f 00000005 01f 0 0 0 1 1 {0 0 0 00}	0000000f 00000006 01f 0 0 0 ...	80000050 00000000 008 2 1 0...
1					