≨ 1 ←	Msgs					
√ /tb/sys_dk	1					
 - <mark>/</mark> /tb/cyc_cnt	13	7	[8	(9	10	[11
 _ / tb/uut/cpu/id_block/decode	1800	(4 80000010 0040a183 1 1	5 80000014 002f8fb3 1 1	6 80000018 003f8fb3 1 1		7 8000001c 0080a203 1 1
/tb/uut/cpu/id_block/decode_advance	St1		Decode,	1	Execution,	
Dispatch			pc=80000014,id=5		pc=8000014, id=5	
/tb/uut/cpu/decode_and_issue_block/issue_stage_ready	1					
📭 🥠 /tb/uut/cpu/decode_and_issue_block/issue_ready	0010	0010		0001		
/tb/uut/cpu/decode_and_issue_block/rs1_conflict	0					
/tb/uut/cpu/decode_and_issue_block/rs2_conflict	0			88		
=-4, /tb/uut/cpu/decode_and_issue_block/issue	80000	, 8000000c 0000a 103 2 LOAD {00	80000010 0040a183 2 LOAD {04	. 🖁 80000014 002f8fb3 0 ARITH {02 1f	f} 1f 1 1 1 5 1 1	, 80000018 003f8fb3 0 ARITH {03 }
i - ∕ pc	80000	, 8000000C	80000010	80000014		80000018
- / instruction	00C0	,0000A103	0040A183	,002F8FB3		,003F8FB3
	2	.2		(o		
— ∜ opcode		LOAD		ARITH		
	0c 01	00 01	0401	02 1f		03 1f
	0C	00	04	02		03
<u> </u>	01	01		, 1F		
	05	02	03	Į IF		
— ✓ uses_rs1	1	2.00				
— ✓ uses_rs2	0	(* <u>*</u>	P	A1		
—∳ uses_rd	1					
	0	3	[4	.5		[6
	1					
└	1		\			
— ALU						
+- / /tb/uut/cpu/decode_and_issue_block/alu_inputs.in1	18000	18000003C	\\	1000000000		000000001
+ /tb/uut/cpu/decode_and_issue_block/alu_inputs.in2	00000	000000000			000000001	(000000002
/tb/uut/cpu/decode_and_issue_block/alu_inputs.logic_op	ALU	ALU LOGIC ADD				
/tb/uut/cpu/decode_and_issue_block/unit_issue[0]/new_request	0					
// /tb/uut/cpu/decode_and_issue_block/unit_issue[0]/id	0	13	4	5		16
** /tb/uut/cpu/register_file_and_writeback_block/unit_wb[0]/id	0	3	4	5		6
/tb/uut/cpu/register_file_and_writeback_block/unit_wb[0]/done	0					
/tb/uut/cpu/register_file_and_writeback_block/unit_wb[0]/rd	00000	00000001		(00000000	00000001	00000003
→ /tb/register_file[31] → /tb/register_file[31]	00000	00000000				00000001