Министерство науки и высшего образования Российской Федерации
Федеральное государственное бюджетное образовательное учреждение высшего образования
«Московский государственный технический университет имени Н.Э. Баумана
(национальный исследовательский университет)»
(МГТУ им. Н.Э. Баумана)

ФАКУЛЬТЕТ «Информатика и системы управления»

КАФЕДРА «Компьютерные системы и сети (ИУ6)»

НАПРАВЛЕНИЕ ПОДГОТОВКИ «09.03.04 Программная инженерия»

ОТЧЕТ ПО ЛАБОРАТОРНОЙ РАБОТЕ №5
по курсу «Архитектура ЭВМ»

«Разработка ускорителей вычислений средствами САПР высокоуровневого синтеза Xilinx Vitis HLS»

Студент: ИУ7-53Б _____ М. Д. Маслова
(группа) (подпись, дата) (И. О. Фамилия)

Преподаватель: _____ Е. Н. Дубровин
(подпись, дата) (И. О. Фамилия)

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Содержание

Введение

Целью данной работы является изучение методики и технологии синтеза аппаратных устройств ускорения вычислений по описаниям на языках высокого уровня.

1 Основные теоретические сведения

2 Практическая часть

Листинг 2.1 – Программа варианта без оптимизаций

```
extern "C"
{
    void var012_no_pragmas(int* c, const int* a, const int* b, const int len)
    {
        int ptr = 0;
        for (int i = 0; i < len; i++)
        {
            ptr = b[i] % len;
            c[i] = a[ptr] + i;
        }
    }
}
```

Листинг 2.2 – Программа варианта с конвейерной организацией

```
extern "C"
{
    void var012_pipelined(int* c, const int* a, const int* b, const int len)
    {
        int ptr = 0;
        for (int i = 0; i < len; i++)
        {
            #pragma HLS PIPELINE
            ptr = b[i] % len;
            c[i] = a[ptr] + i;
        }
    }
}
```

Листинг 2.3 – Программа варианта с разворачиванием цикла

```
extern "C"
{
    void var012_unrolled(int* c, const int* a, const int* b, const int len)
    {
        int ptr = 0;
        for (int i = 0; i < len; i++)
        {
            #pragma HLS UNROLL
            ptr = b[i] % len;
            c[i] = a[ptr] + i;
```

Листинг 2.3 (продолжение)

```
        }
    }
}
```

Листинг 2.4 – Программа варианта с конвейерной организацией и разворачиванием

```
extern "C"
{
    void var012_pipe_unroll(int* c, const int* a, const int* b, const int len)
    {
        int ptr = 0;
        for (int i = 0; i < len; i++)
        {
            #pragma HLS DATAFLOW
            ptr = b[i] % len;
            c[i] = a[ptr] + i;
        }
    }
}
```

Листинг 2.5 – Результаты Emulation-SW

```
[Console output redirected to file:/iu_home/iu7072/workspace/Alveo_lab2/
   Emulation-SW/SystemDebugger_Alveo_lab2_system_Alveo_lab2.launch.log]
Found Platform
Platform Name: Xilinx
INFO: Reading /iu_home/iu7072/workspace/Alveo_lab2_system/Emulation-SW/
   binary_container_1.xclbin
Loading: '/iu_home/iu7072/workspace/Alveo_lab2_system/Emulation-SW/
   binary_container_1.xclbin'
Trying to program device[0]: xilinx_u200_xdma_201830_2
Device[0]: program successful!
|-------------------------+-------------------------|
| Kernel                  |    Wall-Clock Time (ns) |
|-------------------------+-------------------------|
| var012_no_pragmas       |                 2070100 |
|-------------------------+-------------------------|
| var012_urolled          |                 1262177 |
|-------------------------+-------------------------|
| var012_pipelined        |                  438559 |
|-------------------------+-------------------------|
| var012_pipe_unroll      |                  539648 |
|-------------------------+-------------------------|
Note: Wall Clock Time is meaningful for real hardware execution only, not for
```

Листинг 2.5 (продолжение)

```
    emulation.
20 Please refer to profile summary for kernel execution time for hardware emulation
    .
21 TEST PASSED.
```

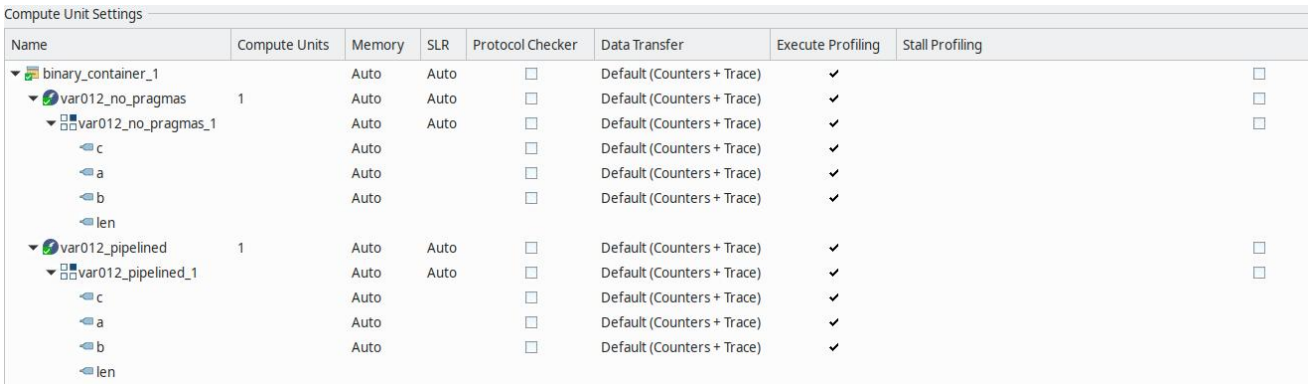

Рисунок 2.1 – Копия экрана Assistant View для Emulation-HW (часть 1)

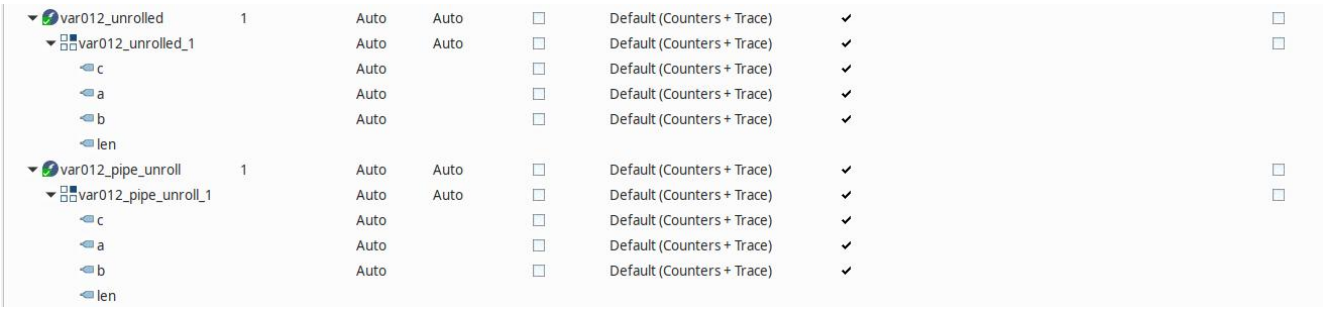

Рисунок 2.2 – Копия экрана Assistant View для Emulation-HW (часть 2)

Листинг 2.6 – Результаты Emulation-HW

```
1 [Console output redirected to file:/iu_home/iu7072/workspace/Alveo_lab2/
    Emulation-HW/SystemDebugger_Alveo_lab2_system_Alveo_lab2.launch.log]
2 Found Platform
3 Platform Name: Xilinx
4 INFO: Reading /iu_home/iu7072/workspace/Alveo_lab2_system/Emulation-HW/
    binary_container_1.xclbin
5 Loading: '/iu_home/iu7072/workspace/Alveo_lab2_system/Emulation-HW/
    binary_container_1.xclbin'
6 Trying to program device[0]: xilinx_u200_xdma_201830_2
7 INFO: [HW-EMU 01] Hardware emulation runs simulation underneath. Using a large
    data set will result in long simulation times. It is recommended that a small
     dataset is used for faster execution. The flow uses approximate models for
    DDR memory and interconnect and hence the performance data generated is
    approximate.
8 Device[0]: program successful!
```

Листинг 2.6 (продолжение)

```
|-------------------------+-------------------------|
| Kernel                  |    Wall-Clock Time (ns) |
|-------------------------+-------------------------|
| var012_no_pragmas       |             15008592508 |
|-------------------------+-------------------------|
INFO::[ Vitis-EM 22 ] [Time elapsed: 3 minute(s) 38 seconds, Emulation time:
    0.200175 ms]
Data transfer between kernel(s) and global memory(s)
var012_no_pragmas_1:m_axi_gmem-DDR[1]          RD = 8.000 KB               WR =
    4.000 KB
var012_pipe_unroll_1:m_axi_gmem-DDR[1]          RD = 0.000 KB               WR =
     0.000 KB
var012_pipelined_1:m_axi_gmem-DDR[1]          RD = 0.000 KB               WR =
    0.000 KB
var012_unrolled_1:m_axi_gmem-DDR[1]          RD = 0.301 KB               WR =
    0.125 KB

INFO::[ Vitis-EM 22 ] [Time elapsed: 8 minute(s) 39 seconds, Emulation time:
    0.466535 ms]
Data transfer between kernel(s) and global memory(s)
var012_no_pragmas_1:m_axi_gmem-DDR[1]          RD = 8.000 KB               WR =
    4.000 KB
var012_pipe_unroll_1:m_axi_gmem-DDR[1]          RD = 0.000 KB               WR =
     0.000 KB
var012_pipelined_1:m_axi_gmem-DDR[1]          RD = 0.000 KB               WR =
    0.000 KB
var012_unrolled_1:m_axi_gmem-DDR[1]          RD = 3.750 KB               WR =
    1.812 KB

INFO::[ Vitis-EM 22 ] [Time elapsed: 13 minute(s) 39 seconds, Emulation time:
    0.771576 ms]
Data transfer between kernel(s) and global memory(s)
var012_no_pragmas_1:m_axi_gmem-DDR[1]          RD = 8.000 KB               WR =
    4.000 KB
var012_pipe_unroll_1:m_axi_gmem-DDR[1]          RD = 0.000 KB               WR =
     0.000 KB
var012_pipelined_1:m_axi_gmem-DDR[1]          RD = 0.000 KB               WR =
    0.000 KB
var012_unrolled_1:m_axi_gmem-DDR[1]          RD = 7.699 KB               WR =
    3.812 KB

| var012_urolled          |            653277479951 |
|-------------------------+-------------------------|
| var012_pipelined        |             24012090705 |
|-------------------------+-------------------------|
INFO::[ Vitis-EM 22 ] [Time elapsed: 18 minute(s) 40 seconds, Emulation time:
    1.05055 ms]
```

Листинг 2.6 (продолжение)

```
Data transfer between kernel(s) and global memory(s)
var012_no_pragmas_1:m_axi_gmem-DDR[1]          RD = 8.000 KB               WR =
    4.000 KB
var012_pipe_unroll_1:m_axi_gmem-DDR[1]          RD = 2.270 KB               WR =
     1.133 KB
var012_pipelined_1:m_axi_gmem-DDR[1]          RD = 8.000 KB               WR =
    4.000 KB
var012_unrolled_1:m_axi_gmem-DDR[1]          RD = 8.000 KB               WR =
    4.000 KB

INFO::[ Vitis-EM 22 ] [Time elapsed: 23 minute(s) 40 seconds, Emulation time:
    1.25502 ms]
Data transfer between kernel(s) and global memory(s)
var012_no_pragmas_1:m_axi_gmem-DDR[1]          RD = 8.000 KB               WR =
    4.000 KB
var012_pipe_unroll_1:m_axi_gmem-DDR[1]          RD = 4.195 KB               WR =
     2.094 KB
var012_pipelined_1:m_axi_gmem-DDR[1]          RD = 8.000 KB               WR =
    4.000 KB
var012_unrolled_1:m_axi_gmem-DDR[1]          RD = 8.000 KB               WR =
    4.000 KB

INFO::[ Vitis-EM 22 ] [Time elapsed: 28 minute(s) 46 seconds, Emulation time:
    1.51806 ms]
Data transfer between kernel(s) and global memory(s)
var012_no_pragmas_1:m_axi_gmem-DDR[1]          RD = 8.000 KB               WR =
    4.000 KB
var012_pipe_unroll_1:m_axi_gmem-DDR[1]          RD = 6.672 KB               WR =
     3.332 KB
var012_pipelined_1:m_axi_gmem-DDR[1]          RD = 8.000 KB               WR =
    4.000 KB
var012_unrolled_1:m_axi_gmem-DDR[1]          RD = 8.000 KB               WR =
    4.000 KB

| var012_pipe_unroll      |          1028355914876 |
|-------------------------+------------------------|
Note: Wall Clock Time is meaningful for real hardware execution only, not for
    emulation.
Please refer to profile summary for kernel execution time for hardware emulation
    .
TEST PASSED.
INFO::[ Vitis-EM 22 ] [Time elapsed: 33 minute(s) 46 seconds, Emulation time:
    1.73059 ms]
Data transfer between kernel(s) and global memory(s)
var012_no_pragmas_1:m_axi_gmem-DDR[1]          RD = 8.000 KB               WR =
    4.000 KB
var012_pipe_unroll_1:m_axi_gmem-DDR[1]          RD = 8.000 KB               WR =
```

Листинг 2.6 (продолжение)

```
    4.000 KB
69 var012_pipelined_1:m_axi_gmem-DDR[1]          RD = 8.000 KB                WR =
    4.000 KB
70 var012_unrolled_1:m_axi_gmem-DDR[1]          RD = 8.000 KB                WR =
    4.000 KB
71
72 INFO::[ Vitis-EM 22 ] [Time elapsed: 35 minute(s) 39 seconds, Emulation time:
    1.79479 ms]
73 Data transfer between kernel(s) and global memory(s)
74 var012_no_pragmas_1:m_axi_gmem-DDR[1]          RD = 8.000 KB                WR =
    4.000 KB
75 var012_pipe_unroll_1:m_axi_gmem-DDR[1]          RD = 8.000 KB                WR =
    4.000 KB
76 var012_pipelined_1:m_axi_gmem-DDR[1]          RD = 8.000 KB                WR =
    4.000 KB
77 var012_unrolled_1:m_axi_gmem-DDR[1]          RD = 8.000 KB                WR =
    4.000 KB
78
79 INFO: [HW-EMU 06-0] Waiting for the simulator process to exit
```

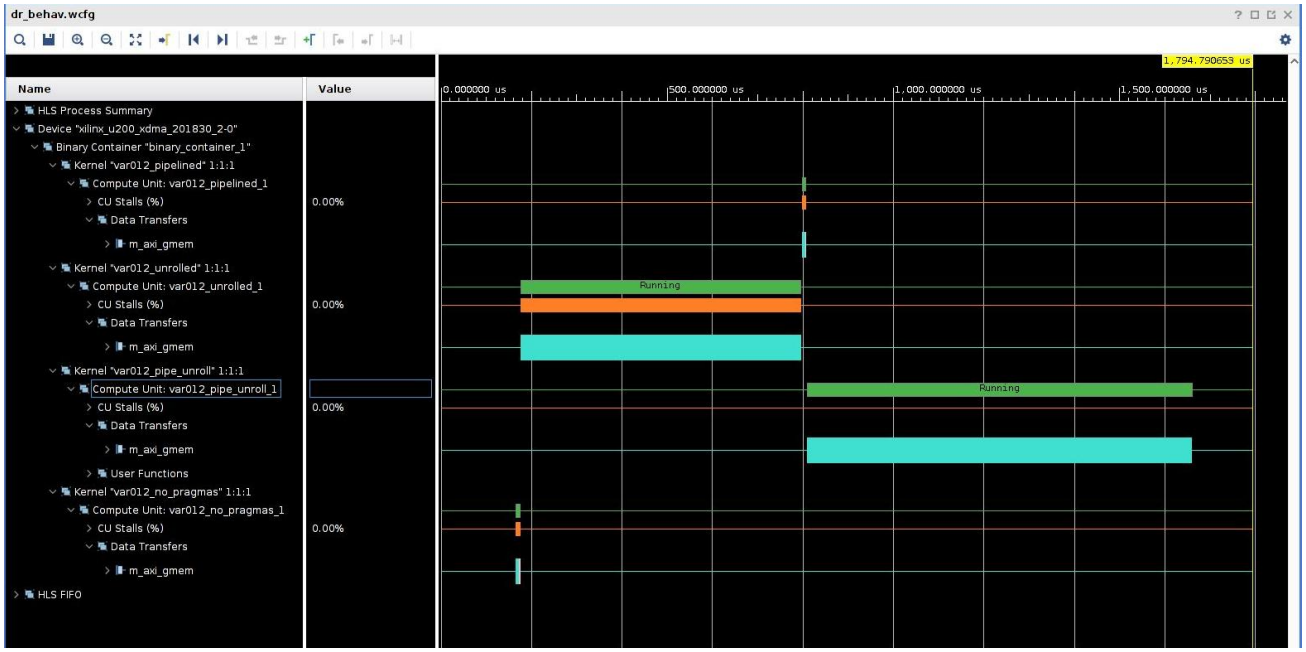

Рисунок 2.3 – Окно внутрисхемного отладчика Vivado для сборки в режиме Emulation-HW

Листинг 2.7 – Результаты Hardware

```
[Console output redirected to file:/iu_home/iu7072/workspace/Alveo_lab2/Hardware
    /SystemDebugger_Alveo_lab2_system_Alveo_lab2.launch.log]
Found Platform
Platform Name: Xilinx
INFO: Reading /iu_home/iu7072/workspace/Alveo_lab2_system/Hardware/
    binary_container_1.xclbin
Loading: '/iu_home/iu7072/workspace/Alveo_lab2_system/Hardware/
    binary_container_1.xclbin'
Trying to program device[0]: xilinx_u200_xdma_201830_2
Device[0]: program successful!
|-------------------------+-------------------------|
| Kernel                  |    Wall-Clock Time (ns) |
|-------------------------+-------------------------|
| var012_no_pragmas       |                45233097 |
|-------------------------+-------------------------|
| var012_urolled          |               662424184 |
|-------------------------+-------------------------|
| var012_pipelined        |                44303683 |
|-------------------------+-------------------------|
| var012_pipe_unroll      |               913769872 |
|-------------------------+-------------------------|
Note: Wall Clock Time is meaningful for real hardware execution only, not for
    emulation.
Please refer to profile summary for kernel execution time for hardware emulation
    .
TEST PASSED.
```

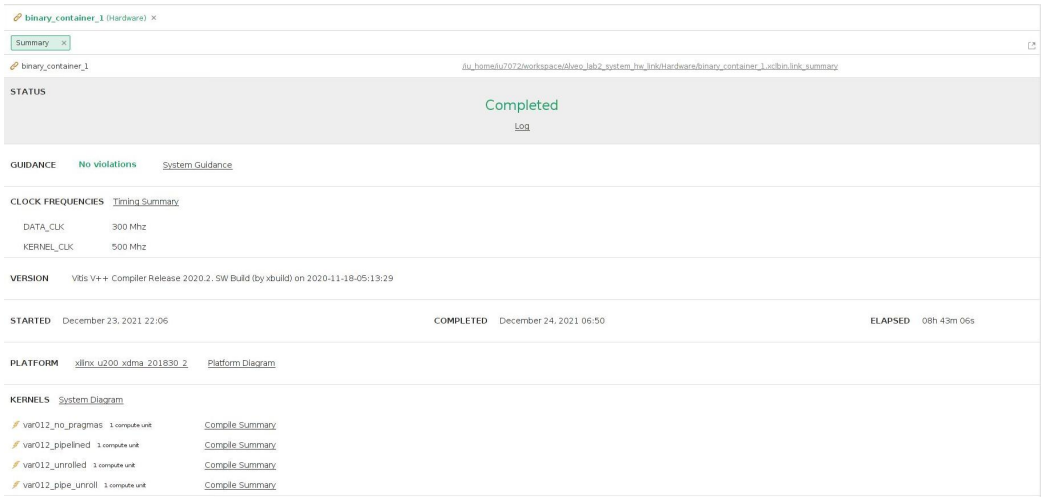

Рисунок 2.4 – Копия экрана вкладки Summary

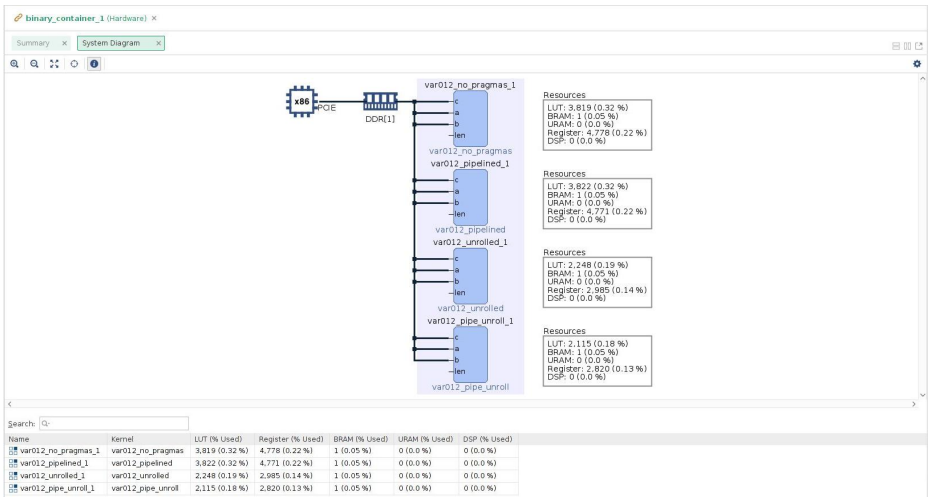

Рисунок 2.5 – Копия экрана вкладки System Diagram

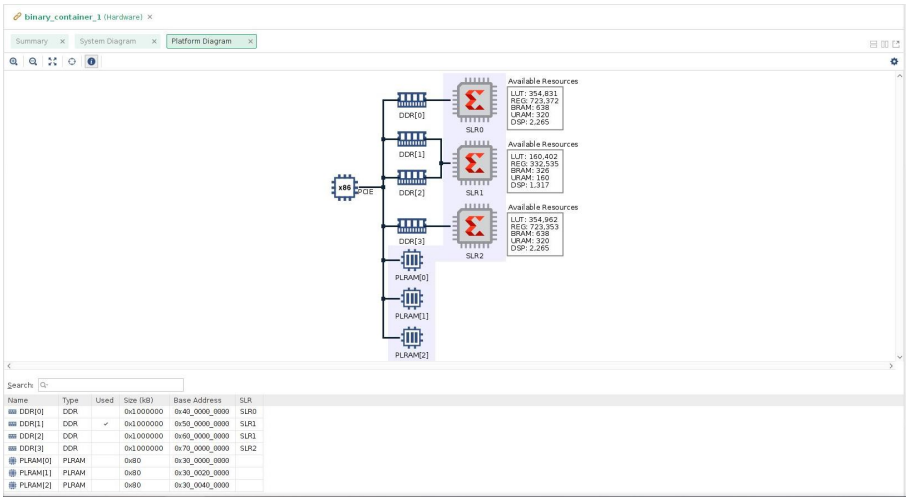

Рисунок 2.6 – Копия экрана вкладки Platform Diagram

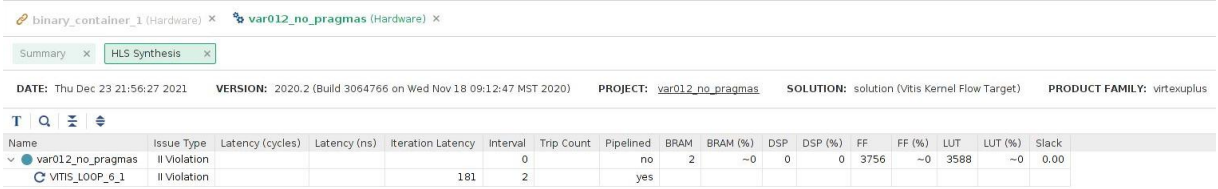

Рисунок 2.7 – Копия экрана вкладки HLSSynthesis (без прагм)

Рисунок 2.8 – Копия экрана вкладки HLSSynthesis (конвейер)

Рисунок 2.9 – Копия экрана вкладки HLSSynthesis (разворачивание)

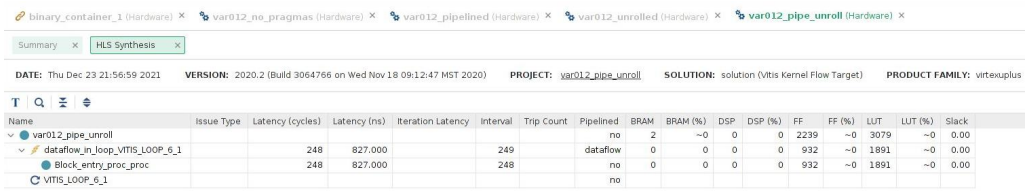

Рисунок 2.10 – Копия экрана вкладки HLSSynthesis (конвейер + разворачивание)

3 Контрольные вопросы

Заключение