EEM216A Design of VLSI Circuits and Systems **Fall 2021**

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Lab #2

Due: Wednesday Nov 17 at 4pm

The goal of this lab is to introduce you to the Synopsys synthesis, timing, and power analysis tools. The lab also covers how to do a gate-level simulation in ModelSim for your synthesized design. In this lab, we will be synthesizing the ALU from HW2, and analyzing its timing and power. To begin, you will need to source the included setup file:

```
$tcsh
$source tool-setup
```

Included files: alu.v, alu_tb.v, saed32nm.v, lab2_synthesis.tcl, lab2_prime.tcl, tool-setup

Part 1: Synthesis

To synthesize the ALU, run Synopsys Design Compiler:

```
$dc_shell -f lab2_synthesis.tcl
```

It will generate the gate-level netlist (alu.vg) and a standard delay format file (alu.sdf), which you will need to do a gate-level accurate simulation in ModelSim. Also created is alu.sdc, which we will need for place and route (which we are not doing in this lab). Finally, several reports are generated, covering power, area, and timing. Using these reports, fill in the following tables.

Report the synthesized design area here:

Combinational	Buf/Inv	Non-combinational	Net Interconnect
681.105919	16.773504	249.061124	165.833152

Report the synthesized design power here:

Switch Power	Int. Power	Leak Power	Total Power
4.466	31.574	1.63e+09	1.67e+03

Report the slack from the 5 worst hold times here:

Path #1	Path #2	Path #3	Path #4	Path #5
0.0	0.0	0.04	0.04	0.04

Report the slack from the 5 worst setup times here:

Path #1	Path #2	Path #3	Path #4	Path #5
7.25	7.25	7.25	7.25	7.25

Part 2: PrimeTime/PrimePower

To check the timing of the ALU, run Synopsys PrimeTime/PrimePower:

```
$pt_shell -file lab2_prime.tcl
```

The PrimePower of the script file has been commented out for now. We will need to run a gate-level ModelSim simulation to generate alu.vcd, a switching activity file, before we can run the PrimePower portion. For now, fill out the following table for PrimeTime.

Report the timing slack for the 2 paths reported by PrimeTime:

Path #1	Path #2
6.33	6.36

To generate alu.vcd, you will need to run alu_tb.v in ModelSim. Create a new project with alu_tb.v, alu.vg (created by synthesis), and the included verilog technology file: saed32nm.v. Run the testbench for $10\mu s$ to create a switching activity file. Now open lab2_prime.tcl and uncomment the PrimePower sections. You will also need to add some code to the script to set the power analysis mode. For this lab, we will only look at the average power. Save and rerun the script. Please fill out the following table for each ALU operation's power. 000 (addition) has been provided so that you can verify your work. Please generate a switching activity file of only $10\mu s$ for each operation when calculating the power.

The line(s) of code added to lab2_prime.tcl for PrimePower:

```
set power_analysis_mode averaged
```

Report the design power for each ALU operation here:

ALU Operation	Switching Power	Int. Power	Leak Power	Total Power
000	$\mathbf{2.445\mu W}$	$\mathbf{35.56\mu W}$	$\mathbf{90.50\mu W}$	$\mathbf{129\mu W}$
001	2.473 uW	35.86 uW	90.33 uW	128.7 uW
010	2.415 uW	35.38 uW	91.15 uW	128.9 uW
011	2.398 uW	35.35 uW	83.83 uW	121.6 uW
100	2.576 uW	36.43 uW	90.97 uW	130 uW
101	2.468 uW	35.53 uW	83.38 uW	121.4 uW
110	2.434 uW	35.99 uW	90.23 uW	128.7 uW