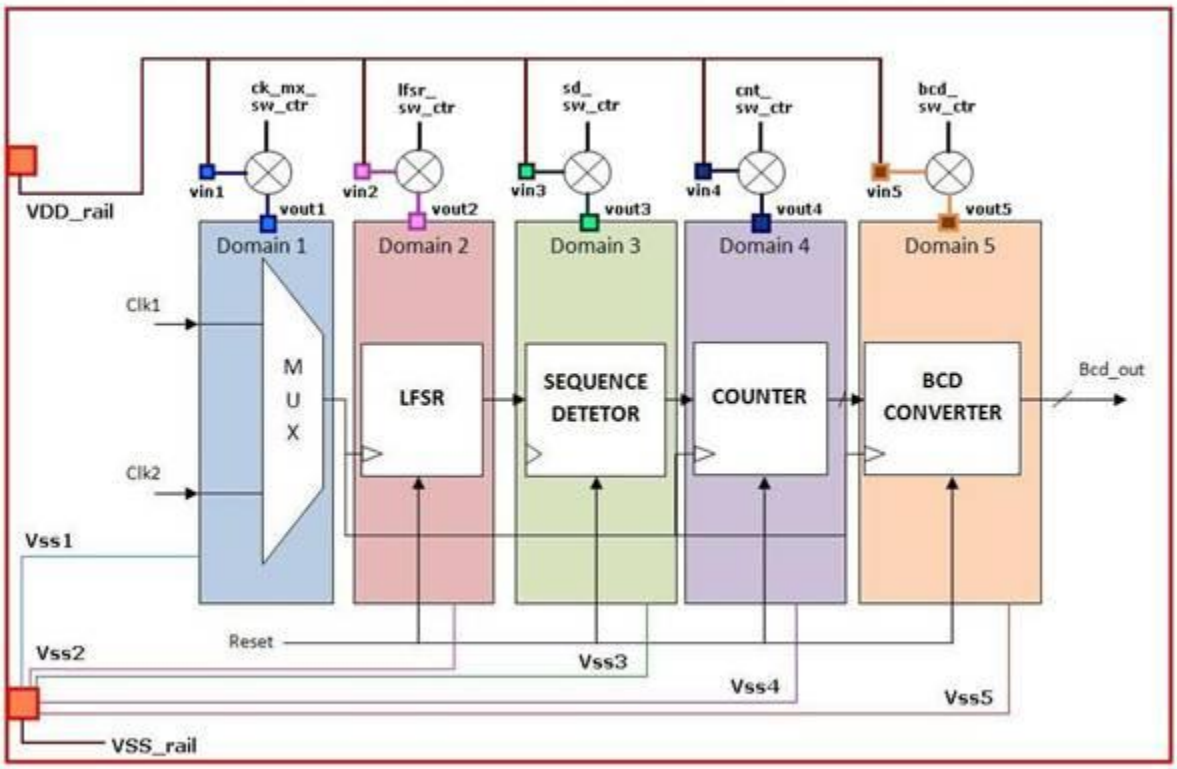
EEM216A Design of VLSI Circuits and Systems **Fall 2021**

Prof. Dejan Marković Lab #3

Myles Johnson
205868607

Due: Wednesday, Dec 1 at 4pm

The goal of this lab is to introduce you to the Unified Power Format, which is used to specify multiple clock and power domains, as well as power and clock gating. This lab will cover the basics of simulating and synthesizing a design with multiple power domains for power gating. Below is a power plan of the design we will be working with.



To begin, you will need to source the included setup file (different from your tool-setup file you usually use):

```
tcsh
source tool-setup
```

Included files: lab3_tb.sv, lab3.upf, top.v, 1_clk_mux.v, 2_lfsr.v, 3_seqdet.v, 4_counter.v, 5_bcd_convert.v, lab3_synthesis.tcl, tool-setup

Part 1: Simulating UPF in ModelSim

The Verilog-2001 standard was created before the UPF format, so it does not support it. However, SystemVerilog is an extension of Verilog-2001 and does support UPF. The testbench (lab3_tb.sv) is written in SystemVerilog (as a reference for you) and does not need to be modified. However, before you can simulate it you will need to complete lab3.upf.

Your first task is to create the power switch for the Counter (power domain 4). You should use the other power switches in lab3.upf as a guideline.
Hint: I found this website is extremely helpful for the upf
https://vlsitutorials.com/upf-low-power-vlsi/

The line(s) of code added to lab3.upf for power switch:

```
create_power_switch cnt_SW \
 -domain Domain_4 \
 -input_supply_port  {vin4     VDD} \
 -output_supply_port {vout4    Vcnt} \
 -control_port       {ctr_sig4 cnt_sw_ctr} \
 -on_state           {CNT_ON vin4 {!ctr_sig4}} \
 -off_state          {CNT_OFF   {ctr_sig4}}
```

Your second task is to create the isolation strategy for the Counter (power domain 4). You should use the other isolation strategies in lab3.upf as a guideline. Note that the "isolation control" and "isolation cells" are different in power domain 4.

The line(s) of code added to lab3.upf for isolation:

```
set_isolation iso_strategy4 \
-domain Domain_4 \
-isolation_power_net VDD \
-isolation_ground_net VSS \
-clamp_value 0 \
-applies_to outputs \
-elements {CNT/count1}
```

```
set_isolation_control iso_strategy4
\
 -domain Domain_4 \
 -isolation_signal iso4 \
 -isolation_sense high
```

```
map_isolation_cell iso_strategy4 \
 -domain Domain_4 \
 -lib_cells {ISOLORX1_RVT ISOLORX2_RVT ISOLORX4_RVT ISOLORX8_RVT ISOLORAOX1_RVT ISOLORAOX2_RVT ISOLORAOX4_RVT ISOLORAOX8_RVT}
```

In ModelSim, you will need to add the UPF and Power Aware libraries:

```
vmap mtiUPF /w/apps3/Mentor/ModelsimSE/v2020.4/modeltech/upf_lib
vmap mtiPA /w/apps3/Mentor/ModelsimSE/v2020.4/modeltech/pa_lib
```

Now you can compile all of the Verilog files.
The whole simulation will be done in three steps. 1.Compile, 2. Optimization, 3. Simulate.
Use the following command to compile you design,

vlog +acc=rn 1_clk_mux.v 2_lfsr.v 3_seqdet.v 4_counter.v 5_bcd_convert.v top.v lab3_tb.sv

The option +acc = rn adds the register and netlist into the monitor, and allows you exam the value of the register and netlist, makes the debugging much easier.

Use the following command to optimize your design, add necessary component to enable the power gating.

vopt lab3_tb -pa_upf lab3.upf -o lab3_pa -pa_enable=supplynetworkdebug

Finally, to run the simulation, you will need to include the power aware library:

vsim -pa work.lab3_pa -pa_lib work -L mtiPA

Your lab3.upf is correct if you see (after you type “quit -sim"):

```
# ================================================
#         TEST CASE PASSED      :)         time:2300
# ================================================
```

Part 2: Synthesis

Before you can synthesize the design you will need to edit the included .tcl file. For UPF synthesis, Synopsys Design Compiler needs to know the operating voltage of each power domain. Add these definitions to lab3_synthesis.tcl.

The line(s) of code added to lab3_synthesis.tcl for operating voltages:

```
set_voltage 1.05 -object_list {Vck_mx}
set_voltage 1.05 -object_list {Vlfsr}
set_voltage 1.05 -object_list {Vsd}
set_voltage 1.05 -object_list {Vcnt}
set_voltage 1.05 -object_list {Vbcd}
# SET ALL VOLTAGES EQUAL TO VDD RAIL
```

Multiple power domains also require the use of isolation cells. By default, the library tells the synthesis tool not to use or touch these cells. Find and uncomment the necessary lines in lab3_synthesis.tcl to enable the isolation cells. Run Synopsys Design Compiler:

```
dc_shell -f lab3_synthesis.tcl
```

Report the synthesized design area here:

Combinational	Buf/Inv	Noncombinational	Net Interconnect
160.11	18.3	186.54	40.6

Report the synthesized design power here:

Switch Power	Int. Power	Leak Power	Total Power
3.31	21.3	3.87e+07	63.26