BIRLA INSTITUTE OF TECHNOLOGY & SCIENCE, PILANI K. K. BIRLA Goa Campus
First Semester 2017-2018
CS F342 Computer Architecture
Lab – 2, 24th August 2017

Implement the following design using verilog HDL in Xilinx 14.7. **Download decodeExecute.v file**. Add **decodeExecute.v** as a source to your project and modify it.

Control Circuit :

Instruction	Opcode (IR[6:0])	Funct3 (IR[14:12])	Aluop(3b)	aluSrcA(1b)	alusrcB(3b)	aluout(2b)
sub	0110011	000	001	0	000	00
or	0110011	110	010	0	000	00
andi	0010011	111	011	0	001	00
lw	0000011	010	000	0	001	00
srai	0010011	101	100	0	010	00
lui	0110111	XXX	000	0	000	01
sw	0100011	010	000	0	011	00
j	1101111	XXX	000	1	100	00
c.addi	XXXXX01	XXX	000	0	101	00
c.mv	XXXXX10	XXX	000	0	000	10

ALU Operations:

ALUop(3b)	Operation
000	Add
001	Subtract
010	OR
011	AND
100	Shift Right Arithmetic

Waveform: