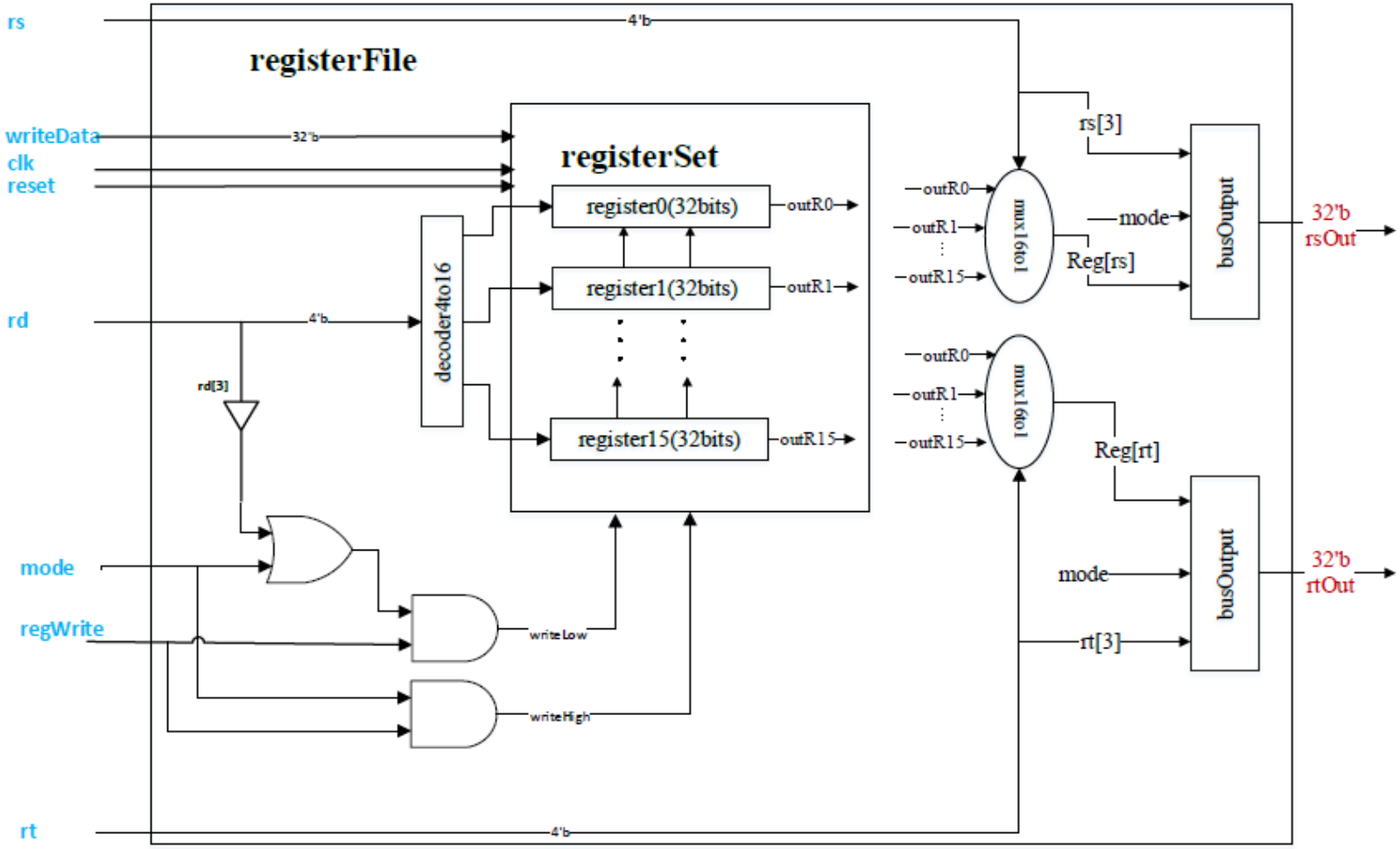
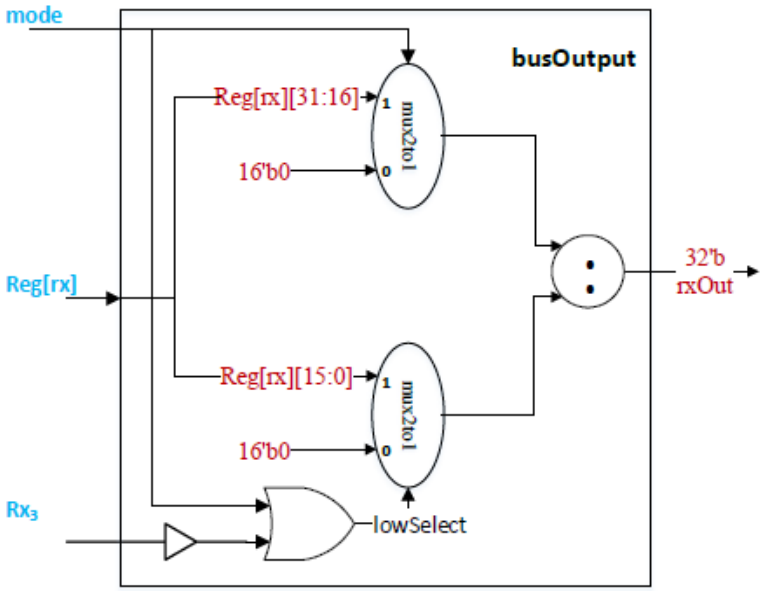
BIRLA INSTITUTE OF TECHNOLOGY & SCIENCE, PILANI K. K. BIRLA Goa Campus
First Semester 2017-2018
CS F342 Computer Architecture
Lab – 1, 17th August 2017

Implement the following design using verilog HDL in Xilinx 14.7. **Download registerFile.v file**. Add **registerFile.v** as a source to your project and modify it.





Truth Table for writeLow and writeHigh :

mode	regWrite	rd[3]	writeLow	writeHigh
X	0	X	0	0
0	1	0	1	0
0	1	1	0	0
1	1	X	1	1

Truth Table for lowSelect :

mode	Rx_3	lowSelect
0	0	1
0	1	0
1	0	1
1	1	1

Output using Xilinx 14.7 :