BIRLA INSTITUTE OF TECHNOLOGY & SCIENCE, PILANI K. K. BIRLA Goa Campus
First Semester 2017-2018
CS F342 Computer Architecture
Lab – 2, 24th August 2017

Implement the following design using verilog HDL in Xilinx 14.7. **Download decodeExecuteInterfaces.v file**. Add **decodeExecuteInterfaces.v** as a source to your project and modify it.