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I2C ADDRESSES	
Designator	I2C Address (7-bit)
U13	0x40

REVISION HISTORY

Rev.	Date	Description	By	ECO
1	12/03/2024	Initial Release	Sagi R.	-
1	12/04/2024	- After design review 1. - See Confluence page link below.	Sagi R.	-
1	12/10/2024	- Remapped the DB 15 channel order to make layout easier. - JP7 pinout changed, swapped _p and _n. - Changed Samtec connectors to the STM32 board to elevated ones. - Added jumper for AFE /PWDN. - Added AGND test points. - Added Screw standoffs as mechanical no BOM. Add item to BOM as needed. - Added series termination resistors to clock and SPI lines.	Sagi R.	-
1	12/11/2024	- DB 15, moved pin 5 to pin 12. - Added fiducials on PCB for assembly.	Sagi R.	-
2	03/26/2025	- Footprints of J5, U8 are not correct. Fixed - U2 is not connected to 5V and 3.3V. Fixed - The ADS1298 START signal should be tied high, R9 to be populated. - Added: High side switch, power monitoring IC, STM32 microcontroller. - Changed a lot of the resistors to 0402 from 0603. - Changed all connectors to smaller ones. - Resized L1.	Sagi R.	-

Review notes: https://myomo.atlassian.net/wiki/spaces/XM3/pages/3562405950/ADS1298+Shield+board+for+STM32+G431RB+Design+review

FID_TOP1 FID_BOT1
FID_TOP2 FID_BOT2
FID_TOP3 FID_BOT3

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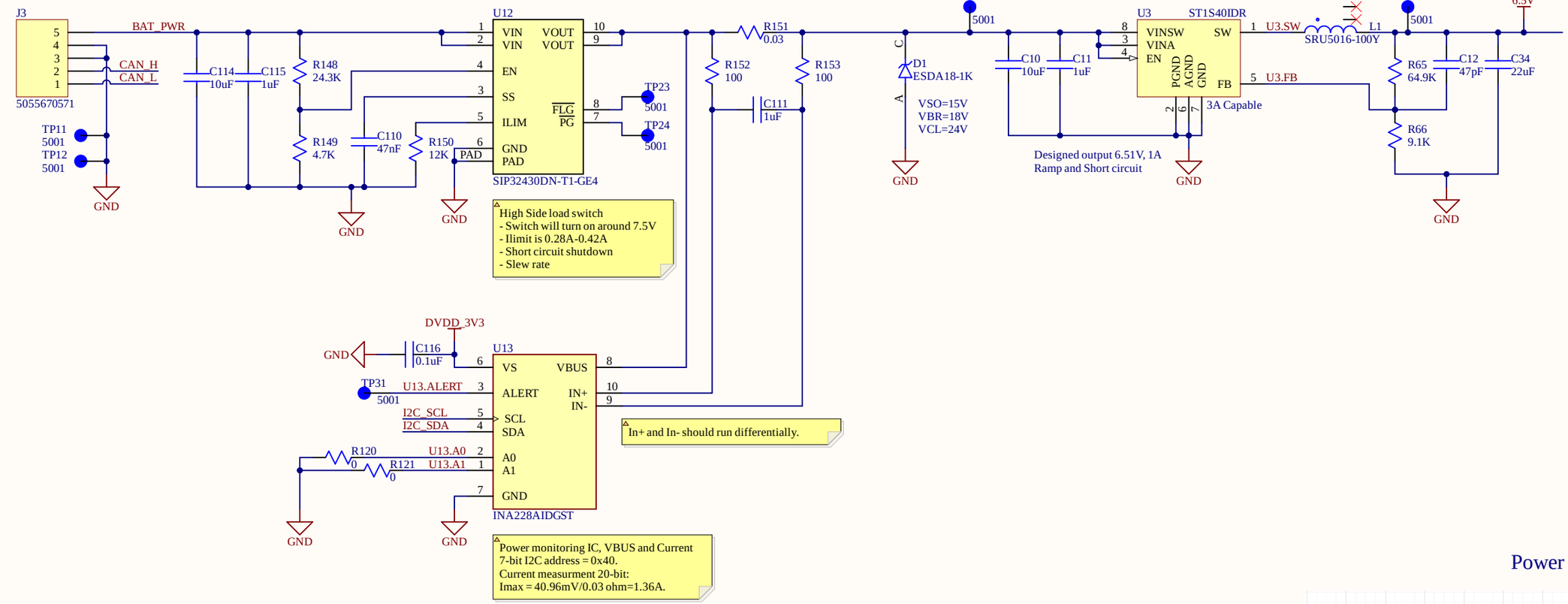
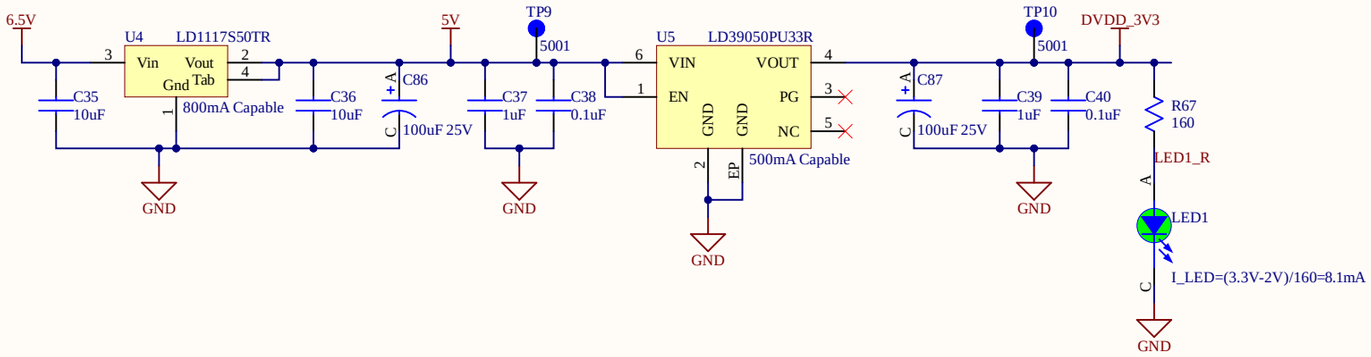
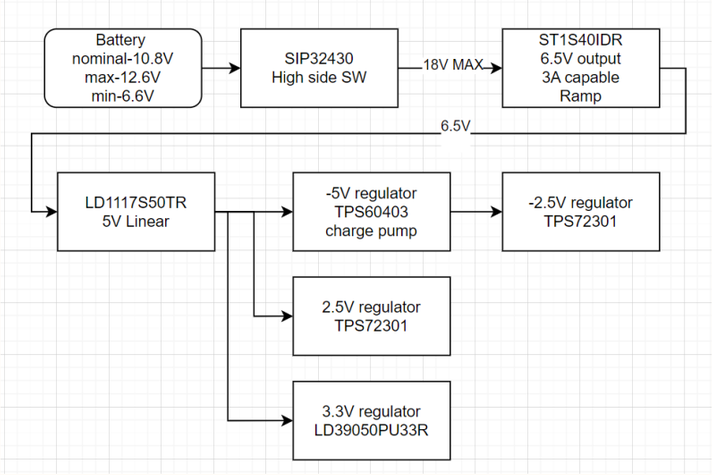
PCA NAME: PCA_ADS1298_SHIELD	DESIGNED BY:	Sagi R.	03/12/2025
PCA REVISION: 2	APPROVED BY:	--	--
PCA NUMBER: 110-0002	DATE: 3/26/2025	DOCUMENT SIZE: B	
TOC_and_Revision.SchDoc	TIME: 18:52:24	SHEET: 1 OF 9	

Battery input votage is between 6.6V-15V





Power scheme



Notes:
STM32 is powered by the 5V rail.

Battery info:
Battery voltage = 12.6V down to 7.5V (cut off)
Discharge current = 4A @35C
OC Protection = 4.8A continuous <2-4 seconds
OL Protection = 15.27A <23ms
SC Protection = 38.88A <916ns

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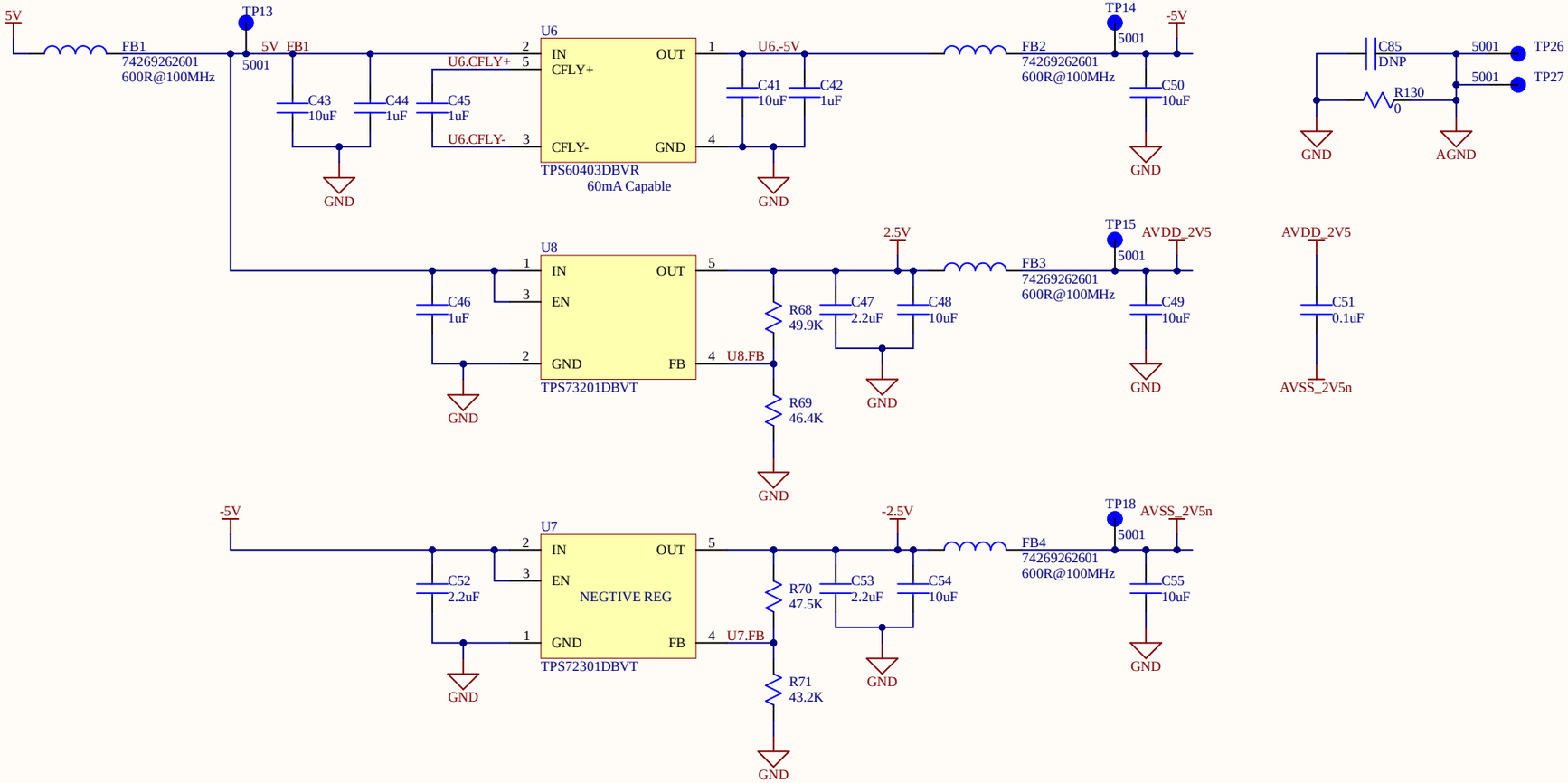

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PCA NUMBER: 110-0002	DATE: 3/26/2025	DOCUMENT SIZE: B	
Regulators_2.SchDoc	TIME: 18:52:24	SHEET: 3 OF 9	

AFE ADS1298

Jumpers for testing and shorting the channels

U1.IN5_p — JP8 — U1.IN5_n
U1.IN6_p — JP9 — U1.IN6_n
U1.IN7_p — JP10 — U1.IN7_n
U1.IN8_p — JP11 — U1.IN8_n

U1.IN1_p — JP4 — U1.IN1_n
U1.IN2_p — JP5 — U1.IN2_n
U1.IN3_p — JP6 — U1.IN3_n
U1.IN4_p — JP7 — U1.IN4_n

Decoupling Pins 19,21,22

AVDD_2V5: C77 1uF, C78 0.1uF, C79 1uF, C80 0.1uF
AVSS_2V5n
AGND

Decoupling Pins 54,56,59

AVDD_2V5: C81 1uF, C82 0.1uF, C83 1uF, C84 0.1uF
AVSS_2V5n
AGND

U1.VREFP — C1 10uF, C2 0.1uF — AVSS_2V5n

AVDD_2V5 — R1 DNP — R2 DNP — AVSS_2V5n

DVDD_3V3

U1 — ADS1298IPAG

U1.IN8_n	1	IN8N	
U1.IN8_p	2	IN8P	
U1.IN7_n	3	IN7N	
U1.IN7_p	4	IN7P	
U1.IN6_n	5	IN6N	
U1.IN6_p	6	IN6P	
U1.IN5_n	7	IN5N	
U1.IN5_p	8	IN5P	
U1.IN4_n	9	IN4N	
U1.IN4_p	10	IN4P	
U1.IN3_n	11	IN3N	
U1.IN3_p	12	IN3P	
U1.IN2_n	13	IN2N	
U1.IN2_p	14	IN2P	
U1.IN1_n	15	IN1N	
U1.IN1_p	16	IN1P	
U1.RLDIN	62	RLDIN	
U1.RLDOUT	63	RLDOUT	
RLD_n	61	RLDINV	
	17	TESTP_PACE_OUT1	
	18	TESTN_PACE_OUT2	
	27	NC	
	29	NC	
	64	WCT	
U1.RLDREF	60	RLDREF	
SPI_SCLK_R	40	SCLK	
SPI_MOSI_R	34	DIN	
SPI_MISO_R	43	DOUT	
SPI_CSn	39	CS	
ADS1298_DRDYn_R	47	DRDY	
U1.CLKSEL	52	CLKSEL	
U1.GPIO4_5001	46	GPIO4	
U1.GPIO3_5001	45	GPIO3	
U1.GPIO2_5001	44	GPIO2	
U1.GPIO1_5001	42	GPIO1	
ADS1298_START	38	START	
U1.CLK	37	CLK	
ADS1298_RESETn	36	RESET	
U1.PWDN	35	PWDN	
	41	DAISY_IN	

AVDD_2V5 — 19, 21, 22, 54, 56, 59
DVDD_3V3 — 50, 48
AVDD, AVDD, AVDD, AVDD1, AVDD, AVDD
DVDD, DVDD
VREFP, VREFN — 24, 25
AVSS, AVSS, AVSS, AVSS1, AVSS, AVSS — 20, 23, 32, 53, 57, 58 — AVSS_2V5n
RESV1, DGND, DGND, DGND — 31, 33, 51, 49 — AGND
VCAP1, VCAP2, VCAP3, VCAP4 — 28, 30, 55, 26

C5 22uF, C6 1uF, C7 1uF, C8 0.1uF, C9 1uF — AVSS_2V5n

series termination resistor
Install near ADS1298

R3 10K, R4 10K, R5 10K, R6 10K, R7 10K

series termination resistors
Install near STM32.

R134 0 — SPI_SCLK
R135 0 — SPI_MOSI
R136 0 — SPI_MISO
R137 0 — ADS1298_DRDYn

Ground CLKSEL for external OSC.

R8 0 — AGND

GPIO4 — TP3
GPIO3 — TP4
GPIO2 — TP5
GPIO1 — TP6

DVDD_3V3
R9 10K, R10 10K, R11 10K, R12 10K
TP19 5001

series termination resistor

R133 0 — X1.CLK

JP16 — AGND

X1 — 632L3I002M04800
OUT, VCC, EN, GND
4, 1, 2
X1.CLK, X1.EN
DVDD_3V3
C3 1uF, C4 DNP
AGND

RLD_p — JP13 — R123 0 — U1.RLDOUT
RLD_p — R124 1M, C72 0.01uF — RLD_n
SH_DRIVE — JP12 (3, 1, 2)

AVDD_2V5
C10 1uF, AGND
U9.POS
U9
SH_DRIVE_AMP — 1
U9.NEG — 3
AVSS_2V5n
SH_DRIVE
LM8261M5X/NOPB
Shield Drive
C11 1uF, AGND
AVSS_2V5n

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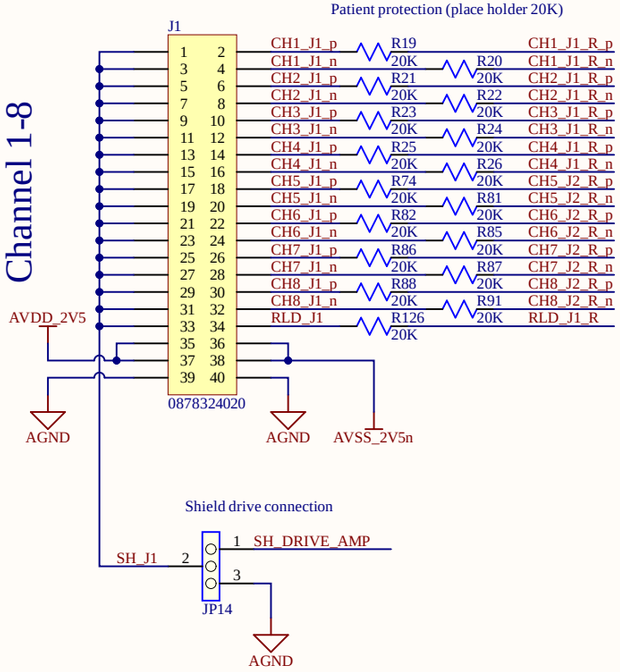
PCA REVISION: 2	APPROVED BY:	--	--
PCA NUMBER: 110-0002	DATE: 3/26/2025	DOCUMENT SIZE: B	
ADS1298.SchDoc	TIME: 18:52:24	SHEET: 4 OF 9	

Channel 1-8

Patient protection (place holder 20K)



Shield drive connection

Channel filtering 3db is at 2.5KHz

AC coupling
Place holder

Channel biasing

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PCA NAME: PCA_ADS1298_SHIELD	DESIGNED BY:	Sagi R.	03/12/2025
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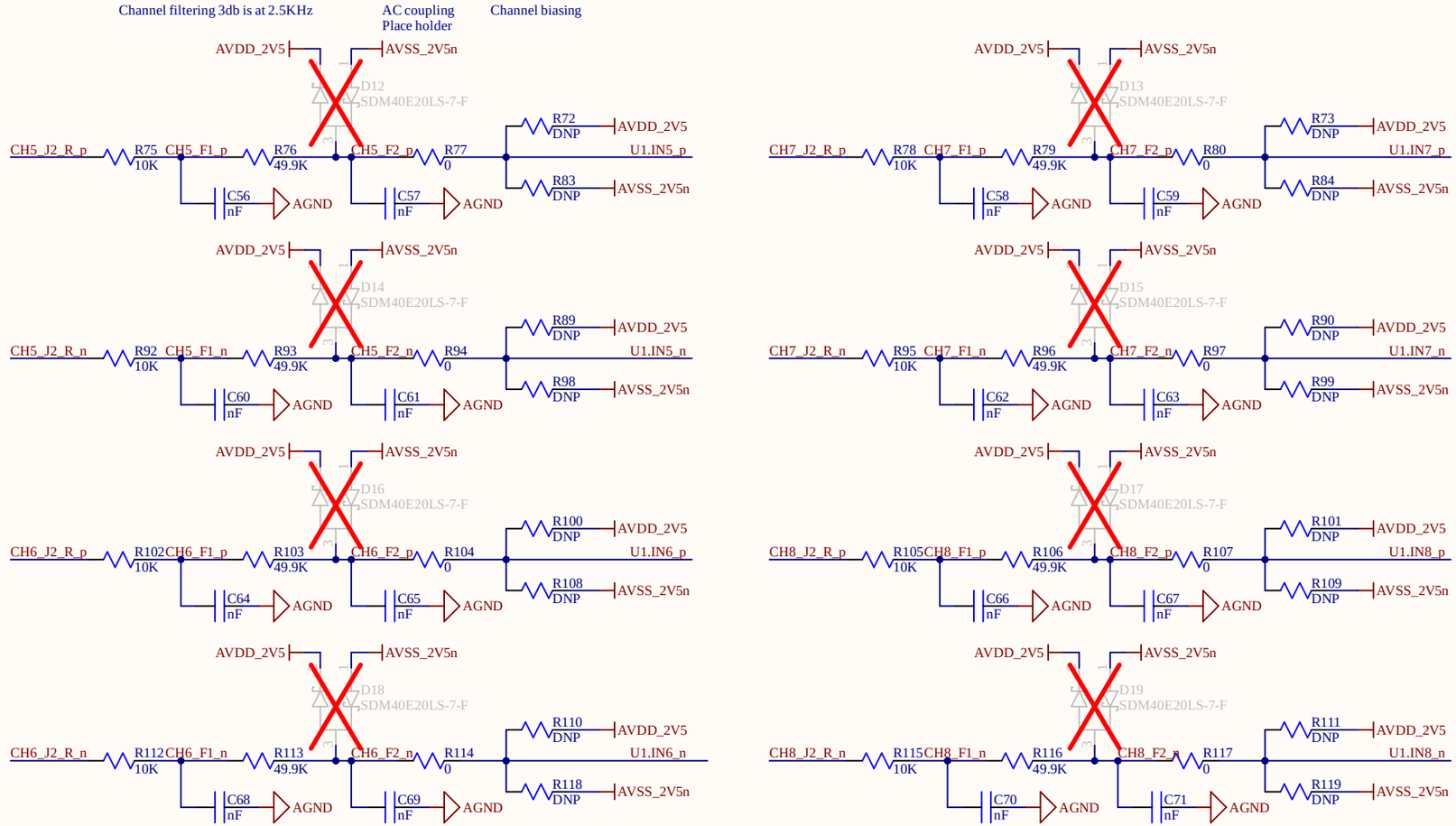
EMG_connectors_and_filters_CH_1_4.SchDoc	TIME: 18:52:24	SHEET: 5 OF 9	



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		NAME	DATE
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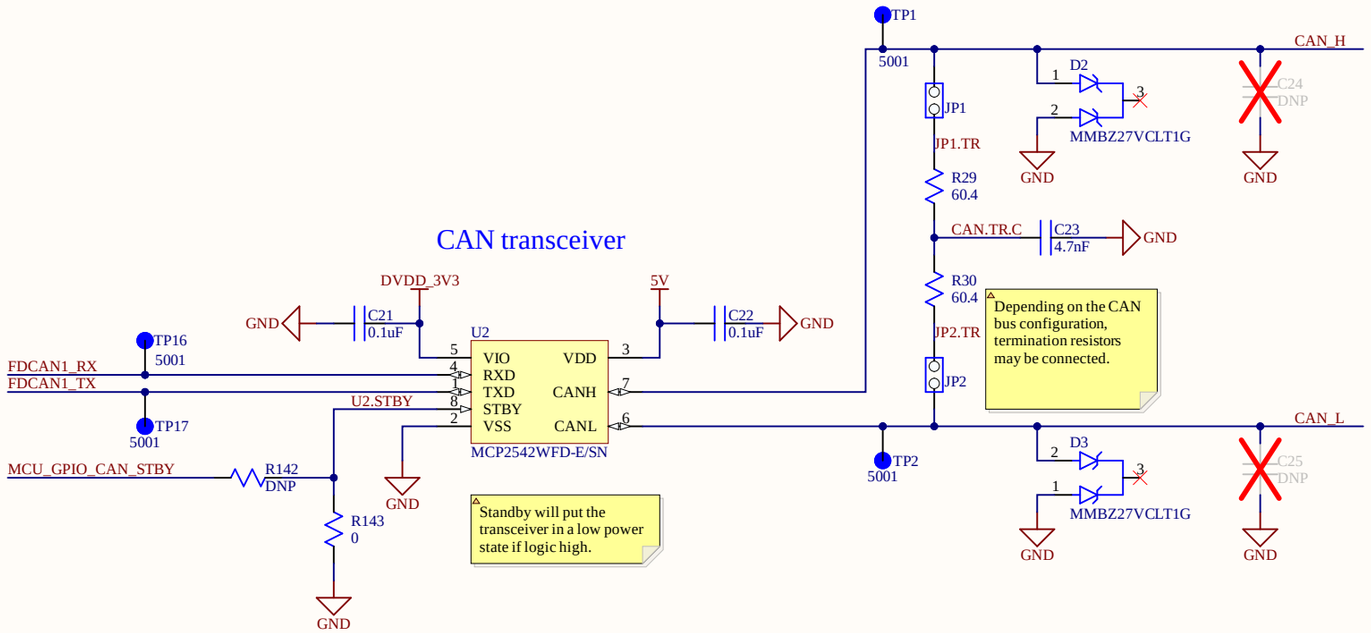
PCA NUMBER: 110-0002	DATE: 3/26/2025	DOCUMENT SIZE: B	
EMG_connectors_and_filters_CH_5_8.SchDoc	TIME: 18:52:24	SHEET: 6 OF 9	

Design base on the MIKROE-2299
https://www.digikey.com/en/products/detail/mikroelektronika/MIKROE-2299/6100137

CAN transceiver



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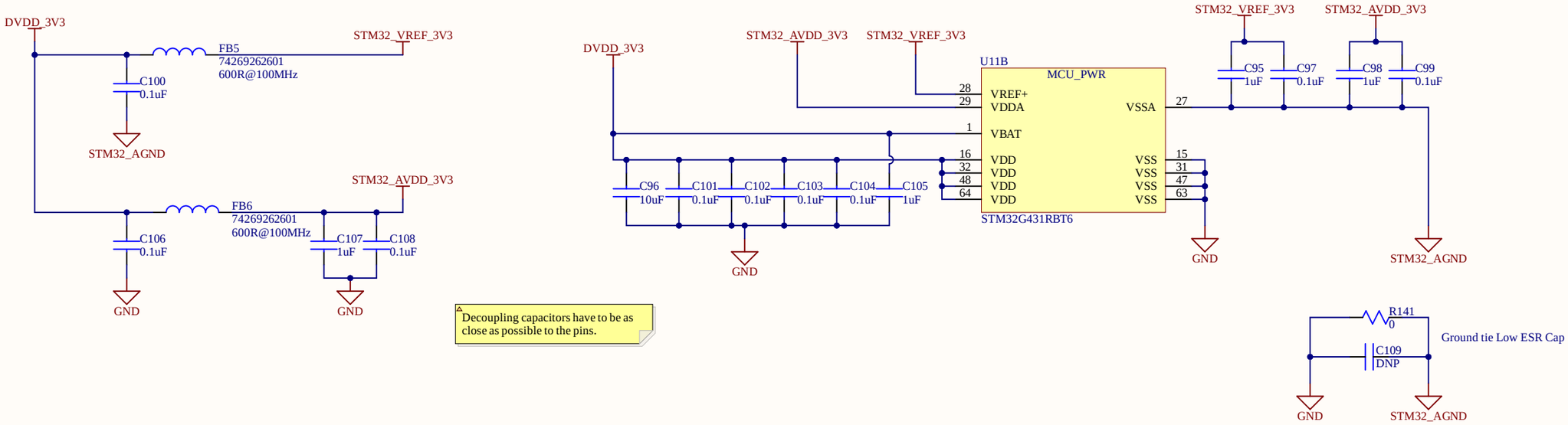
CAN.SchDoc	TIME: 18:52:24	SHEET: 7 OF 9	



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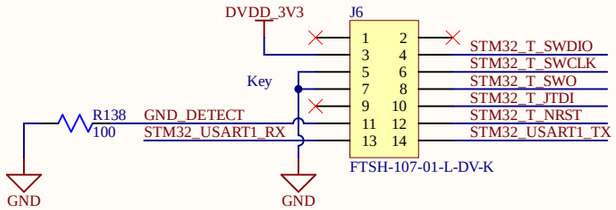
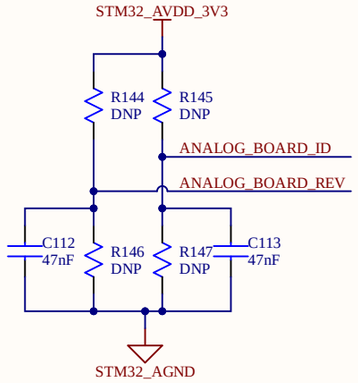
STM32_POWER.SchDoc	TIME: 18:52:24	SHEET: 8 OF 9	

SWD + JTAG Programing port

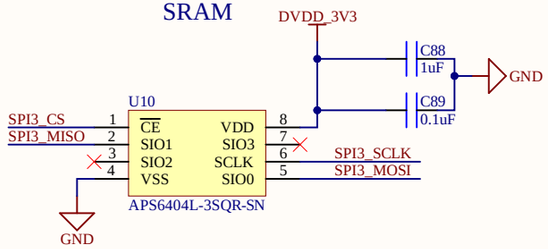


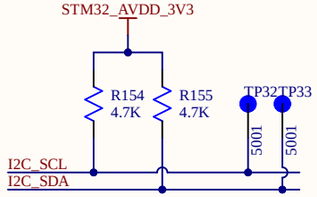
SWDIO and SWCLK should run as a pair with equal length and shielded.

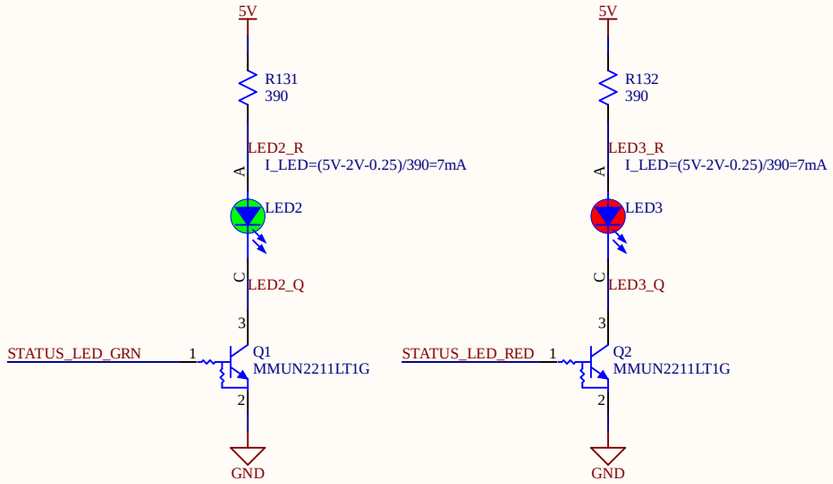


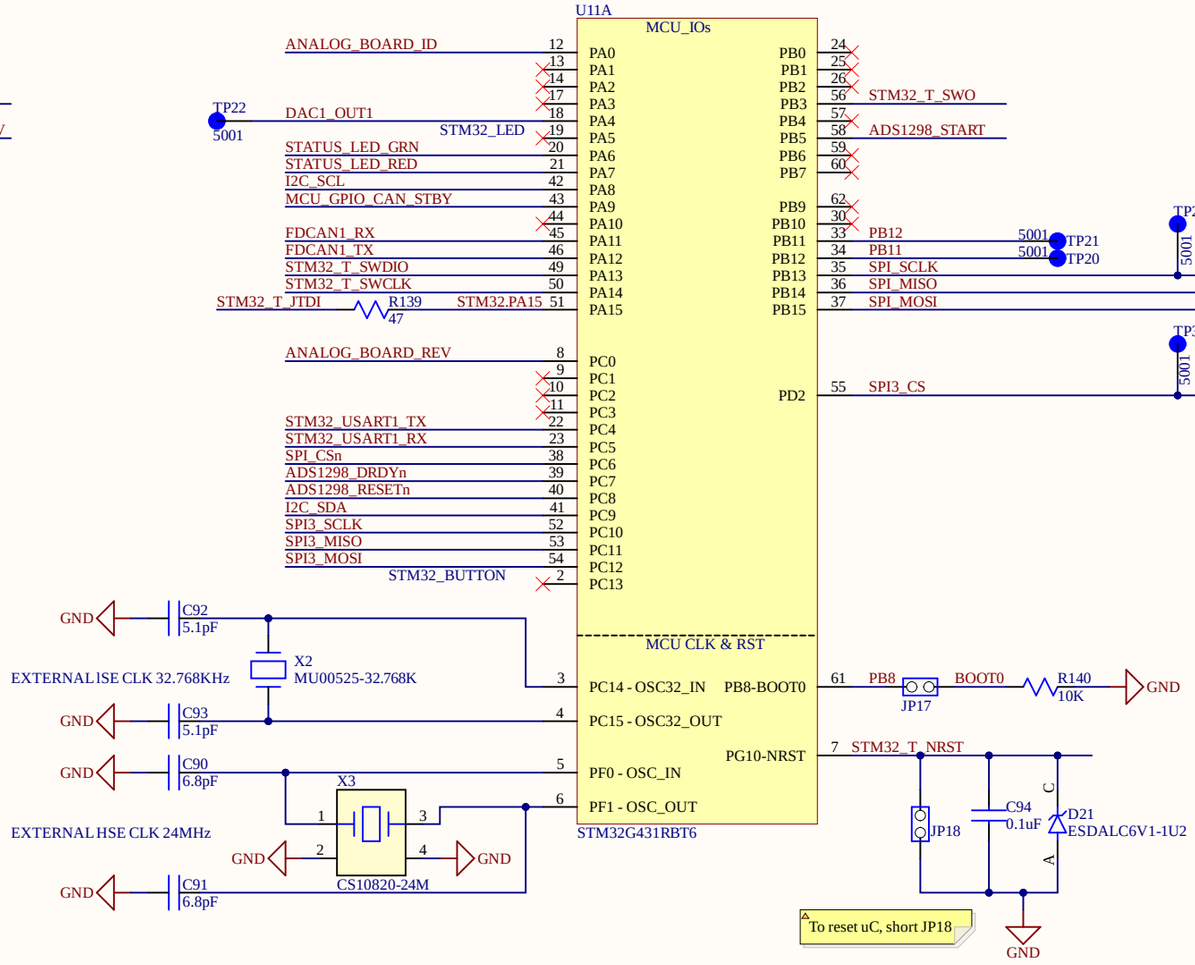
Analog input to determine board model and revision. Place caps close to STM32 analog input.

SRAM









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