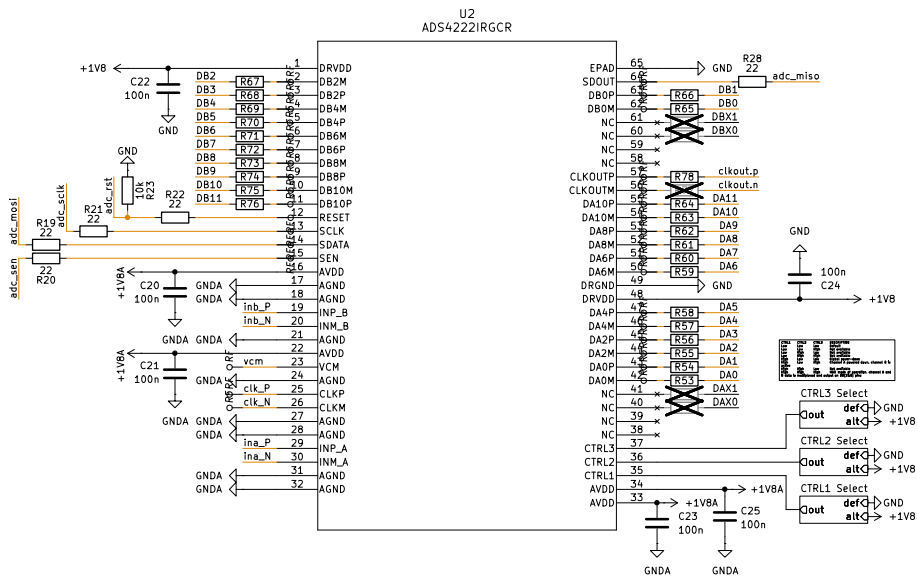
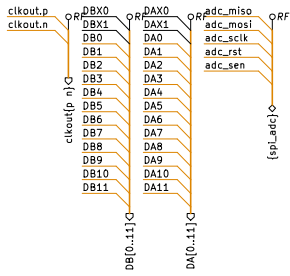


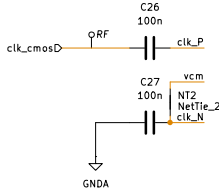
ADC



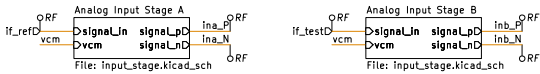
Data and control busses

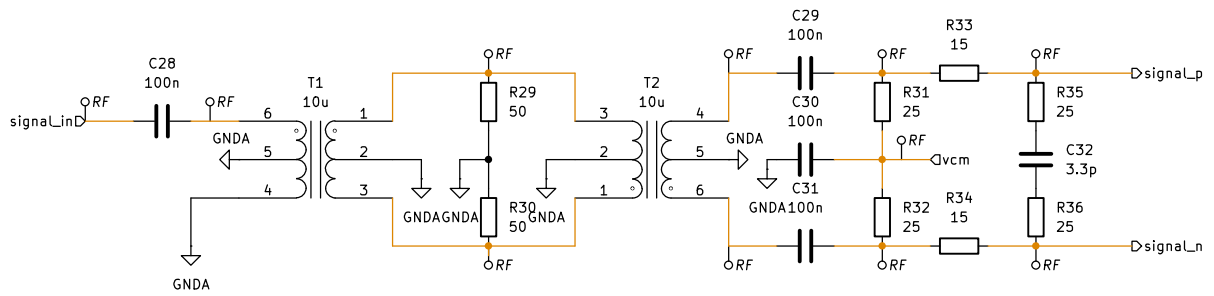


CMOS to diff clock



Input stages (single to dual-ended + filtering)





Sheet: /ADC/Analog Input Stage B/
File: input_stage.kicad_sch

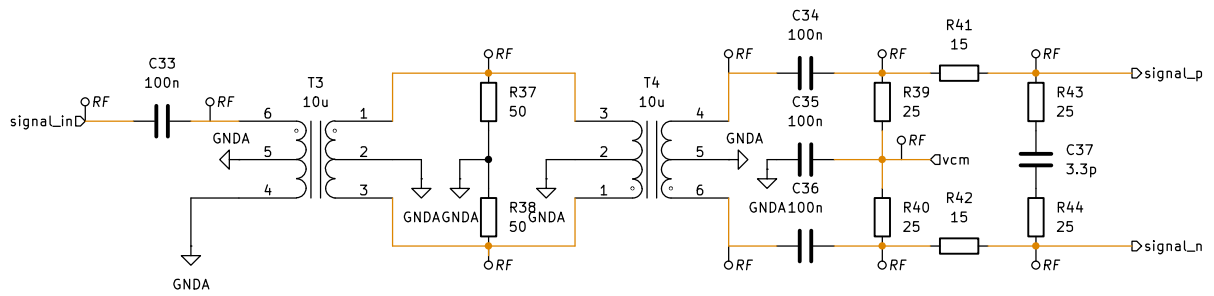
Title:

Size: A5
KiCad E.D.A. 8.0.3

Date:

Rev:

Id: 4/14



Sheet: /ADC/Analog Input Stage A/
File: input_stage.kicad_sch

Title:

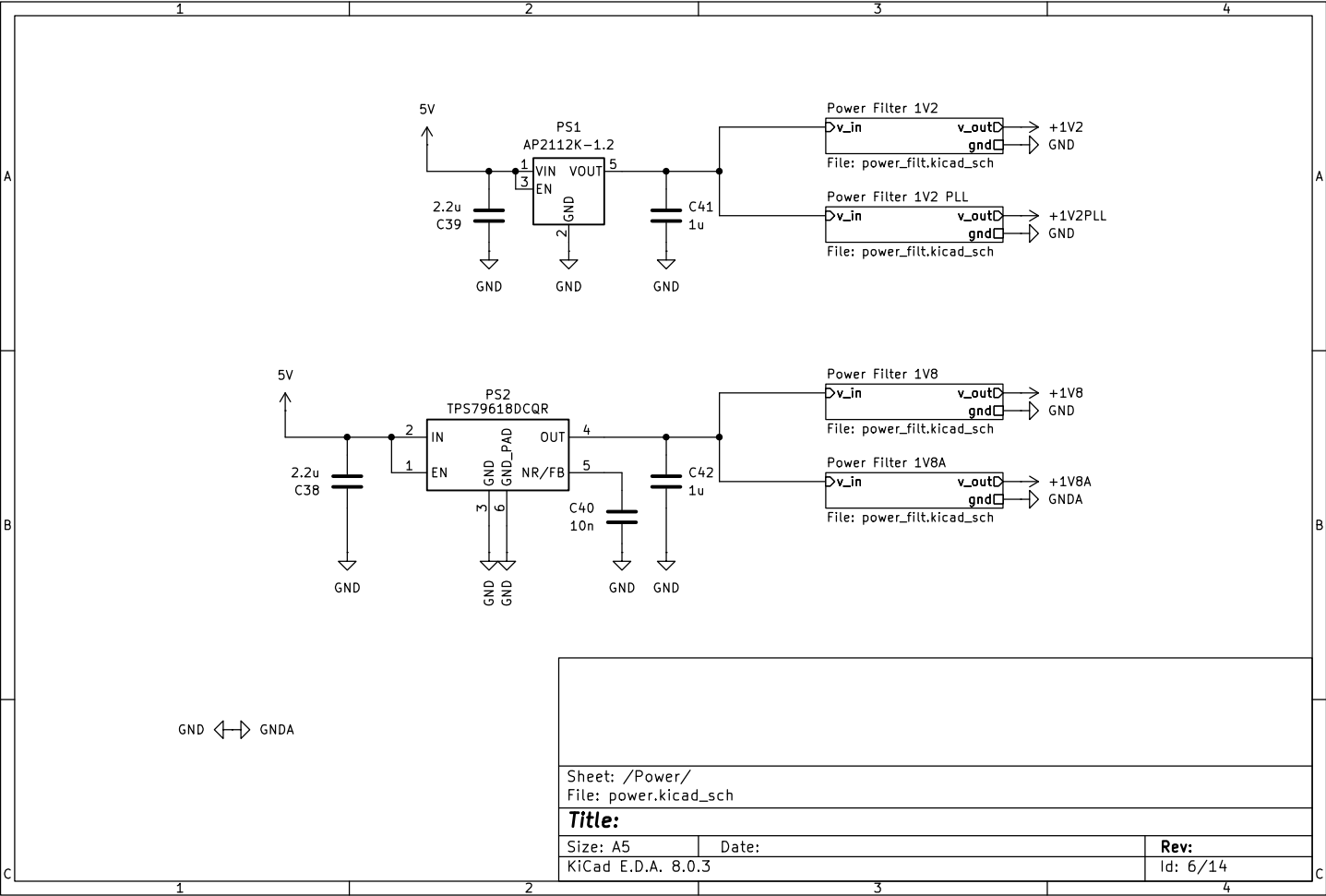
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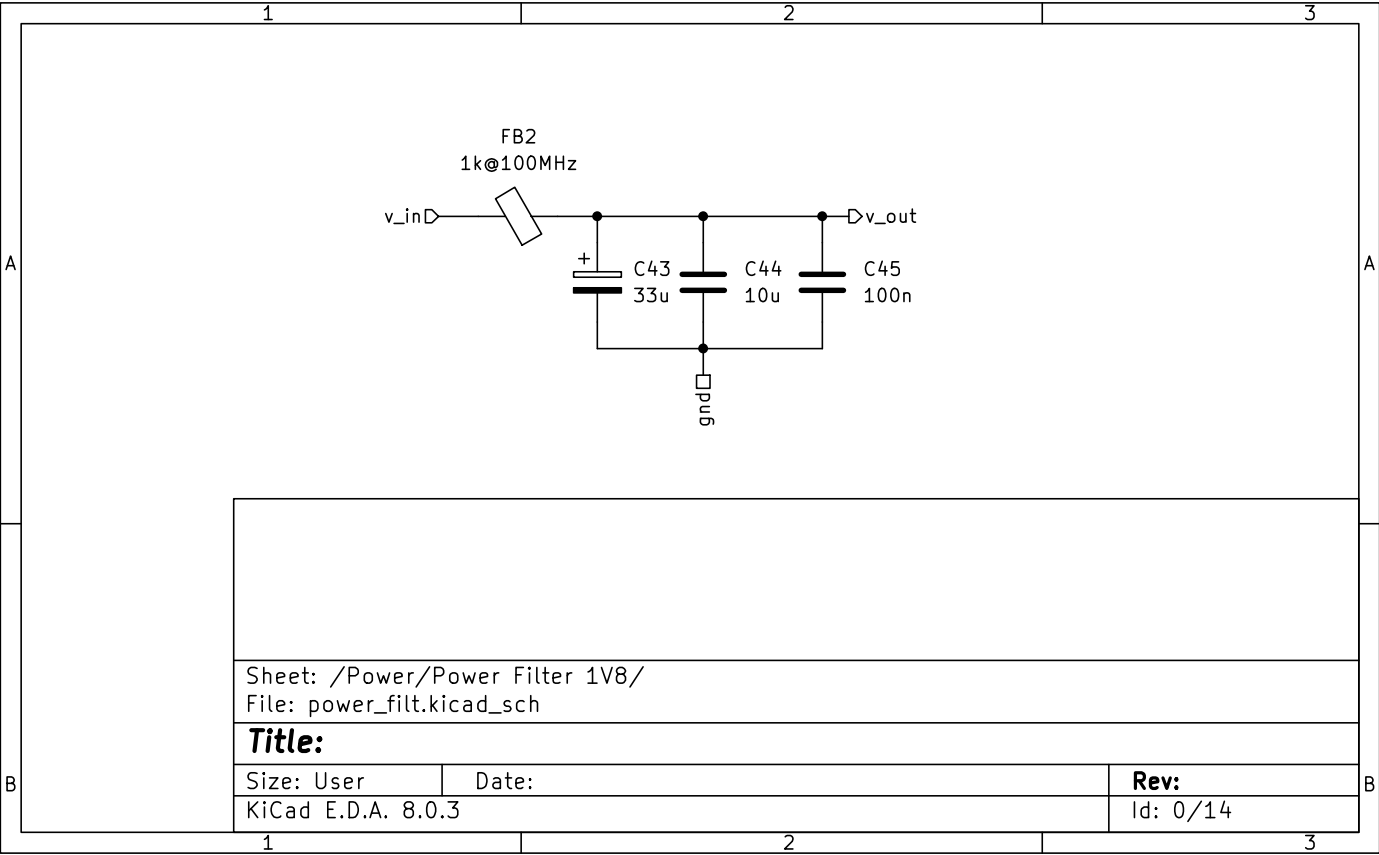
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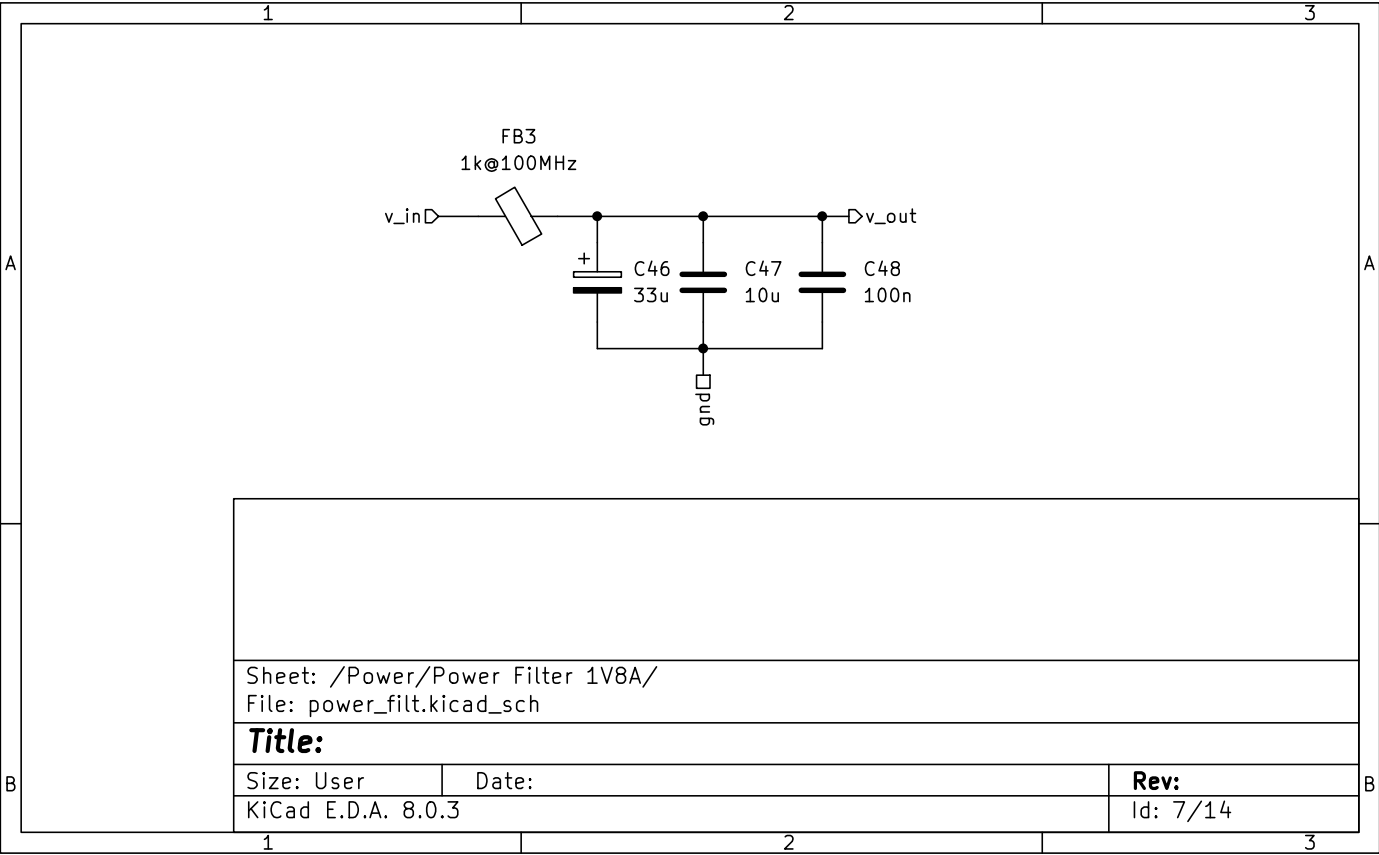
Rev:

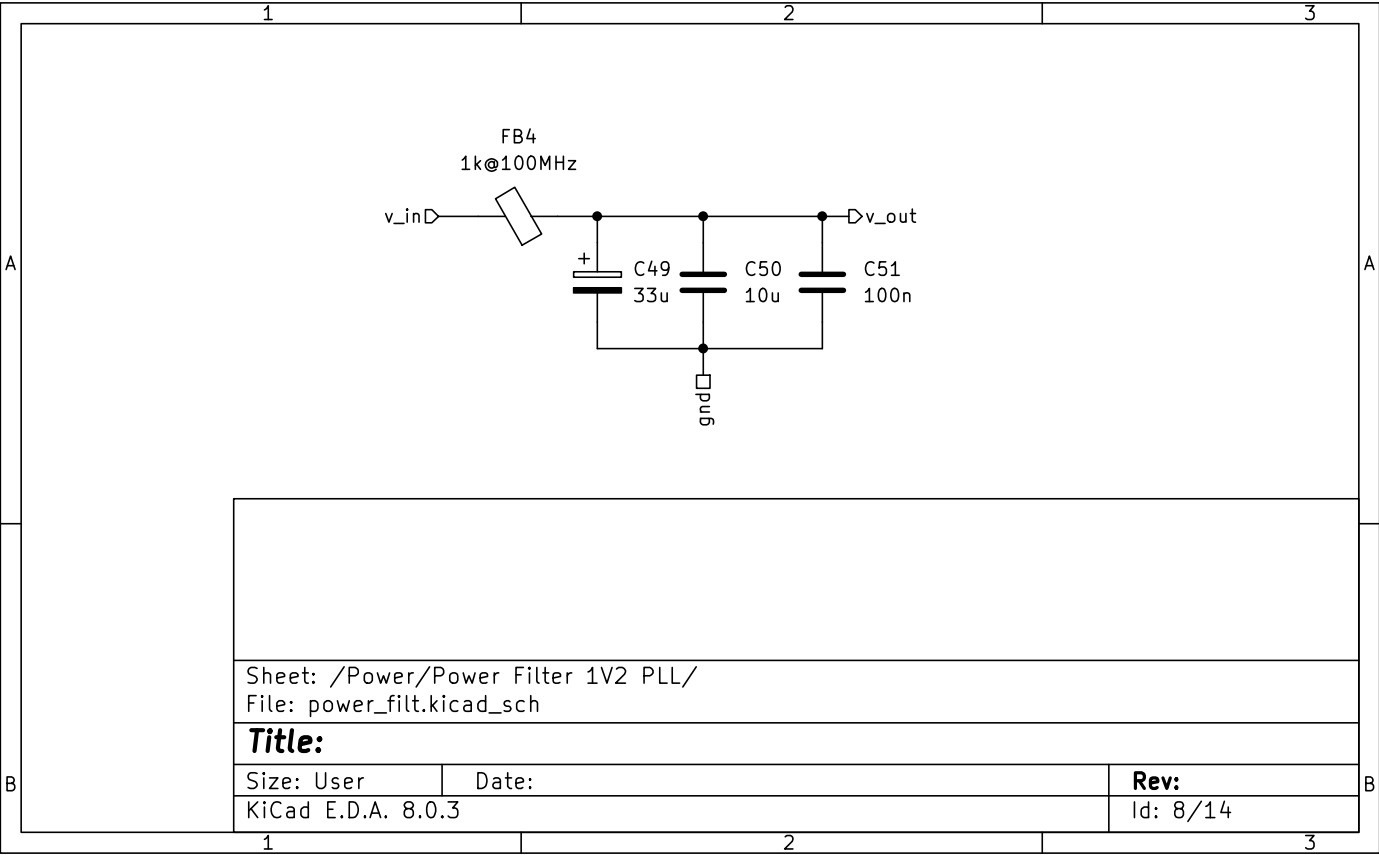
KiCad E.D.A. 8.0.3

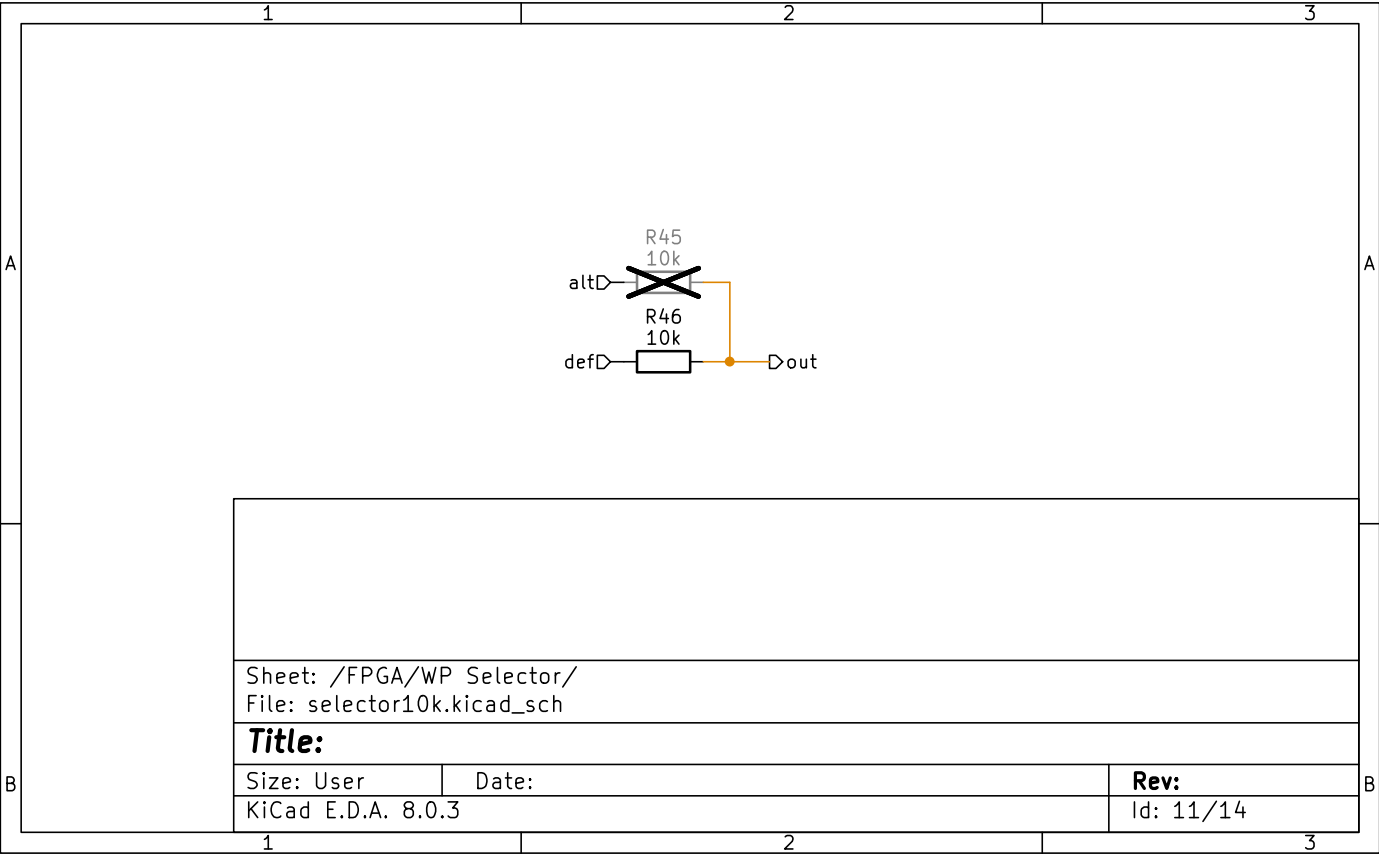
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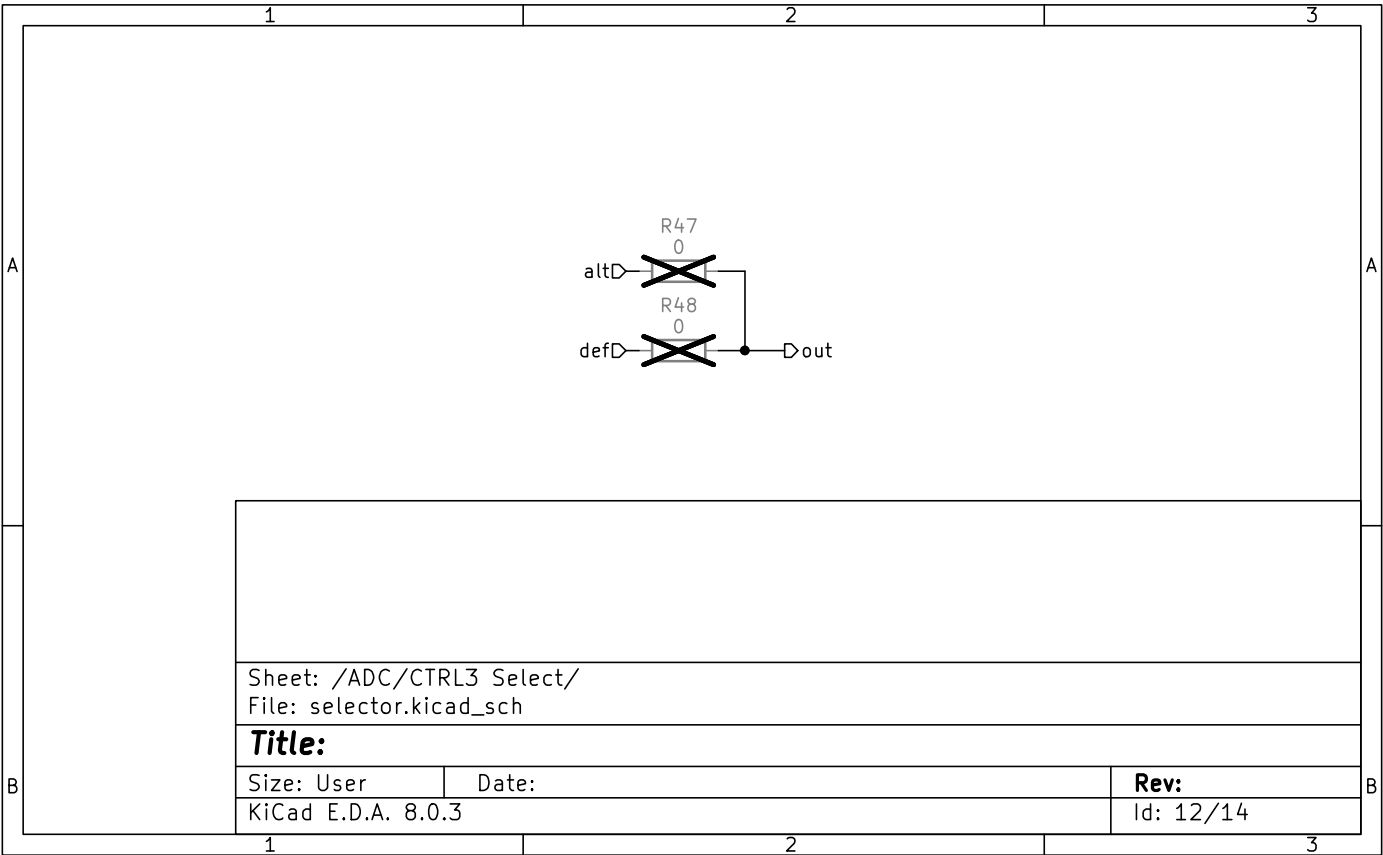




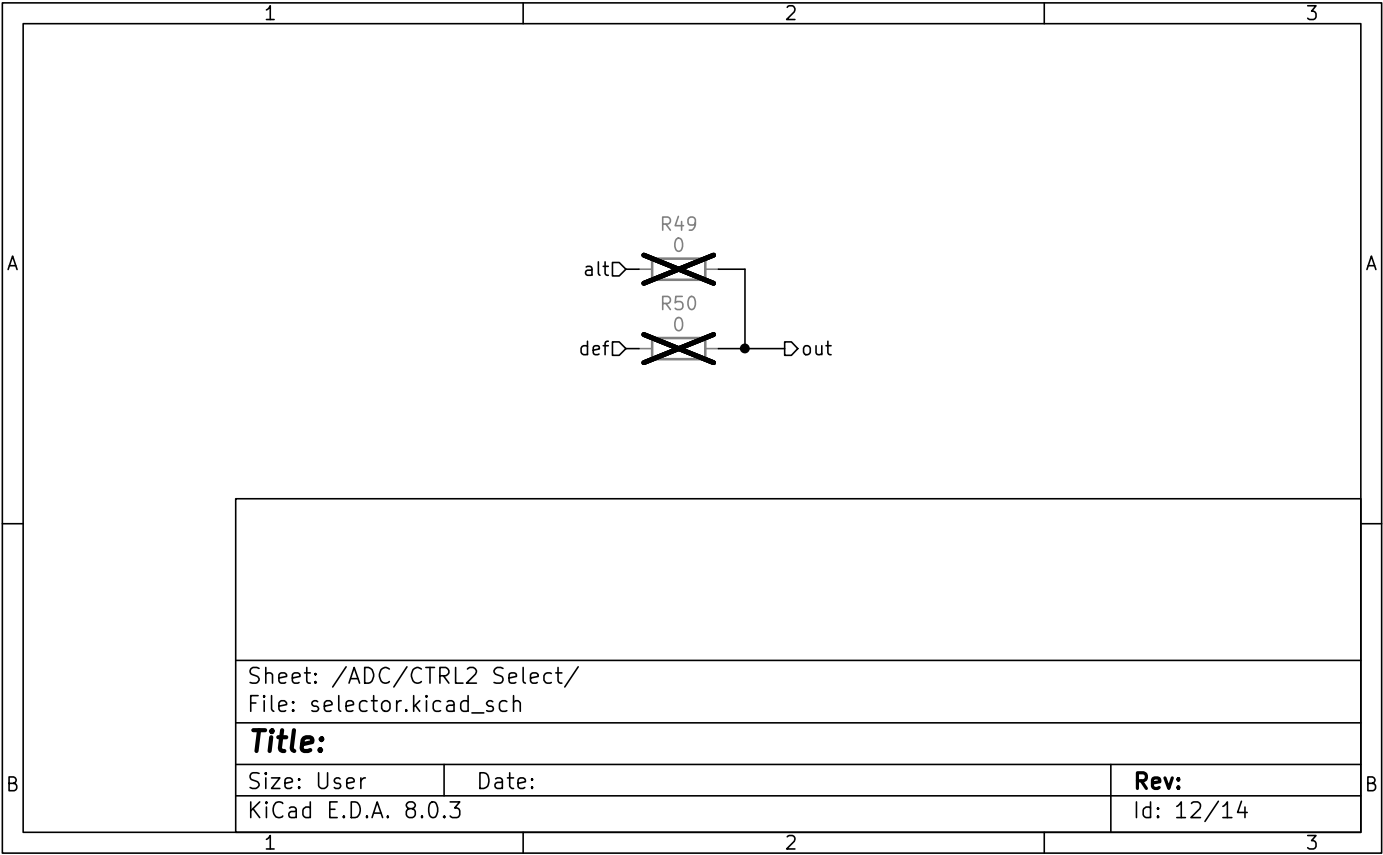




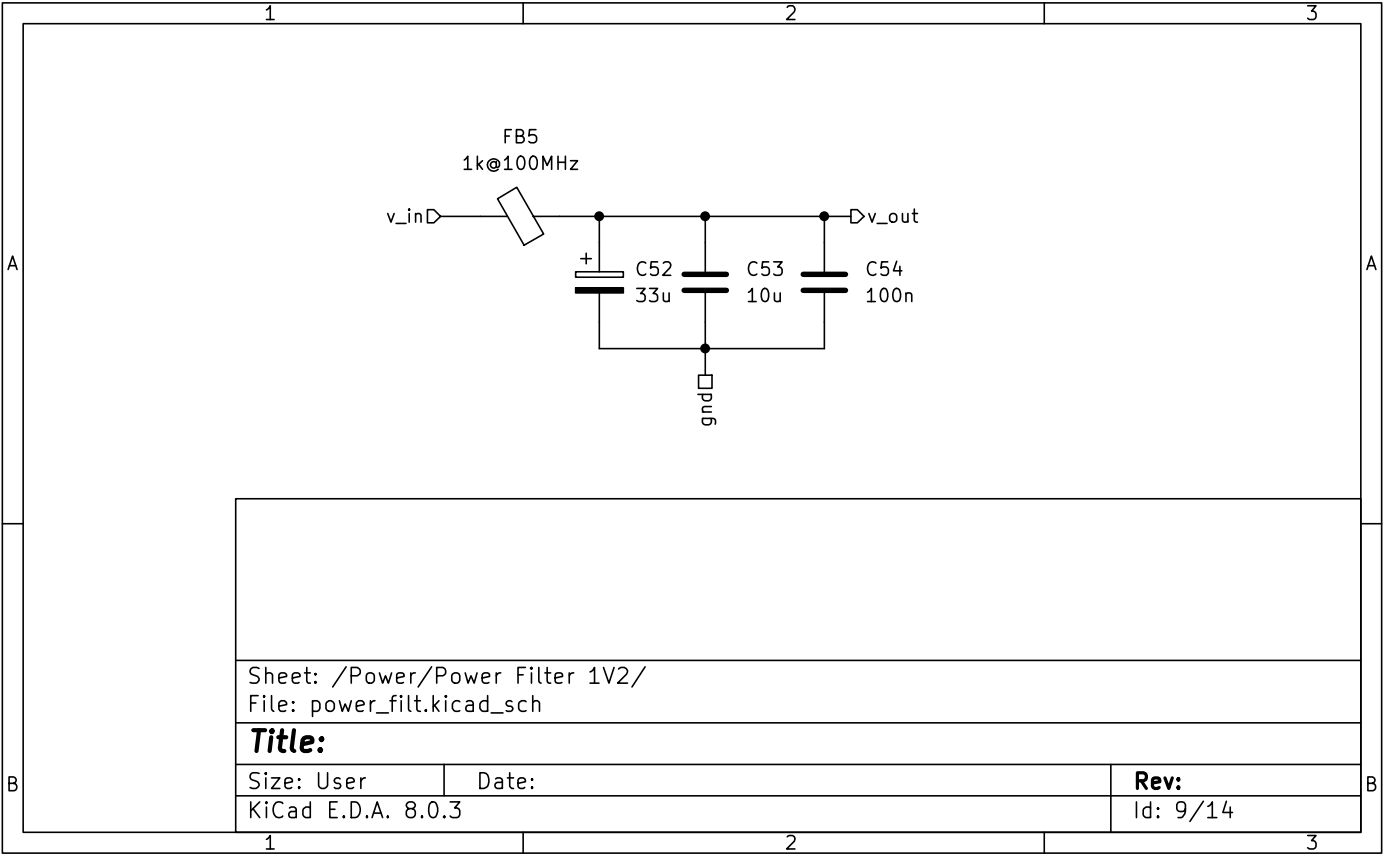




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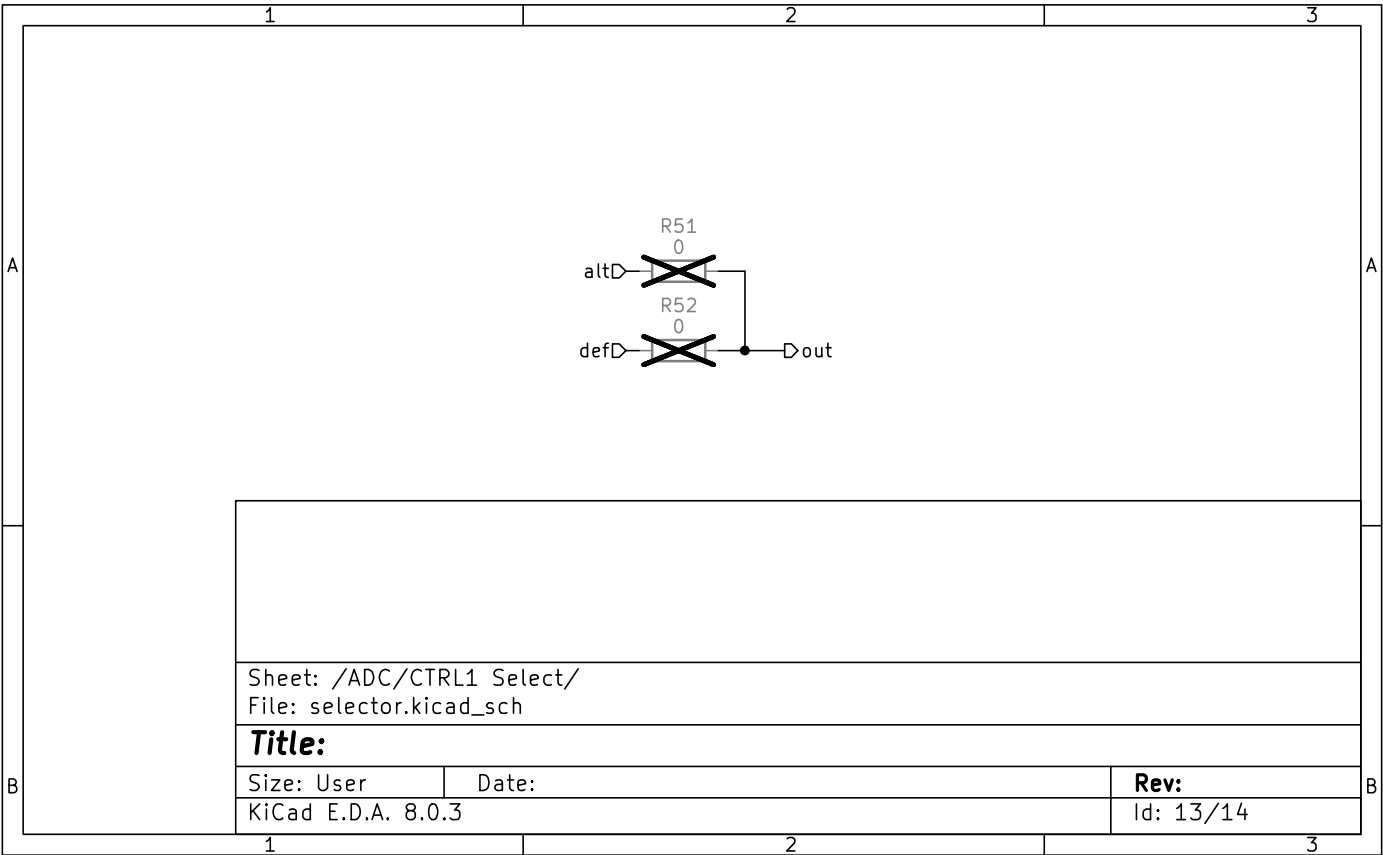


Id: 12/14



Id: 9/14

Id: 9/14



Id: 13/14

Id: 13/14