18CST32 & Computer Organization

CAT - III ANSWER KEY

PART - A

1).

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
I_0	IF	ID	OF	PO	PO	PO	WO								
I_1		IF	ID	OF			PO	PO	PO	PO	PO	PO	WO		
I_2			IF	ID			OF						PO	WO	
I_3				IF			ID						OF	PO	WO

= **15** clock cycles

2). Data Hazard

ADD R_1, R_2, R_3
SUB R_4, R_2, R_5
ADD R_5, R_1, R_6

R_1 Register will be used as Source Register in Instruct 3

(3)

$P_1 = \frac{1}{2} = 0.5$ GHz

$P_2 = \frac{1}{1.5} = 0.67$ GHz

$P_3 = \frac{1}{1} = 1$ GHz

$P_4 = \frac{1}{2} = 0.5$ GHz

So P_3 has the highest Peak clock frequency.

(4) The location that follows a branch Instruction is called Branch Delay Slot.

Example:

```
        Add   R7, R8, R9
        Branch_if_[R3] = 0   TARGET
        Ij+1
        :
TARGET: Ik
```

```
        Branch_If_[R5] = 0  TARGET
        ADD   R7, R8, R9
        Ij+1
        :
TARGET: Ik
```

(5)

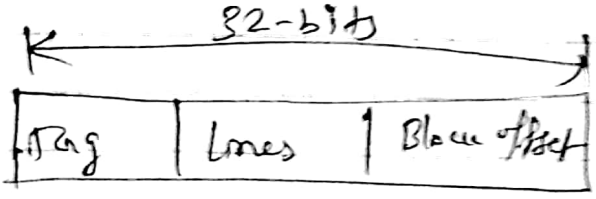
$$= \frac{4M \times 32}{512K \times 16}$$

$$= \frac{2^{27}}{2^{23}}$$

$$= 2^4$$

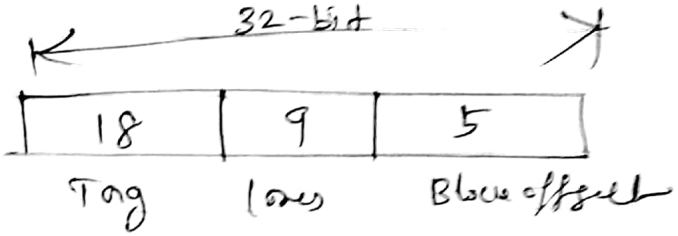
$$= 16 \text{ chips}$$

(6) Main memory $= 2^{32}$ Bytes



Block size = 32 Bytes
= 2^5 bytes

Cache memory = 512 lines
= 2^9 lines



So Tag field contains 18-bit

(7)

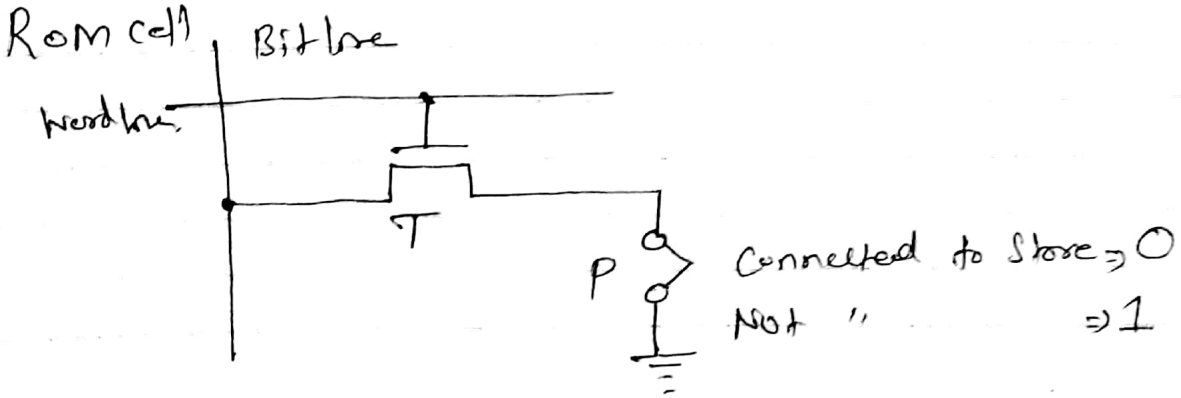
Word size = 32 bits (4 bytes)

5 Instructions, each of size 2+1+1+2+1 = 7 words

= 7 words
= 7 × 4 Bytes
= 28 Bytes

1000 × 28 = 1028 Bytes.

(8)



(9) LOAD R2, DATAIN

[OR]

READWAIT Read KIN flag
Branch to READWAIT if KIN = 0
Transfer data from KBD_DATA to R5

[OR]

```
READWAT :  LoadByte   R4, KBD_STATUS
           AND        R4, R4, #2
           Branch_if_[R4] = 0   READWAIT
           LoadByte   R5, KBD_DATA
```

(10)

Asynchronous Bus	Synchronous Bus
* Slower Data Transfer rates	* faster Data transfer rates
* It takes 2 RTD (Round trip Delay)	* It takes only one RTD (Round trip Delay)

PART-B

11) i)

I_1 : SUB R2, R3, R4
I_2 : SUB R4, R2, R3
I_3 : STORE R2, 100(R1)
I_4 : SUB R3, R4, R2

1) Flow dependency / True dependency (RAW)

I_1 : SUB R2, R3, R4
I_2 : SUB R4, R2, R3 $\quad I_1 \leftarrow I_2$
Ily $I_3 \leftarrow I_4$

2) Anti dependency / False / Name dependency (WAR)

I_1 = SUB R2, R3, R4
I_2 - SUB R4, R2, R3 $\quad I_1 \leftarrow I_2$

Ily I_2 : SUB R4, R2, R3
I_3 : STORE R2, 100(R1) $\quad I_2 \leftarrow I_3$

3) Output dependency (WAW)

I_1 : SUB R2, R3, R4 $\quad I_1 \leftarrow I_3$
I_3 : STORE R2, 100(R1)

4) No dependency (RAR)

I_1 : SUB R2, R3, R4 $\quad I_1 \leftarrow I_2$
I_2 : SUB R4, R2, R3
I_3 : STORE R2, 100(R1) $\quad I_1 \leftarrow I_4$
I_4 : SUB R3, R4, R2

ii) Data Hazard. (RAW)

I1 : SUB R2, R3, R4
I2 : SUB R4, R2, R3
I3 : STORE R2, 100(R1)
I4 : SUB R3, R4, R2

$I_1 \leftarrow I_2$

$I_3 \leftarrow I_4$

$I_2 \leftarrow I_4$

iii) NO. only Data Hazard can be avoided by using operand forwarding.

(12) Main memory Size = 256 kW

Cache size = 4kW

4-way set associative

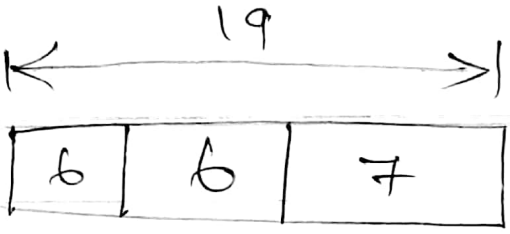
Block size = 64 W

(A) If representation in Byte addressable formate

Block size = 64 W
= 64 × 2 Bytes (1 Word = 16-bit)

Block size = 128 Bytes

1) Direct mapping



Main memory size = $256K \times 2B$

$= 2^{18} \times 2^1 B$

$= 2^{19}$ Bytes

Block size = 128 Bytes

$= 2^7$ Bytes

No. of lines = $\frac{\text{Cache size}}{\text{Block size}}$

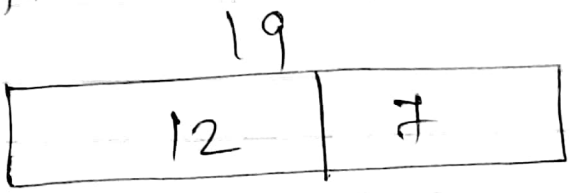
$= \frac{4K \times 2B}{128B}$

$= \frac{2^{13}}{2^7} = 2^6$

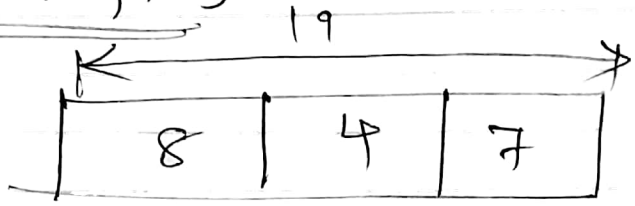
No. of tags = $\frac{\text{mm size}}{\text{Cache size}}$

$= \frac{2^{19}}{2^{13}} = 2^6$

2) Associative mapping :



3) Set Associative mapping :



$$\text{No. of Sets} = \frac{\text{No. of lines}}{\text{Set size}}$$

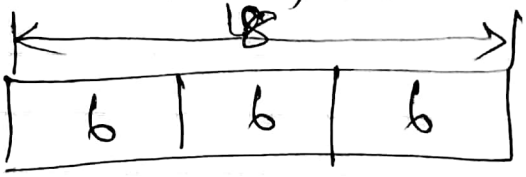
$$= \frac{2^6}{4\text{-way}}$$

$$= \frac{2^6}{2^2} = 2^4 \text{ sets}$$

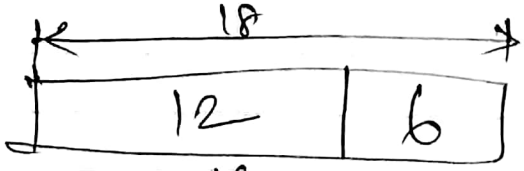
[OR]

if representation in word addressable formate

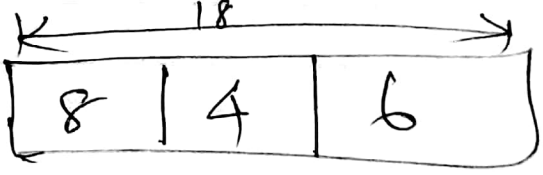
1) Direct mapping



2) Associative mapping



3) Set-Associative mapping



13). Page table — 5 marks

TLB — 5 marks

14) i) DMA → 5 marks

ii) Interrupts → 5 marks.

CO

18CSR166

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SSK	19.8.19
Name and signature of Hall Supdt. with Date	

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Estd : 1984

Name of the Student	S.SAKTHIPRASANNA	Register No.	1	8	C	S	R	1	6	6
Programme	BE	Branch & Semester	Computer Science III							
Course Code and Name	18CST32 Computer Organization	Date	19.08.2019			No.of Pages Used		7.		

MARKS TO BE FILLED IN BY THE EXAMINER

PART - A		PART - B			Grand Total Max. Marks : 50
Question No.	Max Marks : 2	Question No.		Max Marks : 10	
1	0	11	i)	2	24
2	0		ii)	0	
3	0	12	i)		
4	0		ii)		
5	-	13	i)	0	
6	2		ii)	0	
7	0	14	i)	0	
8	0		ii)		
9	0				
10	0				
TOTAL	2	TOTAL		2	

Verified
S.sakthiprasanna

Total marks in words : Zero Four

INSTRUCTION TO THE CANDIDATE

1. Check the Question Paper, Programme, Course Code, Branch Name etc., before answering the questions.
2. Use both sides of the paper for answering questions.
3. POSSESSION OF ANY INCRIMINATING MATERIAL AND MALPRACTICE OF ANY NATURE IS PUNISHABLE AS PER RULES.

Name of the Examiner

Signature of the Examiner with Date

PART-A

1) 2,4

0010 0100

1 1

0110 0101

-2, =4

=0110 0101.

2) 4 3

0100 0011

(-)1

1110 0001

+4 =1110 3 = 0001

43 = 0101.

3) The 8bit that the representation of 2 would require

0100

(-)1

0110

4) Array
Loops
pointers
Constants

5) $C_n \oplus C_{n-1}$

$= 0 \oplus 0 \; 1 \; 0$

$= 0 \; 0 \; 0 \; 1 \; 0$

$0 + 1 \quad 1$

6) A = 1 1 1 1 1 0 1 0

B = 0 0 0 0 1 0 1 0

1 1 1 1 1 0 1 0

0 0 0 0 1 0 1 0

1 1 1 1 1 0 1 0

0 1 1 1 1 0 0 1 1

$= 0 \; 1 \; 1 \; 1 \; 1 \quad 0 \; 0 \; 1 \; 1$

7) $b(n-1)-1$

$= 0 \; 1 \; 1 \; 0 \; (b-1)-1$

$= 0 \; 1 \; 1 \; 0 \; (5)-1$

$= 0 \; 0 \; 1 \; 1 \; 1 \; 0 \; 0 \; 1$

8 4 2 1

Booth algorithm - 4.

9) There 3 (3-2) reduction levels
are needed to reduce 16
Summands 2

0 0 1 0
0 0 1 0
0 0 1 1

0 0 1 1 0 0 1 0
0 0 1 1 0 0 1 0
0 0 1 1 0 0 0 0
0 0 1 0 0 0 0 0
0 0 1 1 0 0 0 0
0 1 0 0 0 0 1 0
0 1 0 0 0 0 1 0
0 0 0 1 0 1 0 0
0 1 0 1 0 1 1 0

10 1 1 0 1 1 0 1 1

0 0 1 0 0 0 1 0

0 1 1 0 1 1 0 0 1

0 1 1 0 0 1 0 1 0

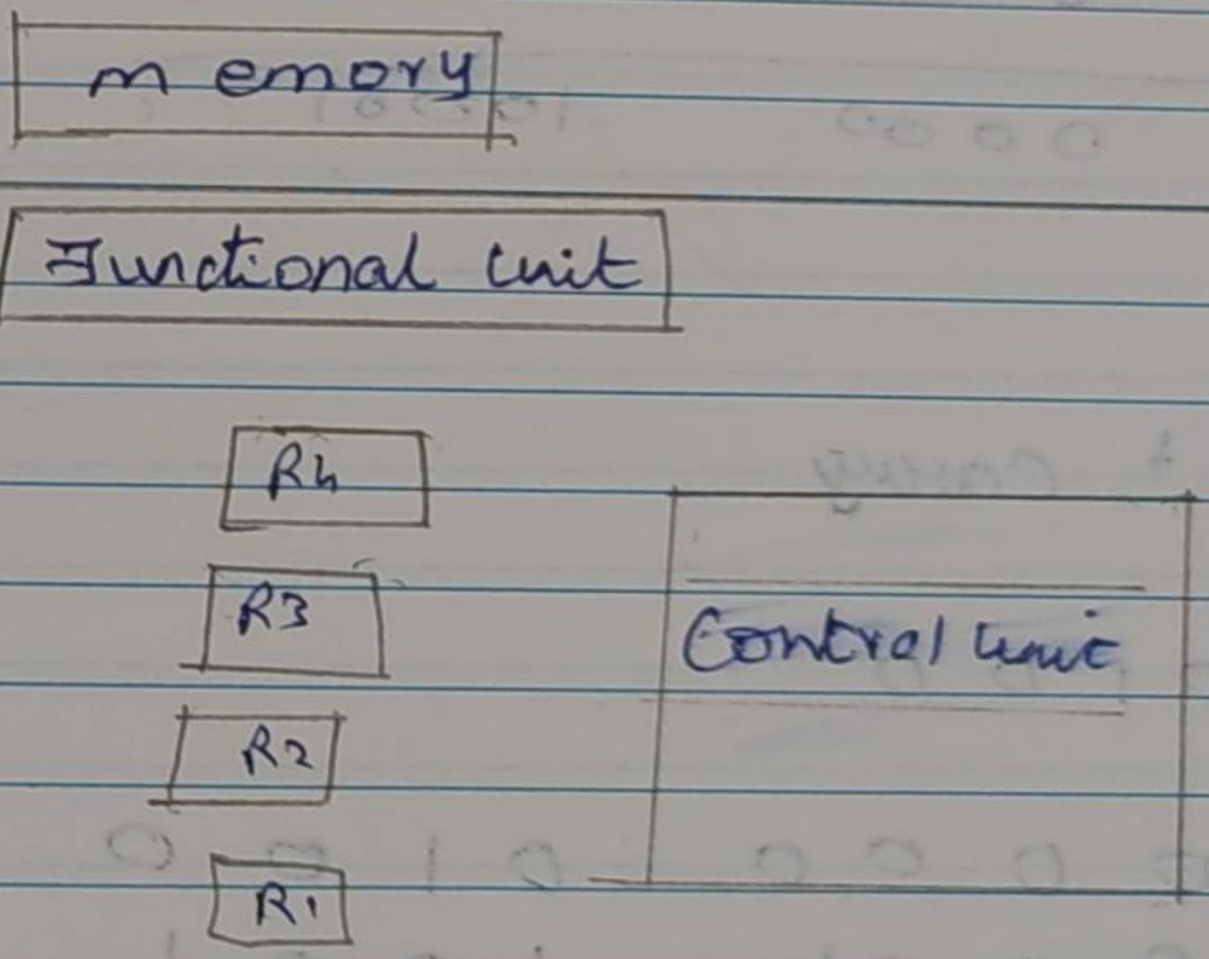
0 0 0 1 1 0 1 1

0 1 0 0 1 1 0 1 0

0 0 0 1 1 0 1 1

PART - B

(i)



(ii)

a) 7 and 9

0 1 1 1 1 0 0 1

1

0 1 1 1 1 0 0 1

0 1 0 1 1 0 1 0

0 1 1 0 0 1 1 1

0 0 0 1 0 1 0 0

0 1 1 1 1 0 1 0

0 0 0 0 0 0 1 0

1 1 1 1 0 0 0 1

0 0 0 1 1 0 0 1

0 0 0 0 1 0 0 0 1

13)

(i) 4 bit carry

0 1 0 0

0 0 0 0 0 1 0 0

0 0 0 1 1 0 0 1

0 0 0 1 1 1 0 1

0 0 0 0 0 0 0 0

0 0 0 1 1 1 0 1

0 1 0 0 0 0 0 1

0 1 0 1 1 0 0 1

1.1 n-1.

ii) 4 5

0 1 0 0

0 1 1 1

1 0 1 0

0 1 0 1

1 0 0 1

0 1 1 1

1 0 1 0

0 1 0 1

1 0 0 1

1 1 1 0

1 1 0 1

4)

A = 0 1 0 1 1 1

B = 1 1 0 1 1 0