	KONGU ENGINEERING COLLEGE PERUNDURAI ERODE - 638 060 (Autonomous)	AC- 04 T Revision -1
Estd : 1984	**COURSE PLAN - THEORY COURSE**	IQAC

Name of the Faculty, Designation & Dept.	Ms.Dr.S.Malliga, Professor/CSE	**Programme & Department of the Students**	BE/CSE
Course Code & Name	18CST32Computer Organization	**Academic Year, Semester & Section**	2019-20, III Sem & C Section

1. COURSE OUTCOMES

On completion of the course, the students will be able to		BT Level
CO1	Describe the basic structure, arithmetic and memory operations of a digital computer and determine the addressing modes for the set of instructions	K3
CO2	Describe and apply algorithms for performing different arithmetic operations.	K3
CO3	Make use of the data path in a processor to write the sequence of steps to fetch and execute a given instruction and apply the concepts of pipelining to determine and handle the hazards	K3
CO4	Distinguish between different types of memory and apply the mapping functions between main memory and cache	K3
CO5	Outline the need for and type of interrupts in I/O transfer and the role of different types of bus in I/O operations.	K2

Mapping of COs with POs, PSOs

COs / POs & PSOs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	2	1										2	1
CO2	3	2	1										2	2
CO3	3	2	1										2	1
CO4	3	2	1										2	1
CO5	2	1											1	

1 – Slight, 2 – Moderate, 3 – Substantial

2. COURSE PLAN

S. No.	Intended learning Outcomes	CO(s) Mapped	BT Level	TLM	Planned		Actual	
					Date	Period	Date	Period
1.	ILO1.1: Explain the working of the functional units of a digital computer	CO1	K2	M1	02.07.2019	2	2/7/19	2
2.	ILO1.2: Show the connections between the processor and memory	CO1	K1	M1	02.07.2019	6	2/7/19	6
3.	ILO1.3: Summarize the different number representation and mention the importance of 2's complement representation	CO1	K3		04.07.2019	7	4/7/19	7
4.	ILO1.4 Explain addition and subtraction of signed and unsigned integers	CO1	K3	M1	08.07.2019	1	8/7/19	1
5.	ILO1.5: Identify the issues related to the performance of a digital computer system	CO1	K2	M1	09.07.2019	2	9/7/19	2
6.	ILO1.6: Summarize the accessing mechanism of memory and byte addressability techniques used in a computer system	CO1	K2	M1	09.07.2019	6	9/7/19	6
7.	ILO1.7: Represent a given HLL instruction in assembly language instructions	CO1	K3	M1	11.07.2019	1	11/7/19	7
8.	ILO1.8: Explain the execution of an assembly language program which involves straight-line and branching instructions	CO1	K3	M1	15.07.2019	1	15/7/19	1
9.	ILO1.9: Describe the general addressing modes supported by a processor and identify the addressing mode in a given instruction	CO1	K3	M1	16.07.2019	2	16/7/19	6
10.	ILO1.9: Describe the general addressing modes supported by a processor and identify the addressing mode in a given instruction	CO1	K3	M1	16.07.2019	6	18/7/19	7

11.	ILO1.10: Explain the instruction sets of CISC	CO1	K2	M1	18.07.2019	7	22/7/19	1
12.	ILO1.11: Outline the difference between the characteristics of RISC and CISC	CO1	K2	M1	22.07.2019	1	23/7/19	2
13.	ILO2.1: Represent binary, signed-integer using sign and magnitude, 1's complement and 2's complement number system	CO2	K2	M1	23.07.2019	2	23/7/19	6
14.	ILO2.2: Describe the logic for addition and subtraction of signed numbers	CO2	K2	M6	23.07.2019	6	25/7/19	7
15.	ILO2.3: Summarize the technique used by carry-look ahead addition for fast addition	CO2	K2	M6	25.07.2019	7	29/7/19	1
16.	ILO2.4: Explain the methods used for multiplication of unsigned numbers	CO2	K2	M1	29.07.2019	1	30/7/19	2
17.	ILO2.5: Apply Booth algorithm for multiplication of signed numbers	CO2	K3	M1	30.07.2019	2	30/7/19	6
18.	ILO2.6: Identify the techniques used for speeding up the multiplication operation and solve the given multiplication problems	CO2	K3	M1	30.07.2019	6	1/8/19	1
19.	ILO2.7: Classify and Solve integer division using different methods	CO2	K3	M1	01.08.2019	7	1/8/19	7
20.	ILO2.8: Illustrate the IEEE standard for representing floating-point numbers in single and double-precision format	CO2	K2	M1	05.08.2019	1	6/8/19	2
21.	ILO2.9: Summarize the rules for performing arithmetic operations on floating-point numbers and solve the same with examples	CO2	K3	M1	06.08.2019	2	6/8/19	6
22.	ILO3.1: Illustrate the functional units of a processor and how they are interconnected.	CO3	K2	M1, M6	06.08.2019	6	8/8/19	2
23.	ILO3.2: Examine the actions involved in fetching and executing instructions and illustrate these actions using RISC style instructions.	CO3	K4, K2	M1	08.08.2019	7	13/8/19	2
24.	ILO3.3: Examine the components of a processor to see how they may be organized in the multi-stage structure.	CO3	K4, K2	M1	13.08.2019	2	13/8/19	6
25.	ILO3.4: Examine the process of fetching and executing instructions in more detail, using the datapath in a processor.	CO3	K4	M1	13.08.2019	6	20/8/19	2
26.	ILO3.5: Outline the signals needed to control the operation of the components in a processor.	CO3	K2	M1	13.08.2019	6	20/8/19	6
27.	ILO3.6: Examine how the processor generates the control signals that cause these actions to take place in the correct sequence using hardwired control.	CO3	K4	M1	20.08.2019	2	22/8/19	7
28.	ILO3.7: Illustrate the organization of a CISC – style processor with interconnect block.	CO3	K2	M1	20.08.2019	6	26/8/19	4
29.	ILO3.8: Explain the basics of pipelining and show how the five – stage organization of a processor can be pipelined.	CO3	K2,K1	M1, M3,M5	22.08.2019	7	27/8/19	2
30.	ILO3.9: Classify the pipeline hazards along with techniques to mitigate their impact on performance.	CO3	K2	M1,M3	26.08.2019	1	27/8/19	6
31.	ILO4.1: Describe the connection between the memory and processor	CO4	K1	M1,M3	27.08.2019	2	29/8/19	7
32.	ILO4.2: Explain the internal organization of memory chips and the execution of read/write operation	CO4	K2	M1	27.08.2019	8	3/9/19	2
33.	ILO4.3: Recall the structure/organization of a static RAM cell and identify the number of static memory chips required to build a large memory module	CO4	K3	M1	29.08.2019	7	3/9/19	6
34.	ILO4.4: Outline the structure of a dynamic memory cell and how it retains its contents	CO4	K2	M1	03.09.2019	2	9/9/19	1
35.	ILO4.5: Compare the working logic between asynchronous and synchronous DRAMs	CO4	K2	M1	03.09.2019	6	10/9/19	6
36.	ILO4.6: Explain the working logic of a ROM cell and classify its types	CO4	K2	M1	05.09.2019	7	12/9/19	7

37.	ILO4.7: Recall the memory hierarchy and compare them on speed, size and cost	CO4	K1	M1,M3	12.09.2019	7	12/9/19	1
38.	ILO4.8: Rephrase the role of cache memory in improving the performance of a memory system in a computer	CO4	K2	M1, M3	16.09.2019	1	19/9/19	7
39.	ILO4.9: Illustrate the mapping of memory blocks onto cache memory using memory-mapping functions and solve the given mapping problem	CO4	K3	M1	17.09.2019	2	23/9/19	1
40.	ILO4.10: Describe how memory interleaving improves the performance of a computer system	CO4	K2	M1	19.09.2019	7	24/9	2,6
41.	ILO4.11: Explain the role of virtual memory in a computer system and virtual-memory address translation method for the translation from virtual addresses to physical addresses	CO4	K2	M1	23.09.2019	1	26/9	7
42.	ILO4.12: Classify the different types of secondary storage devices and describe their functions	CO4	K2	M1,M3	24.09.2019	2	30/9	1
43.	ILO5.1 Examine the various access methods of I/O device	CO5	K2	M1	26.09.2019	7	1/10	2
44.	ILO5.2 Illustrate the concepts of Interrupts	CO5	K2	M1	30.09.2019	1	4/10	6
45.	ILO5.3 Summarize the use of DMA controllers and the arbitration procedure to coordinate the transfer of data among the memory and I/O Devices.	CO5	K2	M1,M3	01.10.2019	2	3/10	7
46.	ILO5.4 Discuss and differentiate the synchronous and asynchronous bus.	CO5	K2	M1	03.10.2019	7	10/10	7
47.	ILO5.5 Recall the functions of I/O Interface	CO5	K1	M1	10.10.2019	7	14/10	1
48.	ILO5.6 Examine the different interface standards for a computer system	CO5	K2	M1	14.10.2019	1	15/10	2
49.	ILO5.7 Illustrate the operation of SCSI bus	CO5	K2	M1	17.10.2019	7	17/10 21/10	5,11
50.	ILO5.8 Explain the technical details and operations of USB	CO5	K2	M1	21.10.2019	1	22/10	2,6

3. Assessment Pattern

Mark Split up					Cognitive Process K Levels Distribution in Percentage					CO Distribution (%)					Proposed Date of Assessment
Sections/ Tests	Part -A	Part -B	Part -C	Total Marks	K1	K2	K3	K4	K5	CO1	CO2	CO3	CO4	CO5	
Test -1	20	65	15	100	10% to 20%	10% to 20%	40% to 60%			40%	40/%	20%			20.07.2019
Test -2	20	65	15	100	10% to 20%	10% to 20%	40% to 60%					20%	40/%	40%	23.10.2019
Assignment		20					100%				40%	20%	40%		01.10.2019
Other Assessment	20									20%	20%	20%	20%	20%	19.10.2019
Course Project	-	-													16.09.2019
ESE	20	65	15	100	10% to 20%	10% to 20%	40% to 60%			20%	20%	20%	20%	20%	11.11.2019

Course Faculty (S Mallya)

Course Coordinator (S Mallya)

HOD