S5KRD2YX

VGA Resolution Dynamic Vision Sensor

Revision 0.00

Apr. 2016

Data Sheet (Preliminary)

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Chip Handling Guide

Precaution against Electrostatic Discharge

When using semiconductor devices, ensure that the environment is protected against static electricity:

1. Wear antistatic clothes and use earth band.
2. All objects that are in direct contact with devices must be made up of materials that do not produce static electricity.
3. Ensure that the equipment and work table are earthed.
4. Use ionizer to remove electron charge.

Contamination

Do not use semiconductor products in an environment exposed to dust or dirt adhesion.

Temperature/Humidity

Semiconductor devices are sensitive to:

- Environment
- Temperature
- Humidity

High temperature or humidity deteriorates the characteristics of semiconductor devices. Therefore, do not store or use semiconductor devices in such conditions.

Mechanical Shock

Do not to apply excessive mechanical shock or force on semiconductor devices.

Chemical

Do not expose semiconductor devices to chemicals because exposure to chemicals leads to reactions that deteriorate the characteristics of the devices.

Light Protection

In non- Epoxy Molding Compound (EMC) package, do not expose semiconductor IC to bright light. Exposure to bright light causes malfunctioning of the devices. However, a few special products that utilize light or with security functions are exempted from this guide.

Radioactive, Cosmic and X-ray

Radioactive substances, cosmic ray, or X-ray may influence semiconductor devices. These substances or rays may cause a soft error during a device operation. Therefore, ensure to shield the semiconductor devices under environment that may be exposed to radioactive substances, cosmic ray, or X-ray.

EMS (Electromagnetic Susceptibility)

Strong electromagnetic wave or magnetic field may affect the characteristic of semiconductor devices during the operation under insufficient PCB circuit design for Electromagnetic Susceptibility (EMS).

Revision History

Revision No.	Date	Description	Author(s)
Preliminary	Apr. 18. 2016	• Preliminary draft for S5KRD2YX	J.-S. Kim

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List of Conventions

Register RW Access Type Conventions

Type	Definition	Description
R	Read Only	The application has permission to read the Register field. Writes to read-only fields have no effect.
W	Write Only	The application has permission to write in the Register field.
RW	Read & Write	The application has permission to read and writes in the Register field. The application sets this field by writing 1'b1 and clears it by writing 1'b0. The Register field is updated immediately.
RW1	Read & Write	The application has permission to read and writes in the Register field. The application sets this field by writing 1'b1 and clears it by writing 1'b0. The Register field is updated after 1 frame.
RWI2	Read & Write	The application has permission to read and writes in the Register field. The application sets this field by writing 1'b1 and clears it by writing 1'b0. The Register field is updated after 2 frames.

Register Value Conventions

Expression	Description
x	Undefined bit
X	Undefined multiple bits
?	Undefined, but depends on the device or pin status
Device dependent	The value depends on the device
Pin value	The value depends on the pin status

Reset Value Conventions

Expression	Description
0	Clears the register field
1	Sets the register field
x	Don't care condition

Warning: Some bits of control registers are driven by hardware or write operation only. As a result the indicated reset value and the read value after reset might be different.

List of Acronyms

Acronyms	Descriptions
VGA	Video Graphics Array
DVS	Dynamic Vision Sensor
AER	Address Event Representation
CIS	CMOS Image Sensor
FPGA	Flexible Programmable Gate Array
BSI	Back Side Illumination
APS	Active Pixel Sensor
PLL	Phase-Locked Loop
SPI	Serial Peripheral Interface
DDR	Double Data Rate

Preliminary product information describes products that are in development, for which full characterization data and associated errata are not yet available. Specifications and information herein are subject to change without notice.

1 Product Overview

1.1 Introduction

The S5KRD2YX is a Video Graphics Array (VGA) resolution pixel Dynamic Vision Sensor (DVS) chip that can detect a light-intensity change, which is called event. It was fabricated using the SAMSUNG 90nm back side illumination (BSI) CMOS Image Sensor (CIS) process. The sensor consists of 640 x 480 effective pixels with 9um pixel pitch. Then, this sensor meets 1/2.46-inch optical format.

DVS is an asynchronous event-based image sensor, which mimics the operating mechanism of a retina in the human eyes. A DVS pixel produces an ON or OFF event in response to relative change in the light intensity only when the degree of light variation is higher (ON event) or lower (OFF event) than pre-defined threshold levels. Otherwise it stays in a steady-state mode. DVS is an image sensor, but is different from a conventional frame-based CIS in terms of an operating methodology. A DVS pixel generates an event when it detects the change of light intensity and its corresponding X-Y coordinates are encoded through so-called an Address Event Representation (AER) circuitry. The information packet with a polarity (event type) and corresponding address (X-Y coordinates) is sent out to an event processing processor, which can be realized by an on-chip implementation or an off-chip commercial flexible programmable gate array (FPGA), In a four phase hand-shaking protocol. In S5KRD2YX, AER circuitry was realized by an on-chip implementation.

The S5KRD2YX has a bias circuitry to generate bias voltages for pixel operation, and digital circuitries for variable I/O interfaces, activity detection, image cropping, etc.

The S5KRD2YX responds much faster than standard CIS camera. Effective frame rate is more than 1,000 frames per second. Fast moving object and scene can be captured with blur-less clean edges.

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1.2 Features

- 0.31Mp sensor with 1/2.46"optics
- Pixel size: 9 μm
- VGA pixel resolution (Effective 640(H) x 480(V), total 644(H) x 484(V))
- Dynamic range: 90 dB (3~100,000 Lux)
- Minimum Contrast Sensitivity: 13%
- Pixel Response Latency: < 1msec
- Read-out speed: 50M Group Event Per Second (GEPS)
- Sub-sampling mode supported (Full/Half/Quarter/One-eighth)
- 32-bit packetized format:
  - Extracted via 16 output pads using Double Data Rate scheme (DDR) scheme
  - Column address including its sub-timestamp
  - Group address including its on/off events data
- Output Interfaces:
  - MIPI CSI-2 2-lane (Max. 1Gbps per lane)
  - Parallel 32-bit (Extracted via 16 output pads using DDR scheme)
  - Connectable to external USB3.0 interface chip (Cypress FX3)
- Control interface:
  - I2C – Two-wire serial communication circuit up to 400kHz
- Supply voltage: 2.8 V for pixel and bias, 3.3 V for I/O, 1.2 V for digital core supply
- Functional Operating temperature: – 30 °C to + 70 °C
- Backside illumination (BSI) structure

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1.3 Functional Block Diagram

The S5KRD2YX consists of pixel array, analog block including bias circuit, digital AER for group address and time stamp, activity detection, spatial histogram, cropper, packetizer, output MUX blocks, etc.

The block diagram of the sensor is shown in *Figure 1*.

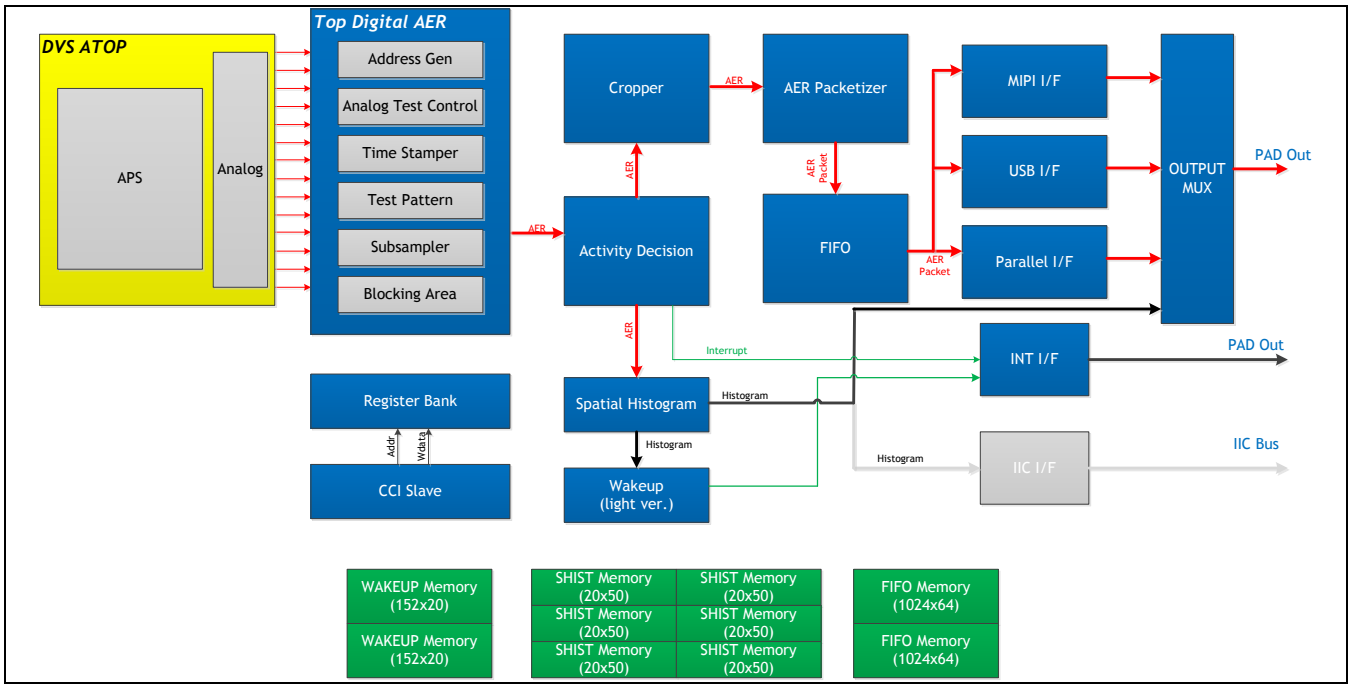

Figure 1 Functional Block Diagram (Top View)

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1.4 System State Diagram

The S5KRD2YX uses I2C as a control interface, which starts to be activated in sleep mode.

Table 1 System State Summary

Power State	Description
Power-off	Power supplies are turned off.
Hardware standby	RSTN is low. Power supplies are turned on but no communication with the sensor is possible. Internal registers are set to default values.
Sleep	RSTN is high. Register setting through I2C is possible.
Monitor	The sensor is partially functional (wakeup, histogram), but any event isn't be printed out.
Stream	The sensor is fully functional, and the event is printed out through Parallel, MIPI or USB I/F

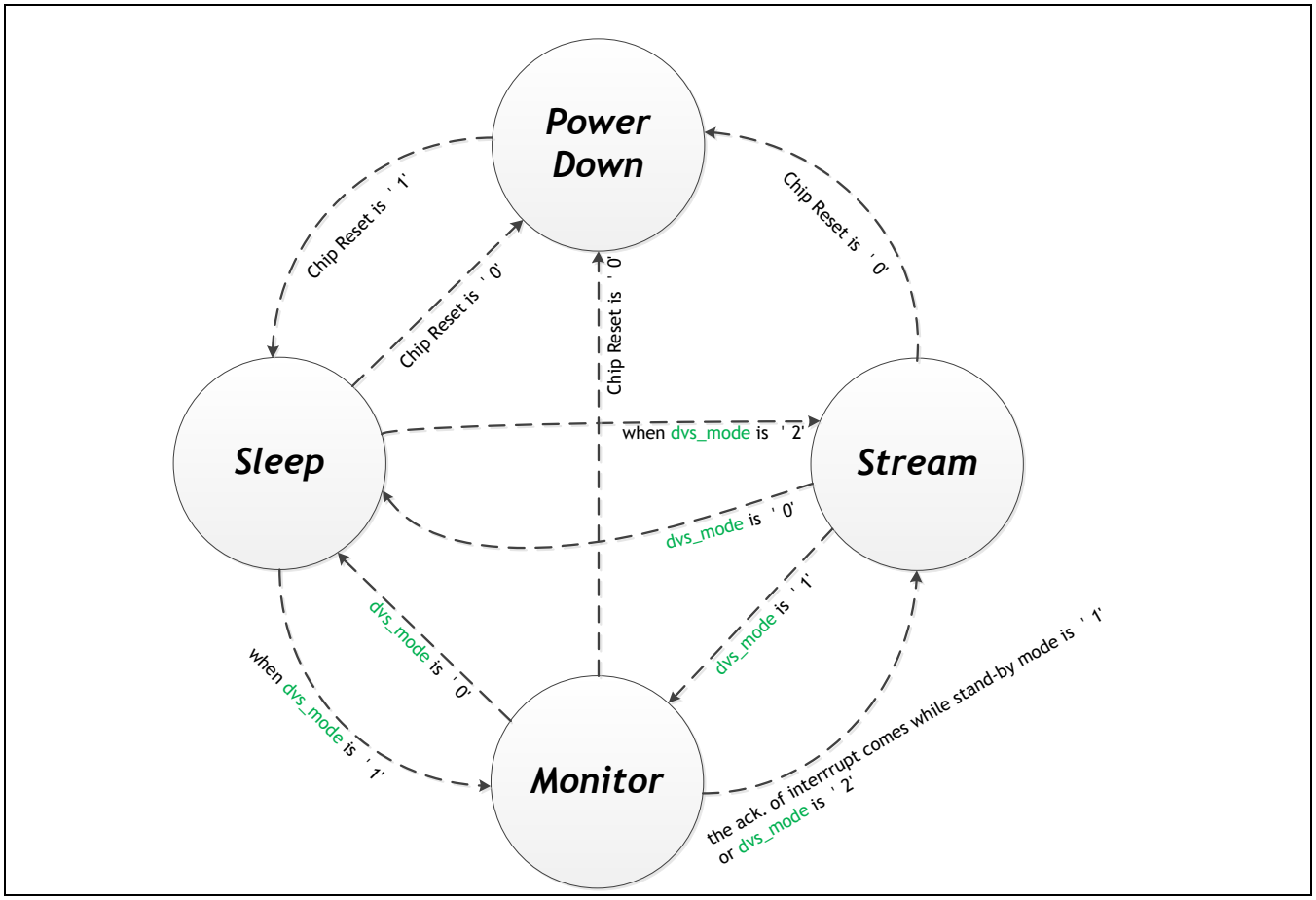

Figure 2 System State Diagram

Preliminary product information describes products that are in development, for which full characterization data and associated errata are not yet available. Specifications and information herein are subject to change without notice.

1.5 Simplified I/O Symbol Diagram

[Note] (I) Input, (O) Output, (OZ) Tri-state output, (IOZ) Tri-state IN/OUT, (OD) Open-Drain output, (IOD) Open-Drain IN/OUT, (P) Power & Ground, (A) Analog Test or Ext. cap. Node

Power & Ground	VDDAP	P	S5KRD2YX	OZ	Pvalid or FX3_ADDR0	Parallel or USB I/F
	VSSAP	P		OZ	Pclk or FX3_CLK	
	VDDA	P		OZ	Pdata[15:0] or FX3_DATA[15:0]	
	VSSA	P				
	VDDAD	P		IO	FX3_FULLA/B	USB control
	VSSAD	P		OZ	FX3_PKTEND	
	VDDD	P		OZ	FX3_SLWR	
	VSSD	P				
				OZ	INT_SHIST	Interrupt
Analog Test or Ext. Cap.	EXTBGSRC	A		OZ	INT_OUT	
	AMUX_IN	A		IO	INT_IN	
	AMUX_I1/I2	A				
	AMUX_V1/V2	A		OZ	DATAN[1:0]	MIPI
	DMUX_OUT0~10	A		OZ	DATAP[1:0]	
	PLL_FLT_PAD	A		OZ	CLKN	
				OZ	CLKP	
Master Clock	EXTCLK	I				
Sensor Control (from Host)	RSTN	I				
	SDA	I				
	SCL	I				

Figure 3 Simplified I/O Symbol Diagram

Preliminary product information describes products that are in development, for which full characterization data and associated errata are not yet available. Specifications and information herein are subject to change without notice.

1.6 Pin Configuration and Description

The S5KRD2YX can be assembled in COB or iBGA package.

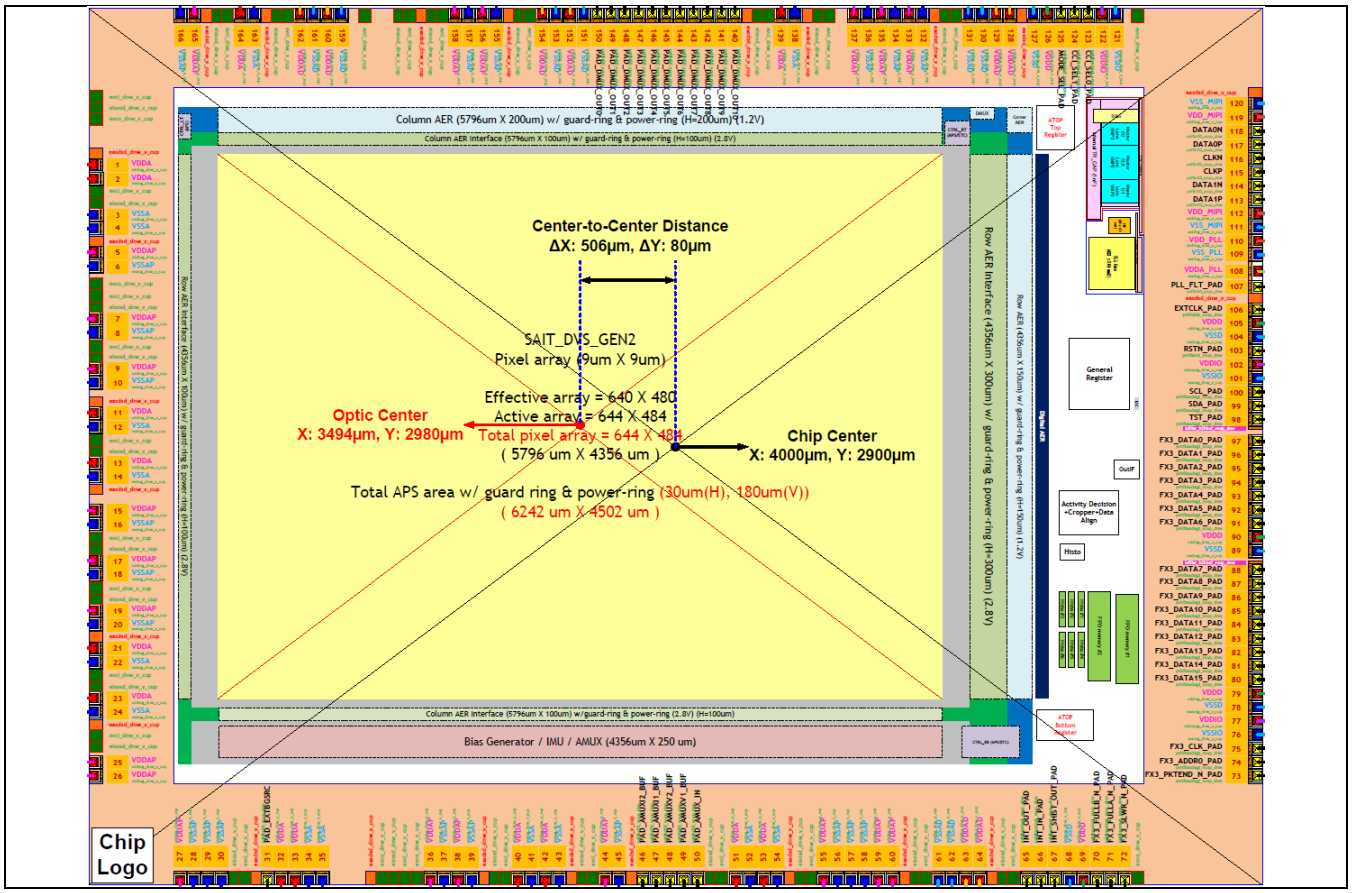

Figure 4 Die Pin Information

Table 2 Die Pin Descriptions

Pad No.	Type	Signal Name	Description
1	PWR	VDDA	Pixel Power (2.8V)
2	PWR	VDDA	Pixel Power (2.8V)
3	GND	VSSA	Pixel Ground
4	GND	VSSA	Pixel Ground
5	PWR	VDDAP	Interface Power (2.8V)
6	GND	VSSAP	Interface Ground
7	PWR	VDDAP	Interface Power (2.8V)
8	GND	VSSAP	Interface Ground
9	PWR	VDDAP	Interface Power (2.8V)
10	GND	VSSAP	Interface Ground

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Pad No.	Type	Signal Name	Description
11	PWR	VDDA	Pixel Power (2.8V)
12	GND	VSSA	Pixel Ground
13	PWR	VDDA	Pixel Power (2.8V)
14	GND	VSSA	Pixel Ground
15	PWR	VDDAP	Interface Power (2.8V)
16	GND	VSSAP	Interface Ground
17	PWR	VDDAP	Interface Power (2.8V)
18	GND	VSSAP	Interface Ground
19	PWR	VDDAP	Interface Power (2.8V)
20	GND	VSSAP	Interface Ground
21	PWR	VDDA	Pixel Power (2.8V)
22	GND	VSSA	Pixel Ground
23	PWR	VDDA	Pixel Power (2.8V)
24	GND	VSSA	Pixel Ground
25	PWR	VDDAP	Interface Power (2.8V)
26	PWR	VDDAP	Interface Power (2.8V)
27	PWR	VDDAP	Interface Power (2.8V)
28	GND	VSSAP	Interface Ground
29	GND	VSSAP	Interface Ground
30	GND	VSSAP	Interface Ground
31	BI	PAD_EXTBGRSRC	External Bandgap Ref. Current Source
32	PWR	VDDA	Pixel Power (2.8V)
33	PWR	VDDA	Pixel Power (2.8V)
34	GND	VSSA	Pixel Ground
35	GND	VSSA	Pixel Ground
36	PWR	VDDAP	Interface Power (2.8V)
37	GND	VSSAP	Interface Ground
38	PWR	VDDAP	Interface Power (2.8V)
39	GND	VSSAP	Interface Ground
40	PWR	VDDA	Pixel Power (2.8V)
41	GND	VSSA	Pixel Ground
42	PWR	VDDA	Pixel Power (2.8V)
43	GND	VSSA	Pixel Ground
44	PWR	VDDAP	Interface Power (2.8V)
45	GND	VSSAP	Interface Ground
46	OUT	PAD_AMUXI2_BUF	ATOP Mux Current Output

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Pad No.	Type	Signal Name	Description
47	OUT	PAD_AMUXI1_BUF	ATOP Mux Current Output
48	OUT	PAD_AMUXV2_BUF	ATOP Mux Voltage Output
49	OUT	PAD_AMUXV1_BUF	ATOP Mux Voltage Output
50	IN	PAD_AMUX_IN	ATOP Mux I/V Input
51	PWR	VDDA	Pixel Power (2.8V)
52	GND	VSSA	Pixel Ground
53	PWR	VDDA	Pixel Power (2.8V)
54	GND	VSSA	Pixel Ground
55	PWR	VDDAP	Interface Power (2.8V)
56	GND	VSSAP	Interface Ground
57	GND	VSSAP	Interface Ground
58	GND	VSSAP	Interface Ground
59	PWR	VDDAP	Interface Power (2.8V)
60	PWR	VDDAP	Interface Power (2.8V)
61	GND	VSSAD	AER Logic Ground
62	GND	VSSAD	AER Logic Ground
63	PWR	VDDAD	AER Logic Power (1.2V)
64	PWR	VDDAD	AER Logic Power (1.2V)
65	BI	INT_OUT_PAD	Interrupt Out
66	IN	INT_IN_PAD	Interrupt In
67	BI	INT_SHIST_OUT_PAD	Interrupt Special Histogram Out
68	GND	VSSD	Digital Ground
69	PWR	VDDD	Digital Power (1.2V)
70	IN	FX3_FULLB_N_PAD	FX3 Full B
71	IN	FX3_FULLA_N_PAD	FX3 Full A
72	BI	FX3_SLWR_N_PAD	FX3 SLWR
73	BI	FX3_PKTEND_N_PAD	FX3 Packet End
74	BI	FX3_ADDR0_PAD	FX3 ADDR[0]
75	BI	FX3_CLK_PAD	FX3 Clock
76	GND	VSSIO	PAD I/O Ground
77	PWR	VDDIO	PAD I/O Power (3.3V)
78	GND	VSSD	Digital Ground
79	PWR	VDDD	Digital Power (1.2V)
80	BI	FX3_DATA15_PAD	FX3 DATA [15]
81	BI	FX3_DATA14_PAD	FX3 DATA [14]
82	BI	FX3_DATA13_PAD	FX3 DATA [13]

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Pad No.	Type	Signal Name	Description
83	BI	FX3_DATA12_PAD	FX3 DATA [12]
84	BI	FX3_DATA11_PAD	FX3 DATA [11]
85	BI	FX3_DATA10_PAD	FX3 DATA [10]
86	BI	FX3_DATA9_PAD	FX3 DATA [9]
87	BI	FX3_DATA8_PAD	FX3 DATA [8]
88	BI	FX3_DATA7_PAD	FX3 DATA [7]
89	GND	VSSD	Digital Ground
90	PWR	VDDD	Digital Power (1.2V)
91	BI	FX3_DATA6_PAD	FX3 DATA [6]
92	BI	FX3_DATA5_PAD	FX3 DATA [5]
93	BI	FX3_DATA4_PAD	FX3 DATA [4]
94	BI	FX3_DATA3_PAD	FX3 DATA [3]
95	BI	FX3_DATA2_PAD	FX3 DATA [2]
96	BI	FX3_DATA1_PAD	FX3 DATA [1]
97	BI	FX3_DATA0_PAD	FX3 DATA [0]
98	IN	TST_PAD	Test Mode Selection PAD
99	BI	SDA_PAD	I2C Data PAD
100	IN	SCL_PAD	I2C Clock PAD
101	GND	VSSIO	PAD I/O Ground
102	PWR	VDDIO	PAD I/O Power (3.3V)
103	IN	RSTN_PAD	Reset (Active Low)
104	GND	VSSD	Digital Ground
105	PWR	VDDD	Digital Power (1.2V)
106	IN	EXTCLK_PAD	External Clock
107	OUT	PLL_FLT_PAD	PLL Monitoring Signal
108	PWR	VDDA_PLL	Digital PLL Power (2.8V)
109	GND	VSS_PLL	Digital PLL Ground
110	PWR	VDD_PLL	Digital PLL Power (1.2V)
111	GND	VSS_MIPI	Digital MIPI Ground
112	PWR	VDD_MIPI	Digital MIPI Power (1.2V)
113	OUT	DATA1P	MIPI Data Lane1 Positive
114	OUT	DATA1N	MIPI Data Lane1 Negative
115	OUT	CLKP	MIPI Clock Positive
116	OUT	CLKN	MIPI Clock Negative
117	OUT	DATA0P	MIPI Data Lane0 Positive
118	OUT	DATA0N	MIPI Data Lane0 Negative

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Pad No.	Type	Signal Name	Description
119	PWR	VDD_MIPI	Digital MIPI Power (1.2V)
120	GND	VSS_MIPI	Digital MIPI Ground
121	GND	VSSIO	PAD I/O Ground
122	PWR	VDDIO	PAD I/O Power (3.3V)
123	IN	CCI_SEL0_PAD	CCI Selection 0
124	IN	CCI_SEL1_PAD	CCI Selection 1
125	IN	MODE_SEL_PAD	Mode Selection
126	PWR	VDDD	Digital Power (1.2V)
127	GND	VSSD	Digital Ground
128	PWR	VDDAD	ATOP Logic Power (1.2V)
129	PWR	VDDAD	ATOP Logic Power (1.2V)
130	GND	VSSAD	ATOP Logic Ground
131	GND	VSSAD	ATOP Logic Ground
132	GND	VSSAP	Interface Ground
133	PWR	VDDAP	Interface Power (2.8V)
134	GND	VSSAP	Interface Ground
135	PWR	VDDAP	Interface Power (2.8V)
136	GND	VSSAP	Interface Ground
137	PWR	VDDAP	Interface Power (2.8V)
138	GND	VSSA	Pixel Ground
139	PWR	VDDA	Pixel Power (2.8V)
140	OUT	PAD_DMUX_OUT10	ATOP Logic Signal MUX
141	OUT	PAD_DMUX_OUT9	ATOP Logic Signal MUX
142	OUT	PAD_DMUX_OUT8	ATOP Logic Signal MUX
143	OUT	PAD_DMUX_OUT7	ATOP Logic Signal MUX
144	OUT	PAD_DMUX_OUT6	ATOP Logic Signal MUX
145	OUT	PAD_DMUX_OUT5	ATOP Logic Signal MUX
146	OUT	PAD_DMUX_OUT4	ATOP Logic Signal MUX
147	OUT	PAD_DMUX_OUT3	ATOP Logic Signal MUX
148	OUT	PAD_DMUX_OUT2	ATOP Logic Signal MUX
149	OUT	PAD_DMUX_OUT1	ATOP Logic Signal MUX
150	OUT	PAD_DMUX_OUT0	ATOP Logic Signal MUX
151	GND	VSSAD	ATOP Logic Ground
152	PWR	VDDAD	ATOP Logic Power (1.2V)
153	GND	VSSAD	ATOP Logic Ground
154	PWR	VDDAD	ATOP Logic Power (1.2V)

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Pad No.	Type	Signal Name	Description
155	GND	VSSAP	Interface Ground
156	PWR	VDDAP	Interface Power (2.8V)
157	GND	VSSAP	Interface Ground
158	PWR	VDDAP	Interface Power (2.8V)
159	GND	VSSAD	ATOP Logic Ground
160	PWR	VDDAD	ATOP Logic Power (1.2V)
161	GND	VSSAD	ATOP Logic Ground
162	PWR	VDDAD	ATOP Logic Power (1.2V)
163	GND	VSSA	Pixel Ground
164	PWR	VDDA	Pixel Power (2.8V)
165	PWR	VDDAP	Interface Power (2.8V)
166	GND	VSSAP	Interface Ground

1.7 Recommended Application Circuit

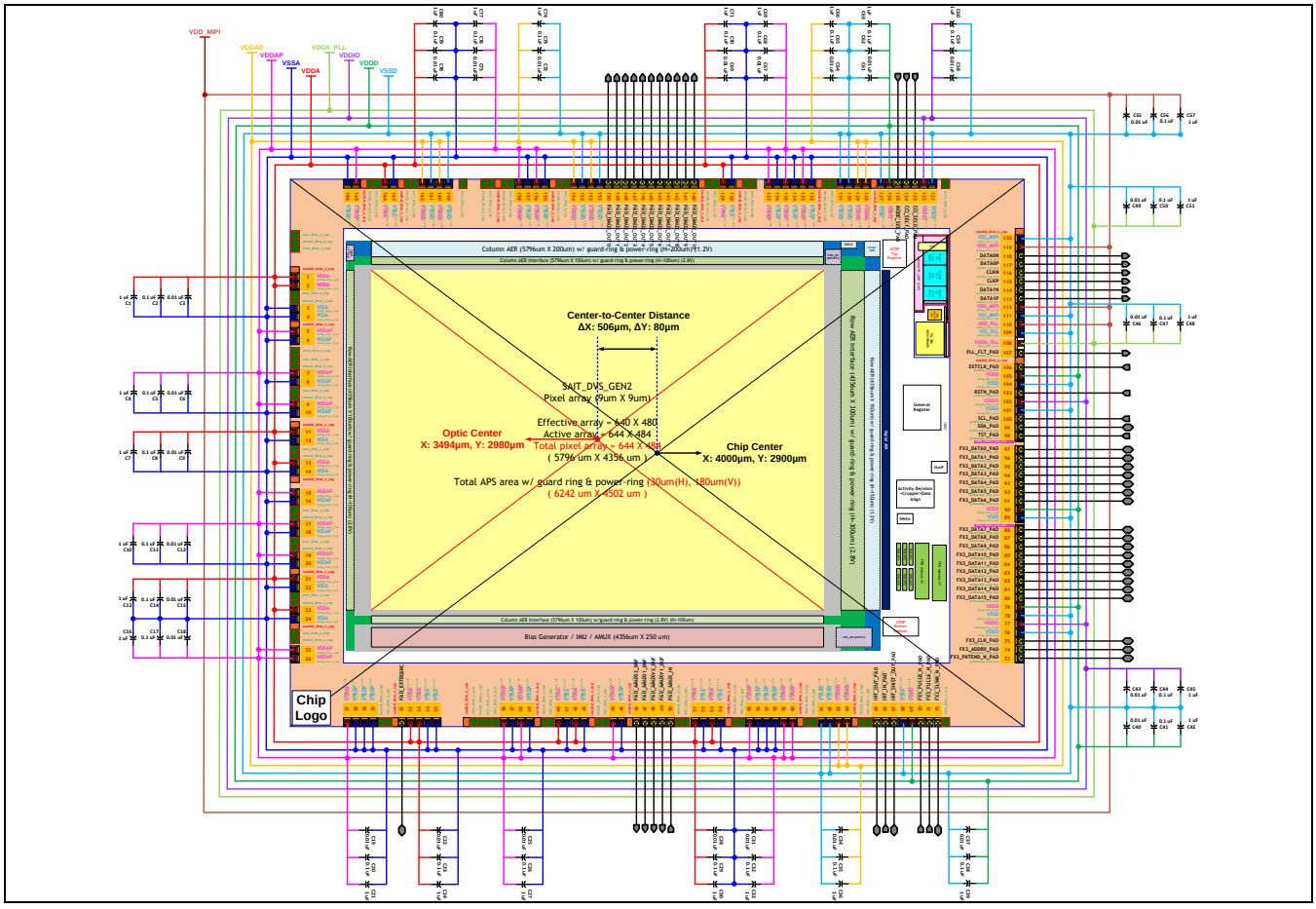

Figure 5 Application Circuit of Die

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2 Physical Dimension

2.1 Chip Dimension

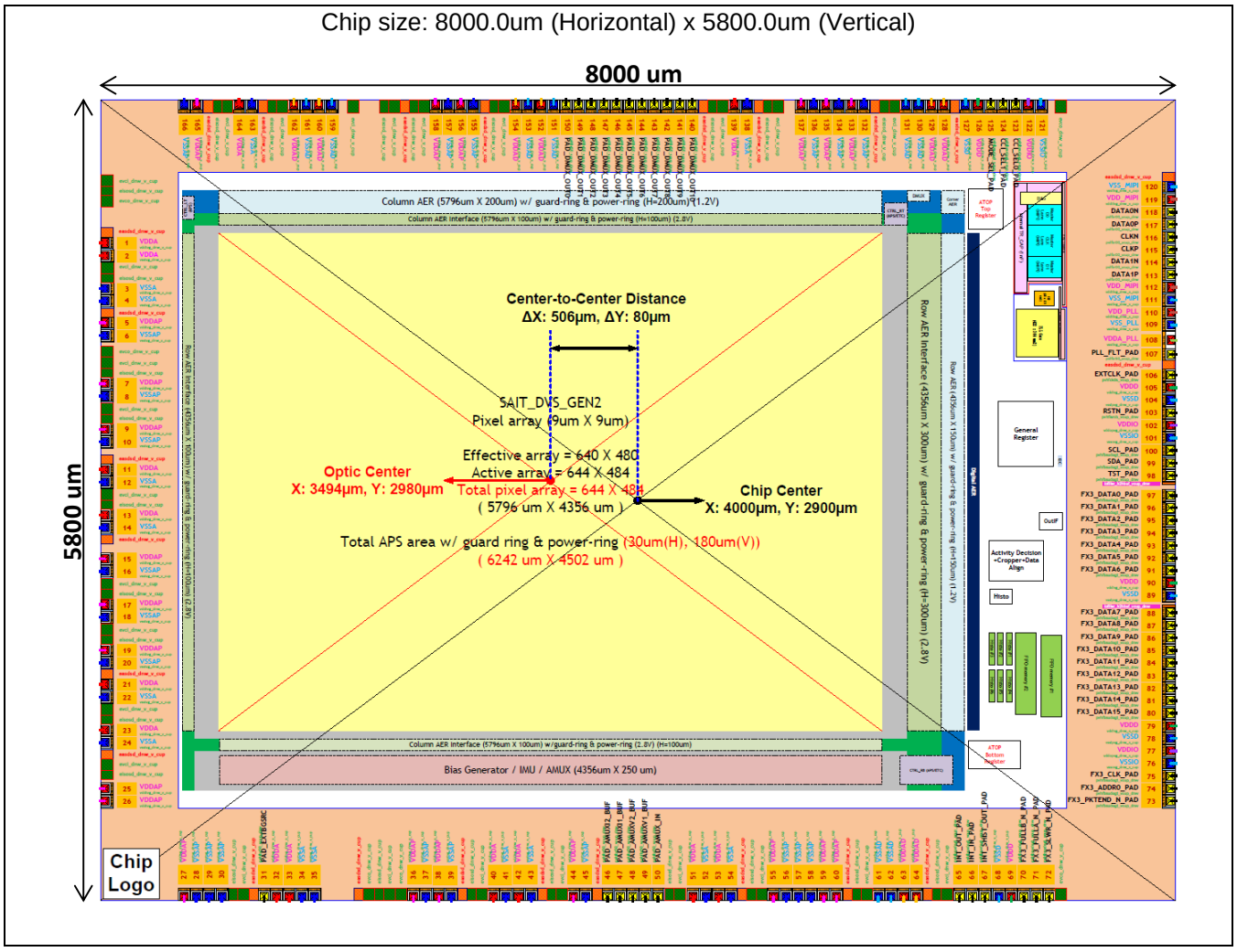


Figure 6 Chip Dimension

NOTE: Top view on chip.

Preliminary product information describes products that are in development, for which full characterization data and associated errata are not yet available. Specifications and information herein are subject to change without notice.

2.2 Module Dimension (To be updated)

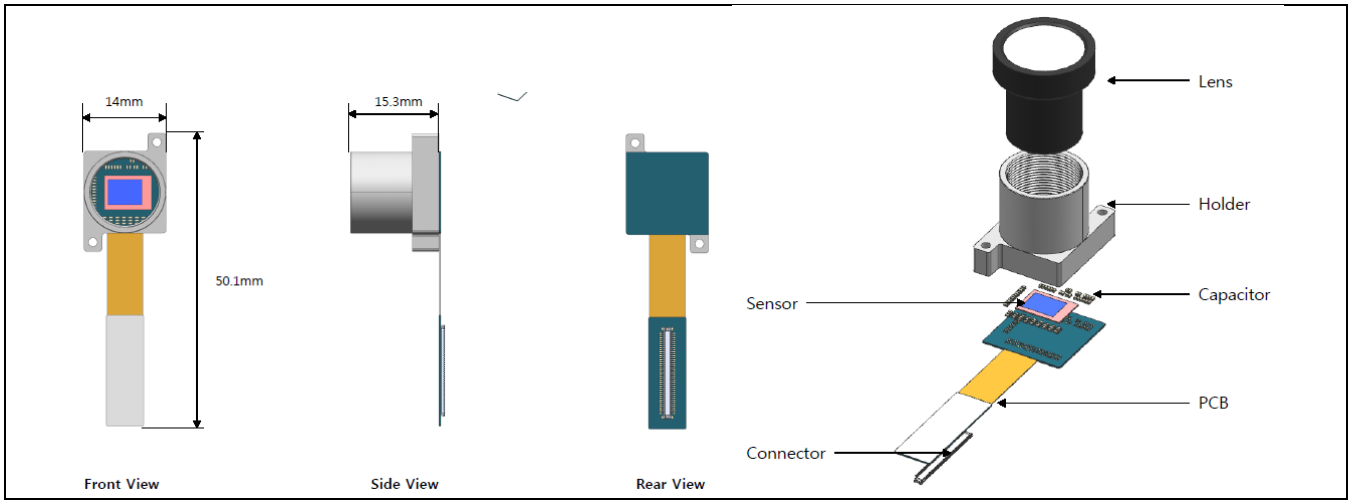


Figure 7 COB Package for test & evaluation

Preliminary product information describes products that are in development, for which full characterization data and associated errata are not yet available. Specifications and information herein are subject to change without notice.

3 Control Interface

3.1 I2C

The S5KRD2YX supports the I2C communication method which is the 2-wired serial interface between a backend processor (host) and a sensor to control the register values. The details are described below.

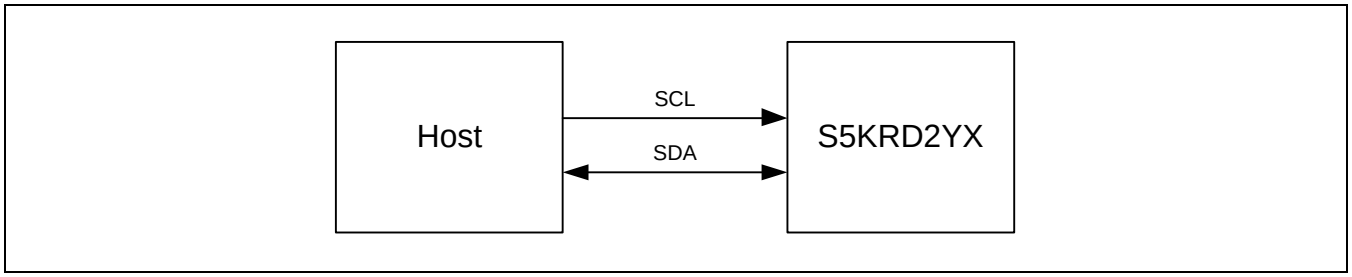


Figure 8 I2C Control Interface

The following table describes I2C signals:

Table 3 I2C Pin description

Pin Name	Description
SCL	Serial communication clock
SDA	Serial communication data

Preliminary product information describes products that are in development, for which full characterization data and associated errata are not yet available. Specifications and information herein are subject to change without notice.

3.2 Camera Control Interface (CCI)

S5KRD2YX supports the Camera Control Interface (CCI), which is an I2C fast-mode compatible interface for controlling the transmitter. S5KRD2YX always acts as a slave in the CCI bus. CCI is capable of handling several slaves in the bus, but multi-master mode is not supported. Typically, only the receiver and transmitter are connected to the CCI bus. This makes a pure SW implementation possible.

Typically the CCI is separate from the system I2C bus, but I2C-compatibility ensures that it is also possible to connect the transmitter to the system I2C bus. CCI is a subset of the I2C protocol, including the minimum combination of obligatory features for the I2C slave device specified in the I2C specification. Therefore, transmitters complying with the CCI specification can also be connected to the system I2C bus. However, it is important to ensure that the I2C masters do not try to utilize these I2C features, which are not supported in transmitters complying with the CCI specification. Each transmitter conformed to the CCI specification may have additional features implemented to support I2C.

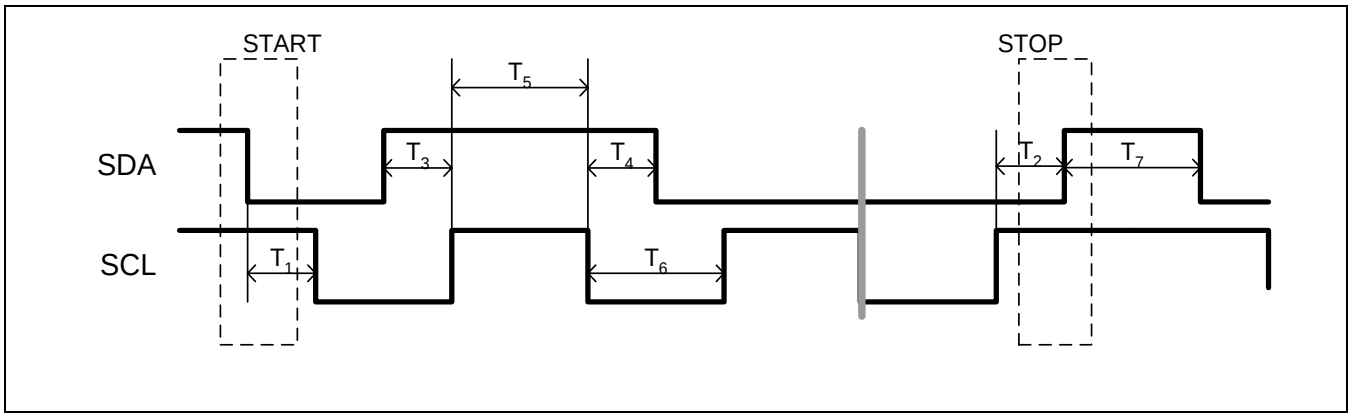


Figure 9 CCI Timing Diagram

Table 4 I2C Standard Mode Timing Specifications

Parameter	Symbol	Min.	Max.	Unit
SCL clock frequency	–	0	100	kHz
Hold time for START condition	T_1	4.0	–	µs
Setup time for STOP condition	T_2	4.0	–	
Data setup time	T_3	250	–	ns
Data hold time	T_4	0	3.45	µs
High period of the SCL clock	T_5	4.0	–	
Low period of the SCL clock	T_6	4.7	–	
Bus free time between STOP and START conditions	T_7	4.7	–	
Rise time for both SDA and SCL signals	–	–	1000	ns
Fall time for both SDA and SCL signals	–	–	300	
Capacitive load for each bus line	CB	–	400	pF

Preliminary product information describes products that are in development, for which full characterization data and associated errata are not yet available. Specifications and information herein are subject to change without notice.

Table 5 I2C Fast Mode Timing Specifications

Parameter	Symbol	Min.	Max.	Unit
SCL clock frequency	–	0	400	kHz
Hold time for start condition	T_1	0.6	–	µs
Setup time for stop condition	T_2	0.6	–	
Data setup time, external clock (MCLK) above 12.8MHz	T_3	0.1	–	µs
Data setup time, external clock (MCLK) below 12.8MHz		0.6	–	
Data hold time	T_4	0	0.9	µs
High period of the SCL clock	T_5	0.6	–	
Low period of the SCL clock	T_6	1.3	–	
Bus free time between stop and start conditions	T_7	1.3	–	
Rise time for both SDA and SCL signals	–	–	300	ns
Fall time for both SDA and SCL signals	–	–	300	
Capacitive load for each bus line	CB	–	400	pF

NOTE: Fast mode can be supported with T3 > 0.1usec, above –12.8 MHz external clock (MCLK).

Preliminary product information describes products that are in development, for which full characterization data and associated errata are not yet available. Specifications and information herein are subject to change without notice.

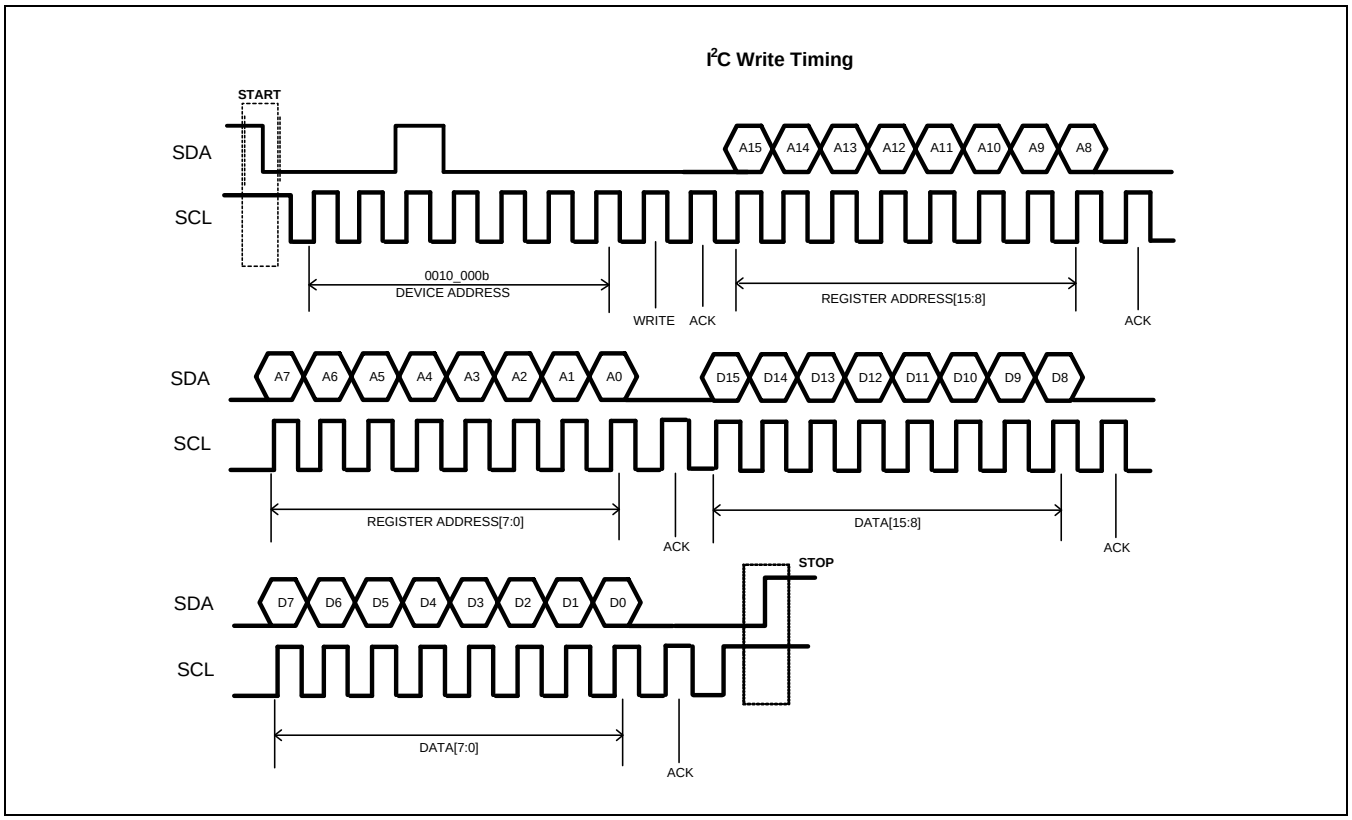


Figure 10 I2C Write Timing Example

NOTE: The device address can be changed by pin configuration of CCI_SEL, as described in the pad description.

Preliminary product information describes products that are in development, for which full characterization data and associated errata are not yet available. Specifications and information herein are subject to change without notice.

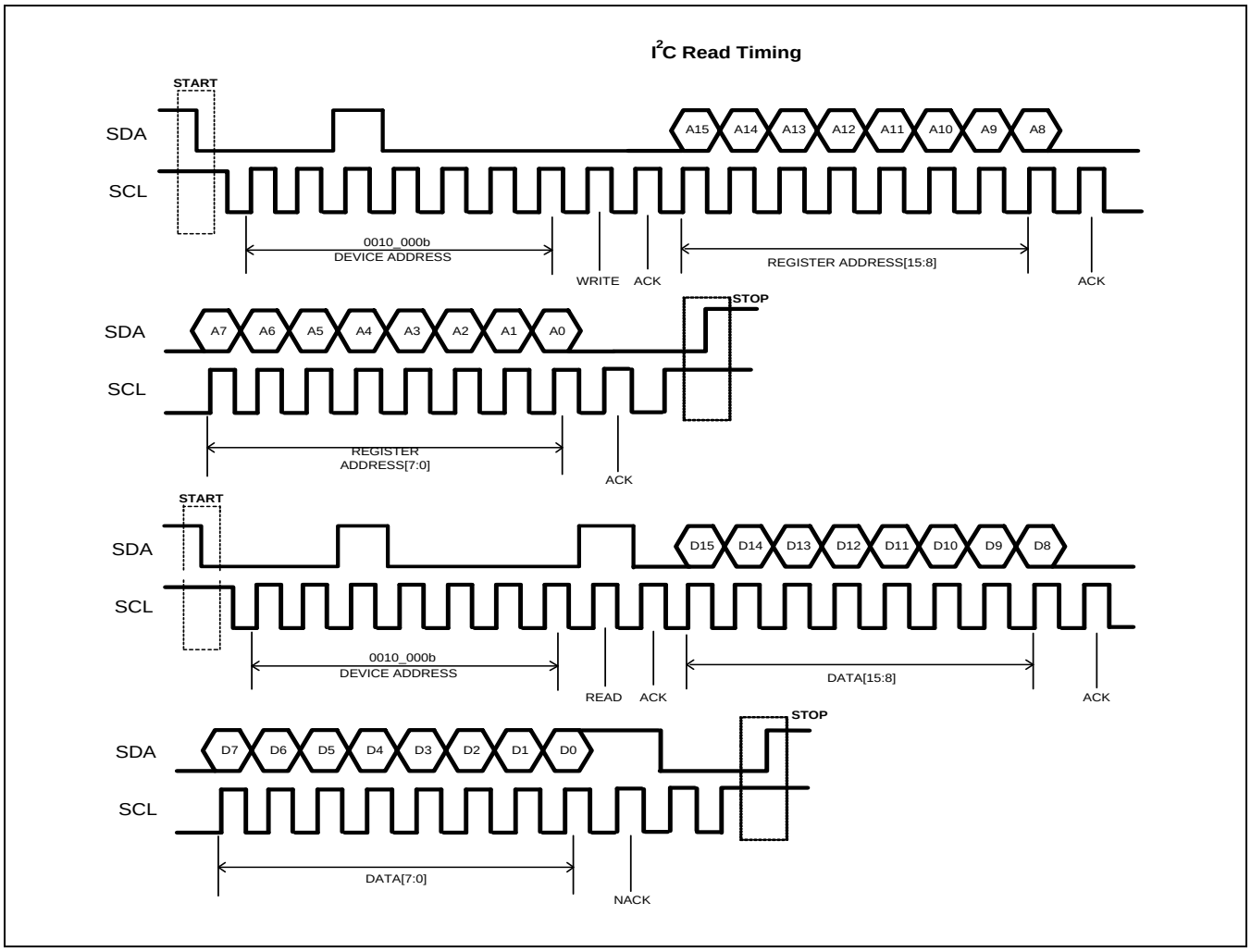


Figure 6 I2C Read Timing Example

NOTE: The device address can be changed by the pin configuration of CCI_SEL[1:0], as described in the pad description.

Preliminary product information describes products that are in development, for which full characterization data and associated errata are not yet available. Specifications and information herein are subject to change without notice.

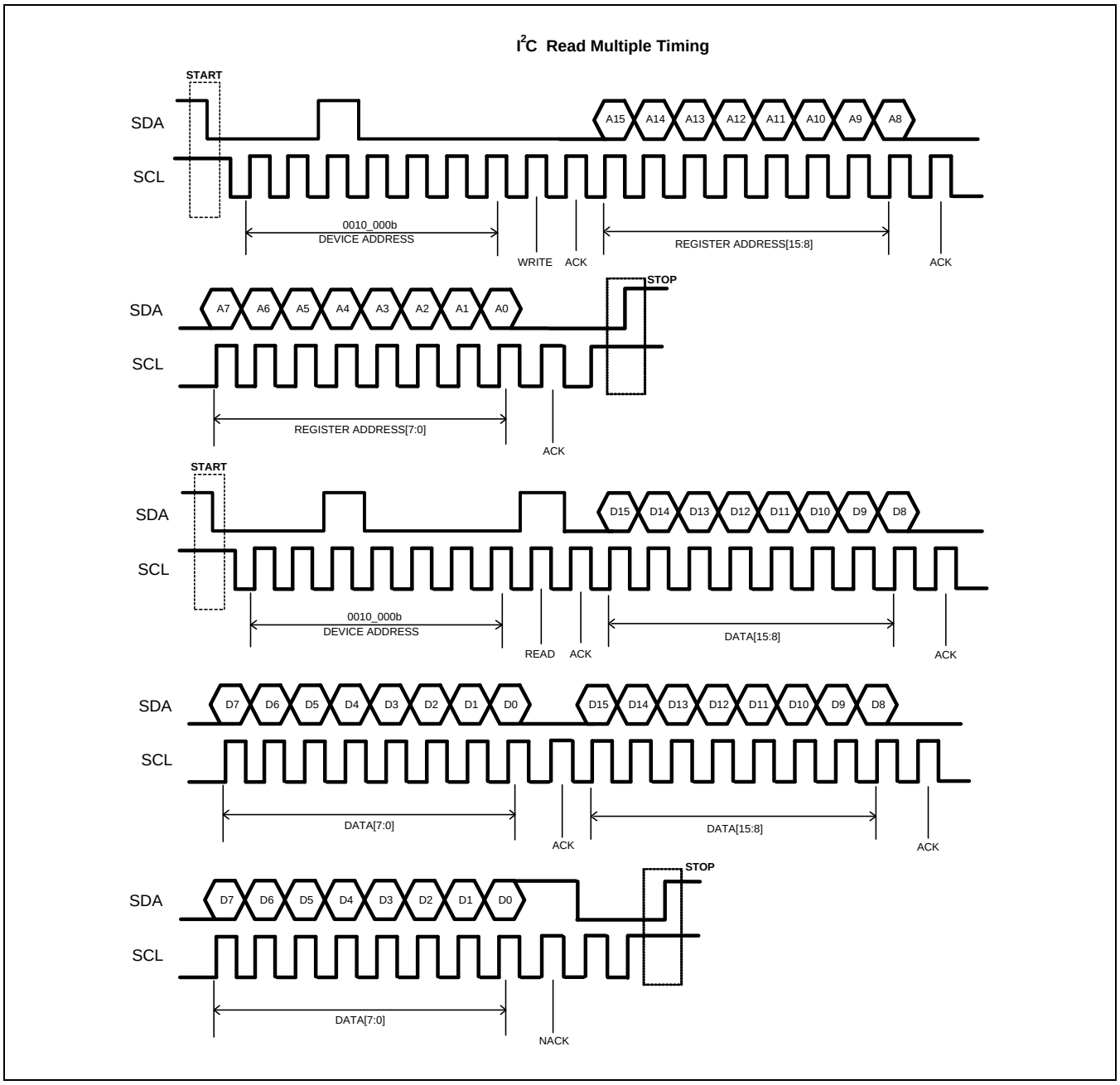


Figure 7 I2C Read Multiple Timing Example

NOTE: The device address can be changed by the pin configuration of CCI_SEL[1:0], as described in the pad description.

Preliminary product information describes products that are in development, for which full characterization data and associated errata are not yet available. Specifications and information herein are subject to change without notice.

It is possible to configure up to three and one arbitrary I2C slave addresses using CCI_SEL[1:0] pins.

Table 6 I2C ID Address

CCI_SEL_PAD	Slave Address (7-bit + Read Mode)	Slave Address (7-bit + Write Mode)	Comment
0(default)	0010_0001b/21h	0010_0000b/20h	Address 1
1	0011_0001b/31h	0011_0000b/30h	Address 2
2	0101_1111/5Fh	0101_1110/5Eh	Address 3
3	User defined	User defined	User defined

Preliminary product information describes products that are in development, for which full characterization data and associated errata are not yet available. Specifications and information herein are subject to change without notice.

4 Power Sequence

4.1 Power-Up Sequence

The digital and analogue supply voltages can be powered up in any order e.g. VDDD → VDDAP → VDDA, VDDD → VDDA → VDDAP, VDDAP → VDDD → VDDA, VDDAP → VDDA → VDDD, VDDA → VDDD → VDDAP or VDDA → VDDAP → VDDD.

On power Up:

- If RSTN is low when the power supplies are brought up then the sensor module will go into hardware standby mode.
- If RSTN is high when the power supplies are brought up then the sensor module will go into software standby mode

In both cases the presence of an on-chip power-on reset cell ensures that the CCI register values are initialized correctly to their default values. The EXTCLK clock can either be initially low and then enabled during software standby mode or EXTCLK can be a free running clock. (*If the EXTCLK is free running and VDDIO power open, leakage current through the protection diode of the EXTCLK I/O are likely to occur.)

Table 7 Power-up Sequence Timing Constraints (Serial Output Case)

Constant	Label	Min.	Max.	Unit
VDDA or VDDAP rising – VDDD rising	t0	VDDA, VDDAP and VDDD may rise in any order. The rising separation can vary from 0 ns to indefinite		ns
VDDD rising – VDDA or VDDAP rising	t1			ns
VDDA or VDDAP rising – VDDIO rising	t2	0		ns
VDDA or VDDAP rising – RSTN rising	t3	0.0	–	ns
RSTN rising – First I2C transaction	t4	6000	–	EXTCLK cycles
Minimum No. of EXTCLK cycles prior to the first I2C transaction	t5	6000	–	EXTCLK cycles
PLL start up/lock time	t6	–	1	ms
Entering streaming mode – First frame start sequence (fixed part)	t7	–	10	ms
Entering streaming mode – First frame start sequence (variable part)	t8	The delay is the coarse integration time value		lines
DPHY recovery time (TWAKEUP)	t9	1	–	ms
DPHY initialization period (TINIT)	t10	0.1	–	ms

Preliminary product information describes products that are in development, for which full characterization data and associated errata are not yet available. Specifications and information herein are subject to change without notice.

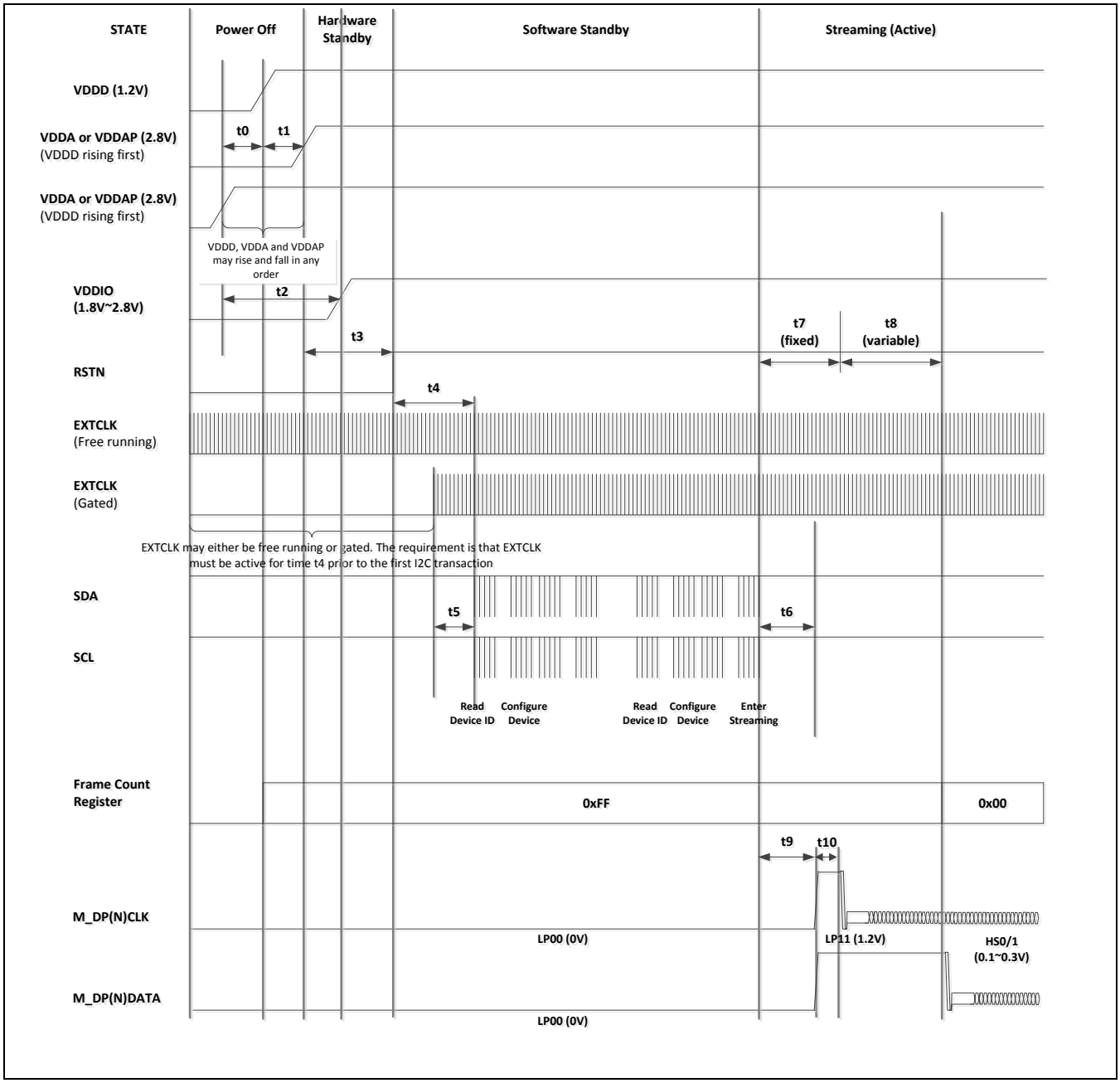


Figure 8 Power-Up Sequence Diagram

Preliminary product information describes products that are in development, for which full characterization data and associated errata are not yet available. Specifications and information herein are subject to change without notice.

4.2 Power Down Sequence

The digital and analogue supply voltages can be powered down in any order e.g. VDDD → VDDAP → VDDA, VDDD → VDDA → VDDAP, VDDAP → VDDD → VDDA, VDDAP → VDDA → VDDD, VDDA → VDDD → VDDAP or VDDA → VDDAP → VDDD.

Similarly to the power-up sequence the EXTCLK: input clock may be either gated or continuous.

If the I2C command to exit streaming is received while a frame of valid active data is being output then the sensor module must wait to the frame end code before entering software standby mode.

If the I2C command to exit streaming mode is received during the inter frame time then the sensor module must enter software standby mode immediately.

Table 8 Power-down Sequence Timing Constraints (Serial Output Case)

Constant	Label	Min.	Max.	Unit
Enter Software Standby CCI command – Device in Software Standby mode	t0	If outputting a frame of MIPI data waits to MIPI frame end code before entering software standby, otherwise enter software standby mode immediately.		
Minimum no of EXTCLK cycles after the last CCI transaction or MIPI frame end code.	t1	2000	–	EXTCLK cycles
Last I2C Transaction or MIPI frame end code- RSTN falling	t2	2000	–	EXTCLK cycles
RSTN falling – VDDA or VDDAP falling	t3	0.0	–	ns
VDDA or VDDAP falling – VDDD falling	t4	VDDA, VDDAP and VDDD may fall in any order. The falling separation can vary from 0 ns to Indefinite.		ns
VDDD falling – VDDA or VDDAP falling	t5			ns
VDDD falling – VDDIO falling	t6	0.0	–	ns

Preliminary product information describes products that are in development, for which full characterization data and associated errata are not yet available. Specifications and information herein are subject to change without notice.

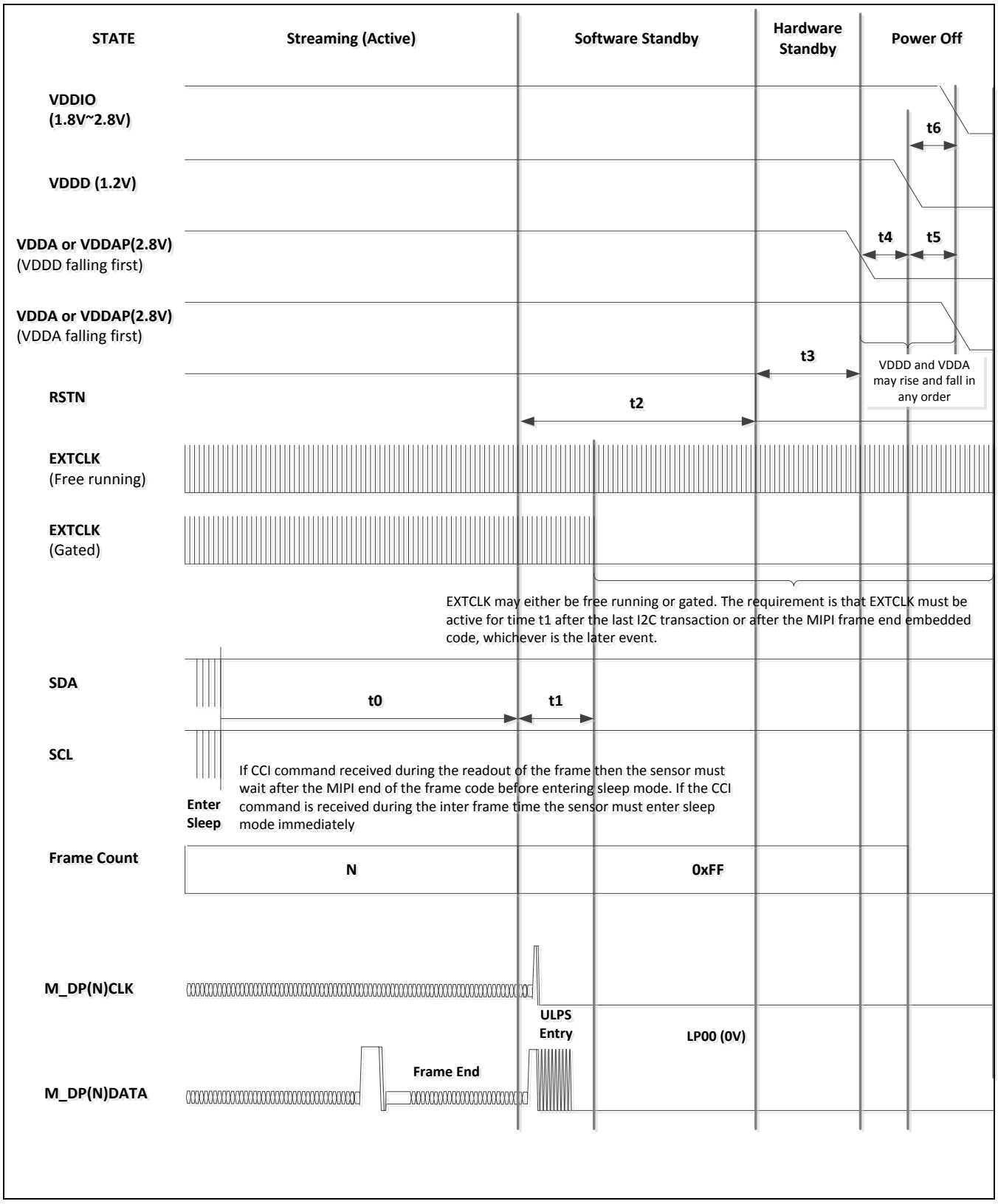


Figure 9 Power-Down Sequence Diagram

Preliminary product information describes products that are in development, for which full characterization data and associated errata are not yet available. Specifications and information herein are subject to change without notice.

4.3 Sensor System Reset

S5KRD2YX can be initialized by changing RSTN to LOW when all the supply voltages are powered on.

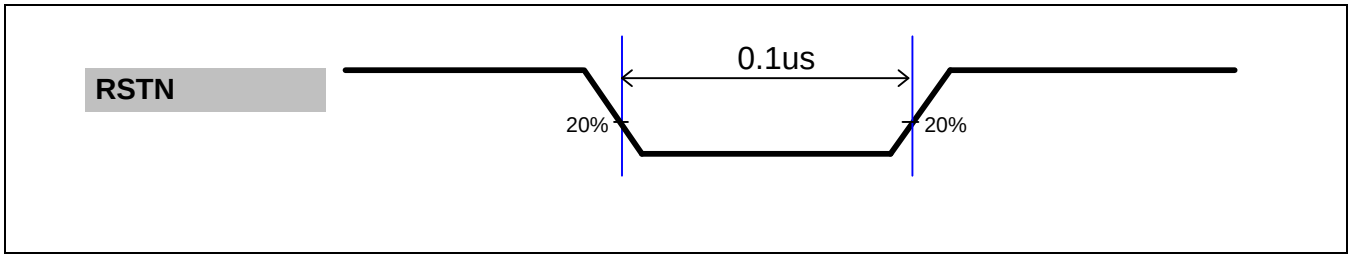


Figure 10 Sensor System Reset

Preliminary product information describes products that are in development, for which full characterization data and associated errata are not yet available. Specifications and information herein are subject to change without notice.

5 Pixel Information

5.1 Pixel Array

The effective pixel array is 640 (H) × 480 (V). Micro-lens is placed to increase the effective fill factor for higher sensitivity.

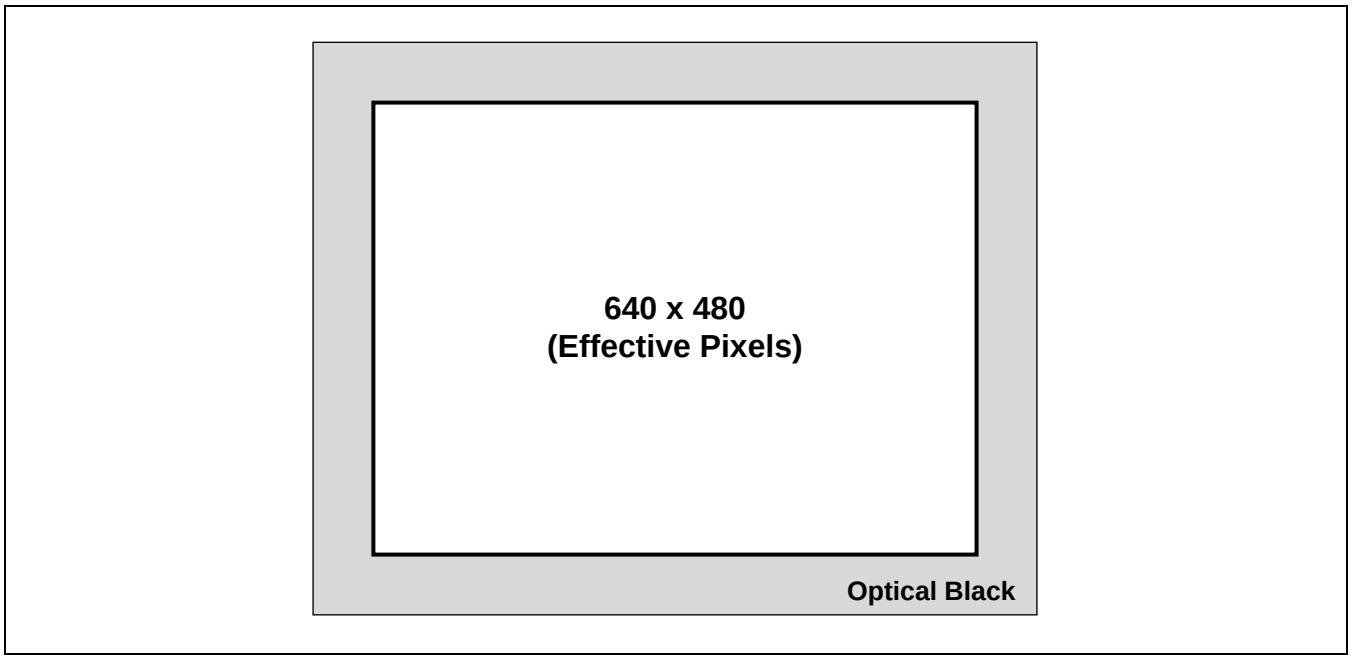


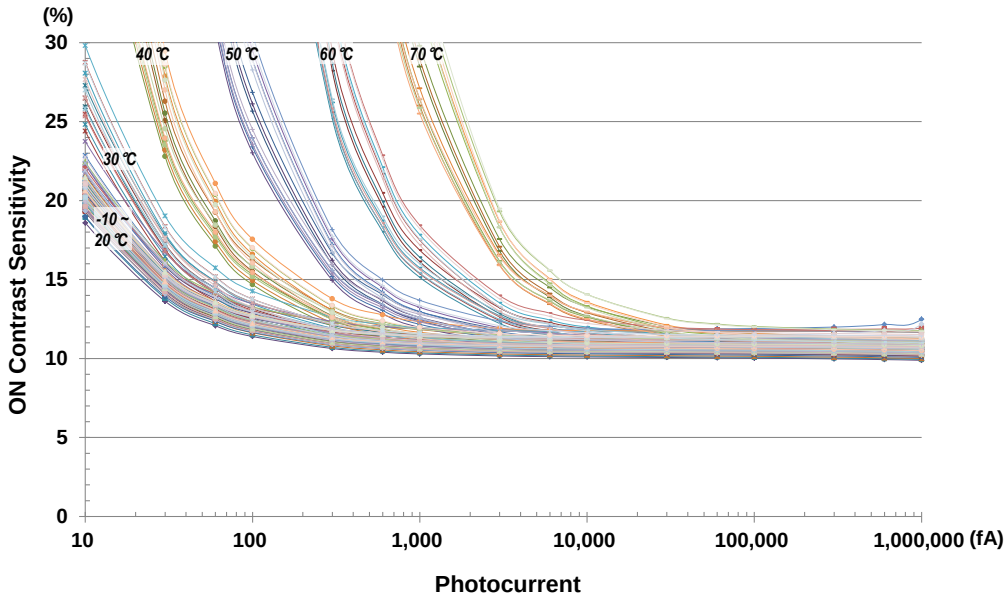
Figure 11 Pixel Array Information

NOTE: Top view on chip.
Displayed image will be flipped vertically and horizontally.

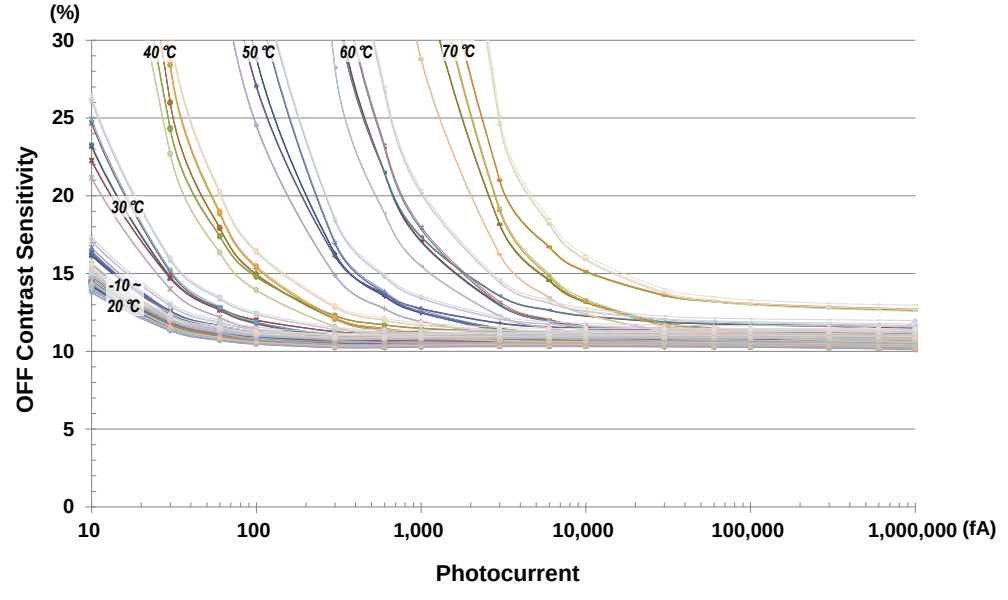
Preliminary product information describes products that are in development, for which full characterization data and associated errata are not yet available. Specifications and information herein are subject to change without notice.

5.2 Contrast Sensitivity Characteristics

The contrast sensitivity of S5KRD2YX is characterized by the responsivity for illumination changes at the certain illumination levels. Both ON and OFF contrast sensitivities are adjustable individually.



(a) ON Contrast Sensitivity (`pixel_on_event_threshold` = 2)



(b) OFF Contrast Sensitivity (`pixel_off_event_threshold` = 6)

Figure 12 The Simulated Contrast Sensitivity Characteristics

NOTE: The simulation was performed with PVT variations. The illumination levels are the expected values without microlens and the contrast sensitivity lines may be shifted to left or right within 1 decade level along x-axis, according to the measurement with the fabricated chip. 10fA is roughly equal to 1Lux.

Preliminary product information describes products that are in development, for which full characterization data and associated errata are not yet available. Specifications and information herein are subject to change without notice.

5.3 Event Generation Probability Characteristics

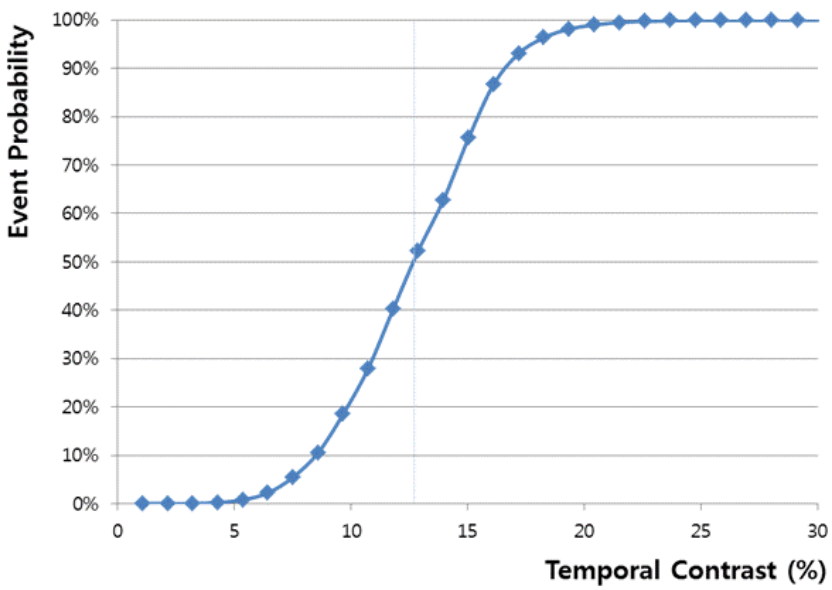


Figure 13 Event Generation Probability Characteristics according to Temporal Contrast

Preliminary product information describes products that are in development, for which full characterization data and associated errata are not yet available. Specifications and information herein are subject to change without notice.

6 Functional Description

S5KRD2YX provides several readout modes and specific functions for the treatment of events and for the required variety of clocks, one phase-locked loops (PLL) is embedded in the sensor. This is generating clocks for systems and the high-speed serial interfaces. The master input clock range is between 6 and 64 MHz.

6.1 PLL and Clock Generator

The S5KRD2YX contains one Phase-Locked Loops (PLLs) and a clock generator, which generate all the necessary event timing, output pixel clocks, and interface serializing clocks.

By setting the divide-ratio for Pre PLL Clock Divider (`pll_p`) and PLL Multiplier (`pll_m`) appropriately, users can get necessary PLL output Clock.

The PLL can handle any External Input Clock in the range of 6 MHz to 64 MHz (20 MHz is default), and synthesize PLL_CLK between 500 MHz and 1000 MHz. For the proper PLL operation, PLL Input Clock should be in the range of 3 MHz to 6 MHz. All PLL programming should be performed during software stand-by mode for the stable system operation.

The overall clock tree structure is shown in *Figure 14*

Preliminary product information describes products that are in development, for which full characterization data and associated errata are not yet available. Specifications and information herein are subject to change without notice.

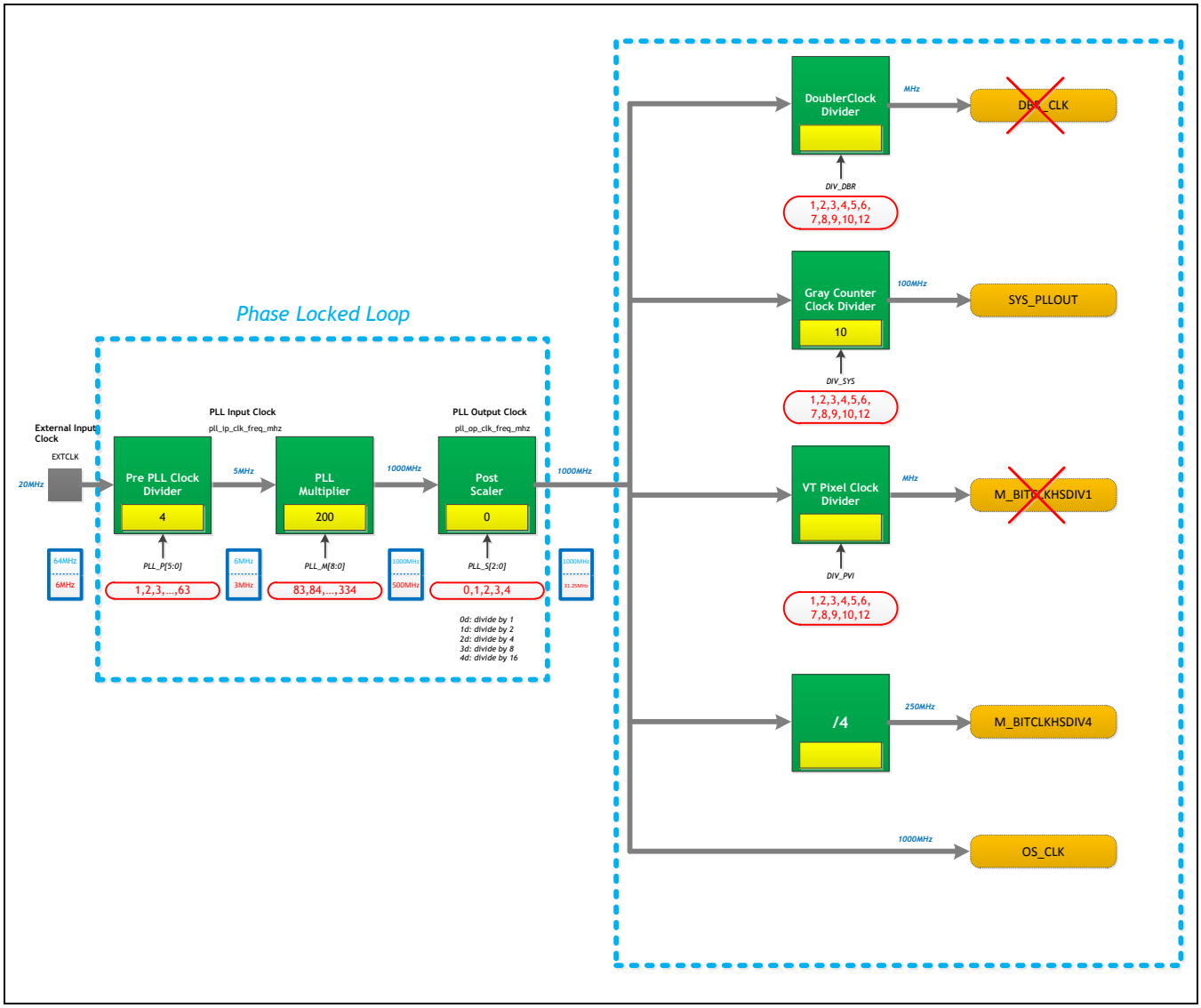


Figure 14 PLL and Clock Generator

NOTE: EXTCLK = 20MHz

All the setting values of registers are represented by decimal unit.

All necessary frequencies are synthesized by the following equations.

PLL Input Clock = External Input Clock (EXTCLK)/pll_p (3 MHz to 6 MHz)

Lock_freq = PLL Input Clock×pll_m (500 MHz to 1000 MHz)

Preliminary product information describes products that are in development, for which full characterization data and associated errata are not yet available. Specifications and information herein are subject to change without notice.

6.2 Sub-sampling Mode

S5KRD2YX supports the following operation modes and their specifications are described in the following table.

Table 9 Sub-sampling Modes

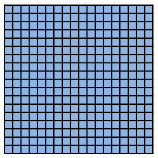
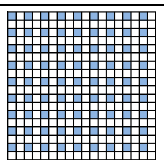
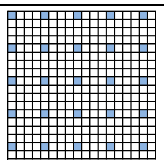
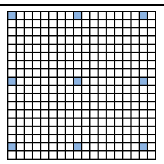
Mode	Resolution	Sub-sampling	Comments
Full Resolution	640 x 480		✓ Analog sub-sampling option enabled ✓ Controlled by register option ✓ Pixel is active ✓ Pixel is turned off and not consuming power
Half Resolution	320 x 240		
Quarter Resolution	160 x 120		
One-eighth Resolution	80 x 60		

Table 10 Sub-sampling Mode Control Register

Register	Address	Default	Bit	Description
REG_STRM_CTRL_APSX_Subsample	0x0111	0b00	[7:6]	Sub-sampling mode control value for columns for streaming mode
REG_STRM_CTRL_APSY_Subsample	0x0111	0b00	[5:4]	Sub-sampling mode control value for rows for streaming mode
REG_CTRL_APSX_Subsample	0x0111	0b11	[3:2]	Sub-sampling mode control value for columns for monitoring mode
REG_CTRL_APSY_Subsample	0x0111	0b11	[1:0]	Sub-sampling mode control value for rows for monitoring mode

Preliminary product information describes products that are in development, for which full characterization data and associated errata are not yet available. Specifications and information herein are subject to change without notice.

6.3 Event Threshold Level Control

The user can control ON and OFF event threshold levels of the pixel array by Event Threshold Level Control Registers (ON_EVTH_C, ON_EVTH_F, ON_EVTH_FP, OFF_EVTH_C, OFF_EVTH_F, OFF_EVTH_FP). The reference for the following expression is the typical condition at 30°C.

†ON event threshold = [10^{ (80 + 14*(C-2) + 4*F*FP) / (80*20) } – 1] x 100% @ typical condition
†OFF event threshold = [10^{ (80 + 14*(6-C) + 4*F*FP) / (80*20) } – 1] x 100% @ typical condition

† Expressions are subject to update in parameters.

Table 11 Event Threshold Level Control Register

Register	Address	Default	Bit	Description
ON_EVTH_C	0x0017	0x2	[2:0]	ON event threshold level coarse control value, unsigned 3-bit binary numbers (*C*)
ON_EVTH_F	0x0018	0x00	[6:1]	ON event threshold level fine control value, unsigned 6-bit binary numbers (*F*)
ON_EVTH_FP	0x0018	0x0	[0]	Sign bit (*FP*) for ON_EVTH_F *FP*=1/-1 for ON_EVTH_FP=1/0
OFF_EVTH_C	0x0019	0x6	[2:0]	OFF event threshold level coarse control value, unsigned 3-bit binary numbers (*C*)
OFF_EVTH_F	0x001A	0x00	[6:0]	OFF event threshold level fine control value, unsigned 6-bit binary numbers (*F*)
OFF_EVTH_FP	0x001A	0x0	[0]	Sign bit (*FP*) for OFF_EVTH_F *FP*=1/-1 for ON_EVTH_FP=1/0

Preliminary product information describes products that are in development, for which full characterization data and associated errata are not yet available. Specifications and information herein are subject to change without notice.

6.4 Refractory Period Control

The user can control the refractory period of the pixel array by Refractory Period Control Register (`pixel_refractory_period`). The reference for the following expression is the typical condition at 30°C.

Refractory period = 1 ms x 1.5^(2 - pixel_refractory_period[2:0]) @ typical condition

Table 12 Event Threshold Level Control Register

Register	Address	Default	Bit	Description
pixel_refractory_period	0x001D	0x02	[2:0]	Refractory period control value, unsigned 3-bit binary numbers

Preliminary product information describes products that are in development, for which full characterization data and associated errata are not yet available. Specifications and information herein are subject to change without notice.

6.5 Output Packet Format

The S5KRD2YX send event data using 32-bit packet format.

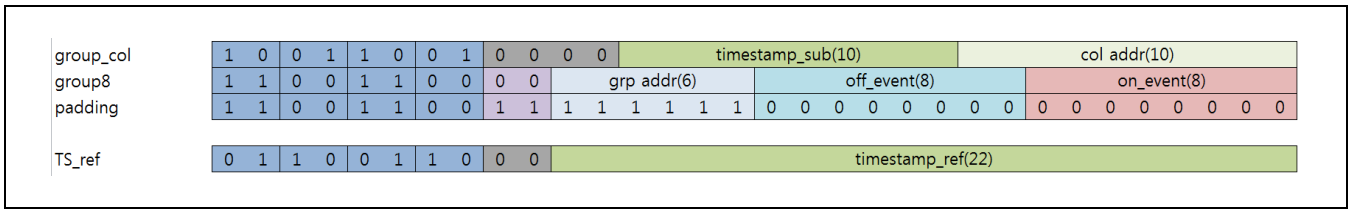


Figure 20 32-bit Packet Format

- 32-bit packetized format:
  - Extracted via 16 output pads using Double Data Rate scheme (DDR) scheme
- group_col:
  - 4 Bytes size
  - column address and sub-timestamp
- group8:
  - 4 Bytes size, 8 event per group
  - group address and on/off events
- TS_ref:
  - 4 Bytes size
  - reference timestamp
- padding:
  - 4 Bytes size
  - fill out the data

Preliminary product information describes products that are in development, for which full characterization data and associated errata are not yet available. Specifications and information herein are subject to change without notice.

7 Electrical Characteristics

7.1 Absolute Maximum Rating

Table 13 Absolute Maximum Rating

Description	Symbol	Value	Unit
ATOP supply absolute Max.	VDDA (1)	–0.3 to 4.0	V
	VDDAP (1)	–0.3 to 4.0	V
	VDDAD (2)	–0.3 to 1.8	V
I/O supply absolute Max.	VDDIO (3)	–0.3 to 3.8	V
PLL supply absolute Max.	VDD_PLL (2)	–0.3 to 1.8	V
	VDDA_PLL (1)	–0.3 to 3.6	V
MIPI supply absolute Max.	VDD_MIPI (2)	–0.3 to 1.8	V
Digital supply absolute Max.	VDDD (2)	–0.3 to 1.8	V
Storage temperature	TSTG	–40 to +85	°C

NOTE:

1. Analog Supply 2.9 V + 1.1 V
2. Digital Supply 1.3 V + 0.5 V
3. IO Supply 3.3 V + 0.5 V

Preliminary product information describes products that are in development, for which full characterization data and associated errata are not yet available. Specifications and information herein are subject to change without notice.

7.2 Operating Conditions

Table 14 Operating Conditions

Description	Symbol	Min.	Typ.	Max.	Unit
ATOP supply voltage	VDDA (1)	2.65	2.8	2.95	V
	VDDAP (1)	2.65	2.8	2.95	V
	VDDAD (2)	1.1	1.2	1.3	V
I/O supply voltage	VDDIO	3.1	3.3	3.5	V
PLL supply voltage	VDD_PLL (2)	1.1	1.2	1.3	V
	VDDA_PLL (1)	2.65	2.8	2.95	V
MIPI supply voltage	VDD_MIPI (2)	1.1	1.2	1.3	V
Digital supply voltage	VDDD (2)	1.1	1.2	1.3	V
Optimum Operating Temperature (3)	TOPT	5	–	40	°C
Normal Operating Temperature (4)	TOPR	–25	–	55	°C
Functional Operating Temperature (5)	TFUNC	–30	–	70	°C

NOTE:

1. Analog Supply Tolerances: Lower Limit: – 150 mV, Upper Limit: + 150mV
2. Digital Supply Tolerances: 1.2 V ± 100 mV
3. Optimum Operating Temperature: No visible degradation in image quality
4. Normal Operating Temperature: Camera produces acceptable images
5. Functional Operating Temperature: Camera fully functional

Preliminary product information describes products that are in development, for which full characterization data and associated errata are not yet available. Specifications and information herein are subject to change without notice.

DC Characteristics

Table 15 DC Characteristics

Description	Symbol	Min.	Typ.	Max.	Unit
Input Capacitance	CIN (2)	–	–	5	pF
Input Operating Frequency	FIN (EXTCLK)	–	20	–	MHz
ATOP supply operating current	IDDA (1)	–	5.2	–	mA
	IDDAP (1)	–	1.9	–	mA
	IDDAD (1)	–	0.3	–	mA
PLL supply operating current	IDDA_PLL (1)	-	3.7	-	mA
MIPI supply operating current	IDDD_MIPI (1)	-	30.3	-	mA
Digital supply operating current	IDDD (1)	–	5.8	–	mA
I/O supply operating current	IDDIO (1)	–	3.7	–	mA

NOTE:

1. Operation currents (IDDA, IDDD, IDDIO, IDDD_MIPI and IDD18_LVDS) will be measured at active mode
2. CIN max can have variation by environment.

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7.3 AC Characteristics

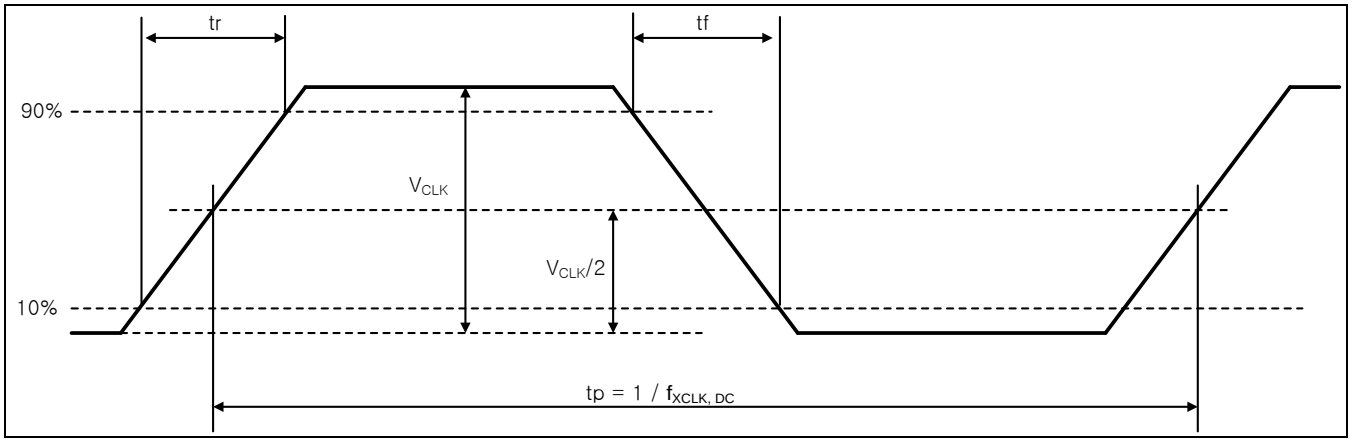

Figure 21 Master Clock Waveform Diagram

Table 16 AC Characteristics

(VDDA_PLL = 2.65 V to 2.95 V, VDDIO = 1.2 V to 3.3 V, VDDD = 1.12 V to 1.28 V, T_{OPR} = –30 to 70 °C)

Characteristics	Symbol	Condition	Min.	Typ.	Max.	Unit
External clock frequency (NOTE)	$f_{XCLK, DC}$	–	6	–	64	MHz
External clock duty cycle (NOTE)	f_{XDUTY}	–	45	–	55	%
PLL locking time	t_{LOCK}	–	–	200	1000	µs

NOTE: Applied to EXTCLK pin.

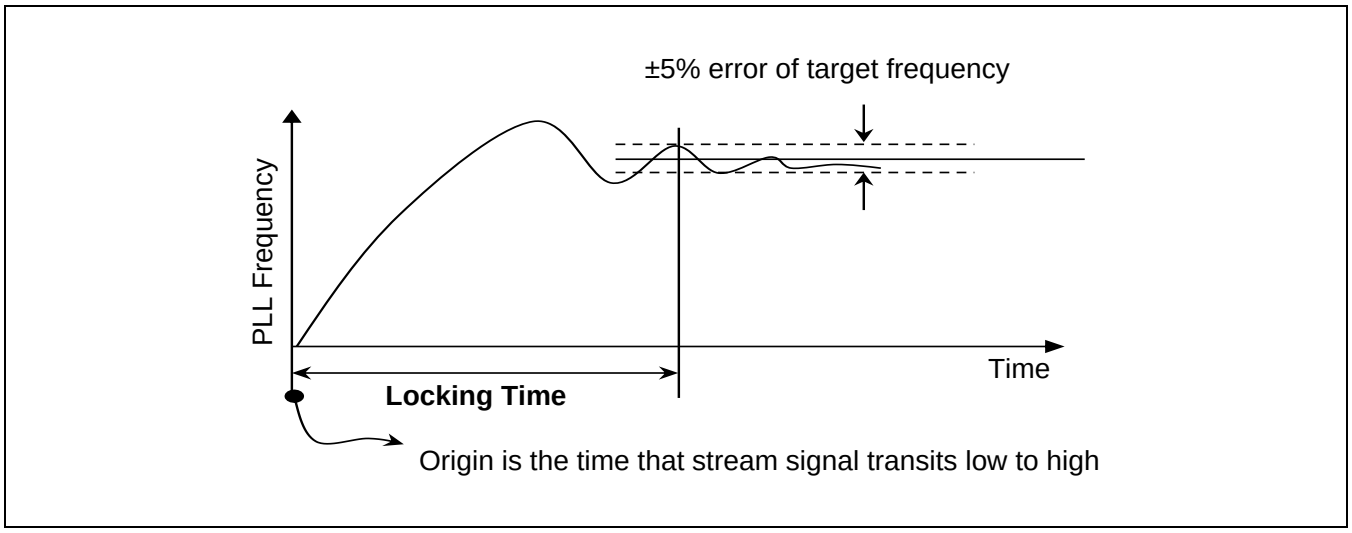

Figure 22 PLL Locking Time

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