ELC 2137 Lab 03: Adders

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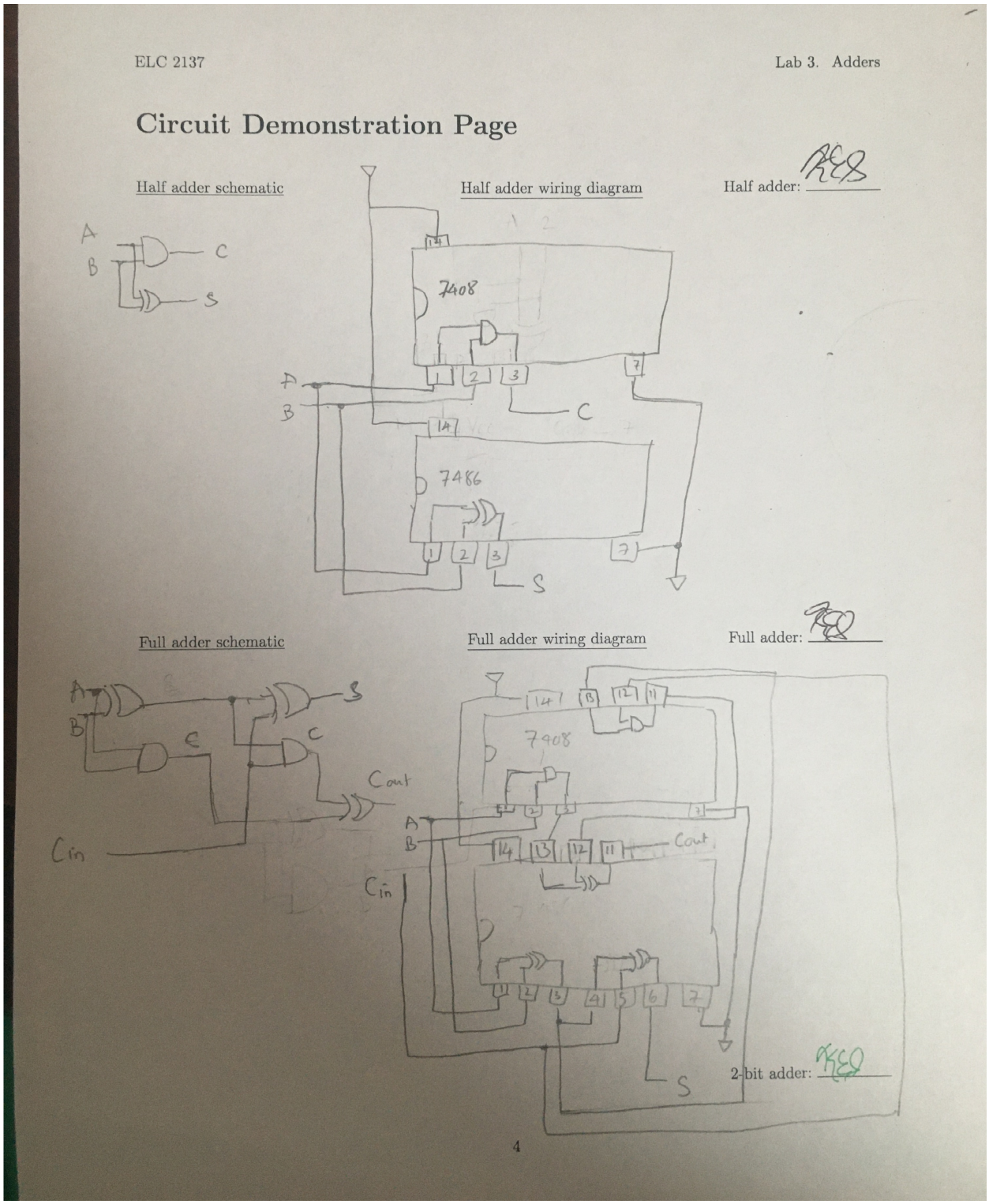
Summary

This lab's purpose is to create a circuit that implement a half, full, and 2-bit adder. To implement a half adder, a XOR gate is used to store the sum between two inputs and an AND gate is used to store the carry between two inputs. To implement a full adder, create a first stage half adder then pass its sum and the carry input into a second stage half adder to find the S. Then pass the second stage half adder carry and the first stage half adder into a XOR gate to find the carry output. To implement a 2-bit adder, use a full bit adder to find the S_1, then use the carry output from the first full adder to as the carry input for a second full adder to find the S_2 and the carry output of the 2-bit adder.

Q&A

1.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Lab 3. Adders
Circuit Demonstration Page
Half adder schematic
Half adder wiring diagram
Half adder:
A
B
C
S
7408
7486
Full adder schematic
Full adder wiring diagram
Full adder:
Cout
Cin
2-bit adder:
4

2.

3.

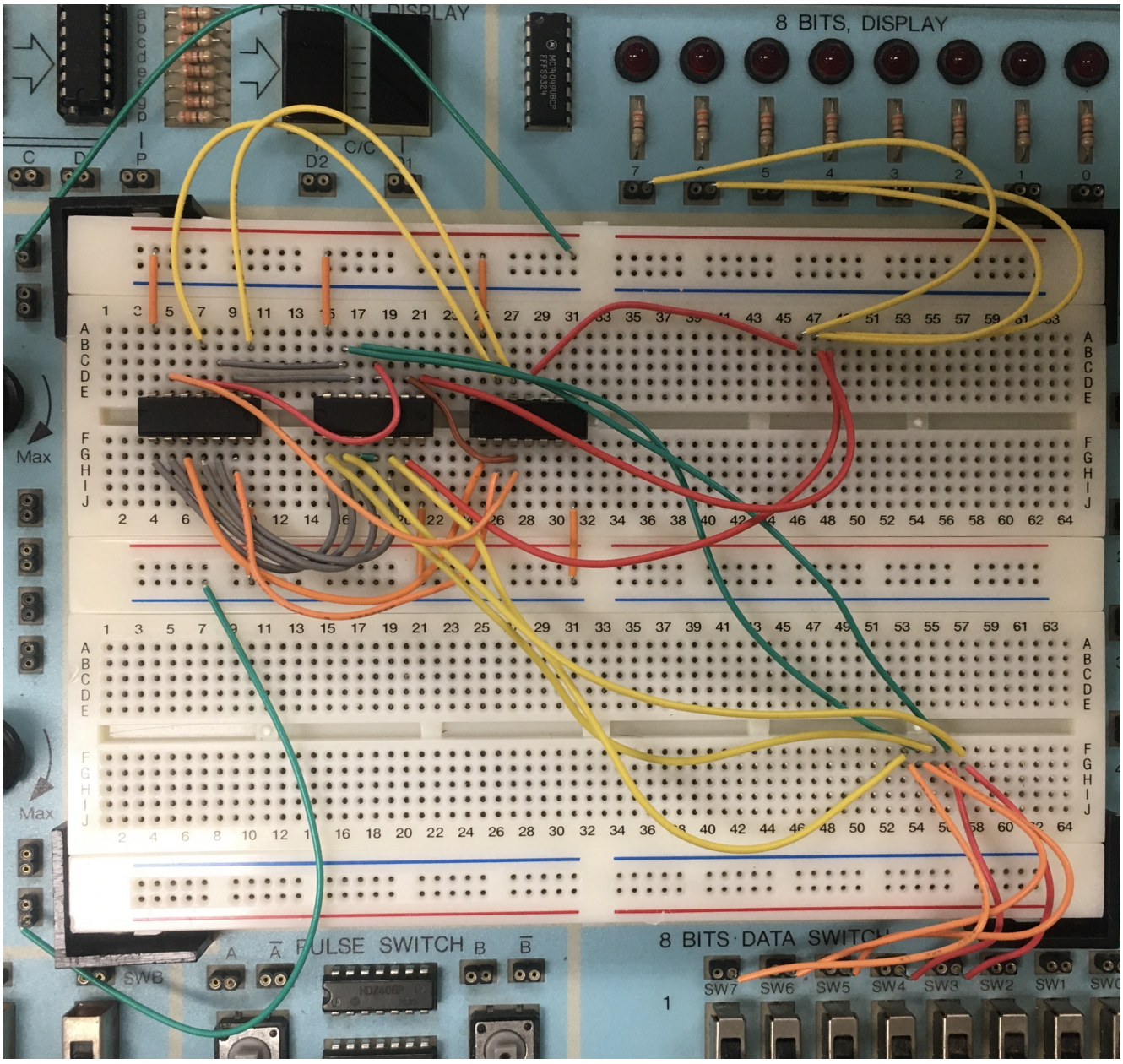

Figure 1: Full Adder

C_{in}	A	B	C_1	C_2
0	0	0	0	0
0	0	1	0	0
0	1	0	0	0
0	1	1	1	0
1	0	0	0	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	0

From the truth table, we have prove by exhaustion that carry outputs of the first half adder and the second half adder cannot be high at the same time

4. We should use an AND gate for carry bits, because when adding two bits, a carry is only needed when both input is a "1" so an AND gate would be appropriate to indicate the carry bits.