Course: Computer Organization - ENCM 369

Lab #: Lab 8

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Lab Section: B02

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Exercise A:

Part I:

Based on the table below:

components	Time(ps)
t_setup	32
t_pcq	27
Sign extender t_pd	38
Multiplier t_pd	195

Since we want the maximum allowed delay for the adder and the desired frequency of CLK is 2.80 GHZ
To convert from GHz to ps we use the formula below:

$$\frac{1}{GHz} * 10^3$$

So

$$\frac{1}{2.8} * 10\text{^}3 = 357.14$$

Then we can use the following formula to calculate the maximum allowed time for the adder

$$t_{pd} \leq T_C - (t_{pcq} + t_{setup})$$

Since the Multiplier has more delay than the extender, we will use it so:

$$195 + t_{pd(add)} = 357.14 \ - (27 + 32)$$

As such the maximum allowed t_{pd} for the adder is 103.14ps

Part II:

Since we want the t_{ccq} of the circuit we can use the equation

$$t_{ccq} \geq t_C - t_{\mathrm{hold}}$$

From the previous question t_c = 357.14 and t_{hold} = 7
Note that there is a wire, that does not pass through either the multiplier or the sign extender. As such:

$$t_{ccq} \geq 357.14 \ - 7$$

So t_{ccq} = 350.14

Exercise B:

Part I:

Based on Timing Parameters Set 1

(1)

When we want to calculate from the PC back to the PC through several elements, including "All Bits 0?"

It seems we go through 8 components: an Adder, I-Mem, R-File, Control, "All Bits 0?", AND gate, and a 2:1 mux.

So, we want to calculate the t_{pd} value so we the values will be as following.

Element	Parameter	Value
I-Mem	t_{pd}	225
R-File	t_{pd}	144
Control	t_{pd}	90
All Bits 0?	t_{pd}	127
AND gate	t_{pd}	24
2:1 mux	t_{pd}	33

And so, adding all the values below together we get:

$$225 + 144 + 90 + 127 + 24 + 33 = 643ps$$

(This is the control signal)
As such to simply go from the PC to the PC back again we need 643 ps

(2)

When we want to calculate from the PC back to the PC through several elements, including the adder that produces the branch target address.
So, we do the same as the last calculation however now we add sign extend, and a "<< 1".

Element	Parameter	Value
Adder	t_{pd}	170
I-Mem	t_{pd}	225
Sign extend	t_{pd}	56
<< 1	t_{pd}	40
Adder	t_{pd}	170
2:1 mux	t_{pd}	33

So now the calculation will be:

$$170 + 225 + 56 + 40 + 170 + 33 = 694ps$$

As such to go to a specified address we need 694 ps

(3)

Now we want to calculate from the PC to the R-File WD3 input through several elements, including the ALU.
So, we will go through: I-Mem, R-File read, Control, ALU, 2:1 mux, R-File write

Element	Parameter	Value
I-Mem	t_{pd}	225
R-File	t_{pd}	144
Control	t_{pd}	90
ALU	t_{pd}	194
2:1 mux	t_{pd}	33

So, the calculation will be:

$$225 + 144 + 90 + 194 + 33 = 686 \text{ ps}$$

As such to calculate a value and go back to the R-File we need 686 ps

(4)

We will have the exact same calculations as before but now there will be an addition of D-mem

As such the values will be as follows:

Element	Parameter	Value
I-Mem	t_{pd}	225
R-File	t_{pd}	144
Control	t_{pd}	90
D-mem	t_{pd}	237
2:1 mux	t_{pd}	33

So, the calculation will be:

$$225 + 144 + 90 + 237 + 33 = 729 \text{ ps}$$

As such to read from the memory and go back to a register you need 729 ps

As such the longest tpd would be that of (4).

For reliable operation, based on the values calculated t_{pd} would be 729 ps, t_{setup} would be 21, and t_{pcq} would be 32.

So, using the equation: $t_{pd} \leq T_C - t_{pcq} - t_{setup}$

$$729 \leq T_C - 32 - 21$$

$$T_C \geq 729 + 32 + 21$$

T_C = 782 ps

As such the minimum clock period for reliable operation would be 782 ps

Part II:

Since it is the exact same calculations but with different values, the tables with calculation under will be put.

(1)

Element	Parameter	Value
I-Mem	t_{pd}	198
R-File	t_{pd}	144
Control	t_{pd}	90
All Bits 0?	t_{pd}	127
AND gate	t_{pd}	24
2:1 mux	t_{pd}	33

t_{pd} = 198 + 144 + 90 + 127 + 24 + 33 = 616 ps

(2)

Element	Parameter	Value
Adder	t_{pd}	192
I-Mem	t_{pd}	198
Sign extend	t_{pd}	56
<< 1	t_{pd}	40
Adder	t_{pd}	192
2:1 mux	t_{pd}	33

t_{pd} = 192 + 198 + 56 + 40 + 192 + 33 = 711 ps

(3)

Element	Parameter	Value
I-Mem	t_{pd}	198
R-File	t_{pd}	144
Control	t_{pd}	90
ALU	t_{pd}	233
2:1 mux	t_{pd}	33

t_{pd} = 198 + 144 + 90 + 233 + 33 = 698 ps

(4)

Element	Parameter	Value
I-Mem	t_{pd}	198
R-File	t_{pd}	144
Control	t_{pd}	90
D-mem	t_{pd}	210
2:1 mux	t_{pd}	33

t_{pd} = 198 + 144 + 90 + 210 + 33 = 675 ps

As such based on the values above: t_{pd} = 711 ps, t_{setup} = 21, t_{pcq} = 32

$$T_C \geq t_{pd} + t_{setup} + t_{pcq}$$

So

$$T_C \geq 711 + 21 + 32$$

T_C = 764 ps

Exercise C:

2. The PC gets the output of the adder in the Fetch stage, which will be 0x0040_0150. InstrD gets the instruction, which is 0x4139_0a33. The decoding phase of the LW instruction and the Fetching phase of the sub instruction has ended. It is also the beginning of the Execution phase for the LW instruction and the beginning of the decoding phase of the sub instruction. Just Before T = 74ns, RD1 will have a value of 10000, RdD will have a value of 10001, and ImmExtD will have a value of 0000011000.

3. RD1 will have a value of 10010, RD2 will have a value of 10011, and RdD will have a value of 10100. The Value of the
ALU will be 0x1001_0318 which is the addition of 0x18(24) and 0x1001_0300(x16).

4. The Value of the ALU will be 0x0000_04FC this is the result of the subtraction between 0x0000_0508(x18) and 0x0000_000c(x19). RDE will have a value of 10100 which is the value of the register where the sub instruction will be saved.

5. The Value of the ALU will be 0x6677_8899 which is the data at the address of 0x1001_0318. The value of RdM will be 10001(x17) which is where the data will be stored for the LW instruction.

Exercise D: