Course : Computer Organization – ENCM 369

Lab # : Lab 6

Group Submission for : B04

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Instr lw t6, 20(sp) 0x0040_0130

sp = 0x7fff_fea0
t6 = 0x0001_2345

imm = 20	rs1 = 0	f3	rd = 6	opcode
0000_0001_0100	0_0010	010	1_1111	00_0011

PCSrc	0	A1	00010
Result Src	1	A2	10100
MemWrite	0	A3	11111
ALU Control	000		
ALU Src	1		
Imm Src	00		
Reg Write	1		

Src A	7fff_fea0
Src B	0000_0014
ALU Result	7fff_feb4
Result	0006_6666
PC Next	0040_0134

WD 3 0006_6666

Instr sub s1, s1, t5

0040_0134

sp = 0000_0064
t6 = ffff_fff0

f7	rs2	rs1	f3	rd	opcode
010_0000	00101	00001	000	00001	011 00 11

PCSrc	0	A1	10001
Result Src	0	A2	01011
MemWrite	0	A3	10001
ALU Control	001		
ALU Src	0		
Imm Src	xx		
Reg Write	1		

Src A	0000_0064
Src B	ffff_fff0
ALU Result	0000_0054
Result	0000_0054
PC Next	0040_0138

WD3 0000_0054

Instr andi t1, t1, -256

0x 8a ab _ cdef

SP =
t6 =

f7	rs1	f3	rd	opcode
1111 111	1000	111		0010011

PCSrc	0	A1	01001
Result Src	0	A2	00000
MemWrite	0	A3	00000
ALU Control	010		
ALU Src	1		
Imm Src	00		
Reg Write	1		

Src A	8a ab _ cdef
Src B	ffff _ ff00
ALU Result	8a ab _ cd e0
Result	8a ab _ cde0
PC Next	0040 _ 0a80

WD 3 8a ab _ cdef

Exercise C6

Figure 4: Incomplete Main Decoder specification for single-cycle computer with support for `jalr`. Compared to textbook Table 7.6, the table here has one more row and one more column.

Instruction	Opcode	RegWrite	ImmSrc	ALUSrc	TargetSrc	MemWrite	ResultSrc	Branch	ALUOp	Jump
`lw`	0000011	1	00	1	X	0	01	0	00	0
`sw`	0100011	0	01	1	X	1	xx	0	00	0
R-type	0110011	1	xx	0	X	0	00	0	10	0
`beq`	1100011	0	10	0	1	0	xx	1	01	0
I-type ALU	0010011	1	00	1	X	0	00	0	10	0
`jal`	1101111	1	11	x	0	0	10	x	xx	1
`jalr`	1100111	1	00	1	0	0	10	X	10	1
		①	②	③	④	⑤	⑥	⑦	⑧	⑨

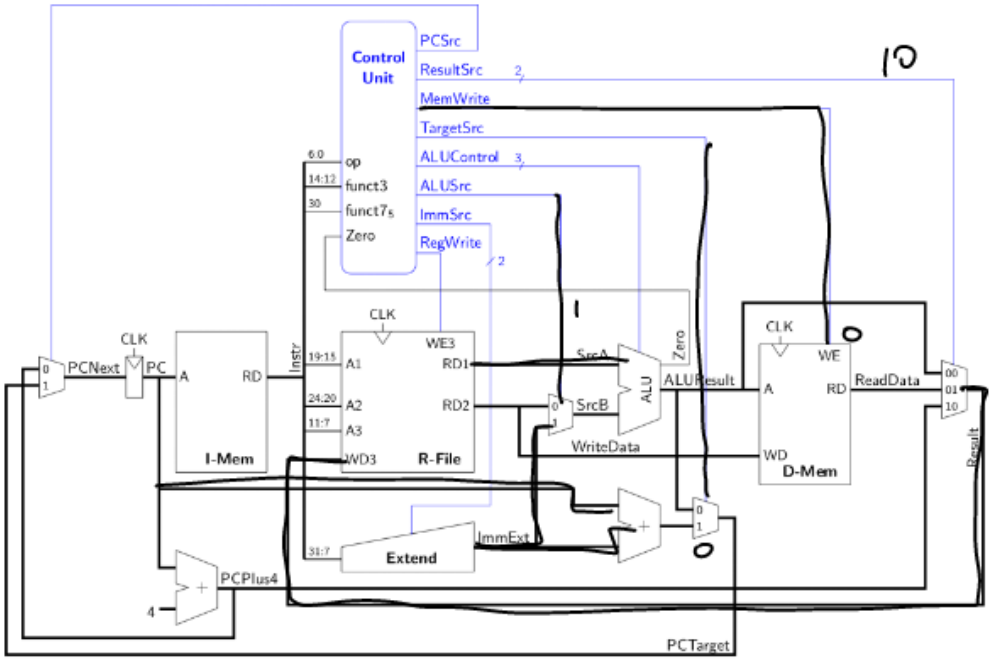

Figure 3: Textbook Figure 7.15 computer enhanced to support `jalr`.

1. RegWrite has to be 1 since we need to write the result to the register file

2. ImmSrc has to be Zero since we are trying to use 32-bit sign extension

3. ALUSrc has to be 1 to select Sign-extended immediate field of the instruction instead of rt to add it with rs1.

4. TargetSrc will be 0 since ALU Result is written into the PC. ALUResult is the sum of sign-extension of the offset and the value of GPR from rs1

5. Since we don't need to write anything to the memory, it should be 0.

6. ResultSrc should be 10 since PC+4 should be written into rd register that is WD3

7. Branch will be X since jump is always 1, also since it is ored with Branch, so either ways PCSrc will be 1.

8. ALU op will be 10 since jalr is a I-type op.

9. jump will be 1, since we need to use jump in jalr instruction.