This is a general outline of what Mr. Galipeau expects to see in your report. **You still need to put it into the EECS department format.** There are more details in the project manual (page 5) about common mistakes.

Abstract

Describe the description of the device you are going to be building (vending machine), the inputs to the device, and the outputs. Describe, at a high level, the finite state machine implementation. Describe the implementation details on the FPGA. One sentence takeaway on the outcomes of your project/design.

Introduction

Fully describe the operation of the machine, what assumptions you made (and why), and forward reference the theory/procedure. How will it work, and how will it be implemented? This is an expanded version of the abstract without the details on the outcomes of the project.

Theory

Start with the top-level diagram of your machine (**do not use mine, make your own or edit the one I provided you**). Explain what the inputs and outputs to the machine are, **define them as variables.** Mention the high-level operation, theoretically, of the machine. Discuss the need for each of your modules. Be sure to point out the Moore FSM design (define your acronyms the first time, use them throughout).

Theory of each module

Go through and describe the theoretical operation of each module. What are the inputs? Outputs? Define these variables. In this section, you do not need to derive any equations. **You must have defined the encoder and encoded inputs in this section for your procedure to make sense.**

Procedure

Start with your state transition diagram and discussion of deriving your next state logic and output equations. You need a table for each of these (state transition table, output table). Write your next state logic equations (numbered) and describe them in text. Put the K-maps in Appendix A. Do the same for your output equations.

If you designed any other equations that are specific to this design, discuss it here. You can assume that the reader knows the equations for the encoder.

Results and Analysis

Discuss how you implemented the equations using SystemVerilog. Put your modules (in a `monospace font`) in Appendix B. Make sure these are commented and well formatted (single space, indented properly).

Discuss how you mapped all of your inputs and outputs to the DE10-Lite board. Put a table with inputs, and a table with outputs. **Do not screencap Mr. Galipeau's table.**

Go over a testing procedure ("results") and describe the operation working on your DE-10 Lite board.

Conclusions

This should be ~2 paragraphs going over the general concluding remarks (paragraph 1) talking about what you did and what the reader learned [main takeaways]. Add a second paragraph talking about what **you learned, mistakes you made, and improvements you would make next time.**

Example equation (do not copy this into your report….):

Let $S_{2:0}$ be the current state, $X_{1:0}$ be the encoded input (description in Table 3), and $S^*_{2:0}$ be the next-state inputs to the D-Flip-Flop state memory. Using the K-maps in Appendix A, the next state logic equations were derived in (1) – (3).

$$S_2^* = S_1 S_0' X_1 + \cdots \quad (1)$$

References

If needed, follow IEEE format.

Appendix A: K-Maps

Appendix B: SystemVerilog Modules

B.1 Top-Level Module

…