Signal Definition for MCPU

IorD	**Memory Access for Instruction or Data**
0	Instruction
1	Data

MemRead	**Memory Read Access Enable**
0	No Memory Read Access
1	Memory Read Access

MemWrite	**Memory Write Access Enable**
0	No Memory Write
1	Memory Write Enable

DatWidth	**Data Width for Memory Access**
000	32-bit Word
010	16-bit Halfword
011	8-bit Byte
110	16-bit Halfword /w Sign Ext
111	8-bit Byte /w Sign Ext

IRwrite	**Instruction Register Write Enable**
0	No Instruction Register Write
1	Instruction Register Write Enable

RegDst	**Selection for Destination Register**
00	Write to $rt
01	Write to $rd
10	Write to $rs
11	Write to $31

RegDatSel	**To Select Data Source for Register Write**
000	Write ALUOut to Register file
001	Write MDR to Register file
010	Write LO to Register file
011	Write HI to Register file
100	Write PC to Register file

RegWrite	**Write Enable to Register File**
0	Do not write to Register file
1	Write to Register file

EXTmode	**Immediate Data Extension Mode**
0	Zero Extension
1	Sign Extension

ALUsrcA	**ALU Input A Source Selection**
000	Register A to ALU input A
001	0x4
010	0x0
011	PC to ALU input A
100	MDR to ALU input A

ALUsrcB	**ALU Input B Source Selection**
000	Register B to ALU input B
001	0x4
010	0x0
011	SEU output to ALU input B
100	SEU output << 2

ALUop	**ALU Operation Code**		
00000	Bitwise AND	01001	a × b
00001	Bitwise OR	01010	Unsigned a × b
00010	Bitwise NOR	01011	a / b
00011	Bitwise XOR	01100	Unsigned a / b
00100	a + b	01101	b << a
00101	Unsigned a + b	01110	b >> a
00110	a – b	01111	b >>> a
00111	Unsigned a – b	10000	Set Less Than
01000	Zero	10001	Unsigned SLT
10010	HI = a	10011	LO = a

ALUctrl[1:0]	**Extra ALU Control Signal**
ALUctrl[0]=0	Shift = Shift Amount
ALUctrl[0]=1	Shift = $rs
ALUctrl[1]=0	Normal ALU input (a,b)
ALUctrl[1]=1	Exchanged ALU input (b,a)

Branch	**Branch Options**
000	No branch condition or Jump
001	Reserved
010	Branch if not negative
011	Branch if negative
100	Branch if equal
101	Branch if not equal
110	Branch if not positive
111	Branch if positive

PCsrc	PC Data Source Selection
00	From ALU output
01	From ALUOut Register
10	From Jump Address
11	From Current PC

PCwrite	PC Register Write Enable
0	No PC Register Write
1	PC Register Write Enable

StateSel	Next State Selection Signal
00	Next State = 0
01	Next State = State Indicated by Instruction
10	Reserved
11	Next State = Current State + 1

*** 8 bits before StateSel signal are reserved. They should be set xxxxxxxx.**