

# CALIFORNIA POLYTECHNIC STATE UNIVERSITY

CENG - DEPARTMENT OF ELECTRICAL ENGINEERING

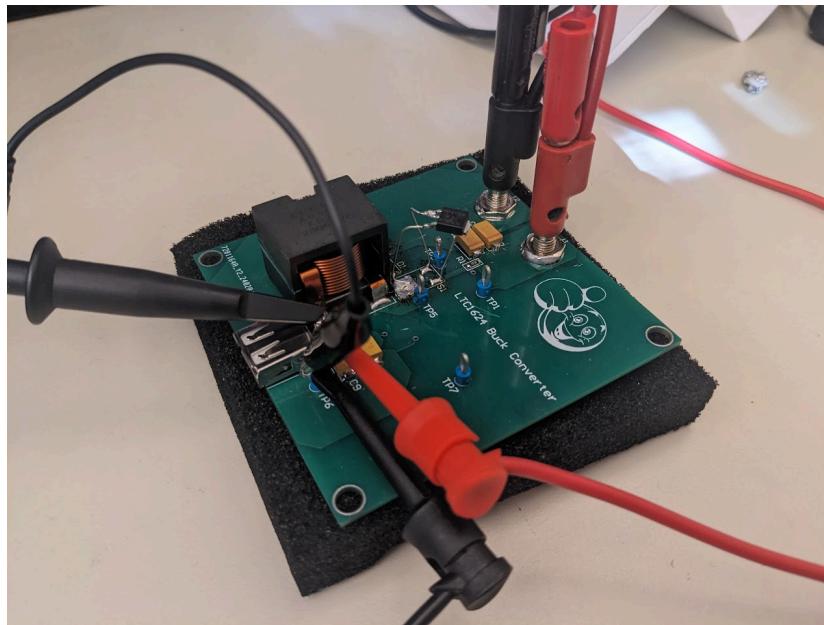


**EE 411-01: Power Electronics II**

*Winter Quarter 2024*

## Hardware Project: Solar-Powered Phone Charger

[Project Github Link](#)



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March 12th, 2024

## Design Equations

### Solar panel

$$P_{\text{PEAK}} = 20 \text{ W} \quad V_{\text{OC}} = 21.7 \text{ V} \quad V_{\text{SC}} = 1.25 \text{ A}$$


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### Buck Converter Requirements

$$V_{\text{NOM-INPUT}} = 15 \text{ V} \quad V_{\text{MAX-INPUT}} = 22 \text{ V} \quad V_{\text{NOM-OUTPUT}} = 5 \text{ V} \quad P_{\text{OUT-MAX}} = 10 \text{ W} \quad \text{Full load} = 2 \text{ A} = I_{\text{OUT-MAX}}$$

$$V_{\text{PP-RIPPLE}} < 5\% \text{ @ full load} \quad \text{Efficiency @ full load} \geq 80\%$$

Load regulation at  $V_{\text{NOM-INPUT}}$  with 10% to 90% load  $\leq 3\%$

Line regulation at full load with  $V_{\text{INPUT}}$  changed from 12 V to 8 V  $\leq 1\%$

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### Calculations of Power Stage Components using LTC1624

$$R_{\text{SENSE}} = \frac{100mV}{I_{\text{MAX}}} \Rightarrow \frac{100mV}{2 \text{ A}} = 0.05 \Omega$$

**Choose  $R_{\text{SENSE}}$ : 0.05ohm 0.5% tolerance 0.5 Watts**

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$$\Delta I_L = \frac{V_{\text{IN}} - V_{\text{OUT}}}{f * L} * \frac{V_{\text{OUT}} + V_D}{V_{\text{IN}} + V_D} \quad \text{where } V_D \text{ is the output Schottky diode forward drop}$$

NOTE: Maximum  $\Delta I_L$  occurs at  $V_{\text{MAX-INPUT}}$

According to the datasheet design equations  $\Delta I_L = 0.4(I_{\text{MAX}})$  is a good starting point

The last part of the equation needed for ripple current is  $V_D$ . Which requires consideration of losses from the diode.

Keeping Schottky diode loss as low as possible will require keeping  $V_D$  at a minimum.

**Choose Schottky Diode: Rated for 5A and at least 22V**

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Schottky loss equation as described in "Efficiency Consideration" section:

$$P_{\text{D-LOSS}} = V_D * (1 - D) * I_{\text{LOAD}} = 315 \text{ mV} * [1 - (\frac{5 + 315 \text{ mV}}{15 + 315 \text{ mV}})] \Rightarrow V_D = 350 \text{ mV}$$

Ripple current can now be calculated using  $V_D = 350 \text{ mV}$

$$\Delta I_L = \frac{V_{\text{IN}} - V_{\text{OUT}}}{f * L} * \frac{V_{\text{OUT}} + V_D}{V_{\text{IN}} + V_D} = 0.4 * 2 \text{ A} = \frac{22 \text{ V} - 5 \text{ V}}{200 \text{ kHz} * L} * \frac{5 \text{ V} + 315 \text{ mV}}{22 \text{ V} + 315 \text{ mV}} \quad \text{Using } V_{\text{IN}} = 22 \text{ V}$$

$L = 25.3 \mu H$

From the datasheet: "High efficiency converters generally cannot afford the core loss found in low cost powdered iron cores, forcing the use of more expensive ferrite, molypermalloy or Kool Mu® cores"

### Choose Inductor: At least 25.3 uH rated at 2.8 A

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$$\text{Main Switch Duty Cycle} = \frac{V_{OUT} + VD}{VIN + VD} = \frac{V_{OUTNOM} + 350 \text{ mV}}{VINNOM + 350 \text{ mV}}$$

$I_D$  rated for  $I_L * D_{NOM} = 2 * \frac{1}{3} = 0.67 \text{ A}$  minimum

$V_{DS}$  rated for  $V_{IN-MAX} = 22 \text{ V}$  minimum

$R_{DS(ON)}$  = make is small       $C_{RSS}$  = make is small

### Choose Switch: 0.67 A $I_D$ minimum and $V_{DS} = 22 \text{ V}$ minimum

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$C_{OUT}$  calculated based on worst case output voltage ripply

$C_{OUT}$  ESR <  $2 * R_{SENSE} = 0.05 \text{ ohm}$

$C_{OUT}$  ESR <  $10\text{mOhm} \Rightarrow$  worst case allowable ESR

For  $\Delta I_L = 0.4 * I_{MAX} = 0.8 \text{ A}$        $f = 200\text{kHz}$        $V_{PP-RIPPLE} = \Delta V_{OUT} = 22\text{V} * 0.05 = 1.1 \text{ V}$  worst case

Then,

$$\Delta V_{OUT} = \Delta I_L (ESR + \frac{1}{4*f*COUT}) \Rightarrow 1.1 = 0.8(10m\Omega + \frac{1}{4*200\text{kHz}*COUT})$$

Gives,  $C_{OUT}$  must be greater than  $915.75 \text{ nF}$  with an ESR of  $10 \text{ mOhm}$  or better

### Choose $C_{OUT}$ greater than $1\mu F$ with ESR of $10\text{mOhm}$ or better

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"The value of the boost capacitor CB needs to be 50 times greater than the total input capacitance of the topside MOSFET. In most applications  $0.1\mu F$  is adequate."

If using a MOSFET with  $1100\text{pF}$ , then

$$C_B > C_{IN} * 50 \Rightarrow C_B > 55.5 \text{ nF}$$

### Choose Boost Capacitor to be $0.1 \text{ uF}$ 5% tolerance (based on reference guide recommendations)

## Simulation Results

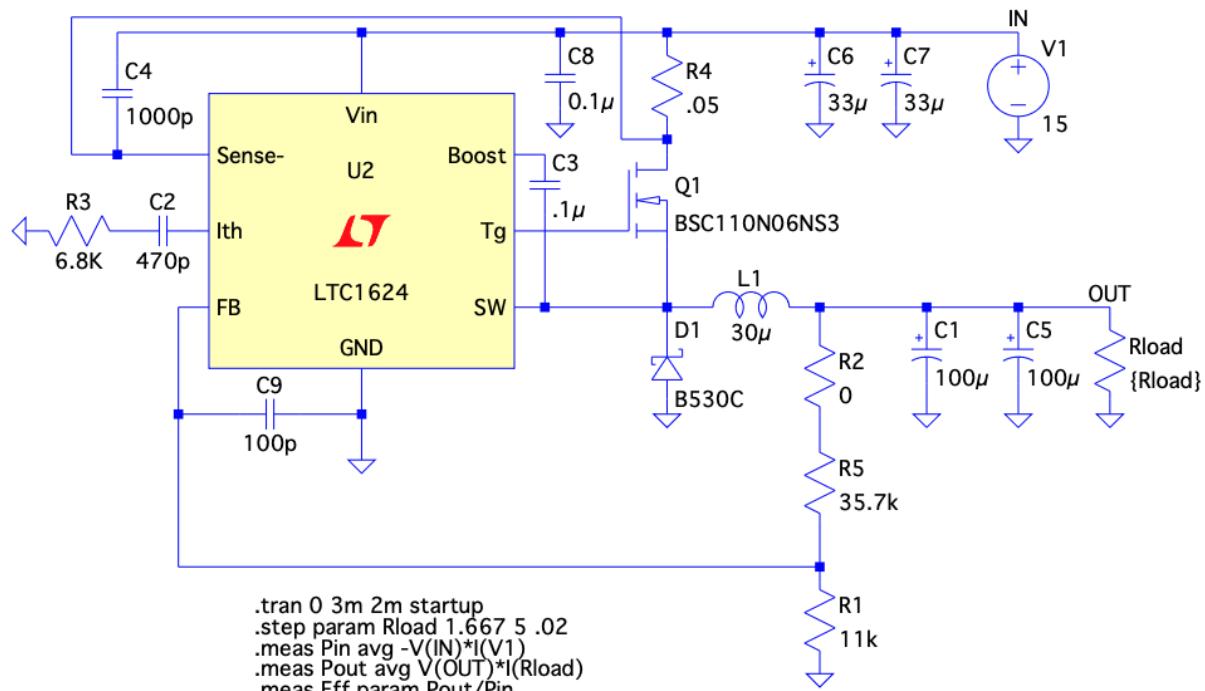


Figure 1: LTspice schematic

2) Nominal Input Voltage is 15 V, but must be able to handle maximum input voltage of 22 V, tested at Full Load

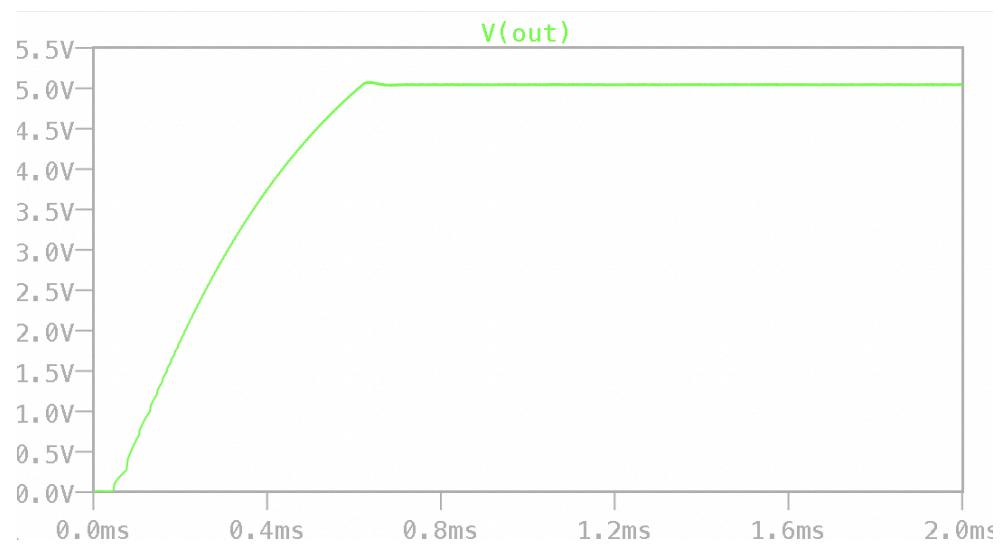


Figure 2: Simulated  $V_{out}$  at full load with  $V_{in} = 22V$

4) Peak to peak output voltage ripple at full load must be < 5%

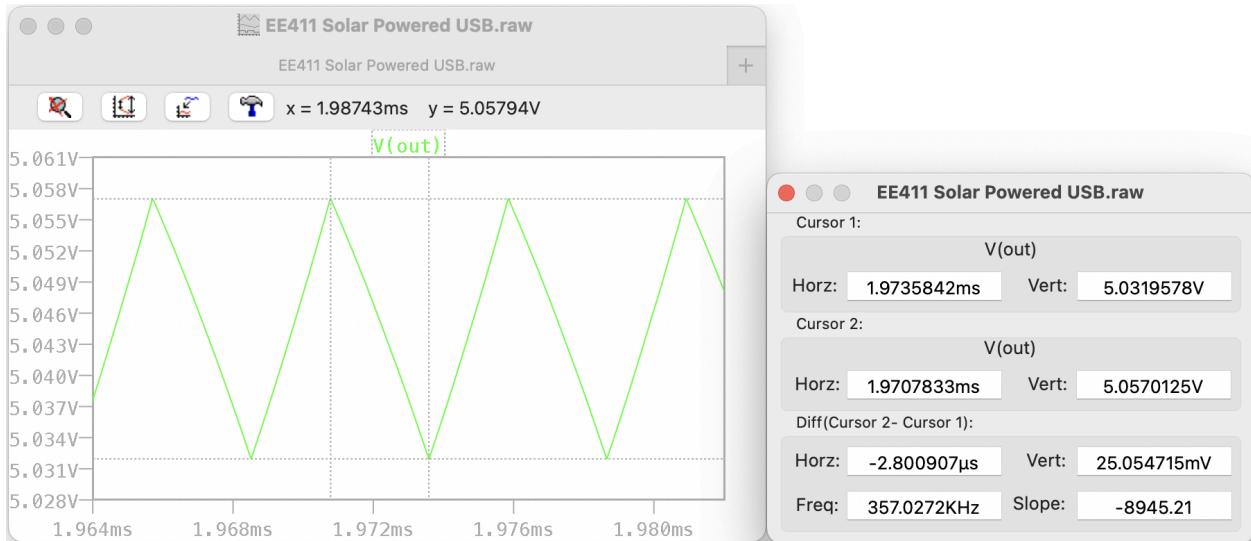


Figure 3: Simulated  $V_{out}$  voltage ripple

$$\Delta V_{ripple} = 25.05 \approx 25 \text{ mV} \quad \bar{V}_o = 5.044 \approx 5 \text{ V}$$

$$\%V_{ripple} = \frac{\Delta V_{ripple}}{\bar{V}_o} * 100\% = \frac{0.025}{5} * 100\% = 0.5\%$$

5) Efficiency at full load  $\geq 80\%$  (measured at nominal input voltage)

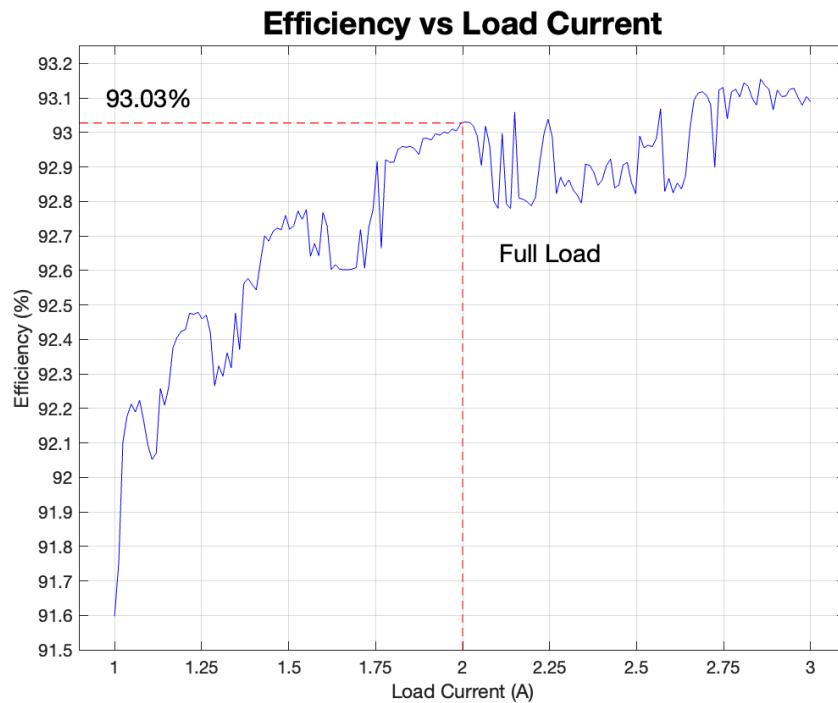


Figure 4: Matlab Plot of Efficiency Curve

Matlab data was taken from .meas command in the ltspice .log file with the following netlist

```
* ./Users/coreyzaas/Documents/LTspice/EE411 Solar Powered USB.asc
L1 N007 OUT 30u Rser=0.0036
M$Q1 N001 N005 N007 N007 BSC110N06NS3
V1 IN 0 15
C1 OUT 0 100u Rser=0.1
C2 N003 N004 470p
R1 N006 0 11k
R3 0 N003 6.8k
D1 0 N007 B530C
C3 N002 N007 .1u
C4 IN N001 1000p
XU2 N001 N004 N006 0 N007 N005 N002 IN LTC1624
R4 IN N001 .05
Rload OUT 0 {Rload}
R5 OUT N006 35.7k
C5 OUT 0 100u Rser=0.1
C6 IN 0 33u Rser=0.1
C7 IN 0 33u Rser=0.1
C8 IN 0 0.1u
C9 0 N006 100p
.model D D
.lib /Users/coreyzaas/Library/Application Support/LTspice/lib/cmp/standard.dio
.model NMOS NMOS
.model PMOS PMOS
.lib /Users/coreyzaas/Library/Application Support/LTspice/lib/cmp/standard.mos
.tran 0 3m 2m startup
.step param Rload 1.667 5 .02
.meas Pin avg -{V(IN)}*({V1})
.meas Pout avg V(OUT)*I(Rload)
.meas Eff param Pout/Pin
.lib LTC1624.sub
.backanno
.end
```

6) Load regulation at nominal input with 10% to 90% load  $\leq 3\%$

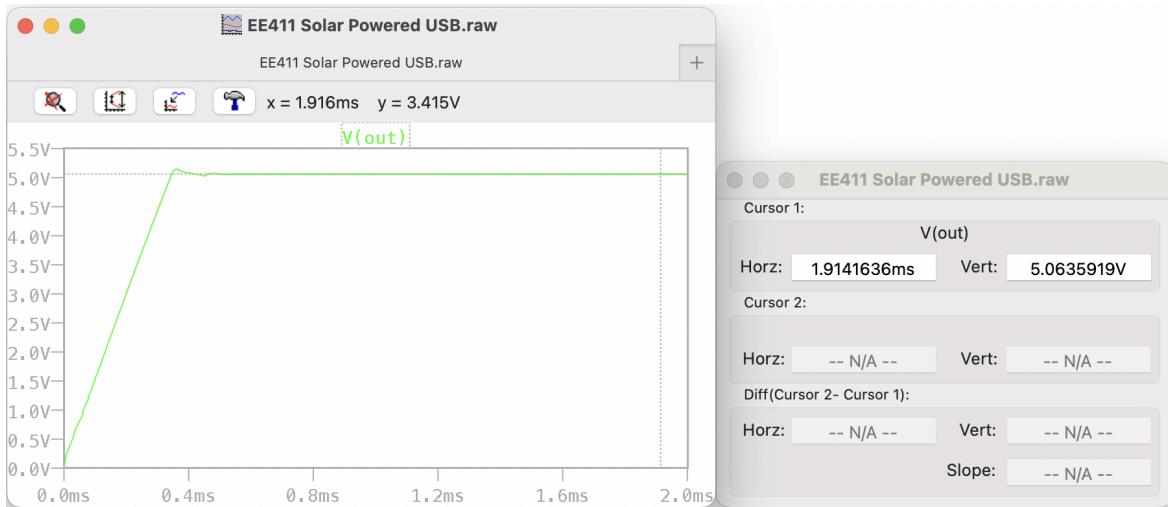


Figure 5: Simulated  $V_{out}$  at Low Load (10% load)

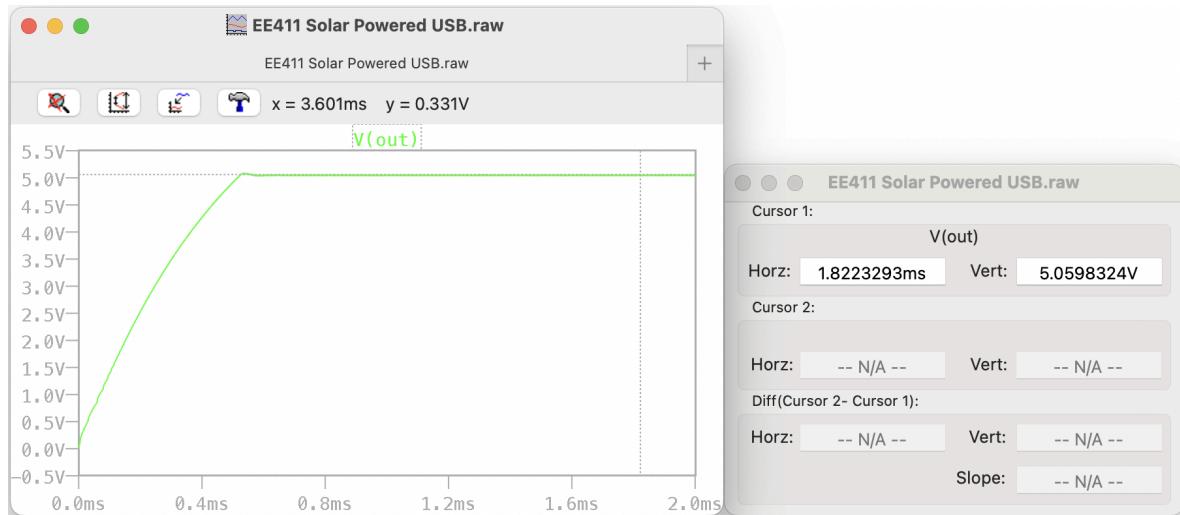


Figure 6: Simulated Vout at high load (90% load)

$$\text{Load Regulation}_{\frac{\text{Nominal Input}}{\text{Nominal Input}}} = \frac{\bar{V}_{\text{out}(\text{low-load})} - \bar{V}_{\text{out}(\text{high-load})}}{\bar{V}_{\text{out}(\text{high-load})}} * 100\%$$

$$\text{Load Regulation}_{\frac{\text{Nominal Input}}{\text{Nominal Input}}} = \frac{5.0635919 - 5.0598324}{5.0598324} * 100\%$$

$$\text{Load Regulation}_{\frac{\text{Nominal Input}}{\text{Nominal Input}}} = 0.074\%$$

7) Line regulation at full load with input changed from 12 V to 18 V  $\leq 1\%$

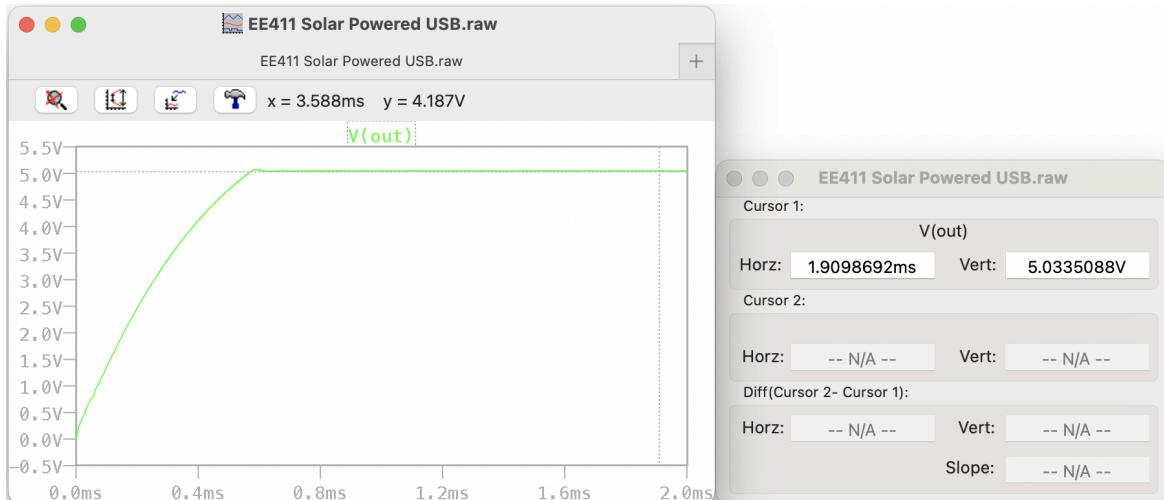


Figure 7: Simulated Vout with Vin at 12V

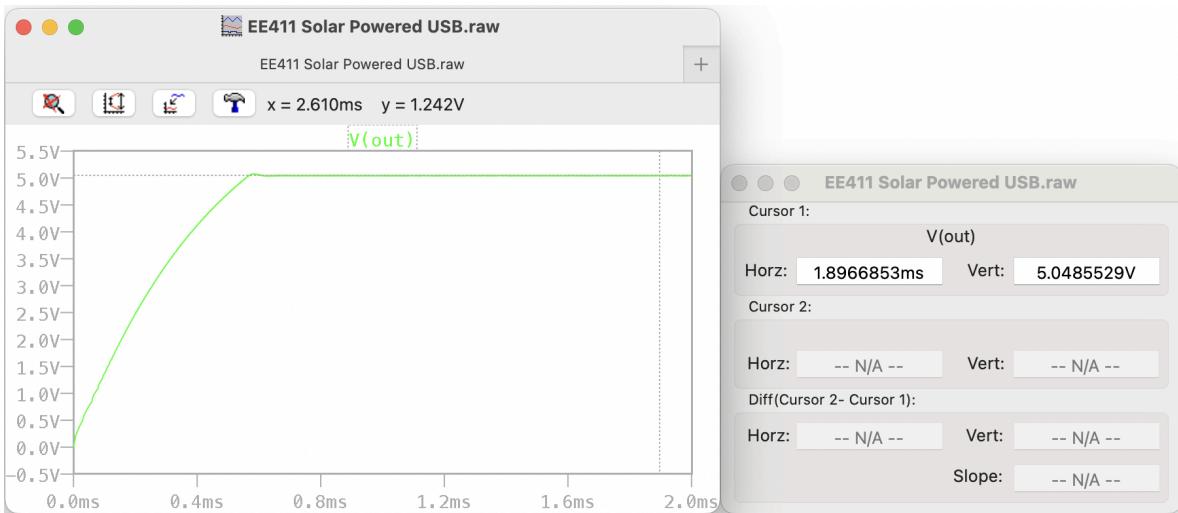


Figure 8: Simulated Vout with Vin at 15V

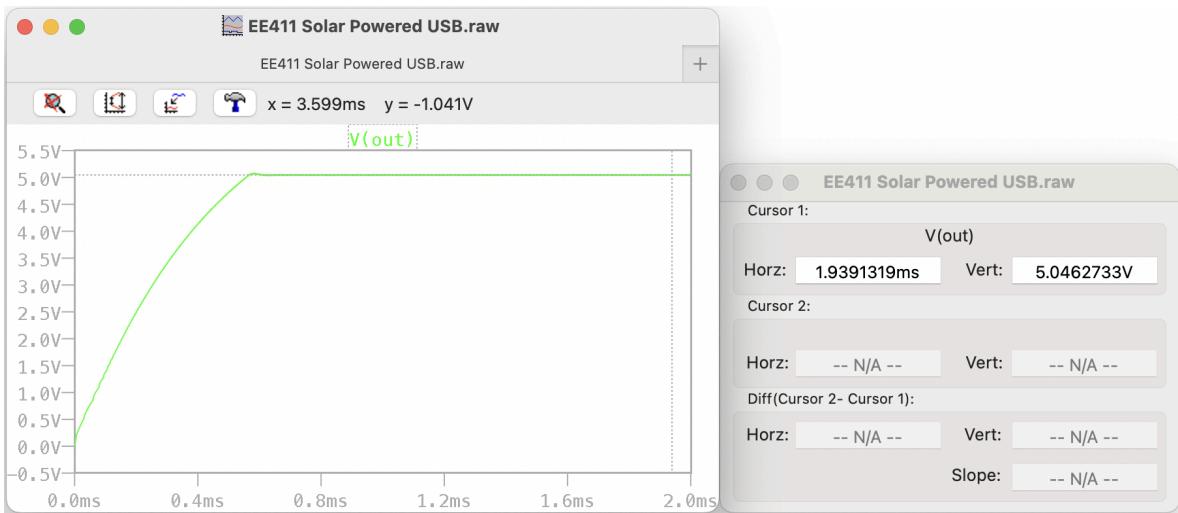


Figure 9: Simulated Vout with Vin at 18V

$$\text{Line Regulation}_{\text{Full Load}} = \frac{\bar{V}_{\text{out}(\text{high-input})} - \bar{V}_{\text{out}(\text{low-input})}}{\bar{V}_{\text{out}(\text{nominal-input})}} * 100\%$$

$$\text{Line Regulation}_{\text{Full Load}} = \frac{5.0462733 - 5.0335088}{5.0485529} * 100\%$$

$$\text{Line Regulation}_{\text{Full Load}} = 0.253\%$$

## Hardware Prototype & Test Results

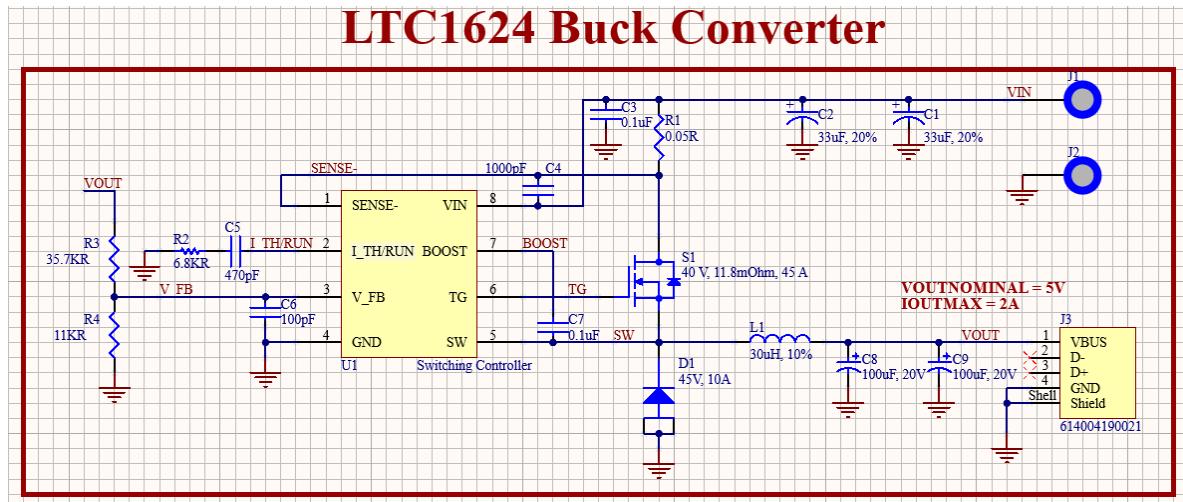


Figure 10: Final Circuit Schematic

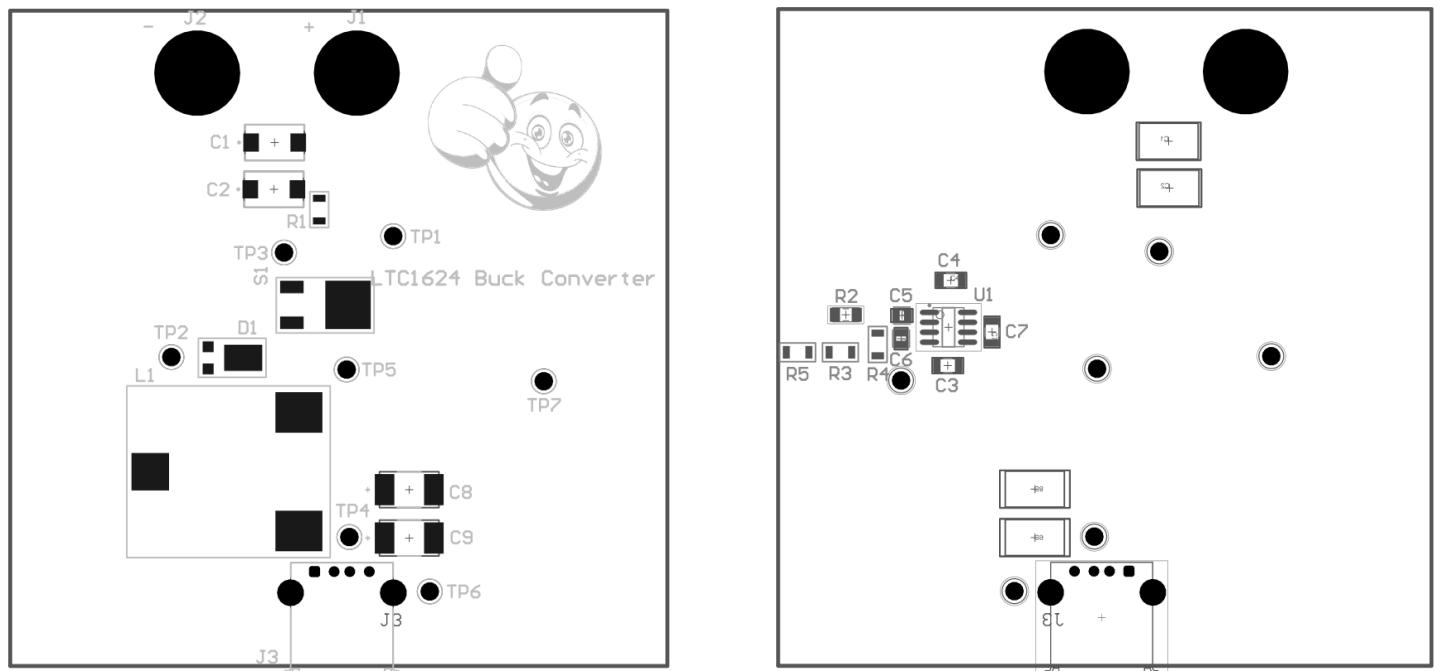


Figure 11: Final PCB. Power Flow Side(left), Controller Side(Right)

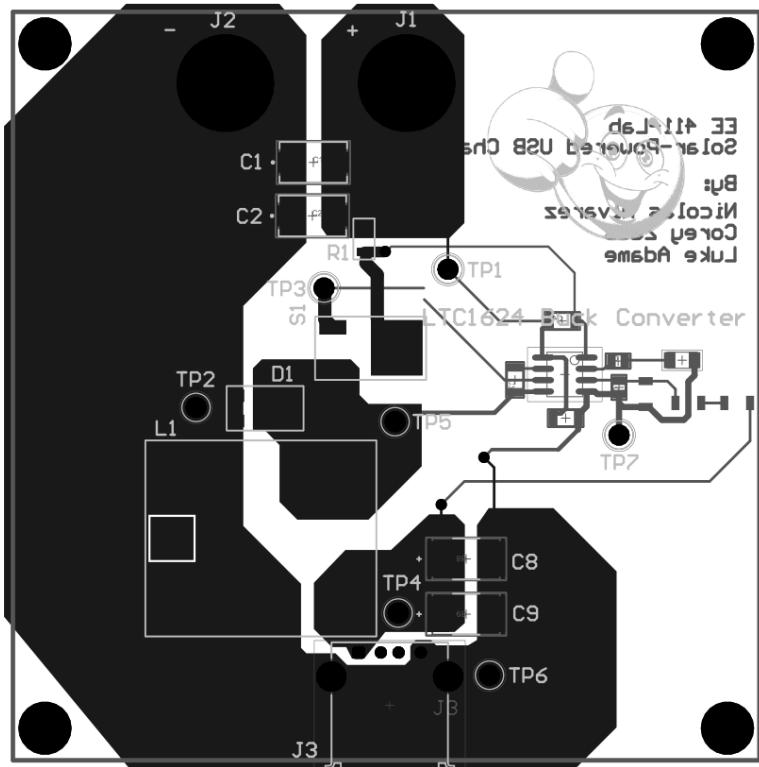


Figure 12: Final PCB Design

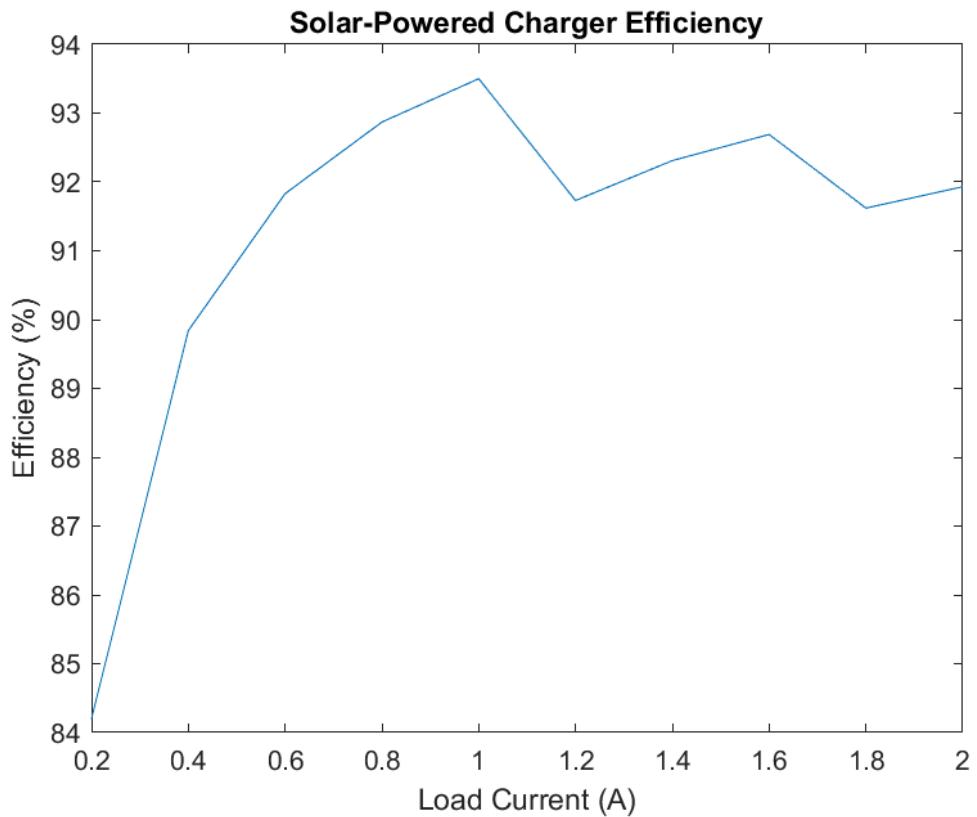


Figure 13: Hardware Efficiency Curve



Figure 14: Vout Voltage Ripple at Full Load

Table 1: Hardware and Simulated Results

	Efficiency - 2A; 15V	Load Regulation	Line Regulation
Hardware	91.93%	0.36%	0.06%
Simulated	93.03%	0.25%	0.074%



Figure 15: Hardware Prototype. Power Flow Side(left), Controller Side(Right)

## Bill of Materials

#	QUANTITY	PART NUMBER	MANUFACTURER PART NUMBER	DESCRIPTION	CUSTOMER REFERENCE	UNIT PRICE	EXTENDED PRICE
1	10	399-C1206C10 4J5RAC7800CT-ND	C1206C104J5RAC7800	CAP CER 0.1UF 50V X7R 1206	OTHER DECOUPLING CAPS	0.166	1.66
2	10	399-C0805C47 1J5GAC7210CT-ND	C0805C471J5GA C7210	CAP CER 470PF 50V COG/NPO 0805	COMPENSATION CAP	0.076	0.76
3	10	399-C0805C10 1K5GAC7210CT-ND	C0805C101K5GA C7210	CAP CER 100PF 50V COG/NPO 0805	IC DECOUPLING	0.059	0.59
4	3	31-SDT10A45P 5-13DCT-ND	SDT10A45P5-13D	DIODE SCHOTTKY 45V 10A POWERDI5	Schottky	0.51	1.53
5	3	495-B82559A0 303A024CT-ND	B82559A0303A0 24	FIXED IND 30UH 22.9A 3.6MOHM SMD	Inductor	8.34	25.02
6	4	273-KDV12DR0 50ETCT-ND	KDV12DR050ET	RES 0.05 OHM 0.5% 1/2W 1206	RSENSE	0.46	1.84
7	3	P18836CT-ND	ERA-8ARW3572V	RES SMD 35.7KOHM 0.05% 1/4W 1206	FEEDBACK	1.53	4.59
8	4	NVD5C478NLT 4GOSCT-ND	NVD5C478NLT4G	MOSFET N-CH 40V 14A/45A DPAK	SWITCH	1.65	6.60
9	22	36-5287-ND	5287	TEST POINT (BLUE) - MULTIPURPOSE	TP	0.281	6.18
10	10	399-8384-1-ND	T491D336M025AT	CAP TANT 33UF 20% 25V 2917	INPUT CAPS	0.983	9.83
11	10	399-17909-1-N D	C1206C102K1GE CAUTO	CAP CER 1206 1NF 100V COG 10%	IC CAPS	0.165	1.65
12	10	478-1724-1-ND	TAJD107K020RNJ	CAP TANT 100UF 10% 20V 2917	OUTPUT CAPS	0.844	8.44
13	10	P11.0KFCT-ND	ERJ-8ENF1102V	RES SMD 11K OHM 1% 1/4W 1206	FEEDBACK	0.091	0.91
14	3	P6.8KBCCT-ND	ERA-8AEB682V	RES SMD 6.8K OHM 0.1% 1/4W 1206	RCOMPENSATION	0.37	1.11