Digital Electronics
CSE 223

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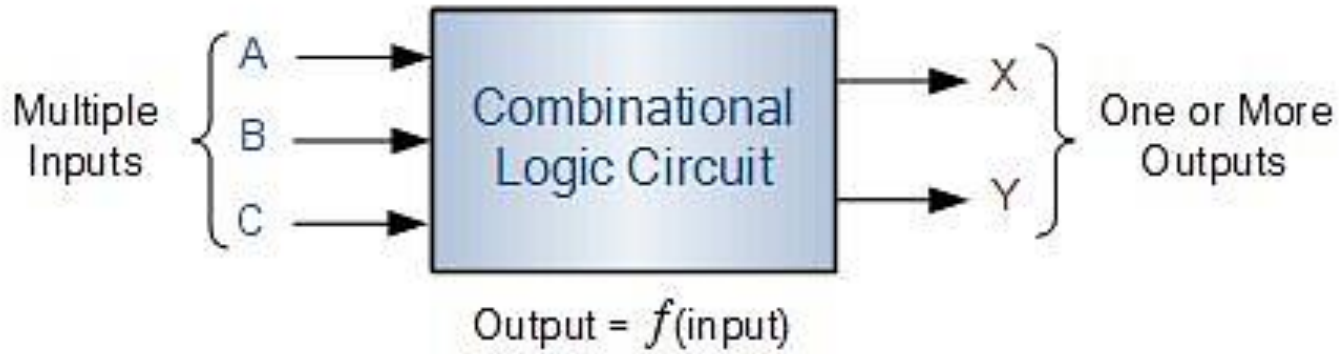
Table of contents

Chapter 4: Combinational Logic

Combinational Logic

- A combinational circuit consists of logic gates whose outputs at any time are determined from only the **present combination of inputs**. A combinational circuit performs an operation that can be specified logically by a set of Boolean functions.
- A combinational circuit consists of an **interconnection of logic gates.** Combinational logic gates react to the values of the signals at their inputs and produce the value of the output signal, transforming binary information from the given input data to a required output data.

Combinational Logic



Adder

- ✓ Digital computers perform a variety of information-processing tasks.
- ✓ Among the functions encountered are the various arithmetic operations.
- ✓ The most basic arithmetic operation is the addition of two binary digits.
- ✓ This simple addition consists of four possible elementary operations: 0 + 0 = 0, 0 + 1 = 1, 1 + 0 = 1, and 1 + 1 = 10. The first three operations produce a sum of one digit, but when both augend and addend bits are equal to 1, the **binary sum** consists of two digits. The higher significant bit of this result is called a **carry** .

Half Adder

- A combinational circuit that performs the **addition of two bits** is called a half adder.
- That means circuit needs **two binary inputs** and two binary outputs.
- The input variables designate the augend and addend bits; the output variables produce the **sum and carry**.

Half Adder

Half Adder

x	y	C	S
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

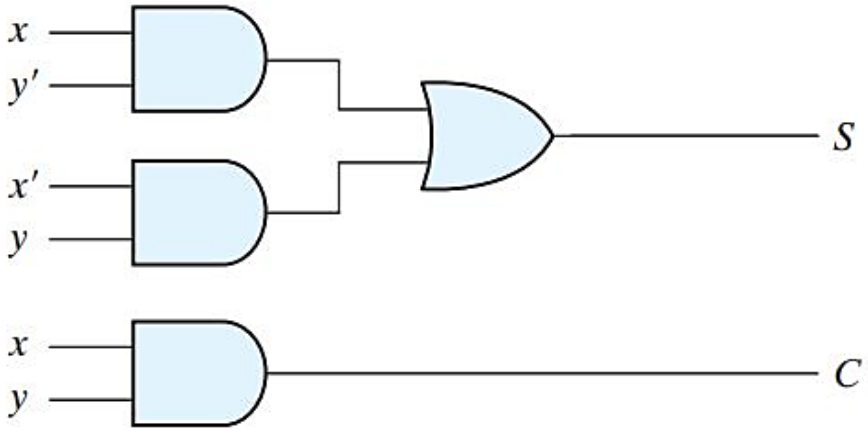
$$S = x'y + xy'$$

$$C = xy$$

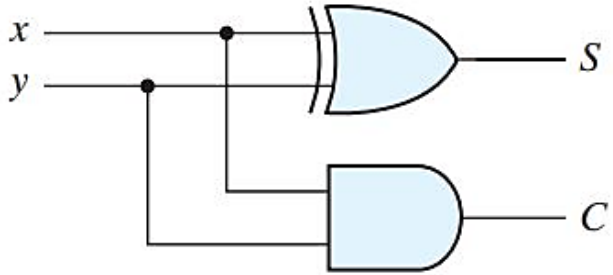
Half Adder

$$S = x'y + xy'$$

$$C = xy$$



(a) $S = xy' + x'y$
$C = xy$



(b) $S = x \oplus y$
$C = xy$

Full Adder

- A full adder is a combinational circuit that forms the arithmetic sum of three bits.
- It consists of three inputs and two outputs.
- Two of the input variables, denoted by x and y , represent the two significant bits to be added. The third input, z , represents the carry from the previous lower significant position.

Full Adder

Full Adder

x	y	z	C	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

$$S = x'y'z + x'yz' + xy'z' + xyz$$

$$C = xy + xz + yz$$

Full Adder

$$S = x'y'z + x'yz' + xy'z' + xyz$$
$$C = xy + xz + yz$$

$$\begin{aligned} S &= z \oplus (x \oplus y) \\ &= z'(xy' + x'y) + z(xy' + x'y)' \\ &= z'(xy' + x'y) + z(xy + x'y') \\ &= xy'z' + x'yz' + xyz + x'y'z \end{aligned}$$

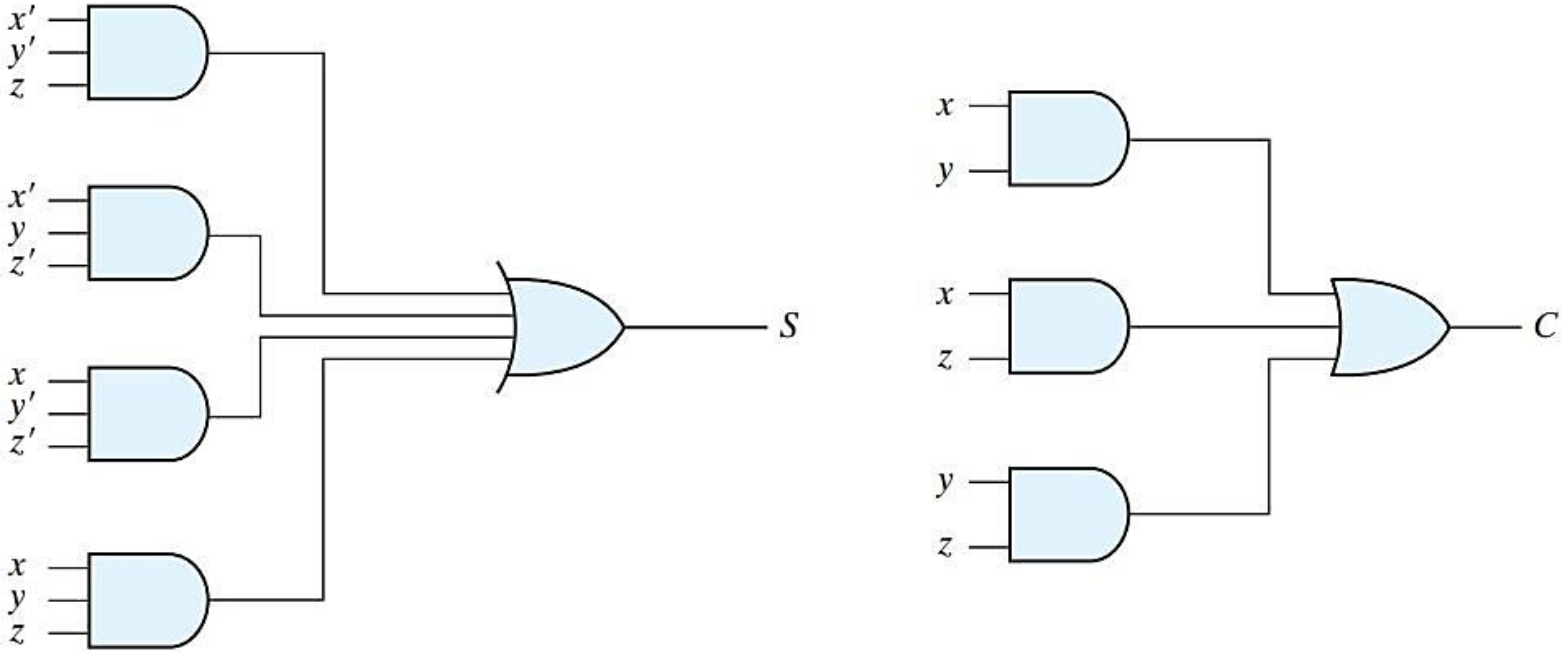
The carry output is

$$C = z(xy' + x'y) + xy = xy'z + x'yz + xy$$

Full Adder

$$S = x'y'z + x'yz' + xy'z' + xyz$$

$$C = xy + xz + yz$$



** Implementation of full adder with two half adders and an OR gate